

Description

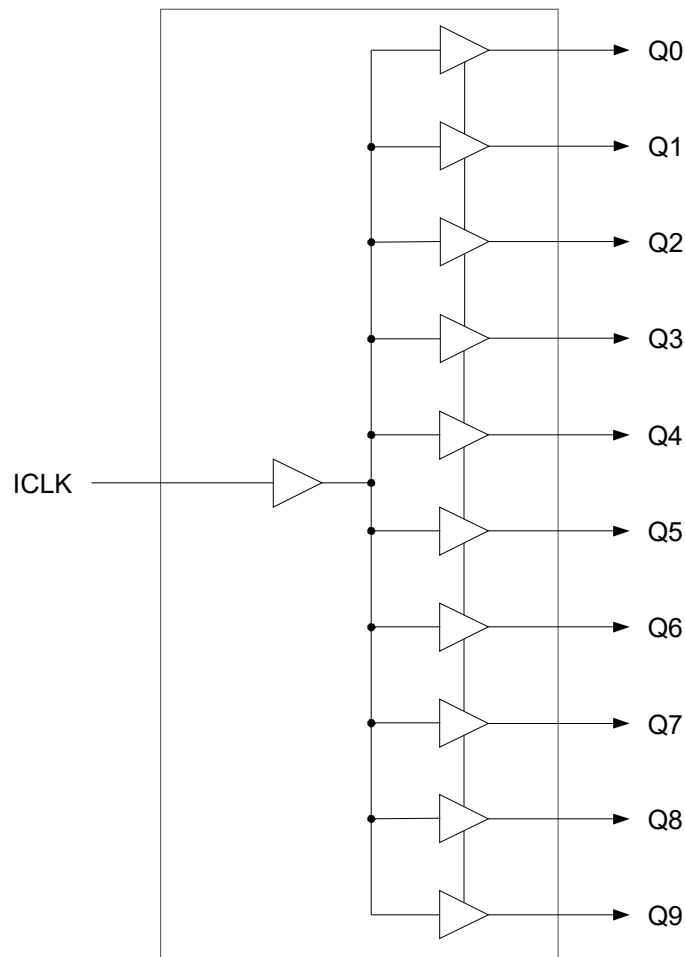
The 74FCT3807S is a low skew, single input to ten output, clock buffer. The 74FCT3807S has best in class additive phase Jitter of sub 50 fsec.

Renesas makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact us for all of your clocking needs.

Features

- Low additive phase jitter RMS: 50fs
- Low skew outputs (50ps)
- Packaged in 20-pin TSSOP, SSOP, QSOP, and VFQFPN packages, Pb (lead) free
- Operating voltages of 1.8V to 3.3V
- Input/Output clock frequency up to 200 MHz
- Advanced, low power CMOS process
- Extended temperature range (-40°C to +105°C)

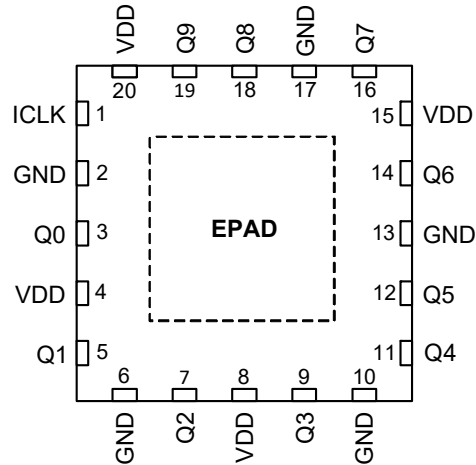
Block Diagram



Pin Assignments

ICLK	1	20	VDD
GND	2	19	Q9
Q0	3	18	Q8
VDD	4	17	GND
Q1	5	16	Q7
GND	6	15	VDD
Q2	7	14	Q6
VDD	8	13	GND
Q3	9	12	Q5
GND	10	11	Q4

20-pin TSSOP/SSOP/QSOP



20-pin VFQFPN

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	ICLK	Input	Clock input.
2	GND	Power	Connect to ground.
3	Q0	Output	Clock output 0.
4	VDD	Power	Connect to +1.8V, +2.5 V, or +3.3 V.
5	Q1	Output	Clock output 1.
6	GND	Power	Connect to ground.
7	Q2	Output	Clock Output 2.
8	VDD	Power	Connect to +1.8V, +2.5 V, or +3.3 V.
9	Q3	Output	Clock Output 3.
10	GND	Power	Connect to ground.
11	Q4	Output	Clock Output 4.
12	Q5	Output	Clock Output 5.
13	GND	Power	Connect to ground.
14	Q6	Output	Clock Output 6.
15	VDD	Power	Connect to +1.8V, +2.5 V, or +3.3 V.
16	Q7	Output	Clock Output 7.
17	GND	Power	Connect to ground.
18	Q8	Output	Clock Output 8.
19	Q9	Output	Clock Output 9.
20	VDD	Power	Connect to +1.8V, +2.5 V, or +3.3 V.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 μ F should be connected between VDD pins and GND pins, as close to the device as possible. A 33 Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skew that the 74FCT3807S is capable of, careful attention must be paid to board layout. Essentially, all ten outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30 Ω series termination on one output (with 33 Ω on the others) will cause at least 15 ps of skew.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 74FCT3807S. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	3.465V
Outputs	-0.5 V to VDD+0.5 V
ICLK	3.465V
Ambient Operating Temperature (extended)	-40° to +105°C
Storage Temperature	-65° to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (extended)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71		+3.465	V

DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD=1.8V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71		1.89	V
Input High Voltage, ICLK	V _{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, ICLK	V _{IL}	Note 1			0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -10 mA	1.3			V
Output Low Voltage	V _{OL}	I _{OL} = 10 mA			0.35	V
Operating Supply Current	IDD	No load, 135 MHz		35		mA
Nominal Output Impedance	Z _O			17		Ω
Input Capacitance	C _{IN}	ICLK		5		pF

Notes: 1. Nominal switching threshold is VDD/2

VDD=2.5 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, ICLK	V _{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, ICLK	V _{IL}	Note 1			0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -16 mA	1.8			V
Output Low Voltage	V _{OL}	I _{OL} = 16 mA			0.5	V
Operating Supply Current	IDD	No load, 135 MHz		45		mA
Nominal Output Impedance	Z _O			17		Ω
Input Capacitance	C _{IN}	ICLK		5		pF

VDD=3.3 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Input High Voltage, ICLK	V _{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, ICLK	V _{IL}	Note 1			0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -25 mA	2.2			V
Output Low Voltage	V _{OL}	I _{OL} = 25 mA			0.7	V
Operating Supply Current	IDD	No load, 135 MHz		55		mA
Nominal Output Impedance	Z _O			17		Ω
Input Capacitance	C _{IN}	ICLK		5		pF

AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.36 to 1.44 V, $C_L=5$ pF		1.4	1.9	ns
Output Fall Time	t_{OF}	1.44 to 0.36 V, $C_L=5$ pF		1.4	1.9	ns
Propagation Delay		Note 1	1.5	2.5	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		50	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms

VDD = 2.5 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.5 to 2.0 V, $C_L=5$ pF		1.0	1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.5 V, $C_L=5$ pF		1.0	1.5	ns
Propagation Delay		Note 1	1.8	2.5	4.5	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		50	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms

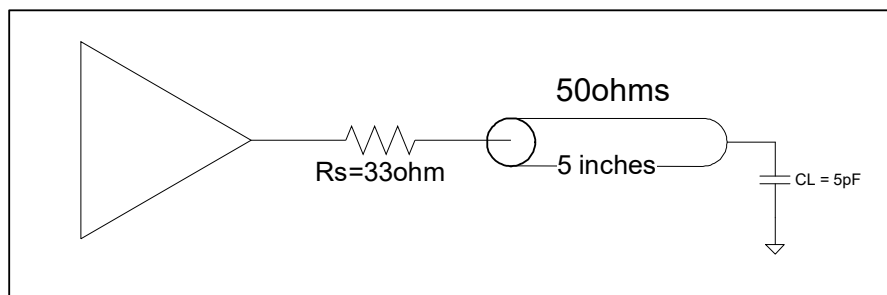
VDD = 3.3 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.66 to 2.64 V, $C_L=5$ pF		0.6	1.0	ns
Output Fall Time	t_{OF}	2.64 to 0.66 V, $C_L=5$ pF		0.6	1.0	ns
Propagation Delay		Note 1	1.5	2.5	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		50	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms

Notes:

1. With rail to rail input clock
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult Renesas for tight duty cycle clock generators.

Test Load and Circuit



Thermal Information

20VFQFPN

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		53.3		$^{\circ}\text{C/W}$
	θ_{JA}	1 m/s air flow		49.7		$^{\circ}\text{C/W}$
	θ_{JA}	2 m/s air flow		48		$^{\circ}\text{C/W}$
	θ_{JA}	3 m/s air flow		47.1		$^{\circ}\text{C/W}$
Thermal Resistance Junction to Board	θ_{JB}			5.1		$^{\circ}\text{C/W}$
Thermal Resistance Junction to Case	θ_{JC}			91.8		$^{\circ}\text{C/W}$

20TSSOP

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		91.9		$^{\circ}\text{C/W}$
	θ_{JA}	1 m/s air flow		89.2		$^{\circ}\text{C/W}$
	θ_{JA}	2 m/s air flow		86		$^{\circ}\text{C/W}$
	θ_{JA}	3 m/s air flow		83.8		$^{\circ}\text{C/W}$
Thermal Resistance Junction to Board	θ_{JB}			75.5		$^{\circ}\text{C/W}$
Thermal Resistance Junction to Case	θ_{JC}			34.7		$^{\circ}\text{C/W}$

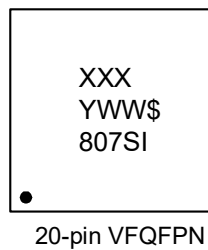
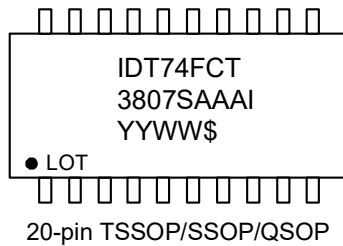
20QSOP

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		77.8		$^{\circ}\text{C/W}$
	θ_{JA}	1 m/s air flow		74.9		$^{\circ}\text{C/W}$
	θ_{JA}	2 m/s air flow		72.2		$^{\circ}\text{C/W}$
	θ_{JA}	3 m/s air flow		70.4		$^{\circ}\text{C/W}$
Thermal Resistance Junction to Board	θ_{JB}			63.1		$^{\circ}\text{C/W}$
Thermal Resistance Junction to Case	θ_{JC}			42.7		$^{\circ}\text{C/W}$

20SSOP

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		76.4		°C/W
	θ_{JA}	1 m/s air flow		73.1		°C/W
	θ_{JA}	2 m/s air flow		70.4		°C/W
	θ_{JA}	3 m/s air flow		68.5		°C/W
Thermal Resistance Junction to Board	θ_{JB}			59.7		°C/W
Thermal Resistance Junction to Case	θ_{JC}			46.4		°C/W

Marking Diagrams



Notes:

1. "LOT" denotes the lot number.
2. "XXX" denotes the lot number.
3. "YYWW" or "YWW" are the last digits of the year and week that the part was assembled.
4. "\$" denotes mark code.
5. "I" denotes extended temperature range device.
6. "AAA" denotes package code.

Package Outline Diagrams

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

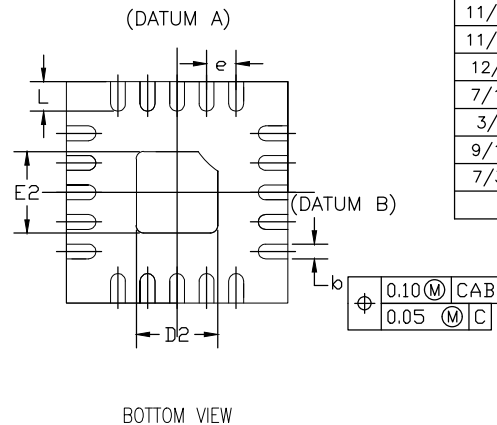
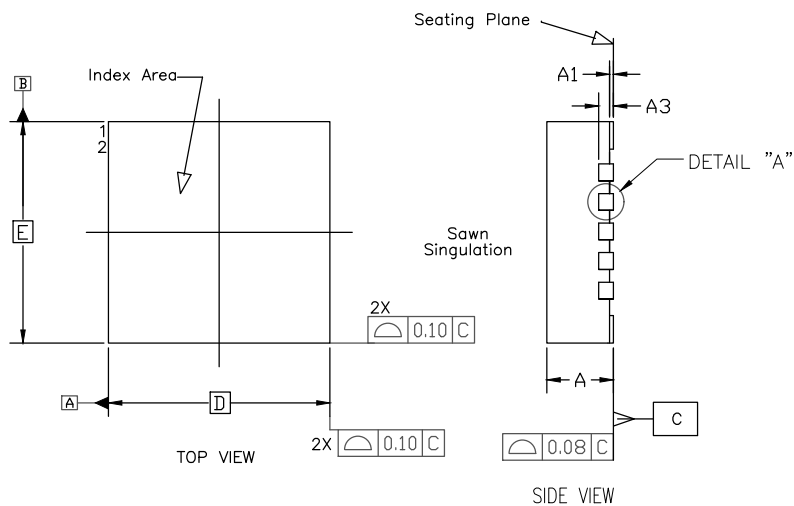
Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
74FCT3807SNDGI	see page 6	Tubes	20-pin VFQFPN	-40° to +105°C
74FCT3807SNDGI8		Tape and Reel	20-pin VFQFPN	-40° to +105°C
74FCT3807SPGGI		Tubes	20-pin TSSOP	-40° to +105°C
74FCT3807SPGGI8		Tape and Reel	20-pin TSSOP	-40° to +105°C
74FCT3807SQGI		Tubes	20-pin QSOP	-40° to +105°C
74FCT3807SQGI8		Tape and Reel	20-pin QSOP	-40° to +105°C
74FCT3807SPYGI		Tubes	20-pin SSOP	-40° to +105°C
74FCT3807SPYGI8		Tape and Reel	20-pin SSOP	-40° to +105°C

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Date	Description of
Jun 9, 2025	- Added Thermal Information for all package types. - Added package links to Ordering Information.
Mar 18, 2015	Initial release.



DETAIL A

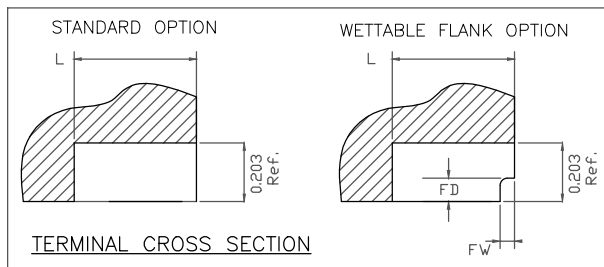


Table 1: Dimensions of wettable flank

Symbol	Unit (mm)	
	MIN	MAX
FD	0.100	—
FW	0.001	0.075

NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.05 mm.
3. WARPAGE SHALL NOT EXCEED 0.05 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. REFER JEDEC MO-220.

COMMON DIMENSION

DIMENSION			
Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	0.20 Ref		
b	0.17	0.20	0.25
e	0.40 BASIC		
N	20		
ND	5		
NE	5		
D	3.00 BASIC		
E	3.00 BASIC		
D2	SEE EPAD OPTION		
E2	SEE EPAD OPTION		
L	0.30	0.40	0.50

REVISIONS

DATE	REV	DESCRIPTION	AUTHOR
11/14/08	00	INITIAL RELEASE	RC
11/28/12	01	ADD EPAD OPTION	RC
12/5/13	02	COMBINE POD & LAND PATTERN	J.HUA
7/14/14	03	Change Dimension aaa	J.HUA
3/1/19	04	Add Wettable Flank Option	J.HUA
9/19/19	05	Add Wettable Flank S2	J.HUA
7/30/21	06	Update Dimensions of Wettable Flank	JHTAN

NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE

EPAD OPTION

Symbol	P1			P2		
	MIN	NOM	MAX	MIN	NOM	MAX
E2	0.95	1.10	1.25	1.55	1.65	1.75
D2	0.95	1.10	1.25	1.55	1.65	1.75

Symbol	S1 (FUSED LEAD)			S2		
	MIN	NOM	MAX	MIN	NOM	MAX
E2	1.55	1.65	1.75	1.55	1.65	1.75
D2	1.55	1.65	1.75	1.55	1.65	1.75
R	0.075	---	0.175	0.075	---	0.175
S	0.001	---	0.09	0.001	---	0.09

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± ±1°
XX±
XXX±

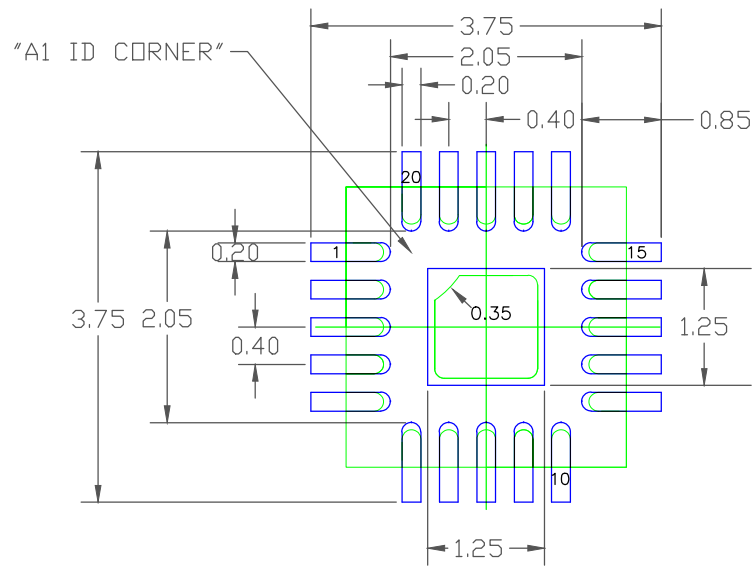
RENESAS

6024 Silver Creek Valley Road
San Jose CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

TITLE NDG20 Package Outline Drawing
3.0 x 3.0 mm Body 0.40mm Pitch
VFQFPN

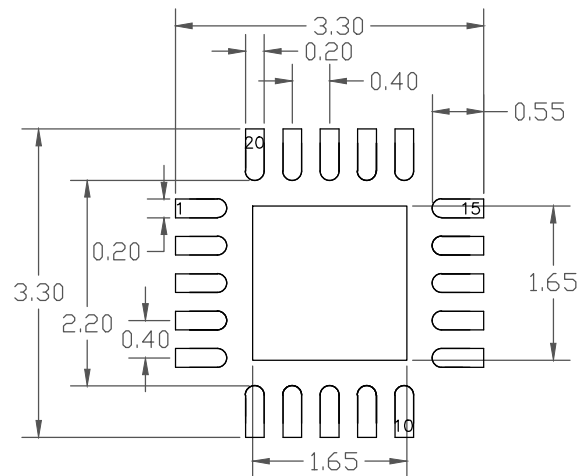
SIZE C DRAWING No. PSC-4179 REV 06

DO NOT SCALE DRAWING SHEET 1 OF 2

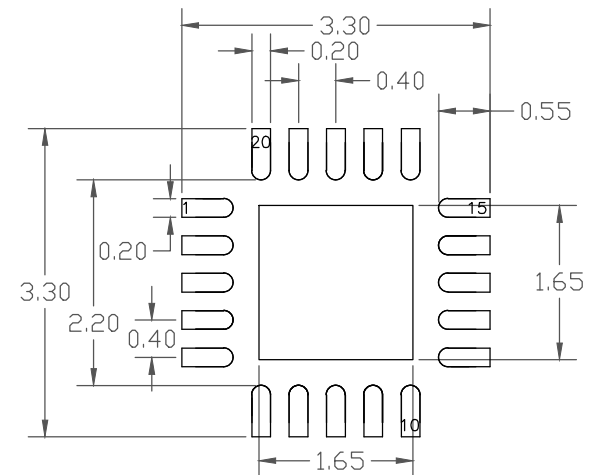


P1
EPAD 1.1 mm SQ

RECOMMENDED LAND PATTERN DIMENSION



P2 & S1
EPAD 1.65 mm SQ



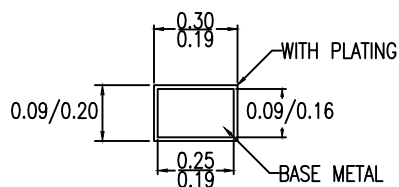
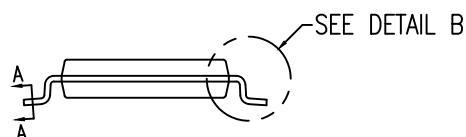
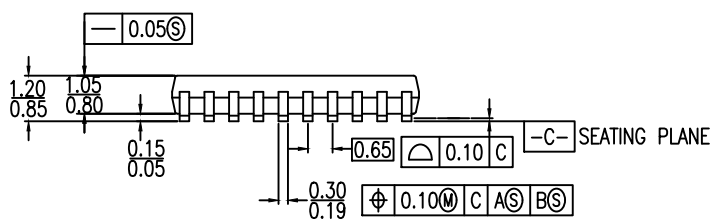
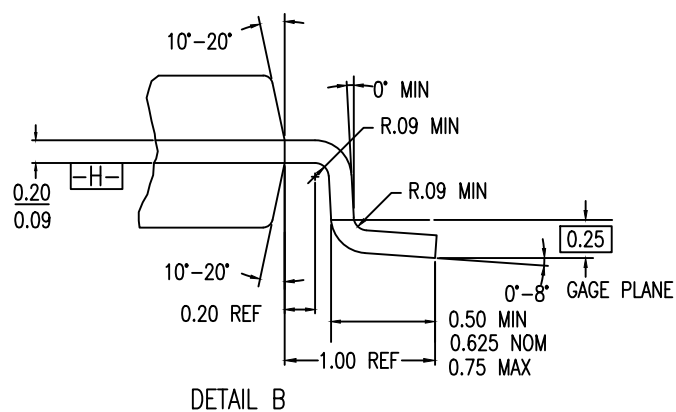
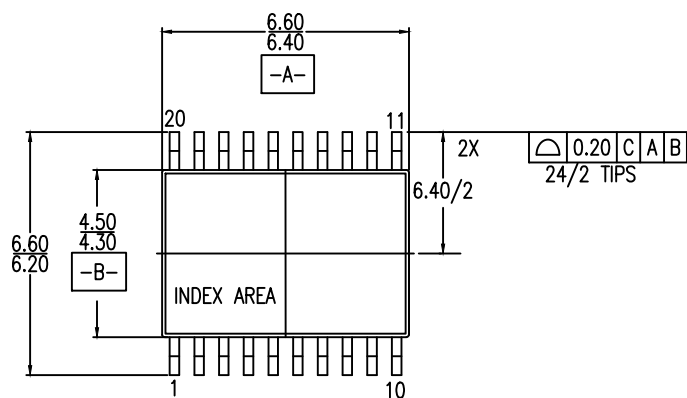
S2
EPAD 1.65 mm SQ

REVISIONS			
DATE	REV	DESCRIPTION	AUTHOR
11/14/08	00	INITIAL RELEASE	RC
11/28/12	01	ADD EPAD OPTION	RC
12/5/13	02	COMBINE POD & LAND PATTERN	J.HUA
7/14/14	03	Change Dimension aaa	J.HUA
3/1/19	04	Add Wettable Flank Option	J.HUA
9/19/19	05	Add Wettable Flank S2	J.HUA
7/30/21	06	Update Dimensions of Wettable Flank	JHTAN
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED		6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591	
DECIMAL	ANGULAR		
X±	±1°		
XX±			
XXX±			
		TITLE NDC20 Package Outline Drawing 3.0 x 3.0 mm Body 0.40mm Pitch VFQFPN	
SIZE	DRAWING No.		
C	PSC-4179	REV 06	
DO NOT SCALE DRAWING		SHEET 2 OF 2	



SECTION A-A

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSION ARE IN MM.

RECOMMENDED LAND PATTERN DIMENSIONS

1. ALL DIMENSIONS ARE IN MILLIMETERS

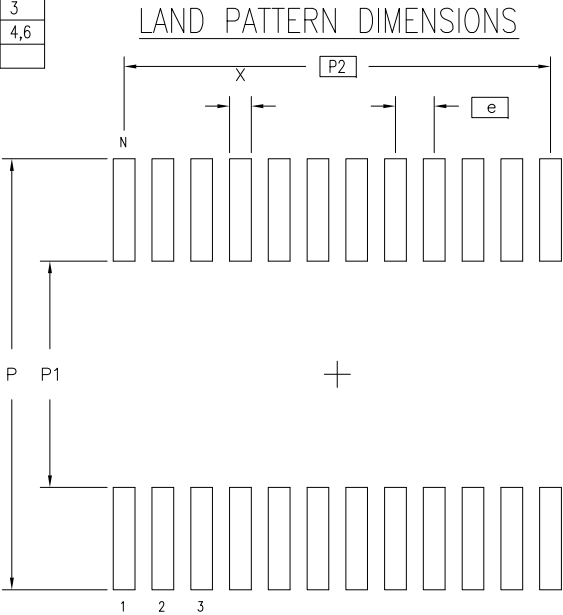
PACKAGE DIMENSION:

SYMBOL	JEDEC VARIATION																								NOTE
	AB (INCHES)			AB (mm)			AD (INCHES)			AD (mm)			AE (INCHES)			AE (mm)			AF (INCHES)			AF (mm)			
	MIN.	NOM.	MAX	MIN.	NOM.	MAX	MIN.	NOM.	MAX	MIN.	NOM.	MAX	MIN.	NOM.	MAX	MIN.	NOM.	MAX	MIN.	NOM.	MAX	MIN.	NOM.	MAX	
A	0.061	0.064	0.068	1.55	1.63	1.73	0.061	0.064	0.068	1.55	1.63	1.73	0.061	0.064	0.068	1.55	1.63	1.73	0.061	0.064	0.068	1.55	1.63	1.73	
A1	0.004	0.006	0.01	0.10	0.15	0.25	0.004	0.006	0.01	0.10	0.15	0.25	0.004	0.006	0.01	0.10	0.15	0.25	0.004	0.006	0.01	0.10	0.15	0.25	
A2	0.055	0.058	0.061	1.40	1.47	1.55	0.055	0.058	0.061	1.40	1.47	1.55	0.055	0.058	0.061	1.40	1.47	1.55	0.055	0.058	0.061	1.40	1.47	1.55	11
D	0.189	0.194	0.196	4.80	4.93	4.98	0.337	0.342	0.344	8.56	8.69	8.74	0.337	0.342	0.344	8.56	8.69	8.74	0.339	0.39	0.394	8.60	9.91	10.01	4,5
E	0.23	0.236	0.244	5.84	5.99	6.20	0.23	0.236	0.244	5.84	5.99	6.20	0.23	0.236	0.244	5.84	5.99	6.20	0.23	0.236	0.244	5.84	5.99	6.20	3
E1	0.15	0.155	0.157	3.81	3.94	3.99	0.15	0.155	0.157	3.81	3.94	3.99	0.15	0.155	0.157	3.81	3.94	3.99	0.15	0.155	0.157	3.81	3.94	3.99	4,6
N	16						20						24						28						

NOTES:

- 1
- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- 2
- DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
- 3
- DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-
- 4
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
- 5
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- 6
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE
- 7
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- 8
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- 9
- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- 10
- ALL DIMENSIONS ARE IN INCHES
- 11
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-137, VARIATION AB, AD, AE & AF. EXCEPTIONS: JEDEC DIMENSION A2 MAX IS .059

DATE CREATED	REVISIONS		
	REV	DESCRIPTION	AUTHOR
03/10/95	01	REDRAW TO JEDEC FORMAT	T. VU
08/15/95	02	ADD 28 LD	T. VU
12/15/99	03	CHANGE TO QSOP	S.SUE
10/08/04	04	ADD "GREEN" PCG NOMENCLATURE	TU VU
11/15/11	05	CHANGE RADIUS DIM	CK LEE
1/13/16	06	ADD mm DIMENSION on TABLE	JH
7/14/17	07	ADD "N" ON TABLE	JH
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			

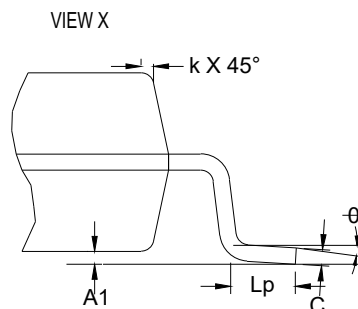
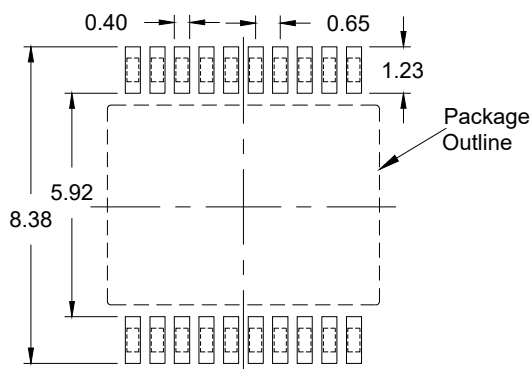
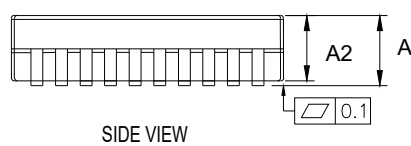
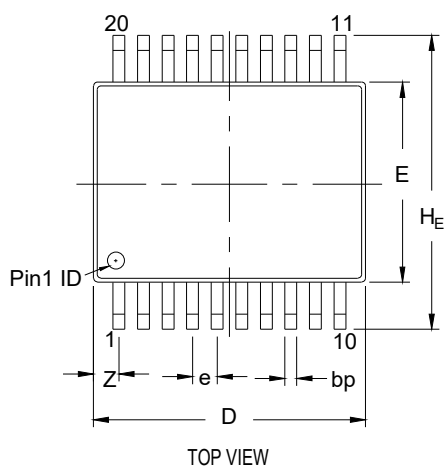


LAND PATTERN DIMENSION:

	INCHES		mm		INCHES		mm		INCHES		mm		INCHES		mm	
	MIN.	MAX	MIN.	MAX	MIN.	MAX	MIN.	MAX	MIN.	MAX	MIN.	MAX	MIN.	MAX	MIN.	MAX
P	0.274	0.282	6.96	7.16	0.274	0.282	6.96	7.16	0.274	0.282	6.96	7.16	0.274	0.282	6.96	7.16
P1	0.142	0.150	3.61	3.81	0.142	0.150	3.61	3.81	0.142	0.150	3.61	3.81	0.142	0.150	3.61	3.81
P2	0.175	BSC	4.45	BSC	0.225	BSC	5.71	BSC	0.275	BSC	6.99	BSC	0.325	BSC	8.25	BSC
X	0.010	0.018	0.254	0.457	0.010	0.018	0.254	0.457	0.010	0.018	0.254	0.457	0.010	0.018	0.254	0.457
e	0.025	BSC	0.635	BSC	0.025	BSC	0.635	BSC	0.025	BSC	0.635	BSC	0.025	BSC	0.635	BSC
N	16				20				24				28			

TOLERANCES UNLESS SPECIFIED		 IDT™ www.IDT.com	2975 Stender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674		
DECIMAL	ANGULAR				
XX±	±				
XXX±					
XXXX±					
		TITLE PC/PCG PACKAGE OUTLINE .150" BODY WIDTH QSOP .025" PITCH			
SIZE C		DRAWING No. PSC-4040		REV 07	
DO NOT SCALE DRAWING			SHEET 2 OF 2		

BASED ON JEDEC JEP95: MO-150



DIMENSIONS OF SUB-GROUP C1	
A min	1.73
A1 min	0.05
A1 max	0.21
A2 min	1.68
A2 max	1.78
c min	0.09
c max	0.20
D min*	7.07
D max*	7.33
E min*	5.20
E max*	5.38
k min	0.25
θ max	0°
θ max	10°

* WITHOUT MOLD FLASH

DIMENSIONS OF SUB-GROUP B1	
A max	1.99
bp min	0.25
bp max	0.38
e nom	0.65
H _E min	7.40
H _E max	8.20
Lpmin	0.63
Z max	0.74

- Dimensions
- Weight ≤ 0.3 g
- Body Material LOW STRESS EPOXY
- Lead Material FeNi-ALLOY or Cu-ALLOY
- Lead Finish SOLDER PLATING
- Lead Form Z-BENDS

NOTES:

- JEDEC compatible.
- All dimensions are in mm and angles are in degrees.

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