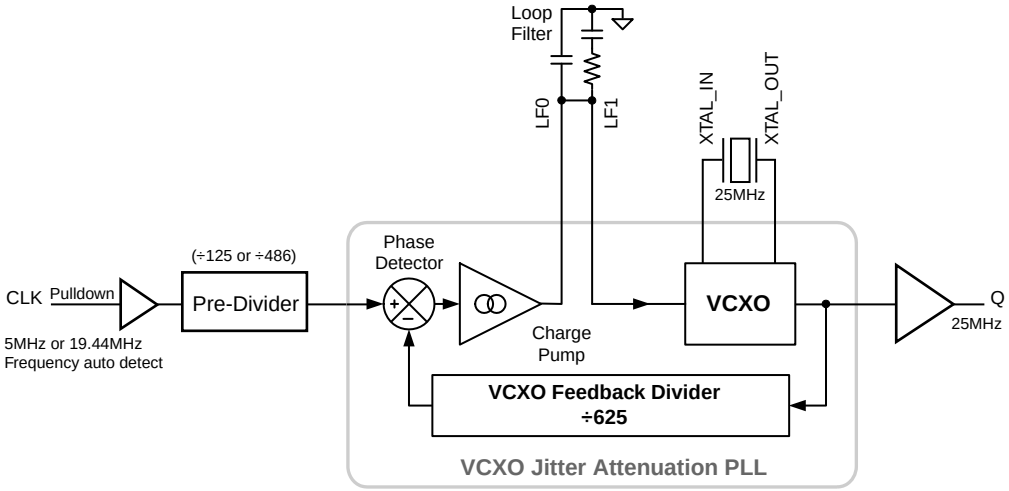
General Description

The 8101925 is a high performance, low jitter/low phase noise VCXO from IDT. The 8101925 works in conjunction with a 25MHz pullable crystal to generate an LVCMOS/LVTTL output clock of 25MHz from an input clock of 5MHz or 19.44MHz. The output range is ±100ppm around the nominal crystal frequency. The device is packaged in a small 16 TSSOP package and is ideal for use on space constrained boards.

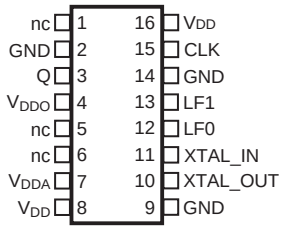
Features

- One single-ended LVCMOS or LVTTL output
- One single-ended clock accepts the following input types: LVCMOS, LVTTL
- Output frequency: 25MHz
- Accepts 5MHz or 19.44MHz with auto input frequency detect
- Absolute pull range (APR): ±100ppm
- RMS phase jitter. (12kHz – 5MHz): 0.4ps (typical)
- Full 3.3V supply, or 3.3V core/2.5V output supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- For functional replacement part use 810252

Block Diagram



Pin Assignment



8101925

16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 5, 6	nc	Unused		No connect.
2, 9, 14	GND	Power		Power supply ground.
3	Q	Output		Single-ended clock output. LVCMOS/ LVTTL interface levels.
4	V_{DDO}	Power		Output power supply pin.
7	V_{DDA}	Power		Analog supply pin.
8, 16	V_{DD}	Power		Core power supply pins.
10, 11	XTAL_OUT, XTAL_IN	Input		VCXO crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
12	LF0	Analog Input/ Output		Output to external loop filter. Charge pump output.
13	LF1	Analog Input/ Output		Input from external loop filter. VCXO control voltage input.
15	CLK	Input	Pulldown	Single-ended clock input with auto frequency detect. LVCMOS/LVTTL interface levels.

NOTE: *Pulldown* refers to an internal input resistor. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance	V_{DDO} = 3.3V±5%		17		Ω
		V_{DDO} = 2.5V±5%		20		Ω

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	81.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.05	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				83	mA
I_{DDA}	Analog Supply Current				5	mA
I_{DDO}	Output Supply Current				1	mA

Table 3B. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.05	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				81	mA
I_{DDA}	Analog Supply Current				5	mA
I_{DDO}	Output Supply Current				1	mA

Table 3C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	V_{DD} = 3.465V	2		V_{DD} + 0.3	V
		V_{DD} = 2.625V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	V_{DD} = 3.465V	-0.3		0.8	V
		V_{DD} = 2.625V	-0.3		0.7	V
V_{LF1}	VCXO Control Voltage		0		V_{DD}	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage	V_{DDO} = 3.3V ± 5%, I_{OH} = -12mA	2.6			V
		V_{DDO} = 2.5V ± 5%, I_{OH} = -12mA	1.8			V
V_{OL}	Output Low Voltage	V_{DDO} = 3.3V or 2.5V ± 5%, I_{OL} = 12mA			0.5	V

AC Electrical Characteristics

Table 4A. AC Characteristics, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			25		MHz
f_{IN}	Input Frequency				5	MHz
					19.44	MHz
tjit(θ)	RMS Phase Jitter (Random); NOTE 1	f_{OUT} = 25MHz, Integration Range: 12kHz – 5MHz		0.4		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	650		1050	ps
odc	Output Duty Cycle		40		60	%

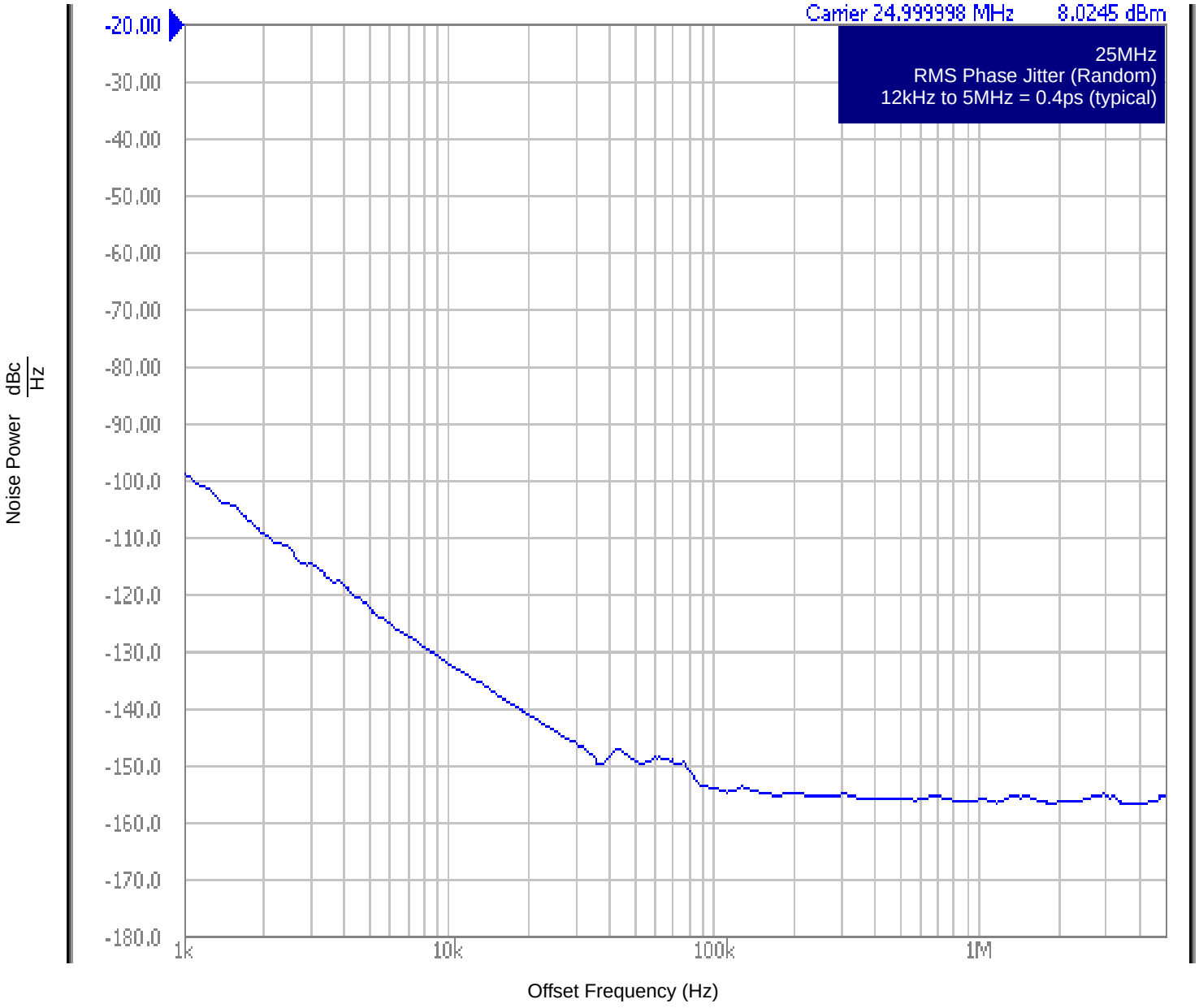
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 48Hz bandwidth filter.
NOTE 1: Refer to the Phase Noise Plot.

Table 4B. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C to 85°C

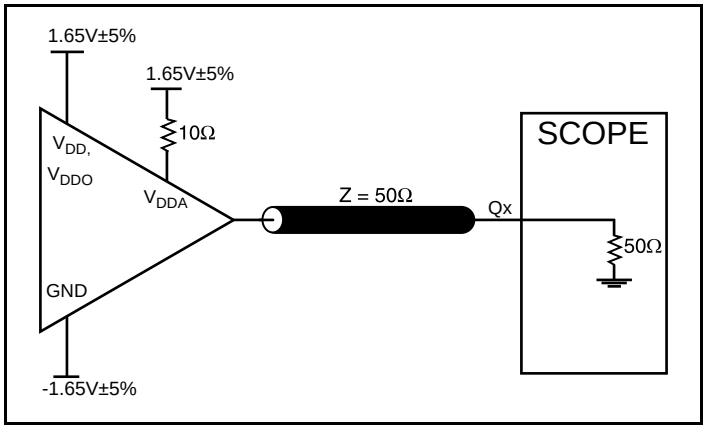
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			25		MHz
f_{IN}	Input Frequency				5	MHz
					19.44	MHz
tjit(θ)	RMS Phase Jitter (Random);	f_{OUT} = 25MHz, Integration Range: 12kHz – 5MHz		0.4		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	900		1600	ps
odc	Output Duty Cycle		40		60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 48Hz bandwidth filter.

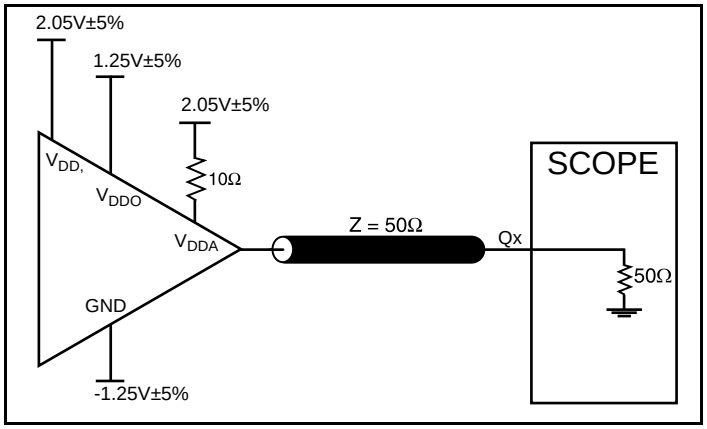
Typical Phase Noise at 25MHz



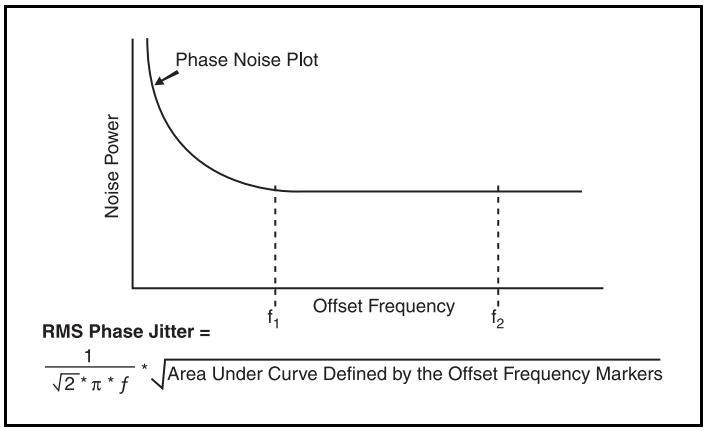
Parameter Measurement Information



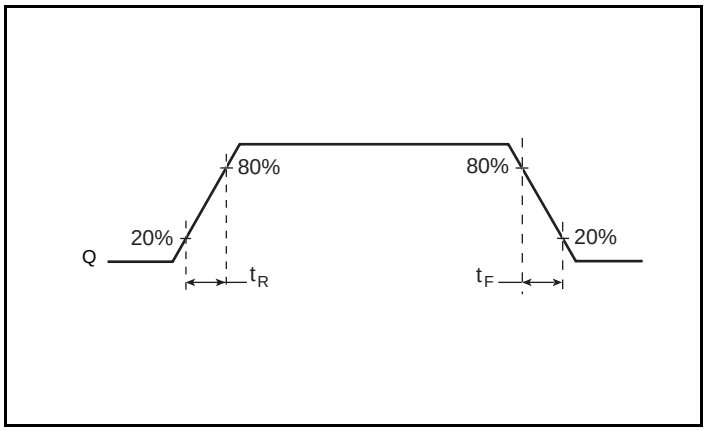
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



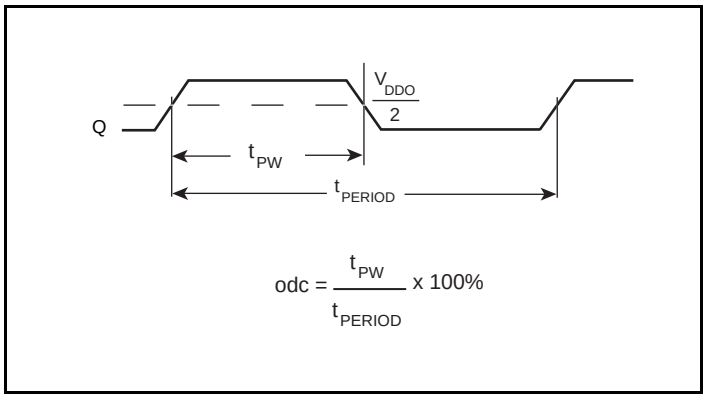
3.3V Core/2.5V LVCMOS Output Load AC Test Circuit



RMS Phase Jitter



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Applications Information

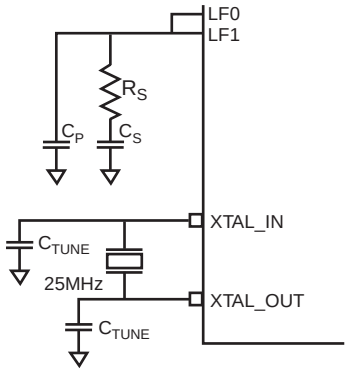
Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the VCXO-PLL. In choosing a crystal, special precaution must be taken with the package and load capacitance (C_L). In addition, frequency, accuracy and temperature range must also be considered. Since the pulling range of a crystal also varies with the package, it is recommended that a metal-canned package like HC49 be used. Generally, a metal-canned package has a larger pulling range than a surface mounted device (SMD). For crystal selection information, refer to the *VCXO Crystal Selection Application Note.*

The crystal's load capacitance C_L characteristic determines its resonating frequency and is closely related to the VCXO tuning range. The total external capacitance seen by the crystal when installed on a board is the sum of the stray board capacitance, IC package lead capacitance, internal varactor capacitance and any installed tuning capacitors (C_{TUNE}).

If the crystal's C_L is greater than the total external capacitance, the VCXO will oscillate at a higher frequency than the crystal specification. If the crystal's C_L is lower than the total external capacitance, the VCXO will oscillate at a lower frequency than the crystal specification. In either case, the absolute tuning range is reduced. The correct value of C_L is dependent on the characteristics of the VCXO. The recommended C_L in the Crystal Parameter Table balances the tuning range by centering the tuning curve.

The frequency of oscillation in the third overtone mode is not necessarily at exactly three times the fundamental frequency. The mechanical properties of the quartz element dictate the position of the overtones relative to the fundamental. The oscillator circuit may excite both the fundamental and overtone modes simultaneously. This will cause a nonlinearity in the tuning curve. This potential problem is the reason VCXO crystals are required to be tested for absence of any activity inside a ±200ppm window at three times the fundamental frequency. Refer to F_{L_3OVT} and $F_{L\_3OVT\_spurs}$ in the Crystal Characteristics Table.

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.



VCXO Characteristics Table

Symbol	Parameter	Typical	Units
k_{VCXO}	VCXO Gain	15	kHz/V
C_{V_LOW}	Low Varactor Capacitance	9.8	pF
C_{V_HIGH}	High Varactor Capacitance	22.7	pF

VCXO-PLL Loop Bandwidth Selection Table

Bandwidth	Crystal Frequency (MHz)	R_S (kΩ)	C_S (µF)	C_P (pF)
48Hz (Low)	25MHz	50	1	1500
210Hz (Mid)	25MHz	220	0.03	270
478Hz (High)	25MHz	500	0.01	100

Crystal Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
	Mode of Oscillation			Fundamental		
f_N	Frequency			25		MHz
f_T	Frequency Tolerance				±20	ppm
f_S	Frequency Stability				±20	ppm
	Operating Temperature Range		-40		+85	^{0}C
C_L	Load Capacitance			10		pF
C_O	Shunt Capacitance			4		pF
F_{L_3OVT}	3rd Overtone F_L		200			ppm
$F_{L\_3OVT\_spurs}$	3rd Overtone F_L Spurs		200			ppm
C_O / C_1	Pullability Ratio			220	240	
ESR	Equivalent Series Resistance				40	Ω
	Drive Level				1	mW
	Aging @ 25 ^{0}C	First Year			±3	ppm
		Ten Years			±10	ppm

Recommendations for Unused Input Pins

Inputs:

CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8101925 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

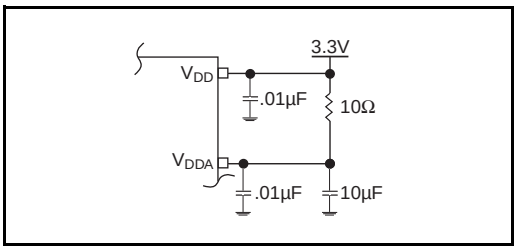


Figure 1. Power Supply Filtering

Power Considerations

This section provides information on power dissipation and junction temperature for the 8101925.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8101925 is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD} + I_{DDA}) = 3.465V * (83mA + 5mA) =$ **304.92mW**
- Power $(output)_{MAX} = V_{DDO\_MAX} * I_{DDO\_MAX} = 3.465V * 1mA =$ **3.465mW**
- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
  Output Current $I_{OUT} = V_{DD\_MAX} / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 17Ω)] =$ **25.8mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 17Ω * (25.8mA)^2 =$ **11.3mW per output**

Total Power Dissipation

Total Power
= Power $(core)_{MAX}$ + Power $(output)_{MAX}$ + Power (R_{OUT})
= 304.92mW + 3.465mW + 11.3mW
= 319.685mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 81.2°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.320W * 81.2°C/W = 111°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 5. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	81.2°C/W	73.9°C/W	70.2°C/W

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	81.2°C/W	73.9°C/W	70.2°C/W

Transistor Count

The transistor count for 8101925: 2265

Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

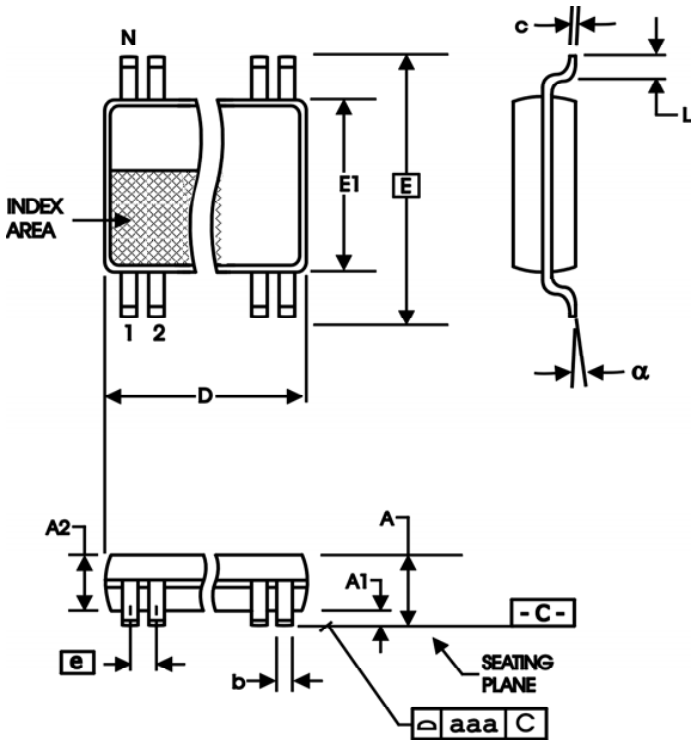


Table 7. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8101925AGILF	01925AIL	16 Lead “Lead-Free” TSSOP	Tube	-40°C to 85°C
8101925AGILFT	01925AIL	16 Lead “Lead-Free” TSSOP	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		1	Product Discontinuation Notice - Last time buy expires November 2, 2016. PDN# CQ-15-05 Update data sheet format.	11/4/15
B		1	Obsolete datasheet per PDN# CQ-15-05. Updated datasheet header/footer.	11/7/16

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