



EBU WAN PLL

IDT82V3203B

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FEATURES

HIGHLIGHTS

- The first single PLL chip:
 - Features 0.1 Hz to 560 Hz bandwidth
 - Exceeds GR-253-CORE (OC-12) and ITU-T G.813 (STM-16/Option I) jitter generation requirements
 - Provides node clocks for Cellular and WLL base-station (GSM and 3G networks)
 - Provides clocks for DSL access concentrators (DSLAM), especially for Japan TCM-ISDN network timing based ADSL equipments

MAIN FEATURES

- Provides an integrated single-chip solution for Synchronous Equipment Timing Source, including Stratum 3, SMC, 4E and 4 clocks
- Employs DPLL and APLL to feature excellent jitter performance and minimize the number of the external components
- Supports Forced or Automatic operating mode switch controlled by an internal state machine; the primary operating modes are Free-Run, Locked and Holdover
- Supports programmable DPLL bandwidth (0.1 Hz to 560 Hz in 11 steps) and damping factor (1.2 to 20 in 5 steps)
- Supports 1.1×10^{-5} ppm absolute holdover accuracy and 4.4×10^{-8} ppm instantaneous holdover accuracy
- Supports PBO to minimize phase transients on T0 DPLL output to be no more than 0.61 ns
- Supports phase absorption when phase-time changes on T0 selected input clock are greater than a programmable limit over an interval of less than 0.1 seconds
- Limits the phase and frequency offset of the outputs
- Supports manual and automatic selected input clock switch
- Supports automatic hitless selected input clock switch on clock failure

- Supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing
- Provides three 2 kHz, 4 kHz or 8 kHz frame sync input signals, and a 2 kHz and an 8 kHz frame sync output signals
- Provides three input clocks whose frequency cover from 2 kHz to 622.08 MHz
- Provides two output clocks whose frequency cover from 1 Hz to 622.08 MHz
- Provides output clocks for BITS, GPS, 3G, GSM, etc.
- Supports CMOS input/output and PECL/LVDS input/output technologies
- Supports master clock calibration
- Supports Line Card application
- Meets Telcordia GR-1244-CORE, GR-253-CORE, ITU-T G.812, ITU-T G.813 and ITU-T G.783 criteria

OTHER FEATURES

- I²C programming interface
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 68-pin VFQFPN package, Green package options available

APPLICATIONS

- BITS / SSU
- SMC / SEC (SONET / SDH)
- DWDM cross-connect and transmission equipments
- Central Office Timing Source and Distribution
- Core and access IP switches / routers
- Gigabit and Terabit IP switches / routers
- IP and ATM core switches and access equipments
- Cellular and WLL base-station node clocks
- Broadband and multi-service access equipments
- Any other telecom equipments that need synchronous equipment system timing

DESCRIPTION

The IDT82V3203B is an integrated, single-chip solution for the Synchronous Equipment Timing Source for Stratum 3, SMC, 4E and 4 clocks in SONET / SDH equipments, DWDM and Wireless base station, such as GSM, 3G, DSL concentrator, Router and Access Network applications.

The device supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing.

An input clock is automatically or manually selected for DPLL locking. The DPLL supports three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode, the DPLL refers to the master clock. In Locked mode, the DPLL locks to the selected input clock. In Holdover mode, the DPLL resorts to the frequency data acquired in Locked mode. Whatever the operating mode is, the DPLL gives a stable

performance without being affected by operating conditions or silicon process variations.

If the DPLL outputs are processed by T0/T4 APLL, the outputs of the device will be in a better jitter/wander performance.

The device provides programmable DPLL bandwidths: 0.1 Hz to 560 Hz in 11 steps and damping factors: 1.2 to 20 in 5 steps. Different settings cover all SONET / SDH clock synchronization requirements.

A high stable input is required for the master clock in different applications. The master clock is used as a reference clock for all the internal circuits in the device. It can be calibrated within ± 741 ppm.

All the read/write registers are accessed only through an I²C programming interface.

The device can be used typically in Line Card application.

FUNCTIONAL BLOCK DIAGRAM

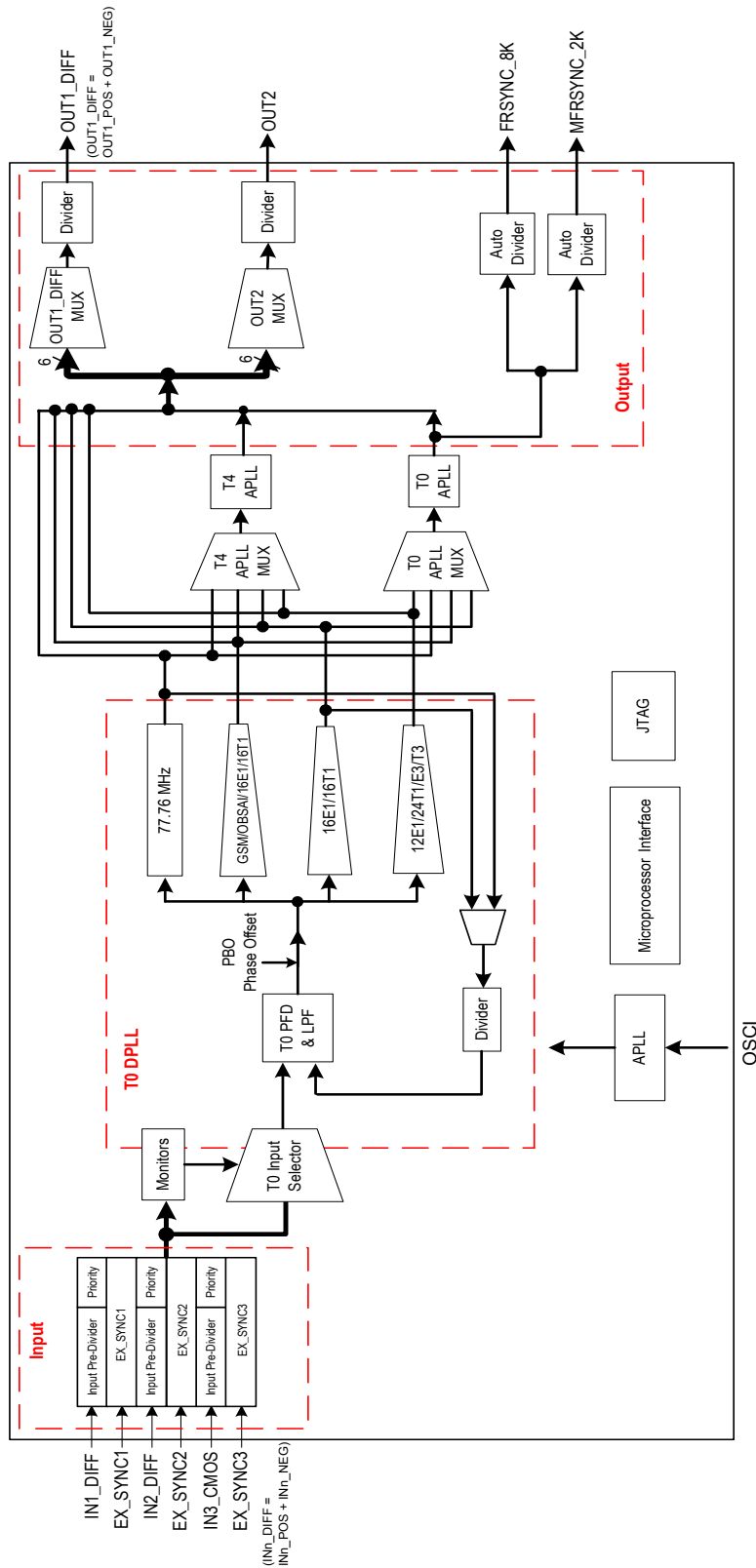


Figure 1. Functional Block Diagram

1 PIN ASSIGNMENT

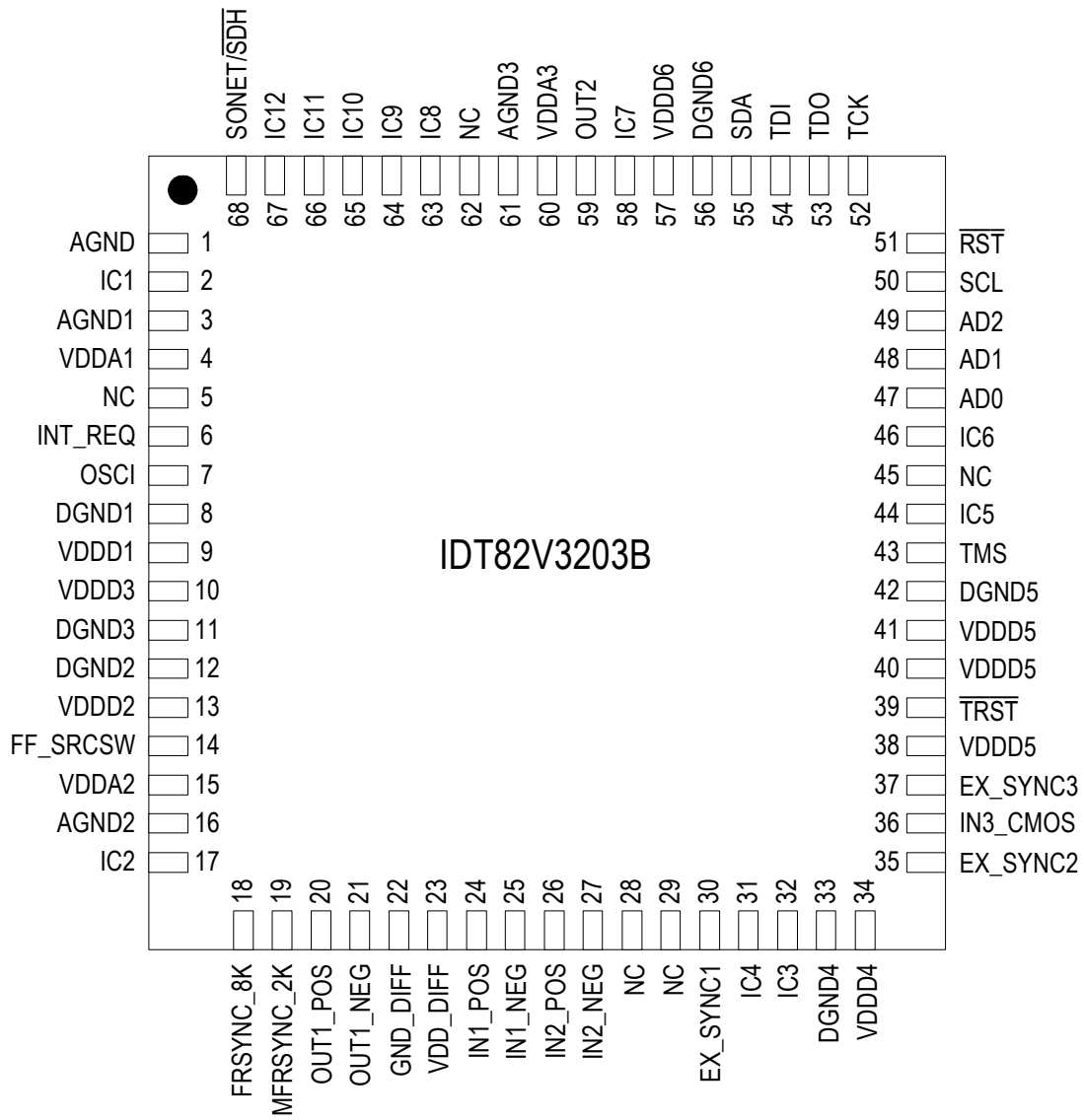


Figure 2. Pin Assignment (Top View)

2 PIN DESCRIPTION

Table 1: Pin Description

| Name | Pin No. | I/O | Type | Description ¹ |
|---|----------|----------------|-----------|--|
| Global Control Signal | | | | |
| OSCI | 7 | I | CMOS | OSCI: Crystal Oscillator Master Clock A nominal 12.8000 MHz clock provided by a crystal oscillator is input on this pin. It is the master clock for the device. |
| FF_SRC SW | 14 | I pull-down | CMOS | FF_SRC SW: External Fast Selection Enable During reset, this pin determines the default value of the EXT_SW bit (b4, 0BH) ² . The EXT_SW bit determines whether the External Fast Selection is enabled. High: The default value of the EXT_SW bit (b4, 0BH) is '1' (External Fast selection is enabled); Low: The default value of the EXT_SW bit (b4, 0BH) is '0' (External Fast selection is disabled). After reset, this pin selects an input clock for the T0 DPLL if the External Fast selection is enabled: High: IN1_DIFF is selected. Low: IN2_DIFF is selected. After reset, the input on this pin takes no effect if the External Fast selection is disabled. |
| SONET/ $\overline{\text{SDH}}$ | 68 | I pull-down | CMOS | SONET/$\overline{\text{SDH}}$: SONET / SDH Frequency Selection During reset, this pin determines the default value of the IN_SONET_SDH bit (b2, 09H): High: The default value of the IN_SONET_SDH bit is '1' (SONET); Low: The default value of the IN_SONET_SDH bit is '0' (SDH). After reset, the value on this pin takes no effect. |
| $\overline{\text{RST}}$ | 51 | I pull-up | CMOS | $\overline{\text{RST}}$: Reset A low pulse of at least 50 μs on this pin resets the device. After this pin is high, the device will still be held in reset state for 500 ms (typical). |
| Frame Synchronization Input Signal | | | | |
| EX_SYNC1 | 30 | I pull-down | CMOS | EX_SYNC1: External Sync Input 1 A 2 kHz, 4 kHz or 8 kHz signal is input on this pin. |
| EX_SYNC2 | 35 | I pull-down | CMOS | EX_SYNC2: External Sync Input 2 A 2 kHz, 4 kHz or 8 kHz signal is input on this pin. |
| EX_SYNC3 | 37 | I pull-down | CMOS | EX_SYNC3: External Sync Input 3 A 2 kHz, 4 kHz or 8 kHz signal is input on this pin. |
| Input Clock | | | | |
| IN1_POS ⁸ IN1_NEG | 24 25 | I | PECL/LVDS | IN1_POS / IN1_NEG: Positive / Negative Input Clock 1 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected. Single-ended input for differential input is also supported. Refer to Chapter 8.3.2.3 Single-Ended Input for Differential Input . |
| IN2_POS ⁹ IN2_NEG | 26 27 | I | PECL/LVDS | IN2_POS / IN2_NEG: Positive / Negative Input Clock 2 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected. Single-ended input for differential input is also supported. Refer to Chapter 8.3.2.3 Single-Ended Input for Differential Input . |
| IN3_CMOS | 36 | I pull-down | CMOS | IN3_CMOS: Input Clock 3 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin. |

Table 1: Pin Description (Continued)

| Name | Pin No. | I/O | Type | Description ¹ |
|---|----------------|----------------|-----------|---|
| Output Frame Synchronization Signal | | | | |
| FRSYNC_8K | 18 | O | CMOS | FRSYNC_8K: 8 kHz Frame Sync Output An 8 kHz signal is output on this pin. |
| MFRSYNC_2K | 19 | O | CMOS | MFRSYNC_2K: 2 kHz Multiframe Sync Output A 2 kHz signal is output on this pin. |
| Output Clock | | | | |
| OUT1_POS OUT1_NEG | 20 21 | O | PECL/LVDS | OUT1_POS / OUT1_NEG: Positive / Negative Output Clock 1 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 ⁴ , N x T1 ⁵ , N x 13.0 MHz ⁶ , N x 3.84 MHz ⁷ , E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially output on this pair of pins. |
| OUT2 | 59 | O | CMOS | OUT2: Output Clock 2 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 ⁴ , N x T1 ⁵ , N x 13.0 MHz ⁶ , N x 3.84 MHz ⁷ , E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin. |
| I²C Programming Interface | | | | |
| INT_REQ | 6 | O | CMOS | INT_REQ: Interrupt Request This pin is used as an interrupt request. The output characteristics are determined by the HZ_EN bit (b1, 0CH) and the INT_POL bit (b0, 0CH). |
| AD0 AD1 AD2 | 47 48 49 | I | CMOS | AD[2:0]: Address Input 2 to 0 The address is input on these pins. |
| SCL | 50 | I | CMOS | SCL: Serial Clock Line The serial clock is input on this pin. The clock is 400 kbit/s in Fast-mode and 3.4 Mbit/s in High-speed mode. |
| SDA | 55 | I/O | CMOS | SDA: Serial Data Input/Output This pin is used as the input/output for the serial data. |
| JTAG (per IEEE 1149.1) | | | | |
| $\overline{\text{TRST}}$ | 39 | I pull-down | CMOS | $\overline{\text{TRST}}$: JTAG Test Reset (Active Low) A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used. |
| TMS | 43 | I pull-up | CMOS | TMS: JTAG Test Mode Select The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK. |
| TCK | 52 | I pull-down | CMOS | TCK: JTAG Test Clock The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state. |
| TDI | 54 | I pull-up | CMOS | TDI: JTAG Test Data Input The test data is input on this pin. It is clocked into the device on the rising edge of TCK. |
| TDO | 53 | O | CMOS | TDO: JTAG Test Data Output The test data is output on this pin. It is clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning. This pin can indicate the interrupt of T0 selected input clock fail, as determined by the LOS_FLAG_ON_TDO bit (b6, 0BH). Refer to Chapter 3.8.1 Input Clock Validity for details. |

Table 1: Pin Description (Continued)

| Name | Pin No. | I/O | Type | Description ¹ |
|---------------------------|------------|--------|------|--|
| Power & Ground | | | | |
| VDDD1 | 9 | Power | - | VDDDn: 3.3 V Digital Power Supply Each VDDDn should be paralleled with ground through a 0.1 μ F capacitor. |
| VDDD2 | 13 | | | |
| VDDD3 | 10 | | | |
| VDDD4 | 34 | | | |
| VDDD5 | 38, 40, 41 | | | |
| VDDD6 | 57 | | | |
| VDDA1 | 4 | Power | - | VDDAn: 3.3 V Analog Power Supply Each VDDAn should be paralleled with ground through a 0.1 μ F capacitor. |
| VDDA2 | 15 | | | |
| VDDA3 | 60 | | | |
| VDD_DIFF | 23 | Power | - | VDD_DIFF: 3.3 V Power Supply for OUT1 |
| DGND1 | 8 | Ground | - | DGNDn: Digital Ground |
| DGND2 | 12 | | | |
| DGND3 | 11 | | | |
| DGND4 | 33 | | | |
| DGND5 | 42 | | | |
| DGND6 | 56 | | | |
| AGND1 | 3 | Ground | - | AGNDn: Analog Ground |
| AGND2 | 16 | | | |
| AGND3 | 61 | | | |
| GND_DIFF | 22 | Ground | - | GND_DIFF: Ground for OUT1 |
| AGND | 1 | Ground | - | AGND: Analog Ground |

Table 1: Pin Description (Continued)

| Name | Pin No. | I/O | Type | Description ¹ |
|--|-------------------|-----|------|---|
| Others | | | | |
| IC1 | 2 | | | IC: Internal Connected Internal Use. These pins should be left open for normal operation. |
| IC2 | 17 | | | |
| IC3 | 32 | | | |
| IC4 | 31 | | | |
| IC5 | 44 | | | |
| IC6 | 46 | | | |
| IC7 | 58 | - | - | |
| IC8 | 63 | | | |
| IC9 | 64 | | | |
| IC10 | 65 | | | |
| IC11 | 66 | | | |
| IC12 | 67 | | | |
| NC | 5, 28, 29, 45, 62 | - | - | NC: Not Connected |
| Note: 1. All the unused input pins should be connected to ground; the output of all the unused output pins are don't-care. 2. The contents in the brackets indicate the position of the register bit/bits. 3. N x 8 kHz: 1 ≤ N ≤ 19440. 4. N x E1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64. 5. N x T1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96. 6. N x 13.0 MHz: N = 1, 2, 4. 7. N x 3.84 MHz: N = 1, 2, 4, 8, 16, 10, 20, 40. 8. IN1_POS and IN1_NEG equals to IN1_DIFF. 9. IN2_POS and IN2_NEG equals to IN2_DIFF. | | | | |

3 FUNCTIONAL DESCRIPTION

3.1 RESET

The reset operation resets all registers and state machines to their default value or status.

After power on, the device must be reset for normal operation.

For a complete reset, the \overline{RST} pin must be asserted low for at least 50 μ s. After the \overline{RST} pin is pulled high, the device will still be in reset state for 500 ms (typical). If the \overline{RST} pin is held low continuously, the device remains in reset state.

3.2 MASTER CLOCK

A nominal 12.8000 MHz clock, provided by a crystal oscillator, is input on the OSC1 pin. This clock is provided for the device as a master clock. The master clock is used as a reference clock for all the internal circuits. A better active edge of the master clock is selected by the OSC_EDGE bit to improve jitter and wander performance.

In fact, an offset from the nominal frequency may input on the OSC1 pin. This offset can be compensated by setting the NOMINAL_FREQ_VALUE[23:0] bits. The calibration range is within ± 741 ppm.

The performance of the master clock should meet GR-1244-CORE, GR-253-CORE, ITU-T G.812 and G.813 criteria.

Table 2: Related Bit / Register in Chapter 3.2

| Bit | Register | Address (Hex) |
|--------------------------|---|---------------|
| NOMINAL_FREQ_VALUE[23:0] | NOMINAL_FREQ[23:16]_CNFG, NOMINAL_FREQ[15:8]_CNFG, NOMINAL_FREQ[7:0]_CNFG | 06, 05, 04 |
| OSC_EDGE | DIFFERENTIAL_IN_OUT_OSCI_CNFG | 0A |

3.3 INPUT CLOCKS & FRAME SYNC SIGNALS

Altogether three clocks and three frame sync signals are input to the device.

3.3.1 INPUT CLOCKS

The device provides a CMOS input clock port: IN3_CMOS, and two PECL/LVDS input clock ports: IN1_DIFF and IN2_DIFF. IN1_DIFF and IN2_DIFF automatically detect whether the signal is PECL or LVDS (IN1_POS and IN1_NEG equals to IN1_DIFF, IN2_POS and IN2_NEG equals to IN2_DIFF).

According to the input clock source, the following clock sources are supported:

- T1: Recovered clock from STM-N or OC-n
- T2: PDH network synchronization timing
- T3: External synchronization reference timing

The clock sources can be from T1, T2 or T3.

For SDH and SONET networks, the default frequency is different. SONET / SDH frequency selection is controlled by the IN_SONET_SDH bit. During reset, the default value of the IN_SONET_SDH bit is deter-

mined by the SONET/SDH pin: high for SONET and low for SDH. After reset, the input signal on the SONET/SDH pin takes no effect.

IDT82V3203B supports single-ended input for differential input. Refer to [Chapter 8.3.2.3 Single-Ended Input for Differential Input](#).

3.3.2 FRAME SYNC INPUT SIGNALS

Three 2 kHz, 4 kHz or 8 kHz frame sync signals are input on the EX_SYNC1, EX_SYNC2 and EX_SYNC3 pins respectively. They are CMOS inputs. The input frequency should match the setting in the SYNC_FREQ[1:0] bits. The frame sync signals are only valid for the OC-n clock (6.48 MHz, 19.44 MHz, 38.88 MHz and 77.76 MHz) input.

Only one of the three frame sync input signals is used for frame sync output signal synchronization. Refer to [Chapter 3.13.2 Frame SYNC Output Signals](#) for details.

Table 3: Related Bit / Register in Chapter 3.3

| Bit | Register | Address (Hex) |
|----------------|-----------------|---------------|
| IN_SONET_SDH | INPUT_MODE_CNFG | 09 |
| SYNC_FREQ[1:0] | | |

3.4 INPUT CLOCK PRE-DIVIDER

Each input clock is assigned an internal Pre-Divider. The Pre-Divider is used to divide the clock frequency down to the DPLL required frequency, which is no more than 38.88 MHz. For each input clock, the DPLL required frequency is set by the corresponding IN_FREQ[3:0] bits.

If the input clock is of 2 kHz, 4 kHz or 8 kHz, the Pre-Divider is bypassed automatically and the corresponding IN_FREQ[3:0] bits should be set to match the input frequency; the input clock can be inverted, as determined by the IN_2K_4K_8K_INV bit.

Each Pre-Divider consists of a HF (High Frequency) Divider (only available for IN1_DIFF and IN2_DIFF), a DivN Divider and a Lock 8k Divider, as shown in Figure 3.

The HF Divider, which is only available for IN1_DIFF and IN2_DIFF, should be used when the input clock is higher than (>) 155.52 MHz. The input clock can be divided by 4, 5 or can bypass the HF Divider, as determined by the IN1_DIFF_DIV[1:0]/IN2_DIFF_DIV[1:0] bits correspondingly.

Either the DivN Divider or the Lock 8k Divider can be used or both can be bypassed, as determined by the DIRECT_DIV bit and the LOCK_8K bit.

When the DivN Divider is used, the division factor setting should observe the following order:

1. Select an input clock by the PRE_DIV_CH_VALUE[3:0] bits;
2. Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits;
3. Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.

Once the division factor is set for the input clock selected by the PRE_DIV_CH_VALUE[3:0] bits, it is valid until a different division factor is set for the same input clock. The division factor is calculated as follows:

$$\text{Division Factor} = (\text{the frequency of the clock input to the DivN Divider} \div \text{the frequency of the DPLL required clock set by the IN_FREQ[3:0] bits}) - 1$$

The DivN Divider can only divide the input clock whose frequency is lower than (<) 155.52 MHz.

When the Lock 8k Divider is used, the input clock is divided down to 8 kHz automatically.

The Pre-Divider configuration and the division factor setting depend on the input clock on one of the clock input pin and the DPLL required clock. Here is an example:

The input clock on the IN2_DIFF pin is 622.08 MHz; the DPLL required clock is 6.48 MHz by programming the IN_FREQ[3:0] bits of register IN2_DIFF to '0010'. Do the following step by step to divide the input clock:

1. Use the HF Divider to divide the clock down to 155.52 MHz:
 $622.08 \div 155.52 = 4$, so set the IN2_DIFF_DIV[1:0] bits to '01';
2. Use the DivN Divider to divide the clock down to 6.48 MHz:
 Set the PRE_DIV_CH_VALUE[3:0] bits to '0110';
 Set the DIRECT_DIV bit in Register IN2_DIFF_CNFG to '1' and the LOCK_8K bit in Register IN2_DIFF_CNFG to '0';
 $155.52 \div 6.48 = 24$; $24 - 1 = 23$, so set the PRE_DIVN_VALUE[14:0] bits to '10111'.

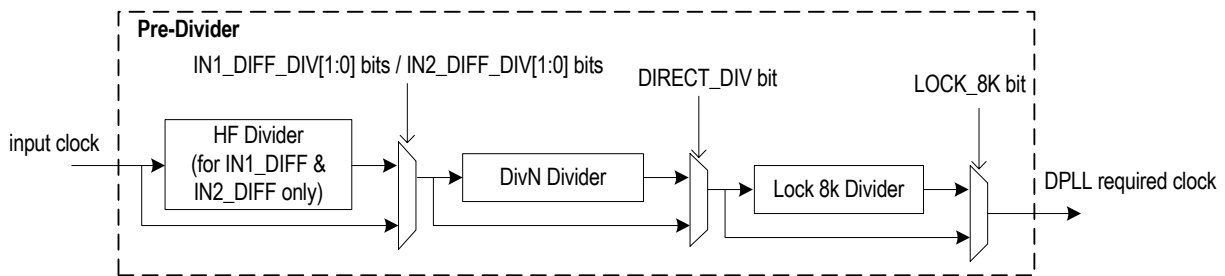


Figure 3. Pre-Divider for An Input Clock

Table 4: Related Bit / Register in Chapter 3.4

| Bit | Register | Address (Hex) |
|-----------------------|---|---------------|
| IN1_DIFF_DIV[1:0] | IN1_DIFF_IN2_DIFF_HF_DIV_CNFG | 18 |
| IN2_DIFF_DIV[1:0] | | |
| IN_FREQ[3:0] | IN1_DIFF_CNFG, IN2_DIFF_CNFG, IN3_CMOS_CNFG | 19, 1A, 1D |
| DIRECT_DIV | | |
| LOCK_8K | | |
| IN_2K_4K_8K_INV | FR_MFR_SYNC_CNFG | 74 |
| PRE_DIV_CH_VALUE[3:0] | PRE_DIV_CH_CNFG | 23 |
| PRE_DIVN_VALUE[14:0] | PRE_DIVN[14:8]_CNFG, PRE_DIVN[7:0]_CNFG | 25, 24 |

3.5 INPUT CLOCK QUALITY MONITORING

The qualities of all the input clocks are always monitored in the following aspects:

- Activity
- Frequency

The qualified clocks are available for T0 DPLL selection. The T0 selected input clock has to be monitored further. Refer to [Chapter 3.7 Selected Input Clock Monitoring](#) for details.

3.5.1 ACTIVITY MONITORING

Activity is monitored by using an internal leaky bucket accumulator, as shown in [Figure 4](#).

Each input clock is assigned an internal leaky bucket accumulator. The input clock is monitored for each period of 128 ms and the internal leaky bucket accumulator increases by 1 when an event is detected; it decreases by 1 if no event is detected within the period set by the decay rate. The event is that an input clock drifts outside ($>$) ± 500 ppm with respect to the master clock within a 128 ms period.

There are four configurations (0 - 3) for a leaky bucket accumulator. The leaky bucket configuration for an input clock is selected by the cor-

responding BUCKET_SEL[1:0] bits. Each leaky bucket configuration consists of four elements: upper threshold, lower threshold, bucket size and decay rate.

The bucket size is the capability of the accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected. The upper threshold is a point above which a no-activity alarm is raised. The lower threshold is a point below which the no-activity alarm is cleared. The decay rate is a certain period during which the accumulator decreases by 1 if no event is detected.

The leaky bucket configuration is programmed by one of four groups of register bits: the BUCKET_SIZE_n_DATA[7:0] bits, the UPPER_THRESHOLD_n_DATA[7:0] bits, the LOWER_THRESHOLD_n_DATA[7:0] bits and the DECAY_RATE_n_DATA[1:0] bits respectively; 'n' is 0 ~ 3.

The no-activity alarm status of the input clock is indicated by the INn_CMOS_NO_ACTIVITY_ALARM bit (n = 3) / INn_DIFF_NO_ACTIVITY_ALARM (n = 1 or 2) bit.

The input clock with a no-activity alarm is disqualified for clock selection for T0 DPLL.

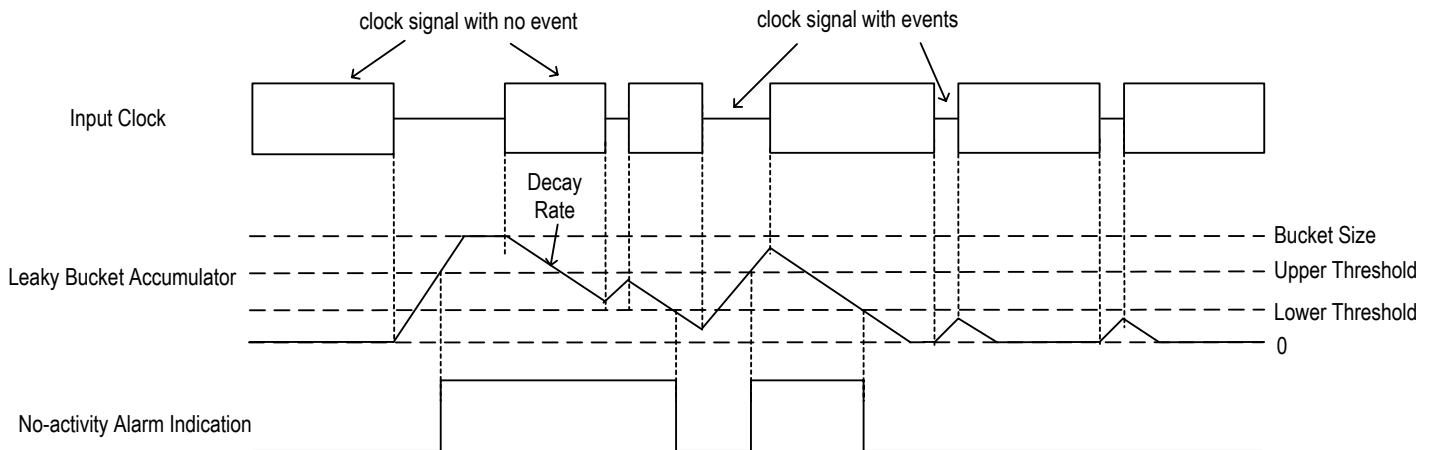


Figure 4. Input Clock Activity Monitoring

3.5.2 FREQUENCY MONITORING

Frequency is monitored by comparing the input clock with a reference clock. The reference clock can be derived from the master clock or the output of T0 DPLL, as determined by the `FREQ_MON_CLK` bit.

A frequency hard alarm threshold is set for frequency monitoring. If the `FREQ_MON_HARD_EN` bit is '1', a frequency hard alarm is raised when the frequency of the input clock with respect to the reference clock is above the threshold; the alarm is cleared when the frequency is below the threshold.

The frequency hard alarm threshold can be calculated as follows:

$$\text{Frequency Hard Alarm Threshold (ppm)} = (\text{ALL_FREQ_HARD_THRESHOLD}[3:0] + 1) \times \text{FREQ_MON_FACTOR}[3:0]$$

If the `FREQ_MON_HARD_EN` bit is '1', the frequency hard alarm status of the input clock is indicated by the `INn_CMOS_FREQ_HARD_ALARM` bit ($n = 3$) / `INn_DIFF_FREQ_HARD_ALARM` bit ($n = 1$ or 2). When the `FREQ_MON_HARD_EN` bit is '0', no frequency hard alarm is raised even if the input clock is above the frequency hard alarm threshold.

The input clock with a frequency hard alarm is disqualified for clock selection for T0 DPLL.

In addition, if the input clock is 2 kHz, 4 kHz or 8 kHz, its clock edges with respect to the reference clock are monitored. If any edge drifts outside $\pm 5\%$, the input clock is disqualified for clock selection for T0 DPLL. The input clock is qualified if any edge drifts inside $\pm 5\%$. This function is supported only when the `IN_NOISE_WINDOW` bit is '1'.

The frequency of each input clock with respect to the reference clock can be read by doing the following step by step:

1. Select an input clock by setting the `IN_FREQ_READ_CH[3:0]` bits;
2. Read the value in the `IN_FREQ_VALUE[7:0]` bits and calculate as follows:

$$\text{Input Clock Frequency (ppm)} = \text{IN_FREQ_VALUE}[7:0] \times \text{FREQ_MON_FACTOR}[3:0]$$

Note that the value set by the `FREQ_MON_FACTOR[3:0]` bits depends on the application.

Table 5: Related Bit / Register in Chapter 3.5

| Bit | Register | Address (Hex) |
|--|--|----------------|
| <code>BUCKET_SIZE_n_DATA[7:0]</code> ($3 \geq n \geq 0$) | <code>BUCKET_SIZE_0_CNFG ~ BUCKET_SIZE_3_CNFG</code> | 33, 37, 3B, 3F |
| <code>UPPER_THRESHOLD_n_DATA[7:0]</code> ($3 \geq n \geq 0$) | <code>UPPER_THRESHOLD_0_CNFG ~ UPPER_THRESHOLD_3_CNFG</code> | 31, 35, 39, 3D |
| <code>LOWER_THRESHOLD_n_DATA[7:0]</code> ($3 \geq n \geq 0$) | <code>LOWER_THRESHOLD_0_CNFG ~ LOWER_THRESHOLD_3_CNFG</code> | 32, 36, 3A, 3E |
| <code>DECAY_RATE_n_DATA[1:0]</code> ($3 \geq n \geq 0$) | <code>DECAY_RATE_0_CNFG ~ DECAY_RATE_3_CNFG</code> | 34, 38, 3C, 40 |
| <code>BUCKET_SEL[1:0]</code> | <code>IN1_DIFF_CNFG, IN2_DIFF_CNFG, IN3_CMOS_CNFG</code> | 19, 1A, 1D |
| <code>INn_CMOS_NO_ACTIVITY_ALARM</code> ($n = 3$) | <code>IN1_IN2_DIFF_STS, IN3_CMOS_STS</code> | 44, 45 |
| <code>INn_CMOS_FREQ_HARD_ALARM</code> ($n = 3$) | | |
| <code>INn_DIFF_NO_ACTIVITY_ALARM</code> ($n = 1$ or 2) | <code>IN1_IN2_DIFF_STS</code> | 45 |
| <code>INn_DIFF_FREQ_HARD_ALARM</code> ($n = 1$ or 2) | | |
| <code>FREQ_MON_CLK</code> | <code>MON_SW_PBO_CNFG</code> | 0B |
| <code>FREQ_MON_HARD_EN</code> | | |
| <code>ALL_FREQ_HARD_THRESHOLD[3:0]</code> | <code>ALL_FREQ_MON_THRESHOLD_CNFG</code> | 2F |
| <code>FREQ_MON_FACTOR[3:0]</code> | <code>FREQ_MON_FACTOR_CNFG</code> | 2E |
| <code>IN_NOISE_WINDOW</code> | <code>PHASE_MON_PBO_CNFG</code> | 78 |
| <code>IN_FREQ_READ_CH[3:0]</code> | <code>IN_FREQ_READ_CH_CNFG</code> | 41 |
| <code>IN_FREQ_VALUE[7:0]</code> | <code>IN_FREQ_READ_STS</code> | 42 |

3.6 DPLL INPUT CLOCK SELECTION

The EXT_SW bit and the T0_INPUT_SEL[3:0] bits determine the input clock selection, as shown in Table 6:

Table 6: Input Clock Selection

| Control Bits | | Input Clock Selection |
|--------------|-------------------|-------------------------|
| EXT_SW | T0_INPUT_SEL[3:0] | |
| 1 | don't-care | External Fast selection |
| 0 | other than 0000 | Forced selection |
| | 0000 | Automatic selection |

External Fast selection is done between IN1_DIFF and IN2_DIFF.

Forced selection is done by setting the related registers.

Automatic selection is done based on the results of input clocks quality monitoring and the related registers configuration.

The selected input clock is attempted to be locked by T0 DPLL.

3.6.1 EXTERNAL FAST SELECTION

In External Fast selection, only IN1_DIFF and IN2_DIFF are available for selection. Refer to Figure 5. The results of input clocks quality

monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring) do not affect input clock selection.

The T0 input clock selection is determined by the FF_SRC SW pin after reset (this pin determines the default value of the EXT_SW bit during reset, refer to Chapter 2 Pin Description), the IN1_DIFF_SEL_PRIORITY[3:0] bits and the IN2_DIFF_SEL_PRIORITY[3:0] bits, as shown in Figure 5 and Table 7:

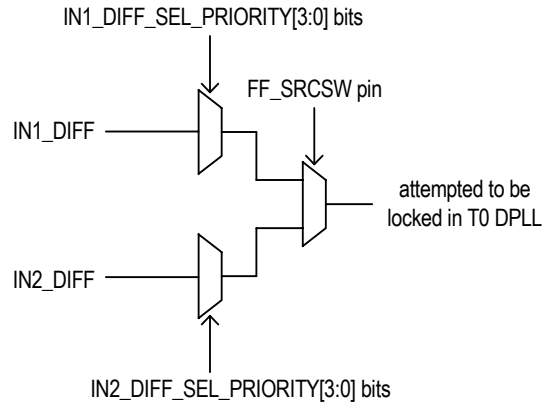


Figure 5. External Fast Selection

Table 7: External Fast Selection

| Control Pin & Bits | | | the Selected Input Clock |
|-------------------------|----------------------------|----------------------------|--------------------------|
| FF_SRC SW (after reset) | IN1_DIFF_SEL_PRIORITY[3:0] | IN2_DIFF_SEL_PRIORITY[3:0] | |
| high | other than 0000 | don't-care | IN1_DIFF |
| low | don't-care | other than 0000 | IN2_DIFF |

3.6.2 FORCED SELECTION

In Forced selection, the selected input clock is set by the T0_INPUT_SEL[3:0] bits. The results of input clocks quality monitoring (refer to [Chapter 3.5 Input Clock Quality Monitoring](#)) do not affect the input clock selection.

3.6.3 AUTOMATIC SELECTION

In Automatic selection, the input clock selection is determined by its validity and priority. The validity depends on the results of input clock quality monitoring (refer to [Chapter 3.5 Input Clock Quality Monitoring](#)). In all the qualified input clocks, the one with the highest priority is

selected. The priority is configured by the corresponding INn_CMOS_SEL_PRIORITY[3:0] bits (n = 3). If more than one qualified input clock is available and has the same priority, the input clock with the smallest 'n' is selected. See [Table 8](#) for the 'n' assigned to the input clock.

Table 8: 'n' Assigned to the Input Clock

| Input Clock | 'n' Assigned to the Input Clock |
|-------------|---------------------------------|
| IN1_DIFF | 2 |
| IN2_DIFF | 4 |
| IN3_CMOS | 5 |

Table 9: Related Bit / Register in Chapter 3.6

| Bit | Register | Address (Hex) |
|---|--------------------------------|---------------|
| EXT_SW | MON_SW_PBO_CNFG | 0B |
| T0_INPUT_SEL[3:0] | T0_INPUT_SEL_CNFG | 50 |
| INn_CMOS_SEL_PRIORITY[3:0] (n = 3) | IN3_CMOS_SEL_PRIORITY_CNFG | 2A |
| INn_DIFF_SEL_PRIORITY[3:0] (n = 1 or 2) | IN1_IN2_DIFF_SEL_PRIORITY_CNFG | 28 |

3.7 SELECTED INPUT CLOCK MONITORING

The quality of the selected input clock is always monitored (refer to [Chapter 3.5 Input Clock Quality Monitoring](#)) and the DPLL locking status is always monitored.

3.7.1 DPLL LOCKING DETECTION

The following events is always monitored:

- Fast Loss;
- Coarse Phase Loss;
- Fine Phase Loss;
- Hard Limit Exceeding.

3.7.1.1 Fast Loss

A fast loss is triggered when the selected input clock misses 2 consecutive clock cycles. It is cleared once an active clock edge is detected.

The occurrence of the fast loss will result in T0 DPLL unlocked if the FAST_LOS_SW bit is '1'.

3.7.1.2 Coarse Phase Loss

The T0 DPLL compares the selected input clock with the feedback signal. If the phase-compared result exceeds the coarse phase limit, a coarse phase loss is triggered. It is cleared once the phase-compared result is within the coarse phase limit.

When the selected input clock is of 2 kHz, 4 kHz or 8 kHz, the coarse phase limit depends on the MULTI_PH_8K_4K_2K_EN bit, the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to [Table 10](#). When the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to [Table 11](#).

Table 10: Coarse Phase Limit Programming (the selected input clock of 2 kHz, 4 kHz or 8 kHz)

| MULTI_PH_8K_4K_2K_EN | WIDE_EN | Coarse Phase Limit |
|----------------------|------------|---|
| 0 | don't-care | ±1 UI |
| 1 | 0 | ±1 UI |
| | 1 | set by the PH_LOS_COARSE_LIMT[3:0] bits |

Table 11: Coarse Phase Limit Programming (the selected input clock of other than 2 kHz, 4 kHz and 8 kHz)

| WIDE_EN | Coarse Phase Limit |
|---------|---|
| 0 | ±1 UI |
| 1 | set by the PH_LOS_COARSE_LIMT[3:0] bits |

The occurrence of the coarse phase loss will result in T0 DPLL unlocked if the COARSE_PH_LOS_LIMT_EN bit is '1'.

3.7.1.3 Fine Phase Loss

The T0 DPLL compares the selected input clock with the feedback signal. If the phase-compared result exceeds the fine phase limit programmed by the PH_LOS_FINE_LIMT[2:0] bits, a fine phase loss is triggered. It is cleared once the phase-compared result is within the fine phase limit.

The occurrence of the fine phase loss will result in T0 DPLL unlocked if the FINE_PH_LOS_LIMT_EN bit is '1'.

3.7.1.4 Hard Limit Exceeding

Two limits are available for this monitoring. They are DPLL soft limit and DPLL hard limit. When the frequency of the DPLL output with respect to the master clock exceeds the DPLL soft / hard limit, a DPLL soft / hard alarm will be raised; the alarm is cleared once the frequency is within the corresponding limit. The occurrence of the DPLL soft alarm does not affect the T0 DPLL locking status. The DPLL soft alarm is indicated by the corresponding T0_DPLL_SOFT_FREQ_ALARM bit. The occurrence of the DPLL hard alarm will result in T0 DPLL unlocked if the FREQ_LIMT_PH_LOS bit is '1'.

The DPLL soft limit is set by the DPLL_FREQ_SOFT_LIMT[6:0] bits and can be calculated as follows:

$$DPLL \text{ Soft Limit (ppm)} = DPLL_FREQ_SOFT_LIMT[6:0] \times 0.724$$

The DPLL hard limit is set by the DPLL_FREQ_HARD_LIMT[15:0] bits and can be calculated as follows:

$$DPLL \text{ Hard Limit (ppm)} = DPLL_FREQ_HARD_LIMT[15:0] \times 0.0014$$

3.7.2 LOCKING STATUS

The DPLL locking status depends on the locking monitoring results. The DPLL is in locked state if none of the following events is triggered during 2 seconds; otherwise, the DPLL is unlocked.

- Fast Loss (the FAST_LOS_SW bit is '1');
- Coarse Phase Loss (the COARSE_PH_LOS_LIMT_EN bit is '1');
- Fine Phase Loss (the FINE_PH_LOS_LIMT_EN bit is '1');
- DPLL Hard Alarm (the FREQ_LIMT_PH_LOS bit is '1').

If the FAST_LOS_SW bit, the COARSE_PH_LOS_LIMT_EN bit, the FINE_PH_LOS_LIMT_EN bit or the FREQ_LIMT_PH_LOS bit is '0', the DPLL locking status will not be affected even if the corresponding event is triggered. If all these bits are '0', the DPLL will be in locked state in 2 seconds.

The DPLL locking status is indicated by the T0_DPLL_LOCK bit.

3.7.3 PHASE LOCK ALARM

A phase lock alarm will be raised when the selected input clock can not be locked in T0 DPLL within a certain period. This period can be calculated as follows:

$$Period \text{ (sec.)} = TIME_OUT_VALUE[5:0] \times MULTI_FACTOR[1:0]$$

The phase lock alarm is indicated by the corresponding INn_CMOS_PH_LOCK_ALARM bit (n = 3) / INn_DIFF_PH_LOCK_ALARM bit (n = 1 or 2).

The phase lock alarm can be cleared by the following two ways, as selected by the PH_ALARM_TIMEOUT bit:

- Be cleared when a '1' is written to the corresponding INn_CMOS_PH_LOCK_ALARM bit / INn_DIFF_PH_LOCK_ALARM bit;
- Be cleared after the period (= $TIME_OUT_VALUE[5:0] \times MULTI_FACTOR[1:0]$ in second) which starts from when the alarm is raised.

The selected input clock with a phase lock alarm is disqualified for T0 DPLL locking.

Table 12: Related Bit / Register in Chapter 3.7

| Bit | Register | Address (Hex) |
|-------------------------------------|--|---------------|
| FAST_LOS_SW | PHASE_LOSS_FINE_LIMIT_CNFG | 5B |
| PH_LOS_FINE_LIMIT[2:0] | | |
| FINE_PH_LOS_LIMIT_EN | | |
| MULTI_PH_8K_4K_2K_EN | PHASE_LOSS_COARSE_LIMIT_CNFG | 5A |
| WIDE_EN | | |
| PH_LOS_COARSE_LIMIT[3:0] | | |
| COARSE_PH_LOS_LIMIT_EN | | |
| T0_DPLL_SOFT_FREQ_ALARM | OPERATING_STS | 52 |
| T0_DPLL_LOCK | | |
| DPLL_FREQ_SOFT_LIMIT[6:0] | DPLL_FREQ_SOFT_LIMIT_CNFG | 65 |
| FREQ_LIMIT_PH_LOS | | |
| DPLL_FREQ_HARD_LIMIT[15:0] | DPLL_FREQ_HARD_LIMIT[15:8]_CNFG, DPLL_FREQ_HARD_LIMIT[7:0]_CNFG | 67, 66 |
| TIME_OUT_VALUE[5:0] | PHASE_ALARM_TIME_OUT_CNFG | 08 |
| MULTI_FACTOR[1:0] | | |
| INn_CMOS_PH_LOCK_ALARM (n = 3) | IN3_CMOS_STS | 47 |
| INn_DIFF_PH_LOCK_ALARM (n = 1 or 2) | IN1_IN2_DIFF_STS | 45 |
| PH_ALARM_TIMEOUT | INPUT_MODE_CNFG | 09 |

3.8 SELECTED INPUT CLOCK SWITCH

If the input clock is selected by External Fast selection or by Forced selection, it can be switched by setting the related registers (refer to [Chapter 3.6.1 External Fast Selection](#) & [Chapter 3.6.2 Forced Selection](#)) any time. In this case, whether the input clock is qualified for DPLL locking does not affect the clock switch.

When the input clock is selected by Automatic selection, the input clock switch depends on its validity and priority. If the current selected input clock is disqualified, a new qualified input clock may be switched to.

3.8.1 INPUT CLOCK VALIDITY

For all the input clocks, the validity depends on the results of input clock quality monitoring (refer to [Chapter 3.5 Input Clock Quality Monitoring](#)). When all of the following conditions are satisfied, the input clock is valid; otherwise, it is invalid.

- No no-activity alarm (the INn_CMOS_NO_ACTIVITY_ALARM / INn_DIFF_NO_ACTIVITY_ALARM bit is '0');
- No frequency hard alarm (the INn_CMOS_FREQ_HARD_ALARM / INn_DIFF_FREQ_HARD_ALARM bit is '0');
- If the IN_NOISE_WINDOW bit is '1', all the edges of the input clock of 2 kHz, 4 kHz or 8 kHz drift inside $\pm 5\%$; if the IN_NOISE_WINDOW bit is '0', this condition is ignored.
- No phase lock alarm, i.e., the INn_CMOS_PH_LOCK_ALARM / INn_DIFF_PH_LOCK bit is '0';
- If the ULTR_FAST_SW bit is '1', the T0 selected input clock misses less than (<) 2 consecutive clock cycles; if the ULTR_FAST_SW bit is '0', this condition is ignored.

The validities of all the input clocks are indicated by the INn_CMOS¹ bit (n = 3) / INn_DIFF¹ bit (n = 1 or 2). When the input clock validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid'), the INn_CMOS² / INn_DIFF² bit will be set. If the INn_CMOS³ / INn_DIFF³ bit is '1', an interrupt will be generated.

When the T0 selected input clock has failed, i.e., the validity of the T0 selected input clock changes from 'valid' to 'invalid', the T0_MAIN_REF_FAILED¹ bit will be set. If the T0_MAIN_REF_FAILED² bit is '1', an interrupt will be generated. This interrupt can also be indicated by hardware - the TDO pin, as determined by the LOS_FLAG_TO_TDO bit. When the TDO pin is used to indicate this interrupt, it will be set high when this interrupt is generated and will remain high until this interrupt is cleared.

3.8.2 SELECTED INPUT CLOCK SWITCH

Revertive and Non-Revertive switches are supported, as selected by the REVERTIVE_MODE bit.

The difference between Revertive and Non-Revertive switches is that whether the selected input clock is switched when another qualified input clock with a higher priority than the current selected input clock is available for selection. In Non-Revertive switch, input clock switch is minimized.

Conditions of the qualified input clocks available for T0 selection are as the following:

- Valid, i.e., the INn_CMOS¹ / INn_DIFF¹ bit is '1';
- Priority enabled, i.e., the corresponding INn_CMOS_SEL_PRIORITY[3:0] / INn_DIFF_SEL_PRIORITY[3:0] bits are not '0000'.

The input clock is disqualified if any of the above conditions is not satisfied.

In summary, the selected input clock can be switched by:

- External Fast selection;
- Forced selection;
- Revertive switch;
- Non-Revertive switch.

3.8.2.1 Revertive Switch

In Revertive switch, the selected input clock is switched when another qualified input clock with a higher priority than the current selected input clock is available.

The selected input clock is switched if any of the following is satisfied:

- The selected input clock is disqualified;
- Another qualified input clock with a higher priority than the selected input clock is available.

A qualified input clock with the highest priority is selected by revertive switch. If more than one qualified input clock is available and has the same priority, the input clock with the smallest 'n' is selected. See [Table 8](#) for the 'n' assigned to each input clock.

3.8.2.2 Non-Revertive Switch

In Non-Revertive switch, the T0 selected input clock is not switched when another qualified input clock with a higher priority than the current selected input clock is available. In this case, the selected input clock is switched and a qualified input clock with the highest priority is selected only when the T0 selected input clock is disqualified. If more than one qualified input clock is available and has the same priority, the input clock with the smallest 'n' is selected. See [Table 8](#) for the 'n' assigned to each input clock.

3.8.3 SELECTED / QUALIFIED INPUT CLOCKS INDICATION

The selected input clock is indicated by the CURRENTLY_SELECTED_INPUT[3:0] bits.

The qualified input clocks with the three highest priorities are indicated by the HIGHEST_PRIORITY_VALIDATED[3:0] bits, the SECOND_HIGHEST_PRIORITY_VALIDATED[3:0] bits and the THIRD_HIGHEST_PRIORITY_VALIDATED[3:0] bits respectively. If more than one input clock has the same priority, the input clock with the smallest 'n' is indicated by the HIGHEST_PRIORITY_VALIDATED[3:0] bits. See [Table 8](#) for the 'n' assigned to the input clock.

When the device is configured in Automatic selection and Revertive switch is enabled, the input clock indicated by the CURRENTLY_SELECTED_INPUT[3:0] bits is the same as the one indi-

cated by the HIGHEST_PRIORITY_VALIDATED[3:0] bits; otherwise, they are not the same.

Table 13: Related Bit / Register in Chapter 3.8

| Bit | Register | Address (Hex) |
|--|--|---------------|
| INn_CMOS ¹ (n = 3) / INn_DIFF ¹ (n = 1 or 2) | INPUT_VALID1_STS, INPUT_VALID2_STS | 4A, 4B |
| INn_CMOS ² (n = 3) / INn_DIFF ² (n = 1 or 2) | INTERRUPTS1_STS, INTERRUPTS2_STS | 0D, 0E |
| INn_CMOS ³ (n = 3) / INn_DIFF ³ (n = 1 or 2) | INTERRUPTS1_ENABLE_CNFG, INTERRUPTS2_ENABLE_CNFG | 10, 11 |
| INn_CMOS_NO_ACTIVITY_ALARM (n = 3) | IN3_CMOS_STS | 47 |
| INn_CMOS_FREQ_HARD_ALARM (n = 3) | | |
| INn_CMOS_PH_LOCK_ALARM (n = 3) | | |
| INn_DIFF_NO_ACTIVITY_ALARM (n = 1 or 2) | IN1_IN2_DIFF_STS | 45 |
| INn_DIFF_FREQ_HARD_ALARM (n = 1 or 2) | | |
| INn_DIFF_PH_LOCK_ALARM (n = 1 or 2) | | |
| IN_NOISE_WINDOW | PHASE_MON_PBO_CNFG | 78 |
| ULTR_FAST_SW | MON_SW_PBO_CNFG | 0B |
| LOS_FLAG_TO_TDO | | |
| T0_MAIN_REF_FAILED ¹ | INTERRUPTS2_STS | 0E |
| T0_MAIN_REF_FAILED ² | INTERRUPTS2_ENABLE_CNFG | 11 |
| REVERTIVE_MODE | INPUT_MODE_CNFG | 09 |
| INn_CMOS_SEL_PRIORITY[3:0] (n = 3) | IN3_CMOS_SEL_PRIORITY_CNFG | 2A |
| INn_DIFF_SEL_PRIORITY[3:0] (n = 1 or 2) | IN1_IN2_DIFF_SEL_PRIORITY_CNFG | 28 |
| CURRENTLY_SELECTED_INPUT[3:0] | PRIORITY_TABLE1_STS | 4E |
| HIGHEST_PRIORITY_VALIDATED[3:0] | | |
| SECOND_HIGHEST_PRIORITY_VALIDATED[3:0] | PRIORITY_TABLE2_STS | 4F |
| THIRD_HIGHEST_PRIORITY_VALIDATED[3:0] | | |

3.9 SELECTED INPUT CLOCK STATUS VS. DPLL OPERATING MODE

T0 DPLL supports three primary operating modes: Free-Run, Locked and Holdover, and three secondary, temporary operating modes: Pre-Locked, Pre-Locked2 and Lost-Phase. The operating mode of T0 DPLL can be switched automatically or by force, as controlled by the T0_OPERATING_MODE[2:0] bits.

When the operating mode is switched by force, the operating mode switch is under external control and the status of the selected input clock takes no effect to the operating mode selection. The forced operating mode switch is applicable for special cases, such as testing.

When the operating mode is switched automatically, the internal state machine for T0 automatically determine the operating mode.

The T0 DPLL operating mode is controlled by the T0_OPERATING_MODE[2:0] bits, as shown in Table 14:

Table 14: T0 DPLL Operating Mode Control

| T0_OPERATING_MODE[2:0] | T0 DPLL Operating Mode |
|------------------------|------------------------|
| 000 | Automatic |
| 001 | Forced - Free-Run |
| 010 | Forced - Holdover |
| 100 | Forced - Locked |
| 101 | Forced - Pre-Locked2 |
| 110 | Forced - Pre-Locked |
| 111 | Forced - Lost-Phase |

When the operating mode is switched automatically, the operation of the internal state machine is shown in Figure 6.

Whether the operating mode is under external control or is switched automatically, the current operating mode is always indicated by the T0_DPLL_OPERATING_MODE[2:0] bits. When the operating mode switches, the T0_OPERATING_MODE¹ bit will be set. If the T0_OPERATING_MODE² bit is '1', an interrupt will be generated.

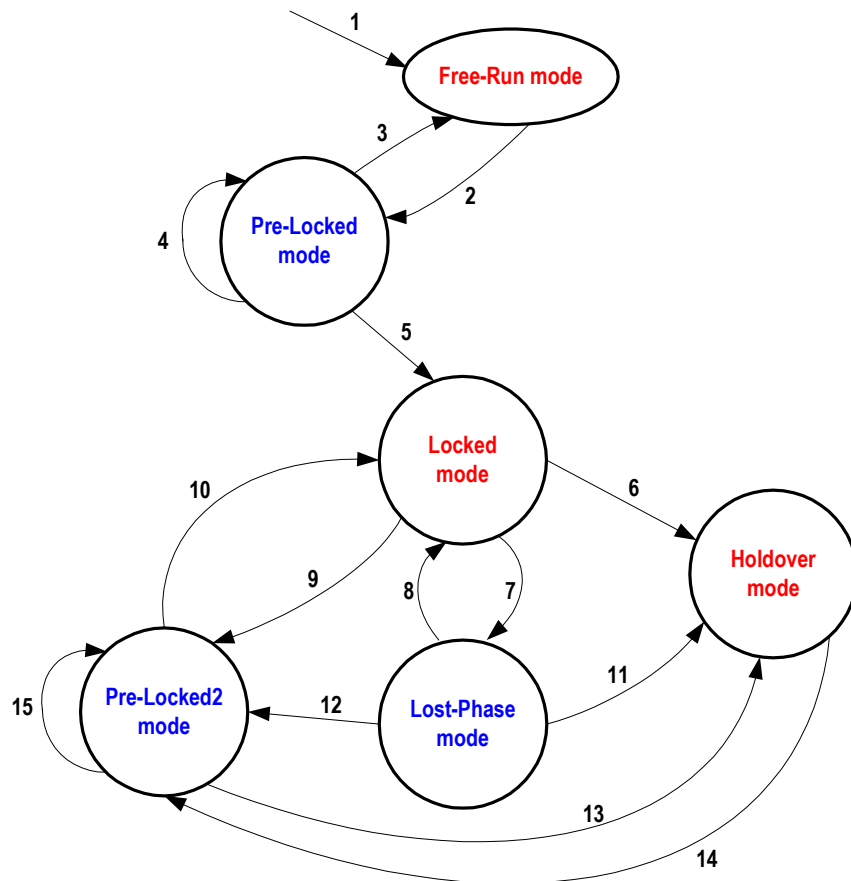


Figure 6. T0 Selected Input Clock vs. DPLL Automatic Operating Mode

Notes to [Figure 6](#):

1. Reset.
2. An input clock is selected.
3. The T0 selected input clock is disqualified **AND** No qualified input clock is available.
4. The T0 selected input clock is switched to another one.
5. The T0 selected input clock is locked (the T0_DPLL_LOCK bit is '1').
6. The T0 selected input clock is disqualified **AND** No qualified input clock is available.
7. The T0 selected input clock is unlocked (the T0_DPLL_LOCK bit is '0').
8. The T0 selected input clock is locked again (the T0_DPLL_LOCK bit is '1').
9. The T0 selected input clock is switched to another one.
10. The T0 selected input clock is locked (the T0_DPLL_LOCK bit is '1').
11. The T0 selected input clock is disqualified **AND** No qualified input clock is available.
12. The T0 selected input clock is switched to another one.
13. The T0 selected input clock is disqualified **AND** No qualified input clock is available.
14. An input clock is selected.
15. The T0 selected input clock is switched to another one.

The causes of Item 4, 9, 12, 15 - 'the T0 selected input clock is switched to another one' - are: (The T0 selected input clock is disqualified **AND** Another input clock is switched to) **OR** (In Revertive switch, a qualified input clock with a higher priority is switched to) **OR** (The T0 selected input clock is switched to another one by External Fast selection or Forced selection).

Refer to [Chapter 3.8.2 Selected Input Clock Switch](#) for details about T0 input clock qualification.

Table 15: Related Bit / Register in Chapter 3.9

| Bit | Register | Address (Hex) |
|--------------------------------|-------------------------|---------------|
| T0_OPERATING_MODE[2:0] | T0_OPERATING_MODE_CNFG | 53 |
| T0_DPLL_OPERATING_MODE[2:0] | OPERATING_STS | 52 |
| T0_DPLL_LOCK | | |
| T0_OPERATING_MODE ¹ | INTERRUPTS2_STS | 0E |
| T0_OPERATING_MODE ² | INTERRUPTS2_ENABLE_CNFG | 11 |

3.10 DPLL OPERATING MODE

The T0 DPLL gives a stable performance in different applications without being affected by operating conditions or silicon process variations. It integrates a PFD (Phase & Frequency Detector), a LPF (Low Pass Filter) and a DCO (Digital Controlled Oscillator), which forms a closed loop. If no input clock is selected, the loop is not closed, and the PFD and LPF do not function.

The PFD detects the phase error, including the fast loss, coarse phase loss and fine phase loss (refer to [Chapter 3.7.1.1 Fast Loss](#) to [Chapter 3.7.1.3 Fine Phase Loss](#)). The averaged phase error of the T0 DPLL feedback with respect to the selected input clock is indicated by the CURRENT_PH_DATA[15:0] bits. It can be calculated as follows:

$$\text{Averaged Phase Error (ns)} = \text{CURRENT_PH_DATA}[15:0] \times 0.61$$

The LPF filters jitters. Its 3 dB bandwidth and damping factor are programmable. A range of bandwidths and damping factors can be set to meet different application requirements. Generally, the lower the damping factor is, the longer the locking time is and the more the gain is.

The DCO controls the DPLL output. The frequency of the DPLL output is always multiplied on the basis of the master clock. The phase and frequency offset of the DPLL output may be locked to those of the selected input clock. The current frequency offset with respect to the master clock is indicated by the CURRENT_DPLL_FREQ[23:0] bits, and can be calculated as follows:

$$\text{Current Frequency Offset (ppm)} = \text{CURRENT_DPLL_FREQ}[23:0] \times 0.000011$$

3.10.1 SIX OPERATING MODES

The T0 DPLL loop is closed except in Free-Run mode and Holdover mode.

For a closed loop, different bandwidths and damping factors can be used depending on DPLL locking stages: starting, acquisition and locked.

In the first two seconds when the T0 DPLL attempts to lock to the selected input clock, the starting bandwidth and damping factor are used. They are set by the T0_DPLL_START_BW[4:0] bits and the T0_DPLL_START_DAMPING[2:0] bits respectively.

During the acquisition, the acquisition bandwidth and damping factor are used. They are set by the T0_DPLL_ACQ_BW[4:0] bits and the T0_DPLL_ACQ_DAMPING[2:0] bits respectively.

When the T0 selected input clock is locked, the locked bandwidth and damping factor are used. They are set by the T0_DPLL_LOCKED_BW[4:0] bits and the T0_DPLL_LOCKED_DAMPING[2:0] bits respectively.

The corresponding bandwidth and damping factor are used when the T0 DPLL operates in different DPLL locking stages: starting, acquisition and locked, as controlled by the device automatically.

Only the locked bandwidth and damping factor can be used regardless of the T0 DPLL locking stage, as controlled by the AUTO_BW_SEL bit.

3.10.1.1 Free-Run Mode

In Free-Run mode, the T0 DPLL output refers to the master clock and is not affected by any input clock. The accuracy of the T0 DPLL output is equal to that of the master clock.

3.10.1.2 Pre-Locked Mode

In Pre-Locked mode, the T0 DPLL output attempts to track the selected input clock.

The Pre-Locked mode is a secondary, temporary mode.

3.10.1.3 Locked Mode

In Locked mode, the T0 selected input clock is locked. The phase and frequency offset of the T0 DPLL output track those of the T0 selected input clock.

In this mode, if the T0 selected input clock is in fast loss status and the FAST_LOS_SW bit is '1', the T0 DPLL is unlocked (refer to [Chapter 3.7.1.1 Fast Loss](#)) and will enter Lost-Phase mode when the operating mode is switched automatically; if the T0 selected input clock is in fast loss status and the FAST_LOS_SW bit is '0', the T0 DPLL locking status is not affected and the T0 DPLL will enter Temp-Holdover mode automatically.

3.10.1.3.1 Temp-Holdover Mode

The T0 DPLL will automatically enter Temp-Holdover mode with a selected input clock switch or no qualified input clock available when the operating mode switch is under external control.

In Temp-Holdover mode, the T0 DPLL has temporarily lost the selected input clock. The T0 DPLL operation in Temp-Holdover mode and that in Holdover mode are alike (refer to [Chapter 3.10.1.5 Holdover Mode](#)) except the frequency offset acquiring methods. See [Chapter 3.10.1.5 Holdover Mode](#) for details about the methods. The method is selected by the TEMP_HOLDOVER_MODE[1:0] bits, as shown in [Table 16](#):

Table 16: Frequency Offset Control in Temp-Holdover Mode

| TEMP_HOLDOVER_MODE[1:0] | Frequency Offset Acquiring Method |
|-------------------------|--|
| 00 | the same as that used in Holdover mode |
| 01 | Automatic Instantaneous |
| 10 | Automatic Fast Averaged |
| 11 | Automatic Slow Averaged |

The device automatically controls the T0 DPLL to exit from Temp-Holdover mode.

3.10.1.4 Lost-Phase Mode

In Lost-Phase mode, the T0 DPLL output attempts to track the selected input clock.

The Lost-Phase mode is a secondary, temporary mode.

3.10.1.5 Holdover Mode

In Holdover mode, the T0 DPLL resorts to the stored frequency data acquired in Locked mode to control its output. The T0 DPLL output is not

phase locked to any input clock. The frequency offset acquiring method is selected by the MAN_HOLD OVER bit, the AUTO_AVG bit and the FAST_AVG bit, as shown in [Table 17](#):

Table 17: Frequency Offset Control in Holdover Mode

| MAN_HOLD OVER | AUTO_AVG | FAST_AVG | Frequency Offset Acquiring Method |
|---------------|------------|------------|-----------------------------------|
| 0 | 0 | don't-care | Automatic Instantaneous |
| | 1 | 0 | Automatic Slow Averaged |
| | | 1 | Automatic Fast Averaged |
| 1 | don't-care | | Manual |

3.10.1.5.1 Automatic Instantaneous

By this method, the T0 DPLL freezes at the operating frequency when it enters Holdover mode. The accuracy is 4.4×10^{-8} ppm.

3.10.1.5.2 Automatic Slow Averaged

By this method, an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3 dB attenuation point corresponding to a period of 110 minutes. The accuracy is 1.1×10^{-5} ppm.

3.10.1.5.3 Automatic Fast Averaged

By this method, an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3 dB attenuation point corresponding to a period of 8 minutes. The accuracy is 1.1×10^{-5} ppm.

3.10.1.5.4 Manual

By this method, the frequency offset is set by the T0_HOLD OVER_FREQ[23:0] bits. The accuracy is 1.1×10^{-5} ppm.

The frequency offset of the T0 DPLL output is indicated by the CURRENT_DPLL_FREQ[23:0] bits.

The device provides a reference for the value to be written to the T0_HOLD OVER_FREQ[23:0] bits. The value to be written can refer to the value read from the CURRENT_DPLL_FREQ[23:0] bits or the T0_HOLD OVER_FREQ[23:0] bits (refer to [Chapter 3.10.1.5.5 Holdover Frequency Offset Read](#)); or then be processed by external software filtering.

3.10.1.5.5 Holdover Frequency Offset Read

The offset value, which is acquired by Automatic Slow Averaged, Automatic Fast Averaged and is set by related register bits, can be read from the T0_HOLD OVER_FREQ[23:0] bits by setting the READ_AVG bit and the FAST_AVG bit, as shown in [Table 18](#).

Table 18: Holdover Frequency Offset Read

| READ_AVG | FAST_AVG | Offset Value Read from T0_HOLD OVER_FREQ[23:0] |
|----------|------------|---|
| 0 | don't-care | The value is equal to the one written to. |
| 1 | 0 | The value is acquired by Automatic Slow Averaged method, not equal to the one written to. |
| | 1 | The value is acquired by Automatic Fast Averaged method, not equal to the one written to. |

The frequency offset in ppm is calculated as follows:

$$\text{Holdover Frequency Offset (ppm)} = T0_HOLD OVER_FREQ[23:0] \times 0.000011$$

3.10.1.6 Pre-Locked2 Mode

In Pre-Locked2 mode, the T0 DPLL output attempts to track the selected input clock.

The Pre-Locked2 mode is a secondary, temporary mode.

Table 19: Related Bit / Register in Chapter 3.10

| Bit | Register | Address (Hex) |
|-----------------------------|---|---------------|
| CURRENT_PH_DATA[15:0] | CURRENT_DPLL_PHASE[15:8]_STS, CURRENT_DPLL_PHASE[7:0]_STS | 69, 68 |
| CURRENT_DPLL_FREQ[23:0] | CURRENT_DPLL_FREQ[23:16]_STS, CURRENT_DPLL_FREQ[15:8]_STS, CURRENT_DPLL_FREQ[7:0]_STS | 64, 63, 62 |
| T0_DPLL_START_BW[4:0] | T0_DPLL_START_BW_DAMPING_CNFG | 56 |
| T0_DPLL_START_DAMPING[2:0] | | |
| T0_DPLL_ACQ_BW[4:0] | T0_DPLL_ACQ_BW_DAMPING_CNFG | 57 |
| T0_DPLL_ACQ_DAMPING[2:0] | | |
| T0_DPLL_LOCKED_BW[4:0] | T0_DPLL_LOCKED_BW_DAMPING_CNFG | 58 |
| T0_DPLL_LOCKED_DAMPING[2:0] | | |
| AUTO_BW_SEL | T0_BW_OVERSHOOT_CNFG | 59 |
| FAST_LOS_SW | PHASE_LOSS_FINE_LIMIT_CNFG | 5B |
| TEMP_HOLDOVER_MODE[1:0] | T0_HOLDOVER_MODE_CNFG | 5C |
| MAN_HOLDOVER | | |
| AUTO_AVG | | |
| FAST_AVG | | |
| READ_AVG | | |
| T0_HOLDOVER_FREQ[23:0] | T0_HOLDOVER_FREQ[23:16]_CNFG, T0_HOLDOVER_FREQ[15:8]_CNFG, T0_HOLDOVER_FREQ[7:0]_CNFG | 5F, 5E, 5D |

3.11 DPLL OUTPUT

The DPLL output is locked to the selected input clock. According to the phase-compared result of the feedback and the selected input clock, and the DPLL output frequency offset, the PFD output is limited and the DPLL output is frequency offset limited.

3.11.1 PFD OUTPUT LIMIT

The PFD output is limited to be within ± 1 UI or within the coarse phase limit (refer to [Chapter 3.7.1.2 Coarse Phase Loss](#)), as determined by the MULTI_PH_APP bit.

3.11.2 FREQUENCY OFFSET LIMIT

The DPLL output is limited to be within the DPLL hard limit (refer to [Chapter 3.7.1.4 Hard Limit Exceeding](#)).

The integral path value can be frozen when the DPLL hard limit is reached. This function, enabled by the T0_LIMT bit, will minimize the subsequent overshoot when T0 DPLL is pulling in.

3.11.3 PBO

When a PBO event is triggered, the phase offset of the selected input clock with respect to the T0 DPLL output is measured. The device then automatically accounts for the measured phase offset and compensates an appropriate phase offset into the DPLL output so that the phase transients on the T0 DPLL output are minimized.

A PBO event is triggered if any one of the following conditions occurs:

- T0 selected input clock switches (the PBO_EN bit is '1');
- T0 DPLL exits from Holdover mode or Free-Run mode (the PBO_EN bit is '1');
- Phase-time changes on the T0 selected input clock are greater than a programmable limit over an interval of less than 0.1 seconds (the PH_MON_PBO_EN bit is '1').

For the first two conditions, the phase transients on the T0 DPLL output are minimized to be no more than 0.61 ns with PBO. The PBO can also be frozen at the current phase offset by setting the PBO_FREZ bit. When the PBO is frozen, the device will ignore any further PBO events triggered by the above two conditions, and maintain the current phase offset. When the PBO is disabled, there may be a phase shift on the T0 DPLL output and the T0 DPLL output tracks back to 0 degree phase offset with respect to the T0 selected input clock.

The last condition is specially for stratum 2 and 3E clocks. The PBO requirement specified in the Telcordia GR-1244-CORE is: 'Input phase-time changes of 3.5 μ s or greater over an interval of less than 0.1 seconds or less shall be built-out by stratum 2 and 3E clocks to reduce the resulting clock phase-time change to less than 50 ns. Phase-time changes of 1.0 μ s or less over an interval of 0.1 seconds shall not be built-out.' Based on this requirement, phase-time changes of more than 1.0 μ s but less than 3.5 μ s that occur over an interval of less than 0.1 seconds may or may not be built-out.

An integrated Phase Transient Monitor can be enabled by the PH_MON_EN bit to monitor the phase-time changes on the T0 selected input clock. When the phase-time changes are greater than a limit over an interval of less than 0.1 seconds, a PBO event is triggered and the phase transients on the DPLL output are absorbed. The limit is programmed by the PH_TR_MON_LIMT[3:0] bits, and can be calculated as follows:

$$\text{Limit (ns)} = (\text{PH_TR_MON_LIMT}[3:0] + 7) \times 156$$

The phase offset induced by PBO will never result in a coarse or fine phase loss.

3.11.4 FOUR PATHS OF T0 DPLL OUTPUTS

The T0 DPLL output are phase aligned with the T0 selected input clock every 125 μ s period. T0 DPLL has four output paths as follows:

- 77.76 MHz path - outputs a 77.76 MHz clock;
- 16E1/16T1 path - outputs a 16E1 or 16T1 clock, as selected by the IN_SONET_SDH bit;
- GSM/OBSAI/16E1/16T1 path - outputs a GSM, OBSAI, 16E1 or 16T1 clock, as selected by the T0_GSM_OBSAI_16E1_16T1_SEL[1:0] bits;
- 12E1/24T1/E3/T3 path - outputs a 12E1, 24T1, E3 or T3 clock, as selected by the T0_12E1_24T1_E3_T3_SEL[1:0] bits.

T0 selected input clock is compared with a T0 DPLL output for DPLL locking. The output can only be derived from the 77.76 MHz path or the 16E1/16T1 path. The output path is automatically selected and the output is automatically divided to get the same frequency as the T0 selected input clock.

T0 DPLL outputs are provided for T0/T4 APLL or device output process.

Table 20: Related Bit / Register in Chapter 3.11

| Bit | Register | Address (Hex) |
|---------------------------------|------------------------------|---------------|
| MULTI_PH_APP | PHASE_LOSS_COARSE_LIMIT_CNFG | 5A |
| T0_LIMIT | T0_BW_OVERSHOOT_CNFG | 59 |
| PBO_EN | MON_SW_PBO_CNFG | 0B |
| PBO_FREZ | | |
| PH_MON_PBO_EN | PHASE_MON_PBO_CNFG | 78 |
| PH_MON_EN | | |
| PH_TR_MON_LIMIT[3:0] | | |
| PH_OFFSET_EN | PHASE_OFFSET[9:8]_CNFG | 7B |
| IN_SONET_SDH | INPUT_MODE_CNFG | 09 |
| T0_GSM_OBSAI_16E1_16T1_SEL[1:0] | T0_DPLL_APLL_PATH_CNFG | 55 |
| T0_12E1_24T1_E3_T3_SEL[1:0] | | |

3.12 T0 / T4 APLL

A T0 APLL and a T4 APLL are provided for a better jitter and wander performance of the device output clocks.

The bandwidths of the T0/T4 APLL are set by the T0_APLL_BW[1:0] / T4_APLL_BW[1:0] bits respectively. The lower the bandwidth is, the better the jitter and wander performance of the T0/T4 APLL output are.

The input of the T0/T4 APLL can be derived from one of the T0 DPLL outputs, as selected by the T0_APLL_PATH[3:0] / T4_APLL_PATH[3:0] bits respectively.

Both the APLL and DPLL outputs are provided for selection for the device output.

Table 21: Related Bit / Register in Chapter 3.12

| Bit | Register | Address (Hex) |
|-------------------|------------------------|---------------|
| T0_APLL_BW[1:0] | T0_T4_APLL_BW_CNFG | 6A |
| T4_APLL_BW[1:0] | | |
| T0_APLL_PATH[3:0] | T0_DPLL_APLL_PATH_CNFG | 55 |
| T4_APLL_PATH[3:0] | T4_APLL_PATH_CNFG | 60 |

3.13 OUTPUT CLOCKS & FRAME SYNC SIGNALS

The device supports 2 output clocks and 2 frame sync output signals altogether.

3.13.1 OUTPUT CLOCKS

The device provides 2 output clocks.

OUT1 outputs a PECL or LVDS signal, as selected by the OUT1_PECL_LVDS bit. OUT2 outputs a CMOS signal.

The outputs on OUT1 and OUT2 are variable, depending on the signals derived from the T0 DPLL and T0/T4 APLL outputs, and the corresponding OUTn_PATH_SEL[3:0] bits (n = 1 or 2). The derived signal can be from the T0 DPLL and T0/T4 APLL outputs, as selected by the corresponding OUTn_PATH_SEL[3:0] bits (n = 1 or 2). If the signal is derived from one of the T0 DPLL outputs, please refer to [Table 22](#) for the output frequency. If the signal is derived from the T0/T4 APLL output, please refer to [Table 23](#) for the output frequency.

The outputs on OUT1 and OUT2 can be inverted, as determined by the corresponding OUTn_INV bit (n = 1 or 2).

Both the output clocks derived from T0 selected input clock are aligned with the T0 selected input clock every 125 μs period.

Table 22: Outputs on OUT1 & OUT2 if Derived from T0 DPLL Outputs

| OUTn_DIVIDER[3:0] (Output Divider) ¹ | outputs on OUT1 & OUT2 if derived from T0 DPLL outputs ² | | | | | | | | |
|--|---|------|------|------|------|----|----|--------------|-------------------|
| | 77.76 MHz | 12E1 | 16E1 | 24T1 | 16T1 | E3 | T3 | GSM (26 MHz) | OBSAI (30.72 MHz) |
| 0000 | Output is disabled (output low). | | | | | | | | |
| 0001 | | | | | | | | | |
| 0010 | | 12E1 | 16E1 | 24T1 | 16T1 | E3 | T3 | | |
| 0011 | | 6E1 | 8E1 | 12T1 | 8T1 | | | 13 MHz | 15.36 MHz |
| 0100 | | 3E1 | 4E1 | 6T1 | 4T1 | | | | |
| 0101 | | 2E1 | | 4T1 | | | | | |
| 0110 | | | 2E1 | 3T1 | 2T1 | | | | |
| 0111 | | E1 | | 2T1 | | | | | |
| 1000 | | | E1 | | T1 | | | | |
| 1001 | | | | T1 | | | | | |
| 1010 | 64 kHz | | | | | | | | |
| 1011 | 8 kHz | | | | | | | | |
| 1100 | 2 kHz | | | | | | | | |
| 1101 | 400 Hz | | | | | | | | |
| 1110 | 1Hz | | | | | | | | |
| 1111 | Output is disabled (output high). | | | | | | | | |

Note:

- n = 1 or 2. Each output is assigned a frequency divider.
- E1 = 2.048 MHz, T1 = 1.544 MHz, E3 = 34.368 MHz, T3 = 44.736 MHz. The blank cell means the configuration is reserved.

Table 23: Outputs on OUT1 & OUT2 if Derived from T0/T4 APLL

| OUTn_DIVIDER[3:0] (Output Divider) ¹ | outputs on OUT1 & OUT2 if derived from T0/T4 APLL output ² | | | | | | | | |
|--|---|----------|----------|----------|----------|----|----|------------------|------------------------|
| | 77.76 MHz X 4 | 12E1 X 4 | 16E1 X 4 | 24T1 X 4 | 16T1 X 4 | E3 | T3 | GSM (26 MHz X 2) | OBSAI (30.72 MHz X 10) |
| 0000 | Output is disabled (output low). | | | | | | | | |
| 0001 | 622.08 MHz ³ | | | | | | | | |
| 0010 | 311.04 MHz ³ | 48E1 | 64E1 | 96T1 | 64T1 | E3 | T3 | 52 MHz | |
| 0011 | 155.52 MHz | 24E1 | 32E1 | 48T1 | 32T1 | | | 26 MHz | 153.6 MHz |
| 0100 | 77.76 MHz | 12E1 | 16E1 | 24T1 | 16T1 | | | 13 MHz | 76.8 MHz |
| 0101 | 51.84 MHz | 8E1 | | 16T1 | | | | | |
| 0110 | 38.88 MHz | 6E1 | 8E1 | 12T1 | 8T1 | | | | 38.4 MHz |
| 0111 | 25.92 MHz | 4E1 | | 8T1 | | | | | |
| 1000 | 19.44 MHz | 3E1 | 4E1 | 6T1 | 4T1 | | | | |
| 1001 | | 2E1 | | 4T1 | | | | | 61.44 MHz ⁴ |
| 1010 | | | 2E1 | 3T1 | 2T1 | | | | 30.72 MHz ⁴ |
| 1011 | 6.48 MHz | E1 | | 2T1 | | | | | 15.36 MHz ⁴ |
| 1100 | | | E1 | | T1 | | | | 7.68 MHz ⁴ |
| 1101 | | | | T1 | | | | | 3.84 MHz ⁴ |
| 1110 | | | | | | | | | |
| 1111 | Output is disabled (output high). | | | | | | | | |

Note:
 1. n = 1 or 2. Each output is assigned a frequency divider.
 2. In the APLL, the selected T0 DPLL output may be multiplied. E1 = 2.048 MHz, T1 = 1.544 MHz, E3 = 34.368 MHz, T3 = 44.736 MHz. The blank cell means the configuration is reserved.
 3. The 622.08 MHz and 311.04 MHz differential signals are only output on OUT1.
 4. The 61.44 MHz, 30.72 MHz, 15.36 MHz, 7.68 MHz and 3.84 MHz outputs are only derived from T0 APLL.

3.13.2 FRAME SYNC OUTPUT SIGNALS

A 2 kHz and an 8 kHz frame sync signals are output on the MFRSYNC_2K and FRSYNC_8K pin if enabled by the 2K_EN and 8K_EN bits respectively. They are CMOS outputs.

The frame sync signals are derived from the T0 APLL output and are aligned with the output clock. They can be synchronized to one of the three frame sync input signals.

One of the three frame sync input signals is selected, as determined by the SYNC_BYPASS bit and the T0 selected input clock, as shown in Table 24:

Table 24: Frame Sync Input Signal Selection

| SYNC_BYPASS | T0 Selected Input Clock | Selected Frame Sync Input Signal |
|-------------|-------------------------|----------------------------------|
| 0 | don't-care | EX_SYNC1 |
| 1 | IN1_DIFF | EX_SYNC1 |
| | IN2_DIFF | EX_SYNC2 |
| | IN3_CMOS | EX_SYNC3 |
| | none | none |

If the selected frame sync input signal with respect to the T0 selected input clock is above a limit set by the SYNC_MON_LIMT[2:0] bits, an external sync alarm will be raised and the selected frame sync input signal is disabled to synchronize the frame sync output signals. The external sync alarm is cleared once the selected frame sync input signal with respect to the T0 selected input clock is within the limit. If it is within the

Table 25: Synchronization Control

| SYNC_BYPASS | AUTO_EXT_SYNC_EN | EXT_SYNC_EN | Synchronization |
|-------------|------------------|-------------|-----------------|
| 0 | don't-care | 0 | Disabled |
| | 0 | 1 | Enabled |
| | 1 | 1 | Disabled |
| 1 | don't-care | | Enabled |

limit, whether the selected frame sync input signal is enabled to synchronize the frame sync output signal is determined by the SYNC_BYPASS bit, the AUTO_EXT_SYNC_EN bit and the EXT_SYNC_EN bit. Refer to Table 25 for details.

When the selected frame sync input signal is enabled to synchronize the frame sync output signal, it should be adjusted to align itself with the T0 selected input clock. Nominally, the falling edge of the selected frame sync input signal is aligned with the rising edge of the T0 selected input clock. The selected frame sync input signal may be 0.5 UI early/late or 1 UI late due to the circuit and board wiring delays. Setting the sampling of the selected frame sync input signal by the SYNC_PHn[1:0] bits (n = 1, 2 or 3 corresponding to EX_SYNC1, EX_SYNC2 or EX_SYNC3 respectively) will compensate this early/late. Refer to Figure 7 to Figure 10.

The EX_SYNC_ALARM_MON bit indicates whether the selected frame sync input signal is in external sync alarm status. The external sync alarm is indicated by the EX_SYNC_ALARM¹ bit. If the EX_SYNC_ALARM² bit is '1', the occurrence of the external sync alarm will trigger an interrupt.

The 8 kHz and the 2 kHz frame sync output signals can be inverted by setting the 8K_INV and 2K_INV bits respectively. The frame sync outputs can be 50:50 duty cycle or pulsed, as determined by the 8K_PUL and 2K_PUL bits respectively. When they are pulsed, the pulse width is defined by the period of OUT2; and they are pulsed on the position of the falling or rising edge of the standard 50:50 duty cycle, as selected by the 2K_8K_PUL_POSITION bit.

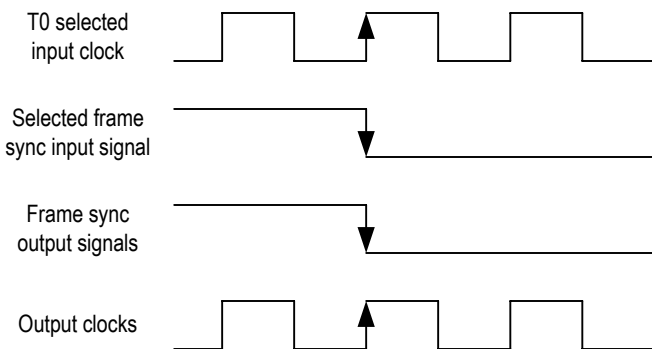


Figure 7. On Target Frame Sync Input Signal Timing

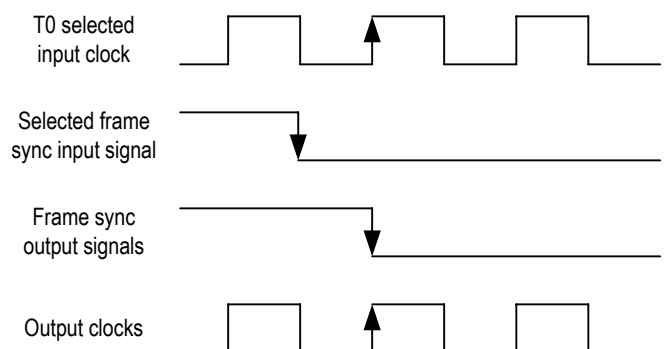


Figure 8. 0.5 UI Early Frame Sync Input Signal Timing

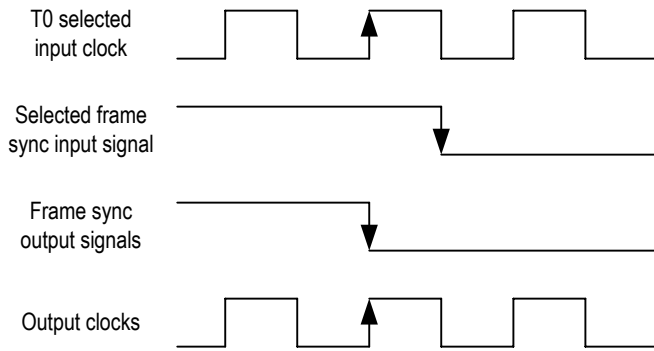


Figure 9. 0.5 UI Late Frame Sync Input Signal Timing

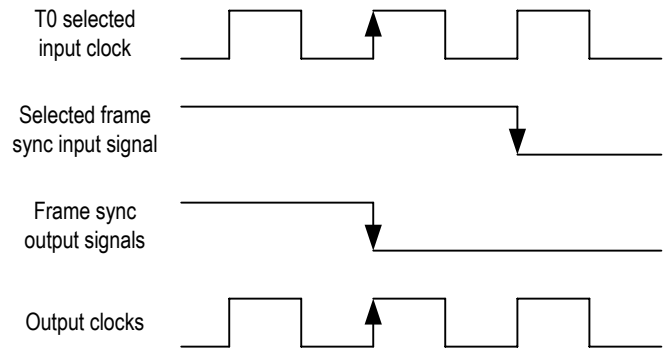


Figure 10. 1 UI Late Frame Sync Input Signal Timing

Table 26: Related Bit / Register in Chapter 3.13

| Bit | Register | Address (Hex) |
|---------------------------------|--------------------------------|---------------|
| OUT1_PECI_LVDS | DIFFERENTIAL_IN_OUT_OSCI_CNFG | 0A |
| OUTn_PATH_SEL[3:0] (n = 1 or 2) | OUT1_FREQ_CNFG, OUT2_FREQ_CNFG | 71, 6D |
| OUTn_DIVIDER[3:0] (n = 1 or 2) | | |
| IN_SONET_SDH | INPUT_MODE_CNFG | 09 |
| AUTO_EXT_SYNC_EN | | |
| EXT_SYNC_EN | | |
| OUTn_INV (n = 1 or 2) | OUT1_INV_CNFG, OUT2_INV_CNFG | 73, 72 |
| 8K_EN | FR_MFR_SYNC_CNFG | 74 |
| 2K_EN | | |
| 8K_INV | | |
| 2K_INV | | |
| 8K_PUL | | |
| 2K_PUL | | |
| 2K_8K_PUL_POSITION | | |
| SYNC_BYPASS | SYNC_MONITOR_CNFG | 7C |
| SYNC_MON_LIMIT[2:0] | | |
| SYNC_PHn[1:0] (n = 1, 2 or 3) | SYNC_PHASE_CNFG | 7D |
| EX_SYNC_ALARM_MON | OPERATING_STS | 52 |
| EX_SYNC_ALARM ¹ | INTERRUPTS3_STS | 0F |
| EX_SYNC_ALARM ² | INTERRUPTS3_ENABLE_CNFG | 12 |

3.14 INTERRUPT SUMMARY

The interrupt sources of the device are as follows:

- T0 Input clocks validity change
- T0 selected input clock fail
- T0 DPLL operating mode switch
- External sync alarm

All of the above interrupt events are indicated by the corresponding interrupt status bit. If the corresponding interrupt enable bit is set, any of the interrupts can be reported by the INT_REQ pin. The output characteristics on the INT_REQ pin are determined by the HZ_EN bit and the INT_POL bit.

Interrupt events are cleared by writing a '1' to the corresponding interrupt status bit. The INT_REQ pin will be inactive only when all the pending enabled interrupts are cleared.

In addition, the interrupt of T0 selected input clock fail can be reported by the TDO pin, as determined by the LOS_FLAG_TO_TDO bit.

Table 27: Related Bit / Register in Chapter 3.14

| Bit | Register | Address (Hex) |
|-----------------|-----------------|---------------|
| HZ_EN | INTERRUPT_CNFG | 0C |
| INT_POL | | |
| LOS_FLAG_TO_TDO | MON_SW_PBO_CNFG | 0B |

3.15 T0 SUMMARY

The main features supported by the T0 path are as follows:

- Phase lock alarm;
- Forced or Automatic input clock selection/switch;
- 3 primary and 3 secondary, temporary DPLL operating modes, switched automatically or under external control;
- Automatic switch between starting, acquisition and locked bandwidths/damping factors;
- Programmable DPLL bandwidths from 0.1 Hz to 560 Hz in 11 steps;
- Programmable damping factors: 1.2, 2.5, 5, 10 and 20;
- Fast loss, coarse phase loss, fine phase loss and hard limit exceeding monitoring;
- Output phase and frequency offset limited;
- Automatic Instantaneous, Automatic Slow Averaged, Automatic Fast Averaged or Manual holdover frequency offset acquiring;
- PBO to minimize output phase transients;
- Programmable output phase offset;
- Low jitter multiple clock outputs with programmable polarity;
- Low jitter 2 kHz and 8 kHz frame sync signal outputs with programmable pulse width and polarity;

3.16 LINE CARD APPLICATION

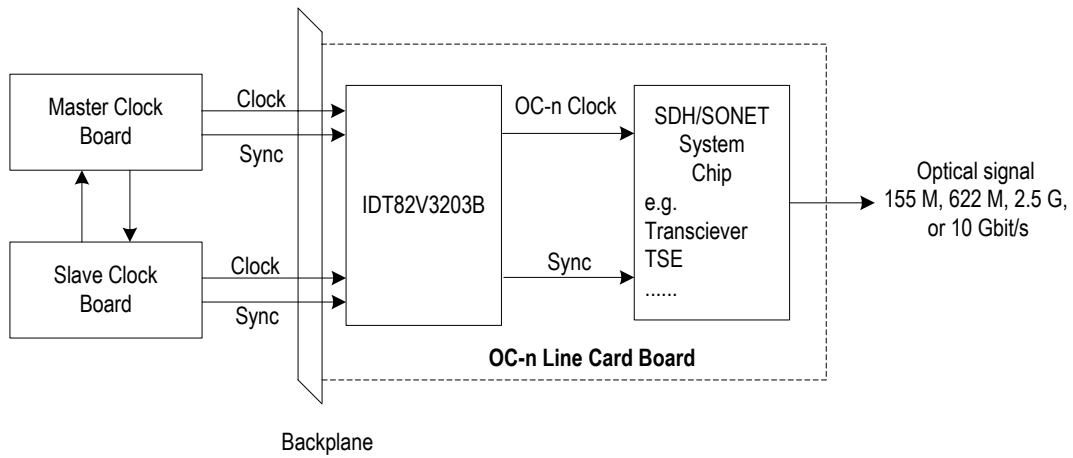


Figure 11. Line Card Application

4 I²C PROGRAMMING INTERFACE

The I²C bus interface provides access to read and write the registers in the IDT82V3203B.

4.1 FUNCTION DESCRIPTION

The timing of a complete data transfer is shown in Figure 12.

The transfer process can be divided into three phases:

- START (S) or repeated START (Sr) condition;
- Byte data transfer condition;
- STOP (P) condition.

The definitions of S/Sr and P conditions are shown in Table 28:

Table 28: Definition of S/Sr and P Conditions

| Condition | Definition |
|-----------|--|
| S/Sr | A high to low transition on the SDA pin while the SCL pin is high. |
| P | A low to high transition on the SDA pin while the SCL pin is high. |

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted in theory. Each byte has to be followed by an acknowledge bit (ACK). So the whole data transfer needs a period of 9 clock cycles. The data is transferred with the most significant bit (MSB) first.

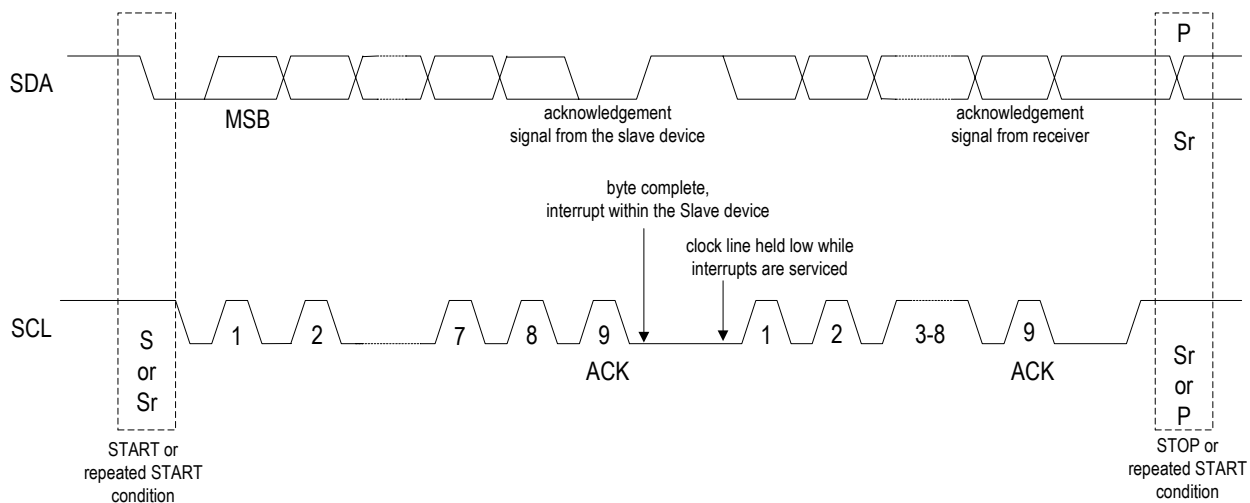


Figure 12. Data Transfer on the I²C-bus

4.1.1 DATA TRANSFER FORMAT

Two kinds of data transfer formats are supported by the IDT82V3203B:

- Slave-receiver mode (Write);
- Slave-transmitter mode (Read);

4.1.1.1 Slave-receiver Mode (Write)

The Slave-receiver mode is as shown in Figure 13.

The Master device asserts the slave address followed by the Write bit. The Slave device acknowledges and the Master device delivers the address byte. The Slave device again acknowledges before the Master device sends the data byte. The Slave device acknowledges each byte, and the entire transaction is finished with a STOP condition.

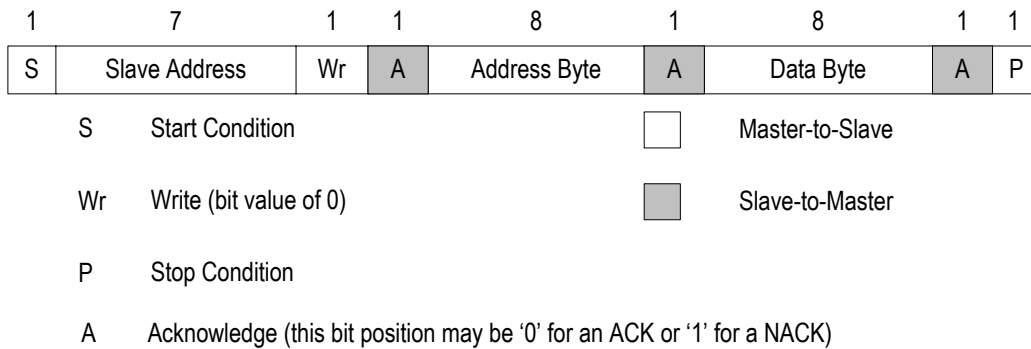


Figure 13. Slave-receiver Mode

4.1.1.2 Slave-transmitter Mode (Read)

The Slave-transmitter mode is as shown in Figure 14.

First the Master device must write an address byte to the slave device. Then it must follow that address byte with a repeated START condition to denote a read from that device's address. The Slave device then returns one byte data corresponding the address. Note that there is no STOP condition before the repeated STRAT condition, and that a no-acknowledge (NACK) signifies the end of the read transfer.

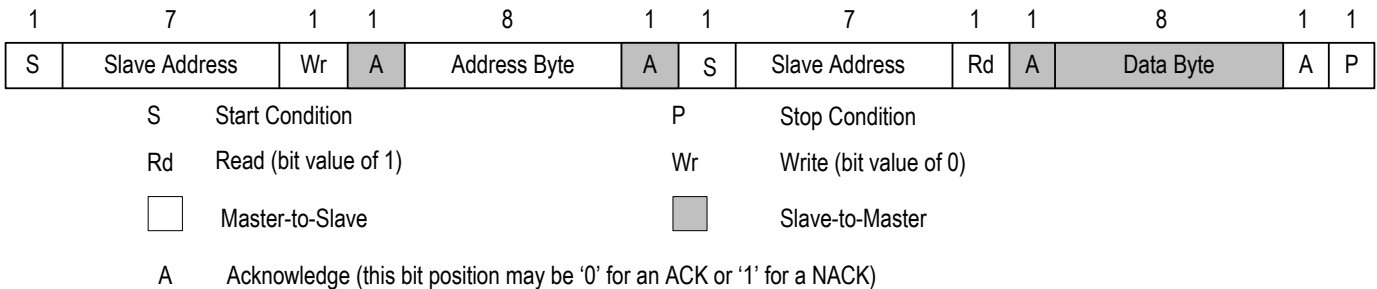


Figure 14. Slave-transmitter Mode

4.1.2 ADDRESS ASSIGNMENT

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|----|----|----|----|-----|-----|-----|-----|
| 1 | 0 | 1 | 0 | AD2 | AD1 | AD0 | 1/0 |

Figure 15. Address Assignment

Each device is recognized by a unique slave address. The slave addressing procedure for the I²C-bus is such that the first byte after the START condition usually determines which slave device will be selected by the Master device. In this specification, the 4 MSB bits of the address byte are fixed and the 3 LSB bits are decided by address input pins AD[2:0], as shown in Figure 15.

The R/W bit is used as a data transfer direction bit which is determined by the Master device. A '0' on this bit indicates a transmission (Write) to registers and a '1' indicates a request for data (Read) from the registers.

4.2 TIMING DEFINITION

The timing of I²C-bus is as shown in Figure 16.

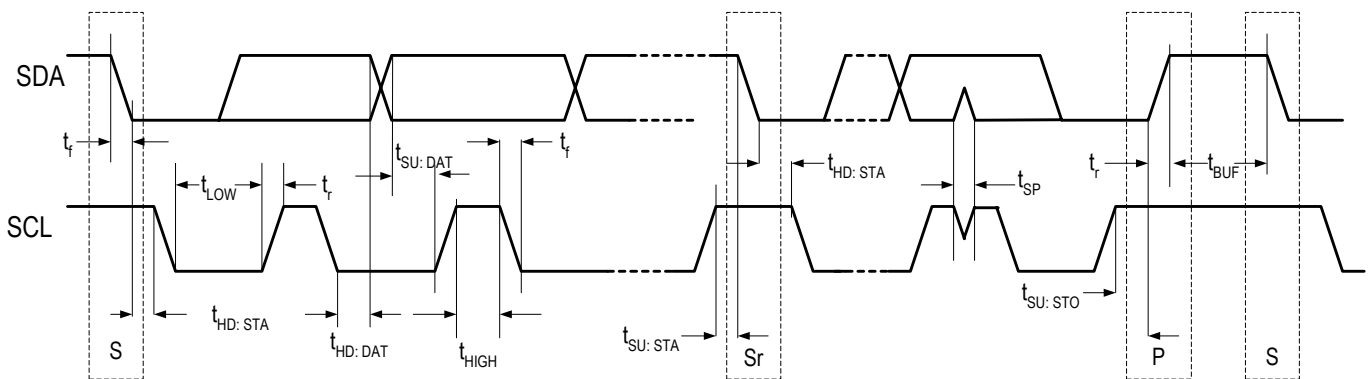


Figure 16. Timing Definition of I²C-bus

Table 29: Timing Definition for Standard Mode and Fast Mode⁽¹⁾

| Symbol | Parameter | Standard Mode | | Fast Mode | | Unit |
|----------------------|---|-------------------------|--------------------------|---------------------------|-------------------------|------|
| | | Min | Max | Min | Max | |
| SCL | Serial clock frequency | 0 | 100 | 0 | 400 | KHz |
| t _{HD; STA} | Hold time (repeated) START condition. After this period, the first clock pulse is generated | 4.0 | - | 0.5 | - | μs |
| t _{LOW} | LOW period of the SCL clock | 4.7 | - | 1.3 | - | μs |
| t _{HIGH} | HIGH period of the SCL clock | 4.0 | - | 0.6 | - | μs |
| t _{SU; STA} | Set-up time for a repeated START condition | 4.7 | - | 0.6 | - | μs |
| t _{HD; DAT} | Data hold time: for CBUS compatible masters for I ² C-bus devices | 5.0 0 ⁽²⁾ | - 3.45 ⁽³⁾ | - 0 ⁽²⁾ | - 0.9 ⁽³⁾ | μs |
| t _{SU; DAT} | Data set-up time | 250 | - | 100 ⁽⁴⁾ | - | ns |
| t _r | Rise time of both SDA and SCL signals | - | 1000 | 20 + 0.1Cb ⁽⁵⁾ | 300 | ns |
| t _f | Fall time of both SDA and SCL signals | - | 300 | 20 + 0.1Cb ⁽⁵⁾ | 300 | ns |
| t _{SU; STO} | Set-up time for STOP condition | 4.0 | - | 0.6 | - | μs |
| t _{BUF} | Bus free time between a STOP and START condition | 4.7 | - | 1.3 | - | μs |
| C _b | Capacitive load for each bus line | - | 400 | - | 400 | pF |
| V _{nL} | Noise margin at the LOW level for each connected device (Including hysteresis) | 0.1VDD | - | 0.1VDD | - | V |
| V _{nH} | Noise margin at the HIGH level for each connected device (Including hysteresis) | 0.2VDD | - | 0.2VDD | - | V |
| t _{sp} | Pulse width of spikes which must be suppressed by the input filter | 0 | 50 | 0 | 50 | ns |

Note:

1. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 37)
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{HD; DAT} has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SU; DAT} ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released.
5. C_b = total capacitance of one bus line in pF. If mixed with Hs-mode device, faster fall-times according to Table 39 allowed.

n/a = not applicable

5 JTAG

This device is compliant with the IEEE 1149.1 Boundary Scan standard except the following:

- The output boundary scan cells do not capture data from the core and the device does not support EXTEST instruction;
- The $\overline{\text{TRST}}$ pin is set low by default and JTAG is disabled in order to be consistent with other manufacturers.

The JTAG interface timing diagram is shown in Figure 17.

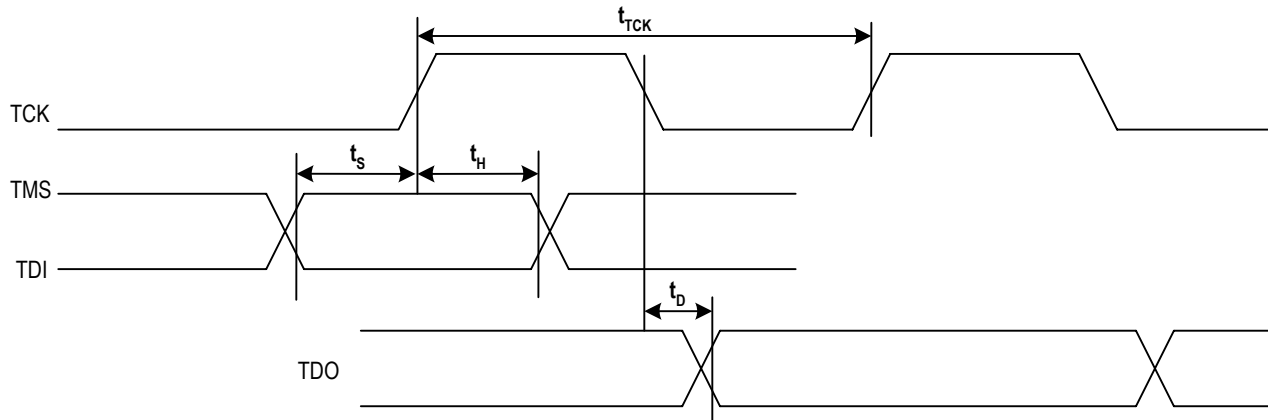


Figure 17. JTAG Interface Timing Diagram

Table 30: JTAG Timing Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------|-----------------------------|-----|-----|-----|------|
| t_{TCK} | TCK period | 100 | | | ns |
| t_s | TMS / TDI to TCK setup time | 25 | | | ns |
| t_H | TCK to TMS / TDI Hold Time | 25 | | | ns |
| t_D | TCK to TDO delay time | | | 50 | ns |

6 PROGRAMMING INFORMATION

After reset, all the registers are set to their default values. The registers are read or written via the microprocessor interface.

Before any write operation, the value in register PROTECTION_CNFG is recommended to be confirmed to make sure whether the write operation is enabled. The device provides 3 register protection modes:

- Protected mode: no other registers can be written except register PROTECTION_CNFG itself;
- Fully Unprotected mode: all the writable registers can be written;
- Single Unprotected mode: one more register can be written besides register PROTECTION_CNFG. After write operation (not including writing a '1' to clear a bit to '0'), the device automatically switches to Protected mode.

Writing '0' to the registers will take no effect if the registers are cleared by writing '1'.

The access of the Multi-word Registers is different from that of the Single-word Registers. Take the registers (04H, 05H and 06H) for an

example, the write operation for the Multi-word Registers follows a fixed sequence. The register (04H) is configured first and the register (06H) is configured last. The three registers are configured continuously and should not be interrupted by any operation. The crystal calibration configuration will take effect after all the three registers are configured. During read operation, the register (04H) is read first and the register (06H) is read last. The crystal calibration reading should be continuous and not be interrupted by any operation.

Certain bit locations within the device register map are designated as Reserved. To ensure proper and predictable operation, bits designated as Reserved should not be written by the users. In addition, their value should be masked out from any testing or error detection methods that are implemented.

6.1 REGISTER MAP

Table 31 is the map of all the registers, sorted in an ascending order of their addresses.

Table 31: Register List and Map

| Address (Hex) | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reference Page |
|---------------------------------|---|---------------------------|------------------------|--------------------------|----------------|--------------|------------------|--------------------|--------------------------|----------------|
| Global Control Registers | | | | | | | | | | |
| 00 | ID[7:0] - Device ID 1 | ID[7:0] | | | | | | | | P 52 |
| 01 | ID[15:8] - Device ID 2 | ID[15:8] | | | | | | | | P 52 |
| 04 | NOMINAL_FREQ[7:0]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 1 | NOMINAL_FREQ_VALUE[7:0] | | | | | | | | P 52 |
| 05 | NOMINAL_FREQ[15:8]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 2 | NOMINAL_FREQ_VALUE[15:8] | | | | | | | | P 53 |
| 06 | NOMINAL_FREQ[23:16]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 3 | NOMINAL_FREQ_VALUE[23:16] | | | | | | | | P 53 |
| 08 | PHASE_ALARM_TIME_OUT_CNFG - Phase Lock Alarm Time-Out Configuration | MULTI_FACTOR[1:0] | | TIME_OUT_VALUE[5:0] | | | | | | P 54 |
| 09 | INPUT_MODE_CNFG - Input Mode Configuration | AUTO_EX T_SYNC_ EN | EXT_SYN C_EN | PH_ALAR M_TIMEO UT | SYNC_FREQ[1:0] | | IN_SONET _SDH | - | REVERTIV E_MODE | P 55 |
| 0A | DIFFERENTIAL_IN_OUT_OSCI_CNFG - Differential Input / Output Port & Master Clock Configuration | - | - | - | - | - | OSC_EDG E | OUT1_PE CL_LVDS | - | P 56 |
| 0B | MON_SW_PBO_CNFG - Frequency Monitor, Input Clock Selection & PBO Control | FREQ_MO N_CLK | LOS_FL G_TO_TD O | ULTR_FAS T_SW | EXT_SW | PBO_FRE Z | PBO_EN | - | FREQ_MO N_HARD_ EN | P 57 |
| 7E | PROTECTION_CNFG - Register Protection Mode Configuration | PROTECTION_DATA[7:0] | | | | | | | | P 58 |
| Interrupt Registers | | | | | | | | | | |
| 0C | INTERRUPT_CNFG - Interrupt Configuration | - | - | - | - | - | - | HZ_EN | INT_POL | P 59 |

Table 31: Register List and Map (Continued)

| Address (Hex) | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reference Page |
|--|--|-----------------------------|----------------------|-----------------|----------------------------|------------------------------|-------|-------------------|----------|----------------|
| 0D | INTERRUPTS1_STS - Interrupt Status 1 | - | - | IN2_DIFF | IN1_DIFF | - | - | - | - | P 59 |
| 0E | INTERRUPTS2_STS - Interrupt Status 2 | T0_OPERATING_MODE | T0_MAIN_REF_FAILED | - | - | - | - | - | IN3_CMOS | P 60 |
| 0F | INTERRUPTS3_STS - Interrupt Status 3 | EX_SYNC_ALARM | - | - | - | - | - | - | - | P 60 |
| 10 | INTERRUPTS1_ENABLE_CNFG - Interrupt Control 1 | - | - | IN2_DIFF | IN1_DIFF | - | - | - | - | P 61 |
| 11 | INTERRUPTS2_ENABLE_CNFG - Interrupt Control 2 | T0_OPERATING_MODE | T0_MAIN_REF_FAILED | - | - | - | - | - | IN3_CMOS | P 61 |
| 12 | INTERRUPTS3_ENABLE_CNFG - Interrupt Control 3 | EX_SYNC_ALARM | - | - | - | - | - | - | - | P 62 |
| Input Clock Frequency & Priority Configuration Registers | | | | | | | | | | |
| 18 | IN1_IN2_DIFF_HF_DIV_CNFG - Differential Input Clock 1 & 2 High Frequency Divider Configuration | IN2_DIFF_DIV[1:0] | | - | - | - | - | IN1_DIFF_DIV[1:0] | | P 63 |
| 19 | IN1_DIFF_CNFG - Differential Input Clock 1 Configuration | DIRECT_DIV | LOCK_8K | BUCKET_SEL[1:0] | | IN_FREQ[3:0] | | | P 64 | |
| 1A | IN2_DIFF_CNFG - Differential Input Clock 2 Configuration | DIRECT_DIV | LOCK_8K | BUCKET_SEL[1:0] | | IN_FREQ[3:0] | | | P 65 | |
| 1D | IN3_CMOS_CNFG - CMOS Input Clock 3 Configuration | DIRECT_DIV | LOCK_8K | BUCKET_SEL[1:0] | | IN_FREQ[3:0] | | | P 66 | |
| 23 | PRE_DIV_CH_CNFG - DivN Divider Channel Selection | - | - | - | - | PRE_DIV_CH_VALUE[3:0] | | | P 67 | |
| 24 | PRE_DIVN[7:0]_CNFG - DivN Divider Division Factor Configuration 1 | PRE_DIVN_VALUE[7:0] | | | | | | | P 67 | |
| 25 | PRE_DIVN[14:8]_CNFG - DivN Divider Division Factor Configuration 2 | - | PRE_DIVN_VALUE[14:8] | | | | | | P 68 | |
| 28 | IN1_IN2_DIFF_SEL_PRIORITY_CNFG - Differential Input Clock 1 & 2 Priority Configuration | IN2_DIFF_SEL_PRIORITY[3:0] | | | IN1_DIFF_SEL_PRIORITY[3:0] | | | P 69 | | |
| 2A | IN3_CMOS_SEL_PRIORITY_CNFG - CMOS Input Clock 3 Priority Configuration | - | - | - | - | IN3_CMOS_SEL_PRIORITY[3:0] | | | P 70 | |
| Input Clock Quality Monitoring Configuration & Status Registers | | | | | | | | | | |
| 2E | FREQ_MON_FACTOR_CNFG - Factor of Frequency Monitor Configuration | - | - | - | - | FREQ_MON_FACTOR[3:0] | | | P 71 | |
| 2F | ALL_FREQ_MON_THRESHOLD_CNFG - Frequency Monitor Threshold for All Input Clocks Configuration | - | - | - | - | ALL_FREQ_HARD_THRESHOLD[3:0] | | | P 71 | |
| 31 | UPPER_THRESHOLD_0_CNFG - Upper Threshold for Leaky Bucket Configuration 0 | UPPER_THRESHOLD_0_DATA[7:0] | | | | | | | P 72 | |
| 32 | LOWER_THRESHOLD_0_CNFG - Lower Threshold for Leaky Bucket Configuration 0 | LOWER_THRESHOLD_0_DATA[7:0] | | | | | | | P 72 | |
| 33 | BUCKET_SIZE_0_CNFG - Bucket Size for Leaky Bucket Configuration 0 | BUCKET_SIZE_0_DATA[7:0] | | | | | | | P 72 | |

Table 31: Register List and Map (Continued)

| Address (Hex) | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reference Page | |
|--|---|-----------------------------|----------------------------------|------------------------------------|----------------------------|----------------------|----------------------------------|------------------------------------|----------------------------|----------------|------|
| 34 | DECAY_RATE_0_CNFG - Decay Rate for Leaky Bucket Configuration 0 | - | - | - | - | - | - | DECAY_RATE_0_DATA [1:0] | | P 73 | |
| 35 | UPPER_THRESHOLD_1_CNFG - Upper Threshold for Leaky Bucket Configuration 1 | UPPER_THRESHOLD_1_DATA[7:0] | | | | | | | | | P 73 |
| 36 | LOWER_THRESHOLD_1_CNFG - Lower Threshold for Leaky Bucket Configuration 1 | LOWER_THRESHOLD_1_DATA[7:0] | | | | | | | | | P 73 |
| 37 | BUCKET_SIZE_1_CNFG - Bucket Size for Leaky Bucket Configuration 1 | BUCKET_SIZE_1_DATA[7:0] | | | | | | | | | P 74 |
| 38 | DECAY_RATE_1_CNFG - Decay Rate for Leaky Bucket Configuration 1 | - | - | - | - | - | - | DECAY_RATE_1_DATA [1:0] | | P 74 | |
| 39 | UPPER_THRESHOLD_2_CNFG - Upper Threshold for Leaky Bucket Configuration 2 | UPPER_THRESHOLD_2_DATA[7:0] | | | | | | | | | P 74 |
| 3A | LOWER_THRESHOLD_2_CNFG - Lower Threshold for Leaky Bucket Configuration 2 | LOWER_THRESHOLD_2_DATA[7:0] | | | | | | | | | P 75 |
| 3B | BUCKET_SIZE_2_CNFG - Bucket Size for Leaky Bucket Configuration 2 | BUCKET_SIZE_2_DATA[7:0] | | | | | | | | | P 75 |
| 3C | DECAY_RATE_2_CNFG - Decay Rate for Leaky Bucket Configuration 2 | - | - | - | - | - | - | DECAY_RATE_2_DATA [1:0] | | P 75 | |
| 3D | UPPER_THRESHOLD_3_CNFG - Upper Threshold for Leaky Bucket Configuration 3 | UPPER_THRESHOLD_3_DATA[7:0] | | | | | | | | | P 76 |
| 3E | LOWER_THRESHOLD_3_CNFG - Lower Threshold for Leaky Bucket Configuration 3 | LOWER_THRESHOLD_3_DATA[7:0] | | | | | | | | | P 76 |
| 3F | BUCKET_SIZE_3_CNFG - Bucket Size for Leaky Bucket Configuration 3 | BUCKET_SIZE_3_DATA[7:0] | | | | | | | | | P 76 |
| 40 | DECAY_RATE_3_CNFG - Decay Rate for Leaky Bucket Configuration 3 | - | - | - | - | - | - | DECAY_RATE_3_DATA [1:0] | | P 77 | |
| 41 | IN_FREQ_READ_CH_CNFG - Input Clock Frequency Read Channel Selection | - | - | - | - | IN_FREQ_READ_CH[3:0] | | | | P 77 | |
| 42 | IN_FREQ_READ_STS - Input Clock Frequency Read Value | IN_FREQ_VALUE[7:0] | | | | | | | | | P 78 |
| 45 | IN1_IN2_DIFF_STS - Differential Input Clock 1 & 2 Status | - | IN2_DIFF_FREQ_HA RD_ALAR M | IN2_DIFF_NO_ACTIV ITY_ALAR M | IN2_DIFF_PH_LOCK _ALARM | - | IN1_DIFF_FREQ_HA RD_ALAR M | IN1_DIFF_NO_ACTIV ITY_ALAR M | IN1_DIFF_PH_LOCK _ALARM | P 78 | |
| 47 | IN3_CMOS_STS - CMOS Input Clock 3 Status | - | - | - | - | - | IN3_CMOS_FREQ_H ARD_ALA RM | IN3_CMOS_NO_ACTI VITY_ALA RM | IN3_CMOS_PH_LOC K_ALARM | P 79 | |
| T0 DPLL Input Clock Selection Registers | | | | | | | | | | | |
| 4A | INPUT_VALID1_STS - Input Clocks Validity 1 | - | - | IN2_DIFF | IN1_DIFF | - | - | - | - | P 80 | |
| 4B | PRIORITY_TABLE1_STS - Priority Status 1 | - | - | - | - | - | - | - | IN3_CMOS | P 81 | |

Table 31: Register List and Map (Continued)

| Address (Hex) | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reference Page |
|---|--|---------------------------------------|-------------|-------------------------|--|-------------------------|-----------------------------|-------|-------|----------------|
| 4E | PRIORITY_TABLE1_STS - Priority Status 1 | HIGHEST_PRIORITY_VALIDATED[3:0] | | | CURRENTLY_SELECTED_INPUT[3:0] | | | | | P 81 |
| 4F | PRIORITY_TABLE2_STS - Priority Status 2 | THIRD_HIGHEST_PRIORITY_VALIDATED[3:0] | | | SECOND_HIGHEST_PRIORITY_VALIDATED[3:0] | | | | | P 82 |
| 50 | T0_INPUT_SEL_CNFG - T0 Selected Input Clock Configuration | - | - | - | - | T0_INPUT_SEL[3:0] | | | P 82 | |
| T0 DPLL State Machine Control Registers | | | | | | | | | | |
| 52 | OPERATING_STS - DPLL Operating Status | EX_SYNC_ALARM_MON | - | T0_DPLL_SOFT_FREQ_ALARM | - | T0_DPLL_LOCK | T0_DPLL_OPERATING_MODE[2:0] | | | P 83 |
| 53 | T0_OPERATING_MODE_CNFG - T0 DPLL Operating Mode Configuration | - | - | - | - | - | T0_OPERATING_MODE[2:0] | | | P 84 |
| T0 DPLL & T0/T4 APLL Configuration Registers | | | | | | | | | | |
| 55 | T0_DPLL_APLL_PATH_CNFG - T0 DPLL & APLL Path Configuration | T0_APLL_PATH[3:0] | | | T0_GSM_OBSAI_16E1_16T1_SEL[1:0] | | T0_12E1_24T1_E3_T3_SEL[1:0] | | | P 85 |
| 56 | T0_DPLL_START_BW_DAMPING_CNFG - T0 DPLL Start Bandwidth & Damping Factor Configuration | T0_DPLL_START_DAMPING[2:0] | | | T0_DPLL_START_BW[4:0] | | | | | P 86 |
| 57 | T0_DPLL_ACQ_BW_DAMPING_CNFG - T0 DPLL Acquisition Bandwidth & Damping Factor Configuration | T0_DPLL_ACQ_DAMPING[2:0] | | | T0_DPLL_ACQ_BW[4:0] | | | | | P 87 |
| 58 | T0_DPLL_LOCKED_BW_DAMPING_CNFG - T0 DPLL Locked Bandwidth & Damping Factor Configuration | T0_DPLL_LOCKED_DAMPING[2:0] | | | T0_DPLL_LOCKED_BW[4:0] | | | | | P 88 |
| 59 | T0_BW_OVERSHOOT_CNFG - T0 DPLL Bandwidth Overshoot Configuration | AUTO_BW_SEL | - | - | - | T0_LIMT | - | - | - | P 88 |
| 5A | PHASE_LOSS_COARSE_LIMIT_CNFG - Phase Loss Coarse Detector Limit Configuration | COARSE_PH_LOS_LIMT_EN | WIDE_EN | MULTI_PH_APP | MULTI_PH_8K_4K_2K_EN | PH_LOS_COARSE_LIMT[3:0] | | | | P 89 |
| 5B | PHASE_LOSS_FINE_LIMIT_CNFG - Phase Loss Fine Detector Limit Configuration | FINE_PH_LOS_LIMT_EN | FAST_LOS_SW | - | - | - | PH_LOS_FINE_LIMT[2:0] | | | P 90 |
| 5C | T0_HOLDOVER_MODE_CNFG - T0 DPLL Holdover Mode Configuration | MAN_HOLDOVER | AUTO_AVG | FAST_AVG | READ_AVG | TEMP_HOLDOVER_MODE[1:0] | | - | - | P 91 |
| 5D | T0_HOLDOVER_FREQ[7:0]_CNFG - T0 DPLL Holdover Frequency Configuration 1 | T0_HOLDOVER_FREQ[7:0] | | | | | | | | P 91 |
| 5E | T0_HOLDOVER_FREQ[15:8]_CNFG - T0 DPLL Holdover Frequency Configuration 2 | T0_HOLDOVER_FREQ[15:8] | | | | | | | | P 92 |
| 5F | T0_HOLDOVER_FREQ[23:16]_CNFG - T0 DPLL Holdover Frequency Configuration 3 | T0_HOLDOVER_FREQ[23:16] | | | | | | | | P 92 |
| 60 | T4_APLL_PATH_CNFG - T4 APLL Path Configuration | T4_APLL_PATH[3:0] | | | | | - | | | P 92 |
| 62 | CURRENT_DPLL_FREQ[7:0]_STS - DPLL Current Frequency Status 1 | CURRENT_DPLL_FREQ[7:0] | | | | | | | | P 93 |
| 63 | CURRENT_DPLL_FREQ[15:8]_STS - DPLL Current Frequency Status 2 | CURRENT_DPLL_FREQ[15:8] | | | | | | | | P 93 |

Table 31: Register List and Map (Continued)

| Address (Hex) | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reference Page | |
|---|--|---------------------------|--------------------------|-----------------|-----------------|---------------------|----------|-----------------|--------|----------------|------|
| 64 | CURRENT_DPLL_FREQ[23:16]_STS - DPLL Current Frequency Status 3 | CURRENT_DPLL_FREQ[23:16] | | | | | | | | P 93 | |
| 65 | DPLL_FREQ_SOFT_LIMIT_CNFG - DPLL Soft Limit Configuration | FREQ_LIM_T_PH_LOS | DPLL_FREQ_SOFT_LIMT[6:0] | | | | | | | | P 94 |
| 66 | DPLL_FREQ_HARD_LIMIT[7:0]_CNFG - DPLL Hard Limit Configuration 1 | DPLL_FREQ_HARD_LIMT[7:0] | | | | | | | | P 94 | |
| 67 | DPLL_FREQ_HARD_LIMIT[15:8]_CNFG - DPLL Hard Limit Configuration 2 | DPLL_FREQ_HARD_LIMT[15:8] | | | | | | | | P 94 | |
| 68 | CURRENT_DPLL_PHASE[7:0]_STS - DPLL Current Phase Status 1 | CURRENT_PH_DATA[7:0] | | | | | | | | P 95 | |
| 69 | CURRENT_DPLL_PHASE[15:8]_STS - DPLL Current Phase Status 2 | CURRENT_PH_DATA[15:8] | | | | | | | | P 95 | |
| 6A | T0_T4_APLL_BW_CNFG - T0 / T4 APLL Bandwidth Configuration | - | - | T0_APLL_BW[1:0] | - | - | - | T4_APLL_BW[1:0] | - | P 95 | |
| Output Configuration Registers | | | | | | | | | | | |
| 6D | OUT2_FREQ_CNFG - Output Clock 2 Frequency Configuration | OUT2_PATH_SEL[3:0] | | | | OUT2_DIVIDER[3:0] | | | | P 96 | |
| 71 | OUT1_FREQ_CNFG - Output Clock 1 Frequency Configuration | OUT1_PATH_SEL[3:0] | | | | OUT1_DIVIDER[3:0] | | | | P 96 | |
| 72 | OUT1_INV_CNFG - Output Clock 1 Invert Configuration | - | - | - | - | - | - | OUT1_INV | - | P 97 | |
| 73 | OUT2_INV_CNFG - Output Clock 2 Invert Configuration | - | - | - | - | - | OUT2_INV | - | - | P 97 | |
| 74 | FR_MFR_SYNC_CNFG - Frame Sync & Multiframe Sync Output Configuration | IN_2K_4K_8K_INV | 8K_EN | 2K_EN | 2K_8K_PUL_POSIT | 8K_INV | 8K_PUL | 2K_INV | 2K_PUL | P 98 | |
| PBO & Phase Offset Control Registers | | | | | | | | | | | |
| 78 | PHASE_MON_PBO_CNFG - Phase Transient Monitor & PBO Configuration | IN_NOISE_WINDOW | - | PH_MON_EN | PH_MON_PBO_EN | PH_TR_MON_LIMT[3:0] | | | | P 99 | |
| Synchronization Configuration Registers | | | | | | | | | | | |
| 7C | SYNC_MONITOR_CNFG - Sync Monitor Configuration | SYNC_BY_PASS | SYNC_MON_LIMT[2:0] | | | - | - | - | - | P 100 | |
| 7D | SYNC_PHASE_CNFG - Sync Phase Configuration | - | - | SYNC_PH3[1:0] | SYNC_PH2[1:0] | SYNC_PH1[1:0] | | | | P 101 | |

6.2 REGISTER DESCRIPTION

6.2.1 GLOBAL CONTROL REGISTERS

ID[7:0] - Device ID 1

| Address: 00H | | | | | | | |
|-------------------------|---------|--|-----|-----|-----|-----|-----|
| Type: Read | | | | | | | |
| Default Value: 10001000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | ID[7:0] | Refer to the description of the ID[15:8] bits (b7~0, 01H). | | | | | |

ID[15:8] - Device ID 2

| Address: 01H | | | | | | | |
|-------------------------|----------|---|------|------|------|-----|-----|
| Type: Read | | | | | | | |
| Default Value: 00010001 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | ID9 | ID8 |
| Bit | Name | Description | | | | | |
| 7 - 0 | ID[15:8] | The value in the ID[15:0] bits are pre-set, representing the identification number for the IDT82V3203B. | | | | | |

NOMINAL_FREQ[7:0]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 1

| Address: 04H | | | | | | | |
|-------------------------|-------------------------|---|---------------------|---------------------|---------------------|---------------------|---------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NOMINAL_FREQ_VALUE7 | NOMINAL_FREQ_VALUE6 | NOMINAL_FREQ_VALUE5 | NOMINAL_FREQ_VALUE4 | NOMINAL_FREQ_VALUE3 | NOMINAL_FREQ_VALUE2 | NOMINAL_FREQ_VALUE1 | NOMINAL_FREQ_VALUE0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | NOMINAL_FREQ_VALUE[7:0] | Refer to the description of the NOMINAL_FREQ_VALUE[23:16] bits (b7~0, 06H). | | | | | |

NOMINAL_FREQ[15:8]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 2

| Address: 05H | | | | | | | |
|-------------------------|--------------------------|---|----------------------|----------------------|----------------------|---------------------|---------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NOMINAL_FREQ_VALUE15 | NOMINAL_FREQ_VALUE14 | NOMINAL_FREQ_VALUE13 | NOMINAL_FREQ_VALUE12 | NOMINAL_FREQ_VALUE11 | NOMINAL_FREQ_VALUE10 | NOMINAL_FREQ_VALUE9 | NOMINAL_FREQ_VALUE8 |
| Bit | Name | Description | | | | | |
| 7 - 0 | NOMINAL_FREQ_VALUE[15:8] | Refer to the description of the NOMINAL_FREQ_VALUE[23:16] bits (b7~0, 06H). | | | | | |

NOMINAL_FREQ[23:16]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 3

| Address: 06H | | | | | | | |
|-------------------------|---------------------------|---|----------------------|----------------------|----------------------|----------------------|----------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NOMINAL_FREQ_VALUE23 | NOMINAL_FREQ_VALUE22 | NOMINAL_FREQ_VALUE21 | NOMINAL_FREQ_VALUE20 | NOMINAL_FREQ_VALUE19 | NOMINAL_FREQ_VALUE18 | NOMINAL_FREQ_VALUE17 | NOMINAL_FREQ_VALUE16 |
| Bit | Name | Description | | | | | |
| 7 - 0 | NOMINAL_FREQ_VALUE[23:16] | <p>The NOMINAL_FREQ_VALUE[23:0] bits represent a 2's complement signed integer. If the value is multiplied by 0.0000884, the calibration value for the master clock in ppm will be gotten.</p> <p>For example, the frequency offset on OSC1 is +3 ppm. Though -3 ppm should be compensated, the calibration value is calculated as +3 ppm:</p> <p>$3 \div 0.0000884 = 33937$ (Dec.) = 8490 (Hex);</p> <p>So '008490' should be written into these bits.</p> <p>The calibration range is within ± 741 ppm.</p> | | | | | |

PHASE_ALARM_TIME_OUT_CNFG - Phase Lock Alarm Time-Out Configuration

| Address: 08H | | | | | | | |
|-------------------------|---------------------|--|---------------------|---------------------|---------------------|---------------------|---------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00110010 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MULTI_FACTO R1 | MULTI_FACTO R0 | TIME_OUT_VA LUE5 | TIME_OUT_VA LUE4 | TIME_OUT_VA LUE3 | TIME_OUT_VA LUE2 | TIME_OUT_VA LUE1 | TIME_OUT_VAL UE0 |
| Bit | Name | Description | | | | | |
| 7 - 6 | MULTI_FACTOR[1:0] | <p>These bits determine a factor which has a relationship with a period in seconds. A phase lock alarm will be raised if the T0 selected input clock is not locked in T0 DPLL within this period. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', the phase lock alarm will be cleared after this period (starting from when the alarm is raised). Refer to the description of the TIME_OUT_VALUE[5:0] bits (b5~0, 08H).</p> <p>00: 2 (default) 01: 4 10: 8 11: 16</p> | | | | | |
| 5 - 0 | TIME_OUT_VALUE[5:0] | <p>These bits represent an unsigned integer. If the value in these bits is multiplied by the value in the MULTI_FACTOR[1:0] bits (b7~6, 08H), a period in seconds will be gotten.</p> <p>A phase lock alarm will be raised if the T0 selected input clock is not locked in T0 DPLL within this period. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', the phase lock alarm will be cleared after this period (starting from when the alarm is raised).</p> | | | | | |

INPUT_MODE_CNFG - Input Mode Configuration

| Address: 09H Type: Read / Write Default Value: 10100X10 | | | | | | | | | | | | | | | | | | | |
|---|------------------|---|------------|------------|--------------|---|----------------|------------------|-------------|-----------------|------------|---|--------------------|---|---|---------|---|---|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | | | | | | | |
| AUTO_EXT_SYNC_EN | EXT_SYNC_EN | PH_ALARM_TIMEOUT | SYNC_FREQ1 | SYNC_FREQ0 | IN_SONET_SDH | - | REVERTIVE_MODE | | | | | | | | | | | | |
| Bit | Name | Description | | | | | | | | | | | | | | | | | |
| 7 | AUTO_EXT_SYNC_EN | This bit is valid only when the SYNC_BYPASS bit (b7, 7CH) is '0'. Refer to the description of the EXT_SYNC_EN bit (b6, 09H). | | | | | | | | | | | | | | | | | |
| 6 | EXT_SYNC_EN | <p>This bit is valid only when the SYNC_BYPASS bit (b7, 7CH) is '0'. This bit, together with the AUTO_EXT_SYNC_EN bit (b7, 09H), determines whether the selected frame sync input signal is enabled to synchronize the frame sync output signals.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>AUTO_EXT_SYNC_EN</th> <th>EXT_SYNC_EN</th> <th>Synchronization</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">don't-care</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Disabled (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Enabled</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Disabled</td> </tr> </tbody> </table> | | | | | | AUTO_EXT_SYNC_EN | EXT_SYNC_EN | Synchronization | don't-care | 0 | Disabled (default) | 0 | 1 | Enabled | 1 | 1 | Disabled |
| AUTO_EXT_SYNC_EN | EXT_SYNC_EN | Synchronization | | | | | | | | | | | | | | | | | |
| don't-care | 0 | Disabled (default) | | | | | | | | | | | | | | | | | |
| 0 | 1 | Enabled | | | | | | | | | | | | | | | | | |
| 1 | 1 | Disabled | | | | | | | | | | | | | | | | | |
| 5 | PH_ALARM_TIMEOUT | <p>This bit determines how to clear the phase lock alarm.</p> <p>0: The phase lock alarm will be cleared when a '1' is written to the corresponding INn_CMOS_PH_LOCK_ALARM bit (n = 1 or 2) (b4/0, 44H).</p> <p>1: The phase lock alarm will be cleared after a period (= $TIME_OUT_VALUE[5:0] (b5\sim 0, 08H) \times MULTI_FACTOR[1:0] (b7\sim 6, 08H)$ in second) which starts from when the alarm is raised. (default)</p> | | | | | | | | | | | | | | | | | |
| 4 - 3 | SYNC_FREQ[1:0] | <p>These bits set the frequency of the frame sync signals input on the EX_SYNC1 ~ EX_SYNC2 pins.</p> <p>00: 8 kHz (default) 01: 8 kHz. 10: 4 kHz. 11: 2 kHz.</p> | | | | | | | | | | | | | | | | | |
| 2 | IN_SONET_SDH | <p>This bit selects the SDH or SONET network type.</p> <p>0: SDH. The DPLL required clock is 2.048 MHz when the IN_FREQ[3:0] bits (b3~0, 16H, 17H) are '0001' and the T0 DPLL output from the 16E1/16T1 path is 16E1.</p> <p>1: SONET. The DPLL required clock is 1.544 MHz when the IN_FREQ[3:0] bits (b3~0, 16H, 17H) are '0001' and the T0 DPLL output from the 16E1/16T1 path is 16T1.</p> <p>The default value of this bit is determined by the SONET/SDH pin during reset.</p> | | | | | | | | | | | | | | | | | |
| 1 | - | Reserved. | | | | | | | | | | | | | | | | | |
| 0 | REVERTIVE_MODE | <p>This bit selects Revertive or Non-Revertive switch.</p> <p>0: Non-Revertive switch. (default) 1: Revertive switch.</p> | | | | | | | | | | | | | | | | | |

DIFFERENTIAL_IN_OUT_OSCI_CNFG - Differential Input / Output Port & Master Clock Configuration

Address: 0AH
 Type: Read / Write
 Default Value: XXXXX00X

| | | | | | | | |
|---|---|---|---|---|----------|----------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | OSC_EDGE | OUT1_PECL_LVDS | - |

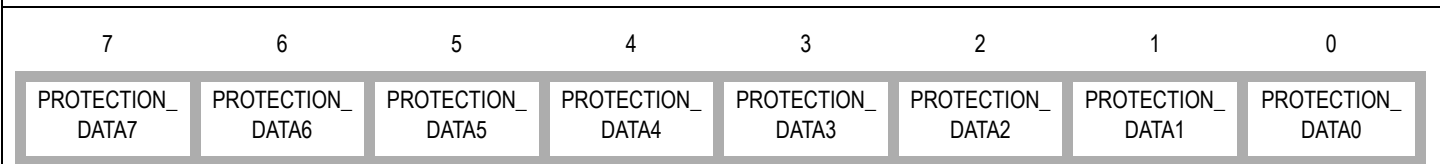
| Bit | Name | Description |
|-------|----------------|---|
| 7 - 3 | - | Reserved. |
| 2 | OSC_EDGE | This bit selects a better active edge of the master clock. 0: The rising edge. (default) 1: The falling edge. |
| 1 | OUT1_PECL_LVDS | This bit selects a port technology for OUT1. 0: LVDS. (default) 1: PECL. |
| 0 | - | Reserved |

MON_SW_PBO_CNFG - Frequency Monitor, Input Clock Selection & PBO Control

| Address: 0BH | | | | | | | |
|-------------------------|------------------|--|--------|----------|--------|---|------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 100X01X1 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FREQ_MON_CLK | LOS_FLAG_TO_TDO | ULTR_FAST_SW | EXT_SW | PBO_FREZ | PBO_EN | - | FREQ_MON_HARD_EN |
| Bit | Name | Description | | | | | |
| 7 | FREQ_MON_CLK | The bit selects a reference clock for input clock frequency monitoring. 0: The output of T0 DPLL. 1: The master clock. (default) | | | | | |
| 6 | LOS_FLAG_TO_TDO | The bit determines whether the interrupt of T0 selected input clock fail - is reported by the TDO pin. 0: Not reported. TDO pin is used as JTAG test data output which complies with IEEE 1149.1. (default) 1: Reported. TDO pin mimics the state of the T0_MAIN_REF_FAILED bit (b6, 0EH) and does not strictly comply with IEEE 1149.1. | | | | | |
| 5 | ULTR_FAST_SW | This bit determines whether the T0 selected input clock is valid when missing 2 consecutive clock cycles or more. 0: Valid. (default) 1: Invalid. | | | | | |
| 4 | EXT_SW | This bit determines the T0 input clock selection. 0: Forced selection or Automatic selection, as controlled by the T0_INPUT_SEL[3:0] bits (b3~0, 50H). 1: External Fast selection. The default value of this bit is determined by the FF_SRCSW pin during reset. | | | | | |
| 3 | PBO_FREZ | This bit is valid only when the PBO is enabled by the PBO_EN bit (b2, 0BH). It determines whether PBO is frozen at the current phase offset when a PBO event is triggered. 0: Not frozen. (default) 1: Frozen. Further PBO events are ignored and the current phase offset is maintained. | | | | | |
| 2 | PBO_EN | This bit determines whether PBO is enabled when the T0 selected input clock switch or the T0 DPLL exiting from Holdover mode or Free-Run mode occurs. 0: Disabled. 1: Enabled. (default) | | | | | |
| 1 | - | Reserved. | | | | | |
| 0 | FREQ_MON_HARD_EN | This bit determines whether the frequency hard alarm is enabled when the frequency of the input clock with respect to the reference clock is above the frequency hard alarm threshold. The reference clock can be the output of T0 DPLL or the master clock, as determined by the FREQ_MON_CLK bit (b7, 0BH). 0: Disabled. 1: Enabled. (default) | | | | | |

PROTECTION_CNFG - Register Protection Mode Configuration

Address: 7EH
 Type: Read / Write
 Default Value: 10000101



| Bit | Name | Description |
|-------|----------------------|--|
| 7 - 0 | PROTECTION_DATA[7:0] | These bits select a register write protection mode. 00000000 - 10000100, 10000111 - 11111111: Protected mode. No other registers can be written except this register. 10000101: Fully Unprotected mode. All the writable registers can be written. (default) 10000110: Single Unprotected mode. One more register can be written besides this register. After write operation (not including writing a '1' to clear the bit to '0'), the device automatically switches to Protected mode. |

6.2.2 INTERRUPT REGISTERS

INTERRUPT_CNFG - Interrupt Configuration

| Address: 0CH | | | | | | | |
|-------------------------|---------|---|---|---|---|-------|---------|
| Type: Read / Write | | | | | | | |
| Default Value: XXXXXX10 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | HZ_EN | INT_POL |
| Bit | Name | Description | | | | | |
| 7 - 2 | - | Reserved. | | | | | |
| 1 | HZ_EN | This bit determines the output characteristics of the INT_REQ pin. 0: The output on the INT_REQ pin is high/low when the interrupt is active; the output is the opposite when the interrupt is inactive. 1: The output on the INT_REQ pin is high/low when the interrupt is active; the output is in high impedance state when the interrupt is inactive. (default) | | | | | |
| 0 | INT_POL | This bit determines the active level on the INT_REQ pin for an active interrupt indication. 0: Active low. (default) 1: Active high. | | | | | |

INTERRUPTS1_STS - Interrupt Status 1

| Address: 0DH | | | | | | | |
|-------------------------|----------|---|----------|---|---|---|---|
| Type: Read / Write | | | | | | | |
| Default Value: XX11XXXX | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | IN2_DIFF | IN1_DIFF | - | - | - | - |
| Bit | Name | Description | | | | | |
| 7 - 6 | - | Reserved. | | | | | |
| 5 - 4 | INn_DIFF | This bit indicates the validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid') for the corresponding INn_DIFF; i.e., whether there is a transition (from '0' to '1' or from '1' to '0') on the corresponding INn_DIFF bit (b5/4, 4AH). Here n is 2 or 1. 0: Has not changed. 1: Has changed. (default) This bit is cleared by writing a '1'. | | | | | |
| 3 - 0 | - | Reserved. | | | | | |

INTERRUPTS2_STS - Interrupt Status 2

| Address: 0EH | | | | | | | |
|-------------------------|--------------------|--|---|---|---|---|----------|
| Type: Read / Write | | | | | | | |
| Default Value: 00XXXXX1 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| T0_OPERATING_MODE | T0_MAIN_REF_FAILED | - | - | - | - | - | IN3_CMOS |
| Bit | Name | Description | | | | | |
| 7 | T0_OPERATING_MODE | This bit indicates the operating mode switch for T0 DPLL; i.e., whether the value in the T0_DPLL_OPERATING_MODE[2:0] bits (b2~0, 52H) changes. 0: Has not switched. (default) 1: Has switched. This bit is cleared by writing a '1'. | | | | | |
| 6 | T0_MAIN_REF_FAILED | This bit indicates whether the T0 selected input clock has failed. The T0 selected input clock fails when its validity changes from 'valid' to 'invalid'; i.e., when there is a transition from '1' to '0' on the corresponding INn_CMOS bit (4AH). 0: Has not failed. (default) 1: Has failed. This bit is cleared by writing a '1'. | | | | | |
| 5 - 1 | - | Reserved. | | | | | |
| 0 | IN3_CMOS | This bit indicates the validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid') for IN3_CMOS for T0 path, i.e., whether there is a transition (from '0' to '1' or from '1' to '0') on the corresponding IN3_CMOS bit (b0, 4BH). 0: Has not changed. 1: Has changed. (default) This bit is cleared by writing a '1'. | | | | | |

INTERRUPTS3_STS - Interrupt Status 3

| Address: 0FH | | | | | | | |
|-------------------------|---------------|---|---|---|---|---|---|
| Type: Read / Write | | | | | | | |
| Default Value: 1XXXXXXX | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EX_SYNC_ALARM | - | - | - | - | - | - | - |
| Bit | Name | Description | | | | | |
| 7 | EX_SYNC_ALARM | This bit indicates whether an external sync alarm is raised; i.e., whether there is a transition from '0' to '1' on the EX_SYNC_ALARM_MON bit (b7, 52H). 0: Has not occurred. 1: Has occurred. (default) This bit is cleared by writing a '1'. | | | | | |
| 6 - 0 | - | Reserved. | | | | | |

INTERRUPTS1_ENABLE_CNFG - Interrupt Control 1

| Address: 10H | | | | | | | |
|-------------------------|----------|---|----------|---|---|---|---|
| Type: Read / Write | | | | | | | |
| Default Value: XX00XXXX | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | IN2_DIFF | IN1_DIFF | - | - | - | - |
| Bit | Name | Description | | | | | |
| 7 - 6 | - | Reserved. | | | | | |
| 5 - 4 | INn_DIFF | This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the input clock validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid'), i.e., when the corresponding INn_DIFF bit (b5/4, 0DH) is '1'. Here n is 2 or 1. 0: Disabled. (default) 1: Enabled. | | | | | |
| 3 - 0 | - | Reserved. | | | | | |

INTERRUPTS2_ENABLE_CNFG - Interrupt Control 2

| Address: 11H | | | | | | | |
|-------------------------|--------------------|---|---|---|---|---|----------|
| Type: Read / Write | | | | | | | |
| Default Value: 00XXXXX0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| T0_OPERATING_MODE | T0_MAIN_REF_FAILED | - | - | - | - | - | IN3_CMOS |
| Bit | Name | Description | | | | | |
| 7 | T0_OPERATING_MODE | This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the T0 DPLL operating mode switches, i.e., when the T0_OPERATING_MODE bit (b7, 0EH) is '1'. 0: Disabled. (default) 1: Enabled. | | | | | |
| 6 | T0_MAIN_REF_FAILED | This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the T0 selected input clock has failed; i.e., when the T0_MAIN_REF_FAILED bit (b6, 0EH) is '1'. 0: Disabled. (default) 1: Enabled. | | | | | |
| 5 - 1 | - | Reserved. | | | | | |
| 0 | IN3_CMOS | This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the input clock validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid'), i.e., when the corresponding IN3_CMOS bit (b0, 0EH) is '1'. 0: Disabled. (default) 1: Enabled. | | | | | |

INTERRUPTS3_ENABLE_CNFG - Interrupt Control 3

Address: 12H
 Type: Read / Write
 Default Value: 0XXXXXXX

| | | | | | | | |
|---------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EX_SYNC_ALARM | - | - | - | - | - | - | - |

| Bit | Name | Description |
|-------|---------------|--|
| 7 | EX_SYNC_ALARM | This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when an external sync alarm has occurred, i.e., when the EX_SYNC_ALARM bit (b7, 0FH) is '1'. 0: Disabled. (default) 1: Enabled. |
| 6 - 0 | - | Reserved. |

6.2.3 INPUT CLOCK FREQUENCY & PRIORITY CONFIGURATION REGISTERS

IN1_IN2_DIFF_HF_DIV_CNFG - Differential Input Clock 1 & 2 High Frequency Divider Configuration

| Address: 18H | | | | | | | |
|-------------------------|-------------------|--|---|---|---|---------------|---------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00XXXX00 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IN2_DIFF_DIV1 | IN2_DIFF_DIV0 | - | - | - | - | IN1_DIFF_DIV1 | IN1_DIFF_DIV0 |
| Bit | Name | Description | | | | | |
| 7 - 6 | IN2_DIFF_DIV[1:0] | These bits determine whether the HF Divider is used and what the division factor is for IN2_DIFF frequency division: 00: Bypassed. (default) 01: Divided by 4. 10: Divided by 5. 11: Reserved. | | | | | |
| 5 - 2 | - | Reserved. | | | | | |
| 1 - 0 | IN1_DIFF_DIV[1:0] | These bits determine whether the HF Divider is used and what the division factor is for IN1_DIFF frequency division: 00: Bypassed. (default) 01: Divided by 4. 10: Divided by 5. 11: Reserved. | | | | | |

IN1_DIFF_CNFG - Differential Input Clock 1 Configuration

Address: 19H
 Type: Read / Write
 Default Value: 00000011



| Bit | Name | Description | | | | | | | | | | | | | | | |
|----------------|-----------------|--|----------------|-------------|--------------|---|---|-------------------------|---|---|-----------------|---|---|--------------|---|---|----------|
| 7 | DIRECT_DIV | Refer to the description of the LOCK_8K bit (b6, 19H). | | | | | | | | | | | | | | | |
| 6 | LOCK_8K | This bit, together with the DIRECT_DIV bit (b7, 19H), determines whether the DivN Divider or the Lock 8k Divider is used for IN1_DIFF: <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">DIRECT_DIV bit</th> <th style="width: 15%;">LOCK_8K bit</th> <th style="width: 70%;">Used Divider</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Both bypassed (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Lock 8k Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">DivN Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Reserved</td> </tr> </tbody> </table> | DIRECT_DIV bit | LOCK_8K bit | Used Divider | 0 | 0 | Both bypassed (default) | 0 | 1 | Lock 8k Divider | 1 | 0 | DivN Divider | 1 | 1 | Reserved |
| DIRECT_DIV bit | LOCK_8K bit | Used Divider | | | | | | | | | | | | | | | |
| 0 | 0 | Both bypassed (default) | | | | | | | | | | | | | | | |
| 0 | 1 | Lock 8k Divider | | | | | | | | | | | | | | | |
| 1 | 0 | DivN Divider | | | | | | | | | | | | | | | |
| 1 | 1 | Reserved | | | | | | | | | | | | | | | |
| 5 - 4 | BUCKET_SEL[1:0] | These bits select one of the four groups of leaky bucket configuration registers for IN1_DIFF: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H. | | | | | | | | | | | | | | | |
| 3 - 0 | IN_FREQ[3:0] | These bits set the DPLL required frequency for IN1_DIFF: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). 0010: 6.48 MHz. 0011: 19.44 MHz. (default) 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011 ~ 1111: Reserved. The required frequency should not be set higher than that of the input clock. | | | | | | | | | | | | | | | |

IN2_DIFF_CNFG - Differential Input Clock 2 Configuration

| Address: 1AH | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------|-----------------|--|-------------|----------|----------|----------|----------|----------------|-------------|--------------|---|---|-------------------------|---|---|-----------------|---|---|--------------|---|---|----------|
| Type: Read / Write | | | | | | | | | | | | | | | | | | | | | | |
| Default Value: 00000011 | | | | | | | | | | | | | | | | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | | | | | | | | | | |
| DIRECT_DIV | LOCK_8K | BUCKET_SEL1 | BUCKET_SEL0 | IN_FREQ3 | IN_FREQ2 | IN_FREQ1 | IN_FREQ0 | | | | | | | | | | | | | | | |
| Bit | Name | Description | | | | | | | | | | | | | | | | | | | | |
| 7 | DIRECT_DIV | Refer to the description of the LOCK_8K bit (b6, 1AH). | | | | | | | | | | | | | | | | | | | | |
| 6 | LOCK_8K | <p>This bit, together with the DIRECT_DIV bit (b7, 1AH), determines whether the DivN Divider or the Lock 8k Divider is used for IN2_DIFF:</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DIRECT_DIV bit</th> <th>LOCK_8K bit</th> <th>Used Divider</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Both bypassed (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Lock 8k Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">DivN Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Reserved</td> </tr> </tbody> </table> | | | | | | DIRECT_DIV bit | LOCK_8K bit | Used Divider | 0 | 0 | Both bypassed (default) | 0 | 1 | Lock 8k Divider | 1 | 0 | DivN Divider | 1 | 1 | Reserved |
| DIRECT_DIV bit | LOCK_8K bit | Used Divider | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | Both bypassed (default) | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Lock 8k Divider | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | DivN Divider | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Reserved | | | | | | | | | | | | | | | | | | | | |
| 5 - 4 | BUCKET_SEL[1:0] | <p>These bits select one of the four groups of leaky bucket configuration registers for IN2_DIFF:</p> <p>00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default)</p> <p>01: Group 1; the addresses of the configuration registers are 35H ~ 38H.</p> <p>10: Group 2; the addresses of the configuration registers are 39H ~ 3CH.</p> <p>11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.</p> | | | | | | | | | | | | | | | | | | | | |
| 3 - 0 | IN_FREQ[3:0] | <p>These bits set the DPLL required frequency for IN2_DIFF:</p> <p>0000: 8 kHz.</p> <p>0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0').</p> <p>0010: 6.48 MHz.</p> <p>0011: 19.44 MHz. (default)</p> <p>0100: 25.92 MHz.</p> <p>0101: 38.88 MHz.</p> <p>0110 ~ 1000: Reserved.</p> <p>1001: 2 kHz.</p> <p>1010: 4 kHz.</p> <p>1011 ~ 1111: Reserved.</p> <p>For IN2_DIFF, the required frequency should not be set higher than that of the input clock.</p> | | | | | | | | | | | | | | | | | | | | |

IN3_CMOS_CNFG - CMOS Input Clock 3 Configuration

Address: 1DH
 Type: Read / Write
 Default Value: 00000011



| Bit | Name | Description | | | | | | | | | | | | | | | |
|----------------|-----------------|--|----------------|-------------|--------------|---|---|-------------------------|---|---|-----------------|---|---|--------------|---|---|----------|
| 7 | DIRECT_DIV | Refer to the description of the LOCK_8K bit (b6, 1DH). | | | | | | | | | | | | | | | |
| 6 | LOCK_8K | This bit, together with the DIRECT_DIV bit (b7, 1DH), determines whether the DivN Divider or the Lock 8k Divider is used for IN3_CMOS: <table border="1" style="margin-left: 20px; border-collapse: collapse; width: 60%;"> <thead> <tr> <th>DIRECT_DIV bit</th> <th>LOCK_8K bit</th> <th>Used Divider</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Both bypassed (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Lock 8k Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">DivN Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Reserved</td> </tr> </tbody> </table> | DIRECT_DIV bit | LOCK_8K bit | Used Divider | 0 | 0 | Both bypassed (default) | 0 | 1 | Lock 8k Divider | 1 | 0 | DivN Divider | 1 | 1 | Reserved |
| DIRECT_DIV bit | LOCK_8K bit | Used Divider | | | | | | | | | | | | | | | |
| 0 | 0 | Both bypassed (default) | | | | | | | | | | | | | | | |
| 0 | 1 | Lock 8k Divider | | | | | | | | | | | | | | | |
| 1 | 0 | DivN Divider | | | | | | | | | | | | | | | |
| 1 | 1 | Reserved | | | | | | | | | | | | | | | |
| 5 - 4 | BUCKET_SEL[1:0] | These bits select one of the four groups of leaky bucket configuration registers for IN3_CMOS: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H. | | | | | | | | | | | | | | | |
| 3 - 0 | IN_FREQ[3:0] | These bits set the DPLL required frequency for IN3_CMOS: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). 0010: 6.48 MHz. 0011: 19.44 MHz. (default) 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011 ~ 1111: Reserved. For IN3_CMOS, the required frequency should not be set higher than that of the input clock. | | | | | | | | | | | | | | | |

PRE_DIV_CH_CNFG - DivN Divider Channel Selection

| Address: 23H | | | | | | | |
|-------------------------|-----------------------|---|---|-------------------|-------------------|-------------------|-------------------|
| Type: Read / Write | | | | | | | |
| Default Value: XXXX0000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | PRE_DIV_CH_VALUE3 | PRE_DIV_CH_VALUE2 | PRE_DIV_CH_VALUE1 | PRE_DIV_CH_VALUE0 |
| Bit | Name | Description | | | | | |
| 7 - 4 | - | Reserved. | | | | | |
| 3 - 0 | PRE_DIV_CH_VALUE[3:0] | <p>This register is an indirect address register for Register 24H and 25H.</p> <p>These bits select an input clock. The value set in the PRE_DIVN_VALUE[14:0] bits (25H, 24H) is available for the selected input clock.</p> <p>0000: Reserved. (default)</p> <p>0001 ~ 0100: Reserved.</p> <p>0101: IN1_DIFF.</p> <p>0110: IN2_DIFF.</p> <p>0111, 1000: Reserved.</p> <p>1001: IN3_CMOS.</p> <p>1010 ~ 1111: Reserved.</p> | | | | | |

PRE_DIVN[7:0]_CNFG - DivN Divider Division Factor Configuration 1

| Address: 24H | | | | | | | |
|-------------------------|---------------------|--|---------------------|---------------------|---------------------|---------------------|---------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PRE_DIVN_VA LUE7 | PRE_DIVN_VA LUE6 | PRE_DIVN_VA LUE5 | PRE_DIVN_VA LUE4 | PRE_DIVN_VA LUE3 | PRE_DIVN_VA LUE2 | PRE_DIVN_VA LUE1 | PRE_DIVN_VA LUE0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | PRE_DIVN_VALUE[7:0] | Refer to the description of the PRE_DIVN_VALUE[14:8] bits (b6~0, 25H). | | | | | |

PRE_DIVN[14:8]_CNFG - DivN Divider Division Factor Configuration 2

| Address: 25H | | | | | | | |
|-------------------------|----------------------|--|----------------------|----------------------|----------------------|---------------------|---------------------|
| Type: Read / Write | | | | | | | |
| Default Value: X0000000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | PRE_DIVN_VAL UE14 | PRE_DIVN_VAL UE13 | PRE_DIVN_VAL UE12 | PRE_DIVN_VAL UE11 | PRE_DIVN_VAL UE10 | PRE_DIVN_VAL UE9 | PRE_DIVN_VAL UE8 |
| Bit | Name | Description | | | | | |
| 7 | - | Reserved. | | | | | |
| 6 - 0 | PRE_DIVN_VALUE[14:8] | <p>If the value in the PRE_DIVN_VALUE[14:0] bits is plus 1, the division factor for an input clock will be gotten. The input clock is selected by the PRE_DIV_CH_VALUE[3:0] bits (b3~0, 23H). A value from '0' to '4BEF' (Hex) can be written into, corresponding to a division factor from 1 to 19440. The others are reserved. So the DivN Divider only supports an input clock whose frequency is lower than (<) 155.52 MHz.</p> <p>The division factor setting should observe the following order: 1. Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits; 2. Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.</p> | | | | | |

IN1_IN2_DIFF_SEL_PRIORITY_CNFG - Differential Input Clock 1 & 2 Priority Configuration

| Address: 28H | | | | | | | |
|-------------------------|----------------------------|--|------------------------|------------------------|------------------------|------------------------|------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IN2_DIFF_SEL_PRIORITY3 | IN2_DIFF_SEL_PRIORITY2 | IN2_DIFF_SEL_PRIORITY1 | IN2_DIFF_SEL_PRIORITY0 | IN1_DIFF_SEL_PRIORITY3 | IN1_DIFF_SEL_PRIORITY2 | IN1_DIFF_SEL_PRIORITY1 | IN1_DIFF_SEL_PRIORITY0 |
| Bit | Name | Description | | | | | |
| 7 - 4 | IN2_DIFF_SEL_PRIORITY[3:0] | These bits set the priority of the corresponding IN2_DIFF. 0000: Disable IN2_DIFF for automatic selection. (default) 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15. | | | | | |
| 3 - 0 | IN1_DIFF_SEL_PRIORITY[3:0] | These bits set the priority of the corresponding IN1_DIFF. 0000: Disable IN1_DIFF for automatic selection. (default) 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15. | | | | | |

IN3_CMOS_SEL_PRIORITY_CNFG - CMOS Input Clock 3 Priority Configuration

| Address: 2AH | | | | | | | |
|-------------------------|----------------------------|---|---|----------------------------|----------------------------|----------------------------|----------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: XXXX0100 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | IN3_CMOS_SE L_PRIORITY3 | IN3_CMOS_SE L_PRIORITY2 | IN3_CMOS_SE L_PRIORITY1 | IN3_CMOS_SE L_PRIORITY0 |
| Bit | Name | Description | | | | | |
| 7 - 4 | - | Reserved. | | | | | |
| 3 - 0 | IN3_CMOS_SEL_PRIORITY[3:0] | <p>These bits set the priority of the corresponding IN3_CMOS.</p> <p>0000: Disable IN3_CMOS for automatic selection.</p> <p>0001: Priority 1.</p> <p>0010: Priority 2.</p> <p>0011: Priority 3.</p> <p>0100: Priority 4. (default)</p> <p>0101: Priority 5.</p> <p>0110: Priority 6.</p> <p>0111: Priority 7.</p> <p>1000: Priority 8.</p> <p>1001: Priority 9.</p> <p>1010: Priority 10.</p> <p>1011: Priority 11.</p> <p>1100: Priority 12.</p> <p>1101: Priority 13.</p> <p>1110: Priority 14.</p> <p>1111: Priority 15.</p> | | | | | |

6.2.4 INPUT CLOCK QUALITY MONITORING CONFIGURATION & STATUS REGISTERS

FREQ_MON_FACTOR_CNFG - Factor of Frequency Monitor Configuration

| Address: 2EH | | | | | | | |
|-------------------------|----------------------|---|---|----------------------|----------------------|----------------------|----------------------|
| Type: Read / Write | | | | | | | |
| Default Value: XXXX1011 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | FREQ_MON_F ACTOR3 | FREQ_MON_F ACTOR2 | FREQ_MON_F ACTOR1 | FREQ_MON_F ACTOR0 |
| Bit | Name | Description | | | | | |
| 7 - 4 | - | Reserved. | | | | | |
| 3 - 0 | FREQ_MON_FACTOR[3:0] | <p>These bits determine a factor. The factor has a relationship with the frequency hard alarm threshold in ppm (refer to the description of the ALL_FREQ_HARD_THRESHOLD[3:0] bits (b3~0, 2FH)) and with the frequency of the input clock with respect to the master clock in ppm (refer to the description of the IN_FREQ_VALUE[7:0] bits (b7~0, 42H)). The factor represents the accuracy of the frequency monitor and should be set according to the requirements of different applications.</p> <p>0000: 0.0032. 0001: 0.0064. 0010: 0.0127. 0011: 0.0257. 0100: 0.0514. 0101: 0.103. 0110: 0.206. 0111: 0.412. 1000: 0.823. 1001: 1.646. 1010: 3.292. 1011: 3.81. (default) 1100 - 1111: 4.6.</p> | | | | | |

ALL_FREQ_MON_THRESHOLD_CNFG - Frequency Monitor Threshold for All Input Clocks Configuration

| Address: 2FH | | | | | | | |
|-------------------------|------------------------------|--|---|------------------------------|------------------------------|------------------------------|------------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: XXXX0011 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | ALL_FREQ_HARD_ THRESHOLD3 | ALL_FREQ_HARD_ THRESHOLD2 | ALL_FREQ_HARD_ THRESHOLD1 | ALL_FREQ_HARD_ THRESHOLD0 |
| Bit | Name | Description | | | | | |
| 7 - 4 | - | Reserved. | | | | | |
| 3 - 0 | ALL_FREQ_HARD_THRESHOLD[3:0] | <p>These bits represent an unsigned integer. The frequency hard alarm threshold in ppm can be calculated as follows:</p> <p>Frequency Hard Alarm Threshold (ppm) = (ALL_FREQ_HARD_THRESHOLD[3:0] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, 2EH)</p> <p>This threshold is symmetrical about zero.</p> | | | | | |

UPPER_THRESHOLD_0_CNFG - Upper Threshold for Leaky Bucket Configuration 0

| Address: 31H Type: Read / Write Default Value: 00000110 | | | | | | | |
|---|---------------------------------|--|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UPPER_THRE SHOLD_0_DAT A7 | UPPER_THRE SHOLD_0_DAT A6 | UPPER_THRE SHOLD_0_DAT A5 | UPPER_THRE SHOLD_0_DAT A4 | UPPER_THRE SHOLD_0_DAT A3 | UPPER_THRE SHOLD_0_DAT A2 | UPPER_THRE SHOLD_0_DAT A1 | UPPER_THRE SHOLD_0_DAT A0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | UPPER_THRESHOLD_0_DATA[7:0] | These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised. | | | | | |

LOWER_THRESHOLD_0_CNFG - Lower Threshold for Leaky Bucket Configuration 0

| Address: 32H Type: Read / Write Default Value: 00000100 | | | | | | | |
|---|---------------------------------|--|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LOWER_THRE SHOLD_0_DAT A7 | LOWER_THRE SHOLD_0_DAT A6 | LOWER_THRE SHOLD_0_DAT A5 | LOWER_THRE SHOLD_0_DAT A4 | LOWER_THRE SHOLD_0_DAT A3 | LOWER_THRE SHOLD_0_DAT A2 | LOWER_THRE SHOLD_0_DAT A1 | LOWER_THRE SHOLD_0_DAT A0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | LOWER_THRESHOLD_0_DATA[7:0] | These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared. | | | | | |

BUCKET_SIZE_0_CNFG - Bucket Size for Leaky Bucket Configuration 0

| Address: 33H Type: Read / Write Default Value: 00001000 | | | | | | | |
|---|-------------------------|--|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUCKET_SIZE _0_DATA7 | BUCKET_SIZE _0_DATA6 | BUCKET_SIZE _0_DATA5 | BUCKET_SIZE _0_DATA4 | BUCKET_SIZE _0_DATA3 | BUCKET_SIZE _0_DATA2 | BUCKET_SIZE _0_DATA1 | BUCKET_SIZE _0_DATA0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | BUCKET_SIZE_0_DATA[7:0] | These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected. | | | | | |

DECAY_RATE_0_CNFG - Decay Rate for Leaky Bucket Configuration 0

| Address: 34H | | | | | | | |
|-------------------------|------------------------|---|---|---|---|--------------------|--------------------|
| Type: Read / Write | | | | | | | |
| Default Value: XXXXXX01 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | DECAY_RATE_0_DATA1 | DECAY_RATE_0_DATA0 |
| Bit | Name | Description | | | | | |
| 7 - 2 | - | Reserved. | | | | | |
| 1 - 0 | DECAY_RATE_0_DATA[1:0] | These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected. | | | | | |

UPPER_THRESHOLD_1_CNFG - Upper Threshold for Leaky Bucket Configuration 1

| Address: 35H | | | | | | | |
|---------------------------------|---------------------------------|--|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000110 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UPPER_THRE SHOLD_1_DAT A7 | UPPER_THRE SHOLD_1_DAT A6 | UPPER_THRE SHOLD_1_DAT A5 | UPPER_THRE SHOLD_1_DAT A4 | UPPER_THRE SHOLD_1_DAT A3 | UPPER_THRE SHOLD_1_DAT A2 | UPPER_THRE SHOLD_1_DAT A1 | UPPER_THRE SHOLD_1_DAT A0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | UPPER_THRESHOLD_1_DATA[7:0] | These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised. | | | | | |

LOWER_THRESHOLD_1_CNFG - Lower Threshold for Leaky Bucket Configuration 1

| Address: 36H | | | | | | | |
|---------------------------------|---------------------------------|--|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000100 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LOWER_THRE SHOLD_1_DAT A7 | LOWER_THRE SHOLD_1_DAT A6 | LOWER_THRE SHOLD_1_DAT A5 | LOWER_THRE SHOLD_1_DAT A4 | LOWER_THRE SHOLD_1_DAT A3 | LOWER_THRE SHOLD_1_DAT A2 | LOWER_THRE SHOLD_1_DAT A1 | LOWER_THRE SHOLD_1_DAT A0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | LOWER_THRESHOLD_1_DATA[7:0] | These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared. | | | | | |

BUCKET_SIZE_1_CNFG - Bucket Size for Leaky Bucket Configuration 1

| Address: 37H | | | | | | | |
|-------------------------|-------------------------|--|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00001000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUCKET_SIZE _1_DATA7 | BUCKET_SIZE _1_DATA6 | BUCKET_SIZE _1_DATA5 | BUCKET_SIZE _1_DATA4 | BUCKET_SIZE _1_DATA3 | BUCKET_SIZE _1_DATA2 | BUCKET_SIZE _1_DATA1 | BUCKET_SIZE _1_DATA0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | BUCKET_SIZE_1_DATA[7:0] | These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected. | | | | | |

DECAY_RATE_1_CNFG - Decay Rate for Leaky Bucket Configuration 1

| Address: 38H | | | | | | | |
|-------------------------|------------------------|---|---|---|---|------------------------|------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: XXXXXX01 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | DECAY_RATE_ 1_DATA1 | DECAY_RATE_ 1_DATA0 |
| Bit | Name | Description | | | | | |
| 7 - 2 | - | Reserved. | | | | | |
| 1 - 0 | DECAY_RATE_1_DATA[1:0] | These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected. | | | | | |

UPPER_THRESHOLD_2_CNFG - Upper Threshold for Leaky Bucket Configuration 2

| Address: 39H | | | | | | | |
|---------------------------------|---------------------------------|--|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000110 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UPPER_THRE SHOLD_2_DAT A7 | UPPER_THRE SHOLD_2_DAT A6 | UPPER_THRE SHOLD_2_DAT A5 | UPPER_THRE SHOLD_2_DAT A4 | UPPER_THRE SHOLD_2_DAT A3 | UPPER_THRE SHOLD_2_DAT A2 | UPPER_THRE SHOLD_2_DAT A1 | UPPER_THRE SHOLD_2_DAT A0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | UPPER_THRESHOLD_2_DATA[7:0] | These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised. | | | | | |

LOWER_THRESHOLD_2_CNFG - Lower Threshold for Leaky Bucket Configuration 2

| Address: 3AH | | | | | | | |
|---------------------------------|---------------------------------|--|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000100 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LOWER_THRE SHOLD_2_DAT A7 | LOWER_THRE SHOLD_2_DAT A6 | LOWER_THRE SHOLD_2_DAT A5 | LOWER_THRE SHOLD_2_DAT A4 | LOWER_THRE SHOLD_2_DAT A3 | LOWER_THRE SHOLD_2_DAT A2 | LOWER_THRE SHOLD_2_DAT A1 | LOWER_THRE SHOLD_2_DAT A0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | LOWER_THRESHOLD_2_DATA[7:0] | These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared. | | | | | |

BUCKET_SIZE_2_CNFG - Bucket Size for Leaky Bucket Configuration 2

| Address: 3BH | | | | | | | |
|-------------------------|-------------------------|--|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00001000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUCKET_SIZE _2_DATA7 | BUCKET_SIZE _2_DATA6 | BUCKET_SIZE _2_DATA5 | BUCKET_SIZE _2_DATA4 | BUCKET_SIZE _2_DATA3 | BUCKET_SIZE _2_DATA2 | BUCKET_SIZE _2_DATA1 | BUCKET_SIZE _2_DATA0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | BUCKET_SIZE_2_DATA[7:0] | These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected. | | | | | |

DECAY_RATE_2_CNFG - Decay Rate for Leaky Bucket Configuration 2

| Address: 3CH | | | | | | | |
|-------------------------|------------------------|---|---|---|---|------------------------|------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: XXXXXX01 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | DECAY_RATE_ 2_DATA1 | DECAY_RATE_ 2_DATA0 |
| Bit | Name | Description | | | | | |
| 7 - 2 | - | Reserved. | | | | | |
| 1 - 0 | DECAY_RATE_2_DATA[1:0] | These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected. | | | | | |

UPPER_THRESHOLD_3_CNFG - Upper Threshold for Leaky Bucket Configuration 3

| Address: 3DH | | | | | | | |
|---------------------------------|---------------------------------|--|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000110 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UPPER_THRE SHOLD_3_DAT A7 | UPPER_THRE SHOLD_3_DAT A6 | UPPER_THRE SHOLD_3_DAT A5 | UPPER_THRE SHOLD_3_DAT A4 | UPPER_THRE SHOLD_3_DAT A3 | UPPER_THRE SHOLD_3_DAT A2 | UPPER_THRE SHOLD_3_DAT A1 | UPPER_THRE SHOLD_3_DAT A0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | UPPER_THRESHOLD_3_DATA[7:0] | These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised. | | | | | |

LOWER_THRESHOLD_3_CNFG - Lower Threshold for Leaky Bucket Configuration 3

| Address: 3EH | | | | | | | |
|---------------------------------|---------------------------------|--|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000100 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LOWER_THRE SHOLD_3_DAT A7 | LOWER_THRE SHOLD_3_DAT A6 | LOWER_THRE SHOLD_3_DAT A5 | LOWER_THRE SHOLD_3_DAT A4 | LOWER_THRE SHOLD_3_DAT A3 | LOWER_THRE SHOLD_3_DAT A2 | LOWER_THRE SHOLD_3_DAT A1 | LOWER_THRE SHOLD_3_DAT A0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | LOWER_THRESHOLD_3_DATA[7:0] | These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared. | | | | | |

BUCKET_SIZE_3_CNFG - Bucket Size for Leaky Bucket Configuration 3

| Address: 3FH | | | | | | | |
|-------------------------|-------------------------|--|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00001000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUCKET_SIZE _3_DATA7 | BUCKET_SIZE _3_DATA6 | BUCKET_SIZE _3_DATA5 | BUCKET_SIZE _3_DATA4 | BUCKET_SIZE _3_DATA3 | BUCKET_SIZE _3_DATA2 | BUCKET_SIZE _3_DATA1 | BUCKET_SIZE _3_DATA0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | BUCKET_SIZE_3_DATA[7:0] | These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected. | | | | | |

DECAY_RATE_3_CNFG - Decay Rate for Leaky Bucket Configuration 3

Address: 40H
 Type: Read / Write
 Default Value: XXXXXX01

| | | | | | | | |
|---|---|---|---|---|---|--------------------|--------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | DECAY_RATE_3_DATA1 | DECAY_RATE_3_DATA0 |

| Bit | Name | Description |
|-------|------------------------|---|
| 7 - 2 | - | Reserved. |
| 1 - 0 | DECAY_RATE_3_DATA[1:0] | These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected. |

IN_FREQ_READ_CH_CNFG - Input Clock Frequency Read Channel Selection

Address: 41H
 Type: Read / Write
 Default Value: XXXX0000

| | | | | | | | |
|---|---|---|---|------------------|------------------|------------------|------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | IN_FREQ_READ_CH3 | IN_FREQ_READ_CH2 | IN_FREQ_READ_CH1 | IN_FREQ_READ_CH0 |

| Bit | Name | Description |
|-------|----------------------|--|
| 7 - 4 | - | Reserved. |
| 3 - 0 | IN_FREQ_READ_CH[3:0] | These bits select an input clock, the frequency of which with respect to the reference clock can be read. 0000: Reserved. (default) 0001 ~ 0100: Reserved. 0101: IN1_DIFF. 0110: IN2_DIFF. 0111, 1000: Reserved. 1001: IN3_CMOS. 1010 ~ 1111: Reserved. |

IN_FREQ_READ_STS - Input Clock Frequency Read Value

| Address: 42H Type: Read Default Value: 00000000 | | | | | | | |
|---|--------------------|--|--------------------|--------------------|--------------------|--------------------|--------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IN_FREQ_VAL UE7 | IN_FREQ_VAL UE6 | IN_FREQ_VAL UE5 | IN_FREQ_VAL UE4 | IN_FREQ_VAL UE3 | IN_FREQ_VAL UE2 | IN_FREQ_VAL UE1 | IN_FREQ_VAL UE0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | IN_FREQ_VALUE[7:0] | These bits represent a 2's complement signed integer. If the value is multiplied by the value in the FREQ_MON_FACTOR[3:0] bits (b3~0, 2EH), the frequency of an input clock with respect to the reference clock in ppm will be gotten. The input clock is selected by the IN_FREQ_READ_CH[3:0] bits (b3~0, 41H). The value in these bits is updated every 16 seconds, starting when an input clock is selected. | | | | | |

IN1_IN2_DIFF_STS - Differential Input Clock 1 & 2 Status

| Address: 45H Type: Read Default Value: X110X110 | | | | | | | |
|---|------------------------------|---|----------------------------|---|------------------------------|--------------------------------|----------------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | IN2_DIFF_FREQ _HARD_ALARM | IN2_DIFF_NO_A CTIVITY_ALARM | IN2_DIFF_PH_L OCK_ALARM | - | IN1_DIFF_FREQ _HARD_ALARM | IN1_DIFF_NO_A CTIVITY_ALARM | IN1_DIFF_PH_L OCK_ALARM |
| Bit | Name | Description | | | | | |
| 7 | - | Reserved. | | | | | |
| 6 | IN2_DIFF_FREQ_HARD_ALARM | This bit indicates whether IN2_DIFF is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default) | | | | | |
| 5 | IN2_DIFF_NO_ACTIVITY_ALARM | This bit indicates whether IN2_DIFF is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default) | | | | | |
| 4 | IN2_DIFF_PH_LOCK_ALARM | This bit indicates whether IN2_DIFF is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised. | | | | | |
| 3 | - | Reserved. | | | | | |
| 2 | IN1_DIFF_FREQ_HARD_ALARM | This bit indicates whether IN1_DIFF is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default) | | | | | |
| 1 | IN1_DIFF_NO_ACTIVITY_ALARM | This bit indicates whether IN1_DIFF is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default) | | | | | |
| 0 | IN1_DIFF_PH_LOCK_ALARM | This bit indicates whether IN1_DIFF is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised. | | | | | |

IN3_CMOS_STS - CMOS Input Clock 3 Status

| Address: 47H | | | | | | | |
|------------------------|----------------------------|---|---|---|--------------------------|----------------------------|------------------------|
| Type: Read | | | | | | | |
| Default Value:XXXXX110 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | IN3_CMOS_FREQ_HARD_ALARM | IN3_CMOS_NO_ACTIVITY_ALARM | IN3_CMOS_PH_LOCK_ALARM |
| Bit | Name | Description | | | | | |
| 7 - 3 | - | Reserved. | | | | | |
| 2 | IN3_CMOS_FREQ_HARD_ALARM | This bit indicates whether IN3_CMOS is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default) | | | | | |
| 1 | IN3_CMOS_NO_ACTIVITY_ALARM | This bit indicates whether IN3_CMOS is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default) | | | | | |
| 0 | IN3_CMOS_PH_LOCK_ALARM | This bit indicates whether IN3_CMOS is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised. | | | | | |

6.2.5 T0 DPLL INPUT CLOCK SELECTION REGISTERS

INPUT_VALID1_STS - Input Clocks Validity 1

| Address: 4AH | | | | | | | |
|-------------------------|----------|--|----------|---|---|---|---|
| Type: Read | | | | | | | |
| Default Value: XX00XXXX | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | IN2_DIFF | IN1_DIFF | - | - | - | - |
| Bit | Name | Description | | | | | |
| 7 - 6 | - | Reserved. | | | | | |
| 5 - 4 | INn_DIFF | This bit indicates the validity of the corresponding INn_DIFF. Here n is 2 or 1. 0: Invalid. (default) 1: Valid. | | | | | |
| 3 - 0 | - | Reserved. | | | | | |

INPUT_VALID2_STS - Input Clocks Validity 2

| Address: 4BH | | | | | | | |
|-------------------------|----------|--|---|---|---|---|----------|
| Type: Read | | | | | | | |
| Default Value: XXXXXXX0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | - | IN3_CMOS |
| Bit | Name | Description | | | | | |
| 7 - 1 | - | Reserved. | | | | | |
| 0 | IN3_CMOS | This bit indicates the validity of the corresponding IN3_CMOS. 0: Invalid. (default) 1: Valid. | | | | | |

PRIORITY_TABLE1_STS - Priority Status 1

Address: 4EH
 Type: Read
 Default Value: 00000000

| | | | | | | | |
|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HIGHEST_PRIORITY_VALIDATED3 TED3 | HIGHEST_PRIORITY_VALIDATED2 TED2 | HIGHEST_PRIORITY_VALIDATED1 TED1 | HIGHEST_PRIORITY_VALIDATED0 TED0 | CURRENTLY_SELECTED_INP3 UT3 | CURRENTLY_SELECTED_INP2 UT2 | CURRENTLY_SELECTED_INP1 UT1 | CURRENTLY_SELECTED_INP0 UT0 |

| Bit | Name | Description |
|-------|---------------------------------|--|
| 7 - 4 | HIGHEST_PRIORITY_VALIDATED[3:0] | These bits indicate a qualified input clock with the highest priority. 0000: No input clock is qualified. (default) 0001 ~ 0100: Reserved. 0101: IN1_DIFF. 0110: IN2_DIFF. 0111, 1000: Reserved. 1001: IN3_CMOS. 1010 ~ 1111: Reserved. |
| 3 - 0 | CURRENTLY_SELECTED_INPUT[3:0] | These bits indicate the T0 selected input clock. 0000: No input clock is selected. (default) 0001 ~ 0100: Reserved. 0101: IN1_DIFF. 0110: IN2_DIFF. 0111, 1000: Reserved. 1001: IN3_CMOS. 1010 ~ 1111: Reserved. |

PRIORITY_TABLE2_STS - Priority Status 2

| Address: 4FH | | | | | | | |
|-----------------------------------|--|---|-----------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|
| Type: Read | | | | | | | |
| Default Value: 00000000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| THIRD_HIGHEST_PRIORITY_VALIDATED3 | THIRD_HIGHEST_PRIORITY_VALIDATED2 | THIRD_HIGHEST_PRIORITY_VALIDATED1 | THIRD_HIGHEST_PRIORITY_VALIDATED0 | SECOND_HIGHEST_PRIORITY_VALIDATED3 | SECOND_HIGHEST_PRIORITY_VALIDATED2 | SECOND_HIGHEST_PRIORITY_VALIDATED1 | SECOND_HIGHEST_PRIORITY_VALIDATED0 |
| Bit | Name | Description | | | | | |
| 7 - 4 | THIRD_HIGHEST_PRIORITY_VALIDATED[3:0] | These bits indicate a qualified input clock with the third highest priority. 0000: No input clock is qualified. (default) 0001 ~ 0100: Reserved. 0101: IN1_DIFF. 0110: IN2_DIFF. 0111, 1000: Reserved. 1001: IN3_CMOS. 1010 ~ 1111: Reserved. | | | | | |
| 3 - 0 | SECOND_HIGHEST_PRIORITY_VALIDATED[3:0] | These bits indicate a qualified input clock with the second highest priority. 0000: No input clock is qualified. (default) 0001 ~ 0100: Reserved. 0101: IN1_DIFF. 0110: IN2_DIFF. 0111, 1000: Reserved. 1001: IN3_CMOS. 1010 ~ 1111: Reserved. | | | | | |

T0_INPUT_SEL_CNFG - T0 Selected Input Clock Configuration

| Address: 50H | | | | | | | |
|-------------------------|-------------------|---|---|---------------|---------------|---------------|---------------|
| Type: Read / Write | | | | | | | |
| Default Value: XXXX0000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | T0_INPUT_SEL3 | T0_INPUT_SEL2 | T0_INPUT_SEL1 | T0_INPUT_SEL0 |
| Bit | Name | Description | | | | | |
| 7 - 4 | - | Reserved. | | | | | |
| 3 - 0 | T0_INPUT_SEL[3:0] | This bit determines T0 input clock selection. It is valid only when the EXT_SW bit (b4, 0BH) is '0'. 0000: Automatic selection. (default) 0001 ~ 0100: Reserved. 0101: Forced selection - IN1_DIFF. is selected 0110: Forced selection - IN2_DIFF. is selected 0111, 1000: Reserved. 1001: Forced selection - IN3_CMOS is selected. 1010 ~ 1111: Reserved. | | | | | |

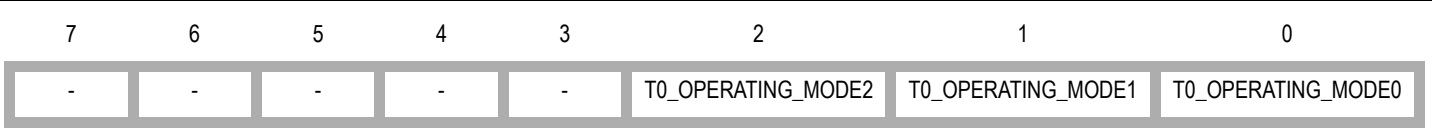
6.2.6 T0 DPLL STATE MACHINE CONTROL REGISTERS

OPERATING_STS - DPLL Operating Status

| Address: 52H | | | | | | | |
|-------------------------|-----------------------------|---|---|--------------|-------------------------|-------------------------|-------------------------|
| Type: Read | | | | | | | |
| Default Value: 1X0X0001 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EX_SYNC_ALARM_MON | - | T0_DPLL_SOFT_FREQ_ALARM | - | T0_DPLL_LOCK | T0_DPLL_OPERATING_MODE2 | T0_DPLL_OPERATING_MODE1 | T0_DPLL_OPERATING_MODE0 |
| Bit | Name | Description | | | | | |
| 7 | EX_SYNC_ALARM_MON | This bit indicates whether the selected frame sync input signal is in external sync alarm status. 0: No external sync alarm. 1: In external sync alarm status. (default) | | | | | |
| 6 | - | Reserved. | | | | | |
| 5 | T0_DPLL_SOFT_FREQ_ALARM | This bit indicates whether the T0 DPLL is in soft alarm status. 0: No T0 DPLL soft alarm. (default) 1: In T0 DPLL soft alarm status. | | | | | |
| 4 | - | Reserved. | | | | | |
| 3 | T0_DPLL_LOCK | This bit indicates the T0 DPLL locking status. 0: Unlocked. (default) 1: Locked. | | | | | |
| 2 - 0 | T0_DPLL_OPERATING_MODE[2:0] | These bits indicate the current operating mode of T0 DPLL. 000: Reserved. 001: Free-Run. (default) 010: Holdover. 011: Reserved. 100: Locked. 101: Pre-Locked2. 110: Pre-Locked. 111: Lost-Phase. | | | | | |

T0_OPERATING_MODE_CNFG - T0 DPLL Operating Mode Configuration

Address: 53H
 Type: Read / Write
 Default Value: XXXXX000



| Bit | Name | Description |
|-------|------------------------|--|
| 7 - 3 | - | Reserved. |
| 2 - 0 | T0_OPERATING_MODE[2:0] | These bits control the T0 DPLL operating mode. 000: Automatic. (default) 001: Forced - Free-Run. 010: Forced - Holdover. 011: Reserved. 100: Forced - Locked. 101: Forced - Pre-Locked2. 110: Forced - Pre-Locked. 111: Forced - Lost-Phase. |

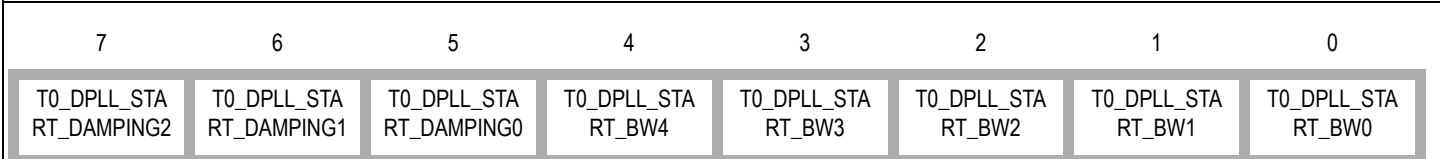
6.2.7 T0 DPLL & T0/T4 APLL CONFIGURATION REGISTERS

T0_DPLL_APLL_PATH_CNFG - T0 DPLL & APLL Path Configuration

| Address: 55H | | | | | | | |
|-------------------------|---------------------------------|--|-------------------|---------------------------------|---------------------------------|-----------------------------|-----------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000X0X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| T0_APLL_PATH 3 | T0_APLL_PA TH2 | T0_APLL_PA TH1 | T0_APLL_PA TH0 | T0_GSM_OBSAI_ 16E1_16T1_SEL1 | T0_GSM_OBSAI_ 16E1_16T1_SELO | T0_12E1_24T1_ E3_T3_SEL1 | T0_12E1_24T1_ E3_T3_SELO |
| Bit | Name | Description | | | | | |
| 7 - 4 | T0_APLL_PATH[3:0] | These bits select an input to the T0 APLL. 0000: The output of T0 DPLL 77.76 MHz path. (default) 0001: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0010: The output of T0 DPLL 16E1/16T1 path. 0011: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 0100 ~ 1111: Reserved. | | | | | |
| 3 - 2 | T0_GSM_OBSAI_16E1_16T1_SEL[1:0] | These bits select an output clock from the T0 DPLL GSM/OBSAI/16E1/16T1 path. 00: 16E1. 01: 16T1. 10: GSM. 11: OBSAI. The default value of the T0_GSM_OBSAI_16E1_16T1_SELO bit is determined by the SONET/SDH pin during reset. | | | | | |
| 1 - 0 | T0_12E1_24T1_E3_T3_SEL[1:0] | These bits select an output clock from the T0 DPLL 12E1/24T1/E3/T3 path. 00: 12E1. 01: 24T1. 10: E3. 11: T3. The default value of the T0_12E1_24T1_E3_T3_SELO bit is determined by the SONET/SDH pin during reset. | | | | | |

T0_DPLL_START_BW_DAMPING_CNFG - T0 DPLL Start Bandwidth & Damping Factor Configuration

Address: 56H
 Type: Read / Write
 Default Value: 01101111



| Bit | Name | Description |
|-------|----------------------------|---|
| 7 - 5 | T0_DPLL_START_DAMPING[2:0] | These bits set the starting damping factor for T0 DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved. |
| 4 - 0 | T0_DPLL_START_BW[4:0] | These bits set the starting bandwidth for T0 DPLL. 00XXX: Reserved. 01000: 0.1 Hz. 01001: 0.3 Hz. 01010: 0.6 Hz. 01011: 1.2 Hz. 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. (default) 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved. |

T0_DPLL_ACQ_BW_DAMPING_CNFG - T0 DPLL Acquisition Bandwidth & Damping Factor Configuration

Address: 57H
 Type: Read / Write
 Default Value: 01101111

| | | | | | | | |
|--------------------------|--------------------------|--------------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| T0_DPLL_ACQ _DAMPING2 | T0_DPLL_ACQ _DAMPING1 | T0_DPLL_ACQ _DAMPING0 | T0_DPLL_ACQ _BW4 | T0_DPLL_ACQ _BW3 | T0_DPLL_ACQ _BW2 | T0_DPLL_ACQ _BW1 | T0_DPLL_ACQ _BW0 |

| Bit | Name | Description |
|-------|--------------------------|--|
| 7 - 5 | T0_DPLL_ACQ_DAMPING[2:0] | These bits set the acquisition damping factor for T0 DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved. |
| 4 - 0 | T0_DPLL_ACQ_BW[4:0] | These bits set the acquisition bandwidth for T0 DPLL. 00XXX: Reserved. 01000: 0.1 Hz. 01001: 0.3 Hz. 01010: 0.6 Hz. 01011: 1.2 Hz. 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. (default) 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved. |

T0_DPLL_LOCKED_BW_DAMPING_CNFG - T0 DPLL Locked Bandwidth & Damping Factor Configuration

| Address: 58H | | | | | | | |
|-----------------------------|-----------------------------|---|------------------------|------------------------|------------------------|------------------------|------------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 01101111 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| T0_DPLL_LOCK ED_DAMPING2 | T0_DPLL_LOCK ED_DAMPING1 | T0_DPLL_LOCK ED_DAMPING0 | T0_DPLL_LOC KED_BW4 | T0_DPLL_LOC KED_BW3 | T0_DPLL_LOC KED_BW2 | T0_DPLL_LOC KED_BW1 | T0_DPLL_LOC KED_BW0 |
| Bit | Name | Description | | | | | |
| 7 - 5 | T0_DPLL_LOCKED_DAMPING[2:0] | These bits set the locked damping factor for T0 DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved. | | | | | |
| 4 - 0 | T0_DPLL_LOCKED_BW[4:0] | These bits set the locked bandwidth for T0 DPLL. 00XXX: Reserved. 01000: 0.1 Hz. 01001: 0.3 Hz. 01010: 0.6 Hz. 01011: 1.2 Hz. (default) 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved. | | | | | |

T0_BW_OVERSHOOT_CNFG - T0 DPLL Bandwidth Overshoot Configuration

| Address: 59H | | | | | | | |
|-------------------------|-------------|---|---|----------|---|---|---|
| Type: Read / Write | | | | | | | |
| Default Value: 1XXX1XXX | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUTO_BW_SEL | - | - | - | T0_LIMIT | - | - | - |
| Bit | Name | Description | | | | | |
| 7 | AUTO_BW_SEL | This bit determines whether starting or acquisition bandwidth / damping factor is used for T0 DPLL. 0: The starting and acquisition bandwidths / damping factors are not used. Only the locked bandwidth / damping factor is used regardless of the T0 DPLL locking stage. 1: The starting, acquisition or locked bandwidth / damping factor is used automatically depending on different T0 DPLL locking stages. (default) | | | | | |
| 6 - 4 | - | Reserved. | | | | | |
| 3 | T0_LIMIT | This bit determines whether the integral path value is frozen when the T0 DPLL hard limit is reached. 0: Not frozen. 1: Frozen. It will minimize the subsequent overshoot when T0 DPLL is pulling in. (default) | | | | | |
| 2 - 0 | - | Reserved. | | | | | |

PHASE_LOSS_COARSE_LIMIT_CNFG - Phase Loss Coarse Detector Limit Configuration

| Address: 5AH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------------------|-------------------------|---|--|---------------------|---------------------|---------------------|---------------------|----------------------|----------------------|---------|--------------------|-----------------------|---|------------|-------|---|---|-------|-----------------------------------|------------|---|--|------------|---|-------|------------|------------|---|--|
| Type: Read / Write | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default Value: 10000101 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | |
| COARSE_PH_LOS_LIMT_EN | WIDE_EN | MULTI_PH_APP | MULTI_PH_8K_4K_2K_EN | PH_LOS_COARSE_LIMT3 | PH_LOS_COARSE_LIMT2 | PH_LOS_COARSE_LIMT1 | PH_LOS_COARSE_LIMT0 | | | | | | | | | | | | | | | | | | | | | | |
| Bit | Name | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | COARSE_PH_LOS_LIMT_EN | This bit controls whether the occurrence of the coarse phase loss will result in the T0 DPLL unlocked. 0: Disabled. 1: Enabled. (default) | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | WIDE_EN | Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH). | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | MULTI_PH_APP | This bit determines whether the PFD output of T0 DPLL is limited to ±1 UI or is limited to the coarse phase limit. 0: Limited to ±1 UI. (default) 1: Limited to the coarse phase limit. When the selected input clock is of 2 kHz, 4 kHz or 8 kHz, the coarse phase limit depends on the MULTI_PH_8K_4K_2K_EN bit, the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits; when the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH) for details. | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | MULTI_PH_8K_4K_2K_EN | <p>This bit, together with the WIDE_EN bit (b6, 5AH) and the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH), determines the coarse phase limit when the selected input clock is of 2 kHz, 4 kHz or 8 kHz. When the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Selected Input Clock</th> <th>MULTI_PH_8K_4K_2K_EN</th> <th>WIDE_EN</th> <th>Coarse Phase Limit</th> </tr> </thead> <tbody> <tr> <td rowspan="2" style="text-align: center;">2 kHz, 4 kHz or 8 kHz</td> <td style="text-align: center;">0</td> <td style="text-align: center;">don't-care</td> <td style="text-align: center;">±1 UI</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">±1 UI</td> </tr> <tr> <td rowspan="2" style="text-align: center;">other than 2 kHz, 4 kHz and 8 kHz</td> <td style="text-align: center;">don't-care</td> <td style="text-align: center;">1</td> <td style="text-align: center;">set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH).</td> </tr> <tr> <td style="text-align: center;">don't-care</td> <td style="text-align: center;">0</td> <td style="text-align: center;">±1 UI</td> </tr> <tr> <td style="text-align: center;">don't-care</td> <td style="text-align: center;">don't-care</td> <td style="text-align: center;">1</td> <td style="text-align: center;">set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH).</td> </tr> </tbody> </table> | | | | | | Selected Input Clock | MULTI_PH_8K_4K_2K_EN | WIDE_EN | Coarse Phase Limit | 2 kHz, 4 kHz or 8 kHz | 0 | don't-care | ±1 UI | 1 | 0 | ±1 UI | other than 2 kHz, 4 kHz and 8 kHz | don't-care | 1 | set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH). | don't-care | 0 | ±1 UI | don't-care | don't-care | 1 | set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH). |
| Selected Input Clock | MULTI_PH_8K_4K_2K_EN | WIDE_EN | Coarse Phase Limit | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 kHz, 4 kHz or 8 kHz | 0 | don't-care | ±1 UI | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | 0 | ±1 UI | | | | | | | | | | | | | | | | | | | | | | | | | | |
| other than 2 kHz, 4 kHz and 8 kHz | don't-care | 1 | set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH). | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | don't-care | 0 | ±1 UI | | | | | | | | | | | | | | | | | | | | | | | | | | |
| don't-care | don't-care | 1 | set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH). | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 - 0 | PH_LOS_COARSE_LIMT[3:0] | <p>These bit set the coarse phase limit. The limit is used only in some cases. Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH).</p> <p>0000: ±1 UI. 0001: ±3 UI. 0010: ±7 UI. 0011: ±15 UI. 0100: ±31 UI. 0101: ±63 UI. (default) 0110: ±127 UI. 0111: ±255 UI. 1000: ±511 UI. 1001: ±1023 UI. 1010-1111: Reserved.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | |

PHASE_LOSS_FINE_LIMIT_CNFG - Phase Loss Fine Detector Limit Configuration

| Address: 5BH | | | | | | | |
|-------------------------|-----------------------|---|---|---|-------------------|-------------------|-------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 10XXX010 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FINE_PH_LOS_LIMT_EN | FAST_LOS_SW | - | - | - | PH_LOS_FINE_LIMT2 | PH_LOS_FINE_LIMT1 | PH_LOS_FINE_LIMT0 |
| Bit | Name | Description | | | | | |
| 7 | FINE_PH_LOS_LIMT_EN | This bit controls whether the occurrence of the fine phase loss will result in the T0 DPLL unlocked. 0: Disabled. 1: Enabled. (default) | | | | | |
| 6 | FAST_LOS_SW | This bit controls whether the occurrence of the fast loss will result in the T0 DPLL unlocked. 0: Does not result in the T0 DPLL unlocked. T0 DPLL will enter Temp-Holdover mode automatically. (default) 1: Results in the T0 DPLL unlocked. T0 DPLL will enter Lost-Phase mode if the T0 DPLL operating mode is switched automatically. | | | | | |
| 5-3 | - | Reserved. | | | | | |
| 2-0 | PH_LOS_FINE_LIMT[2:0] | These bits set a fine phase limit. 000: 0. 001: $\pm (45^\circ \sim 90^\circ)$. 010: $\pm (90^\circ \sim 180^\circ)$. (default) 011: $\pm (180^\circ \sim 360^\circ)$. 100: $\pm (20 \text{ ns} \sim 25 \text{ ns})$. 101: $\pm (60 \text{ ns} \sim 65 \text{ ns})$. 110: $\pm (120 \text{ ns} \sim 125 \text{ ns})$. 111: $\pm (950 \text{ ns} \sim 955 \text{ ns})$. | | | | | |

T0_HOLDOVER_MODE_CNFG - T0 DPLL Holdover Mode Configuration

| Address: 5CH | | | | | | | |
|-------------------------|-------------------------|---|------------|---------------------|-----------------------------------|-------------------------|---|
| Type: Read / Write | | | | | | | |
| Default Value: 010001XX | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MAN_HOLDOVER | AUTO_AVG | FAST_AVG | READ_AVG | TEMP_HOLDOVER_MODE1 | TEMP_HOLDOVER_MODE0 | - | - |
| Bit | Name | Description | | | | | |
| 7 | MAN_HOLDOVER | Refer to the description of the FAST_AVG bit (b5, 5CH). | | | | | |
| 6 | AUTO_AVG | Refer to the description of the FAST_AVG bit (b5, 5CH). | | | | | |
| 5 | FAST_AVG | This bit, together with the AUTO_AVG bit (b6, 5CH) and the MAN_HOLDOVER bit (b7, 5CH), determines a frequency offset acquiring method in T0 DPLL Holdover Mode. | | | | | |
| | | MAN_HOLDOVER | AUTO_AVG | FAST_AVG | Frequency Offset Acquiring Method | | |
| | | 0 | 0 | don't-care | | Automatic Instantaneous | |
| | | | 1 | 0 | Automatic Slow Averaged (default) | | |
| | | 1 | don't-care | | 1 | Automatic Fast Averaged | |
| | | Manual | | | | | |
| 4 | READ_AVG | This bit controls the holdover frequency offset reading, which is read from the T0_HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH). 0: The value read from the T0_HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH) is equal to the one written to them. (default) 1: The value read from the T0_HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH) is not equal to the one written to them. The value is acquired by Automatic Slow Averaged method if the FAST_AVG bit (b5, 5CH) is '0'; or is acquired by Automatic Fast Averaged method if the FAST_AVG bit (b5, 5CH) is '1'. | | | | | |
| 3 - 2 | TEMP_HOLDOVER_MODE[1:0] | These bits determine the frequency offset acquiring method in T0 DPLL Temp-Holdover Mode. 00: The method is the same as that used in T0 DPLL Holdover mode. 01: Automatic Instantaneous. (default) 10: Automatic Fast Averaged. 11: Automatic Slow Averaged. | | | | | |
| 1 - 0 | - | Reserved. | | | | | |

T0_HOLDOVER_FREQ[7:0]_CNFG - T0 DPLL Holdover Frequency Configuration 1

| Address: 5DH | | | | | | | |
|-------------------------|-----------------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| T0_HOLDOVER_FREQ7 | T0_HOLDOVER_FREQ6 | T0_HOLDOVER_FREQ5 | T0_HOLDOVER_FREQ4 | T0_HOLDOVER_FREQ3 | T0_HOLDOVER_FREQ2 | T0_HOLDOVER_FREQ1 | T0_HOLDOVER_FREQ0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | T0_HOLDOVER_FREQ[7:0] | Refer to the description of the T0_HOLDOVER_FREQ[23:16] bits (b7~0, 5FH). | | | | | |

T0_HOLDOVER_FREQ[15:8]_CNFG - T0 DPLL Holdover Frequency Configuration 2

| Address: 5EH | | | | | | | |
|-------------------------|------------------------|---|--------------------|--------------------|--------------------|-------------------|-------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| T0_HOLDOVER_FREQ15 | T0_HOLDOVER_FREQ14 | T0_HOLDOVER_FREQ13 | T0_HOLDOVER_FREQ12 | T0_HOLDOVER_FREQ11 | T0_HOLDOVER_FREQ10 | T0_HOLDOVER_FREQ9 | T0_HOLDOVER_FREQ8 |
| Bit | Name | Description | | | | | |
| 7 - 0 | T0_HOLDOVER_FREQ[15:8] | Refer to the description of the T0_HOLDOVER_FREQ[23:16] bits (b7~0, 5FH). | | | | | |

T0_HOLDOVER_FREQ[23:16]_CNFG - T0 DPLL Holdover Frequency Configuration 3

| Address: 5FH | | | | | | | |
|-------------------------|-------------------------|--|--------------------|--------------------|--------------------|--------------------|--------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00000000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| T0_HOLDOVER_FREQ23 | T0_HOLDOVER_FREQ22 | T0_HOLDOVER_FREQ21 | T0_HOLDOVER_FREQ20 | T0_HOLDOVER_FREQ19 | T0_HOLDOVER_FREQ18 | T0_HOLDOVER_FREQ17 | T0_HOLDOVER_FREQ16 |
| Bit | Name | Description | | | | | |
| 7 - 0 | T0_HOLDOVER_FREQ[23:16] | The T0_HOLDOVER_FREQ[23:0] bits represent a 2's complement signed integer. In T0 DPLL Holdover mode, the value written to these bits multiplied by 0.000011 is the frequency offset set manually; the value read from these bits multiplied by 0.000011 is the frequency offset automatically slow or fast averaged or manually set, as determined by the READ_AVG bit (b4, 5CH) and the FAST_AVG bit (b5, 5CH). | | | | | |

T4_APLL_PATH_CNFG - T4 APLL Path Configuration

| Address: 60H | | | | | | | |
|-------------------------|-------------------|--|---------------|---|---|---|---|
| Type: Read / Write | | | | | | | |
| Default Value: 0100XXXX | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| T4_APLL_PATH3 | T4_APLL_PATH2 | T4_APLL_PATH1 | T4_APLL_PATH0 | - | - | - | - |
| Bit | Name | Description | | | | | |
| 7 - 4 | T4_APLL_PATH[3:0] | These bits select an input to the T4 APLL. 0000: The output of T0 DPLL 77.76 MHz path. 0001: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0010: The output of T0 DPLL 16E1/16T1 path. 0011: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 0100 ~ 1111: Reserved. | | | | | |
| 3 - 0 | - | Reserved. | | | | | |

CURRENT_DPLL_FREQ[7:0]_STS - DPLL Current Frequency Status 1

| Address: 62H Type: Read Default Value: 00000000 | | | | | | | |
|---|------------------------|--|------------------------|------------------------|------------------------|------------------------|------------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CURRENT_DP LL_FREQ7 | CURRENT_DP LL_FREQ6 | CURRENT_DP LL_FREQ5 | CURRENT_DP LL_FREQ4 | CURRENT_DP LL_FREQ3 | CURRENT_DP LL_FREQ2 | CURRENT_DP LL_FREQ1 | CURRENT_DP LL_FREQ0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | CURRENT_DPLL_FREQ[7:0] | Refer to the description of the CURRENT_DPLL_FREQ[23:16] bits (b7~0, 64H). | | | | | |

CURRENT_DPLL_FREQ[15:8]_STS - DPLL Current Frequency Status 2

| Address: 63H Type: Read Default Value: 00000000 | | | | | | | |
|---|-------------------------|--|-------------------------|-------------------------|-------------------------|------------------------|------------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CURRENT_DP LL_FREQ15 | CURRENT_DP LL_FREQ14 | CURRENT_DP LL_FREQ13 | CURRENT_DP LL_FREQ12 | CURRENT_DP LL_FREQ11 | CURRENT_DP LL_FREQ10 | CURRENT_DP LL_FREQ9 | CURRENT_DP LL_FREQ8 |
| Bit | Name | Description | | | | | |
| 7 - 0 | CURRENT_DPLL_FREQ[15:8] | Refer to the description of the CURRENT_DPLL_FREQ[23:16] bits (b7~0, 64H). | | | | | |

CURRENT_DPLL_FREQ[23:16]_STS - DPLL Current Frequency Status 3

| Address: 64H Type: Read Default Value: 00000000 | | | | | | | |
|---|--------------------------|--|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CURRENT_DP LL_FREQ23 | CURRENT_DP LL_FREQ22 | CURRENT_DP LL_FREQ21 | CURRENT_DP LL_FREQ20 | CURRENT_DP LL_FREQ19 | CURRENT_DP LL_FREQ18 | CURRENT_DP LL_FREQ17 | CURRENT_DP LL_FREQ16 |
| Bit | Name | Description | | | | | |
| 7 - 0 | CURRENT_DPLL_FREQ[23:16] | The CURRENT_DPLL_FREQ[23:0] bits represent a 2's complement signed integer. If the value in these bits is multiplied by 0.000011, the current frequency offset of the T0 DPLL output in ppm with respect to the master clock will be gotten. | | | | | |

DPLL_FREQ_SOFT_LIMIT_CNFG - DPLL Soft Limit Configuration

| Address: 65H Type: Read / Write Default Value: 10001100 | | | | | | | |
|---|---------------------------|---|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FREQ_LIMIT_PH_LOS | DPLL_FREQ_SOFT_LIMIT6 | DPLL_FREQ_SOFT_LIMIT5 | DPLL_FREQ_SOFT_LIMIT4 | DPLL_FREQ_SOFT_LIMIT3 | DPLL_FREQ_SOFT_LIMIT2 | DPLL_FREQ_SOFT_LIMIT1 | DPLL_FREQ_SOFT_LIMIT0 |
| Bit | Name | Description | | | | | |
| 7 | FREQ_LIMIT_PH_LOS | This bit determines whether the T0 DPLL in hard alarm status will result in it unlocked. 0: Disabled. 1: Enabled. (default) | | | | | |
| 6 - 0 | DPLL_FREQ_SOFT_LIMIT[6:0] | These bits represent an unsigned integer. If the value is multiplied by 0.724, the DPLL soft limit for T0 path in ppm will be gotten. The DPLL soft limit is symmetrical about zero. | | | | | |

DPLL_FREQ_HARD_LIMIT[7:0]_CNFG - DPLL Hard Limit Configuration 1

| Address: 66H Type: Read / Write Default Value: 10101011 | | | | | | | |
|---|---------------------------|--|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DPLL_FREQ_HARD_LIMIT7 | DPLL_FREQ_HARD_LIMIT6 | DPLL_FREQ_HARD_LIMIT5 | DPLL_FREQ_HARD_LIMIT4 | DPLL_FREQ_HARD_LIMIT3 | DPLL_FREQ_HARD_LIMIT2 | DPLL_FREQ_HARD_LIMIT1 | DPLL_FREQ_HARD_LIMIT0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | DPLL_FREQ_HARD_LIMIT[7:0] | Refer to the description of the DPLL_FREQ_HARD_LIMIT[15:8] bits (b7~0, 67H). | | | | | |

DPLL_FREQ_HARD_LIMIT[15:8]_CNFG - DPLL Hard Limit Configuration 2

| Address: 67H Type: Read / Write Default Value: 00011001 | | | | | | | |
|---|----------------------------|---|------------------------|------------------------|------------------------|-----------------------|-----------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DPLL_FREQ_HARD_LIMIT15 | DPLL_FREQ_HARD_LIMIT14 | DPLL_FREQ_HARD_LIMIT13 | DPLL_FREQ_HARD_LIMIT12 | DPLL_FREQ_HARD_LIMIT11 | DPLL_FREQ_HARD_LIMIT10 | DPLL_FREQ_HARD_LIMIT9 | DPLL_FREQ_HARD_LIMIT8 |
| Bit | Name | Description | | | | | |
| 7 - 0 | DPLL_FREQ_HARD_LIMIT[15:8] | The DPLL_FREQ_HARD_LIMIT[15:0] bits represent an unsigned integer. If the value is multiplied by 0.0014, the DPLL hard limit for T0 path in ppm will be gotten. The DPLL hard limit is symmetrical about zero. | | | | | |

CURRENT_DPLL_PHASE[7:0]_STS - DPLL Current Phase Status 1

| Address: 68H Type: Read Default Value: 00000000 | | | | | | | |
|---|----------------------|---|------------------|------------------|------------------|------------------|------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CURRENT_PH_DATA7 | CURRENT_PH_DATA6 | CURRENT_PH_DATA5 | CURRENT_PH_DATA4 | CURRENT_PH_DATA3 | CURRENT_PH_DATA2 | CURRENT_PH_DATA1 | CURRENT_PH_DATA0 |
| Bit | Name | Description | | | | | |
| 7 - 0 | CURRENT_PH_DATA[7:0] | Refer to the description of the CURRENT_PH_DATA[15:8] bits (b7~0, 69H). | | | | | |

CURRENT_DPLL_PHASE[15:8]_STS - DPLL Current Phase Status 2

| Address: 69H Type: Read Default Value: 00000000 | | | | | | | |
|---|-----------------------|---|-------------------|-------------------|-------------------|------------------|------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CURRENT_PH_DATA15 | CURRENT_PH_DATA14 | CURRENT_PH_DATA13 | CURRENT_PH_DATA12 | CURRENT_PH_DATA11 | CURRENT_PH_DATA10 | CURRENT_PH_DATA9 | CURRENT_PH_DATA8 |
| Bit | Name | Description | | | | | |
| 7 - 0 | CURRENT_PH_DATA[15:8] | The CURRENT_PH_DATA[15:0] bits represent a 2's complement signed integer. If the value is multiplied by 0.61, the averaged phase error of the T0 DPLL feedback with respect to the selected input clock in ns will be gotten. | | | | | |

T0_T4_APLL_BW_CNFG - T0 / T4 APLL Bandwidth Configuration

| Address: 6AH Type: Read / Write Default Value: XX01XX01 | | | | | | | |
|---|-----------------|---|-------------|---|---|-------------|-------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | T0_APLL_BW1 | T0_APLL_BW0 | - | - | T4_APLL_BW1 | T4_APLL_BW0 |
| Bit | Name | Description | | | | | |
| 7 - 6 | - | Reserved. | | | | | |
| 5 - 4 | T0_APLL_BW[1:0] | These bits set the bandwidth for T0 APLL. 00: 100 kHz. 01: 500 kHz. (default) 10: 1 MHz. 11: 2 MHz. | | | | | |
| 3 - 2 | - | Reserved. | | | | | |
| 1 - 0 | T4_APLL_BW[1:0] | These bits set the bandwidth for T4 APLL. 00: 100 kHz. 01: 500 kHz. (default) 10: 1 MHz. 11: 2 MHz. | | | | | |

6.2.8 OUTPUT CONFIGURATION REGISTERS

OUT2_FREQ_CNFG - Output Clock 2 Frequency Configuration

| Address: 6DH | | | | | | | |
|-------------------------|--------------------|--|--------------------|-------------------|-------------------|-------------------|-------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00001000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OUT2_PATH_S EL3 | OUT2_PATH_S EL2 | OUT2_PATH_S EL1 | OUT2_PATH_S EL0 | OUT2_DIVIDER 3 | OUT2_DIVIDER 2 | OUT2_DIVIDER 1 | OUT2_DIVIDER 0 |
| Bit | Name | Description | | | | | |
| 7 - 4 | OUT2_PATH_SEL[3:0] | These bits select an input to OUT2. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1011: The output of T4 APLL. 1100 ~ 1111: Reserved. | | | | | |
| 3 - 0 | OUT2_DIVIDER[3:0] | These bits select a division factor of the divider for OUT2. The output frequency is determined by the division factor and the signal derived from T0 DPLL or T0/T4 APLL output (selected by the OUT2_PATH_SEL[3:0] bits (b7~4, 6DH)). If the signal is derived from one of the T0 DPLL outputs, please refer to Table 22 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 23 for the division factor selection. | | | | | |

OUT1_FREQ_CNFG - Output Clock 1 Frequency Configuration

| Address: 71H | | | | | | | |
|-------------------------|--------------------|--|--------------------|-------------------|-------------------|-------------------|-------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 00001000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OUT1_PATH_S EL3 | OUT1_PATH_S EL2 | OUT1_PATH_S EL1 | OUT1_PATH_S EL0 | OUT1_DIVIDER 3 | OUT1_DIVIDER 2 | OUT1_DIVIDER 1 | OUT1_DIVIDER 0 |
| Bit | Name | Description | | | | | |
| 7 - 4 | OUT1_PATH_SEL[3:0] | These bits select an input to OUT1. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1011: The output of T4 APLL. 1100 ~ 1111: Reserved. | | | | | |
| 3 - 0 | OUT1_DIVIDER[3:0] | These bits select a division factor of the divider for OUT1. The output frequency is determined by the division factor and the signal derived from T0 DPLL or T0/T4 APLL output (selected by the OUT1_PATH_SEL[3:0] bits (b7~4, 71H)). If the signal is derived from one of the T0 DPLL outputs, please refer to Table 22 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 23 for the division factor selection. | | | | | |

OUT1_INV_CNFG - Output Clock 1 Invert Configuration

| Address:72H Type: Read / Write Default Value: XXXXXX0X | | | | | | | |
|--|----------|---|---|---|---|----------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | OUT1_INV | - |
| Bit | Name | Description | | | | | |
| 7 - 2 | - | Reserved. | | | | | |
| 1 | OUT1_INV | This bit determines whether the output on OUT1 is inverted. 0: Not inverted. (default) 1: Inverted. | | | | | |
| 0 | - | Reserved. | | | | | |

OUT2_INV_CNFG - Output Clock 2 Invert Configuration

| Address:73H Type: Read / Write Default Value: XXXXX0XX | | | | | | | |
|--|----------|---|---|---|----------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | OUT2_INV | - | - |
| Bit | Name | Description | | | | | |
| 7 - 3 | - | Reserved. | | | | | |
| 2 | OUT2_INV | This bit determines whether the output on OUT2 is inverted. 0: Not inverted. (default) 1: Inverted. | | | | | |
| 1 - 0 | - | Reserved. | | | | | |

FR_MFR_SYNC_CNFG - Frame Sync & Multiframe Sync Output Configuration

| Address:74H | | | | | | | |
|-------------------------|--------------------|--|------------------------|--------|--------|--------|--------|
| Type: Read / Write | | | | | | | |
| Default Value: 01100000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IN_2K_4K_8K_I NV | 8K_EN | 2K_EN | 2K_8K_PUL_P OSITION | 8K_INV | 8K_PUL | 2K_INV | 2K_PUL |
| Bit | Name | Description | | | | | |
| 7 | IN_2K_4K_8K_INV | This bit determines whether the input clock is inverted before locked by the T0 DPLL when the input clock is 2 kHz, 4 kHz or 8 kHz. 0: Not inverted. (default) 1: Inverted. | | | | | |
| 6 | 8K_EN | This bit determines whether an 8 kHz signal is enabled to be output on FRSYNC_8K. 0: Disabled. FRSYNC_8K outputs low. 1: Enabled. (default) | | | | | |
| 5 | 2K_EN | Reserved. | | | | | |
| 4 | 2K_8K_PUL_POSITION | This bit is valid only when FRSYNC_8K and/or MFRSYNC_2K output pulse; i.e., when one of the 8K_PUL bit (b2, 74H) and the 2K_PUL bit (b0, 74H) is '1' or when the 8K_PUL bit (b2, 74H) and the 2K_PUL bit (b0, 74H) are both '1'. It determines the pulse position referring to the standard 50:50 duty cycle. 0: Pulsed on the falling edge of the standard 50:50 duty cycle position. (default) 1: Pulsed on the rising edge of the standard 50:50 duty cycle position. | | | | | |
| 3 | 8K_INV | This bit determines whether the output on FRSYNC_8K is inverted. 0: Not inverted. (default) 1: Inverted. | | | | | |
| 2 | 8K_PUL | This bit determines whether the output on FRSYNC_8K is 50:50 duty cycle or pulsed. 0: 50:50 duty cycle. (default) 1: Pulsed. The pulse width is defined by the period of the output on OUT2. | | | | | |
| 1 | 2K_INV | This bit determines whether the output on MFRSYNC_2K is inverted. 0: Not inverted. (default) 1: Inverted. | | | | | |
| 0 | 2K_PUL | This bit determines whether the output on MFRSYNC_2K is 50:50 duty cycle or pulsed. 0: 50:50 duty cycle. (default) 1: Pulsed. The pulse width is defined by the period of the output on OUT2. | | | | | |

6.2.9 PBO & PHASE OFFSET CONTROL REGISTERS

PHASE_MON_PBO_CNFG - Phase Transient Monitor & PBO Configuration

| Address: 78H | | | | | | | |
|-------------------------|---------------------|---|-------------------|---------------------|---------------------|---------------------|---------------------|
| Type: Read / Write | | | | | | | |
| Default Value: 0X000110 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IN_NOISE_WIN DOW | - | PH_MON_EN | PH_MON_PBO _EN | PH_TR_MON_L IMT3 | PH_TR_MON_L IMT2 | PH_TR_MON_L IMT1 | PH_TR_MON_L IMT0 |
| Bit | Name | Description | | | | | |
| 7 | IN_NOISE_WINDOW | This bit determines whether the input clock whose edge respect to the reference clock is outside $\pm 5\%$ is enabled to be selected for T0 DPLL. 0: Disabled. (default) 1: Enabled. | | | | | |
| 6 | - | Reserved. | | | | | |
| 5 | PH_MON_EN | This bit is valid only when the PH_MON_PBO_EN bit (b4, 78H) is '1'. It determines whether the Phase Transient Monitor is enabled to monitor the phase-time changes on the T0 selected input clock. 0: Disabled. (default) 1: Enabled. | | | | | |
| 4 | PH_MON_PBO_EN | This bit determines whether a PBO event is triggered when the phase-time changes on the T0 selected input clock are greater than a programmable limit over an interval of less than 0.1 seconds with the PH_MON_EN bit being '1'. The limit is programmed by the PH_TR_MON_LIMT[3:0] bits (b3~0, 78H). 0: Disabled. (default) 1: Enabled. | | | | | |
| 3 - 0 | PH_TR_MON_LIMT[3:0] | These bits represent an unsigned integer. The Phase Transient Monitor limit in ns can be calculated as follows: Limit (ns) = (PH_TR_MON_LIMT[3:0] + 7) X 156. | | | | | |

6.2.10 SYNCHRONIZATION CONFIGURATION REGISTERS

SYNC_MONITOR_CNFG - Sync Monitor Configuration

| Address: 7CH | | | | | | | |
|-------------------------|--------------------|--|----------------|---|---|---|---|
| Type: Read / Write | | | | | | | |
| Default Value: 00101011 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SYNC_BYPASS | SYNC_MON_LIMT2 | SYNC_MON_LIMT1 | SYNC_MON_LIMT0 | - | - | - | - |
| Bit | Name | Description | | | | | |
| 7 | SYNC_BYPASS | This bit selects one frame sync input signal to synchronize the frame sync output signals. 0: EX_SYNC1 is selected. (default) 1: When the T0 selected input clock is IN1_DIFF, EX_SYNC1 is selected; when the T0 selected input clock is IN2_DIFF, EX_SYNC2 is selected; when the T0 selected input clock is IN3_CMOS, EX_SYNC3 is selected; when there is no T0 selected input clock, no frame sync input signal is selected. | | | | | |
| 6 - 4 | SYNC_MON_LIMT[2:0] | These bits set the limit for the external sync alarm. 000: ±1 UI. 001: ±2 UI. 010: ±3 UI. (default) 011: ±4 UI. 100: ±5 UI. 101: ±6 UI. 110: ±7 UI. 111: ±8 UI. | | | | | |
| 3 - 0 | - | These bits must be set to '1011'. | | | | | |

SYNC_PHASE_CNFG - Sync Phase Configuration

| Address: 7DH | | | | | | | |
|-------------------------|---------------|--|-----------|-----------|-----------|-----------|-----------|
| Type: Read / Write | | | | | | | |
| Default Value: XX000000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | SYNC_PH31 | SYNC_PH30 | SYNC_PH21 | SYNC_PH20 | SYNC_PH11 | SYNC_PH10 |
| Bit | Name | Description | | | | | |
| 7 - 6 | - | Reserved. | | | | | |
| 5 - 4 | SYNC_PH3[1:0] | These bits set the sampling of EX_SYNC3 when EX_SYNC3 is enabled to synchronize the frame sync output signal. Nominally, the falling edge of EX_SYNC3 is aligned with the rising edge of the T0 selected input clock. 00: On target. (default) 01: 0.5 UI early. 10: 1 UI late. 11: 0.5 UI late. | | | | | |
| 3 - 2 | SYNC_PH2[1:0] | These bits set the sampling of EX_SYNC2 when EX_SYNC2 is enabled to synchronize the frame sync output signal. Nominally, the falling edge of EX_SYNC2 is aligned with the rising edge of the T0 selected input clock. 00: On target. (default) 01: 0.5 UI early. 10: 1 UI late. 11: 0.5 UI late. | | | | | |
| 1 - 0 | SYNC_PH1[1:0] | These bits set the sampling of EX_SYNC1 when EX_SYNC1 is enabled to synchronize the frame sync output signal. Nominally, the falling edge of EX_SYNC1 is aligned with the rising edge of the T0 selected input clock. 00: On target. (default) 01: 0.5 UI early. 10: 1 UI late. 11: 0.5 UI late. | | | | | |

7 THERMAL MANAGEMENT

The device operates over the industry temperature range -40°C ~ +85°C. To ensure the functionality and reliability of the device, the maximum junction temperature T_{jmax} should not exceed 125°C. In some applications, the device will consume more power and a thermal solution should be provided to ensure the junction temperature T_j does not exceed the T_{jmax} .

7.1 JUNCTION TEMPERATURE

Junction temperature T_j is the temperature of package typically at the geographical center of the chip where the device's electrical circuits are. It can be calculated as follows:

Equation 1: $T_j = T_A + P \times \theta_{JA}$

Where:

θ_{JA} = Junction-to-Ambient Thermal Resistance of the Package

T_j = Junction Temperature

T_A = Ambient Temperature

P = Device Power Consumption

In order to calculate junction temperature, an appropriate θ_{JA} must be used. The θ_{JA} is shown in [Table 32](#):

Power consumption is the core power excluding the power dissipated in the loads. [Table 33](#) provides power consumption in special environments.

Table 32: Power Consumption and Maximum Junction Temperature

| Package | Power Consumption (W) | Operating Voltage (V) | T_A (°C) | Maximum Junction Temperature (°C) |
|-------------|-----------------------|-----------------------|------------|-----------------------------------|
| VFQFPN/NL68 | 1.57 | 3.6 | 85 | 125 |

7.2 EXAMPLE OF JUNCTION TEMPERATURE CALCULATION

Assume:

$T_A = 85^\circ\text{C}$

$\theta_{JA} = \text{°C/W}$ (VFQFPN/NL68 Soldered & when airflow rate is 0 m/s)

$P = 1.57\text{W}$

Table 33: Thermal Data

| Package | Pin Count | Thermal Pad | θ_{JC} (°C/W) | θ_{JB} (°C/W) | θ_{JA} (°C/W) Air Flow in m/s | | | | | |
|-------------|-----------|---------------|----------------------|----------------------|--------------------------------------|------|------|------|------|------|
| | | | | | 0 | 1 | 2 | 3 | 4 | 5 |
| VFQFPN/NL68 | 68 | Yes/Exposed | 9.1 | 8.3 | 39.4 | 34.1 | 31.7 | 30.2 | 29.1 | 28.2 |
| VFQFPN/NL68 | 68 | Yes/Soldered* | 9.1 | 1.2 | 20.9 | 16.2 | 15.2 | 14.6 | 14.1 | 13.8 |

*note: Simulated with 3 x 3 array of thermal vias.

The junction temperature T_j can be calculated as follows:

$T_j = T_A + P \times \theta_{JA} = 85^\circ\text{C} + 1.57\text{W} \times 20.9^\circ\text{C/W} = 117.8^\circ\text{C}$

The junction temperature of 117.8°C is below the maximum junction temperature of 125°C so no extra heat enhancement is required.

In some operation environments, the calculated junction temperature might exceed the maximum junction temperature of 125°C and an external thermal solution such as a heatsink is required.

7.3 HEATSINK EVALUATION

A heatsink is expanding the surface area of the device to which it is attached. θ_{JA} is now a combination of device case and heat-sink thermal resistance, as the heat flowing from the die junction to ambient goes through the package and the heatsink. θ_{JA} can be calculated as follows:

Equation 2: $\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$

Where:

θ_{JC} = Junction-to-Case Thermal Resistance

θ_{CH} = Case-to-Heatsink Thermal Resistance

θ_{HA} = Heatsink-to-Ambient Thermal Resistance

$\theta_{CH} + \theta_{HA}$ determines which heatsink and heatsink attachment can be selected to ensure the junction temperature does not exceed the maximum junction temperature. According to Equation 1 and 2,

$\theta_{CH} + \theta_{HA}$ can be calculated as follows:

Equation 3: $\theta_{CH} + \theta_{HA} = (T_j - T_A) / P - \theta_{JC}$

Assume:

$T_j = 125^\circ\text{C}$ (T_{jmax})

$T_A = 85^\circ\text{C}$

$P = 1.57\text{W}$

$\theta_{JC} = 12.6^\circ\text{C/W}$ (VFQFPN/NL68)

$\theta_{CH} + \theta_{HA}$ can be calculated as follows:

$\theta_{CH} + \theta_{HA} = (125^\circ\text{C} - 85^\circ\text{C}) / 1.57\text{W} - 12.6^\circ\text{C/W} = 12.9^\circ\text{C/W}$

That is, if a heatsink and heatsink attachment whose $\theta_{CH} + \theta_{HA}$ is below or equal to 12.9°C/W is used in such operation environment, the junction temperature will not exceed the maximum junction temperature.

7.4 VFQFPN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in [Figure 18](#). The solderable area on the PCB, as defined

by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

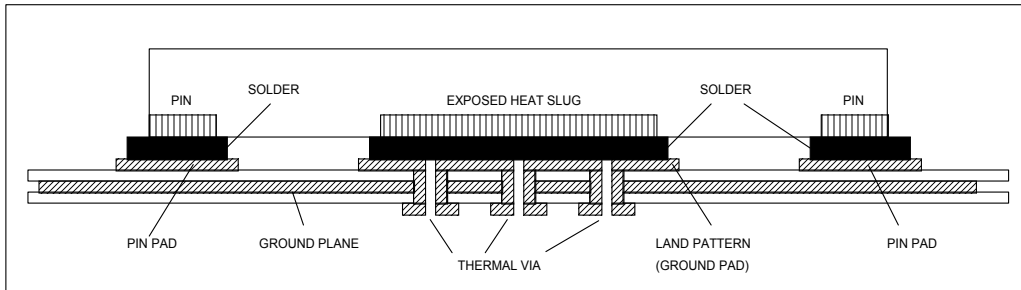


Figure 18. Assembly for Expose Pad thermal Release Path (Side View)

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as 'heat pipes'. The number of vias (i.e. 'heat pipes') are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via

diameter should be 12 to 13mils (0.30 to 0.33mm) with 1 oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern.

Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/Electrically Enhance Lead fame Base Package, Amkor Technology.

8 ELECTRICAL SPECIFICATIONS

8.1 ABSOLUTE MAXIMUM RATING

Table 34: Absolute Maximum Rating

| Symbol | Parameter | Min | Max | Unit |
|------------|----------------------------------|------|------|------|
| V_{DD} | Supply Voltage VDD | -0.5 | 4.0 | V |
| V_{IN} | Input Voltage (non-supply pins) | | 5.5 | V |
| V_{OUT} | Output Voltage (non-supply pins) | | 5.5 | V |
| T_{STOR} | Storage Temperature | -50 | +150 | °C |

8.2 RECOMMENDED OPERATION CONDITIONS

Table 35: Recommended Operation Conditions

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|-----------|-------------------------------|-----|------|------|------|---------------------------------------|
| V_{DD} | Power Supply (DC voltage) VDD | 3.0 | 3.3 | 3.6 | V | |
| T_A | Ambient Temperature Range | -40 | | +85 | °C | |
| I_{DD} | Supply Current | | 233 | 262 | mA | Exclude the loading current and power |
| P_{TOT} | Total Power Dissipation | | 0.77 | 0.94 | W | |

8.3 I/O SPECIFICATIONS

8.3.1 CMOS INPUT / OUTPUT PORT

Table 36: CMOS Input Port Electrical Characteristics

| Parameter | Description | Min | Typ | Max | Unit | Test Condition |
|-----------|--------------------|------|-----|-----|---------|----------------|
| V_{IH} | Input Voltage High | 2.0 | | | V | |
| V_{IL} | Input Voltage Low | | | 0.8 | V | |
| I_{IN} | Input Current | | | 10 | μ A | |
| V_{IN} | Input Voltage | -0.5 | | 5.5 | V | |

Table 37: CMOS Input Port with Internal Pull-Up Resistor Electrical Characteristics

| Parameter | Description | Min | Typ | Max | Unit | Test Condition |
|-----------|--------------------|------|-----|-----|------------|----------------------|
| V_{IH} | Input Voltage High | 2.0 | | | V | |
| V_{IL} | Input Voltage Low | | | 0.8 | V | |
| P_U | Pull-Up Resistor | 23 | | 38 | K Ω | TDI, TMS pin |
| | | 41 | | 82 | | \overline{RST} pin |
| | | 82 | | 165 | | |
| I_{IN} | Input Current | 85 | | 140 | μ A | TDI, TMS pin |
| | | 40 | | 80 | | \overline{RST} pin |
| | | 20 | | 40 | | |
| V_{IN} | Input Voltage | -0.5 | | 5.5 | V | |

Table 38: CMOS Input Port with Internal Pull-Down Resistor Electrical Characteristics

| Parameter | Description | Min | Typ | Max | Unit | Test Condition |
|-----------|--------------------|------|-----|-----|------------|--|
| V_{IH} | Input Voltage High | 2.0 | | | V | |
| V_{IL} | Input Voltage Low | | | 0.8 | V | |
| P_D | Pull-Down Resistor | 8 | | 14 | K Ω | \overline{TRST} and TCK pin |
| | | 16 | | 23 | | other CMOS input port with internal pull-down resistor |
| | | 183 | | 366 | | SDI, CLKE pin |
| I_{IN} | Input Current | 390 | | 640 | μ A | \overline{TRST} and TCK pin |
| | | 180 | | 340 | | other CMOS input port with internal pull-down resistor |
| | | 15 | | 30 | | SDI, CLKE pin |
| V_{IN} | Input Voltage | -0.5 | | 5.5 | V | |

Table 39: CMOS Output Port Electrical Characteristics

| Application Pin | Parameter | Description | Min | Typ | Max | Unit | Test Condition |
|-----------------|-----------|------------------------|-----|-----|----------|------|-------------------------|
| Output Clock | V_{OH} | Output Voltage High | 2.4 | | V_{DD} | V | $I_{OH} = 8 \text{ mA}$ |
| | V_{OL} | Output Voltage Low | 0 | | 0.4 | V | $I_{OL} = 8 \text{ mA}$ |
| | t_R | Rise time (20% to 80%) | | 3 | 4 | ns | 15 pF |
| | t_F | Fall time (20% to 80%) | | 3 | 4 | ns | 15 pF |
| Other Output | V_{OH} | Output Voltage High | 2.4 | | V_{DD} | V | $I_{OH} = 4 \text{ mA}$ |
| | V_{OL} | Output Voltage Low | 0 | | 0.4 | V | $I_{OL} = 4 \text{ mA}$ |
| | t_R | Rise Time (20% to 80%) | | | 10 | ns | 50 pF |
| | t_F | Fall Time (20% to 80%) | | | 10 | ns | 50 pF |

8.3.2 PECL / LVDS INPUT / OUTPUT PORT

8.3.2.1 PECL Input / Output Port

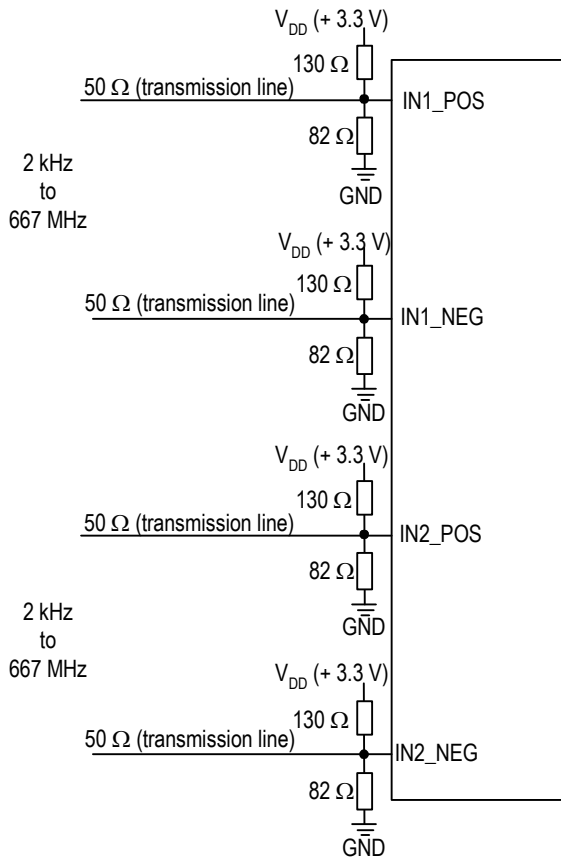


Figure 19. Recommended PECL Input Port Line Termination

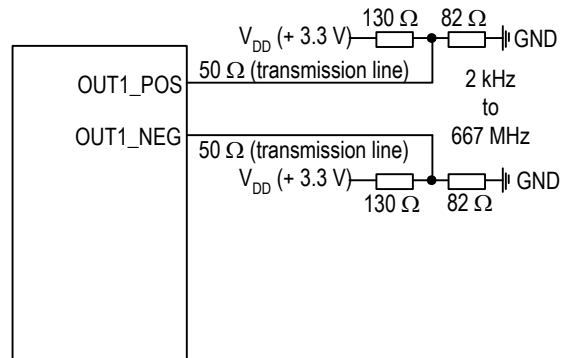


Figure 20. Recommended PECL Output Port Line Termination

Table 40: PECL Input / Output Port Electrical Characteristics

| Parameter | Description | Min | Typ | Max | Unit | Test Condition |
|-------------|---|-----------------|-----|-----------------|---------|----------------|
| V_{IL} | Input Low Voltage, Differential Inputs ¹ | $V_{DD} - 2.5$ | | $V_{DD} - 0.5$ | V | |
| V_{IH} | Input High Voltage, Differential Inputs ¹ | $V_{DD} - 2.4$ | | $V_{DD} - 0.4$ | V | |
| V_{ID} | Input Differential Voltage | 0.1 | | 1.4 | V | |
| V_{IL_S} | Input Low Voltage, Single-ended Input ² | $V_{DD} - 2.4$ | | $V_{DD} - 1.5$ | V | |
| V_{IH_S} | Input High Voltage, Single-ended Input ² | $V_{DD} - 1.3$ | | $V_{DD} - 0.5$ | V | |
| I_{IH} | Input High Current, Input Differential Voltage $V_{ID} = 1.4$ V | -10 | | 10 | μ A | |
| I_{IL} | Input Low Current, Input Differential Voltage $V_{ID} = 1.4$ V | -10 | | 10 | μ A | |
| V_{OL} | Output Voltage Low ³ | $V_{DD} - 2.1$ | | $V_{DD} - 1.62$ | V | |
| V_{OH} | Output Voltage High ³ | $V_{DD} - 1.25$ | | $V_{DD} - 0.88$ | V | |
| V_{OD} | Output Differential Voltage ³ | 580 | | 900 | mV | |
| t_{RISE} | Output Rise time (20% to 80%) | 200 | | 300 | pS | |
| t_{FALL} | Output Fall time (20% to 80%) | 200 | | 300 | pS | |
| t_{SKEW} | Output Differential Skew | | | 50 | pS | |

Note:

1. Assuming a differential input voltage of at least 100 mV.
2. Unused differential input terminated to $V_{DD}-1.4$ V.
3. With 50 Ω load on each pin to $V_{DD}-2$ V, i.e. 82 to GND and 130 to V_{DD} .

8.3.2.2 LVDS Input / Output Port

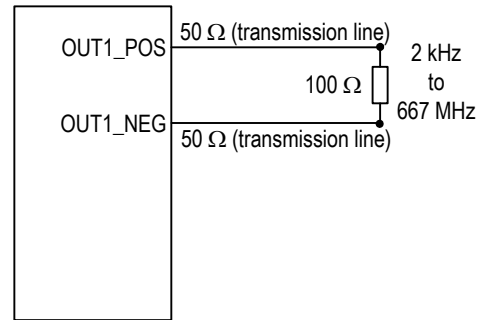
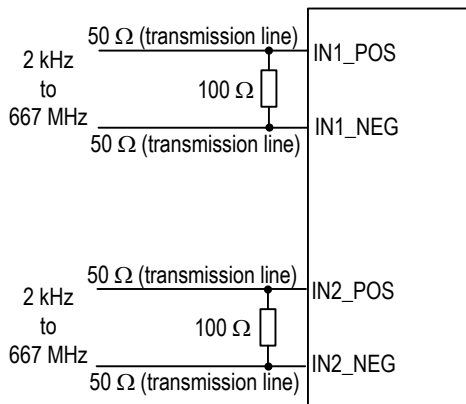


Figure 22. Recommended LVDS Output Port Line Termination

Figure 21. Recommended LVDS Input Port Line Termination

Table 41: LVDS Input / Output Port Electrical Characteristics

| Parameter | Description | Min | Typ | Max | Unit | Test Condition |
|------------------|--|------|------|------|----------|---------------------------------|
| V_{CM} | Input Common-mode Voltage Range | 0 | 1200 | 2400 | mV | |
| V_{DIFF} | Input Peak Differential Voltage | 100 | | 900 | mV | |
| V_{IDTH} | Input Differential Threshold | -100 | | 100 | mV | |
| R_{TERM} | External Differential Termination Impedance | 95 | 100 | 105 | Ω | |
| V_{OH} | Output Voltage High | 1350 | | 1475 | mV | $R_{LOAD} = 100 \Omega \pm 1\%$ |
| V_{OL} | Output Voltage Low | 925 | | 1100 | mV | $R_{LOAD} = 100 \Omega \pm 1\%$ |
| V_{OD} | Differential Output Voltage | 250 | | 400 | mV | $R_{LOAD} = 100 \Omega \pm 1\%$ |
| V_{OS} | Output Offset Voltage | 1125 | | 1275 | mV | $R_{LOAD} = 100 \Omega \pm 1\%$ |
| R_O | Differential Output Impedance | 80 | 100 | 120 | Ω | $V_{CM} = 1.0 V$ or $1.4 V$ |
| ΔR_O | R_O Mismatch between A and B | | | 20 | % | $V_{CM} = 1.0 V$ or $1.4 V$ |
| ΔV_{OD} | Change in V_{OD} between Logic 0 and Logic 1 | | | 25 | mV | $R_{LOAD} = 100 \Omega \pm 1\%$ |
| ΔV_{OS} | Change in V_{OS} between Logic 0 and Logic 1 | | | 25 | mV | $R_{LOAD} = 100 \Omega \pm 1\%$ |
| I_{SA}, I_{SB} | Output Current | | | 24 | mA | Driver shorted to GND |
| I_{SAB} | Output Current | | | 12 | mA | Driver shorted together |
| t_{RISE} | Output Rise time (20% to 80%) | 200 | | 300 | pS | $R_{LOAD} = 100 \Omega \pm 1\%$ |
| t_{FALL} | Output Fall time (20% to 80%) | 200 | | 300 | pS | $R_{LOAD} = 100 \Omega \pm 1\%$ |
| t_{SKEW} | Output Differential Skew | | | 50 | pS | $R_{LOAD} = 100 \Omega \pm 1\%$ |

8.3.2.3 Single-Ended Input for Differential Input

This is a recommended and tested interface circuit to drive differential input with a single-ended signal.

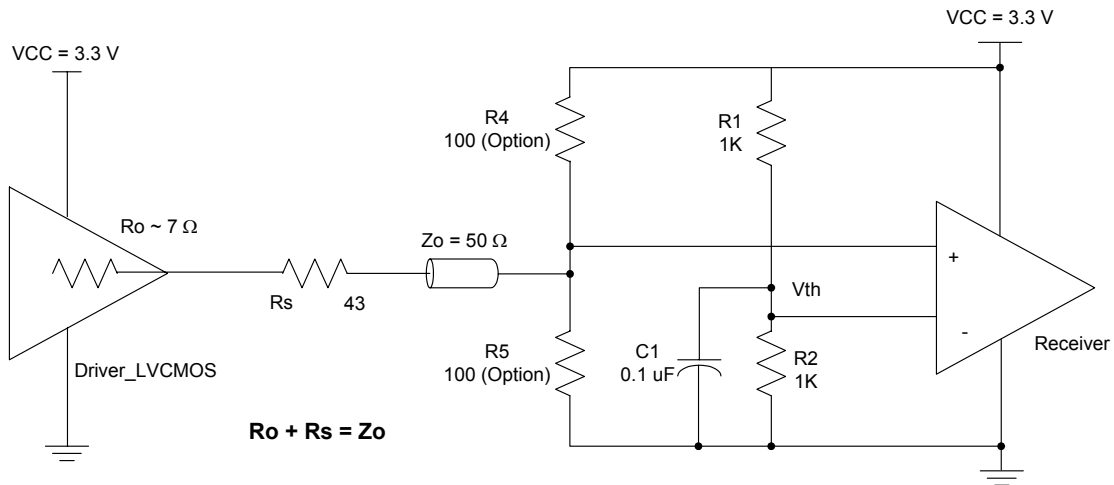


Figure 23. Example of Single-Ended Signal to Drive Differential Input

$$V_{th} = VCC * [R2 / (R1 + R2)]$$

For the example in Figure 23, R1 = R2, so $V_{th} = VCC / 2 = 1.65\text{ V}$

The suggested single-ended signal input:

$$V_{IHmax} = VCC$$

$$V_{ILmin} = 0\text{ V}$$

$$V_{swing} = 0.6\text{ V} \sim VCC$$

$$DC\text{ offset (Swing Center)} = V_{th} / 2 \pm V_{swing} * 10\%$$

8.4 JITTER & WANDER PERFORMANCE

Table 42: Output Clock Jitter Generation

| Test Definition ¹ | Peak to Peak Typ | RMS Typ | Note | Test Filter |
|--|------------------|--------------|--|------------------|
| N x 2.048MHz without APLL | <2 ns | <200 ps | | 20 Hz - 100 kHz |
| N x 2.048MHz with T0/T4 APLL | <1 ns | <100 ps | See Table 43: Output Clock Phase Noise for details | 20 Hz - 100 kHz |
| N x 1.544 MHz without APLL | <2 ns | <200 ps | | 10 Hz - 40 kHz |
| N x 1.544 MHz with T0/T4 APLL | <1 ns | <100 ps | See Table 43: Output Clock Phase Noise for details | 10 Hz - 40 kHz |
| 44.736 MHz with T0/T4 APLL | <1 ns | <100 ps | See Table 43: Output Clock Phase Noise for details | 100 Hz - 800 kHz |
| 44.736 MHz without APLL | <2 ns | <200 ps | | 100 Hz - 800 kHz |
| 34.368 MHz with T0/T4 APLL | <1 ns | <100 ps | See Table 43: Output Clock Phase Noise for details | 10 Hz - 400 kHz |
| 34.368 MHz without APLL | <2 ns | <200 ps | | 10 Hz - 400 kHz |
| OC-3 (Chip T0 DPLL + T0/T4 APLL) 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz output | 0.004 UI p-p | 0.001 UI RMS | GR-253, G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps) | 12 kHz - 1.3 MHz |
| | 0.004 UI p-p | 0.001 UI RMS | G.813 Option 1, G.812 limit 0.5 UI p-p (1 UI-6430 ps) | 500 Hz - 1.3 MHz |
| | 0.001 UI p-p | 0.001 UI RMS | G.813 Option 1 limit 0.1 UI p-p (1 UI-6430 ps) | 65 kHz - 1.3 MHz |
| OC-12 (Chip T0 DPLL + T0/T4 APLL) 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz output + Intel GD16523 + Optical transceiver) | 0.018 UI p-p | 0.007 UI RMS | GR-253, G.813 Option 2 limit 0.1 UI p-p (1 UI-1608 ps) | 12 kHz - 5 MHz |
| | 0.028 UI p-p | 0.009 UI RMS | G.813 Option 1, G.812 limit 0.5 UI p-p (1 UI-1608 ps) | 1 kHz - 5 MHz |
| | 0.002 UI p-p | 0.001 UI RMS | G.813 Option 1, G.812 limit 0.1 UI p-p (1 UI-160 8ps) | 250 kHz - 5 MHz |
| STM-16 (Chip T0 DPLL + T0/T4 APLL) 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz output + Intel GD16523 + Optical transceiver) | 0.162 UI p-p | 0.03 UI RMS | G.813 Option 1, G.812 limit 0.5 UI p-p (1 UI-402 ps) | 5 kHz - 20 MHz |
| | 0.01 UI p-p | 0.009 UI RMS | G.813 Option 1, G.812 limit 0.1 UI p-p (1 UI-402 ps) | 1 MHz - 20 MHz |
| Note: 1. CMAC E2747 TCXO is used. | | | | |

Table 43: Output Clock Phase Noise

| Output Clock ¹ | @100Hz Offset Typ | @1kHz Offset Typ | @10kHz Offset Typ | @100kHz Offset Typ | @1MHz Offset Typ | @5MHz Offset Typ | Unit |
|-----------------------------------|-------------------|------------------|-------------------|--------------------|------------------|------------------|--------|
| 622.08 MHz (T0 DPLL + T0/T4 APLL) | -70 | -86 | -95 | -100 | -107 | -128 | dBc/Hz |
| 155.52 MHz (T0 DPLL + T0/T4 APLL) | -82 | -98 | -107 | -112 | -119 | -140 | dBc/Hz |
| 38.88 MHz (T0 DPLL + T0/T4 APLL) | -94 | -110 | -118 | -124 | -131 | -143 | dBc/Hz |
| 16E1 (T0/T4 APLL) | -94 | -110 | -118 | -125 | -131 | -142 | dBc/Hz |
| 16T1 (T0/T4 APLL) | -95 | -112 | -120 | -127 | -132 | -143 | dBc/Hz |
| E3 (T0/T4 APLL) | -93 | -109 | -116 | -124 | -131 | -138 | dBc/Hz |
| T3 (T0/T4 APLL) | -92 | -108 | -116 | -122 | -126 | -141 | dBc/Hz |

Note:
1. CMAC E2747 TCXO is used.

Table 44: Input Jitter Tolerance (155.52 MHz)

| Jitter Frequency | Jitter Tolerance Amplitude (UI p-p) |
|------------------|-------------------------------------|
| 12 μHz | > 2800 |
| 178 μHz | > 2800 |
| 1.6 mHz | > 311 |
| 15.6 mHz | > 311 |
| 0.125 Hz | > 39 |
| 19.3 Hz | > 39 |
| 500 Hz | > 1.5 |
| 6.5 kHz | > 1.5 |
| 65 kHz | > 0.15 |
| 1.3 MHz | > 0.15 |

Table 46: Input Jitter Tolerance (2.048 MHz)

| Jitter Frequency | Jitter Tolerance Amplitude (UI p-p) |
|------------------|-------------------------------------|
| 1 Hz | 150 |
| 5 Hz | 140 |
| 20 Hz | 130 |
| 300 Hz | 40 |
| 400 Hz | 33 |
| 700 Hz | 18 |
| 2400 Hz | 5.5 |
| 10 kHz | 1.3 |
| 50 kHz | 0.4 |
| 100 kHz | 0.4 |

Table 45: Input Jitter Tolerance (1.544 MHz)

| Jitter Frequency | Jitter Tolerance Amplitude (UI p-p) |
|------------------|-------------------------------------|
| 1 Hz | 150 |
| 5 Hz | 140 |
| 20 Hz | 130 |
| 300 Hz | 38 |
| 400 Hz | 25 |
| 700 Hz | 15 |
| 2400 Hz | 5 |
| 10 kHz | 1.2 |
| 40 kHz | 0.5 |

Table 47: Input Jitter Tolerance (8 kHz)

| Jitter Frequency | Jitter Tolerance Amplitude (UI p-p) |
|------------------|-------------------------------------|
| 1 Hz | 0.8 |
| 5 Hz | 0.7 |
| 20 Hz | 0.6 |
| 300 Hz | 0.16 |
| 400 Hz | 0.14 |
| 700 Hz | 0.07 |
| 2400 Hz | 0.02 |
| 3600 Hz | 0.01 |

Table 48: T0 DPLL Jitter Transfer & Damping Factor

| 3 dB Bandwidth | Programmable Damping Factor |
|----------------|-----------------------------|
| 0.1 Hz | 1.2, 2.5, 5, 10, 20 |
| 0.3 Hz | 1.2, 2.5, 5, 10, 20 |
| 0.6 Hz | 1.2, 2.5, 5, 10, 20 |
| 1.2 Hz | 1.2, 2.5, 5, 10, 20 |
| 2.5 Hz | 1.2, 2.5, 5, 10, 20 |
| 4 Hz | 1.2, 2.5, 5, 10, 20 |
| 8 Hz | 1.2, 2.5, 5, 10, 20 |
| 18 Hz | 1.2, 2.5, 5, 10, 20 |
| 35 Hz | 1.2, 2.5, 5, 10, 20 |
| 70 Hz | 1.2, 2.5, 5, 10, 20 |
| 560 Hz | 1.2, 2.5, 5, 10, 20 |

8.5 OUTPUT WANDER GENERATION

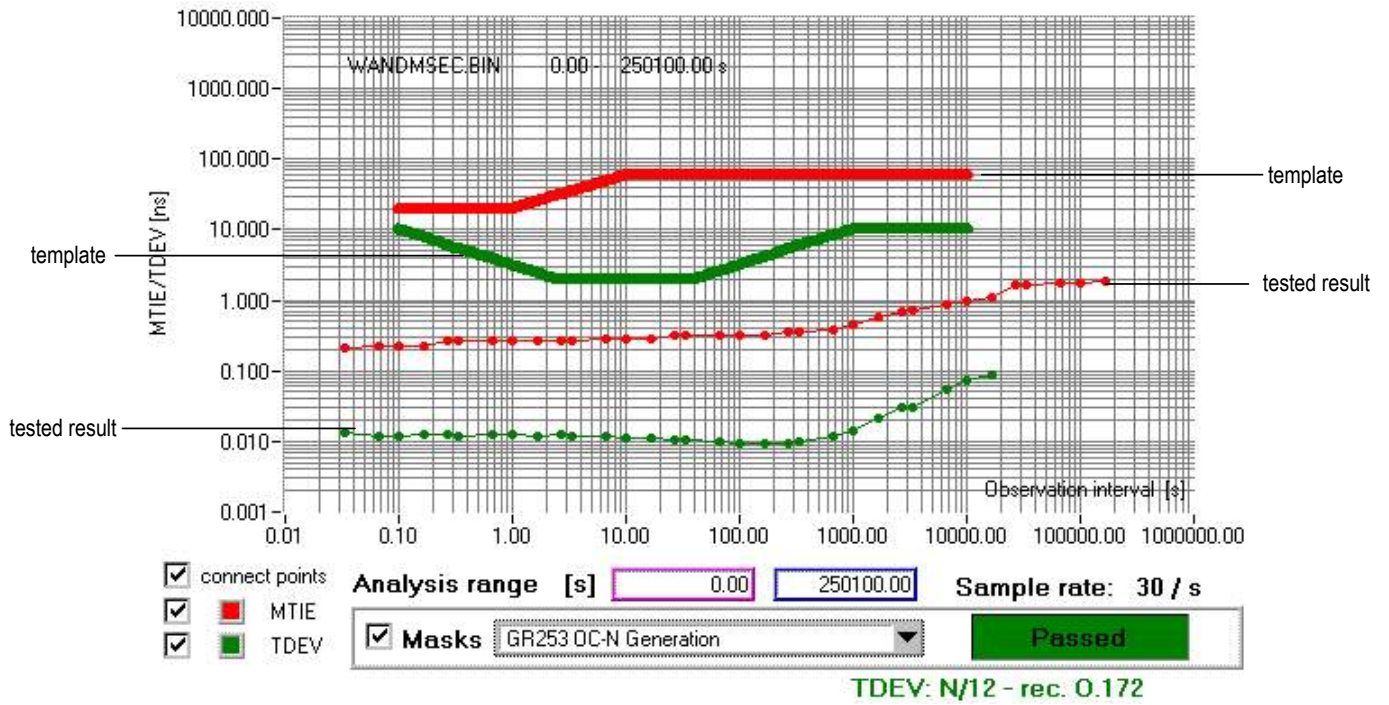


Figure 24. Output Wander Generation

8.6 INPUT / OUTPUT CLOCK TIMING

The inputs and outputs are aligned ideally. But due to the circuit delays, there is delay between the inputs and outputs.

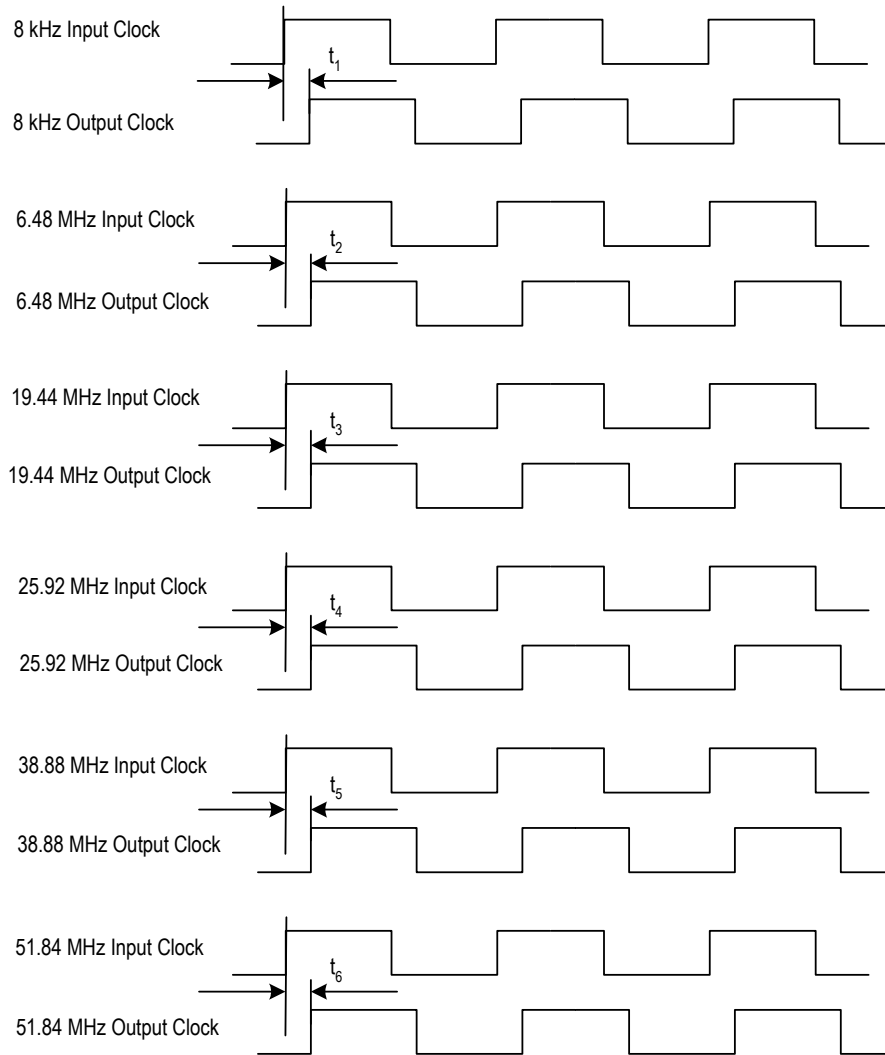


Figure 25. Input / Output Clock Timing

Table 49: Input/Output Clock Timing

| Symbol | Typical Delay ¹ (ns) | Peak to Peak Delay Variation (ns) |
|--------|---------------------------------|-----------------------------------|
| t_1 | 4 | 1.6 |
| t_2 | 1 | 1.6 |
| t_3 | 1 | 1.6 |
| t_4 | 2 | 1.6 |
| t_5 | 1.4 | 1.6 |
| t_6 | 3 | 1.6 |

Note:

1. Typical delay provided as reference only.

8.7 OUTPUT CLOCK TIMING

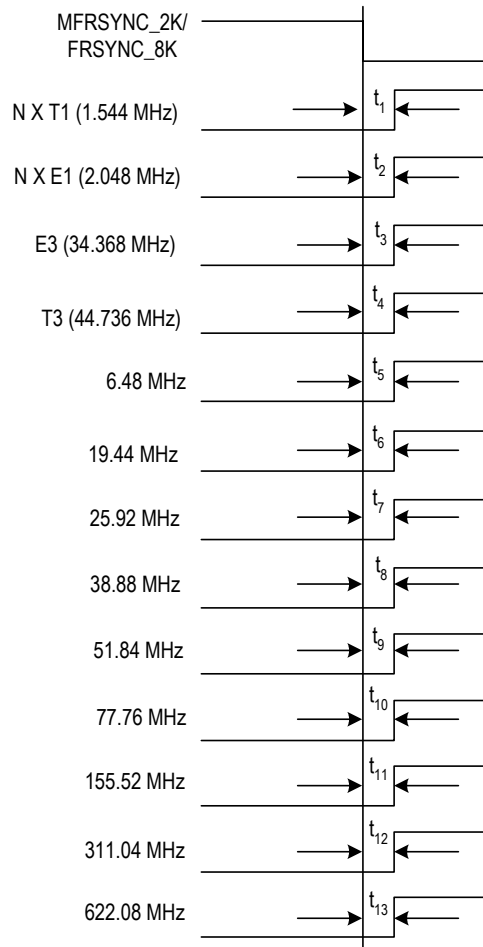


Table 50: Output Clock Timing

| Symbol | Typical Delay (ns) | Peak to Peak Delay Variation (ns) |
|----------|--------------------|-----------------------------------|
| t_1 | 0 | 2 |
| t_2 | 0 | 2 |
| t_3 | 0 | 2 |
| t_4 | 0 | 2 |
| t_5 | 0 | 2 |
| t_6 | 0 | 2 |
| t_7 | 0 | 2 |
| t_8 | 0 | 2 |
| t_9 | 0 | 2 |
| t_{10} | 0 | 2 |
| t_{11} | 0 | 1.5 |
| t_{12} | 0 | 1.5 (not recommended to use) |
| t_{13} | 0 | 1.5 (not recommended to use) |



| | | |
|--------------|-----|--|
| 3G | --- | Third Generation |
| ADSL | --- | Asymmetric Digital Subscriber Line |
| AMI | --- | Alternate Mark Inversion |
| APLL | --- | Analog Phase Locked Loop |
| ATM | --- | Asynchronous Transfer Mode |
| BITS | --- | Building Integrated Timing Supply |
| CMOS | --- | Complementary Metal-Oxide Semiconductor |
| DCO | --- | Digital Controlled Oscillator |
| DPLL | --- | Digital Phase Locked Loop |
| DSL | --- | Digital Subscriber Line |
| DSLAM | --- | Digital Subscriber Line Access MUX |
| DWDM | --- | Dense Wavelength Division Multiplexing |
| EPROM | --- | Erasable Programmable Read Only Memory |
| GPS | --- | Global Positioning System |
| GSM | --- | Global System for Mobile Communications |
| IIR | --- | Infinite Impulse Response |
| IP | --- | Internet Protocol |
| ISDN | --- | Integrated Services Digital Network |
| JTAG | --- | Joint Test Action Group |
| LOS | --- | Loss Of Signal |
| LPF | --- | Low Pass Filter |
| LVDS | --- | Low Voltage Differential Signal |
| MTIE | --- | Maximum Time Interval Error |
| MUX | --- | Multiplexer |
| OBSAI | --- | Open Base Station Architecture Initiative |
| OC-n | --- | Optical Carried rate, n = 1, 3, 12, 48, 192, 768; 51 Mbit/s, 155 Mbit/s, 622 Mbit/s, 2.5 Gbit/s, 10 Gbit/s, 40 Gbit/s. |

| | | |
|----------|-----|---|
| PBO | --- | Phase Build-Out |
| PDH | --- | Plesiochronous Digital Hierarchy |
| PECL | --- | Positive Emitter Coupled Logic |
| PFD | --- | Phase & Frequency Detector |
| PLL | --- | Phase Locked Loop |
| RMS | --- | Root Mean Square |
| PRS | --- | Primary Reference Source |
| SDH | --- | Synchronous Digital Hierarchy |
| SEC | --- | SDH / SONET Equipment Clock |
| SMC | --- | SONET Minimum Clock |
| SONET | --- | Synchronous Optical Network |
| SSU | --- | Synchronization Supply Unit |
| STM | --- | Synchronous Transfer Mode |
| TCM-ISDN | --- | Time Compression Multiplexing Integrated Services Digital Network |
| TDEV | --- | Time Deviation |
| UI | --- | Unit Interval |
| WLL | --- | Wireless Local Loop |



| | | | |
|--|----|---|--------|
| A | | Frequency Hard Alarm | 22, 27 |
| Averaged Phase Error | 31 | Frequency Hard Alarm Threshold | 22 |
| B | | H | |
| Bandwidths and Damping Factors | 31 | Hard Limit | 25 |
| Acquisition Bandwidth and Damping Factor | 31 | Holdover Frequency Offset | 32 |
| Locked Bandwidth and Damping Factor | 31 | I | |
| Starting Bandwidth and Damping Factor | 31 | IIR | 32 |
| C | | Input Clock Frequency | 22 |
| Calibration | 17 | Input Clock Selection | 23 |
| Coarse Phase Loss | 25 | Automatic selection | 24, 27 |
| Crystal Oscillator | 17 | External Fast selection | 27 |
| Current Frequency Offset | 31 | Forced selection | 24, 27 |
| D | | Internal Leaky Bucket Accumulator | 21 |
| DCO | 31 | Bucket Size | 21 |
| Division Factor | 19 | Decay Rate | 21 |
| DPLL Hard Alarm | 25 | Lower Threshold | 21 |
| DPLL Hard Limit | 25 | Upper Threshold | 21 |
| DPLL Operating Mode | | L | |
| Free-Run mode | 31 | Limit | 34 |
| Holdover mode | 31 | LPF | 31 |
| Automatic Fast Averaged | 32 | M | |
| Automatic Instantaneous | 32 | Master Clock | 17 |
| Automatic Slow Averaged | 32 | N | |
| Manual | 32 | No-activity Alarm | 21, 27 |
| Locked mode | 31 | P | |
| Temp-Holdover mode | 31 | PFD | 31 |
| Lost-Phase mode | 31 | Phase Lock Alarm | 25, 27 |
| Pre-Locked mode | 31 | Phase-compared | 25, 34 |
| Pre-Locked2 mode | 32 | Phase-time | 34 |
| DPLL Soft Alarm | 25 | Pre-Divider | 19 |
| DPLL Soft Limit | 25 | DivN Divider | 19 |
| E | | HF Divider | 19 |
| External Sync Alarm | 38 | Lock 8k Divider | 19 |
| F | | | |
| Fast Loss | 25 | | |
| Fine Phase Loss | 25 | | |

| | | | |
|-----------------------------------|----|----------------------------|----|
| R | | Non-Revertive switch | 27 |
| Reference Clock | 22 | Revertive switch | 27 |
| S | | State Machine | 29 |
| Selected Input Clock Switch | 27 | V | |
| | | Validity | 27 |

PACKAGE DIMENSIONS

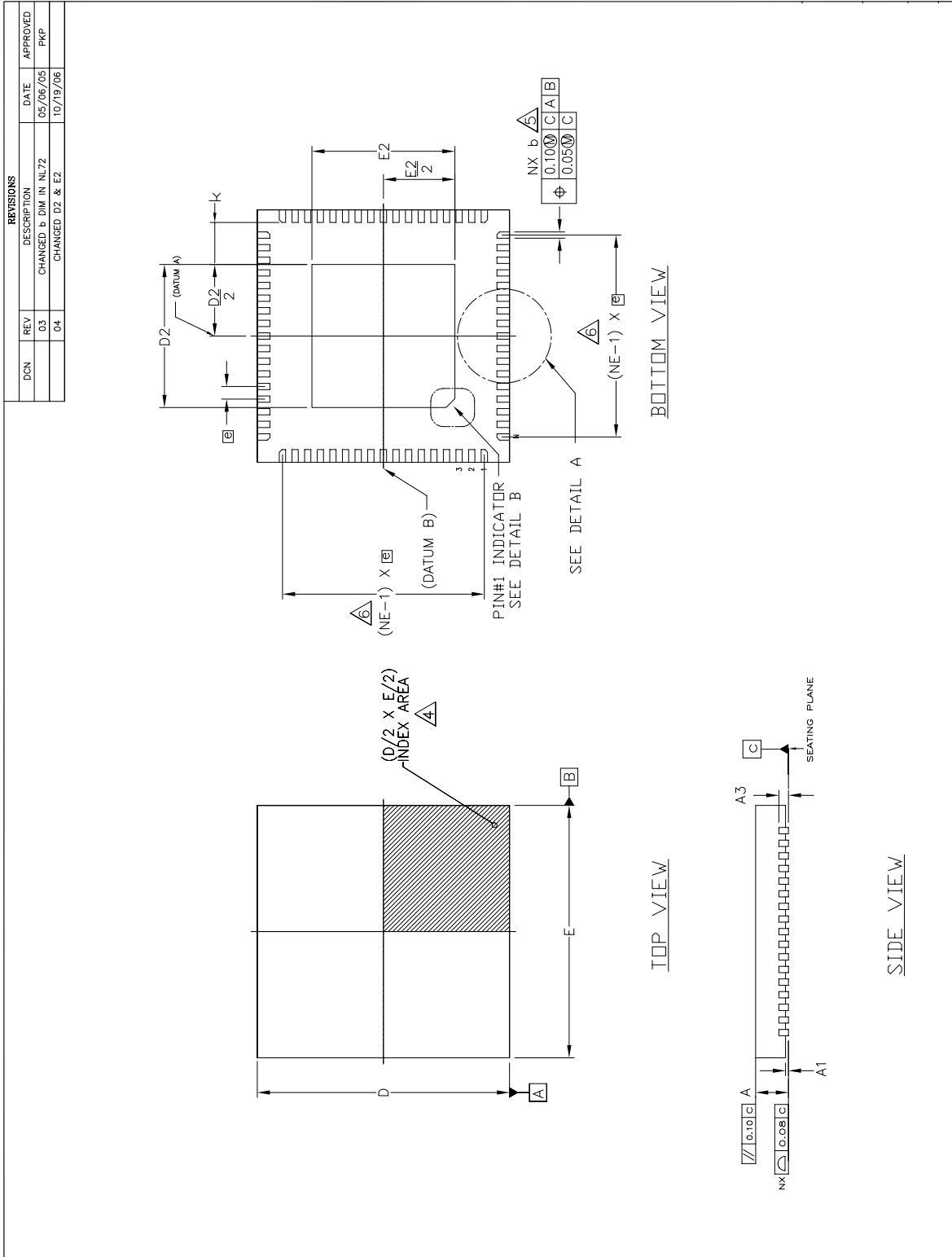


Figure 26. 68-Pin NL Package Dimensions (a) (in Millimeters)

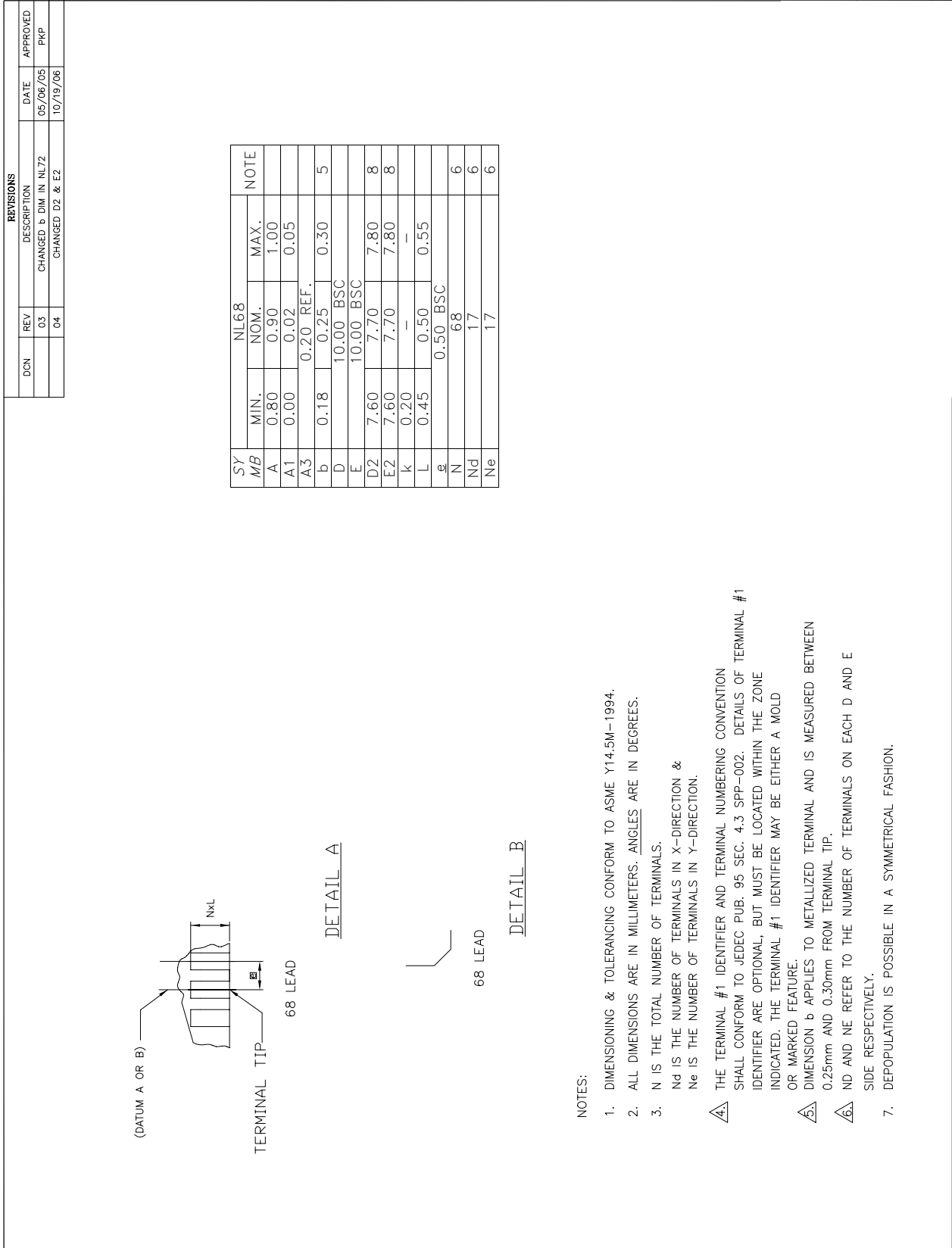
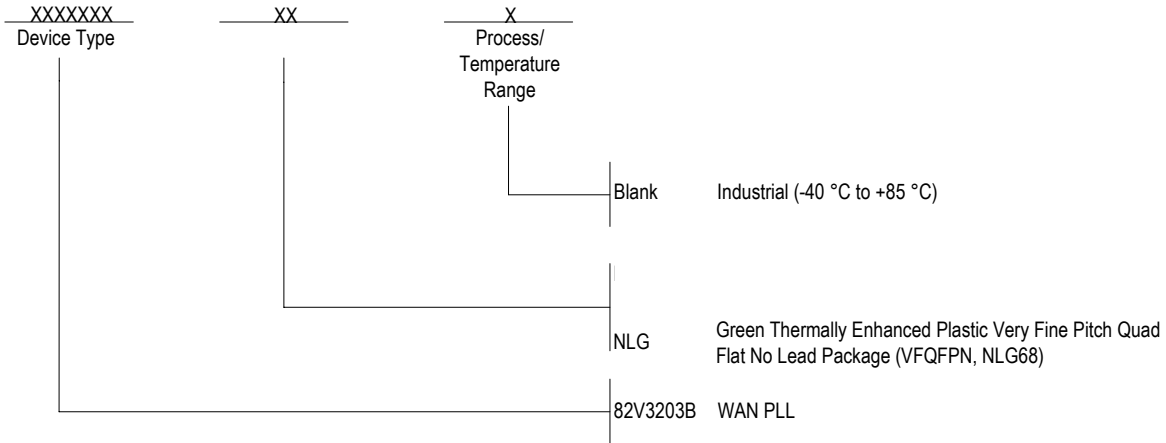


Figure 27. 68-Pin NL Package Dimensions (b) (in Millimeters)

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

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- 3/20/2009 Pages 101, 102, 109
- 5/22/2009 Pages 13, 18, 109
- 7/23/2009 Pages 14, 105
- 9/11/2009 Page 45

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