



SYNCHRONOUS ETHERNET
IDT WAN PLL™

IDT82V3390
DATASHEET

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Table of Contents

Datasheet

FEATURES.....	9
HIGHLIGHTS.....	9
MAIN FEATURES	9
OTHER FEATURES.....	9
APPLICATIONS.....	9
DESCRIPTION.....	10
FUNCTIONAL BLOCK DIAGRAM	11
1 PIN ASSIGNMENT	12
2 PIN DESCRIPTION	13
3 FUNCTIONAL DESCRIPTION	19
3.1 RESET	19
3.2 MASTER CLOCK	19
3.3 INPUT CLOCKS & FRAME SYNC SIGNAL	20
3.3.1 Input Clocks	20
3.3.2 Frame SYNC Input Signals	20
3.4 INPUT CLOCK PRE-DIVIDER	21
3.5 INPUT CLOCK QUALITY MONITORING	23
3.5.1 LOS Monitoring	23
3.5.2 Activity Monitoring	23
3.5.3 Frequency Monitoring	24
3.6 T0 / T4 DPLL INPUT CLOCK SELECTION	26
3.6.1 External Fast Selection (T0 only)	26
3.6.2 Forced Selection	27
3.6.3 Automatic Selection	27
3.7 SELECTED INPUT CLOCK MONITORING	28
3.7.1 T0 / T4 DPLL Locking Detection	28
3.7.1.1 Fast Loss	28
3.7.1.2 Coarse Phase Loss	28
3.7.1.3 Fine Phase Loss	28
3.7.1.4 Hard Limit Exceeding	28
3.7.2 Locking Status	28
3.7.3 Phase Lock Alarm (T0 only)	29
3.8 INPUT CLOCK SELECTION	30
3.8.1 Input Clock Validity	30
3.8.2 Input Clock Selection	30
3.8.2.1 Revertive Switching	30
3.8.2.2 Non-Revertive Switching (T0 only)	31
3.8.3 Selected / Qualified Input Clocks Indication	31
3.9 SELECTED INPUT CLOCK STATUS VS. DPLL OPERATING MODE	32
3.9.1 T0 Selected Input Clock vs. DPLL Operating Mode	32
3.9.2 T4 Selected Input Clock vs. DPLL Operating Mode	34
3.10 T0 / T4 DPLL OPERATING MODE	35
3.10.1 T0 DPLL Operating Mode	35
3.10.1.1 Free-Run Mode	35
3.10.1.2 Pre-Locked Mode	35
3.10.1.3 Locked Mode	35

- 3.10.1.3.1 Temp-Holdover Mode 35
- 3.10.1.4 Lost-Phase Mode 35
- 3.10.1.5 Holdover Mode 35
 - 3.10.1.5.1 Automatic Instantaneous 36
 - 3.10.1.5.2 Automatic Slow Averaged 36
 - 3.10.1.5.3 Automatic Fast Averaged 36
 - 3.10.1.5.4 Manual 36
 - 3.10.1.5.5 Holdover Frequency Offset Read 36
- 3.10.1.6 Pre-Locked2 Mode 36
- 3.10.2 T4 DPLL Operating Mode 36**
 - 3.10.2.1 Free-Run Mode 36
 - 3.10.2.2 Locked Mode 36
 - 3.10.2.3 Holdover Mode 36
- 3.11 T0 / T4 DPLL OUTPUT 38**
 - 3.11.1 PFD Output Limit 38
 - 3.11.2 Frequency Offset Limit 38
 - 3.11.3 Hitless Reference Switching (T0 only) 38
 - 3.11.4 Phase Offset Selection (T0 only) 38
 - 3.11.5 Five Paths of T0 / T4 DPLL Outputs 38
 - 3.11.5.1 T0 Path 38
 - 3.11.5.2 T4 Path 38
- 3.12 T0 / T4 APLL 40**
 - 3.12.1 OPTIONAL EXTERNAL FILTER 40
- 3.13 OUTPUT CLOCKS & FRAME SYNC SIGNALS 41**
 - 3.13.1 Output Clocks 41
 - 3.13.2 Frame SYNC Output Signals 43
- 3.14 MASTER / SLAVE CONFIGURATION 45**
- 3.15 INTERRUPT SUMMARY 46**
- 3.16 T0 AND T4 SUMMARY 46**
- 3.17 POWER SUPPLY FILTERING TECHNIQUES 47**
- 4 TYPICAL APPLICATION 48**
- 4.1 MASTER / SLAVE APPLICATION 48**
- 5 MICROPROCESSOR INTERFACE 49**
 - 5.1 EPROM MODE 51
 - 5.2 MULTIPLEXED MODE 52
 - 5.3 INTEL MODE 55
 - 5.4 MOTOROLA MODE 57
 - 5.5 SERIAL MODE 59
 - 5.6 I2C MODE 61
 - 5.6.1 I2C Device address 61
 - 5.6.2 I2C Bus Timing 61
 - 5.6.3 Supported Transactions 61
- 6 JTAG 63**
- 7 PROGRAMMING INFORMATION 64**
 - 7.1 REGISTER MAP 64
 - 7.2 REGISTER DESCRIPTION 70
 - 7.2.1 Global Control Registers 70
 - 7.2.2 Interrupt Registers 79
 - 7.2.3 Input Clock Frequency & Priority Configuration Registers 84
 - 7.2.4 Input Clock Quality Monitoring Configuration & Status Registers 107
 - 7.2.5 T0 / T4 DPLL Input Clock Selection Registers 123
 - 7.2.6 T0 / T4 DPLL State Machine Control Registers 127
 - 7.2.7 T0 / T4 DPLL & APLL Configuration Registers 129

7.2.8 Output Configuration Registers 143

7.2.9 Phase Transient Monitor & Phase Offset Control Registers 154

7.2.10 Synchronization Configuration Registers 155

8 THERMAL MANAGEMENT 156

8.1 JUNCTION TEMPERATURE 156

8.2 EXAMPLE OF JUNCTION TEMPERATURE CALCULATION 156

8.3 HEATSINK EVALUATION 156

8.4 TQFP EPAD THERMAL RELEASE PATH 157

9 ELECTRICAL SPECIFICATIONS 158

9.1 ABSOLUTE MAXIMUM RATING 158

9.2 RECOMMENDED OPERATION CONDITIONS 158

9.3 I/O SPECIFICATIONS 159

9.3.1 AMI Input / Output Port 159

9.3.1.1 Structure 159

9.3.1.2 I/O Level 159

9.3.1.3 Over-Voltage Protection 161

9.3.2 CMOS Input / Output Port 161

9.3.3 PECL / LVDS Input / Output Port 162

9.3.3.1 PECL Input / Output Port 162

9.3.3.2 LVDS Input / Output Port 164

9.3.3.3 Single-Ended Input for Differential Input 165

9.4 JITTER PERFORMANCE 166

9.5 OUTPUT WANDER GENERATION 170

9.6 INPUT / OUTPUT CLOCK TIMING 171

9.7 OUTPUT CLOCK TIMING 172

PACKAGE DIMENSIONS..... 178

ORDERING INFORMATION..... 181

REVISION HISTORY 181



List of Tables Datasheet

Table 1: Pin Description	13
Table 2: Related Bit / Register in Chapter 3.2	19
Table 3: Related Bit / Register in Chapter 3.3	20
Table 4: Pre-Divider Function	22
Table 5: Related Bit / Register in Chapter 3.5	25
Table 6: Input Clock Selection for T0 Path	26
Table 7: Input Clock Selection for T4 Path	26
Table 8: External Fast Selection	26
Table 9: Related Bit / Register in Chapter 3.6	27
Table 10: Coarse Phase Limit Programming (the selected input clock of 2 kHz, 4 kHz or 8 kHz)	28
Table 11: Coarse Phase Limit Programming (the selected input clock of other than 2 kHz, 4 kHz and 8 kHz)	28
Table 12: Related Bit / Register in Chapter 3.7	29
Table 13: Conditions of Qualified Input Clocks Available for T0 & T4 Selection	30
Table 14: Related Bit / Register in Chapter 3.8	31
Table 15: T0 DPLL Operating Mode Control	32
Table 16: T4 DPLL Operating Mode Control	34
Table 17: Related Bit / Register in Chapter 3.9	34
Table 18: Frequency Offset Control in Temp-Holdover Mode	35
Table 19: Frequency Offset Control in Holdover Mode	36
Table 20: Holdover Frequency Offset Read	36
Table 21: Related Bit / Register in Chapter 3.10	37
Table 22: Related Bit / Register in Chapter 3.11	39
Table 23: Related Bit / Register in Chapter 3.12	40
Table 24: T0 / T4 APLL Approximate Loop Bandwidth Selection	40
Table 25: Outputs on OUT1 ~ OUT7 if Derived from T0/T4 DPLL Outputs	41
Table 26: Outputs on OUT1 ~ OUT7 if Derived from T0/T4 APLL1	42
Table 27: Outputs on OUT8 & OUT9	42
Table 28: Synchronization Control	43
Table 29: Related Bit / Register in Chapter 3.13	44
Table 30: Device Master / Slave Control	45
Table 31: Related Bit / Register in Chapter 3.15	46
Table 32: Microprocessor Interface	49
Table 33: Microprocessor Interface Pins	50
Table 34: Access Timing Characteristics in EPROM Mode	51
Table 35: Read Timing Characteristics in Multiplexed Mode	52
Table 36: Write Timing Characteristics in Multiplexed Mode	54
Table 37: Read Timing Characteristics in Intel Mode	55
Table 38: Write Timing Characteristics in Intel Mode	56
Table 39: Read Timing Characteristics in Motorola Mode	57
Table 40: Write Timing Characteristics in Motorola Mode	58
Table 41: Read Timing Characteristics in Serial Mode	59
Table 42: Write Timing Characteristics in Serial Mode	60
Table 43: Description of Timing Parameters of I2C Master Interface	61
Table 44: Description of I2C Slave Interface Supported Transactions	62
Table 45: JTAG Timing Characteristics	63
Table 46: Register List and Map	64
Table 47: Power Consumption and Maximum Junction Temperature	156
Table 48: Thermal Data	156

Table 49: Absolute Maximum Rating 158

Table 50: Recommended Operation Conditions 158

Table 51: AMI Input / Output Port Electrical Characteristics 160

Table 52: CMOS Input Port Electrical Characteristics 161

Table 53: CMOS Input Port with Internal Pull-Up Resistor Electrical Characteristics 161

Table 54: CMOS Input Port with Internal Pull-Down Resistor Electrical Characteristics 161

Table 55: CMOS Output Port Electrical Characteristics 161

Table 56: PECL Input / Output Port Electrical Characteristics 163

Table 57: LVDS Input / Output Port Electrical Characteristics 164

Table 58: Output Clock Jitter Generation - External T0 APLL Loop Filter 166

Table 59: Output Clock Jitter Generation - External T0 APLL Loop Filter 169

Table 60: Input/Output Clock Timing 1 171

Table 61: Output Clock Timing 173



List of Figures Datasheet

Figure 1. Functional Block Diagram	11
Figure 2. Pin Assignment (Top View)	12
Figure 3. Pre-Divider for An Input Clock	22
Figure 4. Input Clock Activity Monitoring	23
Figure 5. Hysteresis Frequency Monitoring	24
Figure 6. External Fast Selection	26
Figure 7. Qualified Input Clocks for Automatic Selection	27
Figure 8. T0 Selected Input Clock vs. DPLL Automatic Operating Mode	33
Figure 9. T4 Selected Input Clock vs. DPLL Automatic Operating Mode	34
Figure 10. APLL External Filter Components	40
Figure 11. On Target Frame Sync Input Signal Timing	43
Figure 12. 0.5 UI Early Frame Sync Input Signal Timing	43
Figure 13. 0.5 UI Late Frame Sync Input Signal Timing	44
Figure 14. 1 UI Late Frame Sync Input Signal Timing	44
Figure 15. Physical Connection Between Two Devices	45
Figure 16. IDT82V3390 Power Decoupling Scheme	47
Figure 17. Typical Application	48
Figure 18. EPROM Access Timing Diagram	51
Figure 19. Multiplexed Read Timing Diagram	52
Figure 20. Multiplexed Write Timing Diagram	53
Figure 21. Intel Read Timing Diagram	55
Figure 22. Intel Write Timing Diagram	56
Figure 23. Motorola Read Timing Diagram	57
Figure 24. Motorola Write Timing Diagram	58
Figure 25. Serial Read Timing Diagram (CLKE Asserted Low)	59
Figure 26. Serial Read Timing Diagram (CLKE Asserted High)	59
Figure 27. Serial Write Timing Diagram	60
Figure 28. Definition of I2C Bus Timing	61
Figure 29. I2C Slave Interface Supported Transactions	61
Figure 30. JTAG Interface Timing Diagram	63
Figure 31. Assembly for Expose Pad thermal Release Path (Side View)	157
Figure 32. 64 kHz + 8 kHz Signal Structure	159
Figure 33. 64 kHz + 8 kHz + 0.4 kHz Signal Structure	159
Figure 34. 64 kHz + 8 kHz / 64 kHz + 8 kHz + 0.4 kHz Signal Input Level	159
Figure 35. 64 kHz + 8 kHz / 64 kHz + 8 kHz + 0.4 kHz Signal Output Level	159
Figure 36. AMI Input / Output Port Line Termination (Recommended)	160
Figure 37. Recommended PECL Input Port Line Termination	162
Figure 38. Recommended PECL Output Port Line Termination	162
Figure 39. Recommended LVDS Input Port Line Termination	164
Figure 40. Recommended LVDS Output Port Line Termination	164
Figure 41. Example of Single-Ended Signal to Drive Differential Input	165
Figure 42. Output Wander Generation (TDEV)	170
Figure 43. Output Wander Generation (MTIE)	170
Figure 44. Input / Output Clock Timing	171
Figure 45. Output Clock Timing	172
Figure 46. 100-Pin EQG Package Dimensions (a) (in Millimeters)	178
Figure 47. 100-Pin EQG Package Dimensions (b) (in Millimeters)	179
Figure 48. EQG100 Recommended Land Pattern with Exposed Pad (in Millimeters)	180



FEATURES

HIGHLIGHTS

- Single PLL chip:
 - Features 0.5 mHz to 560 Hz bandwidth
 - Provides node clock for ITU-T G.8261/G.8262 Synchronous Ethernet (SyncE)
 - Exceeds GR-253-CORE and ITU-T G.813 jitter generation requirements
 - Provides node clocks for Cellular and WLL base-station (GSM and 3G networks)
 - Provides clocks for DSL access concentrators (DSLAM), especially for Japan TCM-ISDN network timing based ADSL equipments
 - Provides clocks for 1 Gigabit and 10 Gigabit Ethernet applications

MAIN FEATURES

- Provides an integrated single-chip solution for Synchronous Equipment Timing Source, including Stratum 3, Stratum 4E, Stratum 4, SMC, EEC-Option 1 and EEC-Option 2 Clocks
- Provides 156.25 MHz clock for 10 Gig Ethernet Application, with less than 0.7 ps of RMS Phase Jitter (12 kHz - 20 MHz)
- Employs PLL architecture to feature excellent jitter performance and minimize the number of the external components
- Integrates T0 DPLL and T4 DPLL; T4 DPLL locks independently or locks to T0 DPLL
- Supports Forced or Automatic operating mode switch controlled by an internal state machine. It supports Free- Run, Locked and Hold-over modes
- Supports programmable DPLL bandwidth (0.5 mHz to 560 Hz in 19 steps) and damping factor (1.2 to 20 in 5 steps)
- Supports 1.1×10^{-5} ppm absolute holdover accuracy and 4.4×10^{-8} ppm instantaneous holdover accuracy
- Supports hitless reference switching to minimize phase transients on T0 DPLL output to be no more than 0.61 ns
- Supports phase absorption when phase-time changes on T0 selected input clock are greater than a programmable limit over an interval of less than 0.1 seconds
- Supports programmable input-to-output phase offset adjustment
- Limits the phase and frequency offset of the outputs
- Provides OUT1~OUT7 output clock frequencies covering from 2 kHz to 625MHz
 - Includes 125 MHz and 156.25 MHz for CMOS outputs
 - Includes 125 MHz, 156.25 MHz, 312.5 MHz and 625 MHz for differential outputs

- Provides OUT8 for composite clocks and OUT9 for 1.544 MHz/2.048 MHz (BITS/SSU)
- Provides IN1 and IN2 for composite clocks
- Provides IN3~IN14 input clock frequencies covering from 2 kHz to 625 MHz
 - Includes 125 MHz and 156.25 MHz for CMOS inputs
 - Includes 156.25 MHz, 312.5 MHz and 625 MHz for differential inputs
- Supports manual and automatic selected input clock switch
- Supports automatic hitless selected input clock switch on clock failure
- Supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing
- Provides a 2 kHz, 4 kHz or 8 kHz frame sync input signal, and a 2 kHz and an 8 kHz frame sync output signals
- Provides output clocks for BITS, GPS, 3G, GSM, etc.
- Supports AMI, PECL/LVDS and CMOS input/output technologies
- Supports master clock calibration
- Supports Master/Slave application (two chips used together) to enable system protection against single chip failure
- Supports Telcordia GR-1244-CORE, Telcordia GR-253-CORE, ITU-T G.812, ITU-T G.8262, ITU-T G.813 and ITU-T G.783 Recommendations

OTHER FEATURES

- Multiple microprocessor interface modes: EPROM, Multiplexed, Intel, Motorola, I2C and Serial
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 100-pin TQFP package, green package options available

APPLICATIONS

- 1 Gigabit Ethernet and 10 Gigabit Ethernet
- BITS / SSU
- SMC / SEC (SONET / SDH)
- DWDM cross-connect and transmission equipment
- Synchronous Ethernet equipment
- Central Office Timing Source and Distribution
- Core and access IP switches / routers
- Gigabit and terabit IP switches / routers
- IP and ATM core switches and access equipment
- Cellular and WLL base-station node clocks
- Broadband and multi-service access equipment
- Any other telecom equipments that need synchronous equipment system timing

DESCRIPTION

The IDT82V3390 is an integrated, single-chip solution for the Synchronous Equipment Timing Source for Stratum 3, Stratum 4E, Stratum 4, SMC, EEC-Option1, EEC-Option2 clocks in SONET / SDH / Synchronous Ethernet equipment, DWDM and Wireless base station.

The device supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing.

The device consists of T0 and T4 paths. The T0 path is a high quality and highly configurable path to provide system clock for node timing synchronization within a SONET / SDH / Synchronous Ethernet network. The T4 path is simpler and less configurable for equipment synchronization. The T4 path locks independently from the T0 path or locks to the T0 path.

An input clock is automatically or manually selected for T0 and T4 each for DPLL locking. Both the T0 and T4 paths support three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode, the DPLL refers to the master clock. In Locked mode, the DPLL locks to the selected input clock. In Holdover mode, the DPLL resorts to the frequency data acquired in Locked mode. Whatever the operating mode is,

the DPLL gives a stable performance without being affected by operating conditions or silicon process variations.

If the DPLL outputs are processed by T0/T4 APLL, the outputs of the device will be in a better jitter/wander performance.

The device provides programmable DPLL bandwidths: 0.5 mHz to 560 Hz in 19 steps and damping factors: 1.2 to 20 in 5 steps. Different settings cover all SONET / SDH clock synchronization requirements.

A high stable input is required for the master clock in different applications. The master clock is used as a reference clock for all the internal circuits in the device. It can be calibrated within ± 741 ppm.

All the read/write registers are accessed through a microprocessor interface. The device supports six microprocessor interface modes: EPROM, Multiplexed, Intel, Motorola, I2C and Serial.

In general, the device can be used in Master/Slave application. In this application, two devices should be used together to enable system protection against single chip failure. See [Chapter 4 Typical Application](#) for details.

FUNCTIONAL BLOCK DIAGRAM

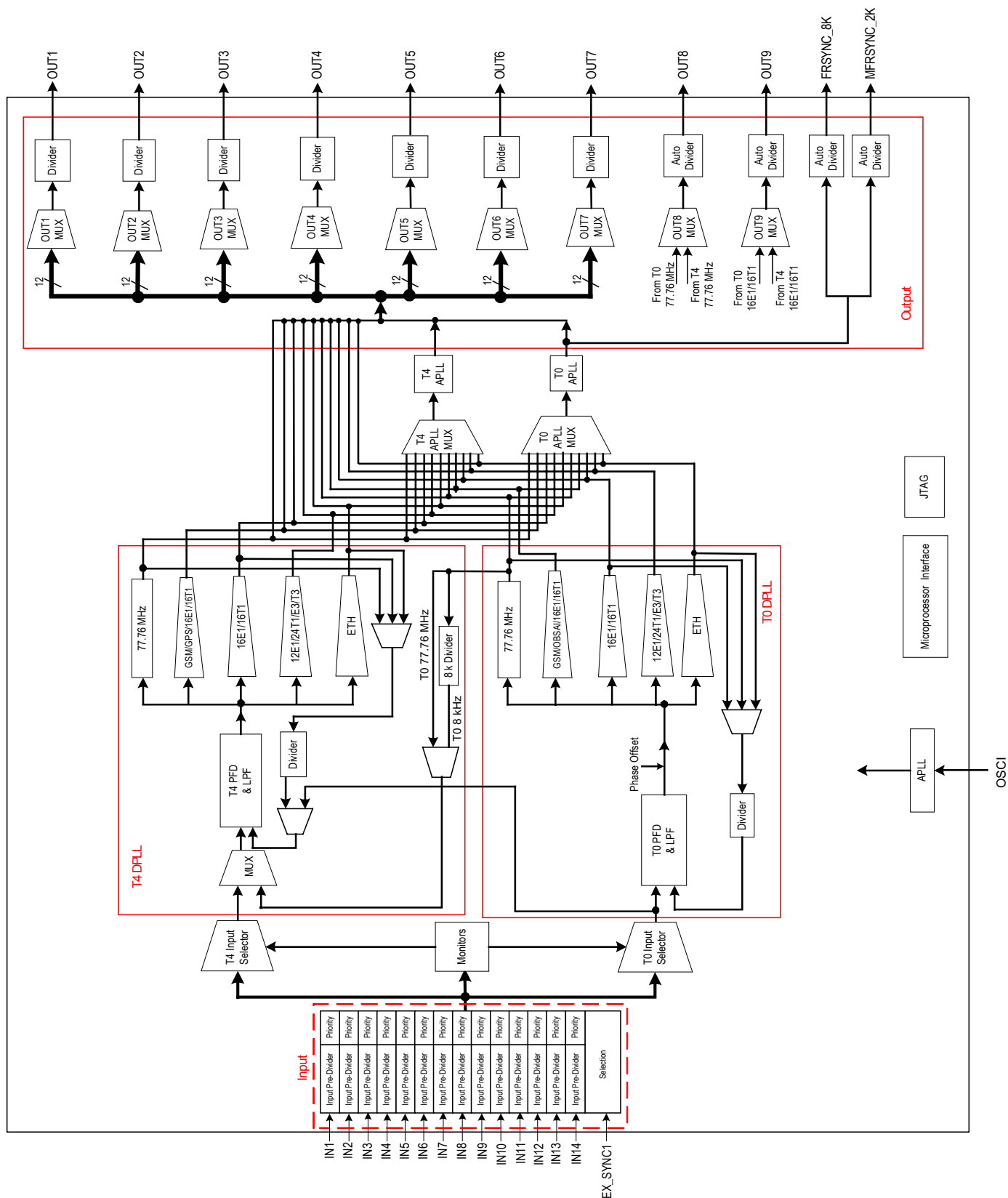


Figure 1. Functional Block Diagram

1 PIN ASSIGNMENT

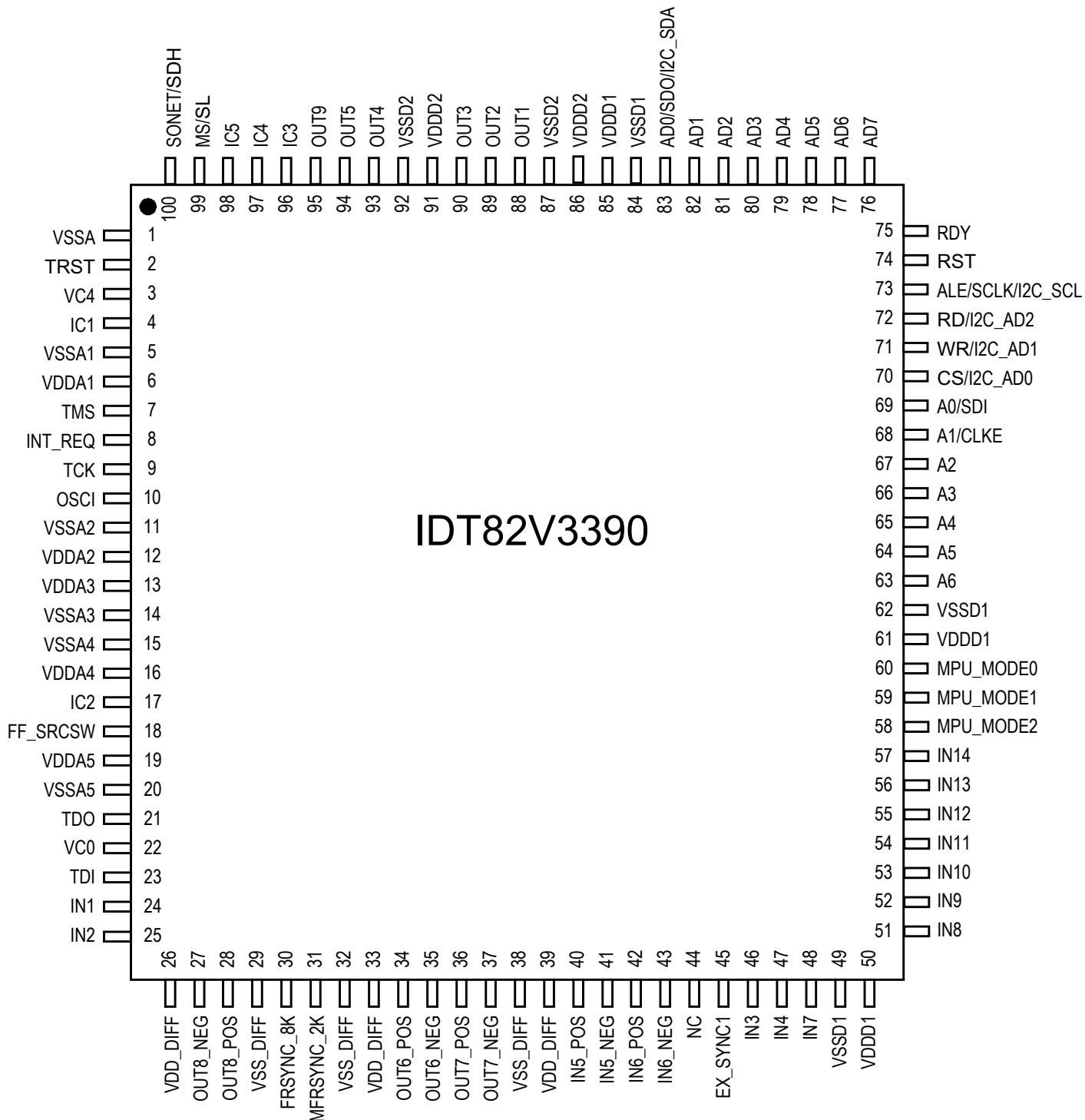


Figure 2. Pin Assignment (Top View)

2 PIN DESCRIPTION

Table 1: Pin Description

Name	Pin No.	I/O	Type	Description ^{1,2}
Global Control Signal				
OSCI	10	I	CMOS	OSCI: Crystal Oscillator Master Clock A nominal 12.8000 MHz clock provided by a crystal oscillator is input on this pin. It is the master clock for the device.
FF_SRCSW	18	I pull-down	CMOS	FF_SRCSW: External Fast Selection Enable During reset, this pin determines the default value of the EXT_SW bit (b4, 0BH) ² . The EXT_SW bit determines whether the External Fast Selection is enabled. High: The default value of the EXT_SW bit (b4, 0BH) is '1' (External Fast selection is enabled); Low: The default value of the EXT_SW bit (b4, 0BH) is '0' (External Fast selection is disabled). After reset, this pin selects an input clock pair for the T0 DPLL if the External Fast selection is enabled: High: Pair IN3 / IN5 is selected. Low: Pair IN4 / IN6 is selected. After reset, the input on this pin takes no effect if the External Fast selection is disabled.
MS/SL	99	I pull-up	CMOS	MS/SL: Master / Slave Selection This pin, together with the MS_SL_CTRL bit (b0, 13H), controls whether the device is configured as the Master or as the Slave. Refer to Chapter 3.14 Master / Slave Configuration for details. The signal level on this pin is reflected by the MASTER_SLAVE bit (b1, 09H).
SONET/SDH	100	I pull-down	CMOS	SONET/SDH: SONET / SDH Frequency Selection During reset, this pin determines the default value of the IN_SONET_SDH bit (b2, 09H): High: The default value of the IN_SONET_SDH bit is '1' (SONET); Low: The default value of the IN_SONET_SDH bit is '0' (SDH). After reset, the value on this pin takes no effect.
RST	74	I pull-up	CMOS	RST: Reset A low pulse of at least 50 μ s on this pin resets the device. After this pin is high, the device will still be held in reset state for 500 ms (typical).
Frame Synchronization Input Signal				
EX_SYNC1	45	I pull-down	CMOS	EX_SYNC1: External Sync Input 1 A 2 kHz, 4 kHz or 8 kHz signal is input on this pin.
Input Clock				
IN1	24	I	AMI	IN1: Input Clock 1 A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is input on this pin.
IN2	25	I	AMI	IN2: Input Clock 2 A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is input on this pin.
IN3	46	I pull-down	CMOS	IN3: Input Clock 3 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.
IN4	47	I pull-down	CMOS	IN4: Input Clock 4 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description ^{1,2}
IN5_POS IN5_NEG	40 41	I	PECL/LVDS	IN5_POS / IN5_NEG: Positive / Negative Input Clock 5 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 156.25 MHz, 311.04 MHz, 312.5 MHz, 622.08 MHz or 625 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected. Single-ended input for differential input is also supported. Refer to Chapter 9.3.3.3 Single-Ended Input for Differential Input .
IN6_POS IN6_NEG	42 43	I	PECL/LVDS	IN6_POS / IN6_NEG: Positive / Negative Input Clock 6 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 156.25 MHz, 311.04 MHz or 312.5 MHz, 622.08 MHz or 625 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected. Single-ended input for differential input is also supported. Refer to Chapter 9.3.3.3 Single-Ended Input for Differential Input .
IN7	48	I pull-down	CMOS	IN7: Input Clock 7 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.
IN8	51	I pull-down	CMOS	IN8: Input Clock 8 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.
IN9	52	I pull-down	CMOS	IN9: Input Clock 9 A 12 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.
IN10	53	I pull-down	CMOS	IN10: Input Clock 10 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.
IN11	54	I pull-down	CMOS	IN11: Input Clock 11 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin. In Slave operation, the frequency of the T0 selected input clock IN11 is recommended to be 6.48 MHz.
IN12	55	I pull-down	CMOS	IN12: Input Clock 12 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.
IN13	56	I pull-down	CMOS	IN13: Input Clock 13 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.
IN14	57	I pull-down	CMOS	IN14: Input Clock 14 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description ^{1, 2}
Output Frame Synchronization Signal				
FRSYNC_8K	30	O	CMOS	FRSYNC_8K: 8 kHz Frame Sync Output An 8 kHz signal is output on this pin.
MFRSYNC_2K	31	O	CMOS	MFRSYNC_2K: 2 kHz Multiframe Sync Output A 2 kHz signal is output on this pin.
Output Clock				
OUT1	88	O	CMOS	OUT1 ~ OUT5: Output Clock 1 ~ 5 A 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 ⁴ , N x T1 ⁵ , N x 13.0 MHz ⁶ , N x 3.84 MHz ⁷ , 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 25MHz, 125 MHz, 155.52 MHz or 156.25 Mhz clock is output on these pins.
OUT2	89			
OUT3	90			
OUT4	93			
OUT5	94			
OUT6_POS	34	O	PECL/LVDS	OUT6_POS / OUT6_NEG: Positive / Negative Output Clock 6 A 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 ⁴ , N x T1 ⁵ , N x 13.0 MHz ⁶ , N x 3.84 MHz ⁷ , 5 MHz, 10 MHz, 20 MHz, 25 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125 MHz, 155.52 MHz, 156.25 MHz, 311.04 MHz, 312.5 MHz, 622.08 MHz or 625 MHz clock is differentially output on this pair of pins.
OUT6_NEG	35			
OUT7_POS	36	O	PECL/LVDS	OUT7_POS / OUT7_NEG: Positive / Negative Output Clock 7 A 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 ⁴ , N x T1 ⁵ , N x 13.0 MHz ⁶ , N x 3.84 MHz ⁷ , 5 MHz, 10 MHz, 20 MHz, 25 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125 MHz, 155.52 MHz, 156.25 MHz, 311.04 MHz, 312.5 MHz 622.08 MHz or 625 MHz clock is differentially output on this pair of pins.
OUT7_NEG	37			
OUT8_POS	28	O	AMI	OUT8_POS / OUT8_NEG: Positive / Negative Output Clock 8 A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is differentially output on this pair of pins.
OUT8_NEG	27			
OUT9	95	O	CMOS	OUT9: Output Clock 9 A 1.544 MHz (SONET) / 2.048 MHz (SDH) BITS/SSU clock is output on this pin.
VC4	3	O	Analog	VC4: T4 APLL VC Output An optional external RC filter can be connected to this pin. If the external RC filter is not implemented then leave this pin unconnected. For 10 Gigabit Ethernet application, it is recommended to use external filter for low bandwidth options.
VC0	22	O	Analog	VC0: T0 APLL VC Output An optional external RC filter can be connected to this pin. If the external RC filter is not implemented then leave this pin unconnected. For 10 Gigabit Ethernet application, it is recommended to use external filter for low bandwidth options.
Microprocessor Interface				
CS / I2C_AD0	70	I/O pull-up	CMOS	CS: Chip Selection In EPROM mode, this pin is an output. In Multiplexed, Intel, Motorola and Serial modes, this pin is an input. A transition from high to low must occur on this pin for each read or write operation and this pin should remain low until the operation is over. I2C_AD0: Device Address Bit 0 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
INT_REQ	8	O	CMOS	INT_REQ: Interrupt Request This pin is used as an interrupt request. The output characteristics are determined by the HZ_EN bit (b1, 0CH) and the INT_POL bit (b0, 0CH).

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description ^{1, 2}
MPU_MODE0 MPU_MODE1 MPU_MODE2	60 59 58	I pull-down	CMOS	<p>MPU_MODE[2:0]: Microprocessor Interface Mode Selection The device supports six microprocessor interface modes: EPROM, Multiplexed, Intel, Motorola, I2C, and Serial. During reset, these pins determine the default value of the MPU_SEL_CNFG[2:0] bits (b2~0, 7FH) as follows: 001 (EPROM mode); 010 (Multiplexed mode); 011 (Intel mode); 100 (Motorola mode); 101 (Serial mode); 110 (I2C mode); 111 (Serial mode).</p> <p>After reset, these pins are general purpose inputs. The microprocessor interface mode is selected by the MPU_SEL_CNFG[2:0] bits (b2~0, 7FH). After reset de-assertion, wait 10μs for the mode to be active. The value of these pins is always reflected by the MPU_PIN_STS[2:0] bits (b2~0, 02H).</p>
A0 / SDI A1 / CLKE A2 A3 A4 A5 A6	69 68 67 66 65 64 63	I/O pull-down	CMOS	<p>A[6:0]: Address Bus In EPROM mode, these pins are outputs. They are the address bus of the EPROM interface. Intel and Motorola modes, these pins are inputs, they are the address bus of the microprocessor interface.</p> <p>SDI: Serial Data Input In Serial mode, this pin is used as the serial data input. Address and data on this pin are serially clocked into the device on the rising edge of SCLK.</p> <p>CLKE: SCLK Active Edge Selection In Serial mode, this pin is an input, it selects the active edge of SCLK to update the SDO: High - The falling edge; Low - The rising edge.</p> <p>In Multiplexed mode, A0/SDI, A1/CLKE and A[6:2] pins should be connected to ground. In Serial mode, A[6:2] pins should be connected to ground. See Table 33 for details.</p>
AD0 / SDO / I2C_SDA AD1 AD2 AD3 AD4 AD5 AD6 AD7	83 82 81 80 79 78 77 76	I/O pull-down	CMOS	<p>AD[7:0]: Address / Data Bus In EPROM, Intel and Motorola modes, these pins are the bi-directional data bus of the microprocessor interface. In Multiplexed mode, these pins are the bi-directional address/data bus of the microprocessor interface.</p> <p>SDO: Serial Data Output In Serial mode, this pin is used as the serial data output. Data on this pin is serially clocked out of the device on the active edge of SCLK. In Serial mode, AD[7:1] pins should be connected to ground.</p> <p>I2C_SDA: Serial Data Input/Output In I2C mode, this pin is used as the input/output for the serial data.</p>

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description ^{1, 2}
WR / I2C_AD1	71	I pull-up	CMOS	<p>WR: Write Operation In Multiplexed and Intel modes, this pin is asserted low to initiate a write operation. In Motorola mode, this pin is asserted low to initiate a write operation or asserted high to initiate a read operation. In EPROM and Serial modes, this pin should be connected to ground.</p> <p>I2C_AD1: Device Address Bit 1 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.</p>
RD / I2C_AD2	72	I pull-up	CMOS	<p>RD: Read Operation In Multiplexed and Intel modes, this pin is asserted low to initiate a read operation. In EPROM, Motorola and Serial modes, this pin should be connected to ground.</p> <p>I2C_AD2: Device Address Bit 2 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.</p>
ALE / SCLK / I2C_SCL	73	I pull-down	CMOS	<p>ALE: Address Latch Enable In Multiplexed mode, the address on AD[7:0] pins is sampled into the device on the falling edge of ALE.</p> <p>SCLK: Shift Clock In Serial mode, a shift clock is input on this pin. Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the active edge of SCLK. The active edge is determined by the CLKE.</p> <p>In EPROM, Intel and Motorola modes, this pin should be connected to ground.</p> <p>I2C_SCL: Serial Clock Line In I2C mode, the serial clock is input on this pin.</p>
RDY	75	O	CMOS	<p>RDY: Ready/Data Acknowledge In Multiplexed and Intel modes, a high level on this pin indicates that a read/write cycle is completed. A low level on this pin indicates that wait state must be inserted. In Motorola mode, a low level on this pin indicates that valid information on the data bus is ready for a read operation or acknowledges the acceptance of the written data during a write operation. In EPROM and Serial modes, this pin should be connected to ground.</p>
JTAG (per IEEE 1149.1)				
TRST	2	I pull-down	CMOS	<p>TRST: JTAG Test Reset (Active Low) A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used.</p>
TMS	7	I pull-up	CMOS	<p>TMS: JTAG Test Mode Select The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.</p>
TCK	9	I pull-down	CMOS	<p>TCK: JTAG Test Clock The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.</p>
TDI	23	I pull-up	CMOS	<p>TDI: JTAG Test Data Input The test data are input on this pin. They are clocked into the device on the rising edge of TCK.</p>
TDO	21	O	CMOS	<p>TDO: JTAG Test Data Output The test data are output on this pin. They are clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning. This pin can indicate the interrupt of T0 selected input clock fail, as determined by the LOS_FLAG_ON_TDO bit (b6, 0BH). Refer to Chapter 3.8.1 Input Clock Validity for details.</p>

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description ^{1,2}
Power & Ground				
VDDD1	50, 61, 85	Power	-	VDDD1: Digital Core Power.
VDDD2	86, 91	Power	-	VDDD2: CMOS CLK Output Power
VDD_DIFF	26, 33, 39	Power	-	VDD_DIFF1: Differential I/O Power Supply
VSSD1	49, 62, 84	Ground	-	VSSD1: Digital Core Ground
VSSD2	87, 92	Ground	-	VSSD2: CMOS CLK Output Ground
VSS_DIFF	32, 38, 29	Ground	-	VSS_DIFF: Differential I/O Ground
VSSA	1	Ground	-	VSSA: Common Ground
VSSA1	5	Ground	-	VSSAn: T4 & T0 APLL Ground
VSSA2	11			
VSSA3	14			
VSSA4	15			
VSSA5	20			
VDDA1	6	Power	-	VDDAn: T4 & T0 APLL Power
VDDA2	12			
VDDA3	13			
VDDA4	16			
VDDA5	19			
Others				
IC1	4	-	-	IC: Internal Connected Internal Use. These pins should be left open for normal operation.
IC2	17			
IC3	96			
IC4	97			
IC5	98			
NC	44	-	-	NC: Not Connected
Note:				
1. All the unused input pins should be connected to ground; the output of all the unused output pins are don't-care.				
2. The contents in the brackets indicate the position of the register bit/bits.				
3. N x 8 kHz: $1 \leq N \leq 19440$.				
4. N x E1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64.				
5. N x T1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96.				
6. N x 13.0 MHz: N = 1, 2, 4.				
7. N x 3.84 MHz: N = 1, 2, 4, 8, 16, 10, 20, 40.				

3 FUNCTIONAL DESCRIPTION

3.1 RESET

The reset operation resets all registers and state machines to their default value or status.

After power on, the device must be reset for normal operation.

For a complete reset, the RST pin must be asserted low for at least 50 μ s. After the RST pin is pulled high, the device will still be in reset state for 500 ms (typical). If the RST pin is held low continuously, the device remains in reset state.

3.2 MASTER CLOCK

A nominal 12.8000 MHz clock, provided by a crystal oscillator, is input on the OSCI pin. This clock is provided for the device as a master clock. The master clock is used as a reference clock for all the internal circuits. A better active edge of the master clock is selected by the OSC_EDGE bit to improve jitter and wander performance.

In fact, an offset from the nominal frequency may be input on the OSCI pin. This offset can be compensated by setting the NOMINAL_FREQ_VALUE[23:0] bits. The calibration range is within ± 741 ppm.

The crystal oscillator should be chosen accordingly to meet GR-1244-CORE, GR-253-CORE, ITU-T G.8262, ITU-T G.812 and ITU-T G.813.

Table 2: Related Bit / Register in Chapter 3.2

Bit	Register	Address (Hex)
NOMINAL_FREQ_VALUE[23:0]	NOMINAL_FREQ[23:16]_CNFG, NOMINAL_FREQ[15:8]_CNFG, NOMINAL_FREQ[7:0]_CNFG	06, 05, 04
OSC_EDGE	DIFFERENTIAL_IN_OUT_OSCI_CNFG	0A

3.3 INPUT CLOCKS & FRAME SYNC SIGNAL

Altogether 14 clocks and 1 frame sync signal are input to the device.

3.3.1 INPUT CLOCKS

The device provides 14 input clock ports.

According to the input port technology, the input ports support the following technologies:

- AMI
- PECL/LVDS
- CMOS

The IDT82V3390 supports Telecom and Ethernet frequencies from 2 kHz up to 625 MHz. It supports 2 kHz, 4 kHz, N x 8 kHz, 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 156.25 MHz, 312.5 MHz and 625 MHz frequencies.

IN1 and IN2 support the AMI input signal only and the clock source is from T3. The input clock is a 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock. The 400HZ_SEL bit should be set to match the input frequency. Any input violation that does not meet the standard composite clock structure will induce an AMI violation. The AMI violation is indicated by the AMI1_VIOL¹ / AMI2_VIOL¹ bit. If the AMI1_VIOL² / AMI2_VIOL² bit is '1', the occurrence of an AMI violation will trigger an interrupt.

IN3, IN4 and IN7 ~ IN14 support CMOS input signal only and the clock sources can be from T1, T2 or T3.

IN5 and IN6 support PECL/LVDS input signal and automatically detect whether the signal is PECL or LVDS. The clock sources can be from T1, T2 or T3.

For SDH and SONET networks, the default frequency is different. SONET / SDH frequency selection is controlled by the IN_SONET_SDH bit. During reset, the default value of the IN_SONET_SDH bit is determined by the SONET/SDH pin: high for SONET and low for SDH. After reset, the input signal on the SONET/SDH pin takes no effect.

IDT82V3390 supports single-ended input for differential input. Refer to [Chapter 9.3.3.3 Single-Ended Input for Differential Input](#).

3.3.2 FRAME SYNC INPUT SIGNALS

A 2 kHz, 4 kHz or 8 kHz frame sync signal is input on the EX_SYNC1 pin. It is a CMOS input. The input frequency should match the setting in the SYNC_FREQ[1:0] bits.

The frame sync input signal is used for frame sync output signal synchronization. Refer to [Chapter 3.13.2 Frame SYNC Output Signals](#) for details.

Table 3: Related Bit / Register in Chapter 3.3

Bit	Register	Address (Hex)
400HZ_SEL	IN1_CNFG	14
	IN2_CNFG	15
AMI1_VIOL ¹	INTERRUPT3_STS	0F
AMI2_VIOL ¹		
AMI1_VIOL ²	INTERRUPTS3_ENABLE_CNFG	12
AMI2_VIOL ²		
IN_SONET_SDH	INPUT_MODE_CNFG	09
SYNC_FREQ[1:0]		

3.4 INPUT CLOCK PRE-DIVIDER

Each input clock is assigned an internal Pre-Divider. The Pre-Divider is used to divide the clock frequency down to the internal DPLL's required input frequency, which is no more than 38.88 MHz.

For IN1 and IN2, the DPLL required frequency is fixed to 8 kHz (i.e., the corresponding IN_FREQ[3:0] bits are '0000'). The 8 kHz clock is extracted from the composite clock and the Pre-Divider is bypassed automatically.

For IN3 ~ IN14, the DPLL required frequency is set by the corresponding IN_FREQ[3:0] bits.

Each Pre-Divider consists of a DivN Divider and a Lock 8k Divider. IN5 and IN6 also include a HF (High Frequency) Divider. Figure 3 shows a block diagram of the pre-dividers for an input clock and Table 4 shows the Pre-Divider Functions.

When the Lock 8k Divider is used, the input clock is divided down to 8 kHz internally; the PRE_DIVN_VALUE [14:0] bits are not required. Lock 8k Divider can be used for 1.544 MHz, 2.048 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz or 38.88 MHz input clock frequency and the corresponding IN_FREQ[3:0] bits should be set to match the input frequency.

For 2 kHz, 4 kHz or 8 kHz input clock frequency only, the Pre-Divider should be bypassed by setting IN5_DIV[1:0] bits / IN6_DIV[1:0] bits = 0, DIRECT_DIV bit = 0, and LOCK_8K bit = 0. The corresponding IN_FREQ[3:0] bits should be set to match the input frequency. The input clock can be inverted, as determined by the IN_2K_4K_8K_INV bit.

The HF Divider, which is only available for IN5 and IN6, should be used when the input clock is higher than (>) 155.52 MHz. The input clock can be divided by 4, 5 or can bypass the HF Divider, as determined by the IN5_DIV[1:0]/IN6_DIV[1:0] bits correspondingly.

Either the DivN Divider or the Lock 8k Divider can be used or both can be bypassed, as determined by the DIRECT_DIV bit and the LOCK_8K bit.

When the DivN Divider is used for INn ($3 \leq n \leq 14$), the division factor setting should observe the following order:

1. Select an input clock by the PRE_DIV_CH_VALUE[3:0] bits;
2. Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits;
3. Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.

Once the division factor is set for the input clock selected by the PRE_DIV_CH_VALUE[3:0] bits, it is valid until a different division factor is set for the same input clock. The division factor is calculated as follows:

$$\text{Division Factor} = (\text{the frequency of the clock input to the DivN Divider} \div \text{the frequency of the DPLL required clock set by the IN_FREQ[3:0] bits}) - 1$$

The DivN Divider can only divide the input clock whose frequency is less than or equal to (\leq) 155.52 MHz.

The Pre-Divider configuration and the division factor setting depend on the input clock on one of the IN3 ~ IN14 pins and the DPLL required clock. Here is an example:

The input clock on the IN6 pin is 622.08 MHz; the DPLL required clock is 6.48 MHz by programming the IN_FREQ[3:0] bits of register IN6 to '0010'. Do the following step by step to divide the input clock:

1. Use the HF Divider to divide the clock down to 155.52 MHz:
 $622.08 \div 155.52 = 4$, so set the IN6_DIV[1:0] bits to '01';
2. Use the DivN Divider to divide the clock down to 6.48 MHz:
 Set the PRE_DIV_CH_VALUE[3:0] bits to '0110';
 Set the DIRECT_DIV bit in Register IN6_CNFG to '1' and the LOCK_8K bit in Register IN6_CNFG to '0';
 $155.52 \div 6.48 = 24$; $24 - 1 = 23$, so set the PRE_DIVN_VALUE[14:0] bits to '10111'.

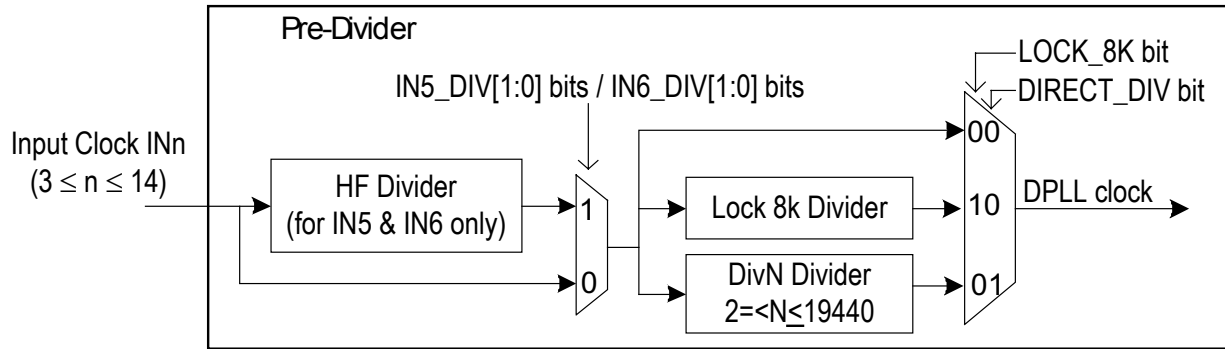


Figure 3. Pre-Divider for An Input Clock

Table 4: Pre-Divider Function

Pre-Divider	Input Clock INn frequency	Control Register	Register/ Address ¹
HF- Divider ²	>155.52 MHz	IN5_DIV[1:0] IN6_DIV[1:0]	IN5_IN6_HF_DIV_CNFG (18)
Divider Bypassed	2 kHz, 4 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz or 38.88 MHz	IN_FREQ[3:0] – set to match input Clock INn frequency. LOCK_8K= 0'b; DIRECT_DIV= 0'b (Bypass Dividers)	IN3_CNFG ~ IN14_CNFG (16 ~ 17, 19 ~ 22)
Lock 8K Divider	1.544 MHz, 2.048 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz or 38.88 MHz	IN_FREQ[3:0] – set to match input Clock INn frequency. LOCK_8K= 1'b; DIRECT_DIV= 0'b (select Lock 8k Divider)	IN3_CNFG ~ IN14_CNFG (16 ~ 17, 19 ~ 22)
DivN	Nx8kHz (2 ≤ N ≤ 19440) Example: 25 MHz = 3125 x 8 kHz	LOCK_8K= 0'b; DIRECT_DIV= 1'b (select DivN Divider) IN_FREQ[3:0] – set to the DPLL required frequency. ('0000': 8 kHz (default)) PRE_DIV_CH_VALUE[3:0] PRE_DIVN_VALUE[14:0] Example: 25 MHz = 3125 x 8kHz Division Factor = 3125 -1= 3124 Dec (or 0C34h) PRE_DIVN_VALUE[7:0]= 34h PRE_DIVN_VALUE[14:8]= 0Ch	IIN3_CNFG ~ IN14_CNFG (16 ~ 17, 19 ~ 22) PRE_DIV_CH_CNFG (23) PRE_DIVN[14:8]_CNFG (25), PRE_DIVN[7:0]_CNFG (24)

Note 1: Please see register description for details.

Note 2: For 156.25 MHz, 312.5 MHz and 625 MHz differential input clock frequency, the divider mode should be DivN with IN_FREQ[3:0] = '1100': 6.25 MHz.

3.5 INPUT CLOCK QUALITY MONITORING

The qualities of all the input clocks are always monitored in the following aspects:

- LOS (loss of signal) (only for IN1 and IN2)
- Activity
- Frequency

LOS monitoring is only conducted on IN1 and IN2. Activity and frequency monitoring are conducted on all the input clocks.

The qualified clocks are available for T0/T4 DPLL selection. The T0 and T4 selected input clocks have to be monitored further. Refer to [Chapter 3.7 Selected Input Clock Monitoring](#) for details.

3.5.1 LOS MONITORING

IN1 and IN2 support the AMI input signal. LOS monitoring is conducted on IN1 and IN2. A LOS event occurs when the amplitude of the input clock falls below +0.6 Vp-p for 1 ms; the LOS event is cleared when the amplitude rises higher than +1 Vp-p.

LOS status is indicated by the AMI1_LOS¹ / AMI2_LOS¹ bit. If the AMI1_LOS² / AMI2_LOS² bit is '1', the occurrence of LOS will trigger an interrupt.

The input clock in LOS status is disqualified for clock selection for T0/T4 DPLL.

3.5.2 ACTIVITY MONITORING

Activity is monitored by using an internal leaky bucket accumulator, as shown in [Figure 4](#).

Each input clock is assigned an internal leaky bucket accumulator. The input clock is monitored for each period of 128 ms and the internal leaky bucket accumulator increases by 1 when an event is detected; it decreases by 1 if no event is detected within the period set by the decay rate. The event is that an input clock drifts outside (>) ±500 ppm with respect to the master clock within a 128 ms period.

There are four configurations (0 - 3) for a leaky bucket accumulator. The leaky bucket configuration for an input clock is selected by the corresponding BUCKET_SEL[1:0] bits. Each leaky bucket configuration consists of four elements: upper threshold, lower threshold, bucket size and decay rate.

The bucket size is the capability of the accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected. The upper threshold is a point above which a no-activity alarm is raised. The lower threshold is a point below which the no-activity alarm is cleared. The decay rate is a certain period during which the accumulator decreases by 1 if no event is detected.

The leaky bucket configuration is programmed by one of four groups of register bits: the BUCKET_SIZE_n_DATA[7:0] bits, the UPPER_THRESHOLD_n_DATA[7:0] bits, the LOWER_THRESHOLD_n_DATA[7:0] bits and the DECAY_RATE_n_DATA[1:0] bits respectively; 'n' is 0 ~ 3.

The no-activity alarm status of the input clock is indicated by the INn_NO_ACTIVITY_ALARM bit (14 ≥ n ≥ 1).

The input clock with a no-activity alarm is disqualified for clock selection for T0/T4 DPLL.

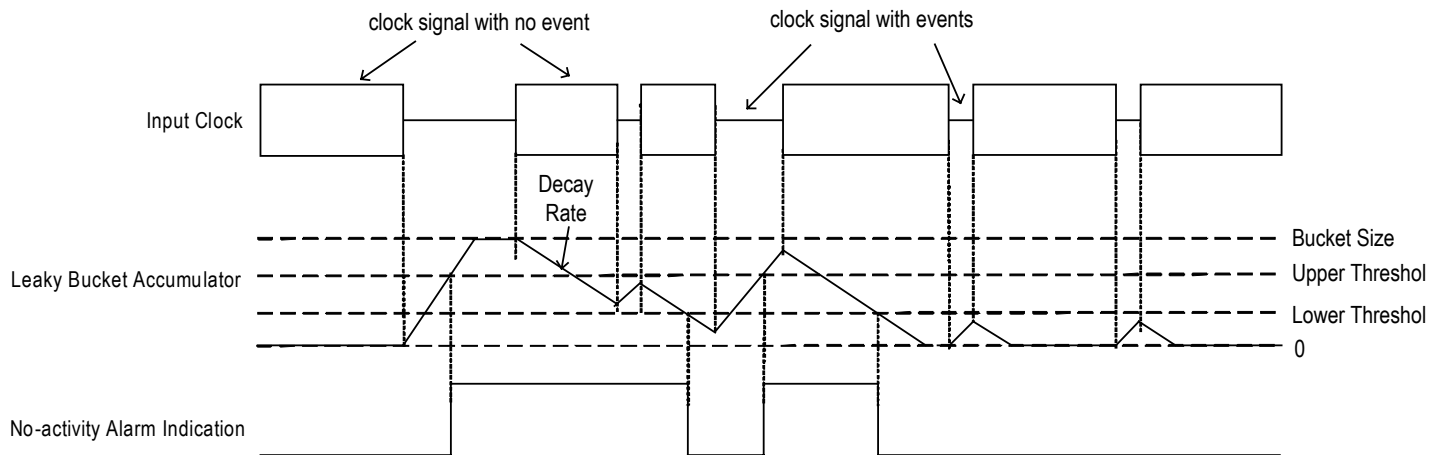


Figure 4. Input Clock Activity Monitoring

3.5.3 FREQUENCY MONITORING

Frequency is monitored by comparing the input clock with a reference clock. The reference clock can be derived from the master clock or the output of T0 DPLL, as determined by the `FREQ_MON_CLK` bit.

Each reference clock has a hard frequency monitor and a soft frequency monitor. Both monitors have two thresholds, rejecting threshold and accepting threshold, which are set in `HARD_FREQ_MON_THRESHOLD[7:0]` and `SOFT_FREQ_MON_THRESHOLD[7:0]`. So four frequency alarm thresholds are set for frequency monitoring: Hard Alarm Accepting Threshold, Hard Alarm Rejecting Threshold, Soft Alarm Accepting Threshold and Soft Alarm Rejecting Threshold.

The frequency hard alarm accepting threshold can be calculated as follows:

$$\text{Frequency Hard Alarm Accepting Threshold (ppm)} = (\text{HARD_FREQ_MON_THRESHOLD}[7:4] + 1) \times \text{FREQ_MON_FACTOR}[3:0] \text{ (b3~0, 2EH)}$$

The frequency hard alarm rejecting threshold can be calculated as follows:

$$\text{Frequency Hard Alarm Rejecting Threshold (ppm)} = (\text{HARD_FREQ_MON_THRESHOLD}[3:0] + 1) \times \text{FREQ_MON_FACTOR}[3:0] \text{ (b3~0, 2EH)}$$

When the input clock frequency rises to above the hard alarm rejecting threshold, the `INn_FREQ_HARD_ALARM` bit ($14 \geq n \geq 1$) will alarm and indicate '1'. The alarm will remain until the frequency is down to below the hard alarm accepting threshold, then the `INn_FREQ_HARD_ALARM` bit will return to '0'. There is a hysteresis

between frequency monitoring, refer to [Figure 5. Hysteresis Frequency Monitoring](#)

The soft alarm is indicated by the `INn_FREQ_SOFT_ALARM` bit ($14 \geq n \geq 1$) in the same way as hard alarm.

If the `FREQ_MON_HARD_EN` bit is '1', the frequency alarm status of the input clock is indicated by the `INn_FREQ_HARD_ALARM` bit ($14 \geq n \geq 1$). When the `FREQ_MON_HARD_EN` bit is '0', no frequency hard alarm is raised even if the input clock is above the frequency alarm threshold.

The input clock with a frequency hard alarm is disqualified for clock selection for T0/T4 DPLL, but the soft alarm doesn't affect the clock selection for T0/T4 DPLL.

In addition, if the input clock is 2 kHz, 4 kHz or 8 kHz, its clock edges with respect to the reference clock are monitored. If any edge drifts outside $\pm 5\%$, the input clock is disqualified for clock selection for T0/T4 DPLL. The input clock is qualified if any edge drifts inside $\pm 5\%$. This function is supported only when the `IN_NOISE_WINDOW` bit is '1'.

The frequency of each input clock with respect to the reference clock can be read by doing the following step by step:

1. Select an input clock by setting the `IN_FREQ_READ_CH[3:0]` bits;
2. Read the value in the `IN_FREQ_VALUE[7:0]` bits and calculate as follows:

$$\text{Input Clock Frequency (ppm)} = \text{IN_FREQ_VALUE}[7:0] \times \text{FREQ_MON_FACTOR}[3:0]$$

Note that the value set by the `FREQ_MON_FACTOR[3:0]` bits depends on the application.

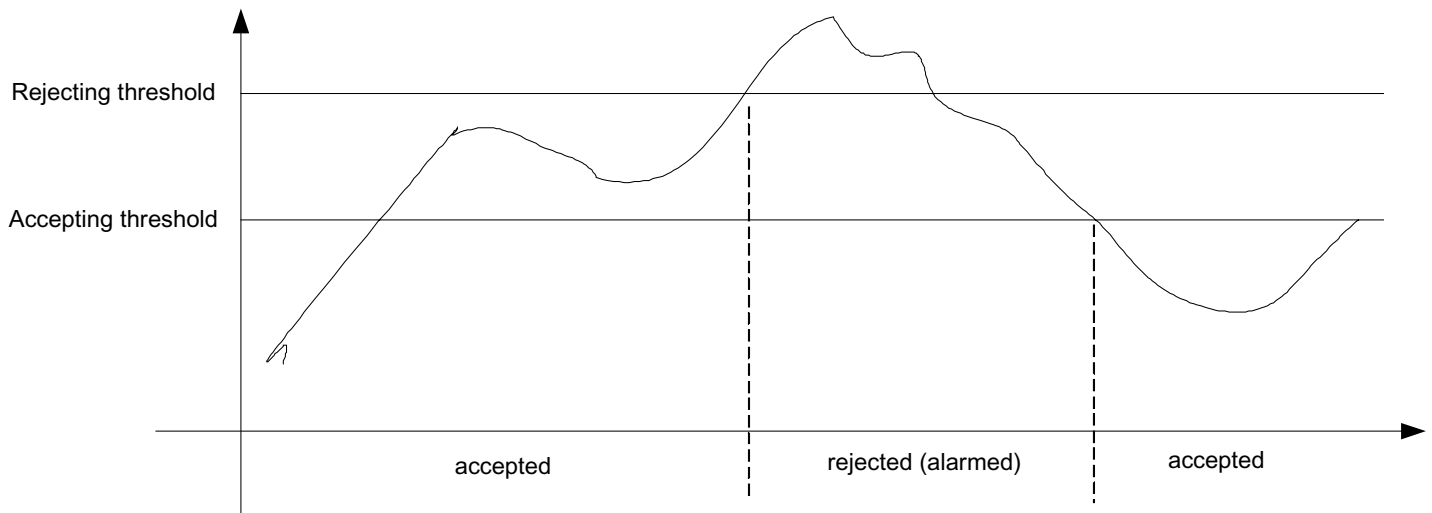


Figure 5. Hysteresis Frequency Monitoring

Table 5: Related Bit / Register in Chapter 3.5

Bit	Register	Address (Hex)
AMI1_LOS ¹	INTERRUPTS3_STS	0F
AMI2_LOS ¹		
AMI1_LOS ²	INTERRUPTS3_ENABLE_CNFG	12
AMI2_LOS ²		
BUCKET_SIZE_n_DATA[7:0] ($3 \geq n \geq 0$)	BUCKET_SIZE_0_CNFG ~ BUCKET_SIZE_3_CNFG	33, 37, 3B, 3F
UPPER_THRESHOLD_n_DATA[7:0] ($3 \geq n \geq 0$)	UPPER_THRESHOLD_0_CNFG ~ UPPER_THRESHOLD_3_CNFG	31, 35, 39, 3D
LOWER_THRESHOLD_n_DATA[7:0] ($3 \geq n \geq 0$)	LOWER_THRESHOLD_0_CNFG ~ LOWER_THRESHOLD_3_CNFG	32, 36, 3A, 3E
DECAY_RATE_n_DATA[1:0] ($3 \geq n \geq 0$)	DECAY_RATE_0_CNFG ~ DECAY_RATE_3_CNFG	34, 38, 3C, 40
BUCKET_SEL[1:0]	IN1_CNFG ~ IN14_CNFG	14 ~ 17, 19 ~ 22
INn_NO_ACTIVITY_ALARM ($14 \geq n \geq 1$)	IN1_IN2_STS ~ IN13_IN14_STS	43 ~ 49
INn_FREQ_HARD_ALARM ($14 \geq n \geq 1$)		
INn_FREQ_SOFT_ALARM ($14 \geq n \geq 1$)		
FREQ_MON_CLK	MON_SW_HS_CNFG	0B
FREQ_MON_HARD_EN		
HARD_FREQ_MON_THRESHOLD[7:0]	HARD_FREQ_MON_THRESHOLD_CNFG	2F
SOFT_FREQ_MON_THRESHOLD[7:0]	SOFT_FREQ_MON_THRESHOLD_CNFG	30
FREQ_MON_FACTOR[3:0]	FREQ_MON_FACTOR_CNFG	2E
IN_NOISE_WINDOW	PHASE_MON_CNFG	78
IN_FREQ_READ_CH[3:0]	IN_FREQ_READ_CH_CNFG	41
IN_FREQ_VALUE[7:0]	IN_FREQ_READ_STS	42

3.6 T0 / T4 DPLL INPUT CLOCK SELECTION

An input clock is selected for T0 DPLL and for T4 DPLL respectively.

For T0 path, the EXT_SW bit and the T0_INPUT_SEL[3:0] bits determine the input clock selection, as shown in [Table 6](#):

Table 6: Input Clock Selection for T0 Path

Control Bits		Input Clock Selection
EXT_SW	T0_INPUT_SEL[3:0]	
1	don't-care	External Fast selection
0	other than 0000	Forced selection
	0000	Automatic selection

For T4 path, the T4 DPLL may lock to a T0 DPLL output or lock independently from T0 path, as determined by the T4_LOCK_T0 bit. When the T4 DPLL locks to the T0 DPLL output, the T4 selected input clock is a 77.76 MHz or 8 kHz signal from the T0 DPLL 77.76 MHz path (refer to [Chapter 3.11.5.1 T0 Path](#)), as determined by the T0_FOR_T4 bit. When the T4 path locks independently from the T0 path, the T4 DPLL input clock selection is determined by the T4_INPUT_SEL[3:0] bits. Refer to [Table 7](#):

Table 7: Input Clock Selection for T4 Path

Control Bits - T4_INPUT_SEL[3:0]	Input Clock Selection
other than 0000	Forced selection
0000	Automatic selection

External Fast selection is done between IN3/IN5 and IN4/IN6 pairs.

Forced selection is done by setting the related registers.

Automatic selection is done based on the results of input clocks quality monitoring and the related registers configuration.

Table 8: External Fast Selection

Control Pin & Bits			the Selected Input Clock
FF_SRC SW (after reset)	IN3_SEL_PRIORITY[3:0]	IN4_SEL_PRIORITY[3:0]	
high	0000	don't-care	IN5
	other than 0000		IN3
low	don't-care	0000	IN6
		other than 0000	IN4

The selected input clock is attempted to be locked in T0/T4 DPLL.

3.6.1 EXTERNAL FAST SELECTION (T0 ONLY)

The External Fast selection is supported by T0 path only. In External Fast selection, only IN3/IN5 and IN4/IN6 pairs are available for selection. Refer to [Figure 6](#). The results of input clocks quality monitoring (refer to [Chapter 3.5 Input Clock Quality Monitoring](#)) do not affect input clock selection.

The T0 input clock selection is determined by the FF_SRC SW pin after reset (this pin determines the default value of the EXT_SW bit during reset, refer to [Chapter 2 Pin Description](#)), the IN3_SEL_PRIORITY[3:0] bits and the IN4_SEL_PRIORITY[3:0] bits, as shown in [Figure 6](#) and [Table 8](#):

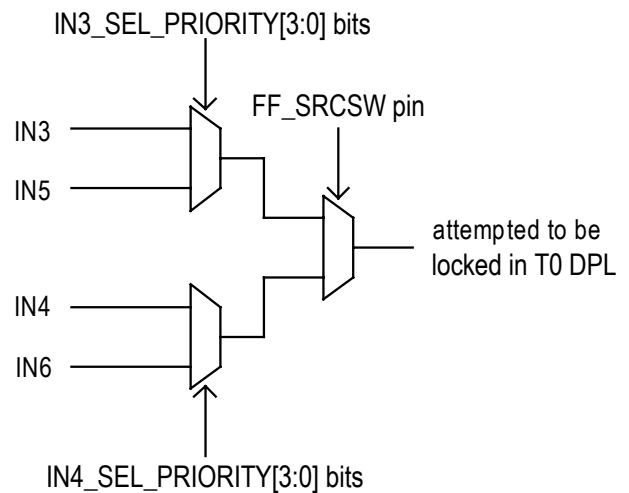


Figure 6. External Fast Selection

3.6.2 FORCED SELECTION

In Forced selection, the selected input clock is set by the T0_INPUT_SEL[3:0] / T4_INPUT_SEL[3:0] bits. The results of input clocks quality monitoring (refer to [Chapter 3.5 Input Clock Quality Monitoring](#)) do not affect the input clock selection.

3.6.3 AUTOMATIC SELECTION

In Automatic selection, the input clock selection is determined by its validity, priority and locking allowance configuration. The validity

depends on the results of input clock quality monitoring (refer to [Chapter 3.5 Input Clock Quality Monitoring](#)). Locking allowance is configured by the corresponding INn_VALID bit ($14 \geq n \geq 1$). Refer to [Figure 7](#). In all the qualified input clocks, the one with the highest priority is selected. The priority is set by the corresponding INn_SEL_PRIORITY[3:0] bits ($14 \geq n \geq 1$). If more than one qualified input clock INn is available and has the same priority, the input clock with the smallest 'n' is selected.

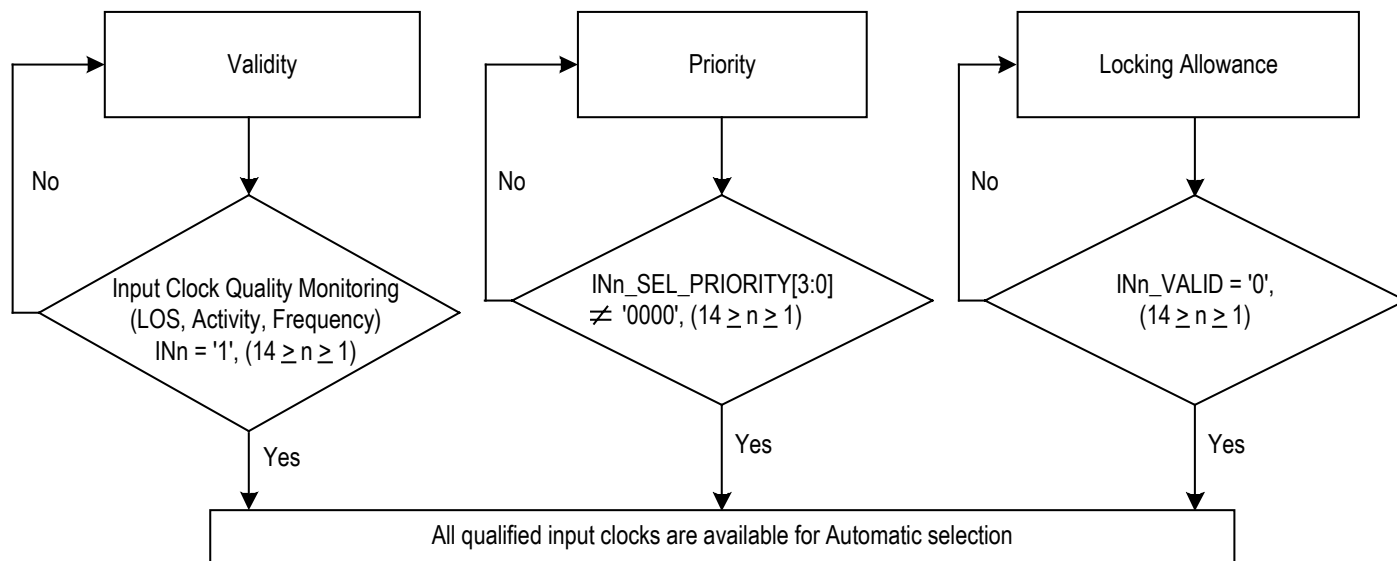


Figure 7. Qualified Input Clocks for Automatic Selection

Table 9: Related Bit / Register in Chapter 3.6

Bit	Register	Address (Hex)
EXT_SW	MON_SW_HS_CNFG	0B
T0_INPUT_SEL[3:0]	T0_INPUT_SEL_CNFG	50
T4_LOCK_T0	T4_INPUT_SEL_CNFG	51
T0_FOR_T4		
T4_INPUT_SEL[3:0]		
INn_SEL_PRIORITY[3:0] ($14 \geq n \geq 1$)	IN1_IN2_SEL_PRIORITY_CNFG ~ IN13_IN14_SEL_PRIORITY_CNFG	26 ~ 2C *
INn_VALID ($14 \geq n \geq 1$)	REMOTE_INPUT_VALID1_CNFG, REMOTE_INPUT_VALID2_CNFG	4C, 4D
INn ($14 \geq n \geq 1$)	INPUT_VALID1_STS, INPUT_VALID2_STS	4A, 4B
T4_T0_SEL	T4_T0_REG_SEL_CNFG	07

Note: * The setting in the 26 ~ 2C registers is either for T0 path or for T4 path, as determined by the T4_T0_SEL bit.

3.7 SELECTED INPUT CLOCK MONITORING

The quality of the selected input clock is always monitored (refer to [Chapter 3.5 Input Clock Quality Monitoring](#)) and the DPLL locking status is always monitored.

3.7.1 T0 / T4 DPLL LOCKING DETECTION

The following events are always monitored:

- Fast Loss;
- Coarse Phase Loss;
- Fine Phase Loss;
- Hard Limit Exceeding.

3.7.1.1 Fast Loss

A fast loss is triggered when the selected input clock misses 2 consecutive clock cycles. It is cleared once an active clock edge is detected.

For T0 path, the occurrence of the fast loss will result in T0 DPLL unlocked if the FAST_LOS_SW bit is '1'. For T4 path, the occurrence of the fast loss will result in T4 DPLL unlocked regardless of the FAST_LOS_SW bit.

3.7.1.2 Coarse Phase Loss

The T0/T4 DPLL compares the selected input clock with the feedback signal. If the phase-compared result exceeds the coarse phase limit, a coarse phase loss is triggered. It is cleared once the phase-compared result is within the coarse phase limit.

When the selected input clock is of 2 kHz, 4 kHz or 8 kHz, the coarse phase limit depends on the MULTI_PH_8K_4K_2K_EN bit, the WIDE_EN bit and the PH_LOS_COARSE_LIMIT[3:0] bits. Refer to [Table 10](#). When the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMIT[3:0] bits. Refer to [Table 11](#).

Table 10: Coarse Phase Limit Programming (the selected input clock of 2 kHz, 4 kHz or 8 kHz)

MULTI_PH_8K_4K_2K_EN	WIDE_EN	Coarse Phase Limit
0	don't-care	±1 UI
1	0	±1 UI
	1	set by the PH_LOS_COARSE_LIMIT[3:0] bits

Table 11: Coarse Phase Limit Programming (the selected input clock of other than 2 kHz, 4 kHz and 8 kHz)

WIDE_EN	Coarse Phase Limit
0	±1 UI
1	set by the PH_LOS_COARSE_LIMIT[3:0] bits

The occurrence of the coarse phase loss will result in T0/T4 DPLL unlocked if the COARSE_PH_LOS_LIMIT_EN bit is '1'.

3.7.1.3 Fine Phase Loss

The T0/T4 DPLL compares the selected input clock with the feedback signal. If the phase-compared result exceeds the fine phase limit programmed by the PH_LOS_FINE_LIMIT[2:0] bits, a fine phase loss is triggered. It is cleared once the phase-compared result is within the fine phase limit.

The occurrence of the fine phase loss will result in T0/T4 DPLL unlocked if the FINE_PH_LOS_LIMIT_EN bit is '1'.

3.7.1.4 Hard Limit Exceeding

Two limits are available for this monitoring. They are DPLL soft limit and DPLL hard limit. When the frequency of the DPLL output with respect to the master clock exceeds the DPLL soft / hard limit, a DPLL soft / hard alarm will be raised; the alarm is cleared once the frequency is within the corresponding limit. The occurrence of the DPLL soft alarm does not affect the T0/T4 DPLL locking status. The DPLL soft alarm is indicated by the corresponding T0_DPLL_SOFT_FREQ_ALARM / T4_DPLL_SOFT_FREQ_ALARM bit. The occurrence of the DPLL hard alarm will result in T0/T4 DPLL unlocked if the FREQ_LIMIT_PH_LOS bit is '1'.

The DPLL soft limit is set by the DPLL_FREQ_SOFT_LIMIT[6:0] bits and can be calculated as follows:

$$DPLL \text{ Soft Limit (ppm)} = DPLL_FREQ_SOFT_LIMIT[6:0] \times 0.724$$

The DPLL hard limit is set by the DPLL_FREQ_HARD_LIMIT[15:0] bits and can be calculated as follows:

$$DPLL \text{ Hard Limit (ppm)} = DPLL_FREQ_HARD_LIMIT[15:0] \times 0.0014$$

3.7.2 LOCKING STATUS

The DPLL locking status depends on the locking monitoring results. The DPLL is in locked state if none of the following events is triggered during 2 seconds; otherwise, the DPLL is unlocked.

- Fast Loss (the FAST_LOS_SW bit is '1');
- Coarse Phase Loss (the COARSE_PH_LOS_LIMIT_EN bit is '1');
- Fine Phase Loss (the FINE_PH_LOS_LIMIT_EN bit is '1');
- DPLL Hard Alarm (the FREQ_LIMIT_PH_LOS bit is '1').

If the FAST_LOS_SW bit, the COARSE_PH_LOS_LIMIT_EN bit, the FINE_PH_LOS_LIMIT_EN bit or the FREQ_LIMIT_PH_LOS bit is '0', the DPLL locking status will not be affected even if the corresponding event is triggered. If all these bits are '0', the DPLL will be in locked state in 2 seconds.

The DPLL locking status is indicated by the T0_DPLL_LOCK / T4_DPLL_LOCK bit.

The T4_STS¹ bit will be set when the locking status of the T4 DPLL changes (from 'lock' to 'unlock' or from 'unlock' to 'lock'). If the T4_STS² bit is '1', an interrupt will be generated.

3.7.3 PHASE LOCK ALARM (T0 ONLY)

A phase lock alarm will be raised when the selected input clock can not be locked in T0 DPLL within a certain period. This period can be calculated as follows:

$$Period (sec.) = TIME_OUT_VALUE[5:0] \times MULTI_FACTOR[1:0]$$

The phase lock alarm is indicated by the corresponding INn_PH_LOCK_ALARM bit (14 ≥ n ≥ 1).

The phase lock alarm can be cleared by the following two ways, as selected by the PH_ALARM_TIMEOUT bit:

- Be cleared when a '1' is written to the corresponding INn_PH_LOCK_ALARM bit;
- Be cleared after the period (= TIME_OUT_VALUE[5:0] X MULTI_FACTOR[1:0] in second) which starts from when the alarm is raised.

The selected input clock with a phase lock alarm is disqualified for T0 DPLL locking.

Note that no phase lock alarm is raised if the T4 selected input clock can not be locked.

Table 12: Related Bit / Register in Chapter 3.7

Bit	Register	Address (Hex)
FAST_LOS_SW	PHASE_LOSS_FINE_LIMIT_CNFG	5B *
PH_LOS_FINE_LIMIT[2:0]		
FINE_PH_LOS_LIMIT_EN		
MULTI_PH_8K_4K_2K_EN	PHASE_LOSS_COARSE_LIMIT_CNFG	5A *
WIDE_EN		
PH_LOS_COARSE_LIMIT[3:0]		
COARSE_PH_LOS_LIMIT_EN	OPERATING_STS	52
T0_DPLL_SOFT_FREQ_ALARM		
T4_DPLL_SOFT_FREQ_ALARM		
T0_DPLL_LOCK		
T4_DPLL_LOCK	DPLL_FREQ_SOFT_LIMIT_CNFG	65
DPLL_FREQ_SOFT_LIMIT[6:0]		
FREQ_LIMIT_PH_LOS	DPLL_FREQ_HARD_LIMIT[15:8]_CNFG, DPLL_FREQ_HARD_LIMIT[7:0]_CNFG	67, 66
DPLL_FREQ_HARD_LIMIT[15:0]		
T4_STS ¹	INTERRUPTS3_STS	0F
T4_STS ²	INTERRUPTS3_ENABLE_CNFG	12
TIME_OUT_VALUE[5:0]	PHASE_ALARM_TIME_OUT_CNFG	08
MULTI_FACTOR[1:0]		
INn_PH_LOCK_ALARM (14 ≥ n ≥ 1)	IN1_IN2_STS ~ IN13_IN14_STS	43 ~ 49
PH_ALARM_TIMEOUT	INPUT_MODE_CNFG	09
T4_T0_SEL	T4_T0_REG_SEL_CNFG	07

Note: * The setting in the 5A and 5B registers is either for T0 path or for T4 path, as determined by the T4_T0_SEL bit.

3.8 INPUT CLOCK SELECTION

If the input clock is selected by External Fast selection or by Forced selection, it can be switched by setting the related registers (refer to [Chapter 3.6.1 External Fast Selection \(T0 only\)](#) & [Chapter 3.6.2 Forced Selection](#)) any time. In this case, whether the input clock is qualified for DPLL locking does not affect the clock switch. If the T4 selected input clock is a T0 DPLL output, it can only be switched by setting the T0_FOR_T4 bit.

When the input clock is selected by Automatic selection, the input clock switch depends on its validity, priority and locking allowance configuration. If the current selected input clock is disqualified, a new qualified input clock may be switched to.

3.8.1 INPUT CLOCK VALIDITY

For all the input clocks, the validity depends on the results of input clock quality monitoring (refer to [Chapter 3.5 Input Clock Quality Monitoring](#)). When all of the following conditions are satisfied, the input clock is valid; otherwise, it is invalid.

- No LOS (the AMI1_LOS / AMI2_LOS bit is '0');
- No no-activity alarm (the INn_NO_ACTIVITY_ALARM bit is '0');
- No frequency hard alarm (the INn_FREQ_HARD_ALARM bit is '0');
- If the IN_NOISE_WINDOW bit is '1', all the edges of the input clock of 2 kHz, 4 kHz or 8 kHz drift inside $\pm 5\%$; if the IN_NOISE_WINDOW bit is '0', this condition is ignored.

The validity qualification of the T0 selected input clock is different from that of the T4 selected input clock. The validity qualification of the T4 selected input clock is the same as the above. The T0 selected input clock is valid when all of the above and the following conditions are satisfied; otherwise, it is invalid.

- No phase lock alarm, i.e., the INn_PH_LOCK_ALARM bit is '0';
- If the ULTR_FAST_SW bit is '1', the T0 selected input clock misses less than (<) 2 consecutive clock cycles; if the ULTR_FAST_SW bit is '0', this condition is ignored.

The validities of all the input clocks are indicated by the INn¹ bit ($14 \geq n \geq 1$). When the input clock validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid'), the INn² bit will be set. If the INn³ bit is '1', an interrupt will be generated.

When the T0 selected input clock has failed, i.e., the validity of the T0 selected input clock changes from 'valid' to 'invalid', the T0_MAIN_REF_FAILED¹ bit will be set. If the T0_MAIN_REF_FAILED² bit is '1', an interrupt will be generated. This interrupt can also be indicated by hardware - the TDO pin, as determined by the LOS_FLAG_TO_TDO bit. When the TDO pin is used to indicate this interrupt, it will be set high when this interrupt is generated and will remain high until this interrupt is cleared.

3.8.2 INPUT CLOCK SELECTION

When the device is configured as Automatic input clock selection, T0 input clock switch is different from T4 input clock switch.

For T0 path, Revertive and Non-Revertive switchings are supported, as selected by the REVERTIVE_MODE bit.

For T4 path, only Revertive switching is supported.

GR-1244 defines Revertive and Non-Revertive Reference switching. In Non-Revertive switching, a switch to an alternate reference is maintained even after the original reference has recovered from the failure that caused the switch. In Revertive switching, the clock switches back to the original reference after that reference recovers from the failure, independent of the condition of the alternate reference. In Non-Revertive switching, input clock switch is minimized.

Conditions of the qualified input clocks available for T0 selection are different from that for T4 selection, as shown in [Table 13](#):

Table 13: Conditions of Qualified Input Clocks Available for T0 & T4 Selection

Conditions of Qualified Input Clocks Available for T0 & T4 Selection	
T0	<ul style="list-style-type: none"> • Valid, i.e., the INn¹ bit is '1'; • Priority enabled, i.e., the corresponding INn_SEL_PRIORITY[3:0] bits are not '0000'; • Locking to the input clock is allowed, i.e., the corresponding INn_VALID bit is '0'.
T4	<ul style="list-style-type: none"> • Valid (all the validity conditions listed in Chapter 3.8.1 Input Clock Validity are satisfied); • Priority enabled, i.e., the corresponding INn_SEL_PRIORITY[3:0] bits are not '0000'; • Locking to the input clock is allowed, i.e., the corresponding INn_VALID bit is '0'.

The input clock is disqualified if any of the above conditions is not satisfied.

In summary, the selected input clock can be switched by:

- External Fast selection (supported by T0 path only);
- Forced selection;
- Revertive switching;
- Non-Revertive switching (supported by T0 path only);
- T4 DPLL locked to T0 DPLL output (supported by T4 path only).

3.8.2.1 Revertive Switching

In Revertive switching, the selected input clock is switched when another qualified input clock with a higher priority than the current selected input clock is available.

The selected input clock is switched if any of the following is satisfied:

- the selected input clock is disqualified;
- another qualified input clock with a higher priority than the selected input clock is available.

A qualified input clock with the highest priority is selected by revertive switching. If more than one qualified input clock INn is available and has the same priority, the input clock with the smallest 'n' is selected.

3.8.2.2 Non-Revertive Switching (T0 only)

In Non-Revertive switching, the T0 selected input clock is not switched when another qualified input clock with a higher priority than the current selected input clock is available. In this case, the selected input clock is switched and a qualified input clock with the highest priority is selected only when the T0 selected input clock is disqualified. If more than one qualified input clock is available and has the same priority, the input clock with the smallest 'n' is selected.

3.8.3 SELECTED / QUALIFIED INPUT CLOCKS INDICATION

The selected input clock is indicated by the CURRENTLY_SELECTED_INPUT[3:0] bits. Note if the T4 selected input clock is a T0 DPLL output, it can not be indicated by these bits.

The qualified input clocks with the three highest priorities are indicated by HIGHEST_PRIORITY_VALIDATED[3:0] bits, the SECOND_PRIORITY_VALIDATED[3:0] bits and the THIRD_PRIORITY_VALIDATED[3:0] bits respectively. If more than one input clock INn has the same priority, the input clock with the smallest 'n' is indicated by the HIGHEST_PRIORITY_VALIDATED[3:0] bits.

When the device is configured in Automatic selection and Revertive switching is enabled, the input clock indicated by the CURRENTLY_SELECTED_INPUT[3:0] bits is the same as the one indicated by the HIGHEST_PRIORITY_VALIDATED[3:0] bits.

When all the input clocks for T4 path changes to be unqualified, the INPUT_TO_T4¹ bit will be set. If the INPUT_TO_T4² bit is '1', an interrupt will be generated.

Table 14: Related Bit / Register in Chapter 3.8

Bit	Register	Address (Hex)
T0_FOR_T4	T4_INPUT_SEL_CNFG	51
INn ¹ (14 ≥ n ≥ 1)	INPUT_VALID1_STS, INPUT_VALID2_STS	4A, 4B
INn ² (14 ≥ n ≥ 1)	INTERRUPTS1_STS, INTERRUPTS2_STS	0D, 0E
INn ³ (14 ≥ n ≥ 1)	INTERRUPTS1_ENABLE_CNFG, INTERRUPTS2_ENABLE_CNFG	10, 11
AMI1_LOS	INTERRUPTS3_STS	0F
AMI2_LOS		
INn_NO_ACTIVITY_ALARM (14 ≥ n ≥ 1)	IN1_IN2_STS ~ IN13_IN14_STS	43 ~ 49
INn_FREQ_HARD_ALARM (14 ≥ n ≥ 1)		
INn_PH_LOCK_ALARM (14 ≥ n ≥ 1)		
IN_NOISE_WINDOW	PHASE_MON_CNFG	78
ULTR_FAST_SW	MON_SW_HS_CNFG	0B
LOS_FLAG_TO_TDO		
T0_MAIN_REF_FAILED ¹	INTERRUPTS2_STS	0E
T0_MAIN_REF_FAILED ²	INTERRUPTS2_ENABLE_CNFG	11
INPUT_TO_T4 ¹	INTERRUPTS3_STS	0F
INPUT_TO_T4 ²	INTERRUPTS3_ENABLE_CNFG	12
REVERTIVE_MODE	INPUT_MODE_CNFG	09
INn_SEL_PRIORITY[3:0] (14 ≥ n ≥ 1)	IN1_IN2_SEL_PRIORITY_CNFG ~ IN13_IN14_SEL_PRIORITY_CNFG	26 ~ 2C *
INn_VALID (14 ≥ n ≥ 1)	REMOTE_INPUT_VALID1_CNFG, REMOTE_INPUT_VALID2_CNFG	4C, 4D
CURRENTLY_SELECTED_INPUT[3:0]	PRIORITY_TABLE1_STS	4E *
HIGHEST_PRIORITY_VALIDATED[3:0]		
SECOND_PRIORITY_VALIDATED[3:0]		
THIRD_PRIORITY_VALIDATED[3:0]	PRIORITY_TABLE2_STS	4F *
T4_T0_SEL	T4_T0_REG_SEL_CNFG	07

Note: * The setting in the 26 ~ 2C, 4E and 4F registers is either for T0 path or for T4 path, as determined by the T4_T0_SEL bit.

3.9 SELECTED INPUT CLOCK STATUS VS. DPLL OPERATING MODE

The operating modes supported by T0 DPLL are more complex than the ones supported by T4 DPLL. T0 DPLL supports three primary operating modes: Free-Run, Locked and Holdover, and three secondary, temporary operating modes: Pre-Locked, Pre-Locked2 and Lost-Phase. T4 DPLL supports three operating modes: Free-Run, Locked and Holdover. The operating modes of T0 DPLL and T4 DPLL can be switched automatically or by force, as controlled by the T0_OPERATING_MODE[2:0] / T4_OPERATING_MODE[2:0] bits respectively.

When the operating mode is switched by force, the operating mode switch is under external control and the status of the selected input clock takes no effect to the operating mode selection.

When the operating mode is switched automatically, the internal state machines for T0 and for T4 automatically determine the operating mode respectively.

3.9.1 T0 SELECTED INPUT CLOCK VS. DPLL OPERATING MODE

The T0 DPLL operating mode is controlled by the T0_OPERATING_MODE[2:0] bits, as shown in [Table 15](#):

Table 15: T0 DPLL Operating Mode Control

T0_OPERATING_MODE[2:0]	T0 DPLL Operating Mode
000	Automatic
001	Forced - Free-Run
010	Forced - Holdover
100	Forced - Locked
101	Forced - Pre-Locked2
110	Forced - Pre-Locked
111	Forced - Lost-Phase

When the operating mode is switched automatically, the operation of the internal state machine is shown in [Figure 8](#).

Whether the operating mode is under external control or is switched automatically, the current operating mode is always indicated by the T0_DPLL_OPERATING_MODE[2:0] bits. When the operating mode switches, the T0_OPERATING_MODE¹ bit will be set. If the T0_OPERATING_MODE² bit is '1', an interrupt will be generated.

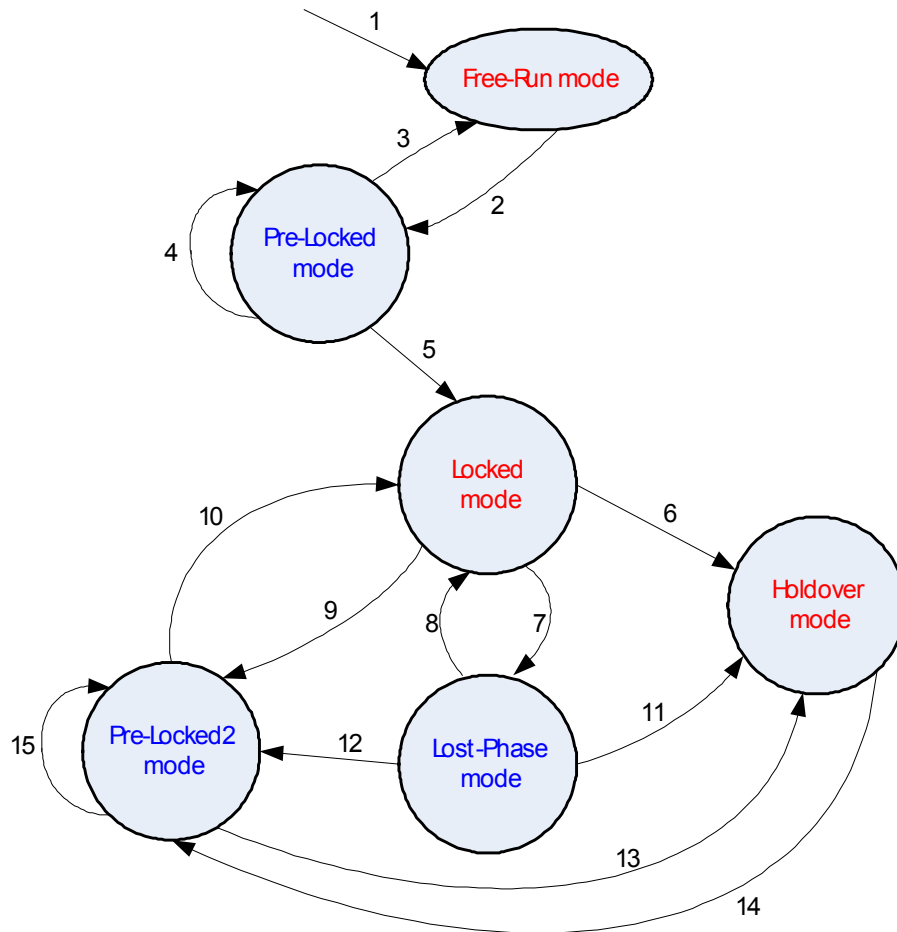


Figure 8. T0 Selected Input Clock vs. DPLL Automatic Operating Mode

Notes to Figure 8:

1. Reset.
2. An input clock is selected.
3. The T0 selected input clock is disqualified **AND** No qualified input clock is available.
4. The T0 selected input clock is switched to another one.
5. The T0 selected input clock is locked (the T0_DPLL_LOCK bit is '1').
6. The T0 selected input clock is disqualified **AND** No qualified input clock is available.
7. The T0 selected input clock is unlocked (the T0_DPLL_LOCK bit is '0').
8. The T0 selected input clock is locked again (the T0_DPLL_LOCK bit is '1').
9. The T0 selected input clock is switched to another one.
10. The T0 selected input clock is locked (the T0_DPLL_LOCK bit is '1').
11. The T0 selected input clock is disqualified **AND** No qualified input clock is available.
12. The T0 selected input clock is switched to another one.
13. The T0 selected input clock is disqualified **AND** No qualified input clock is available.
14. An input clock is selected.
15. The T0 selected input clock is switched to another one.

The causes of Item 4, 9, 12, 15 - 'the T0 selected input clock is switched to another one' - are: (The T0 selected input clock is disqualified **AND** Another input clock is switched to) **OR** (In Revertive switching, a qualified input clock with a higher priority is switched to) **OR** (The T0 selected input clock is switched to another one by External Fast selection or Forced selection).

Refer to Table 13 for details about the input clock qualification for T0 path.

3.9.2 T4 SELECTED INPUT CLOCK VS. DPLL OPERATING MODE

The T4 DPLL operating mode is controlled by the T4_OPERATING_MODE[2:0] bits, as shown in Table 16:

Table 16: T4 DPLL Operating Mode Control

T4_OPERATING_MODE[2:0]	T4 DPLL Operating Mode
000	Automatic
001	Forced - Free-Run
010	Forced - Holdover
100	Forced - Locked

When the operating mode is switched automatically, the operation of the internal state machine is shown in Figure 9:

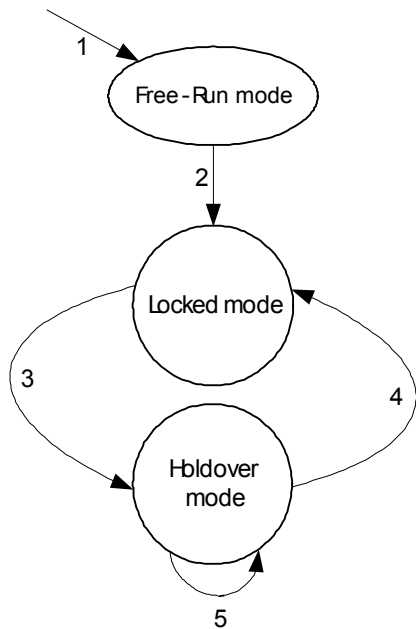


Figure 9. T4 Selected Input Clock vs. DPLL Automatic Operating Mode

Notes to Figure 9:

1. Reset.
2. An input clock is selected.
3. (The T4 selected input clock is disqualified) **OR** (A qualified input clock with a higher priority is switched to) **OR** (The T4 selected input clock is switched to another one by Forced selection) **OR** (When T4 DPLL locks to the T0 DPLL output, the T4 selected input clock is switched by setting the T0_FOR_T4 bit).
4. An input clock is selected.
5. No input clock is selected.

Refer to Table 13 for details about the input clock qualification for T4 path.

Table 17: Related Bit / Register in Chapter 3.9

Bit	Register	Address (Hex)
T0_OPERATING_MODE[2:0]	T0_OPERATING_MODE_CNFG	53
T4_OPERATING_MODE[2:0]	T4_OPERATING_MODE_CNFG	54
T0_DPLL_OPERATING_MODE[2:0]	OPERATING_STS	52
T0_DPLL_LOCK		
T0_OPERATING_MODE ¹	INTERRUPTS2_STS	0E
T0_OPERATING_MODE ²	INTERRUPTS2_ENABLE_CNFG	11
T0_FOR_T4	T4_INPUT_SEL_CNFG	51

3.10 T0 / T4 DPLL OPERATING MODE

The T0/T4 DPLL gives a stable performance in different applications without being affected by operating conditions or silicon process variations. It integrates a PFD (Phase & Frequency Detector), a LPF (Low Pass Filter) and a DCO (Digital Controlled Oscillator), which forms a closed loop. If no input clock is selected, the loop is not closed, and the PFD and LPF do not function.

The PFD detects the phase error, including the fast loss, coarse phase loss and fine phase loss (refer to [Chapter 3.7.1.1 Fast Loss](#) to [Chapter 3.7.1.3 Fine Phase Loss](#)). The averaged phase error of the T0/T4 DPLL feedback with respect to the selected input clock is indicated by the CURRENT_PH_DATA[15:0] bits. It can be calculated as follows:

$$\text{Averaged Phase Error (ns)} = \text{CURRENT_PH_DATA}[15:0] \times 0.61$$

The LPF filters jitter. Its 3 dB bandwidth and damping factor are programmable. A range of bandwidths and damping factors can be set to meet different application requirements. For the same bandwidth setting, a lower damping factor will decrease the locking time but will increase overshoot.

The DCO controls the DPLL output. The frequency of the DPLL output is always multiplied on the basis of the master clock. The phase and frequency offset of the DPLL output may be locked to those of the selected input clock. The current frequency offset with respect to the master clock is indicated by the CURRENT_DPLL_FREQ[23:0] bits, and can be calculated as follows:

$$\text{Current Frequency Offset (ppm)} = \text{CURRENT_DPLL_FREQ}[23:0] \times 0.000011$$

3.10.1 T0 DPLL OPERATING MODE

The T0 DPLL loop is closed except in Free-Run mode and Holdover mode.

For a closed loop, different bandwidths and damping factors can be used depending on DPLL locking stages: starting, acquisition and locked.

In the first two seconds when the T0 DPLL attempts to lock to the selected input clock, the starting bandwidth and damping factor are used. They are set by the T0_DPLL_START_BW[4:0] bits and the T0_DPLL_START_DAMPING[2:0] bits respectively.

During the acquisition, the acquisition bandwidth and damping factor are used. They are set by the T0_DPLL_ACQ_BW[4:0] bits and the T0_DPLL_ACQ_DAMPING[2:0] bits respectively.

When the T0 selected input clock is locked, the locked bandwidth and damping factor are used. They are set by the T0_DPLL_LOCKED_BW[4:0] bits and the T0_DPLL_LOCKED_DAMPING[2:0] bits respectively.

The corresponding bandwidth and damping factor are used when the T0 DPLL operates in different DPLL locking stages: starting, acquisition and locked, as controlled by the device automatically.

Only the locked bandwidth and damping factor can be used regardless of the T0 DPLL locking stage, as controlled by the AUTO_BW_SEL bit.

3.10.1.1 Free-Run Mode

In Free-Run mode, the T0 DPLL output refers to the master clock and is not affected by any input clock. The accuracy of the T0 DPLL output is equal to that of the master clock.

3.10.1.2 Pre-Locked Mode

In Pre-Locked mode, the T0 DPLL output attempts to track the selected input clock.

The Pre-Locked mode is a secondary, temporary mode.

3.10.1.3 Locked Mode

In Locked mode, the T0 selected input clock is locked. The phase and frequency offset of the T0 DPLL output track those of the T0 selected input clock.

In this mode, if the T0 selected input clock is in fast loss status and the FAST_LOS_SW bit is '1', the T0 DPLL is unlocked (refer to [Chapter 3.7.1.1 Fast Loss](#)) and will enter Lost-Phase mode when the operating mode is switched automatically; if the T0 selected input clock is in fast loss status and the FAST_LOS_SW bit is '0', the T0 DPLL locking status is not affected and the T0 DPLL will enter Temp-Holdover mode automatically.

3.10.1.3.1 Temp-Holdover Mode

The T0 DPLL will automatically enter Temp-Holdover mode with a selected input clock switch or no qualified input clock available when the operating mode switch is under external control.

In Temp-Holdover mode, the T0 DPLL has temporarily lost the selected input clock. The T0 DPLL operation in Temp-Holdover mode and that in Holdover mode are alike (refer to [Chapter 3.10.1.5 Holdover Mode](#)) except the frequency offset acquiring methods. See [Chapter 3.10.1.5 Holdover Mode](#) for details about the methods. The method is selected by the TEMP_HOLDOVER_MODE[1:0] bits, as shown in [Table 18](#):

Table 18: Frequency Offset Control in Temp-Holdover Mode

TEMP_HOLDOVER_MODE[1:0]	Frequency Offset Acquiring Method
00	the same as that used in Holdover mode
01	Automatic Instantaneous
10	Automatic Fast Averaged
11	Automatic Slow Averaged

The device automatically controls the T0 DPLL to exit from Temp-Holdover mode.

3.10.1.4 Lost-Phase Mode

In Lost-Phase mode, the T0 DPLL output attempts to track the selected input clock.

The Lost-Phase mode is a secondary, temporary mode.

3.10.1.5 Holdover Mode

In Holdover mode, the T0 DPLL resorts to the stored frequency data acquired in Locked mode to control its output. The T0 DPLL output is not phase locked to any input clock. The frequency offset acquiring method

is selected by the MAN_HOLD OVER bit, the AUTO_AVG bit and the FAST_AVG bit, as shown in [Table 19](#):

Table 19: Frequency Offset Control in Holdover Mode

MAN_HOLD OVER	AUTO_AVG	FAST_AVG	Frequency Offset Acquiring Method
0	0	don't-care	Automatic Instantaneous
	1	0	Automatic Slow Averaged
		1	Automatic Fast Averaged
1	don't-care		Manual

3.10.1.5.1 Automatic Instantaneous

By this method, the T0 DPLL freezes at the operating frequency when it enters Holdover mode. The accuracy is 4.4×10^{-8} ppm.

3.10.1.5.2 Automatic Slow Averaged

By this method, an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3 dB attenuation point corresponding to a period of 110 minutes. The accuracy is 1.1×10^{-5} ppm.

3.10.1.5.3 Automatic Fast Averaged

By this method, an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3 dB attenuation point corresponding to a period of 8 minutes. The accuracy is 1.1×10^{-5} ppm.

3.10.1.5.4 Manual

By this method, the frequency offset is set by the T0_HOLD OVER_FREQ[23:0] bits. The accuracy is 1.1×10^{-5} ppm.

The frequency offset of the T0 DPLL output is indicated by the CURRENT_DPLL_FREQ[23:0] bits.

The device provides a reference for the value to be written to the T0_HOLD OVER_FREQ[23:0] bits. The value to be written can refer to the value read from the CURRENT_DPLL_FREQ[23:0] bits or the T0_HOLD OVER_FREQ[23:0] bits (refer to [Chapter 3.10.1.5.5 Holdover Frequency Offset Read](#)); or then be processed by external software filtering.

3.10.1.5.5 Holdover Frequency Offset Read

The offset value, which is acquired by Automatic Slow Averaged, Automatic Fast Averaged and is set by related register bits, can be read from the T0_HOLD OVER_FREQ[23:0] bits by setting the READ_AVG bit and the FAST_AVG bit, as shown in [Table 20](#).

Table 20: Holdover Frequency Offset Read

READ_AVG	FAST_AVG	Offset Value Read from T0_HOLD OVER_FREQ[23:0]
0	don't-care	The value is equal to the one written to.
1	0	The value is acquired by Automatic Slow Averaged method, not equal to the one written to.
	1	The value is acquired by Automatic Fast Averaged method, not equal to the one written to.

The frequency offset in ppm is calculated as follows:

$$\text{Holdover Frequency Offset (ppm)} = T0_HOLD OVER_FREQ[23:0] \times 0.000011$$

3.10.1.6 Pre-Locked2 Mode

In Pre-Locked2 mode, the T0 DPLL output attempts to track the selected input clock.

The Pre-Locked2 mode is a secondary, temporary mode.

3.10.2 T4 DPLL OPERATING MODE

The T4 path is simpler compared with the T0 path.

3.10.2.1 Free-Run Mode

In Free-Run mode, the T4 DPLL output refers to the master clock and is affected by any input clock. The accuracy of the T4 DPLL output is equal to that of the master clock.

3.10.2.2 Locked Mode

In Locked mode, the T4 selected input clock may be locked in the T4 DPLL.

When the T4 selected input clock is locked, the phase and frequency offset of the T4 DPLL output track those of the T4 selected input clock; when unlocked, the phase and frequency offset of the T4 DPLL output attempt to track those of the selected input clock.

The T4 DPLL loop is closed in Locked mode. Its bandwidth and damping factor are set by the T4_DPLL_LOCKED_BW[1:0] bits and the T4_DPLL_LOCKED_DAMPING[2:0] bits respectively.

3.10.2.3 Holdover Mode

In Holdover mode, the T4 DPLL resorts to the stored frequency data acquired in Locked mode to control its output. The T4 DPLL output is not phase locked to any input clock. The T4 DPLL freezes at the operating frequency when it enters Holdover mode. The accuracy is 4.4×10^{-8} ppm.

Table 21: Related Bit / Register in Chapter 3.10

Bit	Register	Address (Hex)
CURRENT_PH_DATA[15:0]	CURRENT_DPLL_PHASE[15:8]_STS, CURRENT_DPLL_PHASE[7:0]_STS	69 *, 68 *
CURRENT_DPLL_FREQ[23:0]	CURRENT_DPLL_FREQ[23:16]_STS, CURRENT_DPLL_FREQ[15:8]_STS, CURRENT_DPLL_FREQ[7:0]_STS	64 *, 63 *, 62 *
T0_DPLL_START_BW[4:0]	T0_DPLL_START_BW_DAMPING_CNFG	56
T0_DPLL_START_DAMPING[2:0]		
T0_DPLL_ACQ_BW[4:0]	T0_DPLL_ACQ_BW_DAMPING_CNFG	57
T0_DPLL_ACQ_DAMPING[2:0]		
T0_DPLL_LOCKED_BW[4:0]	T0_DPLL_LOCKED_BW_DAMPING_CNFG	58
T0_DPLL_LOCKED_DAMPING[2:0]		
AUTO_BW_SEL	T0_BW_OVERSHOOT_CNFG	59
FAST_LOS_SW	PHASE_LOSS_FINE_LIMIT_CNFG	5B *
TEMP_HOLDOVER_MODE[1:0]	T0_HOLDOVER_MODE_CNFG	5C
MAN_HOLDOVER		
AUTO_AVG		
FAST_AVG		
READ_AVG		
T0_HOLDOVER_FREQ[23:0]	T0_HOLDOVER_FREQ[23:16]_CNFG, T0_HOLDOVER_FREQ[15:8]_CNFG, T0_HOLDOVER_FREQ[7:0]_CNFG	5F, 5E, 5D
T4_DPLL_LOCKED_BW[1:0]	T4_DPLL_LOCKED_BW_DAMPING_CNFG	61
T4_DPLL_LOCKED_DAMPING[2:0]		
T4_T0_SEL	T4_T0_REG_SEL_CNFG	07

Note: * The setting in the 5B, 62 ~ 64, 68 and 69 registers is either for T0 path or for T4 path, as determined by the T4_T0_SEL bit.

3.11 T0 / T4 DPLL OUTPUT

The DPLL output is locked to the selected input clock. According to the phase-compared result of the feedback and the selected input clock, and the DPLL output frequency offset, the PFD output is limited and the DPLL output is frequency offset limited.

3.11.1 PFD OUTPUT LIMIT

The PFD output is limited to be within ± 1 UI or within the coarse phase limit (refer to [Chapter 3.7.1.2 Coarse Phase Loss](#)), as determined by the MULTI_PH_APP bit.

3.11.2 FREQUENCY OFFSET LIMIT

The DPLL output is limited to be within the DPLL hard limit (refer to [Chapter 3.7.1.4 Hard Limit Exceeding](#)).

For T0 DPLL, the integral path value can be frozen when the DPLL hard limit is reached. This function, enabled by the T0_LIMT bit, will minimize the subsequent overshoot when T0 DPLL is pulling in.

3.11.3 HITLESS REFERENCE SWITCHING (T0 ONLY)

The hitless switching (HS) function is only supported by the T0 path.

When a switch event is triggered, the phase offset of the selected input clock with respect to the T0 DPLL output is measured. The device then automatically accounts for the measured phase offset and compensates an appropriate phase offset into the DPLL output so that the phase transients on the T0 DPLL output are minimized.

A switch event is triggered if any one of the following conditions occurs:

- T0 selected input clock switches (the HS_EN bit is '1');
- T0 DPLL exits from Holdover mode or Free-Run mode (the HS_EN bit is '1')

For the above two conditions, the phase transients on the T0 DPLL output are minimized to be no more than 0.61 ns with hitless switch function enabled. The hitless switch can also be frozen at the current phase offset by setting the HS_FREZ bit. When the hitless switch is frozen, the device will ignore any further switch events triggered by the above two conditions, and maintain the current phase offset. When the hitless switch function is disabled, there may be a phase shift on the T0 DPLL output and the T0 DPLL output tracks back to 0 degree phase offset with respect to the T0 selected input clock.

3.11.4 PHASE OFFSET SELECTION (T0 ONLY)

The phase offset of the T0 selected input clock with respect to the T0 DPLL output can be adjusted. If the device is configured as the Master, the PH_OFFSET_EN bit determines whether the input-to-output phase offset is enabled; if the device is configured as the Slave, the input-to-output phase offset is always enabled. If enabled, the input-to-output phase offset can be adjusted by setting the PH_OFFSET[9:0] bits.

The input-to-output phase offset can be calculated as follows:

$$\text{Phase Offset (ns)} = \text{PH_OFFSET}[9:0] \times 0.61$$

3.11.5 FIVE PATHS OF T0 / T4 DPLL OUTPUTS

The T0 DPLL output and the T4 DPLL output are phase aligned with the T0 selected input clock and the T4 selected input clock respectively every 125 μ s period. Each DPLL has five output paths.

3.11.5.1 T0 Path

The five paths for T0 DPLL output are as follows:

- 77.76 MHz path - outputs a 77.76 MHz clock;
- 16E1/16T1 path - outputs a 16E1 or 16T1 clock, as selected by the IN_SONET_SDH bit;
- GSM/OBSAI/16E1/16T1 path - outputs a GSM, OBSAI, 16E1 or 16T1 clock, as selected by the T0_GSM_OBSAI_16E1_16T1_SEL[1:0] bits;
- 12E1/24T1/E3/T3 path - outputs a 12E1, 24T1, E3 or T3 clock, as selected by the T0_12E1_24T1_E3_T3_SEL[1:0] bits;
- 25 MHz path - outputs a 25 MHz clock.

T0 selected input clock is compared with a T0 DPLL output for DPLL locking. The output can only be derived from the 77.76 MHz path or the 16E1/16T1 path. The output path is automatically selected and the output is automatically divided to get the same frequency as the T0 selected input clock.

The T0 DPLL 77.76 MHz output or an 8 kHz signal derived from it can be provided for the T4 DPLL input clock selection (refer to [Chapter 3.6 T0 / T4 DPLL Input Clock Selection](#)).

T0 DPLL outputs are provided for T0/T4 APLL or device output process.

3.11.5.2 T4 Path

The five paths for T4 DPLL output are as follows:

- 77.76 MHz path - outputs a 77.76 MHz clock;
- 16E1/16T1 path - outputs a 16E1 or 16T1 clock, as selected by the IN_SONET_SDH bit;
- GSM/GPS/16E1/16T1 path - outputs an GSM, GPS, 16E1 or 16T1 clock, as selected by the T4_GSM_GPS_16E1_16T1_SEL[1:0] bits;
- 12E1/24T1/E3/T3 path - outputs a 12E1, 24T1, E3 or T3 clock, as selected by the T4_12E1_24T1_E3_T3_SEL[1:0] bits;
- 25 MHz path - outputs a 25 MHz clock.

T4 selected input clock is compared with a T4 DPLL output for DPLL locking. The output can be derived from the 77.76 MHz path or the 16E1/16T1 path. In this case, the output path is automatically selected and the output is automatically divided to get the same frequency as the T4 selected input clock.

In addition, T4 selected input clock is compared with the T0 selected input clock to get the phase difference between T0 and T4 selected input clocks, as determined by the T4_TEST_T0_PH bit.

T4 DPLL outputs are provided for T0/T4 APLL or device output process.

Table 22: Related Bit / Register in Chapter 3.11

Bit	Register	Address (Hex)
MULTI_PH_APP	PHASE_LOSS_COARSE_LIMIT_CNFG	5A *
T0_LIMIT	T0_BW_OVERSHOOT_CNFG	59
HS_EN	MON_SW_HS_CNFG	0B
HS_FREZ		
PH_OFFSET_EN	PHASE_OFFSET[9:8]_CNFG	7B
PH_OFFSET[9:0]	PHASE_OFFSET[9:8]_CNFG, PHASE_OFFSET[7:0]_CNFG	7B, 7A
IN_SONET_SDH	INPUT_MODE_CNFG	09
T0_GSM_OBSAI_16E1_16T1_SEL[1:0]	T0_DPLL_APLL_PATH_CNFG	55
T0_12E1_24T1_E3_T3_SEL[1:0]		
T4_GSM_GPS_16E1_16T1_SEL[1:0]	T4_DPLL_APLL_PATH_CNFG	60
T4_12E1_24T1_E3_T3_SEL[1:0]		
T4_TEST_T0_PH	T4_INPUT_SEL_CNFG	51
T4_T0_SEL	T4_T0_REG_SEL_CNFG	07

Note: * The setting in the 5A register is either for T0 path or for T4 path, as determined by the T4_T0_SEL bit.

3.12 T0 / T4 APLL

A T0 APLL and a T4 APLL are provided for a better jitter and wander performance of the device output clocks.

The bandwidths of the T0/T4 APLL are set by the T0_APLL_BW[1:0] / T4_APLL_BW[1:0] bits respectively. The lower the bandwidth is, the better the jitter and wander performance of the T0/T4 APLL output are.

The input of the T0/T4 APLL can be derived from one of the T0 and T4 DPLL outputs, as selected by the T0_APLL_PATH[3:0] / T4_APLL_PATH[3:0] bits respectively.

Both the APLL and DPLL outputs are provided for selection for the device output.

Table 23: Related Bit / Register in Chapter 3.12

Bit	Register	Address (Hex)
T0_APLL_BW[1:0]	T0_T4_APLL_BW_CNFG	6A
T4_APLL_BW[1:0]		
T0_APLL_PATH[3:0]	T0_DPLL_APLL_PATH_CNFG	55
T4_APLL_PATH[3:0]	T4_DPLL_APLL_PATH_CNFG	60

3.12.1 OPTIONAL EXTERNAL FILTER

If the desire loop bandwidth of T0 APLL and T4 APLL is below 100 kHz for better noise suppressing, it is recommended to use external filter component. The filter components are connected to VC0 for T0 APLL and VC4 for T4 APLL. For internal filter option with loop bandwidth higher or equal to 100 kHz, VC0 and VC4 pins are left floating.

Choosing the correct external components and having a printed circuit board (PCB) layout is a key task for quality operation of the T0 APLL

and T4 APLL external filter option. The T0 APLL and T4 APLL loop bandwidth selection table shows Rs, Cs and Cp values for recommend bandwidth less than 100kHz. The device has been characterized using these parameters. The external loop filter components should be kept as close as possible to the device. Loop filter traces should be kept short. Other signal traces should be kept separated and not run underneath the device and loop filter components.

Table 24: T0 / T4 APLL Approximate Loop Bandwidth Selection

Bandwidth	VC filter pin	Rs (Ω)	Cs (μ F)	Cp (nF)
< 100 kHz	External component	182	2	2
\geq 100 kHz	No Connect	Please refer to Register 6A for detail for internal filter		

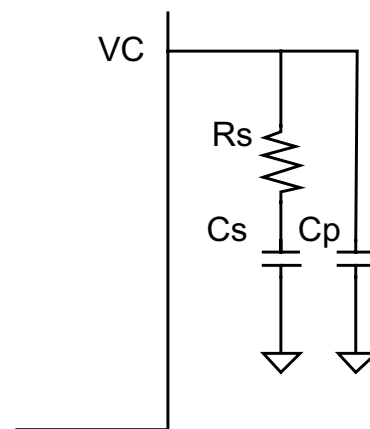


Figure 10. APLL External Filter Components

3.13 OUTPUT CLOCKS & FRAME SYNC SIGNALS

The device supports 9 output clocks and 2 frame sync output signals altogether.

3.13.1 OUTPUT CLOCKS

The device provides 9 output clocks.

According to the output port technology, the output ports support the following technologies:

- AMI;
- PECL/LVDS;
- CMOS.

OUT1 ~ OUT5 and OUT9 output a CMOS signal.

OUT6 and OUT7 output a PECL or LVDS signal, as selected by the OUT6_PECL_LVDS bit and the OUT7_PECL_LVDS bit respectively.

OUT8 outputs an AMI signal.

The outputs on OUT1 ~ OUT7 are variable, depending on the signals derived from the T0/T4 DPLL and T0/T4 APLL outputs, and the corresponding OUTn_PATH_SEL[3:0] bits (1 ≤ n ≤ 7). The derived signal can be from the T0/T4 DPLL and T0/T4 APLL outputs, as selected by the corresponding OUTn_PATH_SEL[3:0] bits (1 ≤ n ≤ 7). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 25 for

the output frequency. If the signal is derived from the T0/T4 APLL output, please refer to Table 26~Table 27 for the output frequency.

The output on OUT8 is derived from T0 or T4 DPLL 77.76 MHz path, as selected by the OUT8_PATH_SEL bit. After being divided automatically, the output is of 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz, as selected by the 400HZ_SEL bit. Its duty cycle is 50:50 or 5:8, as determined by the AMI_OUT_DUTY bit.

The output on OUT9 is derived from T0 or T4 DPLL 16E1/16T1 path, as selected by the OUT9_PATH_SEL bit. After being divided automatically, the output is of 2.048 MHz or 1.544 MHz, as selected by the IN_SONET_SDH bit.

The outputs on OUT8 and OUT9 can be enabled or disabled, or may be affected by the status of the T4 input clock. It is determined by the OUT8_EN / OUT9_EN and T4_INPUT_FAIL¹ / T4_INPUT_FAIL² bits. Refer to Table 27.

The outputs on OUT1 to OUT7 and OUT9 can be inverted, as determined by the corresponding OUTn_INV bit (1 ≤ n ≤ 7 or n = 9).

All the output clocks derived from T0/T4 selected input clock are aligned with the T0/T4 selected input clock respectively every 125 μs period.

Table 25: Outputs on OUT1 ~ OUT7 if Derived from T0/T4 DPLL Outputs

OUTn_DIVIDER[3:0] (Output Divider) ¹	outputs on OUT1 ~ OUT7 if derived from T0/T4 DPLL outputs ²										
	77.76 MHz	12E1	16E1	24T1	16T1	E3	T3	GSM (26 MHz)	ETH	OBSAI (30.72 MHz)	GPS (40 MHz)
0000	Output is disabled (output low).										
0001											
0010		12E1	16E1	24T1	16T1	E3	T3		25 MHz		
0011		6E1	8E1	12T1	8T1			13 MHz		15.36 MHz	20 MHz
0100		3E1	4E1	6T1	4T1						10 MHz
0101		2E1		4T1							
0110			2E1	3T1	2T1						5 MHz
0111		E1		2T1							
1000			E1		T1						
1001				T1							
1010	64 kHz										
1011	8 kHz										
1100	2 kHz										
1101	400 Hz										
1110											
1111	Output is disabled (output high).										

Note:
 1. 1 ≤ n ≤ 7. Each output is assigned a frequency divider.
 2. E1 = 2.048 MHz, T1 = 1.544 MHz, E3 = 34.368 MHz, T3 = 44.736 MHz. The blank cell means the configuration is reserved.

Table 26: Outputs on OUT1 ~ OUT7 if Derived from T0/T4 APLL¹

OUTn_DIVIDER[3:0] (Output Divider) ²	Outputs on OUT1 ~ OUT7 if Derived from T0/T4 APLL Output ³										
	77.76 MHz X 4	12E1 X 4	16E1 X 4	24T1 X 4	16T1 X 4	E3	T3	GSM (26 MHz X 2)	OBSAI (30.72 MHz X 10)	GPS (40 MHz)	ETH
0000	Output is disabled (output low).										
0001	622.08 MHz ⁴										625 MHz
0010	311.04 MHz ⁴	48E1	64E1	96T1	64T1	E3	T3	104 MHz	307.2 MHz	40 MHz	125 MHz
0011	155.52 MHz	24E1	32E1	48T1	32T1			52 MHz	153.6 MHz	20 MHz	312.5 MHz
0100	77.76 MHz	12E1	16E1	24T1	16T1			26 MHz	76.8 MHz	10 MHz	156.25 MHz
0101	51.84 MHz	8E1		16T1				13 MHz			
0110	38.88 MHz	6E1	8E1	12T1	8T1				38.4 MHz	5 MHz	
0111	25.92 MHz	4E1		8T1							
1000	19.44 MHz	3E1	4E1	6T1	4T1						
1001		2E1		4T1					61.44 MHz		125 MHz
1010			2E1	3T1	2T1				30.72 MHz		
1011	6.48 MHz	E1		2T1					15.36 MHz		
1100			E1		T1				7.68 MHz		
1101				T1					3.84 MHz		
1110											
1111	Output is disabled (output high).										

Note:
1. For the APLL path selection, please refer to the registers T0_DPLL_APLL_PATH_CNFG (55H) and T4_DPLL_APLL_PATH_CNFG (60H) in [Chapter 7.2.7 T0 / T4 DPLL & APLL Configuration Registers](#).
2. $1 \leq n \leq 7$. Each output is assigned a frequency divider.
3. In the APLL, the selected T0/T4 DPLL output may be multiplied. E1 = 2.048 MHz, T1 = 1.544 MHz, E3 = 34.368 MHz, T3 = 44.736 MHz. The blank cell means the configuration is reserved.
4. The 622.08 MHz and 311.04 MHz differential signals are only output on OUT6 and OUT7.

Table 27: Outputs on OUT8 & OUT9

OUT8_EN / OUT9_EN	T4_INPUT_FAIL ¹ / T4_INPUT_FAIL ²	Outputs on OUT8 & OUT9
0	don't-care	Output is disabled (output low).
1	0	Output is enabled.
	1	Output is enabled when the T4 selected input clock does not fail. Output is disabled (output low) when the T4 selected input clock fails.

3.13.2 FRAME SYNC OUTPUT SIGNALS

An 8 kHz and a 2 kHz frame sync signals are output on the FRSYNC_8K and MFRSYNC_2K pins if enabled by the 8K_EN and 2K_EN bits respectively. They are CMOS outputs.

The two frame sync signals are derived from the T0 APLL output and are aligned with the output clock. They can be synchronized to the frame sync input signal.

If the frame sync input signal with respect to the T0 selected input clock is above a limit set by the SYNC_MON_LIMT[2:0] bits, an external sync alarm will be raised and EX_SYNC1 is disabled to synchronize the frame sync output signals. The external sync alarm is cleared once EX_SYNC1 with respect to the T0 selected input clock is within the limit. If it is within the limit, whether EX_SYNC1 is enabled to synchronize the frame sync output signal is determined by the AUTO_EXT_SYNC_EN bit and the EXT_SYNC_EN bit. Refer to Table 28 for details.

When the frame sync input signal is enabled to synchronize the frame sync output signal, it should be adjusted to align itself with the T0

selected input clock. Nominally, the falling edge of EX_SYNC1 is aligned with the rising edge of the T0 selected input clock. EX_SYNC1 may be 0.5 UI early/late or 1 UI late due to the circuit and board wiring delays. Setting the sampling of EX_SYNC1 by the SYNC_PH1[1:0] bits will compensate this early/late. Refer to Figure 11 to Figure 14.

The EX_SYNC_ALARM_MON bit indicates whether EX_SYNC1 is in external sync alarm status. The external sync alarm is indicated by the EX_SYNC_ALARM¹ bit. If the EX_SYNC_ALARM² bit is '1', the occurrence of the external sync alarm will trigger an interrupt.

The 8 kHz and the 2 kHz frame sync output signals can be inverted by setting the 8K_INV and 2K_INV bits respectively. The frame sync outputs can be 50:50 duty cycle or pulsed, as determined by the 8K_PUL and 2K_PUL bits respectively. When they are pulsed, the pulse width is defined by the period of OUT3; and they are pulsed on the position of the falling or rising edge of the standard 50:50 duty cycle, as selected by the 2K_8K_PUL_POSITION bit.

Table 28: Synchronization Control

AUTO_EXT_SYNC_EN	EXT_SYNC_EN	Synchronization
don't-care	0	Disabled
0	1	Enabled
1	1	Enabled if the T0 selected input clock is IN11; otherwise, disabled.

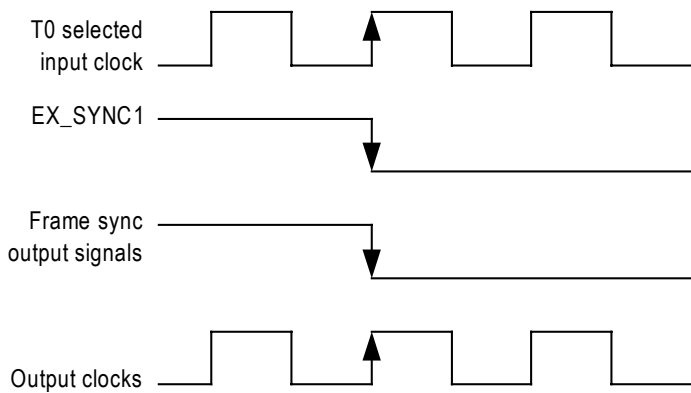


Figure 11. On Target Frame Sync Input Signal Timing

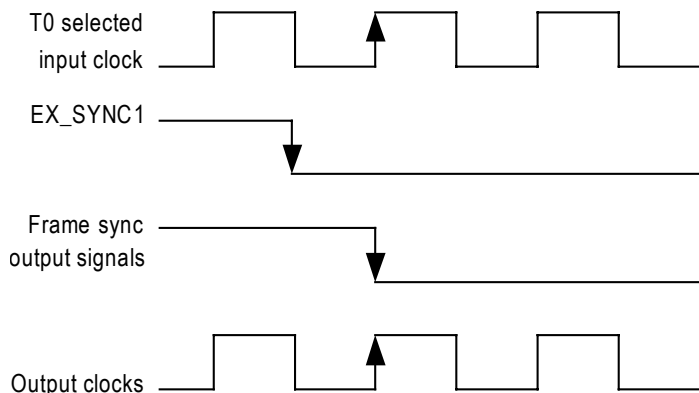


Figure 12. 0.5 UI Early Frame Sync Input Signal Timing

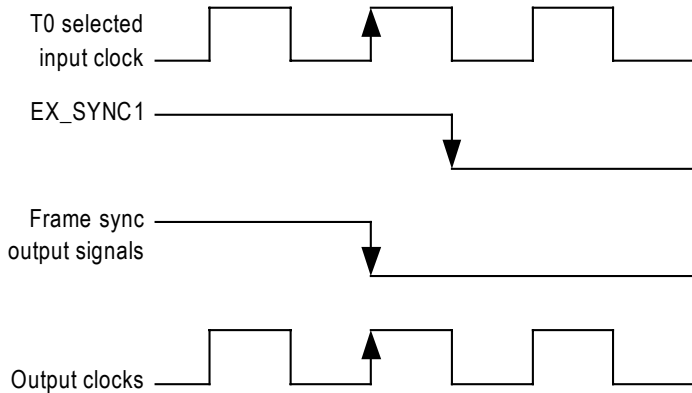


Figure 13. 0.5 UI Late Frame Sync Input Signal Timing

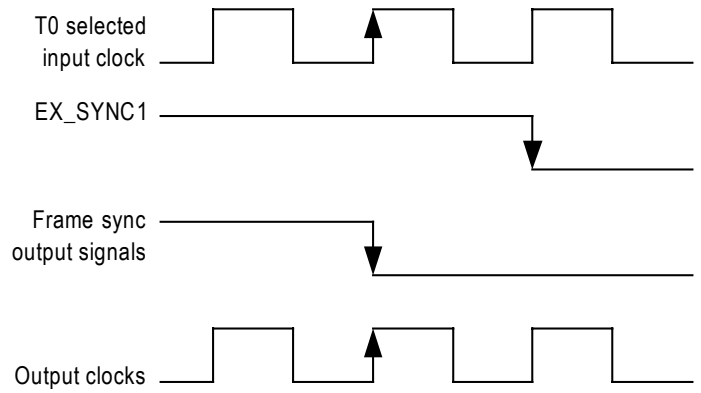


Figure 14. 1 UI Late Frame Sync Input Signal Timing

Table 29: Related Bit / Register in Chapter 3.13

Bit	Register	Address (Hex)
OUT6_PECL_LVDS	DIFFERENTIAL_IN_OUT_OSCI_CNFG	0A
OUT7_PECL_LVDS		
OUTn_PATH_SEL[3:0] (1 ≤ n ≤ 7)	OUT1_FREQ_CNFG ~ OUT7_FREQ_CNFG	6B ~ 71
OUTn_DIVIDER[3:0] (1 ≤ n ≤ 7)		
OUT8_PATH_SEL	OUT8_FREQ_CNFG	72
400HZ_SEL		
AMI_OUT_DUTY		
T4_INPUT_FAIL ¹		
OUT8_EN		
OUT9_PATH_SEL	OUT9_FREQ_CNFG	73
OUT9_EN		
T4_INPUT_FAIL ²		
IN_SONET_SDH	INPUT_MODE_CNFG	09
AUTO_EXT_SYNC_EN		
EXT_SYNC_EN		
OUTn_INV (1 ≤ n ≤ 7 or n = 9)	OUT9_FREQ_CNFG, OUT8_FREQ_CNFG	73, 72
8K_EN	FR_MFR_SYNC_CNFG	74
2K_EN		
8K_INV		
2K_INV		
8K_PUL		
2K_PUL		
2K_8K_PUL_POSITION		
SYNC_MON_LIMT[2:0]	SYNC_MONITOR_CNFG	7C
SYNC_PH1[1:0]	SYNC_PHASE_CNFG	7D
EX_SYNC_ALARM_MON	OPERATING_STS	52
EX_SYNC_ALARM ¹	INTERRUPTS3_STS	0F
EX_SYNC_ALARM ²	INTERRUPTS3_ENABLE_CNFG	12

3.14 MASTER / SLAVE CONFIGURATION

Master / Slave configuration is only supported by the T0 path of the device.

Two devices should be used together in order to:

- Enable system protection against single chip failure;
- Guarantee no service interrupt during system maintenance, such as software or hardware upgrade.

Of the two devices, one is configured as the Master and the other is configured as the Slave. The configuration is made by the MS/SL pin and the MS_SL_CTRL bit (b0, 13H), as shown in Table 30:

Table 30: Device Master / Slave Control

Master / Slave Control		Result
MS/SL pin	MS_SL_CTRL Bit	
High	0	Master
	1	Slave
Low	0	Slave
	1	Master

In this application, all the output clocks derived from the T0 selected input clock and the frame sync output signals from the two devices are at the same frequency offset and phase. Refer to Chapter 3.13.2 Frame SYNC Output Signals for details.

The difference between the Master and the Slave is: in the Master, the IN11 should not be selected by the T0 DPLL; in the Slave, the following functions are automatically forced:

- The T0 selected input clock is IN11;
- T0 HS is disabled;
- T0 DPLL operates at the acquisition bandwidth and damping factor;
- EX_SYNC1 is used for synchronization;
- T0 DPLL operates in Locked mode.

In the Slave, the corresponding registers of the above forced functions can still be configured, but their configuration does not take any effect. The frequency of the T0 selected input clock IN11 is recommended to be 6.48 MHz.

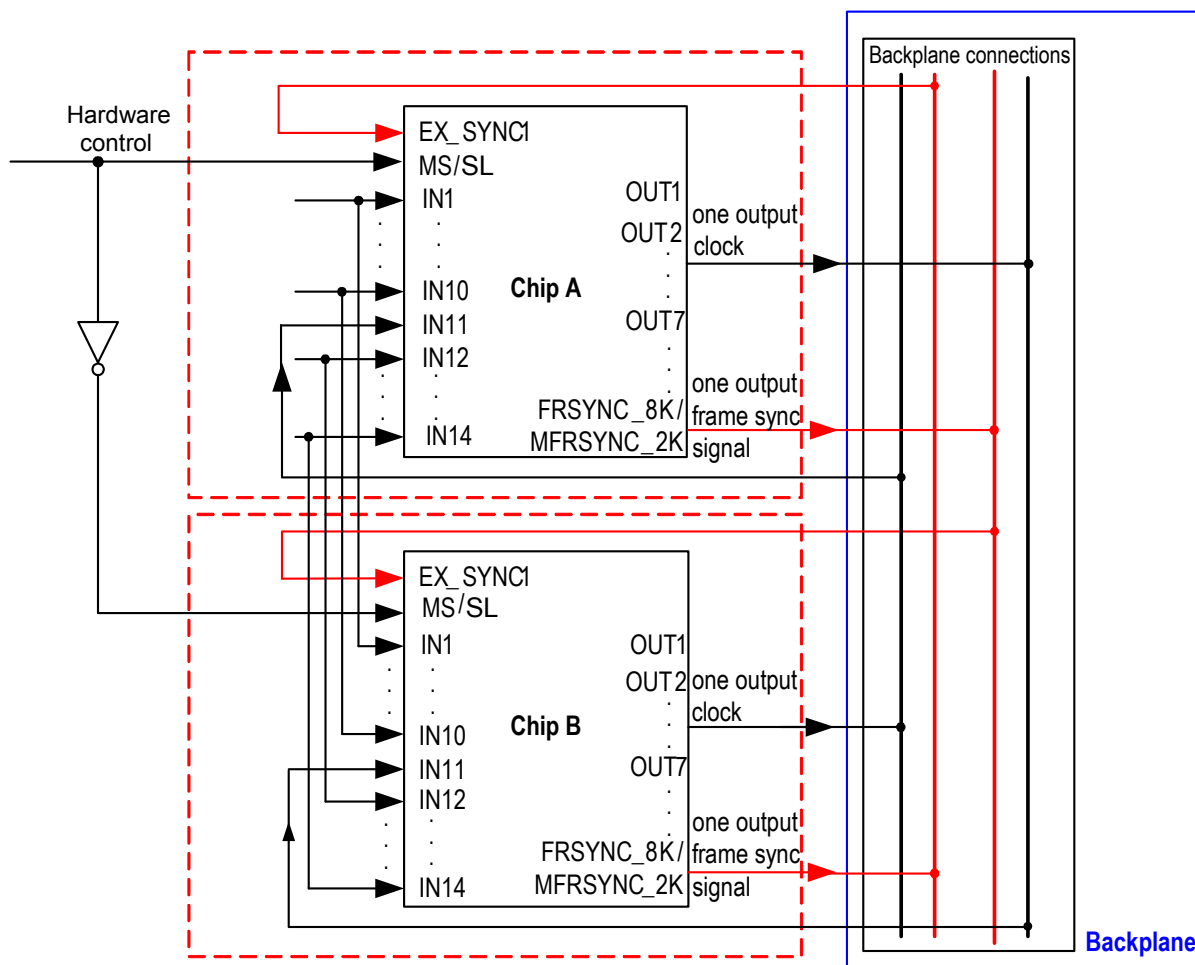


Figure 15. Physical Connection Between Two Devices

3.15 INTERRUPT SUMMARY

The interrupt sources of the device are as follows:

- AMI violation
- LOS
- T4 DPLL locking status change
- Input clocks for T0 path validity change
- T0 selected input clock fail
- Input clocks for T4 path change to be no qualified input clock available
- T0 DPLL operating mode switch
- External sync alarm

All of the above interrupt events are indicated by the corresponding interrupt status bit. If the corresponding interrupt enable bit is set, any of the interrupts can be reported by the INT_REQ pin. The output characteristics on the INT_REQ pin are determined by the HZ_EN bit and the INT_POL bit.

Interrupt events are cleared by writing a '1' to the corresponding interrupt status bit. The INT_REQ pin will be inactive only when all the pending enabled interrupts are cleared.

In addition, the interrupt of T0 selected input clock fail can be reported by the TDO pin, as determined by the LOS_FLAG_TO_TDO bit. Refer to [Chapter 7.2.2 Interrupt Registers](#).

Table 31: Related Bit / Register in Chapter 3.15

Bit	Register	Address (Hex)
HZ_EN	INTERRUPT_CNFG	0C
INT_POL		
LOS_FLAG_TO_TDO	MON_SW_HS_CNFG	0B

3.16 T0 AND T4 SUMMARY

The main features supported by the T0 path are as follows:

- Phase lock alarm;
- Forced or Automatic input clock selection/switch;
- 3 primary and 3 secondary, temporary DPLL operating modes, switched automatically or under external control;
- Automatic switch between starting, acquisition and locked bandwidths/damping factors;
- Programmable DPLL bandwidths from 0.5 mHz to 560 Hz in 19 steps;
- Programmable damping factors: 1.2, 2.5, 5, 10 and 20;
- Fast loss, coarse phase loss, fine phase loss and hard limit exceeding monitoring;
- Output phase and frequency offset limited;
- Automatic Instantaneous, Automatic Slow Averaged, Automatic Fast Averaged or Manual holdover frequency offset acquiring;
- Hitless switch to minimize output phase transients;
- Programmable output phase offset;
- Low jitter multiple clock outputs with programmable polarity;
- Low jitter 2 kHz and 8 kHz frame sync signal outputs with programmable pulse width and polarity;
- Master / Slave application to enable system protection against single device failure.

The main features supported by the T4 path are as follows:

- Forced or Automatic input clock selection/switch;
- Locking to T0 DPLL output;
- 3 DPLL operating modes, switched automatically or under external control;
- Programmable DPLL bandwidth: 18 Hz, 35 Hz, 70 Hz and 560 Hz;
- Programmable damping factor: 1.2, 2.5, 5, 10 and 20;
- Fast loss, coarse phase loss, fine phase loss and hard limit exceeding monitoring;
- Output phase and frequency offset limited;
- Automatic Instantaneous holdover frequency offset;
- Low jitter multiple clock outputs with programmable polarity.

3.17 POWER SUPPLY FILTERING TECHNIQUES

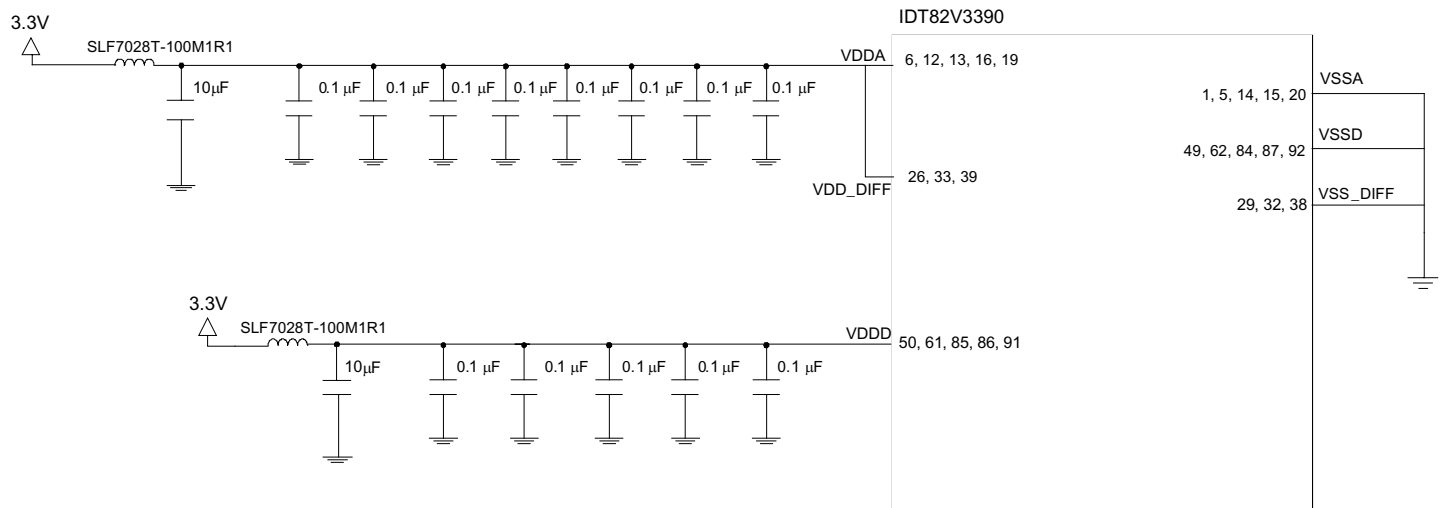


Figure 16. IDT82V3390 Power Decoupling Scheme

To achieve optimum jitter performance, power supply filtering is required to minimize supply noise modulation of the output clocks. The common sources of power supply noise are switch power supplies and the high switching noise from the outputs to the internal PLL. The IDT82V3390 provides separate VDDA power pins for the internal analog PLL, VDD_DIFF for the differential output driver circuit and VDDD pins for the core logic as well as I/O driver circuits.

To minimize switching power supply noise generated by the switching regulator, the power supply output should be filtering with sufficient bulk capacity to minimize ripple and 0.1 uF (0402 case size, ceramic) caps to filter out the switching transients.

For the IDT82V3390, the decoupling for VDDA, VDD_DIFF and VDDD are handled individually. VDDD, VDD_DIFF and VDDA should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. Figure 16 illustrated how bypass capacitor and ferrite bead should be connected to power pins.

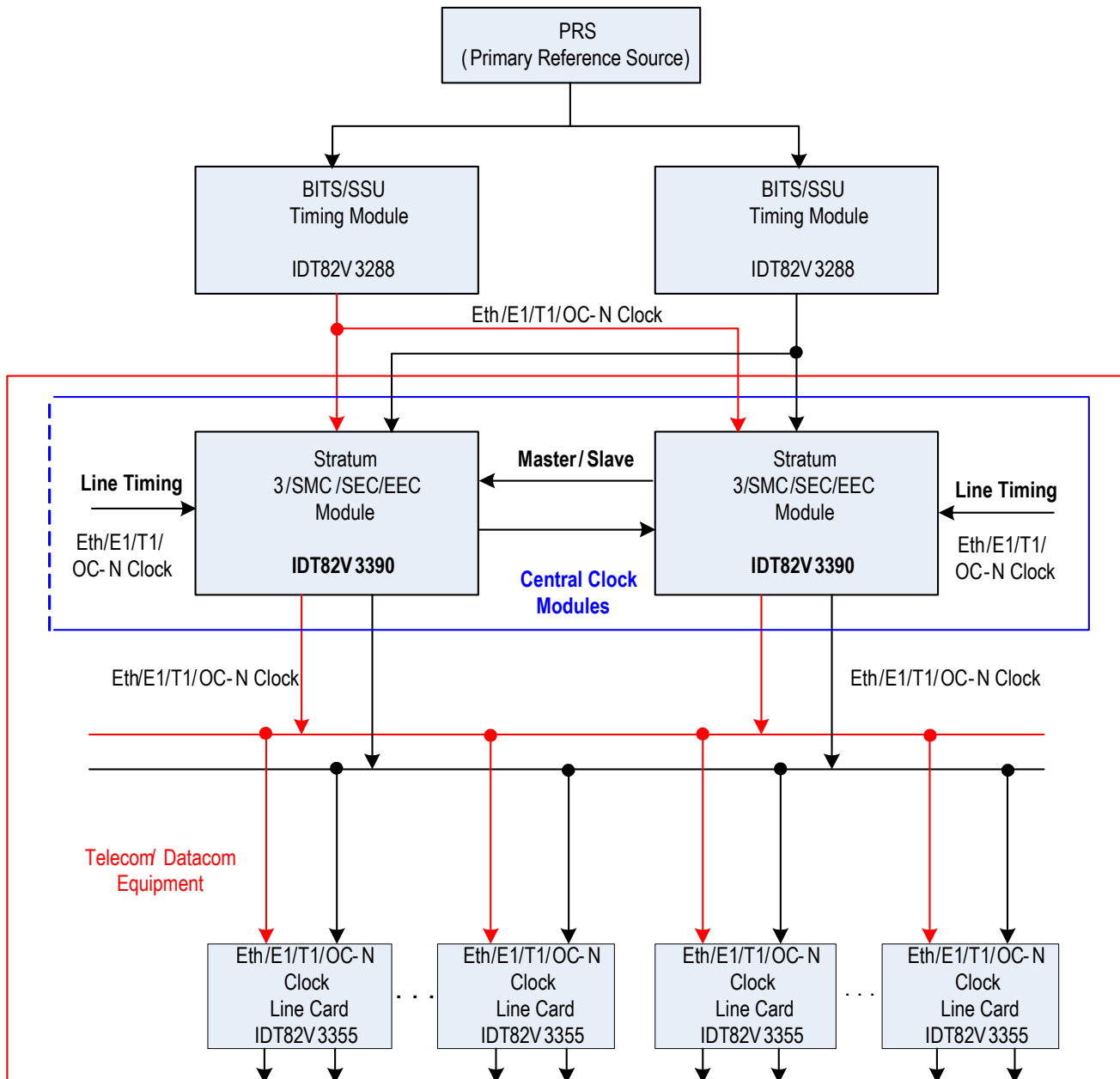
The analog power supply VDDA and VDD_DIFF should have low impedance. This can be achieved by using one 10 uF (1210 case size, ceramic) and at least eight 0.1 uF (0402 case size, ceramic) capacitors in parallel. The 0.1 uF (0402 case size, ceramic) capacitors must be placed right next to the VDDA and VDD_DIFF pins as close as possible. Note that the 10 uF capacitor must be of 1210 case size, and it must be ceramic for lowest ESR (Effective Series Resistance) possible. The 0.1 uF should be of case size 0402, this offers the lowest ESL (Effective Series Inductance) to achieve low impedance towards the high speed range.

For VDDD, at least five 0.1 uF (0402 case size, ceramic) and one 10 uF (1210 case size, ceramic) capacitors are recommended. The 0.1 uF capacitors should be placed as close to the VDDD pins as possible.

Please refer to evaluation board schematic for details.

4 TYPICAL APPLICATION

The device supports Master / Slave application, as shown in Figure 17:



note: Eth = Ethernet

Figure 17. Typical Application

4.1 MASTER / SLAVE APPLICATION

Master / Slave application is only supported by the T0 path of the device.

In Master / Slave application, two devices should be used together. Of the two devices, one is configured as the Master and the other is configured as the Slave. Refer to Chapter 3.14 Master / Slave Configuration for details.

5 MICROPROCESSOR INTERFACE

The microprocessor interface provides access to read and write the registers in the device. The microprocessor interface supports the following six modes:

- EPROM mode;
- Multiplexed mode;
- Intel mode;
- Motorola mode;
- Serial mode.
- I2C mode

The microprocessor interface mode is selected by the MPU_SEL_CNFG[2:0] bits (b2~0, 7FH). The interface pins in different interface modes are listed in Table 32 and Table 33.

Table 32: Microprocessor Interface

MPU_SEL_CNFG[2:0] bits	Microprocessor Interface Mode	Interface Pins
001	EPROM	CS, A[6:0], AD[7:0]
010	Multiplexed	CS, ALE, WR, RD, AD[7:0], RDY
011	Intel	CS, WR, RD, A[6:0], AD[7:0], RDY
100	Motorola	CS, WR, A[6:0], AD[7:0], RDY
101	Serial	CS, SCLK, SDI, SDO, CLKE
110	I2C	I2C_AD[2:0], I2C_SDA, I2C_SCL
111	Serial	CS, SCLK, SDI, SDO, CLKE

Table 33: Microprocessor Interface Pins

PIN	MODE					
	EPROM	MULTIPLEXED	INTEL	MOTOROLA	SERIAL	I2C
A0 / SDI	OUTPUT	INPUT (Note 1)	INPUT	INPUT	INPUT	INPUT (Note 1)
A1 / CLKE	OUTPUT	INPUT (Note 1)	INPUT	INPUT	INPUT	INPUT (Note 1)
A2	OUTPUT	INPUT (Note 1)	INPUT	INPUT	INPUT (Note 1)	INPUT (Note 1)
A3	OUTPUT	INPUT (Note 1)	INPUT	INPUT	INPUT (Note 1)	INPUT (Note 1)
A4	OUTPUT	INPUT (Note 1)	INPUT	INPUT	INPUT (Note 1)	INPUT (Note 1)
A5	OUTPUT	INPUT (Note 1)	INPUT	INPUT	INPUT (Note 1)	INPUT (Note 1)
A6	OUTPUT	INPUT (Note 1)	INPUT	INPUT	INPUT (Note 1)	INPUT (Note 1)
AD0/SD0/I2C_SDA	INPUT	INPUT/OUTPUT	INPUT/OUTPUT	INPUT/OUTPUT	OUTPUT	INPUT/OUTPUT
AD[7:1]	INPUT	INPUT/OUTPUT	INPUT/OUTPUT	INPUT/OUTPUT	INPUT (Note 1)	INPUT (Note 1)
CS/I2C_AD0	OUTPUT	INPUT	INPUT	INPUT	INPUT	INPUT
WR/I2C_AD1	INPUT (Note 1)	INPUT	INPUT	INPUT	INPUT (Note 1)	INPUT
RD/I2C_AD2	INPUT (Note 1)	INPUT	INPUT	INPUT (Note 1)	INPUT (Note 1)	INPUT
RDY (Note 2)	Output (Note 1)	OUTPUT	OUTPUT	OUTPUT	Output (Note 1)	Output (Note 1)
ALE/SCLK/I2C_SCL	INPUT (Note 1)	INPUT	INPUT (Note 1)	INPUT (Note 1)	INPUT	INPUT

After reset de-assertion, wait 10 us for the mode to be active.

Note 1: This pin is not used in this mode, this pin should be connected to ground

Note 2: This pin is open drain

5.1 EPROM MODE

When the MPU_SEL_CNFG[2:0] bits (b2~0, 7FH) is set to '001', EPROM mode is selected. In this mode, the device is used with an EPROM, in which configuration data is stored in a sequential way. The address 0 of configuration data is corresponding the register 00H. An

internal counter controls the read operations to the EPROM data. The value of ID[15:0] is checked with the device ID of our chip. If the number is matched, The configuration data will be automatically read from the EPROM.

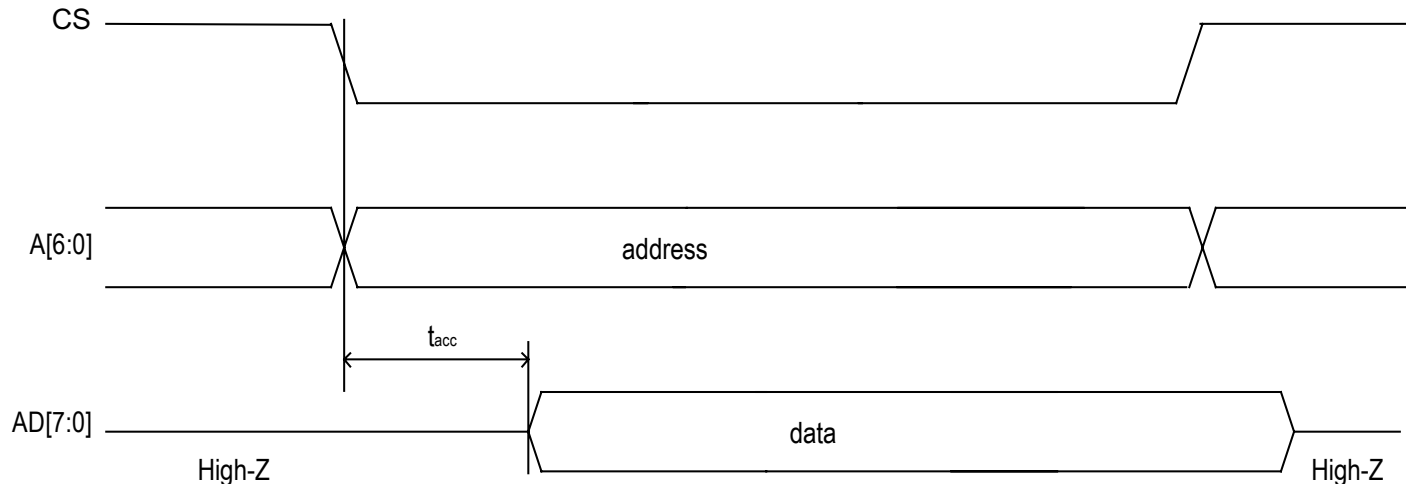


Figure 18. EPROM Access Timing Diagram

Table 34: Access Timing Characteristics in EPROM Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_{acc}	CS to valid data delay time			920	ns

5.2 MULTIPLEXED MODE

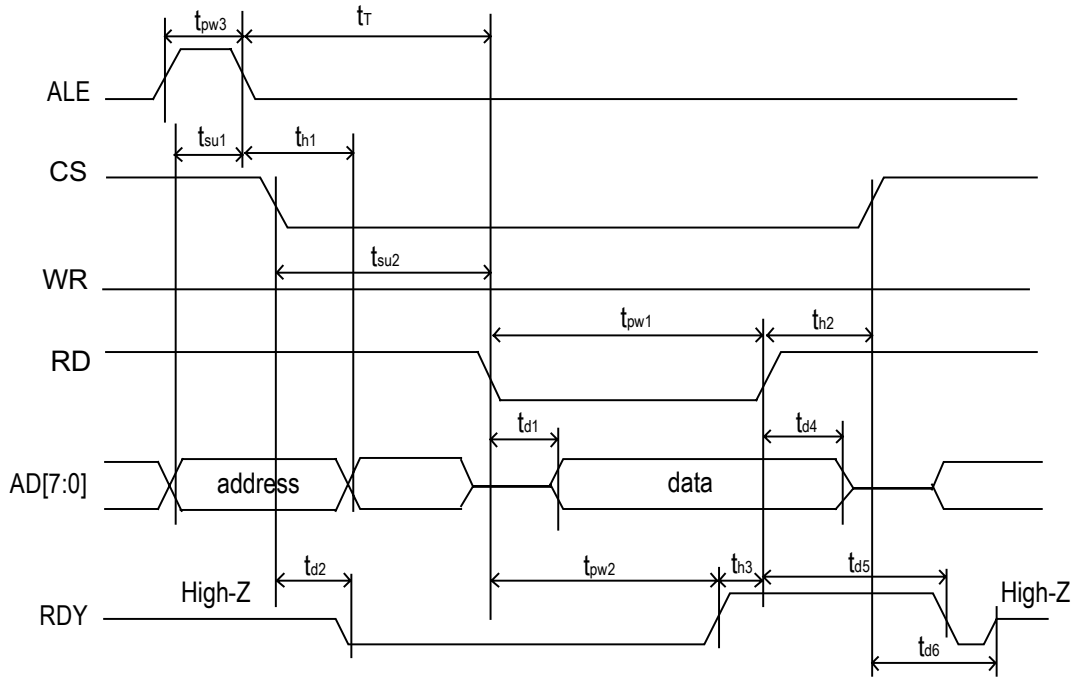


Figure 19. Multiplexed Read Timing Diagram

Table 35: Read Timing Characteristics in Multiplexed Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns

Table 35: Read Timing Characteristics in Multiplexed Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid address to ALE falling edge setup time	2			ns
t_{su2}	Valid CS to Valid RD setup time	0			ns
t_{d1}	Valid RD to valid data delay time			5T + 10	ns
t_{d2}	Valid CS to valid RDY delay time		13		ns
t_{d4}	RD rising edge to AD[7:0] high impedance delay time		10		ns
t_{d5}	RD rising edge to RDY low delay time		13		ns
t_{d6}	CS rising edge to RDY release delay time		13		ns
t_{pw1}	Valid RD pulse width low	4.5T + 10 *			ns
t_{pw2}	Valid RDY pulse width low	4.5T + 10			ns
t_{pw3}	Valid ALE pulse width high	2			ns
t_{h1}	Valid address after ALE falling edge hold time	3			ns
t_{h2}	Valid CS after RD rising edge hold time	0			ns
t_{h3}	Valid RD after RDY rising edge hold time	0			ns
t_T	Time between ALE falling edge and RD falling edge	0			ns
t_{T1}	Time between consecutive Read-Read or Read-Write accesses (RD rising edge to ALE rising edge)	>T			ns

Note:

* Timing with RDY. If RDY is not used, t_{pw1} is 3.5T + 10.

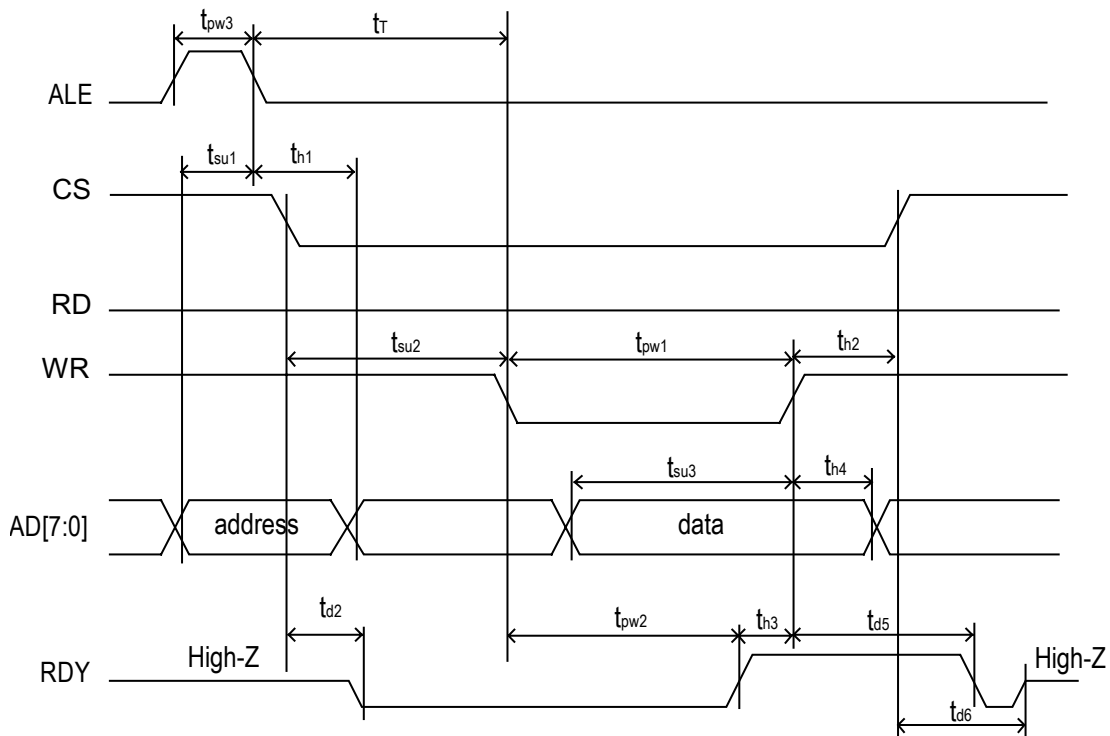


Figure 20. Multiplexed Write Timing Diagram

Table 36: Write Timing Characteristics in Multiplexed Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t _{in}	Delay of input pad		5		ns
t _{out}	Delay of output pad		5		ns
t _{su1}	Valid address to ALE falling edge setup time	2			ns
t _{su2}	Valid CS to valid WR setup time	0			ns
t _{su3}	Valid data to WR rising edge setup time	3			ns
t _{d2}	Valid CS to valid RDY delay time		13		ns
t _{d5}	WR rising edge to RDY low delay time		13		ns
t _{d6}	CS rising edge to RDY release delay time		13		ns
t _{pw1}	Valid WR pulse width low	1.5T + 10			ns
t _{pw2}	Valid RDY pulse width low	1.5T + 10			ns
t _{pw3}	Valid ALE pulse width high	2			ns
t _{h1}	Valid address after ALE falling edge hold time	3			ns
t _{h2}	Valid CS after WR rising edge hold time	0			ns
t _{h3}	Valid WR after RDY rising edge hold time	0			ns
t _{h4}	Valid data after WR rising edge hold time	9			ns
t _T	Time between ALE falling edge and WR falling edge	0			ns
t _{T1}	Time between consecutive Write-Read or Write-Write accesses (WR rising edge to ALE rising edge)	>7T			ns

5.3 INTEL MODE

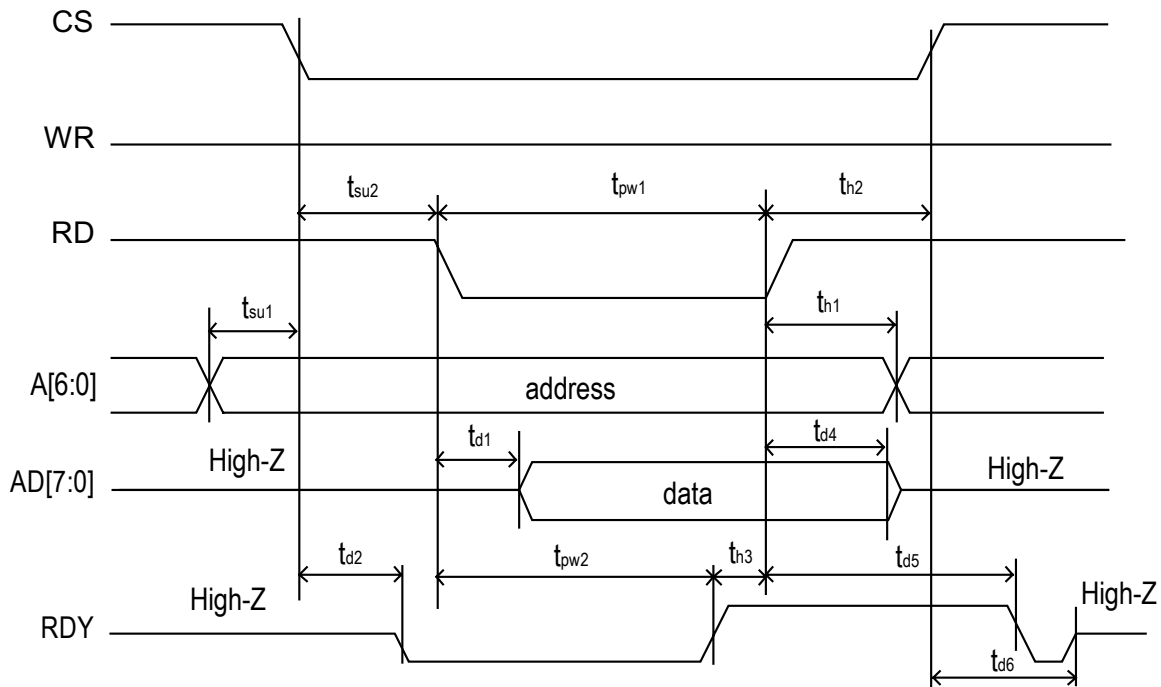


Figure 21. Intel Read Timing Diagram

Table 37: Read Timing Characteristics in Intel Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid address to valid CS setup time	0			ns
t_{su2}	Valid CS to valid RD setup time	0			ns
t_{d1}	Valid RD to valid data delay time			5T + 10	ns
t_{d2}	Valid CS to valid RDY delay time		13		ns
t_{d4}	RD rising edge to AD[7:0] high impedance delay time		10		ns
t_{d5}	RD rising edge to RDY low delay time		13		ns
t_{d6}	CS rising edge to RDY release delay time		13		ns
t_{pw1}	Valid RD pulse width low	4.5T + 10 *			ns
t_{pw2}	Valid RDY pulse width low	4.5T + 10			ns
t_{h1}	Valid address after RD rising edge hold time	0			ns
t_{h2}	Valid CS after RD rising edge hold time	0			ns
t_{h3}	Valid RD after RDY rising edge hold time	0			ns
t_{T1}	Time between consecutive Read-Read or Read-Write accesses (RD rising edge to RD falling edge, or RD rising edge to WR falling edge)	>T			ns

Note:

* Timing with RDY. If RDY is not used, t_{pw1} is 3.5T + 10.

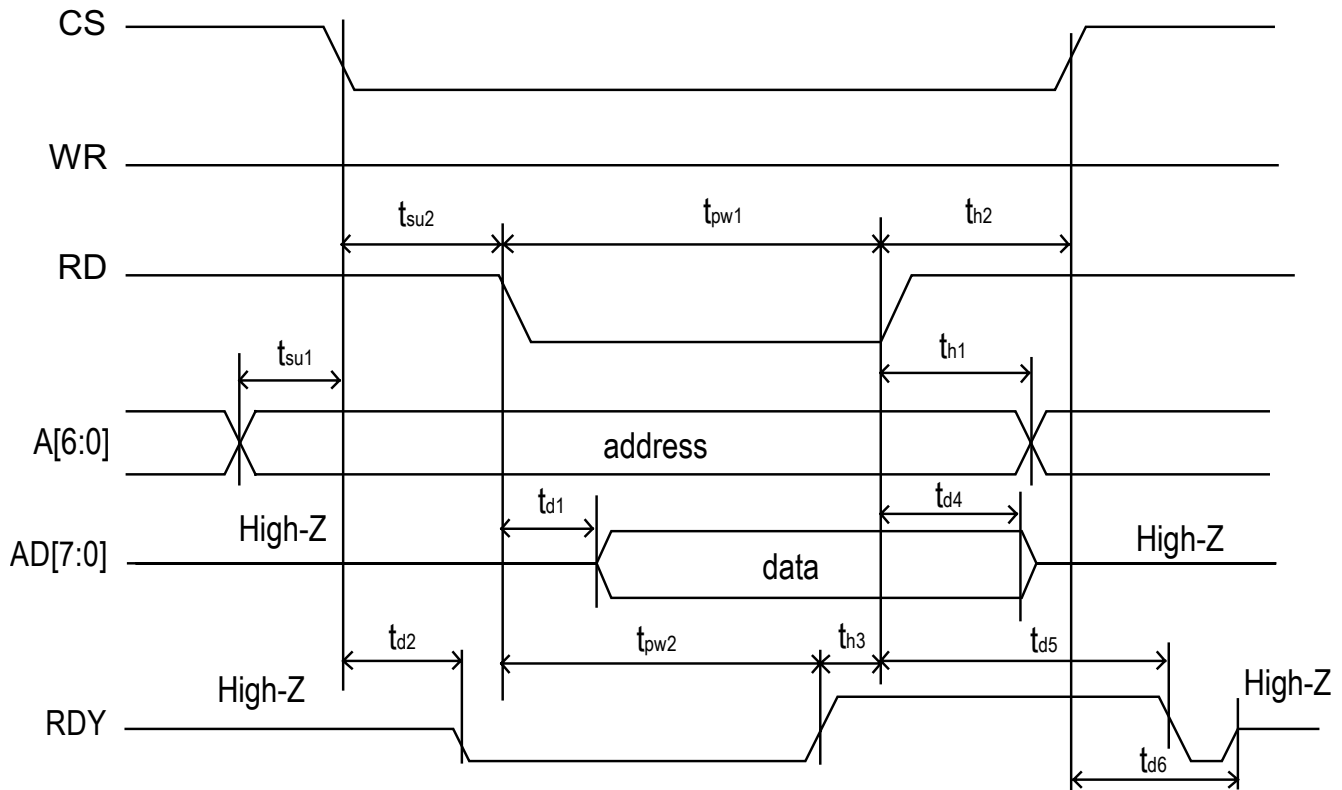


Figure 22. Intel Write Timing Diagram

Table 38: Write Timing Characteristics in Intel Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid address to valid CS setup time	0			ns
t_{su2}	Valid CS to valid WR setup time	0			ns
t_{su3}	Valid data before WR rising edge setup time	3			ns
t_{d2}	Valid CS to valid RDY delay time		13		ns
t_{d5}	WR rising edge to RDY low delay time		13		ns
t_{d6}	CS rising edge to RDY release delay time		13		ns
t_{pw1}	Valid WR pulse width low	$1.5T + 10$			ns
t_{pw2}	Valid RDY pulse width low	$1.5T + 10$			ns
t_{h1}	Valid address after WR rising edge hold time	0			ns
t_{h2}	Valid CS after WR rising edge hold time	0			ns
t_{h3}	Valid WR after RDY rising edge hold time	0			ns
t_{h4}	Valid data after WR rising edge hold time	9			ns
t_{T1}	Time between consecutive Write-Read or Write-Write accesses (WR rising edge to WR falling edge, or WR rising edge to RD falling edge)	$>7T$			ns

5.4 MOTOROLA MODE

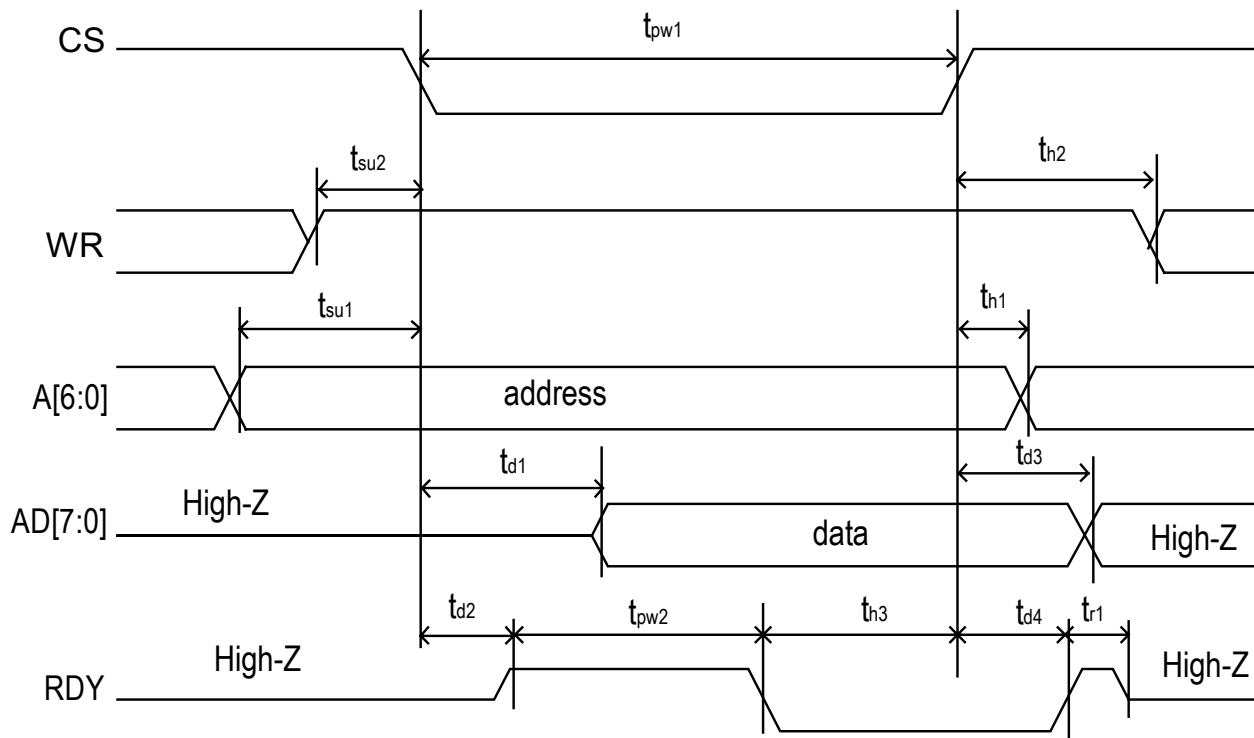


Figure 23. Motorola Read Timing Diagram

Table 39: Read Timing Characteristics in Motorola Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid address to valid CS setup time	0			ns
t_{su2}	Valid WR to valid CS setup time	0			ns
t_{d1}	Valid CS to valid data delay time			5T + 10	ns
t_{d2}	Valid CS to valid RDY delay time		13		ns
t_{d3}	CS rising edge to AD[7:0] high impedance delay time		10		ns
t_{d4}	CS rising edge to RDY release delay time		13		ns
t_{pw1}	Valid CS pulse width low	4.5T + 10 *			ns
t_{pw2}	Valid RDY pulse width high	4.5T + 10			ns
t_{h1}	Valid address after CS rising edge hold time	0			ns
t_{h2}	Valid WR after CS rising edge hold time	0			ns
t_{h3}	Valid CS after RDY falling edge hold time	0			ns
t_{r1}	RDY release time		3		ns
t_{T1}	Time between consecutive Read-Read or Read-Write accesses (CS rising edge to CS falling edge)	> T			ns

Note:

* Timing with RDY. If RDY is not used, t_{pw1} is 3.5T + 10.

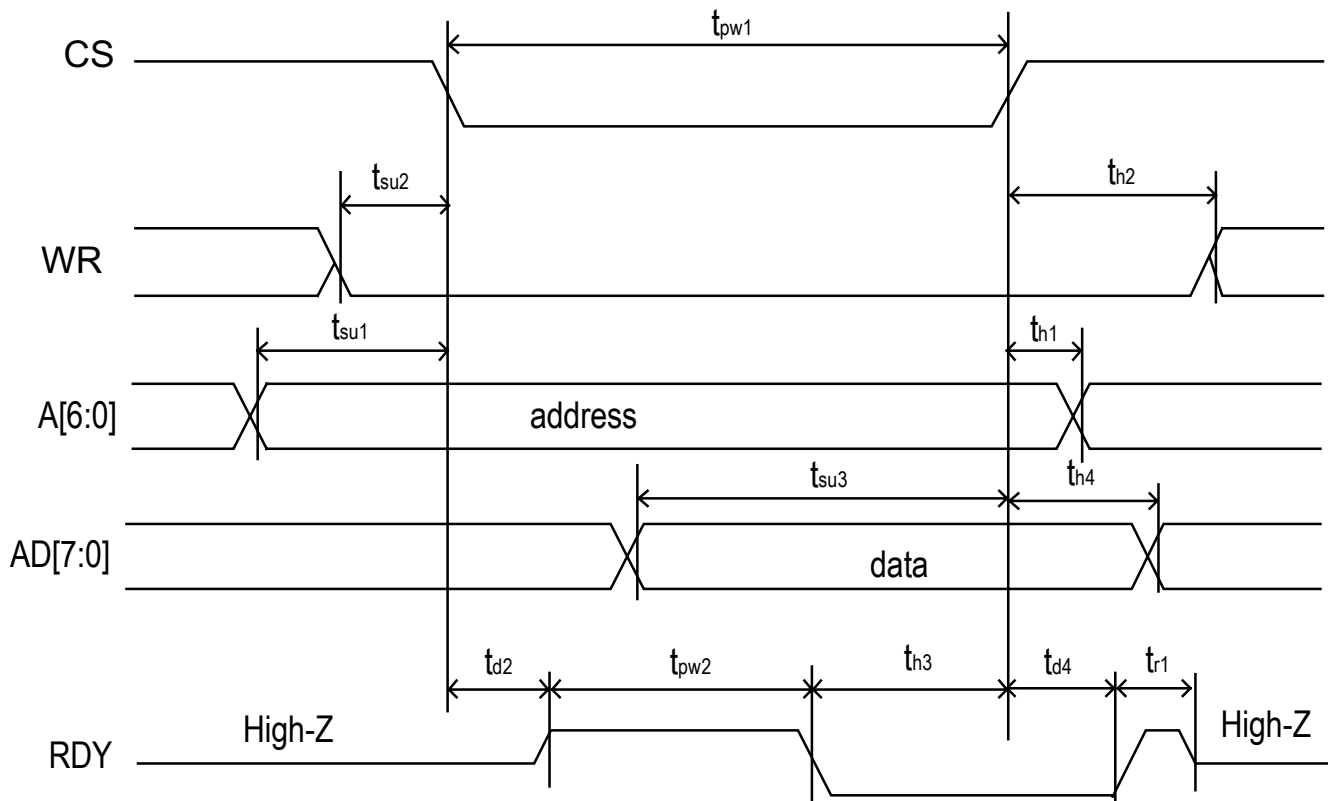


Figure 24. Motorola Write Timing Diagram

Table 40: Write Timing Characteristics in Motorola Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid address to valid CS setup time	0			ns
t_{su2}	Valid WR to valid CS setup time	0			ns
t_{su3}	Valid data before CS rising edge setup time	3			ns
t_{d2}	Valid CS to valid RDY delay time		13		ns
t_{d4}	CS rising edge to RDY release delay time		13		ns
t_{pw1}	Valid CS pulse width low	5T			ns
t_{pw2}	Valid RDY pulse width high	5T			ns
t_{h1}	Valid address after valid CS rising edge hold time	0			ns
t_{h2}	Valid WR after valid CS rising edge hold time	0			ns
t_{h3}	Valid CS after RDY falling edge hold time	0			ns
t_{h4}	Valid data after valid CS rising edge hold time	9			ns
t_{r1}	RDY release time		3		ns
t_{T1}	Time between consecutive Write-Write or Write-Read accesses (CS rising edge to CS falling edge)	> 7T			ns

5.5 SERIAL MODE

In a read operation, the active edge of SCLK is selected by CLKE. When CLKE is asserted low, data on SDO will be clocked out on the rising edge of SCLK.

When CLKE is asserted high, data on SDO will be clocked out on the falling edge of SCLK.

In a write operation, data on SDI will be clocked in on the rising edge of SCLK.

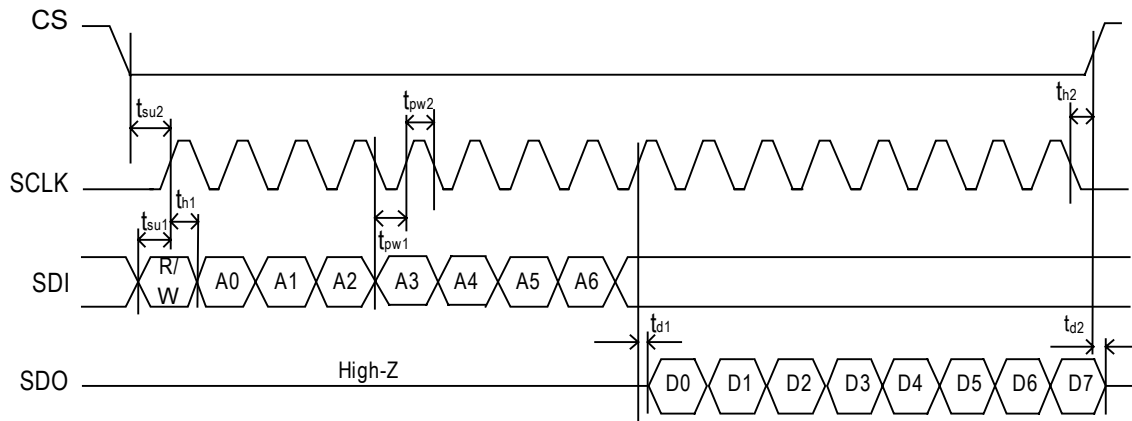


Figure 25. Serial Read Timing Diagram (CLKE Asserted Low)

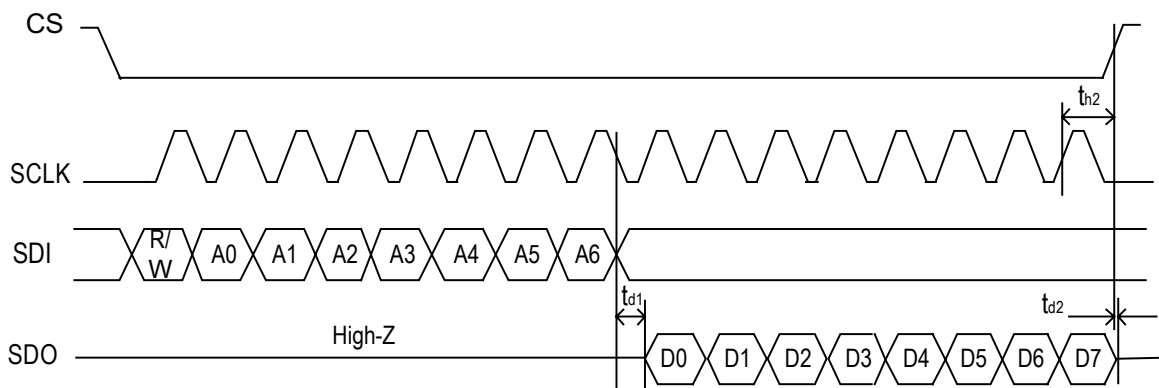


Figure 26. Serial Read Timing Diagram (CLKE Asserted High)

Table 41: Read Timing Characteristics in Serial Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t _{in}	Delay of input pad		5		ns
t _{out}	Delay of output pad		5		ns
t _{su1}	Valid SDI to valid SCLK setup time	4			ns
t _{su2}	Valid CS to valid SCLK setup time	14			ns
t _{d1}	Valid SCLK to valid data delay time		10		ns
t _{d2}	CS rising edge to SDO high impedance delay time		10		ns
t _{pw1}	SCLK pulse width low	5T + 10			ns
t _{pw2}	SCLK pulse width high	5T + 10			ns
t _{h1}	Valid SDI after valid SCLK hold time	6			ns
t _{h2}	Valid CS after valid SCLK hold time (CLKE = 0/1)	5			ns
t _{T1}	Time between consecutive Read-Read or Read-Write accesses (CS rising edge to CS falling edge)	10			ns

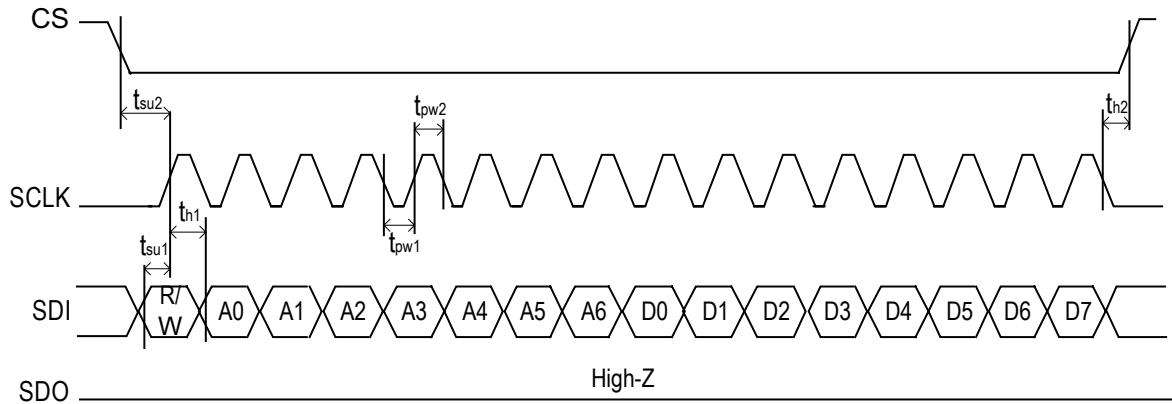


Figure 27. Serial Write Timing Diagram

Table 42: Write Timing Characteristics in Serial Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid SDI to valid SCLK setup time	4			ns
t_{su2}	Valid CS to valid SCLK setup time	14			ns
t_{pw1}	SCLK pulse width low	5T+10			ns
t_{pw2}	SCLK pulse width high	5T+10			ns
t_{h1}	Valid SDI after valid SCLK hold time	6			ns
t_{h2}	Valid CS after valid SCLK hold time	5			ns
t_{T1}	Time between consecutive Write-Write or Write-Read accesses (CS rising edge to CS falling edge)	10			ns

5.6 I2C MODE

5.6.2 I2C BUS TIMING

5.6.1 I2C DEVICE ADDRESS

Figure 28 shows the definition of I2C bus timing.

The higher 4-bit address is fixed to 4'b1010. The lower 3-bit address is set by pins I2C_AD2, I2C_AD1, I2C_AD0.

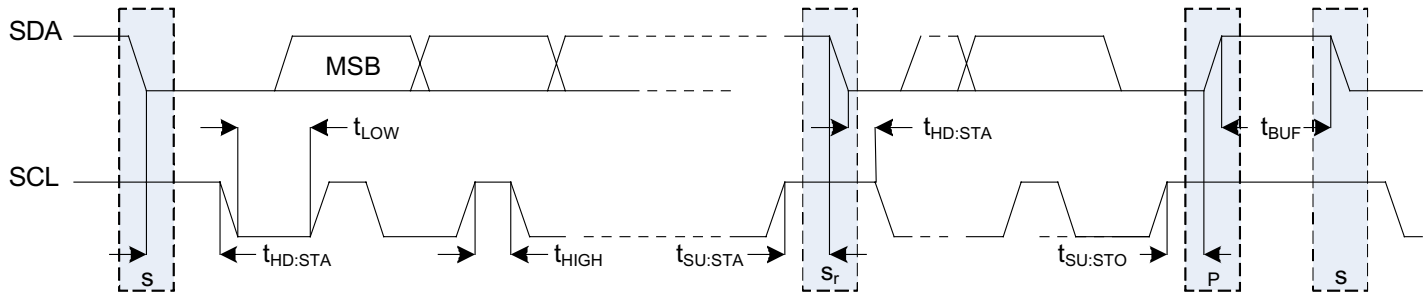


Figure 28. Definition of I2C Bus Timing

Table 43: Description of Timing Parameters of I2C Master Interface

Symbol	Description
f _{SCL}	SCL clock frequency
t _{SCL}	SCL clock period
t _{SU:DAT}	Data setup time
t _{HD:DAT}	Data hold time
t _{HD:STA}	Hold time for (repeated) START condition
t _{LOW}	LOW period of the SCL clock
t _{HIGH}	HIGH period of the SCL clock
t _{SU:STA}	Setup time for a repeated START condition
t _{SU:STO}	Setup time for STOP condition
t _{BUF}	Bus free time between a STOP and START condition

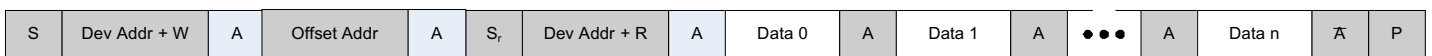
5.6.3 SUPPORTED TRANSACTIONS

The supported types of transactions are shown below.

Current Read



Sequential Read



Sequential Write



- from master to slave
- from slave to master
- S = start
- S_r = repeated start
- A = acknowledge
- A-bar = not acknowledge
- P = stop

Figure 29. I2C Slave Interface Supported Transactions

Table 44: Description of I2C Slave Interface Supported Transactions

Operation	Description
Current Read	Reads a burst of data from an internal determined starting address, this starting address is equal to the last address accessed during the last read or write operation, increment by one. If the address exceeds the address space, it will start from 0 again.
Sequential Read	Reads a burst of data from a specified address space. The starting address of the space is specified as offset address.
Sequential Write	Writes a burst of data to a specified address space, the starting address of the space is specified as offset address.

6 JTAG

This device is compliant with the IEEE 1149.1 Boundary Scan standard except the following:

- The output boundary scan cells do not capture data from the core and the device does not support EXTEST instruction;
- The TRST pin is set low by default and JTAG is disabled in order to be consistent with other manufacturers.

The JTAG interface timing diagram is shown in [Figure 30](#).

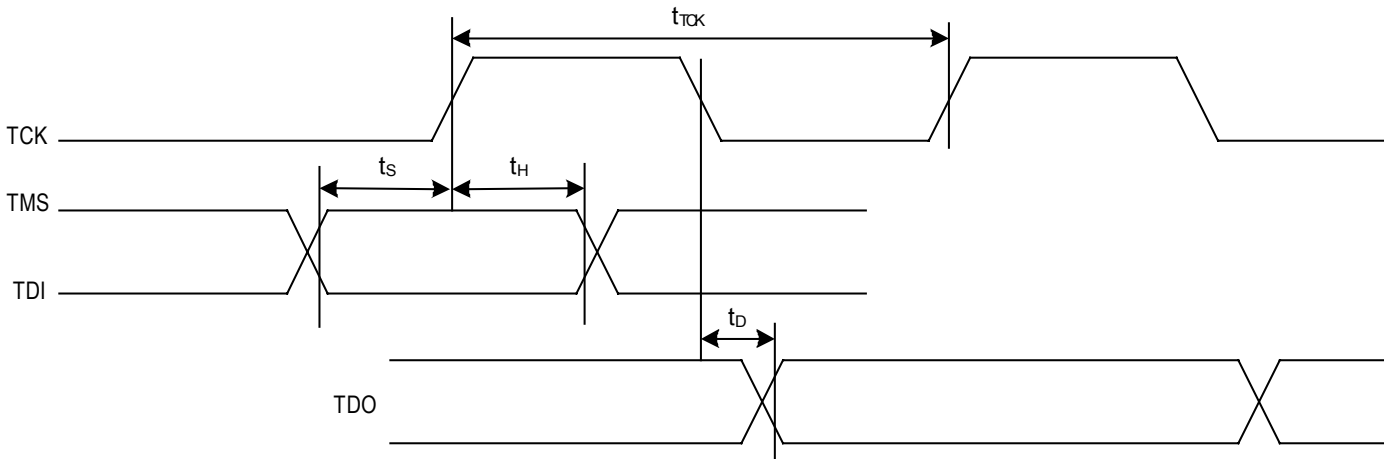


Figure 30. JTAG Interface Timing Diagram

Table 45: JTAG Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{TCK}	TCK period	100			ns
t_s	TMS / TDI to TCK setup time	25			ns
t_H	TCK to TMS / TDI Hold Time	25			ns
t_D	TCK to TDO delay time			50	ns

7 PROGRAMMING INFORMATION

After reset, all the registers are set to their default values. The registers are read or written via the microprocessor interface.

Before any write operation, the value in register PROTECTION_CNFG is recommended to be confirmed to make sure whether the write operation is enabled. The device provides 3 register protection modes:

- Protected mode: no other registers can be written except register PROTECTION_CNFG itself;
- Fully Unprotected mode: all the writable registers can be written;
- Single Unprotected mode: one more register can be written besides register PROTECTION_CNFG. After write operation (not including writing a '1' to clear a bit to '0'), the device automatically switches to Protected mode.

Writing '0' to the registers will take no effect if the registers are cleared by writing '1'.

T0 and T4 paths share some registers, whose addresses are 26H ~ 2CH, 4EH, 4FH, 5AH, 5BH, 62H ~ 64H, 68H and 69H. The names of shared registers are marked with a *. Before register read/write operation, register T4_T0_REG_SEL_CNFG is recommended to be confirmed to make sure whether the register operation is available for T0 or T4 path.

The access of the Multi-word Registers is different from that of the Single-word Registers. Take the registers (04H, 05H and 06H) for an example, the write operation for the Multi-word Registers follows a fixed sequence. The register (04H) is configured first and the register (06H) is configured last. The three registers are configured continuously and should not be interrupted by any operation. The crystal calibration configuration will take effect after all the three registers are configured. During read operation, the register (04H) is read first and the register (06H) is read last. The crystal calibration reading should be continuous and not be interrupted by any operation.

Certain bit locations within the device register map are designated as Reserved. To ensure proper and predictable operation, bits designated as Reserved must be set with their default values.

7.1 REGISTER MAP

Table 46 depicts the map of all the registers sorted in an ascending order of their addresses.

Table 46: Register List and Map

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
Global Control Registers										
00	ID[7:0] - Device ID 1	ID[7:0]								P 70
01	ID[15:8] - Device ID 2	ID[15:8]								P 71
02	MPU_PIN_STS - MPU_MODE[2:0] Pins Status	-	-	-	-	-	MPU_PIN_STS[2:0]			P 71
04	NOMINAL_FREQ[7:0]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 1	NOMINAL_FREQ_VALUE[7:0]								P 71
05	NOMINAL_FREQ[15:8]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 2	NOMINAL_FREQ_VALUE[15:8]								P 72
06	NOMINAL_FREQ[23:16]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 3	NOMINAL_FREQ_VALUE[23:16]								P 72
07	T4_T0_REG_SEL_CNFG - T0 / T4 Registers Selection Configuration	-	-	-	T4_T0_SEL	-	-	-	-	P 72
08	PHASE_ALARM_TIME_OUT_CNFG - Phase Lock Alarm Time-Out Configuration	MULTI_FACTOR[1:0]			TIME_OUT_VALUE[5:0]					P 73
09	INPUT_MODE_CNFG - Input Mode Configuration	AUTO_EX T_SYNC_ EN	EXT_SYN C_EN	PH_ALAR M_TIMEO UT	SYNC_FREQ[1:0]		IN_SONET _SDH	MASTER_ SLAVE	REVERTIV E_MODE	P 74
0A	DIFFERENTIAL_IN_OUT_OSCI_CNFG - Differential Input / Output Port & Master Clock Configuration	-	-	-	-	OSC_EDG E		OUT7_PE CL_LVDS	OUT6_PE CL_LVDS	P 75

Table 46: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page	
0B	MON_SW_HS_CNFG - Frequency Monitor, Input Clock Selection & HS Control	FREQ_MON_CLK	LOS_FLAG_TO_TDO	ULTR_FAST_SW	EXT_SW	HS_FREZ	HS_EN	-	FREQ_MON_HARDEN	P 76	
13	MS_SL_CTRL_CNFG - Master Slave Control	-	-	-	-	-	-	-	MS_SL_CTRL	P 77	
7E	PROTECTION_CNFG - Register Protection Mode Configuration	PROTECTION_DATA[7:0]								P 77	
7F	MPU_SEL_CNFG - Microprocessor Interface Mode Configuration	-	-	-	-	-	MPU_SEL_CNFG[2:0]			P 78	
Interrupt Registers											
0C	INTERRUPT_CNFG - Interrupt Configuration	-	-	-	-	-	-	HZ_EN	INT_POL	P 79	
0D	INTERRUPTS1_STS - Interrupt Status 1	IN[8:1]								P 79	
0E	INTERRUPTS2_STS - Interrupt Status 2	T0_OPERATING_MODE	T0_MAIN_REF_FAILED	IN[14:9]							P 80
0F	INTERRUPTS3_STS - Interrupt Status 3	EX_SYNC_ALARM	T4_STS	-	INPUT_TO_T4	AMI2_VIOL	AMI2_LOS	AMI1_VIOL	AMI1_LOS	P 81	
10	INTERRUPTS1_ENABLE_CNFG - Interrupt Control 1	IN[8:1]								P 82	
11	INTERRUPTS2_ENABLE_CNFG - Interrupt Control 2	T0_OPERATING_MODE	T0_MAIN_REF_FAILED	IN[14:9]							P 82
12	INTERRUPTS3_ENABLE_CNFG - Interrupt Control 3	EX_SYNC_ALARM	T4_STS	-	INPUT_TO_T4	AMI2_VIOL	AMI2_LOS	AMI1_VIOL	AMI1_LOS	P 83	
Input Clock Frequency & Priority Configuration Registers											
14	IN1_CNFG - Input Clock 1 Configuration	-	400HZ_SE_L	BUCKET_SEL[1:0]		IN_FREQ[3:0]			P 84		
15	IN2_CNFG - Input Clock 2 Configuration	-	400HZ_SE_L	BUCKET_SEL[1:0]		IN_FREQ[3:0]			P 84		
16	IN3_CNFG - Input Clock 3 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]			P 85		
17	IN4_CNFG - Input Clock 4 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]			P 86		
18	IN5_IN6_HF_DIV_CNFG - Input Clock 5 & 6 High Frequency Divider Configuration	IN6_DIV[1:0]		-	-	-	-	IN5_DIV[1:0]		P 87	
19	IN5_CNFG - Input Clock 5 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]			P 88		
1A	IN6_CNFG - Input Clock 6 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]			P 89		
1B	IN7_CNFG - Input Clock 7 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]			P 90		
1C	IN8_CNFG - Input Clock 8 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]			P 91		
1D	IN9_CNFG - Input Clock 9 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]			P 92		
1E	IN10_CNFG - Input Clock 10 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]			P 93		

Table 46: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
1F	IN11_CNFG - Input Clock 11 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 94
20	IN12_CNFG - Input Clock 12 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 95
21	IN13_CNFG - Input Clock 13 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 96
22	IN14_CNFG - Input Clock 14 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 97
23	PRE_DIV_CH_CNFG - DivN Divider Channel Selection	-	-	-	-	PRE_DIV_CH_VALUE[3:0]				P 98
24	PRE_DIVN[7:0]_CNFG - DivN Divider Division Factor Configuration 1	PRE_DIVN_VALUE[7:0]								P 98
25	PRE_DIVN[14:8]_CNFG - DivN Divider Division Factor Configuration 2	-	PRE_DIVN_VALUE[14:8]							P 99
26	IN1_IN2_SEL_PRIORITY_CNFG - Input Clock 1 & 2 Priority Configuration *	IN2_SEL_PRIORITY[3:0]			IN1_SEL_PRIORITY[3:0]					P 100
27	IN3_IN4_SEL_PRIORITY_CNFG - Input Clock 3 & 4 Priority Configuration *	IN4_SEL_PRIORITY[3:0]			IN3_SEL_PRIORITY[3:0]					P 101
28	IN5_IN6_SEL_PRIORITY_CNFG - Input Clock 5 & 6 Priority Configuration *	IN6_SEL_PRIORITY[3:0]			IN5_SEL_PRIORITY[3:0]					P 102
29	IN7_IN8_SEL_PRIORITY_CNFG - Input Clock 7 & 8 Priority Configuration *	IN8_SEL_PRIORITY[3:0]			IN7_SEL_PRIORITY[3:0]					P 103
2A	IN9_IN10_SEL_PRIORITY_CNFG - Input Clock 9 & 10 Priority Configuration *	IN10_SEL_PRIORITY[3:0]			IN9_SEL_PRIORITY[3:0]					P 104
2B	IN11_IN12_SEL_PRIORITY_CNFG - Input Clock 11 & 12 Priority Configuration *	IN12_SEL_PRIORITY[3:0]			IN11_SEL_PRIORITY[3:0]					P 105
2C	IN13_IN14_SEL_PRIORITY_CNFG - Input Clock 13 & 14 Priority Configuration *	IN14_SEL_PRIORITY[3:0]			IN13_SEL_PRIORITY[3:0]					P 106
Input Clock Quality Monitoring Configuration & Status Registers										
2E	FREQ_MON_FACTOR_CNFG - Factor of Frequency Monitor Configuration	-	-	-	-	FREQ_MON_FACTOR[3:0]				P 107
2F	HARD_FREQ_MON_THRESHOLD_CNFG - Frequency Monitor Threshold for Hard Input Clocks Configuration	HARD_FREQ_MON_THRESHOLD[7:4]			HARD_FREQ_MON_THRESHOLD[3:0]					P 108
30	SOFT_FREQ_MON_THRESHOLD_CNFG - Frequency Monitor Threshold for Soft Input Clocks Configuration	SOFT_FREQ_MON_THRESHOLD[7:4]			SOFT_FREQ_MON_THRESHOLD[3:0]					P 108
31	UPPER_THRESHOLD_0_CNFG - Upper Threshold for Leaky Bucket Configuration 0	UPPER_THRESHOLD_0_DATA[7:0]								P 109
32	LOWER_THRESHOLD_0_CNFG - Lower Threshold for Leaky Bucket Configuration 0	LOWER_THRESHOLD_0_DATA[7:0]								P 109

Table 46: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
33	BUCKET_SIZE_0_CNFG - Bucket Size for Leaky Bucket Configuration 0	BUCKET_SIZE_0_DATA[7:0]								P 109
34	DECAY_RATE_0_CNFG - Decay Rate for Leaky Bucket Configuration 0	-	-	-	-	-	-	DECAY_RATE_0_DATA [1:0]		P 110
35	UPPER_THRESHOLD_1_CNFG - Upper Threshold for Leaky Bucket Configuration 1	UPPER_THRESHOLD_1_DATA[7:0]								P 110
36	LOWER_THRESHOLD_1_CNFG - Lower Threshold for Leaky Bucket Configuration 1	LOWER_THRESHOLD_1_DATA[7:0]								P 110
37	BUCKET_SIZE_1_CNFG - Bucket Size for Leaky Bucket Configuration 1	BUCKET_SIZE_1_DATA[7:0]								P 111
38	DECAY_RATE_1_CNFG - Decay Rate for Leaky Bucket Configuration 1	-	-	-	-	-	-	DECAY_RATE_1_DATA [1:0]		P 111
39	UPPER_THRESHOLD_2_CNFG - Upper Threshold for Leaky Bucket Configuration 2	UPPER_THRESHOLD_2_DATA[7:0]								P 111
3A	LOWER_THRESHOLD_2_CNFG - Lower Threshold for Leaky Bucket Configuration 2	LOWER_THRESHOLD_2_DATA[7:0]								P 112
3B	BUCKET_SIZE_2_CNFG - Bucket Size for Leaky Bucket Configuration 2	BUCKET_SIZE_2_DATA[7:0]								P 112
3C	DECAY_RATE_2_CNFG - Decay Rate for Leaky Bucket Configuration 2	-	-	-	-	-	-	DECAY_RATE_2_DATA [1:0]		P 112
3D	UPPER_THRESHOLD_3_CNFG - Upper Threshold for Leaky Bucket Configuration 3	UPPER_THRESHOLD_3_DATA[7:0]								P 113
3E	LOWER_THRESHOLD_3_CNFG - Lower Threshold for Leaky Bucket Configuration 3	LOWER_THRESHOLD_3_DATA[7:0]								P 113
3F	BUCKET_SIZE_3_CNFG - Bucket Size for Leaky Bucket Configuration 3	BUCKET_SIZE_3_DATA[7:0]								P 113
40	DECAY_RATE_3_CNFG - Decay Rate for Leaky Bucket Configuration 3	-	-	-	-	-	-	DECAY_RATE_3_DATA [1:0]		P 114
41	IN_FREQ_READ_CH_CNFG - Input Clock Frequency Read Channel Selection	-	-	-	-	IN_FREQ_READ_CH[3:0]				P 114
42	IN_FREQ_READ_STS - Input Clock Frequency Read Value	IN_FREQ_VALUE[7:0]								P 115
43	IN1_IN2_STS - Input Clock 1 & 2 Status	IN2_FREQ_SOFT_ALARM	IN2_FREQ_HARD_ALARM	IN2_NO_ACTIVITY_ALARM	IN2_PH_LOCK_ALARM	IN1_FREQ_SOFT_ALARM	IN1_FREQ_HARD_ALARM	IN1_NO_ACTIVITY_ALARM	IN1_PH_LOCK_ALARM	P 116
44	IN3_IN4_STS - Input Clock 3 & 4 Status	IN4_FREQ_SOFT_ALARM	IN4_FREQ_HARD_ALARM	IN4_NO_ACTIVITY_ALARM	IN4_PH_LOCK_ALARM	IN3_FREQ_SOFT_ALARM	IN3_FREQ_HARD_ALARM	IN3_NO_ACTIVITY_ALARM	IN3_PH_LOCK_ALARM	P 117
45	IN5_IN6_STS - Input Clock 5 & 6 Status	IN6_FREQ_SOFT_ALARM	IN6_FREQ_HARD_ALARM	IN6_NO_ACTIVITY_ALARM	IN6_PH_LOCK_ALARM	IN5_FREQ_SOFT_ALARM	IN5_FREQ_HARD_ALARM	IN5_NO_ACTIVITY_ALARM	IN5_PH_LOCK_ALARM	P 118
46	IN7_IN8_STS - Input Clock 7 & 8 Status	IN8_FREQ_SOFT_ALARM	IN8_FREQ_HARD_ALARM	IN8_NO_ACTIVITY_ALARM	IN8_PH_LOCK_ALARM	IN7_FREQ_SOFT_ALARM	IN7_FREQ_HARD_ALARM	IN7_NO_ACTIVITY_ALARM	IN7_PH_LOCK_ALARM	P 119

Table 46: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
47	IN9_IN10_STS - Input Clock 9 & 10 Status	IN10_FREQ_SOFT_ALARM	IN10_FREQ_HARD_ALARM	IN10_NO_ACTIVITY_ALARM	IN10_PHASE_LOCK_ARM	IN9_FREQ_SOFT_ALARM	IN9_FREQ_HARD_ALARM	IN9_NO_ACTIVITY_ALARM	IN9_PHASE_LOCK_ARM	P 120
48	IN11_IN12_STS - Input Clock 11 & 12 Status	IN12_FREQ_SOFT_ALARM	IN12_FREQ_HARD_ALARM	IN12_NO_ACTIVITY_ALARM	IN12_PHASE_LOCK_ARM	IN11_FREQ_SOFT_ALARM	IN11_FREQ_HARD_ALARM	IN11_NO_ACTIVITY_ALARM	IN11_PHASE_LOCK_ARM	P 121
49	IN13_IN14_STS - Input Clock 13 & 14 Status	IN14_FREQ_SOFT_ALARM	IN14_FREQ_HARD_ALARM	IN14_NO_ACTIVITY_ALARM	IN14_PHASE_LOCK_ALARM	IN13_FREQ_SOFT_ALARM	IN13_FREQ_HARD_ALARM	IN13_NO_ACTIVITY_ALARM	IN13_PHASE_LOCK_ALARM	P 122
T0 / T4 DPLL Input Clock Selection Registers										
4A	INPUT_VALID1_STS - Input Clocks Validity 1	IN[8:1]								P 123
4B	INPUT_VALID2_STS - Input Clocks Validity 2	-	-	IN[14:9]						P 123
4C	REMOTE_INPUT_VALID1_CNFG - Input Clocks Validity Configuration 1	IN8_VALID	IN7_VALID	IN6_VALID	IN5_VALID	IN4_VALID	IN3_VALID	IN2_VALID	IN1_VALID	P 123
4D	REMOTE_INPUT_VALID2_CNFG - Input Clocks Validity Configuration 2	-	-	IN14_VALID	IN13_VALID	IN12_VALID	IN11_VALID	IN10_VALID	IN9_VALID	P 124
4E	PRIORITY_TABLE1_STS - Priority Status 1 *	HIGHEST_PRIORITY_VALIDATED[3:0]				CURRENTLY_SELECTED_INPUT[3:0]				P 124
4F	PRIORITY_TABLE2_STS - Priority Status 2 *	THIRD_HIGHEST_PRIORITY_VALIDATED[3:0]				SECOND_HIGHEST_PRIORITY_VALIDATED[3:0]				P 125
50	T0_INPUT_SEL_CNFG - T0 Selected Input Clock Configuration	-	-	-	-	T0_INPUT_SEL[3:0]				P 125
51	T4_INPUT_SEL_CNFG - T4 Selected Input Clock Configuration	-	T4_LOCK_T0	T0_FOR_T4	T4_TEST_T0_PH	T4_INPUT_SEL[3:0]				P 126
T0 / T4 DPLL State Machine Control Registers										
52	OPERATING_STS - DPLL Operating Status	EX_SYNC_ALARM_MON	T4_DPLL_LOCK	T0_DPLL_SOFT_FR_EQ_ALARM	T4_DPLL_SOFT_FR_EQ_ALARM	T0_DPLL_LOCK	T0_DPLL_OPERATING_MODE[2:0]			P 127
53	T0_OPERATING_MODE_CNFG - T0 DPLL Operating Mode Configuration	-	-	-	-	-	T0_OPERATING_MODE[2:0]			P 128
54	T4_OPERATING_MODE_CNFG - T4 DPLL Operating Mode Configuration	-	-	-	-	-	T4_OPERATING_MODE[2:0]			P 128
T0 / T4 DPLL & APLL Configuration Registers										
55	T0_DPLL_APLL_PATH_CNFG - T0 DPLL & APLL Path Configuration	T0_APLL_PATH[3:0]				T0_GSM_OBSAI_16E1_16T1_SEL[1:0]		T0_12E1_24T1_E3_T3_SEL[1:0]		P 129
56	T0_DPLL_START_BW_DAMPING_CNFG - T0 DPLL Start Bandwidth & Damping Factor Configuration	T0_DPLL_START_DAMPING[2:0]			T0_DPLL_START_BW[4:0]					P 130
57	T0_DPLL_ACQ_BW_DAMPING_CNFG - T0 DPLL Acquisition Bandwidth & Damping Factor Configuration	T0_DPLL_ACQ_DAMPING[2:0]			T0_DPLL_ACQ_BW[4:0]					P 131
58	T0_DPLL_LOCKED_BW_DAMPING_CNFG - T0 DPLL Locked Bandwidth & Damping Factor Configuration	T0_DPLL_LOCKED_DAMPING[2:0]			T0_DPLL_LOCKED_BW[4:0]					P 132
59	T0_BW_OVERSHOOT_CNFG - T0 DPLL Bandwidth Overshoot Configuration	AUTO_BW_SEL	-	-	-	T0_LIMIT	-	-	-	P 133

Table 46: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page	
5A	PHASE_LOSS_COARSE_LIMIT_CNFG - Phase Loss Coarse Detector Limit Configuration *	COARSE_PH_LOS_LIMT_EN	WIDE_EN	MULTI_PH_APP	MULTI_PH_8K_4K_2K_EN	PH_LOS_COARSE_LIMT[3:0]				P 134	
5B	PHASE_LOSS_FINE_LIMIT_CNFG - Phase Loss Fine Detector Limit Configuration *	FINE_PH_LOS_LIMT_EN	FAST_LOS_SW	-	-	-	PH_LOS_FINE_LIMT[2:0]			P 135	
5C	T0_HOLDOVER_MODE_CNFG - T0 DPLL Holdover Mode Configuration	MAN_HOLDOVER	AUTO_AVG	FAST_AVG	READ_AVG	TEMP_HOLDOVER_MODE[1:0]		-	-	P 136	
5D	T0_HOLDOVER_FREQ[7:0]_CNFG - T0 DPLL Holdover Frequency Configuration 1	T0_HOLDOVER_FREQ[7:0]								P 136	
5E	T0_HOLDOVER_FREQ[15:8]_CNFG - T0 DPLL Holdover Frequency Configuration 2	T0_HOLDOVER_FREQ[15:8]								P 137	
5F	T0_HOLDOVER_FREQ[23:16]_CNFG - T0 DPLL Holdover Frequency Configuration 3	T0_HOLDOVER_FREQ[23:16]								P 137	
60	T4_DPLL_APLL_PATH_CNFG - T4 DPLL & APLL Path Configuration	T4_APLL_PATH[3:0]			T4_GSM_GPS_16E1_1_6T1_SEL[1:0]		T4_12E1_24T1_E3_T3_SEL[1:0]			P 138	
61	T4_DPLL_LOCKED_BW_DAMPING_CNFG - T4 DPLL Locked Bandwidth & Damping Factor Configuration	T4_DPLL_LOCKED_DAMPING[2:0]		-	-	-	T4_DPLL_LOCKED_BW[1:0]			P 139	
62	CURRENT_DPLL_FREQ[7:0]_STS - DPLL Current Frequency Status 1 *	CURRENT_DPLL_FREQ[7:0]								P 139	
63	CURRENT_DPLL_FREQ[15:8]_STS - DPLL Current Frequency Status 2 *	CURRENT_DPLL_FREQ[15:8]								P 139	
64	CURRENT_DPLL_FREQ[23:16]_STS - DPLL Current Frequency Status 3 *	CURRENT_DPLL_FREQ[23:16]								P 140	
65	DPLL_FREQ_SOFT_LIMIT_CNFG - DPLL Soft Limit Configuration	FREQ_LIMT_PH_LOS	DPLL_FREQ_SOFT_LIMT[6:0]								P 140
66	DPLL_FREQ_HARD_LIMIT[7:0]_CNFG - DPLL Hard Limit Configuration 1	DPLL_FREQ_HARD_LIMT[7:0]								P 140	
67	DPLL_FREQ_HARD_LIMIT[15:8]_CNFG - DPLL Hard Limit Configuration 2	DPLL_FREQ_HARD_LIMT[15:8]								P 141	
68	CURRENT_DPLL_PHASE[7:0]_STS - DPLL Current Phase Status 1 *	CURRENT_PH_DATA[7:0]								P 141	
69	CURRENT_DPLL_PHASE[15:8]_STS - DPLL Current Phase Status 2 *	CURRENT_PH_DATA[15:8]								P 141	
6A	T0_T4_APLL_BW_CNFG - T0 / T4 APLL Bandwidth Configuration	-	-	T0_APLL_BW[2:0]		T4_APLL_BW[2:0]				P 142	
Output Configuration Registers											
6B	OUT1_FREQ_CNFG - Output Clock 1 Frequency Configuration	OUT1_PATH_SEL[3:0]			OUT1_DIVIDER[3:0]						P 143
6C	OUT2_FREQ_CNFG - Output Clock 2 Frequency Configuration	OUT2_PATH_SEL[3:0]			OUT2_DIVIDER[3:0]						P 144
6D	OUT3_FREQ_CNFG - Output Clock 3 Frequency Configuration	OUT3_PATH_SEL[3:0]			OUT3_DIVIDER[3:0]						P 145
6E	OUT4_FREQ_CNFG - Output Clock 4 Frequency Configuration	OUT4_PATH_SEL[3:0]			OUT4_DIVIDER[3:0]						P 146

Table 46: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
6F	OUT5_FREQ_CNFG - Output Clock 5 Frequency Configuration	OUT5_PATH_SEL[3:0]			OUT5_DIVIDER[3:0]					P 147
70	OUT6_FREQ_CNFG - Output Clock 6 Frequency Configuration	OUT6_PATH_SEL[3:0]			OUT6_DIVIDER[3:0]					P 148
71	OUT7_FREQ_CNFG - Output Clock 7 Frequency Configuration	OUT7_PATH_SEL[3:0]			OUT7_DIVIDER[3:0]					P 149
72	OUT8_FREQ_CNFG - Output Clock 8 Frequency Configuration & Output Clock 6, 7 & 9 Invert Configuration	OUT8_PAT_H_SEL	OUT8_EN	T4_INPUT_FAIL	AMI_OUT_DUTY	400HZ_SE L	OUT9_INV	OUT7_INV	OUT6_INV	P 150
73	OUT9_FREQ_CNFG - Output Clock 9 Frequency Configuration & Output Clock 1 ~ 5 Invert Configuration	OUT9_PAT_H_SEL	OUT9_EN	T4_INPUT_FAIL	OUT5_INV	OUT4_INV	OUT3_INV	OUT2_INV	OUT1_INV	P 151
74	FR_MFR_SYNC_CNFG - Frame Sync & Multiframe Sync Output Configuration	IN_2K_4K_8K_INV	8K_EN	2K_EN	2K_8K_PU L_POSITI ON	8K_INV	8K_PUL	2K_INV	2K_PUL	P 152
Phase Offset Control Registers										
78	PHASE_MON_CNFG - Phase Transient Monitor Configuration	IN_NOISE_WINDOW	-	-	-	-				P 154
7A	PHASE_OFFSET[7:0]_CNFG - Phase Offset Configuration 1	PH_OFFSET[7:0]								P 154
7B	PHASE_OFFSET[9:8]_CNFG - Phase Offset Configuration 2	PH_OFFSET_EN	-	-	-	-	-	PH_OFFSET[9:8]		P 154
Synchronization Configuration Registers										
7C	SYNC_MONITOR_CNFG - Sync Monitor Configuration	-	SYNC_MON_LIMT[2:0]		-	-	-	-		P 155
7D	SYNC_PHASE_CNFG - Sync Phase Configuration	-	-	-	-	-	-	SYNC_PH1[1:0]		P 155

7.2 REGISTER DESCRIPTION

7.2.1 GLOBAL CONTROL REGISTERS

ID[7:0] - Device ID 1

Address: 00H																										
Type: Read																										
Default Value: 10010000																										
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 12.5%; text-align: center;">7</td> <td style="width: 12.5%; text-align: center;">6</td> <td style="width: 12.5%; text-align: center;">5</td> <td style="width: 12.5%; text-align: center;">4</td> <td style="width: 12.5%; text-align: center;">3</td> <td style="width: 12.5%; text-align: center;">2</td> <td style="width: 12.5%; text-align: center;">1</td> <td style="width: 12.5%; text-align: center;">0</td> </tr> <tr> <td style="text-align: center;">ID7</td> <td style="text-align: center;">ID6</td> <td style="text-align: center;">ID5</td> <td style="text-align: center;">ID4</td> <td style="text-align: center;">ID3</td> <td style="text-align: center;">ID2</td> <td style="text-align: center;">ID1</td> <td style="text-align: center;">ID0</td> </tr> </table>											7	6	5	4	3	2	1	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
7	6	5	4	3	2	1	0																			
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0																			
Bit	Name	Description																								
7 - 0	ID[7:0]	Refer to the description of the ID[15:8] bits (b7~0, 01H).																								

ID[15:8] - Device ID 2

Address: 01H Type: Read Default Value: 00110011							
7	6	5	4	3	2	1	0
ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
Bit	Name	Description					
7 - 0	ID[15:8]	The value in the ID[15:0] bits are pre-set, representing the identification number for the IDT82V3390.					

MPU_PIN_STS - MPU_MODE[2:0] Pins Status

Address: 02H Type: Read Default Value: XXXXXXXX							
7	6	5	4	3	2	1	0
-	-	-	-	-	MPU_PIN_STS2	MPU_PIN_STS1	MPU_PIN_STS0
Bit	Name	Description					
7 - 3	-	Reserved.					
2 - 0	MPU_PIN_STS[2:0]	These bits indicate the value of the MPU_MODE[2:0] pins. The default value of these bits is determined by the MPU_MODE[2:0] pins during reset. 000: Reserved 001: EPROM mode 010: Multiplexed mode 011: Intel mode 100: Motorola mode 101: Serial mode 110: I2C mode 111: Serial mode					

NOMINAL_FREQ[7:0]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 1

Address: 04H Type: Read / Write Default Value: 00000000							
7	6	5	4	3	2	1	0
NOMINAL_FREQ_VALUE7	NOMINAL_FREQ_VALUE6	NOMINAL_FREQ_VALUE5	NOMINAL_FREQ_VALUE4	NOMINAL_FREQ_VALUE3	NOMINAL_FREQ_VALUE2	NOMINAL_FREQ_VALUE1	NOMINAL_FREQ_VALUE0
Bit	Name	Description					
7 - 0	NOMINAL_FREQ_VALUE[7:0]	Refer to the description of the NOMINAL_FREQ_VALUE[23:16] bits (b7~0, 06H).					

NOMINAL_FREQ[15:8]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 2

Address: 05H Type: Read / Write Default Value: 00000000							
7	6	5	4	3	2	1	0
NOMINAL_FREQ_VALUE15	NOMINAL_FREQ_VALUE14	NOMINAL_FREQ_VALUE13	NOMINAL_FREQ_VALUE12	NOMINAL_FREQ_VALUE11	NOMINAL_FREQ_VALUE10	NOMINAL_FREQ_VALUE9	NOMINAL_FREQ_VALUE8
Bit	Name	Description					
7 - 0	NOMINAL_FREQ_VALUE[15:8]	Refer to the description of the NOMINAL_FREQ_VALUE[23:16] bits (b7~0, 06H).					

NOMINAL_FREQ[23:16]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 3

Address: 06H Type: Read / Write Default Value: 00000000							
7	6	5	4	3	2	1	0
NOMINAL_FREQ_VALUE23	NOMINAL_FREQ_VALUE22	NOMINAL_FREQ_VALUE21	NOMINAL_FREQ_VALUE20	NOMINAL_FREQ_VALUE19	NOMINAL_FREQ_VALUE18	NOMINAL_FREQ_VALUE17	NOMINAL_FREQ_VALUE16
Bit	Name	Description					
7 - 0	NOMINAL_FREQ_VALUE[23:16]	<p>The NOMINAL_FREQ_VALUE[23:0] bits represent a 2's complement signed integer. The calibration value for the master clock in ppm is obtained by multiplying this register value by 0.0000884.</p> <p>For example, the frequency offset on OSC1 is +3 ppm. Although -3 ppm should be compensated, the calibration value is calculated as +3 ppm:</p> $3 \div 0.0000884 = 33937 \text{ (Dec.)} = 8490 \text{ (Hex);}$ <p>So '008490' should be written into these bits.</p> <p>The calibration range is within ± 741 ppm.</p>					

T4_T0_REG_SEL_CNFG - T0 / T4 Registers Selection Configuration

Address: 07H Type: Read / Write Default Value: XXX0XXXX							
7	6	5	4	3	2	1	0
-	-	-	T4_T0_SEL	-	-	-	-
Bit	Name	Description					
7 - 5	-	Reserved.					
4	T4_T0_SEL	<p>A part of the registers are shared by T0 and T4 paths. These registers are addressed 26H ~ 2CH, 4EH, 4FH, 5AH, 5BH, 62H ~ 64H, 68H and 69H. This bit determines whether the register configuration is available for T0 or T4 path.</p> <p>0: T0 path (default). 1: T4 path.</p>					
3 - 0	-	Reserved.					

PHASE_ALARM_TIME_OUT_CNFG - Phase Lock Alarm Time-Out Configuration

Address: 08H							
Type: Read / Write							
Default Value: 00110010							
7	6	5	4	3	2	1	0
MULTI_FACTO R1	MULTI_FACTO R0	TIME_OUT_VA LUE5	TIME_OUT_VA LUE4	TIME_OUT_VA LUE3	TIME_OUT_VA LUE2	TIME_OUT_VA LUE1	TIME_OUT_VAL UE0
Bit	Name	Description					
7 - 6	MULTI_FACTOR[1:0]	<p>These bits determine a factor which has a relationship with a period in seconds. A phase lock alarm will be raised if the T0 selected input clock is not locked in T0 DPLL within this period. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', the phase lock alarm will be cleared after this period (starting from when the alarm is raised). Refer to the description of the TIME_OUT_VALUE[5:0] bits (b5~0, 08H).</p> <p>00: 2 (default) 01: 4 10: 8 11: 16</p>					
5 - 0	TIME_OUT_VALUE[5:0]	<p>These bits represent an unsigned integer. The value of these bits multiplied by the value in the MULTI_FACTOR[1:0] bits (b7~6, 08H) is equal to the period in seconds.</p> <p>A phase lock alarm will be raised if the T0 selected input clock is not locked in T0 DPLL within this period. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', the phase lock alarm will be cleared after this period (starting from when the alarm is raised).</p>					

INPUT_MODE_CNFG - Input Mode Configuration

Address: 09H																			
Type: Read / Write																			
Default Value: 10100XX0																			
7	6	5	4	3	2	1	0												
AUTO_EXT_SYNC_EN	EXT_SYNC_EN	PH_ALARM_TIMEOUT	SYNC_FREQ1	SYNC_FREQ0	IN_SONET_SDH	MASTER_SLAVE	REVERTIVE_MODE												
Bit	Name	Description																	
7	AUTO_EXT_SYNC_EN	Refer to the description of the EXT_SYNC_EN bit (b6, 09H).																	
6	EXT_SYNC_EN	<p>This bit, together with the AUTO_EXT_SYNC_EN bit (b7, 09H), determines whether EX_SYNC1 is enabled to synchronize the frame sync output signals.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>AUTO_EXT_SYNC_EN</th> <th>EXT_SYNC_EN</th> <th>Synchronization</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">don't-care</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Disabled (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Enabled</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Enabled if the T0 selected input clock is IN11; otherwise, disabled.</td> </tr> </tbody> </table>						AUTO_EXT_SYNC_EN	EXT_SYNC_EN	Synchronization	don't-care	0	Disabled (default)	0	1	Enabled	1	1	Enabled if the T0 selected input clock is IN11; otherwise, disabled.
AUTO_EXT_SYNC_EN	EXT_SYNC_EN	Synchronization																	
don't-care	0	Disabled (default)																	
0	1	Enabled																	
1	1	Enabled if the T0 selected input clock is IN11; otherwise, disabled.																	
5	PH_ALARM_TIMEOUT	<p>This bit determines how to clear the phase lock alarm.</p> <p>0: The phase lock alarm will be cleared when a '1' is written to the corresponding INn_PH_LOCK_ALARM bit (b4/0, 43H~49H).</p> <p>1: The phase lock alarm will be cleared after a period (= $TIME_OUT_VALUE[5:0] (b5-0, 08H) \times MULTI_FACTOR[1:0] (b7-6, 08H)$ in second) which starts from when the alarm is raised. (default)</p>																	
4 - 3	SYNC_FREQ[1:0]	<p>These bits set the frequency of the frame sync signal input on the EX_SYNC1 pin.</p> <p>00: 8 kHz (default)</p> <p>01: 8 kHz.</p> <p>10: 4 kHz.</p> <p>11: 2 kHz.</p>																	
2	IN_SONET_SDH	<p>This bit selects the SDH or SONET network type.</p> <p>0: SDH. The DPLL required clock is 2.048 MHz when the IN_FREQ[3:0] bits (b3~0, 14H~17H & 19H~22H) are '0001'; the T0/T4 DPLL output from the 16E1/16T1 path is 16E1; and OUT9 outputs a 2.048 MHz signal if enabled.</p> <p>1: SONET. The DPLL required clock is 1.544 MHz when the IN_FREQ[3:0] bits (b3~0, 14H~17H & 19H~22H) are '0001'; the T0/T4 DPLL output from the 16E1/16T1 path is 16T1; and OUT9 outputs a 1.544 MHz signal if enabled.</p> <p>The default value of this bit is determined by the SONET/SDH pin during reset.</p>																	
1	MASTER_SLAVE	<p>This bit is read only. It indicates the value of the MS/SL pin.</p> <p>Its default value is determined by the MS/SL pin during reset.</p>																	
0	REVERTIVE_MODE	<p>This bit selects Revertive or Non-Revertive switching for T0 path.</p> <p>0: Non-Revertive switching. (default)</p> <p>1: Revertive switching.</p>																	

DIFFERENTIAL_IN_OUT_OSCI_CNFG - Differential Input / Output Port & Master Clock Configuration

Address: 0AH							
Type: Read / Write							
Default Value: XXXXX001							
7	6	5	4	3	2	1	0
-	-	-	-	-	OSC_EDGE	OUT7_PECL_LVDS	OUT6_PECL_LVDS
Bit	Name	Description					
7 - 3	-	Reserved.					
2	OSC_EDGE	This bit selects a better active edge of the master clock. 0: The rising edge. (default) 1: The falling edge.					
1	OUT7_PECL_LVDS	This bit selects a port technology for OUT7. 0: LVDS. (default) 1: PECL.					
0	OUT6_PECL_LVDS	This bit selects a port technology for OUT6. 0: LVDS. 1: PECL. (default)					

MON_SW_HS_CNFG - Frequency Monitor, Input Clock Selection & HS Control

Address: 0BH							
Type: Read / Write							
Default Value: 100X01X1							
7	6	5	4	3	2	1	0
FREQ_MON_CLK	LOS_FLAG_TO_TDO	ULTR_FAST_SW	EXT_SW	HS_FREZ	HS_EN	-	FREQ_MON_HARD_EN
Bit	Name	Description					
7	FREQ_MON_CLK	The bit selects a reference clock for input clock frequency monitoring. 0: The output of T0 DPLL. 1: The master clock. (default)					
6	LOS_FLAG_TO_TDO	The bit determines whether the interrupt of T0 selected input clock fail - is reported by the TDO pin. 0: Not reported. TDO pin is used as JTAG test data output which complies with IEEE 1149.1. (default) 1: Reported. TDO pin mimics the state of the T0_MAIN_REF_FAILED bit (b6, 0EH) and does not strictly comply with IEEE 1149.1.					
5	ULTR_FAST_SW	This bit determines whether the T0 selected input clock is valid when missing 2 consecutive clock cycles or more. 0: Valid. (default) 1: Invalid.					
4	EXT_SW	This bit determines the T0 input clock selection. 0: Forced selection or Automatic selection, as controlled by the T0_INPUT_SEL[3:0] bits (b3~0, 50H). 1: External Fast selection. The default value of this bit is determined by the FF_SRCSW pin during reset.					
3	HS_FREZ	This bit is valid only when the HS is enabled by the HS_EN bit (b2, 0BH). It determines whether HS is frozen at the current phase offset when a HS event is triggered. 0: Not frozen. (default) 1: Frozen. Further HS events are ignored and the current phase offset is maintained.					
2	HS_EN	This bit determines whether HS is enabled when the T0 selected input clock switch or the T0 DPLL exiting from Holdover mode or Free-Run mode occurs. 0: Disabled. 1: Enabled. (default)					
1	-	Reserved.					
0	FREQ_MON_HARD_EN	This bit determines whether the frequency hard alarm is enabled when the frequency of the input clock with respect to the reference clock is above the frequency hard alarm threshold. The reference clock can be the output of T0 DPLL or the master clock, as determined by the FREQ_MON_CLK bit (b7, 0BH). 0: Disabled. 1: Enabled. (default)					

MS_SL_CTRL_CNFG - Master Slave Control

Address: 13H
 Type: Read / Write
 Default Value: 00001xx00

7	6	5	4	3	2	1	0
APLL	APLL	APLL	APLL	APLL	-	-	MS_SL_CTRL

Bit	Name	Description															
7-3	APLL Settings	For best jitter performance, the following bits in the MS_SL_CTRL_CNFG, T0_T4_APLL_BW_CNFG and APLL_CNFG registers must be set. Bit 7 to Bit 3 of MS_SL_CTRL_CNFG register (address 13H) must be set to 01010. Bit 6 to Bit 0 of T0_T4_APLL_BW_CNFG (address 6AH) must be set to 1010010. Bit 7 of APLL_CNFG (address 77H) must be set to 0.															
2-1	-	Reserved.															
0	MS_SL_CTRL	These bits, together with the MS/SL pin, control whether the device is configured as the Master or as the Slave. <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th colspan="2">Master/Slave Control</th> <th rowspan="2">Result</th> </tr> <tr> <th>MS/SL pin</th> <th>MS_SL_CTRL Bit</th> </tr> </thead> <tbody> <tr> <td rowspan="2" style="text-align:center;">High</td> <td style="text-align:center;">0</td> <td style="text-align:center;">Master</td> </tr> <tr> <td style="text-align:center;">1</td> <td style="text-align:center;">Slave</td> </tr> <tr> <td rowspan="2" style="text-align:center;">Low</td> <td style="text-align:center;">0</td> <td style="text-align:center;">Slave</td> </tr> <tr> <td style="text-align:center;">1</td> <td style="text-align:center;">Master</td> </tr> </tbody> </table> The default value of this bit is '0'.	Master/Slave Control		Result	MS/SL pin	MS_SL_CTRL Bit	High	0	Master	1	Slave	Low	0	Slave	1	Master
Master/Slave Control		Result															
MS/SL pin	MS_SL_CTRL Bit																
High	0	Master															
	1	Slave															
Low	0	Slave															
	1	Master															

PROTECTION_CNFG - Register Protection Mode Configuration

Address: 7EH
 Type: Read / Write
 Default Value: 10000101

7	6	5	4	3	2	1	0
PROTECTION_DATA7	PROTECTION_DATA6	PROTECTION_DATA5	PROTECTION_DATA4	PROTECTION_DATA3	PROTECTION_DATA2	PROTECTION_DATA1	PROTECTION_DATA0

Bit	Name	Description
7 - 0	PROTECTION_DATA[7:0]	These bits select a register write protection mode. 00000000 - 10000100, 10000111 - 11111111: Protected mode. No other registers can be written except this register. 10000101: Fully Unprotected mode. All the writable registers can be written. (default) 10000110: Single Unprotected mode. One more register can be written besides this register. After write operation (not including writing a '1' to clear the bit to '0'), the device automatically switches to Protected mode.

MPU_SEL_CNFG - Microprocessor Interface Mode Configuration

Address: 7FH							
Type: Read / Write							
Default Value: XXXXXXXX							
7	6	5	4	3	2	1	0
-	-	-	-	-	MPU_SEL_CNFG2	MPU_SEL_CNFG1	MPU_SEL_CNFG0
Bit	Name	Description					
7 - 3	-	Reserved.					
2 - 0	MPU_SEL_CNFG[2:0]	These bits select a microprocessor interface mode: 000: Reserved. 001: EPROM mode. 010: Multiplexed mode. 011: Intel mode. 100: Motorola mode. 101: Serial mode. 110: I2C mode. 111: Serial mode. The default value of these bits are determined by the MPU_MODE[2:0] pins during reset.					

7.2.2 INTERRUPT REGISTERS

INTERRUPT_CNFG - Interrupt Configuration

Address: 0CH							
Type: Read / Write							
Default Value: XXXXXX10							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	HZ_EN	INT_POL
Bit	Name	Description					
7 - 2	-	Reserved.					
1	HZ_EN	This bit determines the output characteristics of the INT_REQ pin. 0: The output on the INT_REQ pin is high/low when the interrupt is active; the output is the opposite when the interrupt is inactive. 1: The output on the INT_REQ pin is high/low when the interrupt is active; the output is in high impedance state when the interrupt is inactive. (default)					
0	INT_POL	This bit determines the active level on the INT_REQ pin for an active interrupt indication. 0: Active low. (default) 1: Active high.					

INTERRUPTS1_STS - Interrupt Status 1

Address: 0DH							
Type: Read / Write							
Default Value: 11111111							
7	6	5	4	3	2	1	0
IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1
Bit	Name	Description					
7 - 0	INn	This bit indicates the validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid') for the corresponding INn; i.e., whether there is a transition (from '0' to '1' or from '1' to '0') on the corresponding INn bit (b7~0, 4AH). Here n is any one of 8 to 1. 0: Has not changed. 1: Has changed. (default) This bit is cleared by writing a '1'.					

INTERRUPTS2_STS - Interrupt Status 2

Address: 0EH							
Type: Read / Write							
Default Value: 00111111							
7	6	5	4	3	2	1	0
T0_OPERATING_MODE	T0_MAIN_REF_FAILED	IN14	IN13	IN12	IN11	IN10	IN9
Bit	Name	Description					
7	T0_OPERATING_MODE	This bit indicates the operating mode switch for T0 DPLL; i.e., whether the value in the T0_DPLL_OPERATING_MODE[2:0] bits (b2~0, 52H) changes. 0: Has not switched. (default) 1: Has switched. This bit is cleared by writing a '1'.					
6	T0_MAIN_REF_FAILED	This bit indicates whether the T0 selected input clock has failed. The T0 selected input clock fails when its validity changes from 'valid' to 'invalid'; i.e., when there is a transition from '1' to '0' on the corresponding INn bit (4AH, 4BH). 0: Has not failed. (default) 1: Has failed. This bit is cleared by writing a '1'.					
5 - 0	INn	This bit indicates the validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid') for the corresponding INn for T0 path, i.e., whether there is a transition (from '0' to '1' or from '1' to '0') on the corresponding INn bit (b5~0, 4BH). Here n is any one of 14 to 9. 0: Has not changed. 1: Has changed. (default) This bit is cleared by writing a '1'.					

INTERRUPTS3_STS - Interrupt Status 3

Address: 0FH							
Type: Read / Write							
Default Value: 11X10000							
7	6	5	4	3	2	1	0
EX_SYNC_ALARM	T4_STS	-	INPUT_TO_T4	AMI2_VIOL	AMI2_LOS	AMI1_VIOL	AMI1_LOS
Bit	Name	Description					
7	EX_SYNC_ALARM	This bit indicates whether an external sync alarm is raised; i.e., whether there is a transition from '0' to '1' on the EX_SYNC_ALARM_MON bit (b7, 52H). 0: Has not occurred. 1: Has occurred. (default) This bit is cleared by writing a '1'.					
6	T4_STS	This bit indicates the T4 DPLL locking status changes (from 'locked' to 'unlocked' or from 'unlocked' to 'locked'); i.e., whether there is a transition (from '0' to '1' or from '1' to '0') on the T4_DPLL_LOCK bit (b6, 52H). 0: Has not changed. 1: Has changed. (default) This bit is cleared by writing a '1'.					
5	-	Reserved.					
4	INPUT_TO_T4	This bit indicates whether all the input clocks for T4 path changes to be unqualified; i.e., whether the HIGHEST_PRIORITY_VALIDATED[3:0] bits (b7~4, 4EH) are set to '0000' when these bits are available for T4 path. 0: Has not changed. 1: Has changed. (default) This bit is cleared by writing a '1'.					
3	AMI2_VIOL	This bit indicates whether IN2 has an AMI violation. 0: Has no AMI violation. (default) 1: Has an AMI violation. This bit is cleared by writing a '1'.					
2	AMI2_LOS	This bit indicates whether IN2 has a LOS error. 0: Has no LOS error. (default) 1: Has a LOS error. This bit is cleared by writing a '1'.					
1	AMI1_VIOL	This bit indicates whether IN1 has an AMI violation. 0: Has no AMI violation. (default) 1: Has an AMI violation. This bit is cleared by writing a '1'.					
0	AMI1_LOS	This bit indicates whether IN1 has a LOS error. 0: Has no LOS error. (default) 1: Has a LOS error. This bit is cleared by writing a '1'.					

INTERRUPTS1_ENABLE_CNFG - Interrupt Control 1

Address: 10H							
Type: Read / Write							
Default Value: 00000000							
7	6	5	4	3	2	1	0
IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1
Bit	Name	Description					
7 - 0	INn	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the input clock validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid'), i.e., when the corresponding INn bit (b7-0, 0DH) is '1'. Here n is any one of 8 to 1. 0: Disabled. (default) 1: Enabled.					

INTERRUPTS2_ENABLE_CNFG - Interrupt Control 2

Address: 11H							
Type: Read / Write							
Default Value: 00000000							
7	6	5	4	3	2	1	0
T0_OPERATING_MODE	T0_MAIN_REF_FAILED	IN14	IN13	IN12	IN11	IN10	IN9
Bit	Name	Description					
7	T0_OPERATING_MODE	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the T0 DPLL operating mode switches, i.e., when the T0_OPERATING_MODE bit (b7, 0EH) is '1'. 0: Disabled. (default) 1: Enabled.					
6	T0_MAIN_REF_FAILED	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the T0 selected input clock has failed; i.e., when the T0_MAIN_REF_FAILED bit (b6, 0EH) is '1'. 0: Disabled. (default) 1: Enabled.					
5 - 0	INn	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the input clock validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid'), i.e., when the corresponding INn bit (b5-0, 0EH) is '1'. Here n is any one of 14 to 9. 0: Disabled. (default) 1: Enabled.					

INTERRUPTS3_ENABLE_CNFG - Interrupt Control 3

Address: 12H
 Type: Read / Write
 Default Value: 00X00000

7	6	5	4	3	2	1	0
EX_SYNC_ALARM	T4_STS	-	INPUT_TO_T4	AMI2_VIOL	AMI2_LOS	AMI1_VIOL	AMI1_LOS

Bit	Name	Description
7	EX_SYNC_ALARM	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when an external sync alarm has occurred, i.e., when the EX_SYNC_ALARM bit (b7, 0FH) is '1'. 0: Disabled. (default) 1: Enabled.
6	T4_STS	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the T4 DPLL locking status changes (from 'locked' to 'unlocked' or from 'unlocked' to 'locked'), i.e., when the T4_STS bit (b6, 0FH) is '1'. 0: Disabled. (default) 1: Enabled.
5	-	Reserved.
4	INPUT_TO_T4	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when all the input clocks for T4 path change to be unqualified, i.e., when the INPUT_TO_T4 bit (b4, 0FH) is '1'. 0: Disabled. (default) 1: Enabled.
3	AMI2_VIOL	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when IN2 has AMI violation, i.e., when the AMI2_VIOL bit (b3, 0FH) is '1'. 0: Disabled. (default) 1: Enabled.
2	AMI2_LOS	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when IN2 has LOS error, i.e., when the AMI2_LOS bit (b2, 0FH) is '1'. 0: Disabled. (default) 1: Enabled.
1	AMI1_VIOL	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when IN1 has AMI violation, i.e., when the AMI1_VIOL bit (b1, 0FH) is '1'. 0: Disabled. (default) 1: Enabled.
0	AMI1_LOS	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when IN1 has LOS error, i.e., when the AMI1_LOS bit (b0, 0FH) is '1'. 0: Disabled. (default) 1: Enabled.

7.2.3 INPUT CLOCK FREQUENCY & PRIORITY CONFIGURATION REGISTERS

IN1_CNFG - Input Clock 1 Configuration

Address: 14H
 Type: Read / Write
 Default Value: X0000000

7	6	5	4	3	2	1	0
-	400HZ_SEL	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

Bit	Name	Description
7	-	Reserved.
6	400HZ_SEL	This bit should be set to match the clock input on IN1: 0: 64 kHz + 8 kHz. (default) 1: 64 kHz + 8 kHz + 0.4 kHz.
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN1: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN1: 0000: 8 kHz. (default) 0001 ~ 1111: Reserved.

IN2_CNFG - Input Clock 2 Configuration

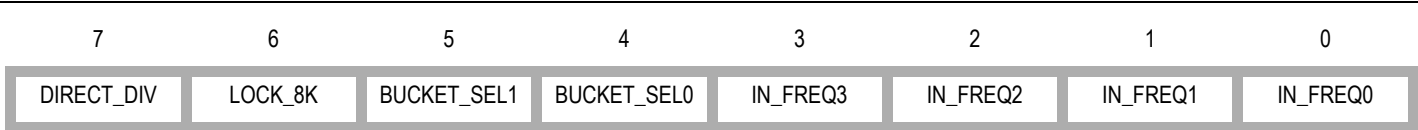
Address: 15H
 Type: Read / Write
 Default Value: X0000000

7	6	5	4	3	2	1	0
-	400HZ_SEL	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

Bit	Name	Description
7	-	Reserved.
6	400HZ_SEL	This bit should be set to match the clock input on IN2: 0: 64 kHz + 8 kHz. (default) 1: 64 kHz + 8 kHz + 0.4 kHz.
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN2: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN2: 0000: 8 kHz. (default) 0001 ~ 1111: Reserved.

IN3_CNFG - Input Clock 3 Configuration

Address: 16H
 Type: Read / Write
 Default Value: 00000000



Bit	Name	Description															
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 16H).															
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 16H), determines whether the DivN Divider or the Lock 8k Divider is used for IN3: <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">DIRECT_DIV bit</th> <th style="width: 20%;">LOCK_8K bit</th> <th style="width: 60%;">Used Divider</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Both bypassed (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Lock 8k Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">DivN Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Reserved</td> </tr> </tbody> </table>	DIRECT_DIV bit	LOCK_8K bit	Used Divider	0	0	Both bypassed (default)	0	1	Lock 8k Divider	1	0	DivN Divider	1	1	Reserved
DIRECT_DIV bit	LOCK_8K bit	Used Divider															
0	0	Both bypassed (default)															
0	1	Lock 8k Divider															
1	0	DivN Divider															
1	1	Reserved															
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN3: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.															
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN3: 0000: 8 kHz. (default) 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). 0010: 6.48 MHz. 0011: 19.44 MHz. 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011: Reserved. 1100: 6.25 MHz. 1101 ~ 1111: Reserved. For IN3, the required frequency should not be set higher than that clock.															

IN4_CNFG - Input Clock 4 Configuration

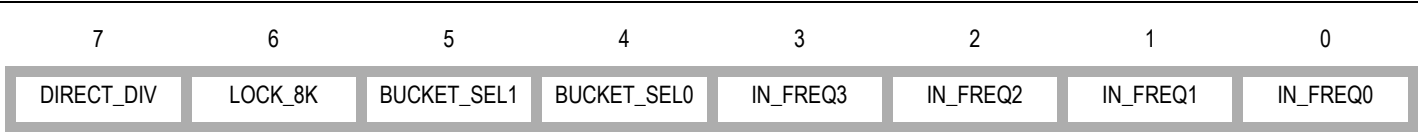
Address: 17H																						
Type: Read / Write																						
Default Value: 00000000																						
7	6	5	4	3	2	1	0															
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0															
Bit	Name	Description																				
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 17H).																				
6	LOCK_8K	<p>This bit, together with the DIRECT_DIV bit (b7, 17H), determines whether the DivN Divider or the Lock 8k Divider is used for IN4:</p> <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>DIRECT_DIV bit</th> <th>LOCK_8K bit</th> <th>Used Divider</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Both bypassed (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Lock 8k Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">DivN Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Reserved</td> </tr> </tbody> </table>						DIRECT_DIV bit	LOCK_8K bit	Used Divider	0	0	Both bypassed (default)	0	1	Lock 8k Divider	1	0	DivN Divider	1	1	Reserved
DIRECT_DIV bit	LOCK_8K bit	Used Divider																				
0	0	Both bypassed (default)																				
0	1	Lock 8k Divider																				
1	0	DivN Divider																				
1	1	Reserved																				
5 - 4	BUCKET_SEL[1:0]	<p>These bits select one of the four groups of leaky bucket configuration registers for IN4:</p> <p>00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default)</p> <p>01: Group 1; the addresses of the configuration registers are 35H ~ 38H.</p> <p>10: Group 2; the addresses of the configuration registers are 39H ~ 3CH.</p> <p>11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.</p>																				
3 - 0	IN_FREQ[3:0]	<p>These bits set the DPLL required frequency for IN4:</p> <p>0000: 8 kHz. (default)</p> <p>0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0').</p> <p>0010: 6.48 MHz.</p> <p>0011: 19.44 MHz.</p> <p>0100: 25.92 MHz.</p> <p>0101: 38.88 MHz.</p> <p>0110 ~ 1000: Reserved.</p> <p>1001: 2 kHz.</p> <p>1010: 4 kHz.</p> <p>1011: Reserved.</p> <p>1100: 6.25 MHz.</p> <p>1101 ~ 1111: Reserved.</p> <p>For the IN4, the required frequency should not be set higher than that clock.</p>																				

IN5_IN6_HF_DIV_CNFG - Input Clock 5 & 6 High Frequency Divider Configuration

Address: 18H							
Type: Read / Write							
Default Value: 00XXXX00							
7	6	5	4	3	2	1	0
IN6_DIV1	IN6_DIV0	-	-	-	-	IN5_DIV1	IN5_DIV0
Bit	Name	Description					
7 - 6	IN6_DIV[1:0]	These bits determine whether the HF Divider is used and what the division factor is for IN6 frequency division: 00: Bypassed. (default) 01: Divided by 4. 10: Divided by 5. 11: Reserved.					
5 - 2	-	Reserved.					
1 - 0	IN5_DIV[1:0]	These bits determine whether the HF Divider is used and what the division factor is for IN5 frequency division: 00: Bypassed. (default) 01: Divided by 4. 10: Divided by 5. 11: Reserved.					

IN5_CNFG - Input Clock 5 Configuration

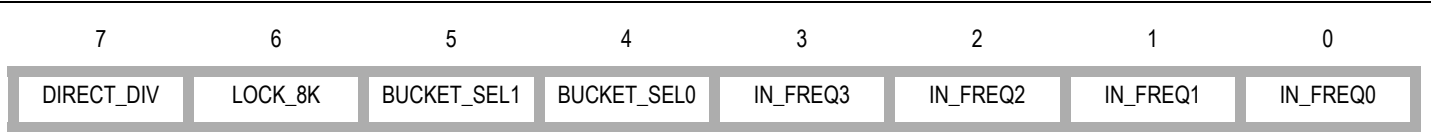
Address: 19H
 Type: Read / Write
 Default Value: 00000011



Bit	Name	Description															
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 19H).															
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 19H), determines whether the DivN Divider or the Lock 8k Divider is used for IN5: <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">DIRECT_DIV bit</th> <th style="width: 15%;">LOCK_8K bit</th> <th style="width: 70%;">Used Divider</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Both bypassed (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Lock 8k Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">DivN Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Reserved</td> </tr> </tbody> </table>	DIRECT_DIV bit	LOCK_8K bit	Used Divider	0	0	Both bypassed (default)	0	1	Lock 8k Divider	1	0	DivN Divider	1	1	Reserved
DIRECT_DIV bit	LOCK_8K bit	Used Divider															
0	0	Both bypassed (default)															
0	1	Lock 8k Divider															
1	0	DivN Divider															
1	1	Reserved															
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN5: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.															
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN5: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). 0010: 6.48 MHz. 0011: 19.44 MHz. (default) 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011: Reserved. 1100: 6.25 MHz. 1101 ~ 1111: Reserved. The required frequency should not be set higher than that clock.															

IN6_CNFG - Input Clock 6 Configuration

Address: 1AH
 Type: Read / Write
 Default Value: 00000011



Bit	Name	Description															
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 1AH).															
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 1AH), determines whether the DivN Divider or the Lock 8k Divider is used for IN6: <table border="1" style="margin: 10px auto; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>DIRECT_DIV bit</th> <th>LOCK_8K bit</th> <th>Used Divider</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Both bypassed (default)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Lock 8k Divider</td> </tr> <tr> <td>1</td> <td>0</td> <td>DivN Divider</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> </tbody> </table>	DIRECT_DIV bit	LOCK_8K bit	Used Divider	0	0	Both bypassed (default)	0	1	Lock 8k Divider	1	0	DivN Divider	1	1	Reserved
DIRECT_DIV bit	LOCK_8K bit	Used Divider															
0	0	Both bypassed (default)															
0	1	Lock 8k Divider															
1	0	DivN Divider															
1	1	Reserved															
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN6: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.															
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN6: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). 0010: 6.48 MHz. 0011: 19.44 MHz. (default) 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011: Reserved. 1100: 6.25 MHz. 1101 ~ 1111: Reserved. For IN6, the required frequency should not be set higher than that clock.															

IN7_CNFG - Input Clock 7 Configuration

Address: 1BH
 Type: Read / Write
 Default Value: 00000011



Bit	Name	Description															
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 1BH).															
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 1BH), determines whether the DivN Divider or the Lock 8k Divider is used for IN7: <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">DIRECT_DIV bit</th> <th style="width: 15%;">LOCK_8K bit</th> <th style="width: 70%;">Used Divider</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Both bypassed (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Lock 8k Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">DivN Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Reserved</td> </tr> </tbody> </table>	DIRECT_DIV bit	LOCK_8K bit	Used Divider	0	0	Both bypassed (default)	0	1	Lock 8k Divider	1	0	DivN Divider	1	1	Reserved
DIRECT_DIV bit	LOCK_8K bit	Used Divider															
0	0	Both bypassed (default)															
0	1	Lock 8k Divider															
1	0	DivN Divider															
1	1	Reserved															
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN7: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.															
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN7: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). 0010: 6.48 MHz. 0011: 19.44 MHz. (default) 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011: Reserved. 1100: 6.25 MHz. 1101 ~ 1111: Reserved. For IN7, the required frequency should not be set higher than that clock.															

IN8_CNFG - Input Clock 8 Configuration

Address: 1CH
 Type: Read / Write
 Default Value: 00000011



Bit	Name	Description															
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 1CH).															
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 1CH), determines whether the DivN Divider or the Lock 8k Divider is used for IN8: <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">DIRECT_DIV bit</th> <th style="width: 15%;">LOCK_8K bit</th> <th style="width: 70%;">Used Divider</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Both bypassed (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Lock 8k Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">DivN Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Reserved</td> </tr> </tbody> </table>	DIRECT_DIV bit	LOCK_8K bit	Used Divider	0	0	Both bypassed (default)	0	1	Lock 8k Divider	1	0	DivN Divider	1	1	Reserved
DIRECT_DIV bit	LOCK_8K bit	Used Divider															
0	0	Both bypassed (default)															
0	1	Lock 8k Divider															
1	0	DivN Divider															
1	1	Reserved															
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN8: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.															
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN8: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). 0010: 6.48 MHz. 0011: 19.44 MHz. (default) 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011: Reserved. 1100: 6.25 MHz. 1101 ~ 1111: Reserved. For IN8, the required frequency should not be set higher than that clock.															

IN9_CNFG - Input Clock 9 Configuration

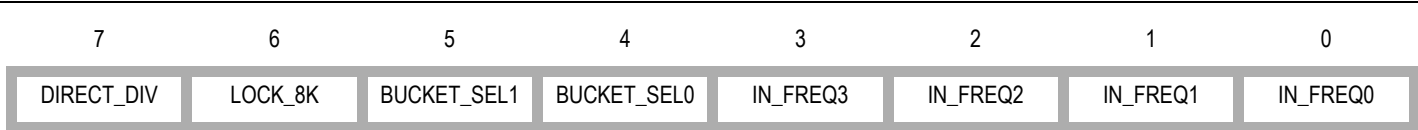
Address: 1DH
 Type: Read / Write
 Default Value: 00000011



Bit	Name	Description															
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 1DH).															
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 1DH), determines whether the DivN Divider or the Lock 8k Divider is used for IN9: <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">DIRECT_DIV bit</th> <th style="width: 15%;">LOCK_8K bit</th> <th style="width: 70%;">Used Divider</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Both bypassed (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Lock 8k Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">DivN Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Reserved</td> </tr> </tbody> </table>	DIRECT_DIV bit	LOCK_8K bit	Used Divider	0	0	Both bypassed (default)	0	1	Lock 8k Divider	1	0	DivN Divider	1	1	Reserved
DIRECT_DIV bit	LOCK_8K bit	Used Divider															
0	0	Both bypassed (default)															
0	1	Lock 8k Divider															
1	0	DivN Divider															
1	1	Reserved															
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN9: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.															
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN9: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). 0010: 6.48 MHz. 0011: 19.44 MHz. (default) 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011: Reserved. 1100: 6.25 MHz. 1101 ~ 1111: Reserved. For IN9, the required frequency should not be set higher than that clock.															

IN10_CNFG - Input Clock 10 Configuration

Address: 1EH
 Type: Read / Write
 Default Value: 00000011



Bit	Name	Description															
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 1EH).															
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 1EH), determines whether the DivN Divider or the Lock 8k Divider is used for IN10: <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">DIRECT_DIV bit</th> <th style="width: 15%;">LOCK_8K bit</th> <th style="width: 70%;">Used Divider</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Both bypassed (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Lock 8k Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">DivN Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Reserved</td> </tr> </tbody> </table>	DIRECT_DIV bit	LOCK_8K bit	Used Divider	0	0	Both bypassed (default)	0	1	Lock 8k Divider	1	0	DivN Divider	1	1	Reserved
DIRECT_DIV bit	LOCK_8K bit	Used Divider															
0	0	Both bypassed (default)															
0	1	Lock 8k Divider															
1	0	DivN Divider															
1	1	Reserved															
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN10: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.															
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN10: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). 0010: 6.48 MHz. 0011: 19.44 MHz. (default) 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011: Reserved. 1100: 6.25 MHz. 1101 ~ 1111: Reserved. For IN10, the required frequency should not be set higher than that clock.															

IN11_CNFG - Input Clock 11 Configuration

Address: 1FH																						
Type: Read / Write																						
Default Value: 0000XXXX																						
7	6	5	4	3	2	1	0															
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0															
Bit	Name	Description																				
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 1FH).																				
6	LOCK_8K	<p>This bit, together with the DIRECT_DIV bit (b7, 1FH), determines whether the DivN Divider or the Lock 8k Divider is used for IN11:</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DIRECT_DIV bit</th> <th>LOCK_8K bit</th> <th>Used Divider</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Both bypassed (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Lock 8k Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">DivN Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Reserved</td> </tr> </tbody> </table>						DIRECT_DIV bit	LOCK_8K bit	Used Divider	0	0	Both bypassed (default)	0	1	Lock 8k Divider	1	0	DivN Divider	1	1	Reserved
DIRECT_DIV bit	LOCK_8K bit	Used Divider																				
0	0	Both bypassed (default)																				
0	1	Lock 8k Divider																				
1	0	DivN Divider																				
1	1	Reserved																				
5 - 4	BUCKET_SEL[1:0]	<p>These bits select one of the four groups of leaky bucket configuration registers for IN11:</p> <p>00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default)</p> <p>01: Group 1; the addresses of the configuration registers are 35H ~ 38H.</p> <p>10: Group 2; the addresses of the configuration registers are 39H ~ 3CH.</p> <p>11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.</p>																				
3 - 0	IN_FREQ[3:0]	<p>These bits set the DPLL required frequency for IN11:</p> <p>0000: 8 kHz.</p> <p>0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0').</p> <p>0010: 6.48 MHz.</p> <p>0011: 19.44 MHz.</p> <p>0100: 25.92 MHz.</p> <p>0101: 38.88 MHz.</p> <p>0110 ~ 1000: Reserved.</p> <p>1001: 2 kHz.</p> <p>1010: 4 kHz.</p> <p>1011: Reserved.</p> <p>1100: 6.25 MHz.</p> <p>1101 ~ 1111: Reserved.</p> <p>For IN11, the required frequency should not be set higher than that clock.</p> <p>The default value of these bits depends on the device application as follows:</p> <p>In Master / Slave application, when the device is configured as the Master, the default value is '0001'; when the device is configured as the Slave, the default value is '0010'.</p>																				

IN12_CNFG - Input Clock 12 Configuration

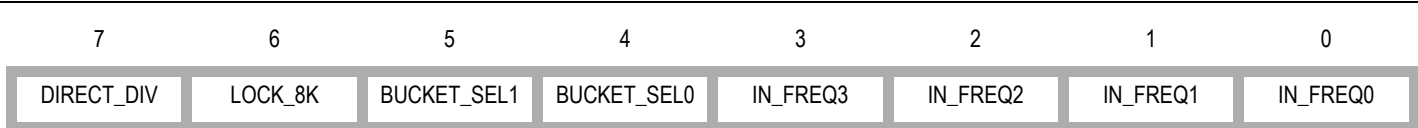
Address: 20H																						
Type: Read / Write																						
Default Value: 00000001																						
7	6	5	4	3	2	1	0															
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0															
Bit	Name	Description																				
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 20H).																				
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 20H), determines whether the DivN Divider or the Lock 8k Divider is used for IN12: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DIRECT_DIV bit</th> <th>LOCK_8K bit</th> <th>Used Divider</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Both bypassed (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Lock 8k Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">DivN Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Reserved</td> </tr> </tbody> </table>						DIRECT_DIV bit	LOCK_8K bit	Used Divider	0	0	Both bypassed (default)	0	1	Lock 8k Divider	1	0	DivN Divider	1	1	Reserved
DIRECT_DIV bit	LOCK_8K bit	Used Divider																				
0	0	Both bypassed (default)																				
0	1	Lock 8k Divider																				
1	0	DivN Divider																				
1	1	Reserved																				
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN12: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.																				
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN12: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). (default) 0010: 6.48 MHz. 0011: 19.44 MHz. 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011: Reserved. 1100: 6.25 MHz. 1101 ~ 1111: Reserved. For IN12, the required frequency should not be set higher than that clock.																				

IN13_CNFG - Input Clock 13 Configuration

Address: 21H Type: Read / Write Default Value: 00000001																						
7	6	5	4	3	2	1	0															
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0															
Bit	Name	Description																				
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 21H).																				
6	LOCK_8K	<p>This bit, together with the DIRECT_DIV bit (b7, 21H), determines whether the DivN Divider or the Lock 8k Divider is used for IN13:</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DIRECT_DIV bit</th> <th>LOCK_8K bit</th> <th>Used Divider</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Both bypassed (default)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Lock 8k Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">DivN Divider</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Reserved</td> </tr> </tbody> </table>						DIRECT_DIV bit	LOCK_8K bit	Used Divider	0	0	Both bypassed (default)	0	1	Lock 8k Divider	1	0	DivN Divider	1	1	Reserved
DIRECT_DIV bit	LOCK_8K bit	Used Divider																				
0	0	Both bypassed (default)																				
0	1	Lock 8k Divider																				
1	0	DivN Divider																				
1	1	Reserved																				
5 - 4	BUCKET_SEL[1:0]	<p>These bits select one of the four groups of leaky bucket configuration registers for IN13:</p> <p>00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default)</p> <p>01: Group 1; the addresses of the configuration registers are 35H ~ 38H.</p> <p>10: Group 2; the addresses of the configuration registers are 39H ~ 3CH.</p> <p>11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.</p>																				
3 - 0	IN_FREQ[3:0]	<p>These bits set the DPLL required frequency for IN13:</p> <p>0000: 8 kHz.</p> <p>0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). (default)</p> <p>0010: 6.48 MHz.</p> <p>0011: 19.44 MHz.</p> <p>0100: 25.92 MHz.</p> <p>0101: 38.88 MHz.</p> <p>0110 ~ 1000: Reserved.</p> <p>1001: 2 kHz.</p> <p>1010: 4 kHz.</p> <p>1011: Reserved.</p> <p>1100: 6.25 MHz.</p> <p>1101 ~ 1111: Reserved.</p> <p>For IN13, the required frequency should not be set higher than that clock.</p>																				

IN14_CNFG - Input Clock 14 Configuration

Address: 22H
 Type: Read / Write
 Default Value: 00000001



Bit	Name	Description															
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 22H).															
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 22H), determines whether the DivN Divider or the Lock 8k Divider is used for IN14: <table border="1" style="margin: 10px auto; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>DIRECT_DIV bit</th> <th>LOCK_8K bit</th> <th>Used Divider</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Both bypassed (default)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Lock 8k Divider</td> </tr> <tr> <td>1</td> <td>0</td> <td>DivN Divider</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> </tbody> </table>	DIRECT_DIV bit	LOCK_8K bit	Used Divider	0	0	Both bypassed (default)	0	1	Lock 8k Divider	1	0	DivN Divider	1	1	Reserved
DIRECT_DIV bit	LOCK_8K bit	Used Divider															
0	0	Both bypassed (default)															
0	1	Lock 8k Divider															
1	0	DivN Divider															
1	1	Reserved															
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN14: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.															
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN14: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). (default) 0010: 6.48 MHz. 0011: 19.44 MHz. 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011: Reserved. 1100: 6.25 MHz. 1101 ~ 1111: Reserved. For IN14, the required frequency should not be set higher than that clock.															

PRE_DIV_CH_CNFG - DivN Divider Channel Selection

Address: 23H							
Type: Read / Write							
Default Value: XXXX0000							
7	6	5	4	3	2	1	0
-	-	-	-	PRE_DIV_CH_VALUE3	PRE_DIV_CH_VALUE2	PRE_DIV_CH_VALUE1	PRE_DIV_CH_VALUE0
Bit	Name	Description					
7 - 4	-	Reserved.					
3 - 0	PRE_DIV_CH_VALUE[3:0]	This register is an indirect address register for Register 24H and 25H. These bits select an input clock. The value set in the PRE_DIVN_VALUE[14:0] bits (25H, 24H) is available for the selected input clock. 0000: Reserved. (default) 0001, 0010: Reserved. 0011: IN3. 0100: IN4. 1101: IN13. 1110: IN14. 1111: Reserved.					

PRE_DIVN[7:0]_CNFG - DivN Divider Division Factor Configuration 1

Address: 24H							
Type: Read / Write							
Default Value: 00000000							
7	6	5	4	3	2	1	0
PRE_DIVN_VA LUE7	PRE_DIVN_VA LUE6	PRE_DIVN_VA LUE5	PRE_DIVN_VA LUE4	PRE_DIVN_VA LUE3	PRE_DIVN_VA LUE2	PRE_DIVN_VA LUE1	PRE_DIVN_VA LUE0
Bit	Name	Description					
7 - 0	PRE_DIVN_VALUE[7:0]	Refer to the description of the PRE_DIVN_VALUE[14:8] bits (b6~0, 25H).					

PRE_DIVN[14:8]_CNFG - DivN Divider Division Factor Configuration 2

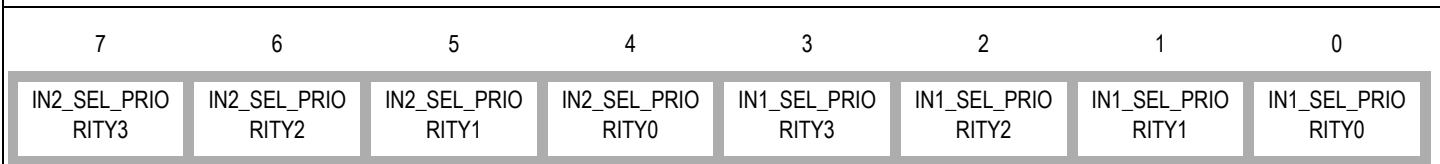
Address: 25H
 Type: Read / Write
 Default Value: X0000000

7	6	5	4	3	2	1	0
-	PRE_DIVN_VAL UE14	PRE_DIVN_VAL UE13	PRE_DIVN_VAL UE12	PRE_DIVN_VAL UE11	PRE_DIVN_VAL UE10	PRE_DIVN_VAL UE9	PRE_DIVN_VAL UE8

Bit	Name	Description
7	-	Reserved.
6 - 0	PRE_DIVN_VALUE[14:8]	<p>The division factor for an input clock is equal to PRE_DIVN_VALUE[14:0] plus 1. The input clock is selected by the PRE_DIV_CH_VALUE[3:0] bits (b3~0, 23H). A value from '1' to '4BEF' (Hex) can be written into, corresponding to a division factor from 2 to 19440. The others are reserved. So the DivN Divider only supports an input clock whose frequency is less than or equal to (\leq) 155.52 MHz.</p> <p>The division factor setting should observe the following order: 1. Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits; 2. Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.</p>

IN1_IN2_SEL_PRIORITY_CNFG - Input Clock 1 & 2 Priority Configuration *

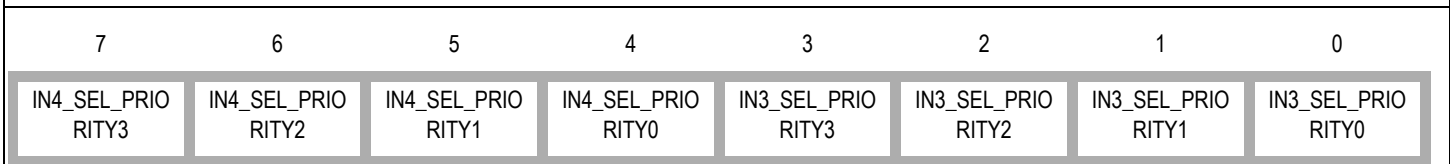
Address: 26H
 Type: Read / Write
 Default Value: T0 - 00110010 / T4 - 00000000



Bit	Name	Description
7 - 4	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 2: 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. (T0 default) 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.
3 - 0	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 1: 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. 0010: Priority 2. (T0 default) 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.

IN3_IN4_SEL_PRIORITY_CNFG - Input Clock 3 & 4 Priority Configuration *

Address: 27H
 Type: Read / Write
 Default Value: T0 - 01010100 / T4 - 00000000



Bit	Name	Description
7 - 4	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 4. 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. (T0 default) 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.
3 - 0	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 3. 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. (T0 default) 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.

IN5_IN6_SEL_PRIORITY_CNFG - Input Clock 5 & 6 Priority Configuration *

Address: 28H							
Type: Read / Write							
Default Value: T0/T4 - 01110110							
7	6	5	4	3	2	1	0
IN6_SEL_PRIORITY3	IN6_SEL_PRIORITY2	IN6_SEL_PRIORITY1	IN6_SEL_PRIORITY0	IN5_SEL_PRIORITY3	IN5_SEL_PRIORITY2	IN5_SEL_PRIORITY1	IN5_SEL_PRIORITY0
Bit	Name	Description					
7 - 4	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 6. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. (default) 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.					
3 - 0	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 5. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. (default) 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.					

IN7_IN8_SEL_PRIORITY_CNFG - Input Clock 7 & 8 Priority Configuration *

Address: 29H
 Type: Read / Write
 Default Value: 10011000

7	6	5	4	3	2	1	0
IN8_SEL_PRIORITY3	IN8_SEL_PRIORITY2	IN8_SEL_PRIORITY1	IN8_SEL_PRIORITY0	IN7_SEL_PRIORITY3	IN7_SEL_PRIORITY2	IN7_SEL_PRIORITY1	IN7_SEL_PRIORITY0

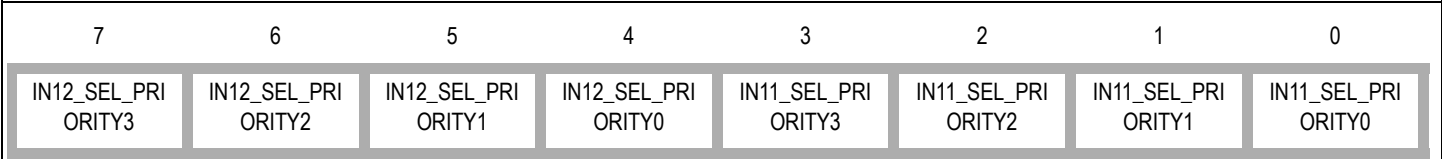
Bit	Name	Description
7 - 4	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 8. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. (default) 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.
3 - 0	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 7. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. (default) 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.

IN9_IN10_SEL_PRIORITY_CNFG - Input Clock 9 & 10 Priority Configuration *

Address: 2AH							
Type: Read / Write							
Default Value: 10111010							
7	6	5	4	3	2	1	0
IN10_SEL_PRIORITY3	IN10_SEL_PRIORITY2	IN10_SEL_PRIORITY1	IN10_SEL_PRIORITY0	IN9_SEL_PRIORITY3	IN9_SEL_PRIORITY2	IN9_SEL_PRIORITY1	IN9_SEL_PRIORITY0
Bit	Name	Description					
7 - 4	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 10. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. (default) 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.					
3 - 0	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 9. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. (default) 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.					

IN11_IN12_SEL_PRIORITY_CNFG - Input Clock 11 & 12 Priority Configuration *

Address: 2BH
 Type: Read / Write
 Default Value: 11011100 (T0 Master)/11010001 (T0 Slave) 00000000 (T4)



Bit	Name	Description
7 - 4	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 12: 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. (T0 Master/Slave default) 1110: Priority 14. 1111: Priority 15.
3 - 0	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 11: 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. (T0 Slave default) 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. (T0 Master default) 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.

IN13_IN14_SEL_PRIORITY_CNFG - Input Clock 13 & 14 Priority Configuration *

Address: 2CH							
Type: Read / Write							
Default Value: 11111110 (T0) 00000000 (T4)							
7	6	5	4	3	2	1	0
IN14_SEL_PRIORITY3	IN14_SEL_PRIORITY2	IN14_SEL_PRIORITY1	IN14_SEL_PRIORITY0	IN13_SEL_PRIORITY3	IN13_SEL_PRIORITY2	IN13_SEL_PRIORITY1	IN13_SEL_PRIORITY0
Bit	Name	Description					
7 - 4	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 14: 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15. (T0 default)					
3 - 0	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 13: 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. (T0 default) 1111: Priority 15.					

7.2.4 INPUT CLOCK QUALITY MONITORING CONFIGURATION & STATUS REGISTERS

FREQ_MON_FACTOR_CNFG - Factor of Frequency Monitor Configuration

Address: 2EH							
Type: Read / Write							
Default Value: XXXX1011							
7	6	5	4	3	2	1	0
-	-	-	-	FREQ_MON_F ACTOR3	FREQ_MON_F ACTOR2	FREQ_MON_F ACTOR1	FREQ_MON_F ACTOR0
Bit	Name	Description					
7 - 4	-	Reserved.					
3 - 0	FREQ_MON_FACTOR[3:0]	<p>These bits determine a factor. The factor has a relationship with the frequency hard alarm threshold in ppm (refer to the description of the ALL_FREQ_HARD_THRESHOLD[3:0] bits (b3~0, 2FH)) and with the frequency of the input clock with respect to the master clock in ppm (refer to the description of the IN_FREQ_VALUE[7:0] bits (b7~0, 42H)). The factor represents the accuracy of the frequency monitor and should be set according to the requirements of different applications.</p> <p>0000: 0.0032. 0001: 0.0064. 0010: 0.0127. 0011: 0.0257. 0100: 0.0514. 0101: 0.103. 0110: 0.206. 0111: 0.412. 1000: 0.823. 1001: 1.646. 1010: 3.292. 1011: 3.81. (default) 1100 - 1111: 4.6.</p>					

HARD_FREQ_MON_THRESHOLD_CNFG - Frequency Monitor Threshold for Hard Input Clocks Configuration

Address: 2FH							
Type: Read / Write							
Default Value: 00100011							
7	6	5	4	3	2	1	0
HARD_FREQ_MON_THRESH OLD7	HARD_FREQ_MON_THRESH OLD6	HARD_FREQ_MON_THRESH OLD5	HARD_FREQ_MON_THRESH OLD4	HARD_FREQ_MON_THRESH OLD3	HARD_FREQ_MON_THRESH OLD2	HARD_FREQ_MON_THRESH OLD1	HARD_FREQ_MON_THRESH OLD0
Bit	Name	Description					
7 - 4	HARD_FREQ_MON_THRESHOLD[7:4]	<p>These bits are the accepting threshold of reference clock monitoring. The frequency hard alarm threshold in ppm is calculated as follows: Frequency Hard Alarm Threshold (ppm) = (HARD_FREQ_MON_THRESHOLD[7:4] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, 2EH) This threshold is symmetrical about zero. A value of 0010 bin corresponds to an alarm limit of +/- 11.43 ppm.</p>					
3 - 0	HARD_FREQ_MON_THRESHOLD[3:0]	<p>These bits are the rejecting threshold of reference clock monitoring. The frequency hard alarm threshold in ppm is calculated as follows: Frequency Hard Alarm Threshold (ppm) = (HARD_FREQ_MON_THRESHOLD[3:0] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, 2EH) This threshold is symmetrical about zero. A value of 0010 bin corresponds to an alarm limit of +/- 11.43 ppm.</p>					

SOFT_FREQ_MON_THRESHOLD_CNFG - Frequency Monitor Threshold for Soft Input Clocks Configuration

Address: 30H							
Type: Read / Write							
Default Value: 00100011							
7	6	5	4	3	2	1	0
SOFT_FREQ_MON_THRESHO LD7	SOFT_FREQ_MON_THRESHO LD6	SOFT_FREQ_MON_THRESHO LD5	SOFT_FREQ_MON_THRESHO LD4	SOFT_FREQ_MON_THRESH OLD3	SOFT_FREQ_MON_THRESH OLD2	SOFT_FREQ_MON_THRESH OLD1	SOFT_FREQ_MON_THRESH OLD0
Bit	Name	Description					
7 - 4	SOFT_FREQ_MON_THRESHOLD[7:4]	<p>These bits are the accepting threshold of reference clock monitoring. The frequency soft alarm threshold in ppm is calculated as follows: Frequency Soft Alarm Threshold (ppm) = (SOFT_FREQ_MON_THRESHOLD[7:4] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, 2EH) This threshold is symmetrical about zero. A value of 0010 bin corresponds to an alarm limit of +/- 11.43 ppm.</p>					
3 - 0	SOFT_FREQ_MON_THRESHOLD[3:0]	<p>These bits are the rejecting threshold of reference clock monitoring. The frequency soft alarm threshold in ppm is calculated as follows: Frequency Soft Alarm Threshold (ppm) = (SOFT_FREQ_MON_THRESHOLD[3:0] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, 2EH) This threshold is symmetrical about zero. A value of 0010 bin corresponds to an alarm limit of +/- 11.43 ppm.</p>					

UPPER_THRESHOLD_0_CNFG - Upper Threshold for Leaky Bucket Configuration 0

Address: 31H							
Type: Read / Write							
Default Value: 00000110							
7	6	5	4	3	2	1	0
UPPER_THRE SHOLD_0_DAT A7	UPPER_THRE SHOLD_0_DAT A6	UPPER_THRE SHOLD_0_DAT A5	UPPER_THRE SHOLD_0_DAT A4	UPPER_THRE SHOLD_0_DAT A3	UPPER_THRE SHOLD_0_DAT A2	UPPER_THRE SHOLD_0_DAT A1	UPPER_THRE SHOLD_0_DAT A0
Bit	Name	Description					
7 - 0	UPPER_THRESHOLD_0_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.					

LOWER_THRESHOLD_0_CNFG - Lower Threshold for Leaky Bucket Configuration 0

Address: 32H							
Type: Read / Write							
Default Value: 00000100							
7	6	5	4	3	2	1	0
LOWER_THRE SHOLD_0_DAT A7	LOWER_THRE SHOLD_0_DAT A6	LOWER_THRE SHOLD_0_DAT A5	LOWER_THRE SHOLD_0_DAT A4	LOWER_THRE SHOLD_0_DAT A3	LOWER_THRE SHOLD_0_DAT A2	LOWER_THRE SHOLD_0_DAT A1	LOWER_THRE SHOLD_0_DAT A0
Bit	Name	Description					
7 - 0	LOWER_THRESHOLD_0_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.					

BUCKET_SIZE_0_CNFG - Bucket Size for Leaky Bucket Configuration 0

Address: 33H							
Type: Read / Write							
Default Value: 00001000							
7	6	5	4	3	2	1	0
BUCKET_SIZE _0_DATA7	BUCKET_SIZE _0_DATA6	BUCKET_SIZE _0_DATA5	BUCKET_SIZE _0_DATA4	BUCKET_SIZE _0_DATA3	BUCKET_SIZE _0_DATA2	BUCKET_SIZE _0_DATA1	BUCKET_SIZE _0_DATA0
Bit	Name	Description					
7 - 0	BUCKET_SIZE_0_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.					

DECAY_RATE_0_CNFG - Decay Rate for Leaky Bucket Configuration 0

Address: 34H							
Type: Read / Write							
Default Value: XXXXXX01							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_0_DATA1	DECAY_RATE_0_DATA0
Bit	Name	Description					
7 - 2	-	Reserved.					
1 - 0	DECAY_RATE_0_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.					

UPPER_THRESHOLD_1_CNFG - Upper Threshold for Leaky Bucket Configuration 1

Address: 35H							
Type: Read / Write							
Default Value: 00000110							
7	6	5	4	3	2	1	0
UPPER_THRE SHOLD_1_DAT A7	UPPER_THRE SHOLD_1_DAT A6	UPPER_THRE SHOLD_1_DAT A5	UPPER_THRE SHOLD_1_DAT A4	UPPER_THRE SHOLD_1_DAT A3	UPPER_THRE SHOLD_1_DAT A2	UPPER_THRE SHOLD_1_DAT A1	UPPER_THRE SHOLD_1_DAT A0
Bit	Name	Description					
7 - 0	UPPER_THRESHOLD_1_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.					

LOWER_THRESHOLD_1_CNFG - Lower Threshold for Leaky Bucket Configuration 1

Address: 36H							
Type: Read / Write							
Default Value: 00000100							
7	6	5	4	3	2	1	0
LOWER_THRE SHOLD_1_DAT A7	LOWER_THRE SHOLD_1_DAT A6	LOWER_THRE SHOLD_1_DAT A5	LOWER_THRE SHOLD_1_DAT A4	LOWER_THRE SHOLD_1_DAT A3	LOWER_THRE SHOLD_1_DAT A2	LOWER_THRE SHOLD_1_DAT A1	LOWER_THRE SHOLD_1_DAT A0
Bit	Name	Description					
7 - 0	LOWER_THRESHOLD_1_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.					

BUCKET_SIZE_1_CNFG - Bucket Size for Leaky Bucket Configuration 1

Address: 37H							
Type: Read / Write							
Default Value: 00001000							
7	6	5	4	3	2	1	0
BUCKET_SIZE _1_DATA7	BUCKET_SIZE _1_DATA6	BUCKET_SIZE _1_DATA5	BUCKET_SIZE _1_DATA4	BUCKET_SIZE _1_DATA3	BUCKET_SIZE _1_DATA2	BUCKET_SIZE _1_DATA1	BUCKET_SIZE _1_DATA0
Bit	Name	Description					
7 - 0	BUCKET_SIZE_1_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.					

DECAY_RATE_1_CNFG - Decay Rate for Leaky Bucket Configuration 1

Address: 38H							
Type: Read / Write							
Default Value: XXXXXX01							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_ 1_DATA1	DECAY_RATE_ 1_DATA0
Bit	Name	Description					
7 - 2	-	Reserved.					
1 - 0	DECAY_RATE_1_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.					

UPPER_THRESHOLD_2_CNFG - Upper Threshold for Leaky Bucket Configuration 2

Address: 39H							
Type: Read / Write							
Default Value: 00000110							
7	6	5	4	3	2	1	0
UPPER_THRE SHOLD_2_DAT A7	UPPER_THRE SHOLD_2_DAT A6	UPPER_THRE SHOLD_2_DAT A5	UPPER_THRE SHOLD_2_DAT A4	UPPER_THRE SHOLD_2_DAT A3	UPPER_THRE SHOLD_2_DAT A2	UPPER_THRE SHOLD_2_DAT A1	UPPER_THRE SHOLD_2_DAT A0
Bit	Name	Description					
7 - 0	UPPER_THRESHOLD_2_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.					

LOWER_THRESHOLD_2_CNFG - Lower Threshold for Leaky Bucket Configuration 2

Address: 3AH							
Type: Read / Write							
Default Value: 00000100							
7	6	5	4	3	2	1	0
LOWER_THRE SHOLD_2_DAT A7	LOWER_THRE SHOLD_2_DAT A6	LOWER_THRE SHOLD_2_DAT A5	LOWER_THRE SHOLD_2_DAT A4	LOWER_THRE SHOLD_2_DAT A3	LOWER_THRE SHOLD_2_DAT A2	LOWER_THRE SHOLD_2_DAT A1	LOWER_THRE SHOLD_2_DAT A0
Bit	Name	Description					
7 - 0	LOWER_THRESHOLD_2_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.					

BUCKET_SIZE_2_CNFG - Bucket Size for Leaky Bucket Configuration 2

Address: 3BH							
Type: Read / Write							
Default Value: 00001000							
7	6	5	4	3	2	1	0
BUCKET_SIZE _2_DATA7	BUCKET_SIZE _2_DATA6	BUCKET_SIZE _2_DATA5	BUCKET_SIZE _2_DATA4	BUCKET_SIZE _2_DATA3	BUCKET_SIZE _2_DATA2	BUCKET_SIZE _2_DATA1	BUCKET_SIZE _2_DATA0
Bit	Name	Description					
7 - 0	BUCKET_SIZE_2_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.					

DECAY_RATE_2_CNFG - Decay Rate for Leaky Bucket Configuration 2

Address: 3CH							
Type: Read / Write							
Default Value: XXXXXX01							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_ 2_DATA1	DECAY_RATE_ 2_DATA0
Bit	Name	Description					
7 - 2	-	Reserved.					
1 - 0	DECAY_RATE_2_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.					

UPPER_THRESHOLD_3_CNFG - Upper Threshold for Leaky Bucket Configuration 3

Address: 3DH							
Type: Read / Write							
Default Value: 00000110							
7	6	5	4	3	2	1	0
UPPER_THRE SHOLD_3_DAT A7	UPPER_THRE SHOLD_3_DAT A6	UPPER_THRE SHOLD_3_DAT A5	UPPER_THRE SHOLD_3_DAT A4	UPPER_THRE SHOLD_3_DAT A3	UPPER_THRE SHOLD_3_DAT A2	UPPER_THRE SHOLD_3_DAT A1	UPPER_THRE SHOLD_3_DAT A0
Bit	Name	Description					
7 - 0	UPPER_THRESHOLD_3_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.					

LOWER_THRESHOLD_3_CNFG - Lower Threshold for Leaky Bucket Configuration 3

Address: 3EH							
Type: Read / Write							
Default Value: 00000100							
7	6	5	4	3	2	1	0
LOWER_THRE SHOLD_3_DAT A7	LOWER_THRE SHOLD_3_DAT A6	LOWER_THRE SHOLD_3_DAT A5	LOWER_THRE SHOLD_3_DAT A4	LOWER_THRE SHOLD_3_DAT A3	LOWER_THRE SHOLD_3_DAT A2	LOWER_THRE SHOLD_3_DAT A1	LOWER_THRE SHOLD_3_DAT A0
Bit	Name	Description					
7 - 0	LOWER_THRESHOLD_3_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.					

BUCKET_SIZE_3_CNFG - Bucket Size for Leaky Bucket Configuration 3

Address: 3FH							
Type: Read / Write							
Default Value: 00001000							
7	6	5	4	3	2	1	0
BUCKET_SIZE _3_DATA7	BUCKET_SIZE _3_DATA6	BUCKET_SIZE _3_DATA5	BUCKET_SIZE _3_DATA4	BUCKET_SIZE _3_DATA3	BUCKET_SIZE _3_DATA2	BUCKET_SIZE _3_DATA1	BUCKET_SIZE _3_DATA0
Bit	Name	Description					
7 - 0	BUCKET_SIZE_3_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.					

DECAY_RATE_3_CNFG - Decay Rate for Leaky Bucket Configuration 3

Address: 40H
 Type: Read / Write
 Default Value: XXXXXX01

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_3_DATA1	DECAY_RATE_3_DATA0

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	DECAY_RATE_3_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.

IN_FREQ_READ_CH_CNFG - Input Clock Frequency Read Channel Selection

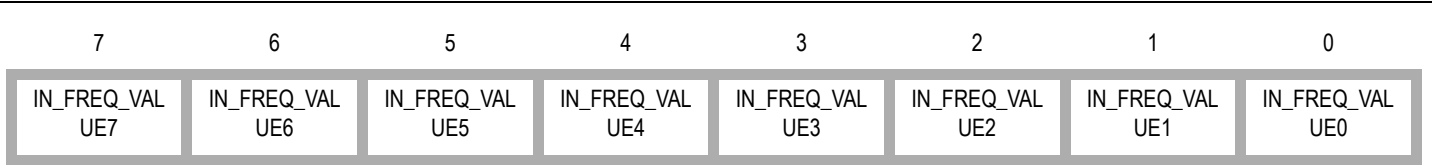
Address: 41H
 Type: Read / Write
 Default Value: XXXX0000

7	6	5	4	3	2	1	0
-	-	-	-	IN_FREQ_READ_CH3	IN_FREQ_READ_CH2	IN_FREQ_READ_CH1	IN_FREQ_READ_CH0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	IN_FREQ_READ_CH[3:0]	These bits select an input clock, the frequency of which with respect to the reference clock can be read. 0000: Reserved. (default) 0001: IN1. 0010: IN2. 1101: IN13. 1110: IN14. 1111: Reserved.

IN_FREQ_READ_STS - Input Clock Frequency Read Value

Address: 42H
 Type: Read
 Default Value: 00000000



Bit	Name	Description
7 - 0	IN_FREQ_VALUE[7:0]	These bits represent a 2's complement signed integer. If the value is multiplied by the value in the FREQ_MON_FACTOR[3:0] bits (b3~0, 2EH), the frequency of an input clock with respect to the reference clock in ppm will be obtained. The input clock is selected by the IN_FREQ_READ_CH[3:0] bits (b3~0, 41H). The value in these bits is updated every 16 seconds, starting when an input clock is selected.

IN1_IN2_STS - Input Clock 1 & 2 Status

Address: 43H
 Type: Read
 Default Value: 01100110

7	6	5	4	3	2	1	0
IN2_FREQ_SOFT_ALARM	IN2_FREQ_HARD_ALARM	IN2_NO_ACTIVITY_ALARM	IN2_PH_LOCK_ALARM	IN1_FREQ_SOFT_ALARM	IN1_FREQ_HARD_ALARM	IN1_NO_ACTIVITY_ALARM	IN1_PH_LOCK_ALARM

Bit	Name	Description
7	IN2_FREQ_SOFT_ALARM	This bit indicates whether IN2 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.
6	IN2_FREQ_HARD_ALARM	This bit indicates whether IN2 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.
5	IN2_NO_ACTIVITY_ALARM	This bit indicates whether IN2 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
4	IN2_PH_LOCK_ALARM	This bit indicates whether IN2 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised.
3	IN1_FREQ_SOFT_ALARM	This bit indicates whether IN1 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.
2	IN1_FREQ_HARD_ALARM	This bit indicates whether IN1 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.
1	IN1_NO_ACTIVITY_ALARM	This bit indicates whether IN1 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
0	IN1_PH_LOCK_ALARM	This bit indicates whether IN1 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised.

IN3_IN4_STS - Input Clock 3 & 4 Status

Address: 44H
 Type: Read
 Default Value: 01100110

7	6	5	4	3	2	1	0
IN4_FREQ_SOFT_ALARM	IN4_FREQ_HARD_ALARM	IN4_NO_ACTIVITY_ALARM	IN4_PH_LOCK_ALARM	IN3_FREQ_SOFT_ALARM	IN3_FREQ_HARD_ALARM	IN3_NO_ACTIVITY_ALARM	IN3_PH_LOCK_ALARM

Bit	Name	Description
7	IN4_FREQ_SOFT_ALARM	This bit indicates whether IN4 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.
6	IN4_FREQ_HARD_ALARM	This bit indicates whether IN4 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.
5	IN4_NO_ACTIVITY_ALARM	This bit indicates whether IN4 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
4	IN4_PH_LOCK_ALARM	This bit indicates whether IN4 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised.
3	IN3_FREQ_SOFT_ALARM	This bit indicates whether IN3 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.
2	IN3_FREQ_HARD_ALARM	This bit indicates whether IN3 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.
1	IN3_NO_ACTIVITY_ALARM	This bit indicates whether IN3 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
0	IN3_PH_LOCK_ALARM	This bit indicates whether IN3 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised.

IN5_IN6_STS - Input Clock 5 & 6 Status

Address: 45H
 Type: Read
 Default Value: 01100110

7	6	5	4	3	2	1	0
IN6_FREQ_SOFT_ALARM	IN6_FREQ_HARD_ALARM	IN6_NO_ACTIVITY_ALARM	IN6_PH_LOCK_ALARM	IN5_FREQ_SOFT_ALARM	IN5_FREQ_HARD_ALARM	IN5_NO_ACTIVITY_ALARM	IN5_PH_LOCK_ALARM

Bit	Name	Description
7	IN6_FREQ_SOFT_ALARM	This bit indicates whether IN6 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.
6	IN6_FREQ_HARD_ALARM	This bit indicates whether IN6 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.
5	IN6_NO_ACTIVITY_ALARM	This bit indicates whether IN6 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
4	IN6_PH_LOCK_ALARM	This bit indicates whether IN6 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised.
3	IN5_FREQ_SOFT_ALARM	This bit indicates whether IN5 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.
2	IN5_FREQ_HARD_ALARM	This bit indicates whether IN5 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.
1	IN5_NO_ACTIVITY_ALARM	This bit indicates whether IN5 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
0	IN5_PH_LOCK_ALARM	This bit indicates whether IN5 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised.

IN7_IN8_STS - Input Clock 7 & 8 Status

Address: 46H							
Type: Read							
Default Value: 01100110							
7	6	5	4	3	2	1	0
IN8_FREQ_SOFT_ALARM	IN8_FREQ_HARD_ALARM	IN8_NO_ACTIVITY_ALARM	IN8_PH_LOCK_ALARM	IN7_FREQ_SOFT_ALARM	IN7_FREQ_HARD_ALARM	IN7_NO_ACTIVITY_ALARM	IN7_PH_LOCK_ALARM
Bit	Name	Description					
7	IN8_FREQ_SOFT_ALARM	This bit indicates whether IN8 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.					
6	IN8_FREQ_HARD_ALARM	This bit indicates whether IN8 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.					
5	IN8_NO_ACTIVITY_ALARM	This bit indicates whether IN8 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)					
4	IN8_PH_LOCK_ALARM	This bit indicates whether IN8 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised.					
3	IN7_FREQ_SOFT_ALARM	This bit indicates whether IN7 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.					
2	IN7_FREQ_HARD_ALARM	This bit indicates whether IN7 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.					
1	IN7_NO_ACTIVITY_ALARM	This bit indicates whether IN7 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)					
0	IN7_PH_LOCK_ALARM	This bit indicates whether IN7 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised.					

IN9_IN10_STS - Input Clock 9 & 10 Status

Address: 47H							
Type: Read							
Default Value: 01100110							
7	6	5	4	3	2	1	0
IN10_FREQ_SOFT_ALARM	IN10_FREQ_HARD_ALARM	IN10_NO_ACTIVITY_ALARM	IN10_PH_LOCK_ALARM	IN9_FREQ_SOFT_ALARM	IN9_FREQ_HARD_ALARM	IN9_NO_ACTIVITY_ALARM	IN9_PH_LOCK_ALARM
Bit	Name	Description					
7	IN10_FREQ_SOFT_ALARM	This bit indicates whether IN10 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.					
6	IN10_FREQ_HARD_ALARM	This bit indicates whether IN10 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.					
5	IN10_NO_ACTIVITY_ALARM	This bit indicates whether IN10 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)					
4	IN10_PH_LOCK_ALARM	This bit indicates whether IN10 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised.					
3	IN9_FREQ_SOFT_ALARM	This bit indicates whether IN9 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.					
2	IN9_FREQ_HARD_ALARM	This bit indicates whether IN9 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.					
1	IN9_NO_ACTIVITY_ALARM	This bit indicates whether IN9 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)					
0	IN9_PH_LOCK_ALARM	This bit indicates whether IN9 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised.					

IN11_IN12_STS - Input Clock 11 & 12 Status

Address: 48H
 Type: Read
 Default Value: 01100110

7	6	5	4	3	2	1	0
IN12_FREQ_SOFT_ALARM	IN12_FREQ_HARD_ALARM	IN12_NO_ACTIVITY_ALARM	IN12_PH_LOCK_ALARM	IN11_FREQ_SOFT_ALARM	IN11_FREQ_HARD_ALARM	IN11_NO_ACTIVITY_ALARM	IN11_PH_LOCK_ALARM

Bit	Name	Description
7	IN12_FREQ_SOFT_ALARM	This bit indicates whether IN12 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.
6	IN12_FREQ_HARD_ALARM	This bit indicates whether IN12 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.
5	IN12_NO_ACTIVITY_ALARM	This bit indicates whether IN12 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
4	IN12_PH_LOCK_ALARM	This bit indicates whether IN12 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised.
3	IN11_FREQ_SOFT_ALARM	This bit indicates whether IN11 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.
2	IN11_FREQ_HARD_ALARM	This bit indicates whether IN11 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.
1	IN11_NO_ACTIVITY_ALARM	This bit indicates whether IN11 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
0	IN11_PH_LOCK_ALARM	This bit indicates whether IN11 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised.

IN13_IN14_STS - Input Clock 13 & 14 Status

Address: 49H Type: Read Default Value: X110X110							
7	6	5	4	3	2	1	0
IN14_FREQ_SOFT_ALARM	IN14_FREQ_HARD_ALARM	IN14_NO_ACTIVITY_ALARM	IN14_PH_LOCK_ALARM	IN13_FREQ_SOFT_ALARM	IN13_FREQ_HARD_ALARM	IN13_NO_ACTIVITY_ALARM	IN13_PH_LOCK_ALARM
Bit	Name	Description					
7	IN14_FREQ_SOFT_ALARM	This bit indicates whether IN14 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.					
6	IN14_FREQ_HARD_ALARM	This bit indicates whether IN14 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.					
5	IN14_NO_ACTIVITY_ALARM	This bit indicates whether IN14 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)					
4	IN14_PH_LOCK_ALARM	This bit indicates whether IN14 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised.					
3	IN13_FREQ_SOFT_ALARM	This bit indicates whether IN13 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.					
2	IN13_FREQ_HARD_ALARM	This bit indicates whether IN13 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.					
1	IN13_NO_ACTIVITY_ALARM	This bit indicates whether IN13 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)					
0	IN13_PH_LOCK_ALARM	This bit indicates whether IN13 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised.					

7.2.5 T0 / T4 DPLL INPUT CLOCK SELECTION REGISTERS

INPUT_VALID1_STS - Input Clocks Validity 1

Address: 4AH							
Type: Read							
Default Value: 00000000							
7	6	5	4	3	2	1	0
IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1
Bit	Name	Description					
7 - 0	INn	This bit indicates the validity of the corresponding INn. Here n is any one of 8 to 1. 0: Invalid. (default) 1: Valid.					

INPUT_VALID2_STS - Input Clocks Validity 2

Address: 4BH							
Type: Read							
Default Value: XX000000							
7	6	5	4	3	2	1	0
-	-	IN14	IN13	IN12	IN11	IN10	IN9
Bit	Name	Description					
7 - 6	-	Reserved.					
5 - 0	INn	This bit indicates the validity of the corresponding INn. Here n is any one of 14 to 9. 0: Invalid. (default) 1: Valid.					

REMOTE_INPUT_VALID1_CNFG - Input Clocks Validity Configuration 1

Address: 4CH							
Type: Read / Write							
Default Value: 11111111							
7	6	5	4	3	2	1	0
IN8_VALID	IN7_VALID	IN6_VALID	IN5_VALID	IN4_VALID	IN3_VALID	IN2_VALID	IN1_VALID
Bit	Name	Description					
7 - 0	INn_VALID	This bit controls whether the corresponding INn is allowed to be locked for automatic selection. Here n is any one of 8 to 1. 0: Enabled. 1: Disabled. (default)					

REMOTE_INPUT_VALID2_CNFG - Input Clocks Validity Configuration 2

Address: 4DH							
Type: Read / Write							
Default Value: XX111111							
7	6	5	4	3	2	1	0
-	-	IN14_VALID	IN13_VALID	IN12_VALID	IN11_VALID	IN10_VALID	IN9_VALID
Bit	Name	Description					
7 - 6	-	Reserved.					
5 - 0	INn_VALID	This bit controls whether the corresponding INn is allowed to be locked for automatic selection. Here n is any one of 14 to 9. 0: Enabled. 1: Disabled. (default)					

PRIORITY_TABLE1_STS - Priority Status 1 *

Address: 4EH							
Type: Read							
Default Value: 00000000							
7	6	5	4	3	2	1	0
HIGHEST_PRIORITY_VALIDATED3	HIGHEST_PRIORITY_VALIDATED2	HIGHEST_PRIORITY_VALIDATED1	HIGHEST_PRIORITY_VALIDATED0	CURRENTLY_SELECTED_INPUT3	CURRENTLY_SELECTED_INPUT2	CURRENTLY_SELECTED_INPUT1	CURRENTLY_SELECTED_INPUT0
Bit	Name	Description					
7 - 4	HIGHEST_PRIORITY_VALIDATED[3:0]	These bits indicate a qualified input clock with the highest priority. 0000: No input clock is qualified. (default) 0001: IN1. 0010: IN2. 1101: IN13. 1110: IN14. 1111: Reserved. Note that the input clock is indicated by these bits only when the corresponding INn (b7-0, 4CH) or INn (b5-0, 4DH) bit is '0'.					
3 - 0	CURRENTLY_SELECTED_INPUT[3:0]	These bits indicate the T0/T4 selected input clock. 0000: No input clock is selected; or the T4 selected input clock is the T0 DPLL output. (default) 0001: IN1 is selected. 0010: IN2 is selected. 1101: IN13 is selected. 1110: IN14 is selected. 1111: Reserved. Note that the input clock is indicated by these bits only when the corresponding INn (b7-0, 4CH) or INn (b5-0, 4DH) bit is '0'.					

PRIORITY_TABLE2_STS - Priority Status 2 *

Address: 4FH							
Type: Read							
Default Value: 00000000							
7	6	5	4	3	2	1	0
THIRD_HIGHEST_PRIORITY_VALIDATED3	THIRD_HIGHEST_PRIORITY_VALIDATED2	THIRD_HIGHEST_PRIORITY_VALIDATED1	THIRD_HIGHEST_PRIORITY_VALIDATED0	SECOND_HIGHEST_PRIORITY_VALIDATED3	SECOND_HIGHEST_PRIORITY_VALIDATED2	SECOND_HIGHEST_PRIORITY_VALIDATED1	SECOND_HIGHEST_PRIORITY_VALIDATED0
Bit	Name	Description					
7 - 4	THIRD_HIGHEST_PRIORITY_VALIDATED[3:0]	These bits indicate a qualified input clock with the third highest priority. 0000: No input clock is qualified. (default) 0001: IN1. 0010: IN2. 1101: IN13. 1110: IN14. 1111: Reserved. Note that the input clock is indicated by these bits only when the corresponding INn (b7-0, 4CH) or INn (b5-0, 4DH) bit is '0'.					
3 - 0	SECOND_HIGHEST_PRIORITY_VALIDATED[3:0]	These bits indicate a qualified input clock with the second highest priority. 0000: No input clock is qualified. (default) 0001: IN1. 0010: IN2. 1101: IN13. 1110: IN14. 1111: Reserved. Note that the input clock is indicated by these bits only when the corresponding INn (b7-0, 4CH) or INn (b5-0, 4DH) bit is '0'.					

T0_INPUT_SEL_CNFG - T0 Selected Input Clock Configuration

Address: 50H							
Type: Read / Write							
Default Value: XXXX0000							
7	6	5	4	3	2	1	0
-	-	-	-	T0_INPUT_SEL3	T0_INPUT_SEL2	T0_INPUT_SEL1	T0_INPUT_SEL0
Bit	Name	Description					
7 - 4	-	Reserved.					
3 - 0	T0_INPUT_SEL[3:0]	This bit determines T0 input clock selection. It is valid only when the EXT_SW bit (b4, 0BH) is '0'. 0000: Automatic selection. (default) 0001: Forced selection - IN1 is selected. 0010: Forced selection - IN2 is selected. 1101: Forced selection - IN13 is selected. 1110: Forced selection - IN14 is selected. 1111: Reserved.					

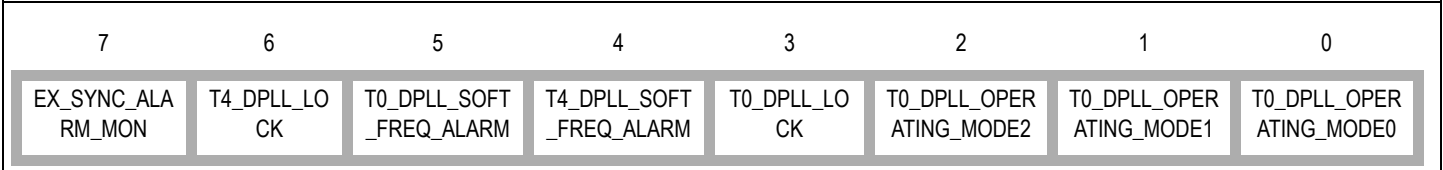
T4_INPUT_SEL_CNFG - T4 Selected Input Clock Configuration

Address: 51H							
Type: Read / Write							
Default Value: X0000000							
7	6	5	4	3	2	1	0
-	T4_LOCK_T0	T0_FOR_T4	T4_TEST_T0_PH	T4_INPUT_SEL3	T4_INPUT_SEL2	T4_INPUT_SEL1	T4_INPUT_SELO
Bit	Name	Description					
7	-	Reserved.					
6	T4_LOCK_T0	This bit determines whether the T4 DPLL locks to a T0 DPLL output or locks independently from the T0 DPLL. 0: Independently from the T0 path. (default) 1: Locks to a 77.76 MHz or 8 kHz signal from the T0 DPLL 77.76 MHz path.					
5	T0_FOR_T4	This bit is valid only when the T4_LOCK_T0 bit (b6, 51H) is '1'. It determines whether a 77.76 MHz or 8 kHz signal from the T0 DPLL 77.76 MHz path is selected by the T4 DPLL. 0: 77.76 MHz. (default) 1: 8 kHz.					
4	T4_TEST_T0_PH	This bit determines whether T4 selected input clock is compared with the feedback signal of the T4 DPLL for T4 DPLL locking or is compared with the T0 selected input clock to get the phase difference between T0 and T4 selected input clocks. 0: The T4 DPLL output. (default) 1: The T0 selected input clock.					
3 - 0	T4_INPUT_SEL[3:0]	These bits are valid only when the T4_LOCK_T0 bit (b6, 51H) is '0'. They determines the T4 DPLL input clock selection. 0000: Automatic selection. (default) 0001: Forced selection - IN1 is selected. 0010: Forced selection - IN2 is selected. 1101: Forced selection - IN13 is selected. 1110: Forced selection - IN14 is selected. 1111: Reserved.					

7.2.6 T0 / T4 DPLL STATE MACHINE CONTROL REGISTERS

OPERATING_STS - DPLL Operating Status

Address: 52H
 Type: Read
 Default Value: 10000001



Bit	Name	Description
7	EX_SYNC_ALARM_MON	This bit indicates whether the frame sync input signal is in external sync alarm status. 0: No external sync alarm. 1: In external sync alarm status. (default)
6	T4_DPLL_LOCK	This bit indicates the T4 DPLL locking status. 0: Unlocked. (default) 1: Locked.
5	T0_DPLL_SOFT_FREQ_ALARM	This bit indicates whether the T0 DPLL is in soft alarm status. 0: No T0 DPLL soft alarm. (default) 1: In T0 DPLL soft alarm status.
4	T4_DPLL_SOFT_FREQ_ALARM	This bit indicates whether the T4 DPLL is in soft alarm status. 0: No T4 DPLL soft alarm. (default) 1: In T4 DPLL soft alarm status.
3	T0_DPLL_LOCK	This bit indicates the T0 DPLL locking status. 0: Unlocked. (default) 1: Locked.
2 - 0	T0_DPLL_OPERATING_MODE[2:0]	These bits indicate the current operating mode of T0 DPLL. 000: Reserved. 001: Free-Run. (default) 010: Holdover. 011: Reserved. 100: Locked. 101: Pre-Locked2. 110: Pre-Locked. 111: Lost-Phase.

T0_OPERATING_MODE_CNFG - T0 DPLL Operating Mode Configuration

Address: 53H							
Type: Read / Write							
Default Value: XXXXX000							
7	6	5	4	3	2	1	0
-	-	-	-	-	T0_OPERATING_MODE2	T0_OPERATING_MODE1	T0_OPERATING_MODE0
Bit	Name	Description					
7 - 3	-	Reserved.					
2 - 0	T0_OPERATING_MODE[2:0]	These bits control the T0 DPLL operating mode. 000: Automatic. (default) 001: Forced - Free-Run. 010: Forced - Holdover. 011: Reserved. 100: Forced - Locked. 101: Forced - Pre-Locked2. 110: Forced - Pre-Locked. 111: Forced - Lost-Phase.					

T4_OPERATING_MODE_CNFG - T4 DPLL Operating Mode Configuration

Address: 54H							
Type: Read / Write							
Default Value: XXXXX000							
7	6	5	4	3	2	1	0
-	-	-	-	-	T4_OPERATING_MODE2	T4_OPERATING_MODE1	T4_OPERATING_MODE0
Bit	Name	Description					
7 - 3	-	Reserved.					
2 - 0	T4_OPERATING_MODE[2:0]	These bits control the T4 DPLL operating mode. 000: Automatic. (default) 001: Forced - Free-Run. 010: Forced - Holdover. 011: Reserved. 100: Forced - Locked. 101, 110, 111: Reserved.					

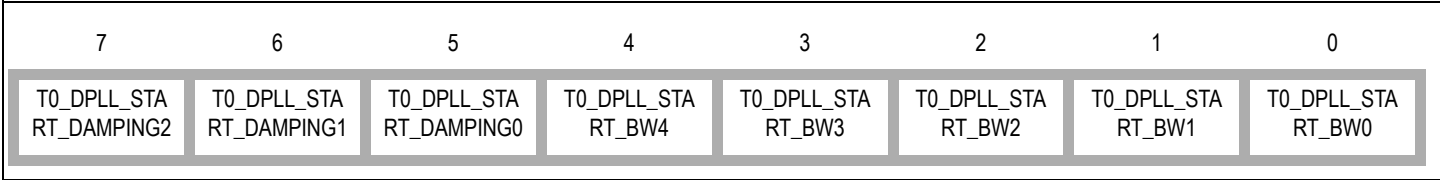
7.2.7 T0 / T4 DPLL & APLL CONFIGURATION REGISTERS

T0_DPLL_APLL_PATH_CNFG - T0 DPLL & APLL Path Configuration

Address: 55H							
Type: Read / Write							
Default Value: 00000X0X							
7	6	5	4	3	2	1	0
T0_APLL_PATH 3	T0_APLL_PA TH2	T0_APLL_PA TH1	T0_APLL_PA TH0	T0_GSM_OBSAI_ 16E1_16T1_SEL1	T0_GSM_OBSAI_ 16E1_16T1_SELO	T0_12E1_24T1_ E3_T3_SEL1	T0_12E1_24T1_ E3_T3_SELO
Bit	Name	Description					
7 - 4	T0_APLL_PATH[3:0]	These bits select an input to the T0 APLL. 0000: The output of T0 DPLL 77.76 MHz path. (default) 0001: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0010: The output of T0 DPLL 16E1/16T1 path. 0011: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 0100: The output of T4 DPLL 77.76 MHz path. 0101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T4 DPLL 16E1/16T1 path. 0111: The output of T4 DPLL GSM/GPS/16E1/16T1 path. 1000: T0 ETH path. 1100: T4 ETH path. 1101~1111: Reserved.					
3 - 2	T0_GSM_OBSAI_16E1_16T1_SEL[1:0]	These bits select an output clock from the T0 DPLL GSM/OBSAI/16E1/16T1 path. 00: 16E1. 01: 16T1. 10: GSM. 11: OBSAI. The default value of the T0_GSM_OBSAI_16E1_16T1_SELO bit is determined by the SONET/SDH pin during reset.					
1 - 0	T0_12E1_24T1_E3_T3_SEL[1:0]	These bits select an output clock from the T0 DPLL 12E1/24T1/E3/T3 path. 00: 12E1. 01: 24T1. 10: E3. 11: T3. The default value of the T0_12E1_24T1_E3_T3_SELO bit is determined by the SONET/SDH pin during reset.					

T0_DPLL_START_BW_DAMPING_CNFG - T0 DPLL Start Bandwidth & Damping Factor Configuration

Address: 56H
 Type: Read / Write
 Default Value: 01101111



Bit	Name	Description
7 - 5	T0_DPLL_START_DAMPING[2:0]	These bits set the starting damping factor for T0 DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved.
4 - 0	T0_DPLL_START_BW[4:0]	These bits set the starting bandwidth for T0 DPLL. 00000: 0.5 mHz. 00001: 1 mHz. 00010: 2 mHz. 00011: 4 mHz. 00100: 8 mHz. 00101: 15 mHz. 00110: 30 mHz. 00111: 60 mHz. 01000: 0.1 Hz. 01001: 0.3 Hz. 01010: 0.6 Hz. 01011: 1.2 Hz. 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. (default) 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved.

T0_DPLL_ACQ_BW_DAMPING_CNFG - T0 DPLL Acquisition Bandwidth & Damping Factor Configuration

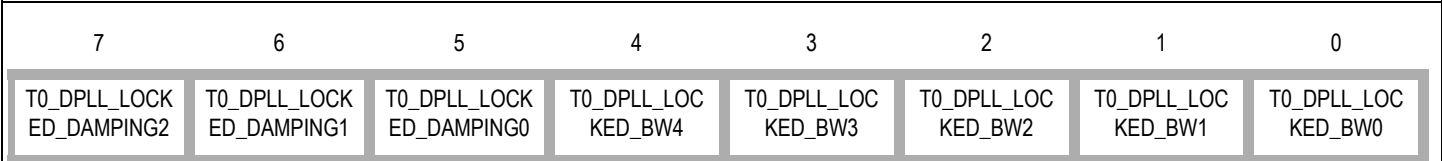
Address: 57H
 Type: Read / Write
 Default Value: 01101111

7	6	5	4	3	2	1	0
T0_DPLL_ACQ _DAMPING2	T0_DPLL_ACQ _DAMPING1	T0_DPLL_ACQ _DAMPING0	T0_DPLL_ACQ _BW4	T0_DPLL_ACQ _BW3	T0_DPLL_ACQ _BW2	T0_DPLL_ACQ _BW1	T0_DPLL_ACQ _BW0

Bit	Name	Description
7 - 5	T0_DPLL_ACQ_DAMPING[2:0]	These bits set the acquisition damping factor for T0 DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved.
4 - 0	T0_DPLL_ACQ_BW[4:0]	These bits set the acquisition bandwidth for T0 DPLL. 00000: 0.5 mHz. 00001: 1 mHz. 00010: 2 mHz. 00011: 4 mHz. 00100: 8 mHz. 00101: 15 mHz. 00110: 30 mHz. 00111: 60 mHz. 01000: 0.1 Hz. 01001: 0.3 Hz. 01010: 0.6 Hz. 01011: 1.2 Hz. 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. (default) 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved.

T0_DPLL_LOCKED_BW_DAMPING_CNFG - T0 DPLL Locked Bandwidth & Damping Factor Configuration

Address: 58H
 Type: Read / Write
 Default Value: 01101011



Bit	Name	Description
7 - 5	T0_DPLL_LOCKED_DAMPING[2:0]	These bits set the locked damping factor for T0 DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved.
4 - 0	T0_DPLL_LOCKED_BW[4:0]	These bits set the locked bandwidth for T0 DPLL. 00000: 0.5 mHz. 00001: 1 mHz. 00010: 2 mHz. 00011: 4 mHz. 00100: 8 mHz. 00101: 15 mHz. 00110: 30 mHz. 00111: 60 mHz. 01000: 0.1 Hz. 01001: 0.3 Hz. 01010: 0.6 Hz. 01011: 1.2 Hz. (default) 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved.

T0_BW_OVERSHOOT_CNFG - T0 DPLL Bandwidth Overshoot Configuration

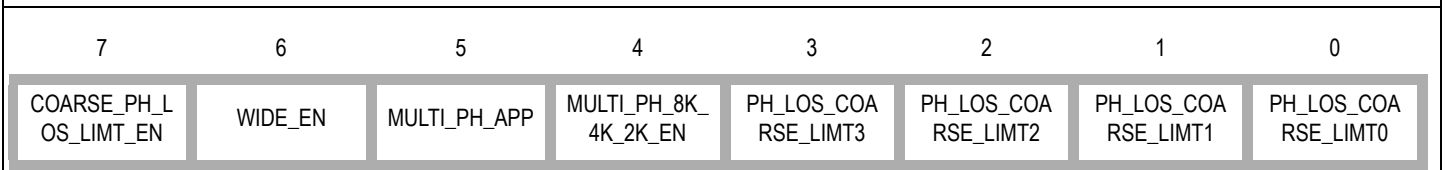
Address: 59H
 Type: Read / Write
 Default Value: 1XXX1XXX

7	6	5	4	3	2	1	0
AUTO_BW_SEL	-	-	-	T0_LIMT	-	-	-

Bit	Name	Description
7	AUTO_BW_SEL	This bit determines whether starting or acquisition bandwidth / damping factor is used for T0 DPLL. 0: The starting and acquisition bandwidths / damping factors are not used. Only the locked bandwidth / damping factor is used regardless of the T0 DPLL locking stage. 1: The starting, acquisition or locked bandwidth / damping factor is used automatically depending on different T0 DPLL locking stages. (default)
6 - 4	-	Reserved.
3	T0_LIMT	This bit determines whether the integral path value is frozen when the T0 DPLL hard limit is reached. 0: Not frozen. 1: Frozen. It will minimize the subsequent overshoot when T0 DPLL is pulling in. (default)
2 - 0	-	Reserved.

PHASE_LOSS_COARSE_LIMIT_CNFG - Phase Loss Coarse Detector Limit Configuration *

Address: 5AH
 Type: Read / Write
 Default Value: 10000101



Bit	Name	Description																					
7	COARSE_PH_LOS_LIMT_EN	This bit controls whether the occurrence of the coarse phase loss will result in the T0/T4 DPLL unlocked. 0: Disabled. 1: Enabled. (default)																					
6	WIDE_EN	Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH).																					
5	MULTI_PH_APP	This bit determines whether the PFD output of T0/T4 DPLL is limited to ±1 UI or is limited to the coarse phase limit. 0: Limited to ±1 UI. (default) 1: Limited to the coarse phase limit. When the selected input clock is of 2 kHz, 4 kHz or 8 kHz, the coarse phase limit depends on the MULTI_PH_8K_4K_2K_EN bit, the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits; when the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH) for details.																					
4	MULTI_PH_8K_4K_2K_EN	This bit, together with the WIDE_EN bit (b6, 5AH) and the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH), determines the coarse phase limit when the selected input clock is of 2 kHz, 4 kHz or 8 kHz. When the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. <table border="1" style="margin: 10px auto; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="width: 15%;">Selected Input Clock</th> <th style="width: 15%;">MULTI_PH_8K_4K_2K_EN</th> <th style="width: 15%;">WIDE_EN</th> <th style="width: 55%;">Coarse Phase Limit</th> </tr> </thead> <tbody> <tr> <td rowspan="2">2 kHz, 4 kHz or 8 kHz</td> <td>0</td> <td>don't-care</td> <td>±1 UI</td> </tr> <tr> <td rowspan="2">1</td> <td>0</td> <td>±1 UI</td> </tr> <tr> <td rowspan="2">other than 2 kHz, 4 kHz and 8 kHz</td> <td rowspan="2">don't-care</td> <td>1</td> <td>set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH).</td> </tr> <tr> <td>0</td> <td>±1 UI</td> </tr> <tr> <td></td> <td></td> <td>1</td> <td>set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH).</td> </tr> </tbody> </table>	Selected Input Clock	MULTI_PH_8K_4K_2K_EN	WIDE_EN	Coarse Phase Limit	2 kHz, 4 kHz or 8 kHz	0	don't-care	±1 UI	1	0	±1 UI	other than 2 kHz, 4 kHz and 8 kHz	don't-care	1	set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH).	0	±1 UI			1	set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH).
Selected Input Clock	MULTI_PH_8K_4K_2K_EN	WIDE_EN	Coarse Phase Limit																				
2 kHz, 4 kHz or 8 kHz	0	don't-care	±1 UI																				
	1	0	±1 UI																				
other than 2 kHz, 4 kHz and 8 kHz		don't-care	1	set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH).																			
	0		±1 UI																				
		1	set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH).																				
3 - 0	PH_LOS_COARSE_LIMT[3:0]	These bit set the coarse phase limit. The limit is used only in some cases. Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH). 0000: ±1 UI. 0001: ±3 UI. 0010: ±7 UI. 0011: ±15 UI. 0100: ±31 UI. 0101: ±63 UI. (default) 0110: ±127 UI. 0111: ±255 UI. 1000: ±511 UI. 1001: ±1023 UI (T0); Reserved (T4). 1010-1111: Reserved.																					

PHASE_LOSS_FINE_LIMIT_CNFG - Phase Loss Fine Detector Limit Configuration *

Address: 5BH							
Type: Read / Write							
Default Value: 10XXX010							
7	6	5	4	3	2	1	0
FINE_PH_LOS_LIMT_EN	FAST_LOS_SW	-	-	-	PH_LOS_FINE_LIMT2	PH_LOS_FINE_LIMT1	PH_LOS_FINE_LIMT0
Bit	Name	Description					
7	FINE_PH_LOS_LIMT_EN	This bit controls whether the occurrence of the fine phase loss will result in the T0/T4 DPLL unlocked. 0: Disabled. 1: Enabled. (default)					
6	FAST_LOS_SW	The value in this bit can be switched only when it is available for T0 path; this bit is always '1' when it is available for T4 path. This bit controls whether the occurrence of the fast loss will result in the T0/T4 DPLL unlocked. 0: Does not result in the T0 DPLL unlocked. T0 DPLL will enter Temp-Holdover mode automatically. (default) 1: Results in the T0/T4 DPLL unlocked. For T0 path, T0 DPLL will enter Lost-Phase mode if the T0 DPLL operating mode is switched automatically.					
5 - 3	-	Reserved.					
2 - 0	PH_LOS_FINE_LIMT[2:0]	These bits set a fine phase limit. 000: 0. 001: ± (45 ° ~ 90 °). 010: ± (90 ° ~ 180 °). (default) 011: ± (180 ° ~ 360 °). 100: ± (20 ns ~ 25 ns). 101: ± (60 ns ~ 65 ns). 110: ± (120 ns ~ 125 ns). 111: ± (950 ns ~ 955 ns).					

T0_HOLDOVER_MODE_CNFG - T0 DPLL Holdover Mode Configuration

Address: 5CH							
Type: Read / Write							
Default Value: 010001XX							
7	6	5	4	3	2	1	0
MAN_HOLD OVER	AUTO_AVG	FAST_AVG	READ_AVG	TEMP_HOLD OVER_MODE1	TEMP_HOLD OVER_MODE0	-	-
Bit	Name	Description					
7	MAN_HOLDOVER	Refer to the description of the FAST_AVG bit (b5, 5CH).					
6	AUTO_AVG	Refer to the description of the FAST_AVG bit (b5, 5CH).					
5	FAST_AVG	This bit, together with the AUTO_AVG bit (b6, 5CH) and the MAN_HOLDOVER bit (b7, 5CH), determines a frequency offset acquiring method in T0 DPLL Holdover Mode.					
		MAN_HOLDOVER	AUTO_AVG	FAST_AVG	Frequency Offset Acquiring Method		
		0	0	don't-care		Automatic Instantaneous	
			1	0	Automatic Slow Averaged (default)		
		1	don't-care		1	Automatic Fast Averaged	
		Manual					
4	READ_AVG	This bit controls the holdover frequency offset reading, which is read from the T0_HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH). 0: The value read from the T0_HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH) is equal to the one written to them. (default) 1: The value read from the T0_HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH) is not equal to the one written to them. The value is acquired by Automatic Slow Averaged method if the FAST_AVG bit (b5, 5CH) is '0'; or is acquired by Automatic Fast Averaged method if the FAST_AVG bit (b5, 5CH) is '1'.					
3 - 2	TEMP_HOLDOVER_MODE[1:0]	These bits determine the frequency offset acquiring method in T0 DPLL Temp-Holdover Mode. 00: The method is the same as that used in T0 DPLL Holdover mode. 01: Automatic Instantaneous. (default) 10: Automatic Fast Averaged. 11: Automatic Slow Averaged.					
1 - 0	-	Reserved.					

T0_HOLDOVER_FREQ[7:0]_CNFG - T0 DPLL Holdover Frequency Configuration 1

Address: 5DH							
Type: Read / Write							
Default Value: 00000000							
7	6	5	4	3	2	1	0
T0_HOLD OVER _FREQ7	T0_HOLD OVER _FREQ6	T0_HOLD OVER _FREQ5	T0_HOLD OVE R_FREQ4	T0_HOLD OVE R_FREQ3	T0_HOLD OVE R_FREQ2	T0_HOLD OVE R_FREQ1	T0_HOLD OVE R_FREQ0
Bit	Name	Description					
7 - 0	T0_HOLDOVER_FREQ[7:0]	Refer to the description of the T0_HOLDOVER_FREQ[23:16] bits (b7~0, 5FH).					

T0_HOLDOVER_FREQ[15:8]_CNFG - T0 DPLL Holdover Frequency Configuration 2

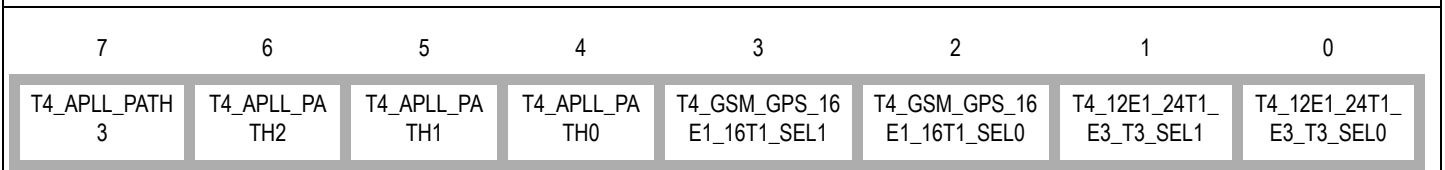
Address: 5EH							
Type: Read / Write							
Default Value: 00000000							
7	6	5	4	3	2	1	0
T0_HOLDOVER_FREQ15	T0_HOLDOVER_FREQ14	T0_HOLDOVER_FREQ13	T0_HOLDOVER_FREQ12	T0_HOLDOVER_FREQ11	T0_HOLDOVER_FREQ10	T0_HOLDOVER_FREQ9	T0_HOLDOVER_FREQ8
Bit	Name	Description					
7 - 0	T0_HOLDOVER_FREQ[15:8]	Refer to the description of the T0_HOLDOVER_FREQ[23:16] bits (b7~0, 5FH).					

T0_HOLDOVER_FREQ[23:16]_CNFG - T0 DPLL Holdover Frequency Configuration 3

Address: 5FH							
Type: Read / Write							
Default Value: 00000000							
7	6	5	4	3	2	1	0
T0_HOLDOVER_FREQ23	T0_HOLDOVER_FREQ22	T0_HOLDOVER_FREQ21	T0_HOLDOVER_FREQ20	T0_HOLDOVER_FREQ19	T0_HOLDOVER_FREQ18	T0_HOLDOVER_FREQ17	T0_HOLDOVER_FREQ16
Bit	Name	Description					
7 - 0	T0_HOLDOVER_FREQ[23:16]	The T0_HOLDOVER_FREQ[23:0] bits represent a 2's complement signed integer. In T0 DPLL Holdover mode, the value written to these bits multiplied by 0.000011 is the frequency offset set manually; the value read from these bits multiplied by 0.000011 is the frequency offset automatically slow or fast averaged or manually set, as determined by the READ_AVG bit (b4, 5CH) and the FAST_AVG bit (b5, 5CH).					

T4_DPLL_APLL_PATH_CNFG - T4 DPLL & APLL Path Configuration

Address: 60H
 Type: Read / Write
 Default Value: 01000X0X



Bit	Name	Description
7 - 4	T4_APLL_PATH[3:0]	These bits select an input to the T4 APLL. 0000: The output of T0 DPLL 77.76 MHz path. 0001: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0010: The output of T0 DPLL 16E1/16T1 path. 0011: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 0100: The output of T4 DPLL 77.76 MHz path. (default) 0101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T4 DPLL 16E1/16T1 path. 0111: The output of T4 DPLL GSM/GPS/16E1/16T1 path. 1000: T0 ETH path. 1100: T4 ETH path. 1101~1111: Reserved.
3 - 2	T4_GSM_GPS_16E1_16T1_SEL[1:0]	These bits select an output clock from the T4 DPLL GSM/GPS/16E1/16T1 path. 00: 16E1. 01: 16T1. 10: GSM. 11: GPS. The default value of the T0_GSM_GPS_16E1_16T1_SELO bit is determined by the SONET/SDH pin during reset.
1 - 0	T4_12E1_24T1_E3_T3_SEL[1:0]	These bits select an output clock from the T4 DPLL 12E1/24T1/E3/T3 path. 00: 12E1. 01: 24T1. 10: E3. 11: T3. The default value of the T4_12E1_24T1_E3_T3_SELO bit is determined by the SONET/SDH pin during reset.

T4_DPLL_LOCKED_BW_DAMPING_CNFG - T4 DPLL Locked Bandwidth & Damping Factor Configuration

Address: 61H
 Type: Read / Write
 Default Value: 011XXX00

7	6	5	4	3	2	1	0
T4_DPLL_LOCKED_DAMPING2	T4_DPLL_LOCKED_DAMPING1	T4_DPLL_LOCKED_DAMPING0	-	-	-	T4_DPLL_LOCKED_BW1	T4_DPLL_LOCKED_BW0

Bit	Name	Description
7 - 5	T4_DPLL_LOCKED_DAMPING[2:0]	These bits set the locked damping factor for T4 DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved.
4 - 2	-	Reserved.
1 - 0	T4_DPLL_LOCKED_BW[1:0]	These bits set the locked bandwidth for T4 DPLL. 00: 18 Hz. (default) 01: 35 Hz. 10: 70 Hz. 11: 560 Hz.

CURRENT_DPLL_FREQ[7:0]_STS - DPLL Current Frequency Status 1 *

Address: 62H
 Type: Read
 Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_DPLL_FREQ7	CURRENT_DPLL_FREQ6	CURRENT_DPLL_FREQ5	CURRENT_DPLL_FREQ4	CURRENT_DPLL_FREQ3	CURRENT_DPLL_FREQ2	CURRENT_DPLL_FREQ1	CURRENT_DPLL_FREQ0

Bit	Name	Description
7 - 0	CURRENT_DPLL_FREQ[7:0]	Refer to the description of the CURRENT_DPLL_FREQ[23:16] bits (b7~0, 64H).

CURRENT_DPLL_FREQ[15:8]_STS - DPLL Current Frequency Status 2 *

Address: 63H
 Type: Read
 Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_DPLL_FREQ15	CURRENT_DPLL_FREQ14	CURRENT_DPLL_FREQ13	CURRENT_DPLL_FREQ12	CURRENT_DPLL_FREQ11	CURRENT_DPLL_FREQ10	CURRENT_DPLL_FREQ9	CURRENT_DPLL_FREQ8

Bit	Name	Description
7 - 0	CURRENT_DPLL_FREQ[15:8]	Refer to the description of the CURRENT_DPLL_FREQ[23:16] bits (b7~0, 64H).

CURRENT_DPLL_FREQ[23:16]_STS - DPLL Current Frequency Status 3 *

Address: 64H Type: Read Default Value: 00000000							
7	6	5	4	3	2	1	0
CURRENT_DP LL_FREQ23	CURRENT_DP LL_FREQ22	CURRENT_DP LL_FREQ21	CURRENT_DP LL_FREQ20	CURRENT_DP LL_FREQ19	CURRENT_DP LL_FREQ18	CURRENT_DP LL_FREQ17	CURRENT_DP LL_FREQ16
Bit	Name	Description					
7 - 0	CURRENT_DPLL_FREQ[23:16]	The CURRENT_DPLL_FREQ[23:0] bits represent a 2's complement signed integer. If the value in these bits is multiplied by 0.000011, the current frequency offset of the T0/T4 DPLL output in ppm with respect to the master clock will be obtained.					

DPLL_FREQ_SOFT_LIMIT_CNFG - DPLL Soft Limit Configuration

Address: 65H Type: Read / Write Default Value: 10001100							
7	6	5	4	3	2	1	0
FREQ_LIMIT_P H_LOS	DPLL_FREQ_S OFT_LIMIT6	DPLL_FREQ_S OFT_LIMIT5	DPLL_FREQ_S OFT_LIMIT4	DPLL_FREQ_S OFT_LIMIT3	DPLL_FREQ_S OFT_LIMIT2	DPLL_FREQ_S OFT_LIMIT1	DPLL_FREQ_S OFT_LIMIT0
Bit	Name	Description					
7	FREQ_LIMIT_PH_LOS	This bit determines whether the T0/T4 DPLL in hard alarm status will result in it unlocked. 0: Disabled. 1: Enabled. (default)					
6 - 0	DPLL_FREQ_SOFT_LIMIT[6:0]	These bits represent an unsigned integer. If the value is multiplied by 0.724, the DPLL soft limit for T0 and T4 paths in ppm will be obtained. The DPLL soft limit is symmetrical about zero.					

DPLL_FREQ_HARD_LIMIT[7:0]_CNFG - DPLL Hard Limit Configuration 1

Address: 66H Type: Read / Write Default Value: 10101011							
7	6	5	4	3	2	1	0
DPLL_FREQ_H ARD_LIMIT7	DPLL_FREQ_H ARD_LIMIT6	DPLL_FREQ_H ARD_LIMIT5	DPLL_FREQ_H ARD_LIMIT4	DPLL_FREQ_H ARD_LIMIT3	DPLL_FREQ_H ARD_LIMIT2	DPLL_FREQ_H ARD_LIMIT1	DPLL_FREQ_H ARD_LIMIT0
Bit	Name	Description					
7 - 0	DPLL_FREQ_HARD_LIMIT[7:0]	Refer to the description of the DPLL_FREQ_HARD_LIMIT[15:8] bits (b7~0, 67H).					

DPLL_FREQ_HARD_LIMIT[15:8]_CNFG - DPLL Hard Limit Configuration 2

Address: 67H
 Type: Read / Write
 Default Value: 00011001

7	6	5	4	3	2	1	0
DPLL_FREQ_H ARD_LIMT15	DPLL_FREQ_H ARD_LIMT14	DPLL_FREQ_H ARD_LIMT13	DPLL_FREQ_H ARD_LIMT12	DPLL_FREQ_H ARD_LIMT11	DPLL_FREQ_H ARD_LIMT10	DPLL_FREQ_H ARD_LIMT9	DPLL_FREQ_H ARD_LIMT8

Bit	Name	Description
7 - 0	DPLL_FREQ_HARD_LIMIT[15:8]	The DPLL_FREQ_HARD_LIMIT[15:0] bits represent an unsigned integer. If the value is multiplied by 0.0014, the DPLL hard limit for T0 and T4 paths in ppm will be obtained. The DPLL hard limit is symmetrical about zero.

CURRENT_DPLL_PHASE[7:0]_STS - DPLL Current Phase Status 1 *

Address: 68H
 Type: Read
 Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_PH _DATA7	CURRENT_PH _DATA6	CURRENT_PH _DATA5	CURRENT_PH _DATA4	CURRENT_PH _DATA3	CURRENT_PH _DATA2	CURRENT_PH _DATA1	CURRENT_PH _DATA0

Bit	Name	Description
7 - 0	CURRENT_PH_DATA[7:0]	Refer to the description of the CURRENT_PH_DATA[15:8] bits (b7~0, 69H).

CURRENT_DPLL_PHASE[15:8]_STS - DPLL Current Phase Status 2 *

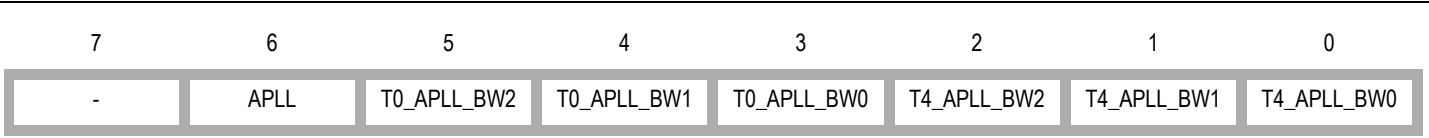
Address: 69H
 Type: Read
 Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_PH _DATA15	CURRENT_PH _DATA14	CURRENT_PH _DATA13	CURRENT_PH _DATA12	CURRENT_PH _DATA11	CURRENT_PH _DATA10	CURRENT_PH _DATA9	CURRENT_PH _DATA8

Bit	Name	Description
7 - 0	CURRENT_PH_DATA[15:8]	The CURRENT_PH_DATA[15:0] bits represent a 2's complement signed integer. If the value is multiplied by 0.61, the averaged phase error of the T0/T4 DPLL feedback with respect to the selected input clock in ns will be obtained.

T0_T4_APLL_BW_CNFG - T0 / T4 APLL Bandwidth Configuration

Address: 6AH
 Type: Read / Write
 Default Value: 10011011



Bit	Name	Description
7	-	Reserved.
6	APLL Settings	For best jitter performance, the following bits in the MS_SL_CTRL_CNFG, T0_T4_APLL_BW_CNFG and APLL_CNFG registers must be set. Bit 7 to Bit 3 of MS_SEL_CTRL_CNFG register (address 13H) must be set to 01010. Bit 6 to Bit 0 of T0_T4_APLL_BW_CNFG (address 6AH) must be set to 1010010. Bit 7 of APLL_CNFG (address 77H) must be set to 0.
5 - 3	T0_APLL_BW[2:0]	These bits set the bandwidth for T0 APLL. 000: 10 kHz. 001: 20 kHz. 010: 50 kHz. 011: 100 kHz. 100: 200 kHz. 101: 500 kHz. 110: 1 MHz. 111: 2 MHz.
2 - 0	T4_APLL_BW[2:0]	These bits set the bandwidth for T4 APLL. 000: 10 kHz. 001: 20 kHz. 010: 50 kHz. 011: 100 kHz. 100: 200 kHz. 101: 500 kHz. 110: 1 MHz. 111: 2 MHz.

7.2.8 OUTPUT CONFIGURATION REGISTERS

OUT1_FREQ_CNFG - Output Clock 1 Frequency Configuration

Address: 6BH							
Type: Read / Write							
Default Value: 00001011							
7	6	5	4	3	2	1	0
OUT1_PATH_S EL3	OUT1_PATH_S EL2	OUT1_PATH_S EL1	OUT1_PATH_S EL0	OUT1_DIVIDER 3	OUT1_DIVIDER 2	OUT1_DIVIDER 1	OUT1_DIVIDER 0
Bit	Name	Description					
7 - 4	OUT1_PATH_SEL[3:0]	These bits select an input to OUT1. 0000 ~ 0010: The output of T0 APLL. (default: 0000) 0011: T0 DPLL ETH path 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1010: The output of T4 APLL. 1011: T4 DPLL ETH path. 1100: The output of T4 DPLL 77.76 MHz path. 1101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 1110: The output of T4 DPLL 16E1/16T1 path. 1111: The output of T4 DPLL GSM/GPS/16E1/16T1 path.					
3 - 0	OUT1_DIVIDER[3:0]	These bits select a division factor of the divider for OUT1. The output frequency is determined by the division factor and the signal derived from T0/T4 DPLL or T0/T4 APLL output (selected by the OUT1_PATH_SEL[3:0] bits (b7~4, 6BH)). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 25 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 26~Table 27 for the division factor selection.					

OUT2_FREQ_CNFG - Output Clock 2 Frequency Configuration

Address: 6CH							
Type: Read / Write							
Default Value: 00000110							
7	6	5	4	3	2	1	0
OUT2_PATH_S EL3	OUT2_PATH_S EL2	OUT2_PATH_S EL1	OUT2_PATH_S EL0	OUT2_DIVIDER 3	OUT2_DIVIDER 2	OUT2_DIVIDER 1	OUT2_DIVIDER 0
Bit	Name	Description					
7 - 4	OUT2_PATH_SEL[3:0]	These bits select an input to OUT2. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1010: The output of T4 APLL. 1011: T4 DPLL ETH path. 1100: The output of T4 DPLL 77.76 MHz path. 1101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 1110: The output of T4 DPLL 16E1/16T1 path. 1111: The output of T4 DPLL GSM/GPS/16E1/16T1 path.					
3 - 0	OUT2_DIVIDER[3:0]	These bits select a division factor of the divider for OUT2. The output frequency is determined by the division factor and the signal derived from T0/T4 DPLL or T0/T4 APLL output (selected by the OUT2_PATH_SEL[3:0] bits (b7~4, 6CH)). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 25 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 26~Table 27 for the division factor selection.					

OUT3_FREQ_CNFG - Output Clock 3 Frequency Configuration

Address: 6DH							
Type: Read / Write							
Default Value: 00001000							
7	6	5	4	3	2	1	0
OUT3_PATH_S EL3	OUT3_PATH_S EL2	OUT3_PATH_S EL1	OUT3_PATH_S EL0	OUT3_DIVIDER 3	OUT3_DIVIDER 2	OUT3_DIVIDER 1	OUT3_DIVIDER 0
Bit	Name	Description					
7 - 4	OUT3_PATH_SEL[3:0]	These bits select an input to OUT3. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1010: The output of T4 APLL. 1011: T4 DPLL ETH path. 1100: The output of T4 DPLL 77.76 MHz path. 1101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 1110: The output of T4 DPLL 16E1/16T1 path. 1111: The output of T4 DPLL GSM/GPS/16E1/16T1 path.					
3 - 0	OUT3_DIVIDER[3:0]	These bits select a division factor of the divider for OUT3. The output frequency is determined by the division factor and the signal derived from T0/T4 DPLL or T0/T4 APLL output (selected by the OUT3_PATH_SEL[3:0] bits (b7~4, 6DH)). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 25 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 26~Table 27 for the division factor selection.					

OUT4_FREQ_CNFG - Output Clock 4 Frequency Configuration

Address: 6EH							
Type: Read / Write							
Default Value: 00000110							
7	6	5	4	3	2	1	0
OUT4_PATH_S EL3	OUT4_PATH_S EL2	OUT4_PATH_S EL1	OUT4_PATH_S EL0	OUT4_DIVIDER 3	OUT4_DIVIDER 2	OUT4_DIVIDER 1	OUT4_DIVIDER 0
Bit	Name	Description					
7 - 4	OUT4_PATH_SEL[3:0]	These bits select an input to OUT4. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1010: The output of T4 APLL. 1011: T4 DPLL ETH path. 1100: The output of T4 DPLL 77.76 MHz path. 1101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 1110: The output of T4 DPLL 16E1/16T1 path. 1111: The output of T4 DPLL GSM/GPS/16E1/16T1 path.					
3 - 0	OUT4_DIVIDER[3:0]	These bits select a division factor of the divider for OUT4. The output frequency is determined by the division factor and the signal derived from T0/T4 DPLL or T0/T4 APLL output (selected by the OUT4_PATH_SEL[3:0] bits (b7~4, 6EH)). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 25 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 26~Table 27 for the division factor selection.					

OUT5_FREQ_CNFG - Output Clock 5 Frequency Configuration

Address: 6FH
 Type: Read / Write
 Default Value: 00000100

7	6	5	4	3	2	1	0
OUT5_PATH_S EL3	OUT5_PATH_S EL2	OUT5_PATH_S EL1	OUT5_PATH_S EL0	OUT5_DIVIDER 3	OUT5_DIVIDER 2	OUT5_DIVIDER 1	OUT5_DIVIDER 0

Bit	Name	Description
7 - 4	OUT5_PATH_SEL[3:0]	These bits select an input to OUT5. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1010: The output of T4 APLL. 1011: T4 DPLL ETH path. 1100: The output of T4 DPLL 77.76 MHz path. 1101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 1110: The output of T4 DPLL 16E1/16T1 path. 1111: The output of T4 DPLL GSM/GPS/16E1/16T1 path.
3 - 0	OUT5_DIVIDER[3:0]	These bits select a division factor of the divider for OUT5. The output frequency is determined by the division factor and the signal derived from T0/T4 DPLL or T0/T4 APLL output (selected by the OUT5_PATH_SEL[3:0] bits (b7~4, 6FH)). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 25 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 26~Table 27 for the division factor selection.

OUT6_FREQ_CNFG - Output Clock 6 Frequency Configuration

Address: 70H							
Type: Read / Write							
Default Value: 00000110							
7	6	5	4	3	2	1	0
OUT6_PATH_S EL3	OUT6_PATH_S EL2	OUT6_PATH_S EL1	OUT6_PATH_S EL0	OUT6_DIVIDER 3	OUT6_DIVIDER 2	OUT6_DIVIDER 1	OUT6_DIVIDER 0
Bit	Name	Description					
7 - 4	OUT6_PATH_SEL[3:0]	These bits select an input to OUT6. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1010: The output of T4 APLL. 1011: T4 DPLL ETH path. 1100: The output of T4 DPLL 77.76 MHz path. 1101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 1110: The output of T4 DPLL 16E1/16T1 path. 1111: The output of T4 DPLL GSM/GPS/16E1/16T1 path.					
3 - 0	OUT6_DIVIDER[3:0]	These bits select a division factor of the divider for OUT6. The output frequency is determined by the division factor and the signal derived from T0/T4 DPLL or T0/T4 APLL output (selected by the OUT6_PATH_SEL[3:0] bits (b7~4, 70H)). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 25 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 26~Table 27 for the division factor selection.					

OUT7_FREQ_CNFG - Output Clock 7 Frequency Configuration

Address: 71H							
Type: Read / Write							
Default Value: 00001000							
7	6	5	4	3	2	1	0
OUT7_PATH_S EL3	OUT7_PATH_S EL2	OUT7_PATH_S EL1	OUT7_PATH_S EL0	OUT7_DIVIDER 3	OUT7_DIVIDER 2	OUT7_DIVIDER 1	OUT7_DIVIDER 0
Bit	Name	Description					
7 - 4	OUT7_PATH_SEL[3:0]	These bits select an input to OUT7. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1010: The output of T4 APLL. 1011: T4 DPLL ETH path. 1100: The output of T4 DPLL 77.76 MHz path. 1101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 1110: The output of T4 DPLL 16E1/16T1 path. 1111: The output of T4 DPLL GSM/GPS/16E1/16T1 path.					
3 - 0	OUT7_DIVIDER[3:0]	These bits select a division factor of the divider for OUT7. The output frequency is determined by the division factor and the signal derived from T0/T4 DPLL or T0/T4 APLL output (selected by the OUT7_PATH_SEL[3:0] bits (b7~4, 71H)). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 25 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 26~Table 27 for the division factor selection.					

OUT8_FREQ_CNFG - Output Clock 8 Frequency Configuration & Output Clock 6, 7 & 9 Invert Configuration

Address: 72H																		
Type: Read / Write																		
Default Value: 01000000																		
7	6	5	4	3	2	1	0											
OUT8_PATH_SEL	OUT8_EN	T4_INPUT_FAIL	AMI_OUT_DUTY	400HZ_SEL	OUT9_INV	OUT7_INV	OUT6_INV											
Bit	Name	Description																
7	OUT8_PATH_SEL	These bits select an input to OUT8. 0: The output of T4 DPLL 77.76 MHz path. (default) 1: The output of T0 DPLL 77.76 MHz path.																
6	OUT8_EN	Refer to the description of the T4_INPUT_FAIL bit (b5, 72H).																
5	T4_INPUT_FAIL	This bit, together with the OUT8_EN bit (b6, 72H), determines whether a clock is enabled to be output on OUT8.																
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>OUT8_EN</th> <th>T4_INPUT_FAIL</th> <th>Output on OUT8</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">don't-care</td> <td style="text-align: center;">Output is disabled (output low).</td> </tr> <tr> <td rowspan="2" style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Output is enabled. (default)</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">Output is enabled when the T4 selected input clock does not fail. Output is disabled (output low) when the T4 selected input clock fails.</td> </tr> </tbody> </table>						OUT8_EN	T4_INPUT_FAIL	Output on OUT8	0	don't-care	Output is disabled (output low).	1	0	Output is enabled. (default)	1	Output is enabled when the T4 selected input clock does not fail. Output is disabled (output low) when the T4 selected input clock fails.
OUT8_EN	T4_INPUT_FAIL	Output on OUT8																
0	don't-care	Output is disabled (output low).																
1	0	Output is enabled. (default)																
	1	Output is enabled when the T4 selected input clock does not fail. Output is disabled (output low) when the T4 selected input clock fails.																
4	AMI_OUT_DUTY	This bit determines the duty cycle of the output on OUT8. 0: 50:50. (default) 1: 5:8.																
3	400HZ_SEL	This bit determines the frequency of the output on OUT8. 0: 64 kHz + 8 kHz. (default) 1: 64 kHz + 8 kHz + 0.4 kHz.																
2	OUT9_INV	This bit determines whether the output on OUT9 is inverted. 0: Not inverted. (default) 1: Inverted.																
1	OUT7_INV	This bit determines whether the output on OUT7 is inverted. 0: Not inverted. (default) 1: Inverted.																
0	OUT6_INV	This bit determines whether the output on OUT6 is inverted. 0: Not inverted. (default) 1: Inverted.																

OUT9_FREQ_CNFG - Output Clock 9 Frequency Configuration & Output Clock 1 ~ 5 Invert Configuration

Address: 73H							
Type: Read / Write							
Default Value: 01000000							
7	6	5	4	3	2	1	0
OUT9_PATH_SEL	OUT9_EN	T4_INPUT_FAIL	OUT5_INV	OUT4_INV	OUT3_INV	OUT2_INV	OUT1_INV
Bit	Name	Description					
7	OUT9_PATH_SEL	These bits select an input to OUT9. 0: The output of T4 DPLL 16E1/16T1 path. (default) 1: The output of T0 DPLL 16E1/16T1 path.					
6	OUT9_EN	Refer to the description of the T4_INPUT_FAIL bit (b5, 73H).					
5	T4_INPUT_FAIL	This bit, together with the OUT9_EN bit (b6, 73H), determines whether clock is enabled to output on OUT9.					
		OUT9_EN	T4_INPUT_FAIL	Output on OUT9			
		0	don't-care	Output is disabled (output low).			
		1	0	Output is enabled. (default)			
		1	1	Output is enabled when the T4 selected input clock does not fail. Output is disabled (output low) when the T4 selected input clock fails. (Whether the T4 selected input clock is switched or not, as long as the T4 selected input clock does not change to be invalid, the T4 selected input clock does not fail).			
4	OUT5_INV	This bit determines whether the output on OUT5 is inverted. 0: Not inverted. (default) 1: Inverted.					
3	OUT4_INV	This bit determines whether the output on OUT4 is inverted. 0: Not inverted. (default) 1: Inverted.					
2	OUT3_INV	This bit determines whether the output on OUT3 is inverted. 0: Not inverted. (default) 1: Inverted.					
1	OUT2_INV	This bit determines whether the output on OUT2 is inverted. 0: Not inverted. (default) 1: Inverted.					
0	OUT1_INV	This bit determines whether the output on OUT1 is inverted. 0: Not inverted. (default) 1: Inverted.					

FR_MFR_SYNC_CNFG - Frame Sync & Multiframe Sync Output Configuration

Address:74H
 Type: Read / Write
 Default Value: 01100000

7	6	5	4	3	2	1	0
IN_2K_4K_8K_I NV	8K_EN	2K_EN	2K_8K_PUL_P OSITION	8K_INV	8K_PUL	2K_INV	2K_PUL

Bit	Name	Description
7	IN_2K_4K_8K_INV	This bit determines whether the input clock is inverted before locked by the T0/T4 DPLL when the input clock is 2 kHz, 4 kHz or 8 kHz. 0: Not inverted. (default) 1: Inverted.
6	8K_EN	This bit determines whether an 8 kHz signal is enabled to be output on FRSYNC_8K. 0: Disabled. FRSYNC_8K outputs low. 1: Enabled. (default)
5	2K_EN	This bit determines whether a 2 kHz signal is enabled to be output on MFRSYNC_2K. 0: Disabled. MFRSYNC_2K outputs low. 1: Enabled. (default)
4	2K_8K_PUL_POSITION	This bit is valid only when FRSYNC_8K and/or MFRSYNC_2K output pulse; i.e., when one of the 8K_PUL bit (b2, 74H) and the 2K_PUL bit (b0, 74H) is '1' or when the 8K_PUL bit (b2, 74H) and the 2K_PUL bit (b0, 74H) are both '1'. It determines the pulse position referring to the standard 50:50 duty cycle. 0: Pulsed on the falling edge of the standard 50:50 duty cycle position. (default) 1: Pulsed on the rising edge of the standard 50:50 duty cycle position.
3	8K_INV	This bit determines whether the output on FRSYNC_8K is inverted. 0: Not inverted. (default) 1: Inverted.
2	8K_PUL	This bit determines whether the output on FRSYNC_8K is 50:50 duty cycle or pulsed. 0: 50:50 duty cycle. (default) 1: Pulsed. The pulse width is defined by the period of the output on OUT3.
1	2K_INV	This bit determines whether the output on MFRSYNC_2K is inverted. 0: Not inverted. (default) 1: Inverted.
0	2K_PUL	This bit determines whether the output on MFRSYNC_2K is 50:50 duty cycle or pulsed. 0: 50:50 duty cycle. (default) 1: Pulsed. The pulse width is defined by the period of the output on OUT3.

APLL Configuration

Address: 77H
 Type: Read / Write
 Default Value: 1xxxxxxx

7	6	5	4	3	2	1	0
APLL	-	-	-	-	-	-	-

Bit	Name	Description
7	APLL Settings	For best jitter performance, the following bits in the MS_SL_CTRL_CNFG, T0_T4_APLL_BW_CNFG and APLL_CNFG registers must be set. Bit 7 to Bit 3 of MS_SL_CTRL_CNFG register (address 13H) must be set to 01010. Bit 6 to Bit 0 of T0_T4_APLL_BW_CNFG (address 6AH) must be set to 1010010. Bit 7 of APLL_CNFG (address 77H) must be set to 0..
6 - 0	-	Reserved.

7.2.9 PHASE TRANSIENT MONITOR & PHASE OFFSET CONTROL REGISTERS

PHASE_MON_CNFG - Phase Transient Monitor Configuration

Address:78H
 Type: Read / Write
 Default Value: 0X000110

7	6	5	4	3	2	1	0
IN_NOISE_WIN DOW	-	-	-	-	-	-	-

Bit	Name	Description
7	IN_NOISE_WINDOW	This bit determines whether the input clock whose edge respect to the reference clock is outside $\pm 5\%$ is enabled to be selected for T0/T4 DPLL. 0: Disabled. (default) 1: Enabled.
6 - 0	-	Reserved.

PHASE_OFFSET[7:0]_CNFG - Phase Offset Configuration 1

Address:7AH
 Type: Read / Write
 Default Value: 00000000

7	6	5	4	3	2	1	0
PH_OFFSET7	PH_OFFSET6	PH_OFFSET5	PH_OFFSET4	PH_OFFSET3	PH_OFFSET2	PH_OFFSET1	PH_OFFSET0

Bit	Name	Description
7 - 0	PH_OFFSET[7:0]	Refer to the description of the PH_OFFSET[9:8] bits (b1~0, 7BH).

PHASE_OFFSET[9:8]_CNFG - Phase Offset Configuration 2

Address:7BH
 Type: Read / Write
 Default Value: 0XXXXX00

7	6	5	4	3	2	1	0
PH_OFFSET_EN	-	-	-	-	-	PH_OFFSET9	PH_OFFSET8

Bit	Name	Description
7	PH_OFFSET_EN	This bit determines whether the input-to-output phase offset is enabled. If the device is configured as the Master, the input-to-output phase offset: 0: Disabled. (default) 1: Enabled. If the device is configured as the Slave, the input-to-output phase offset is always enabled.
6 - 2	-	Reserved.
1 - 0	PH_OFFSET[9:8]	These bits represent a 2's complement signed integer. The input-to-output phase offset adjustment in ns is equal to this register value is multiplied by 0.61.

7.2.10 SYNCHRONIZATION CONFIGURATION REGISTERS

SYNC_MONITOR_CNFG - Sync Monitor Configuration

Address:7CH
 Type: Read / Write
 Default Value: X0101011

7	6	5	4	3	2	1	0
-	SYNC_MON_LIMT2	SYNC_MON_LIMT1	SYNC_MON_LIMT0	-	-	-	-

Bit	Name	Description
7	-	Reserved.
6 - 4	SYNC_MON_LIMT[2:0]	These bits set the limit for the external sync alarm. 000: ±1 UI. 001: ±2 UI. 010: ±3 UI. (default) 011: ±4 UI. 100: ±5 UI. 101: ±6 UI. 110: ±7 UI. 111: ±8 UI.
3 - 0	-	These bits must be set to '1011'.

SYNC_PHASE_CNFG - Sync Phase Configuration

Address:7DH
 Type: Read / Write
 Default Value: 00XXXX00

7	6	5	4	3	2	1	0
-	-	-	-	-	-	SYNC_PH11	SYNC_PH10

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	SYNC_PH1[1:0]	These bits set the sampling of EX_SYNC1 when EX_SYNC1 is enabled to synchronize the frame sync output signal. Nominally, the falling edge of EX_SYNC1 is aligned with the rising edge of the T0 selected input clock. 00: On target. (default) 01: 0.5 UI early. 10: 1 UI late. 11: 0.5 UI late.

8 THERMAL MANAGEMENT

The device operates over the industry temperature range -40°C ~ +85°C. To ensure the functionality and reliability of the device, the maximum junction temperature T_{jmax} should not exceed 125°C. In some applications, the device will consume more power and a thermal solution should be provided to ensure the junction temperature T_j does not exceed the T_{jmax} .

8.1 JUNCTION TEMPERATURE

Junction temperature T_j is the temperature of package typically at the geographical center of the chip where the device's electrical circuits are. It can be calculated as follows:

$$\text{Equation 1: } T_j = T_A + P \times \theta_{JA}$$

Where:

θ_{JA} = Junction-to-Ambient Thermal Resistance of the Package

T_j = Junction Temperature

T_A = Ambient Temperature

P = Device Power Consumption

In order to calculate junction temperature, an appropriate θ_{JA} must be used. The θ_{JA} is shown in Table 48:

Power consumption is the core power excluding the power dissipated in the loads. Table 47 provides power consumption in special environments.

Table 47: Power Consumption and Maximum Junction Temperature

Package	Power Consumption (W)	Operating Voltage (V)	T_A (°C)	Maximum Junction Temperature (°C)
TQFP/EQG100	1.2	3.465	85	125

8.2 EXAMPLE OF JUNCTION TEMPERATURE CALCULATION

Assume:

$$T_A = 85^\circ\text{C}$$

$$\theta_{JA} = 18.9^\circ\text{C/W (TQFP/EQG100 Soldered \& when airflow rate is 0 m/s)}$$

$$P = 1.2\text{W}$$

Table 48: Thermal Data

Package	Pin Count	Thermal Pad	θ_{JC} (°C/W)	θ_{JB} (°C/W)	θ_{JA} (°C/W) Air Flow in m/s					
					0	1	2	3	4	5
TQFP/EQG100	100	Yes/Exposed	16.1	34.2	35.8	31.1	29.5	28.6	27.9	27.4
TQFP/EQG100	100	Yes/Soldered*	16.1	1.3	18.9	14.6	13.5	12.9	12.6	12.4

*note: Simulated with 3 x 3 array of thermal vias.

The junction temperature T_j can be calculated as follows:

$$T_j = T_A + P \times \theta_{JA} = 85^\circ\text{C} + 1.2\text{W} \times 18.9^\circ\text{C/W} = 107.7^\circ\text{C}$$

The junction temperature of 107.7°C is below the maximum junction temperature of 125°C so no extra heat enhancement is required.

In some operation environments, the calculated junction temperature might exceed the maximum junction temperature of 125°C and an external thermal solution such as a heatsink is required.

8.3 HEATSINK EVALUATION

A heatsink is expanding the surface area of the device to which it is attached. θ_{JA} is now a combination of device case and heat-sink thermal resistance, as the heat flowing from the die junction to ambient goes through the package and the heatsink. θ_{JA} can be calculated as follows:

$$\text{Equation 2: } \theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$$

Where:

θ_{JC} = Junction-to-Case Thermal Resistance

θ_{CH} = Case-to-Heatsink Thermal Resistance

θ_{HA} = Heatsink-to-Ambient Thermal Resistance

$\theta_{CH} + \theta_{HA}$ determines which heatsink and heatsink attachment can be selected to ensure the junction temperature does not exceed the maximum junction temperature. According to Equation 1 and 2,

$\theta_{CH} + \theta_{HA}$ can be calculated as follows:

$$\text{Equation 3: } \theta_{CH} + \theta_{HA} = (T_j - T_A) / P - \theta_{JC}$$

Assume:

$$T_j = 125^\circ\text{C (} T_{jmax} \text{)}$$

$$T_A = 85^\circ\text{C}$$

$$P = 1.2\text{W}$$

$$\theta_{JC} = 16.1^\circ\text{C/W (TQFP/EQG100)}$$

$\theta_{CH} + \theta_{HA}$ can be calculated as follows:

$$\theta_{CH} + \theta_{HA} = (125^\circ\text{C} - 85^\circ\text{C}) / 1.2\text{W} - 16.1^\circ\text{C/W} = 17.2^\circ\text{C/W}$$

That is, if a heatsink and heatsink attachment whose $\theta_{CH} + \theta_{HA}$ is below or equal to 17.2°C/W is used in such operation environment, the junction temperature will not exceed the maximum junction temperature.

8.4 TQFP EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in [Figure 31](#). The solderable area on the PCB, as defined

by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

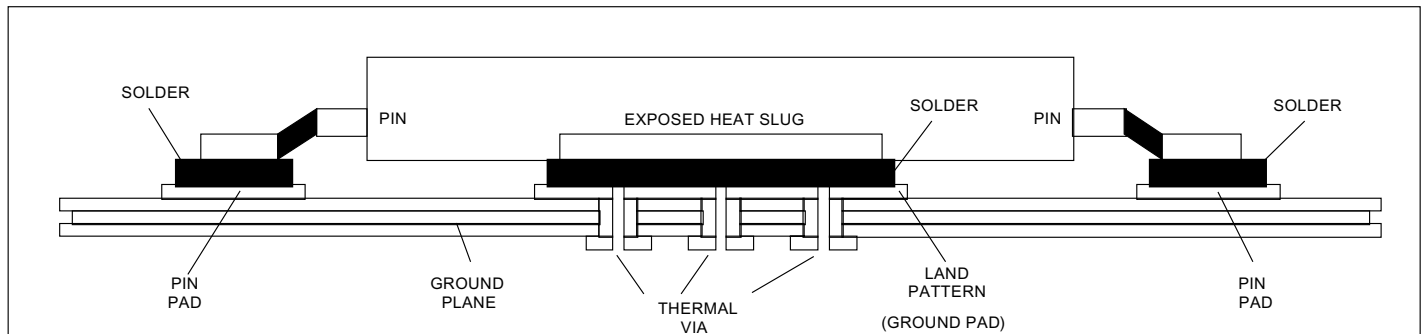


Figure 31. Assembly for Expose Pad thermal Release Path (Side View)

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as 'heat pipes'. The number of vias (i.e. 'heat pipes') are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias con-

nected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1 oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

9 ELECTRICAL SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATING

Table 49: Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage VDD	-0.5	5.5	V
V_{IN}	Input Voltage (non-supply pins)		5.5	V
V_{OUT}	Output Voltage (non-supply pins)		5.5	V
T_A	Ambient Operating Temperature Range	-40	+85	°C
T_{STOR}	Storage Temperature	-50	+150	°C
ESD Performance CDM Classification - Class II (JESD22 - C101E) HBM Classification - Class 2 (JESD22-A114)				

9.2 RECOMMENDED OPERATION CONDITIONS

Table 50: Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power Supply (DC voltage) VDD	3.135	3.3	3.465	V	
T_A	Ambient Temperature Range	-40		+85	°C	
I_{DD}	Supply Current			345	mA	Exclude the loading current and power
P_{TOT}	Total Power Dissipation			1.2	W	

9.3 I/O SPECIFICATIONS

9.3.1 AMI INPUT / OUTPUT PORT

9.3.1.1 Structure

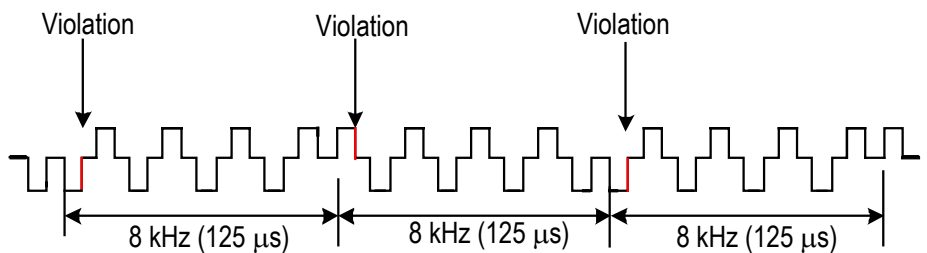


Figure 32. 64 kHz + 8 kHz Signal Structure

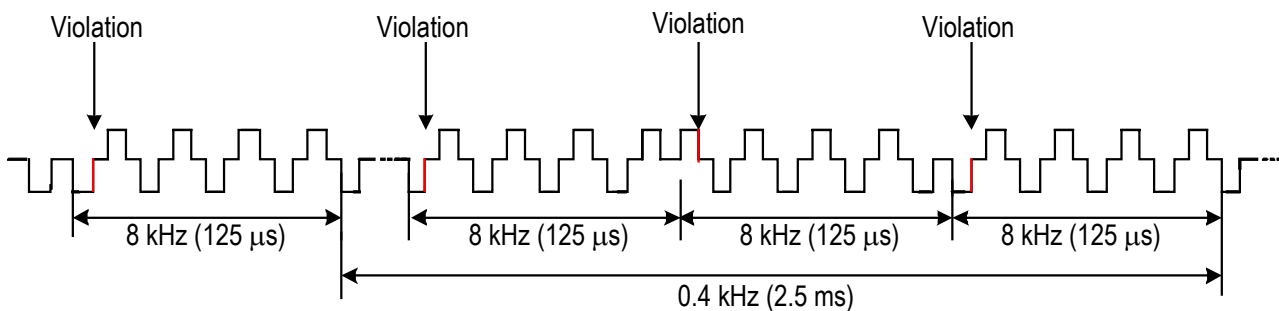


Figure 33. 64 kHz + 8 kHz + 0.4 kHz Signal Structure

9.3.1.2 I/O Level

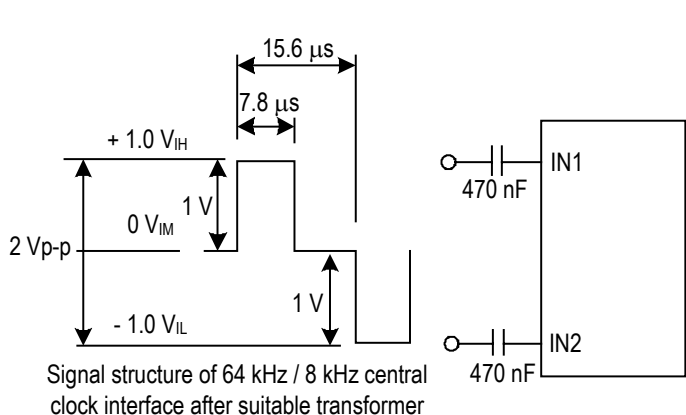


Figure 34. 64 kHz + 8 kHz / 64 kHz + 8 kHz + 0.4 kHz Signal Input Level

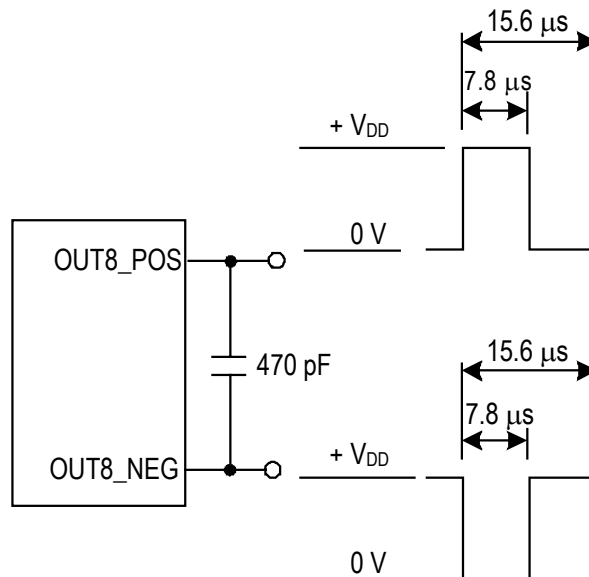
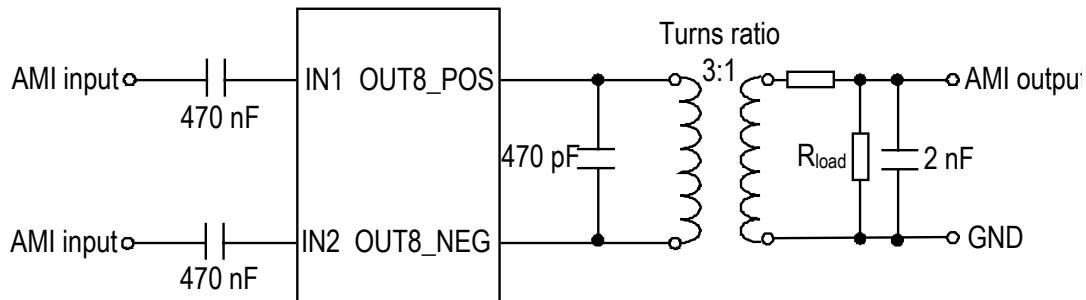


Figure 35. 64 kHz + 8 kHz / 64 kHz + 8 kHz + 0.4 kHz Signal Output Level



For a transformer with a turns ratio of 1:1, a 3:1 ratio potential divider R_{load} must be used to achieve the required 1 V pk-pk voltage level for the positive and negative pulses.

Figure 36. AMI Input / Output Port Line Termination (Recommended)

Table 51: AMI Input / Output Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit
t_{PW}	Input Pulse Width		7.8		μS
$t_{R/F}$	Input Pulse Rise/Fall Time			2	μS
V_{IH}	Input Voltage High	2.13		$V_{DD} + 0.3$	V
V_{IM}	Input Voltage Middle	1.5	1.65	1.8	V
V_{IL}	Input Voltage Low	0		1.4	V
I_{OUT}	Output Current Drive			20	mA
V_{OH}	Output Voltage High, Output Current = -4 mA	2.4			V
V_{OL}	Output Voltage Low, Output Current = 4 mA			0.4	V
R_{TEST}	Nominal Test Load Impedance		110		Ω
V_{MARK}	Peak 'Mark' Amplitude after Transformer	0.9	1	1.1	V
V_{SPACE}	Peak "Space" Amplitude after Transformer	-0.1	0	0.1	V

9.3.1.3 Over-Voltage Protection

The device may require over-voltage protection on AMI input ports according to ITU Recommendation K.41.

9.3.2 CMOS INPUT / OUTPUT PORT

Table 52: CMOS Input Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2			V	
V_{IL}	Input Voltage Low			0.8	V	
I_{IN}	Input Current			± 10	μA	
V_{IN}	Input Voltage	-0.5		5.5	V	

Table 53: CMOS Input Port with Internal Pull-Up Resistor Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2			V	
V_{IL}	Input Voltage Low			0.8	V	
P_U	Pull-Up Resistor		44		$K\Omega$	
I_{IN}	Input Current			± 150	μA	
V_{IN}	Input Voltage	-0.5		5.5	V	

Table 54: CMOS Input Port with Internal Pull-Down Resistor Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2			V	
V_{IL}	Input Voltage Low			0.8	V	
P_D	Pull-Down Resistor		60		$K\Omega$	
I_{IN}	Input Current			± 150	μA	
V_{IN}	Input Voltage	-0.5		5.5	V	

Table 55: CMOS Output Port Electrical Characteristics

Application Pin	Parameter	Description	Min	Typ	Max	Unit	Test Condition
Output Clock	V_{OH}	Output Voltage High	2.4		VDD	V	$I_{OH} = -8 \text{ mA}$
	V_{OL}	Output Voltage Low			0.4	V	$I_{OL} = 8 \text{ mA}$
	t_R	Rise time			4	ns	15 pF
	t_F	Fall time			4	ns	15 pF
Other Output	V_{OH}	Output Voltage High	2.4		VDD	V	$I_{OH} = -4 \text{ mA}$
	V_{OL}	Output Voltage Low			0.4	V	$I_{OL} = 4 \text{ mA}$
	t_R	Rise Time			15	ns	50 pF
	t_F	Fall Time			15	ns	50 pF

9.3.3 PECL / LVDS INPUT / OUTPUT PORT

9.3.3.1 PECL Input / Output Port

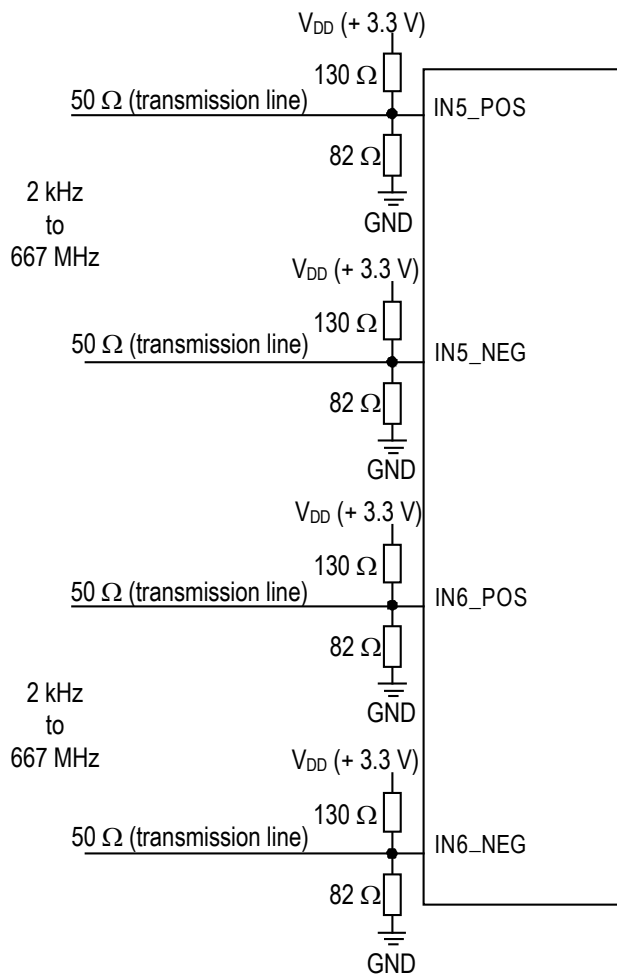


Figure 37. Recommended PECL Input Port Line Termination

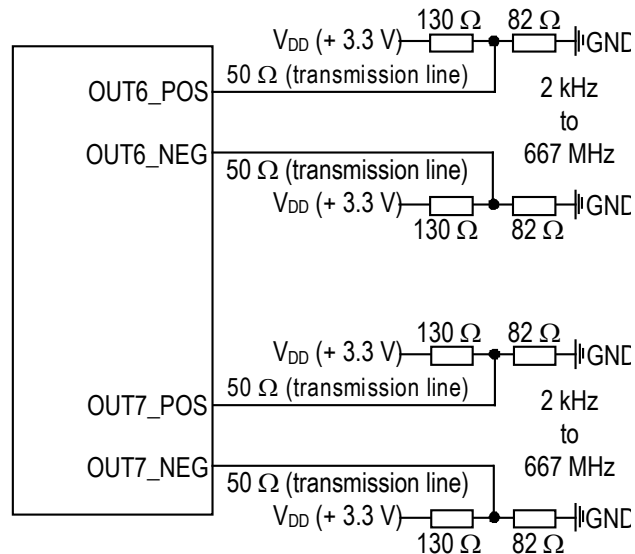


Figure 38. Recommended PECL Output Port Line Termination

Table 56: PECL Input / Output Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IL}	Input Low Voltage, Differential Inputs ¹	$V_{DD} - 2.5$		$V_{DD} - 0.5$	V	
V_{IH}	Input High Voltage, Differential Inputs ¹	$V_{DD} - 2.4$		$V_{DD} - 0.4$	V	
V_{ID}	Input Differential Voltage	1		1.4	V	
V_{IL_S}	Input Low Voltage, Single-ended Input ²	$V_{DD} - 2.4$		$V_{DD} - 1.5$	V	
V_{IH_S}	Input High Voltage, Single-ended Input ²	$V_{DD} - 1.3$		$V_{DD} - 0.5$	V	
I_{IH}	Input High Current, Input Differential Voltage $V_{ID} = 1.4$ V			10	μ A	
I_{IL}	Input Low Current, Input Differential Voltage $V_{ID} = 1.4$ V	-10			μ A	
V_{OL}	Output Voltage Low ³	1.15		1.75	V	
V_{OH}	Output Voltage High ³	1.95		2.55	V	
V_{OD}	Output Differential Voltage ³	0.65		0.85	V	
t_{RISE}	Output Rise time (20% to 80%)	150		300	pS	
t_{FALL}	Output Fall time (20% to 80%)	150		300	pS	
t_{SKEW}	Output Differential Skew			100	pS	

Note:

1. Assuming a differential input voltage of at least 100 mV.
2. Unused differential input terminated to $V_{DD}-1.4$ V.
3. With 50 Ω load on each pin to $V_{DD}-2$ V, i.e. 82 to GND and 130 to V_{DD} .

9.3.3.2 LVDS Input / Output Port

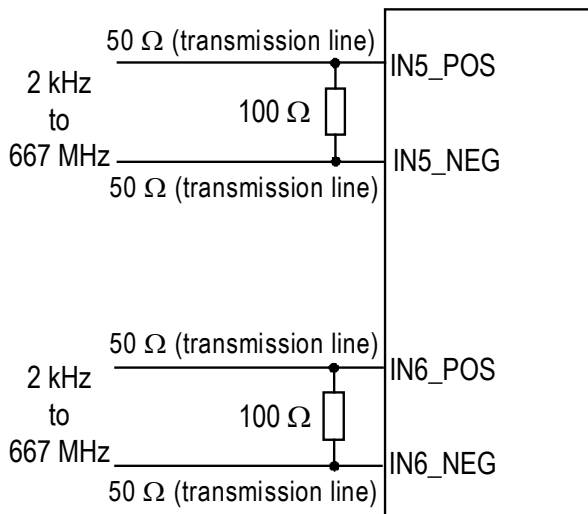


Figure 39. Recommended LVDS Input Port Line Termination

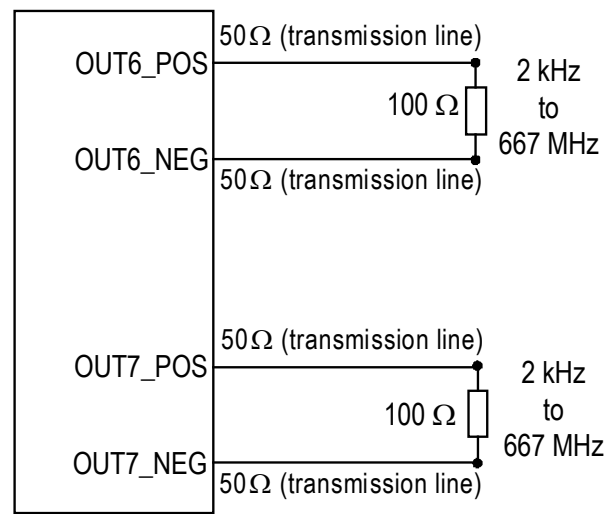


Figure 40. Recommended LVDS Output Port Line Termination

Table 57: LVDS Input / Output Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{CM}	Input Common-mode Voltage Range	200	1200	2200	mV	
V_{DIFF}	Input Peak Differential Voltage	100		900	mV	
V_{IDTH}	Input Differential Threshold	-100		100	mV	
R_{TERM}	External Differential Termination Impedance	95	100	105	Ω	
V_{OH}	Output Voltage High	1150		1850	mV	$R_{LOAD} = 100 \Omega \pm 1\%$
V_{OL}	Output Voltage Low	850		1350	mV	$R_{LOAD} = 100 \Omega \pm 1\%$
V_{OD}	Differential Output Voltage	247	350	454	mV	$R_{LOAD} = 100 \Omega \pm 1\%$
V_{OS}	Output Offset Voltage	1095		1405	mV	$R_{LOAD} = 100 \Omega \pm 1\%$
R_O	Differential Output Impedance	80		120	Ω	$V_{CM} = 1.0 V$ or $1.4 V$
ΔR_O	R_O Mismatch between A and B			20	%	$V_{CM} = 1.0 V$ or $1.4 V$
ΔV_{OD}	Change in V_{OD} between Logic 0 and Logic 1			50	mV	$R_{LOAD} = 100 \Omega \pm 1\%$
ΔV_{OS}	Change in V_{OS} between Logic 0 and Logic 1			50	mV	$R_{LOAD} = 100 \Omega \pm 1\%$
I_{SA}, I_{SB}	Output Current			24	mA	Driver shorted to GND
I_{SAB}	Output Current			12	mA	Driver shorted together
t_{RISE}	Output Rise time (20% to 80%)	100		300	pS	$R_{LOAD} = 100 \Omega \pm 1\%$
t_{FALL}	Output Fall time (20% to 80%)	100		300	pS	$R_{LOAD} = 100 \Omega \pm 1\%$
t_{SKEW}	Output Differential Skew			100	pS	$R_{LOAD} = 100 \Omega \pm 1\%$

9.3.3.3 Single-Ended Input for Differential Input

This is a recommended and tested interface circuit to drive differential input with a single-ended signal.

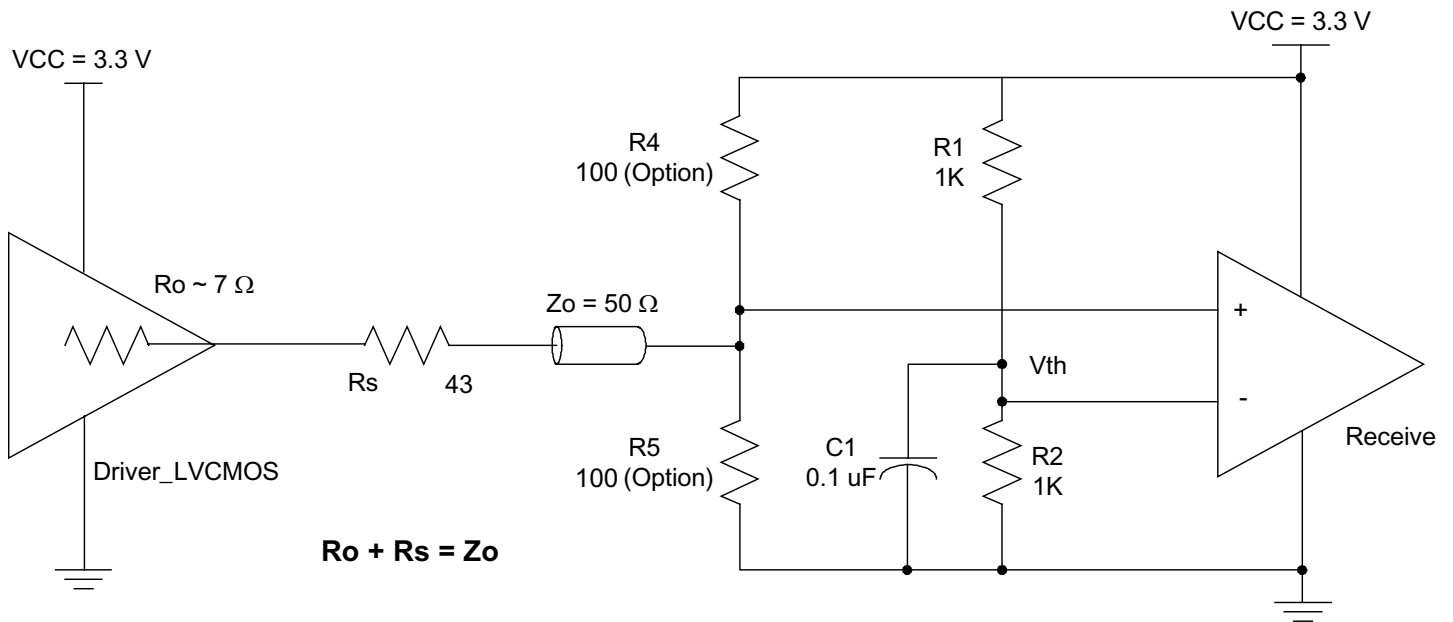


Figure 41. Example of Single-Ended Signal to Drive Differential Input

$$V_{th} = V_{DD} \cdot [R_2 / (R_1 + R_2)]$$

For the example in Figure 41, $R_1 = R_2$, so $V_{th} = V_{DD} / 2 = 1.65 \text{ V}$

The suggested single-ended signal input:

$$V_{IHmax} = V_{DD}$$

$$V_{ILmin} = 0 \text{ V}$$

$$V_{swing} = 0.6 \text{ V} \sim V_{DD}$$

$$\text{DC offset (Swing Center)} = V_{th} / 2 \pm V_{swing} * 10\%$$

9.4 JITTER PERFORMANCE

Table 58: Output Clock Jitter Generation - External T0 APLL Loop Filter
(jitter measured on one differential output (OUT6 or OUT7) with all other outputs disabled)

Test Definition ¹	Output Frequency	RMS Typ (pS)	RMS Max (pS)	Note	Test Filter
25 MHz without T0 APLL	25 MHz	71	80		12 kHz - 5 MHz
125 MHz with T0 APLL	125 MHz	16	20		12 kHz - 20 MHz
156.25 MHz with T0 APLL	156.25 MHz	17	21		12 kHz - 20 MHz
N x 2.048 MHz without APLL		44	200		20 Hz - 100 kHz
N x 2.048 MHz with T0 APLL		42	200		20 Hz - 100 kHz
N x 1.544 MHz without APLL		44	200		10 Hz - 40 kHz
N x 1.544 MHz with T0 APLL		42	200		10 Hz - 40 kHz
44.736 MHz without APLL	44.736 MHz	47	100		100 Hz - 800 kHz
44.736 MHz with T0 APLL	44.736 MHz	40	100		100 Hz - 800 kHz
34.368 MHz without APLL	34.368 MHz	44	100		10 Hz - 400 kHz
34.368 MHz with T0 APLL	34.368 MHz	41	100		10 Hz - 400 kHz
625 MHz with T0 APLL	625 MHz	0.3	1		1.875 MHz - 20 MHz

Table 58: Output Clock Jitter Generation - External T0 APLL Loop Filter
(jitter measured on one differential output (OUT6 or OUT7) with all other outputs disabled)

Test Definition ¹	Output Frequency	RMS Typ (pS)	RMS Max (pS)	Note	Test Filter
OC-3 and STM-1 (Chip T0 DPLL + T0 APLL) 19.44 MHz, 77.76 MHz, 155.52 MHz output	19.44 MHz	2	3.5	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		3	5.6	ITU-T G.813 Option 1 limit 0.5 UI p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		1	2.2	ITU-T G.813 Option 1 limit 0.1 UI p-p (1 UI-6430 ps)	65 kHz to 1.3 MHz
	77.76 MHz	2	3.5	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		3	5.6	ITU-T G.813 Option 1 limit 0.5 UI p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		1	2.1	ITU-T G.813 Option 1 limit 0.1 UI p-p (1 UI-6430 ps)	65 kHz to 1.3 MHz
	155.52 MHz	2	3.2	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		3	5.1	ITU-T G.813 Option 1 limit 0.5 UI p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		1	2	ITU-T G.813 Option 1 limit 0.1 UI p-p (1 UI-6430 ps)	65 kHz to 1.3 MHz

Table 58: Output Clock Jitter Generation - External T0 APLL Loop Filter
(jitter measured on one differential output (OUT6 or OUT7) with all other outputs disabled)

Test Definition ¹	Output Frequency	RMS Typ (pS)	RMS Max (pS)	Note	Test Filter
OC-12 and STM-4 (Chip T0 DPPLL + T0 APLL) 77.76 MHz, 155.52 MHz, 622.08 MHz output	77.76 MHz	2	3.5	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-1608 ps)	12 kHz - 5 MHz
		3	5	ITU-T G.813 Option 1 limit 0.5 UI p-p (1 UI-1608 ps)	1000 Hz to 5 MHz
		0.8	1.3	ITU-T G.813 Option 1 limit 0.1 UI p-p (1 UI-1608 ps)	250 kHz to 5 MHz
	155.52 MHz	2	3.2	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-1608 ps)	12 kHz - 5 MHz
		3	4.7	ITU-T G.813 Option 1 limit 0.5 UI p-p (1 UI-1608 ps)	1000 Hz to 5 MHz
		0.8	1.3	ITU-T G.813 Option 1 limit 0.1 UI p-p (1 UI-1608 ps)	250 kHz to 5 MHz
	622.08 MHz	2	3.4	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-1608 ps)	12 kHz - 5 MHz
		3	4.9	ITU-T G.813 Option 1 limit 0.5 UI p-p (1 UI-1608 ps)	1000 Hz to 5 MHz
		0.8	1.5	ITU-T G.813 Option 1 limit 0.1 UI p-p (1 UI-1608 ps)	250 kHz to 5 MHz
OC-48 and STM-16 (Chip T0 DPPLL + T0 APLL) 155.52 MHz, 622.08 MHz output	155.52 MHz	2	3.2	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-401.878 ps)	12 kHz - 20 MHz
		2	3.8	ITU-T G.813 Option 1 limit 0.5 UI p-p (1 UI-401.878 ps)	5000 Hz to 20 MHz
		0.4	0.7	ITU-T G.813 Option 1 limit 0.1 UI p-p (1 UI-401.878 ps)	1 MHz to 20 MHz
	622.08 MHz	2	3.5	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-401.878 ps)	12 kHz - 20 MHz
		2	4.2	ITU-T G.813 Option 1 limit 0.5 UI p-p (1 UI-401.878 ps)	5000 Hz to 20 MHz
		0.3	0.6	ITU-T G.813 Option 1 limit 0.1 UI p-p (1 UI-401.878 ps)	1 MHz to 20 MHz
Note:					
1. Rakon TCXO E3198 is used.					
2. Lock to 19.44MHz at IN3.					

Table 59: Output Clock Jitter Generation - External T0 APLL Loop Filter
 (jitter measured on one CMOS output (OUT1 - OUT5) with all other outputs disabled)

Test Definition ¹	Output Frequency	RMS Typ (pS)	RMS Max (pS)	Note	Test Filter
25 MHz without T0 APLL	25 MHz	68	120		12 kHz - 5 MHz
125 MHz with T4 APLL	125 MHz	17	21		12 kHz - 20 MHz
156.25 MHz with T4 APLL	156.25 MHz	17	22		12 kHz - 20 MHz
N x 2.048 MHz without APLL		42	200		20 Hz - 100 kHz
N x 2.048 MHz with T0/T4 APLL		43	200		20 Hz - 100 kHz
N x 1.544 MHz without APLL		44	200		10 Hz - 40 kHz
N x 1.544 MHz with T0/T4 APLL		43	200		10 Hz - 40 kHz
44.736 MHz without APLL	44.736 MHz	49	100		100 Hz - 800 kHz
44.736 MHz with T0/T4 APLL	44.736 MHz	43	100		100 Hz - 800 kHz
34.368 MHz without APLL	34.368 MHz	46	100		10 Hz - 400 kHz
34.368 MHz with T0/T4 APLL	34.368 MHz	43	100		10 Hz - 400 kHz
OC-3 and STM-1 (Chip T0 DPLL + T0 APLL) 19.44 MHz, 77.76 MHz, 155.52 MHz output	19.44 MHz	2	3.1	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		3	4.7	ITU-T G.813 Option 1 limit 0.5 UI p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		1	2.1	ITU-T G.813 Option 1 limit 0.1 UI p-p (1 UI-6430 ps)	65 kHz to 1.3 MHz
	77.76 MHz	2	2.9	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		3	4.7	ITU-T G.813 Option 1 limit 0.5 UI p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		1	2.1	ITU-T G.813 Option 1 limit 0.1 UI p-p (1 UI-6430 ps)	65 kHz to 1.3 MHz
	155.52 MHz	2	3	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		3	4.9	ITU-T G.813 Option 1 limit 0.5 UI p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		1	2	ITU-T G.813 Option 1 limit 0.1 UI p-p (1 UI-6430 ps)	65 kHz to 1.3 MHz

Note:
 1. Rakon TCXO E3198 is used.
 2. Lock to 19.44MHz at IN3.

9.5 OUTPUT WANDER GENERATION

GR-1244 TDEV Wander Generation Stratum 3

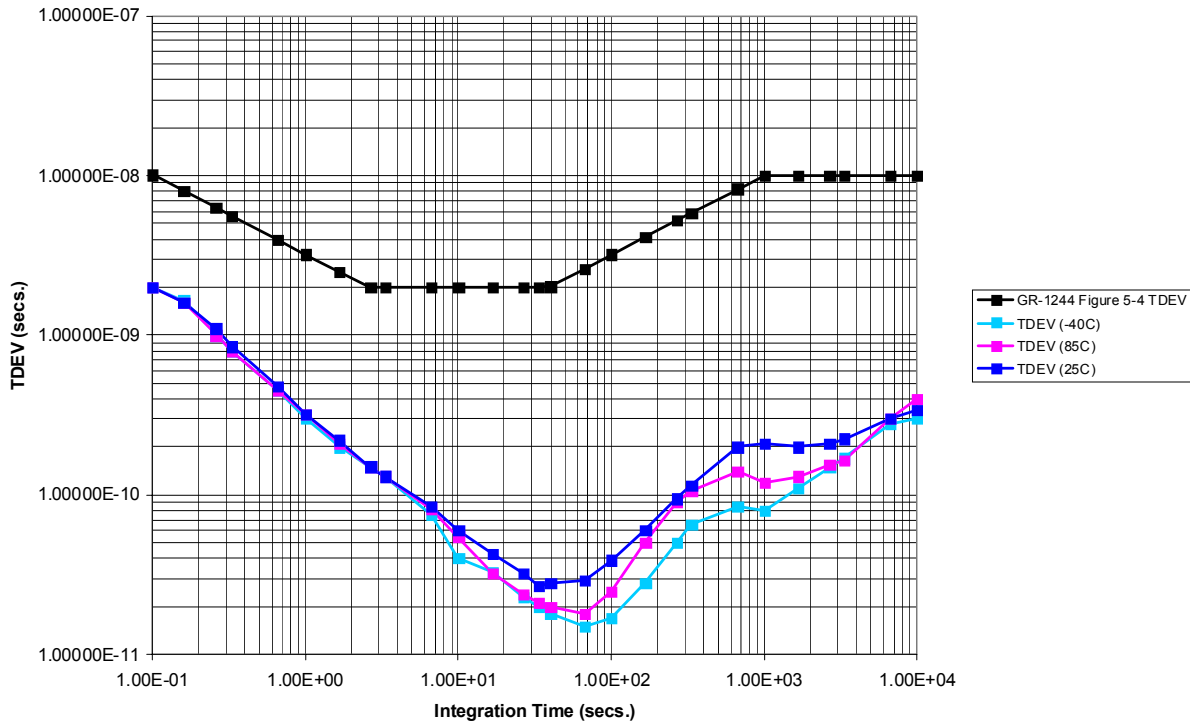


Figure 42. Output Wander Generation (TDEV)

GR-1244 MTIE Wander Generation Stratum 3

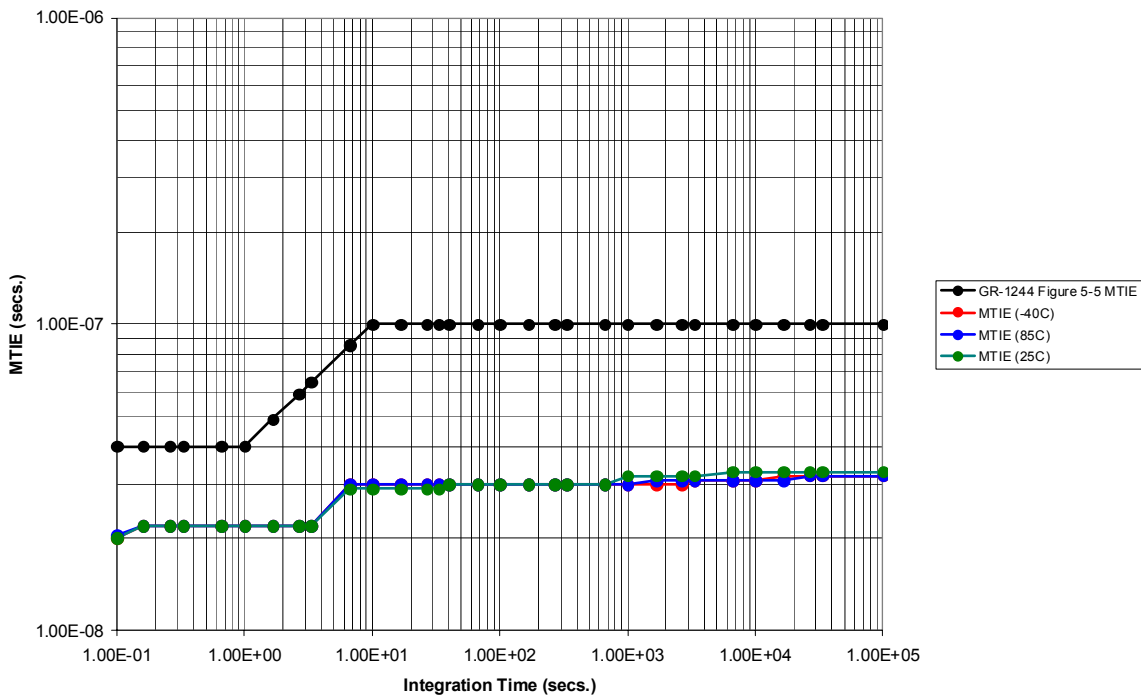


Figure 43. Output Wander Generation (MTIE)

9.6 INPUT / OUTPUT CLOCK TIMING

The inputs and outputs are aligned ideally. But due to the circuit delays, there is delay between the inputs and outputs.

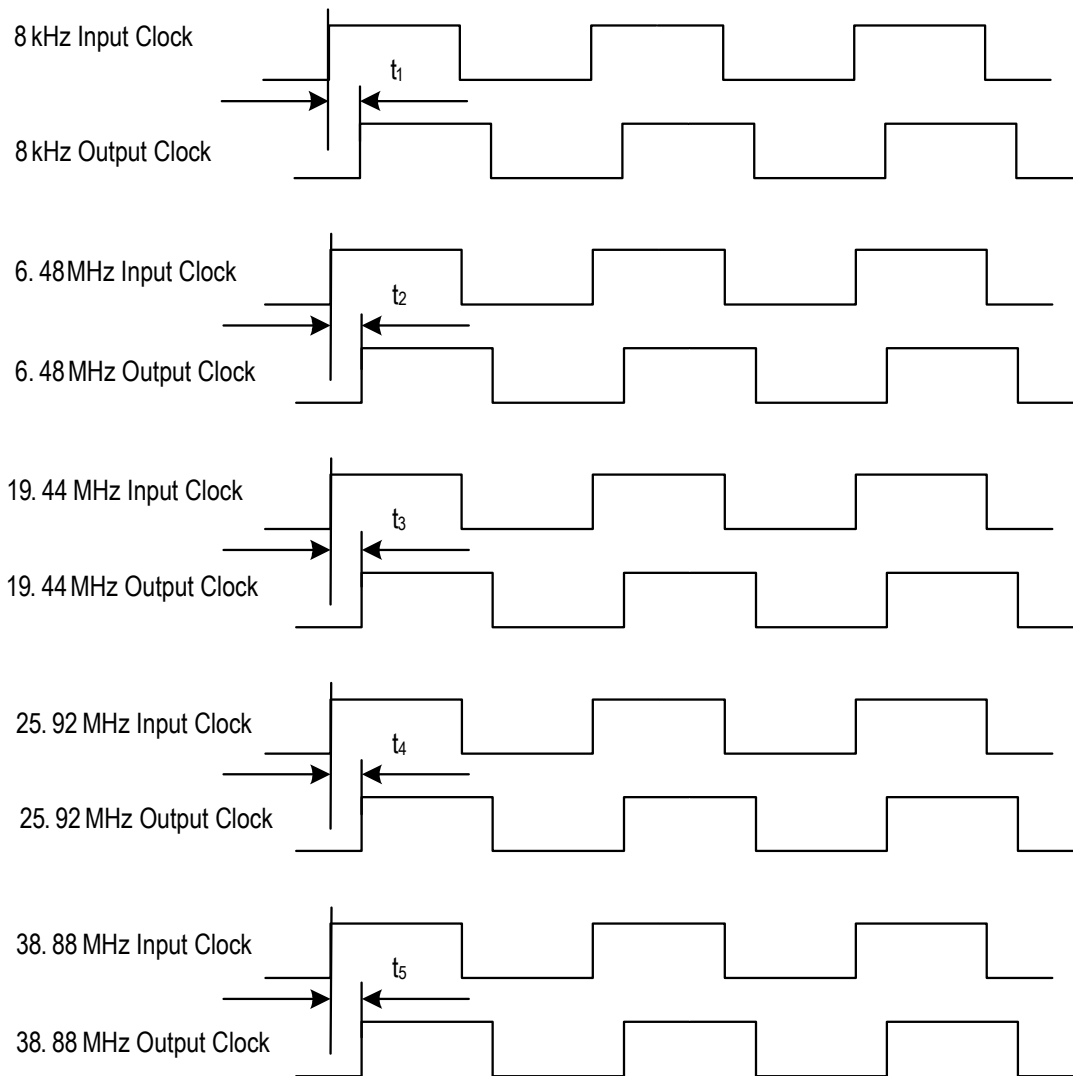


Figure 44. Input / Output Clock Timing

Table 60: Input/Output Clock Timing ¹

Symbol	Typical Delay ² (ns)	Maximum Delay (ns)	Peak to Peak Delay Variation (ns)
t_1	8	20	1
t_2	5	18	1
t_3	5	19	1
t_4	6.5	23	1.5
t_5	5	15	1

Note:

- 1. ¹Tested when IN3 is selected.
- 2. Test for typical value is done with 3.3V VDD, at 25°C.

9.7 OUTPUT CLOCK TIMING

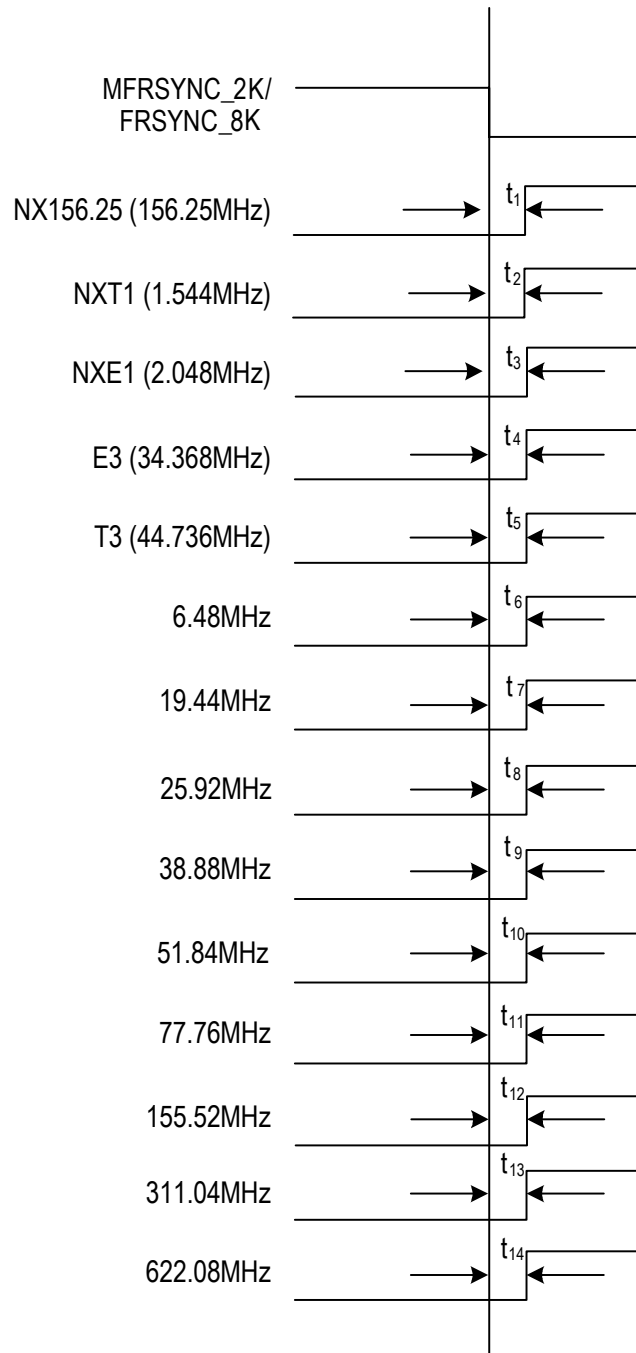


Figure 45. Output Clock Timing

Table 61: Output Clock Timing

Symbol	Typical Delay (ns)	Maximum Delay (ns)	Peak to Peak Delay Variation (ns)
t_1	2	4	1
t_2	-1	-2	2
t_3	-1	-2	2
t_4	-2	-4	2
t_5	-2	-4	2
t_6	-2.5	-5	2
t_7	-2.5	-5	2
t_8	-2	-4	2
t_9	-2	-4	2
t_{10}	-1.5	-3	2
t_{11}	-1.5	-3	2
t_{12}	1.5	3	2
t_{13}	0.5	1	1
t_{14}	-1	-2	1

3G	---	Third Generation
ADSL	---	Asymmetric Digital Subscriber Line
APLL	---	Analog Phase Locked Loop
ATM	---	Asynchronous Transfer Mode
BITS	---	Building Integrated Timing Supply
CMOS	---	Complementary Metal-Oxide Semiconductor
DCO	---	Digital Controlled Oscillator
DPLL	---	Digital Phase Locked Loop
DSL	---	Digital Subscriber Line
DSLAM	---	Digital Subscriber Line Access MUX
DWDM	---	Dense Wavelength Division Multiplexing
EPROM	---	Erasable Programmable Read Only Memory
ETH	---	Synchronous Ethernet System
GPS	---	Global Positioning System
GSM	---	Global System for Mobile Communications
HS	---	Hitless Switching
IIR	---	Infinite Impulse Response
IP	---	Internet Protocol
ISDN	---	Integrated Services Digital Network
JTAG	---	Joint Test Action Group
LPF	---	Low Pass Filter
LVDS	---	Low Voltage Differential Signal
MTIE	---	Maximum Time Interval Error
MUX	---	Multiplexer
OBSAI	---	Open Base Station Architecture Initiative
OC-n	---	Optical Carried rate, n = 1, 3, 12, 48, 192, 768; 51 Mbit/s, 155 Mbit/s, 622 Mbit/s, 2.5 Gbit/s, 10 Gbit/s, 40 Gbit/s.

PDH	---	Plesiochronous Digital Hierarchy
PECL	---	Positive Emitter Coupled Logic
PFD	---	Phase & Frequency Detector
PLL	---	Phase Locked Loop
RMS	---	Root Mean Square
PRS	---	Primary Reference Source
SDH	---	Synchronous Digital Hierarchy
SEC	---	SDH / SONET Equipment Clock
SMC	---	SONET Minimum Clock
SONET	---	Synchronous Optical Network
SSU	---	Synchronization Supply Unit
STM	---	Synchronous Transfer Mode
TCM-ISDN	---	Time Compression Multiplexing Integrated Services Digital Network
TDEV	---	Time Deviation
UI	---	Unit Interval
WLL	---	Wireless Local Loop



Index Datasheet

A		Fine Phase Loss	28
AMI Violation	20	Frequency Hard Alarm	30
Averaged Phase Error	35	H	
B		Hard Limit	28
Bandwidths and Damping Factors	35	Holdover Frequency Offset	36
Acquisition Bandwidth and Damping Factor	35	I	
Locked Bandwidth and Damping Factor	35	IIR	36
Starting Bandwidth and Damping Factor	35	Input Clock Frequency	24
C		Input Clock Selection	26, 30
Calibration	19	Automatic selection	27, 30
Coarse Phase Loss	28	External Fast selection	26, 30
Crystal Oscillator	19	Forced selection	27, 30
Current Frequency Offset	35	Non-Revertive switching	31
D		Revertive switching	30
DCO	35	Internal Leaky Bucket Accumulator	23
Division Factor	21	Bucket Size	23
DPLL Hard Alarm	28	Decay Rate	23
DPLL Hard Limit	28	Lower Threshold	23
DPLL Operating Mode	35, 36	Upper Threshold	23
Free-Run mode	35, 36	L	
Holdover mode	35, 36	LOS	23, 30
Automatic Fast Averaged	36	LPF	35
Automatic Instantaneous	36	M	
Automatic Slow Averaged	36	Master / Slave Configuration	45
Manual	36	Master Clock	19
Locked mode	35, 36	Microprocessor Interface	49
Temp-Holdover mode	35	microprocessor interface	
Lost-Phase mode	35	EPROM	51
Pre-Locked mode	35	Intel	55
Pre-Locked2 mode	36	Motorola	57
DPLL Soft Alarm	28	Multiplexed	52
DPLL Soft Limit	28	Serial	59, 61
E		MON_SW_HS_CNFG - Frequency Monitor, Input Clock Selection & HS Control	65
External Sync Alarm	43	MON_SW_PBO_CNFG - Frequency Monitor, Input Clock Selection & PBO Control	65
F			
Fast Loss	28		

N		DivN Divider	21
No-activity Alarm	23, 30	HF Divider	21
P		Lock 8k Divider	21
PFD	35	R	
Phase Lock Alarm	29, 30	Reference Clock	24
Phase Offset	38	S	
Phase-compared	28, 38	State Machine	32, 34
Phase-time	38	V	
Pre-Divider	21	Validity	30

PACKAGE DIMENSIONS

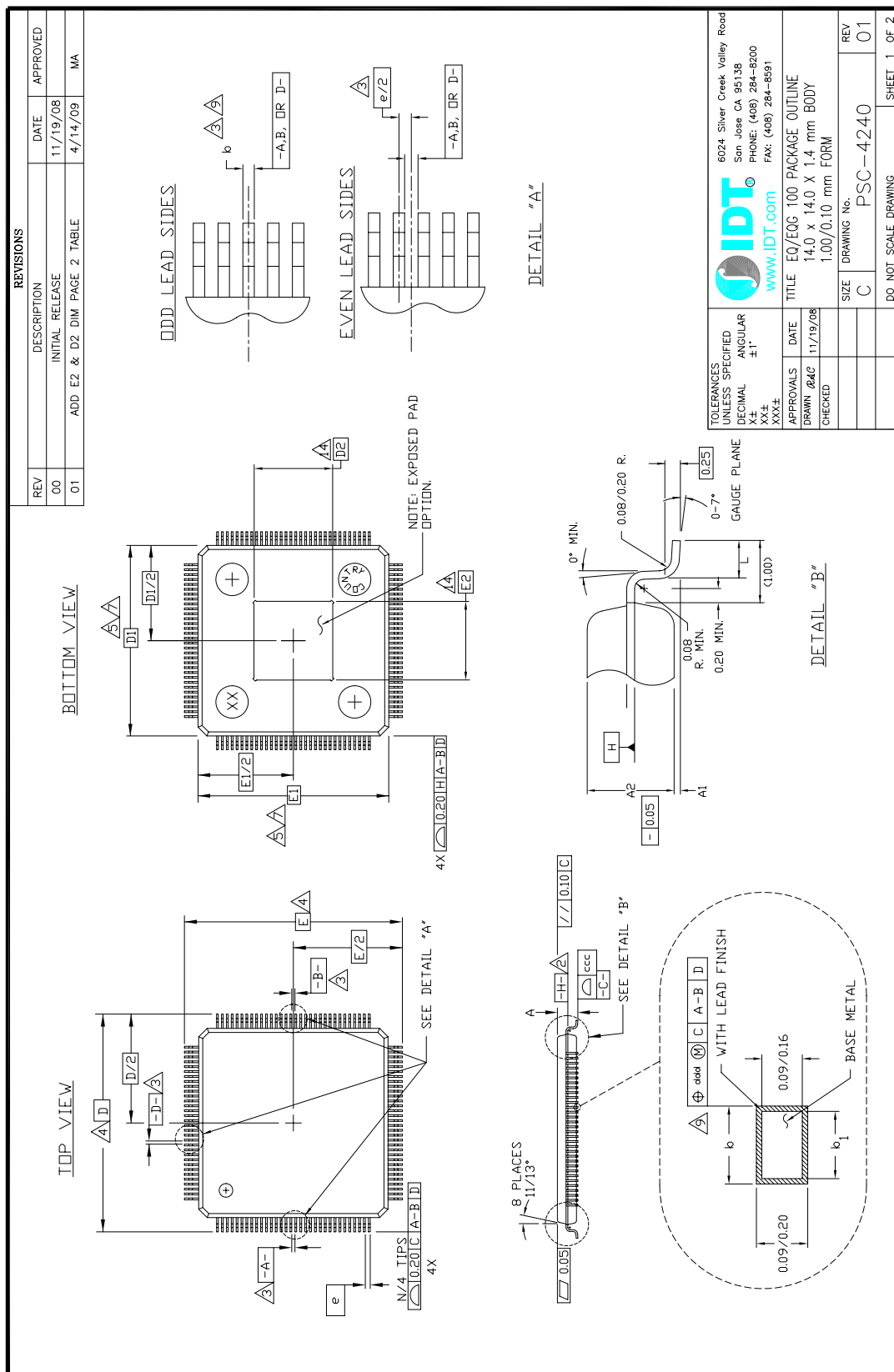


Figure 46. 100-Pin EQG Package Dimensions (a) (in Millimeters)

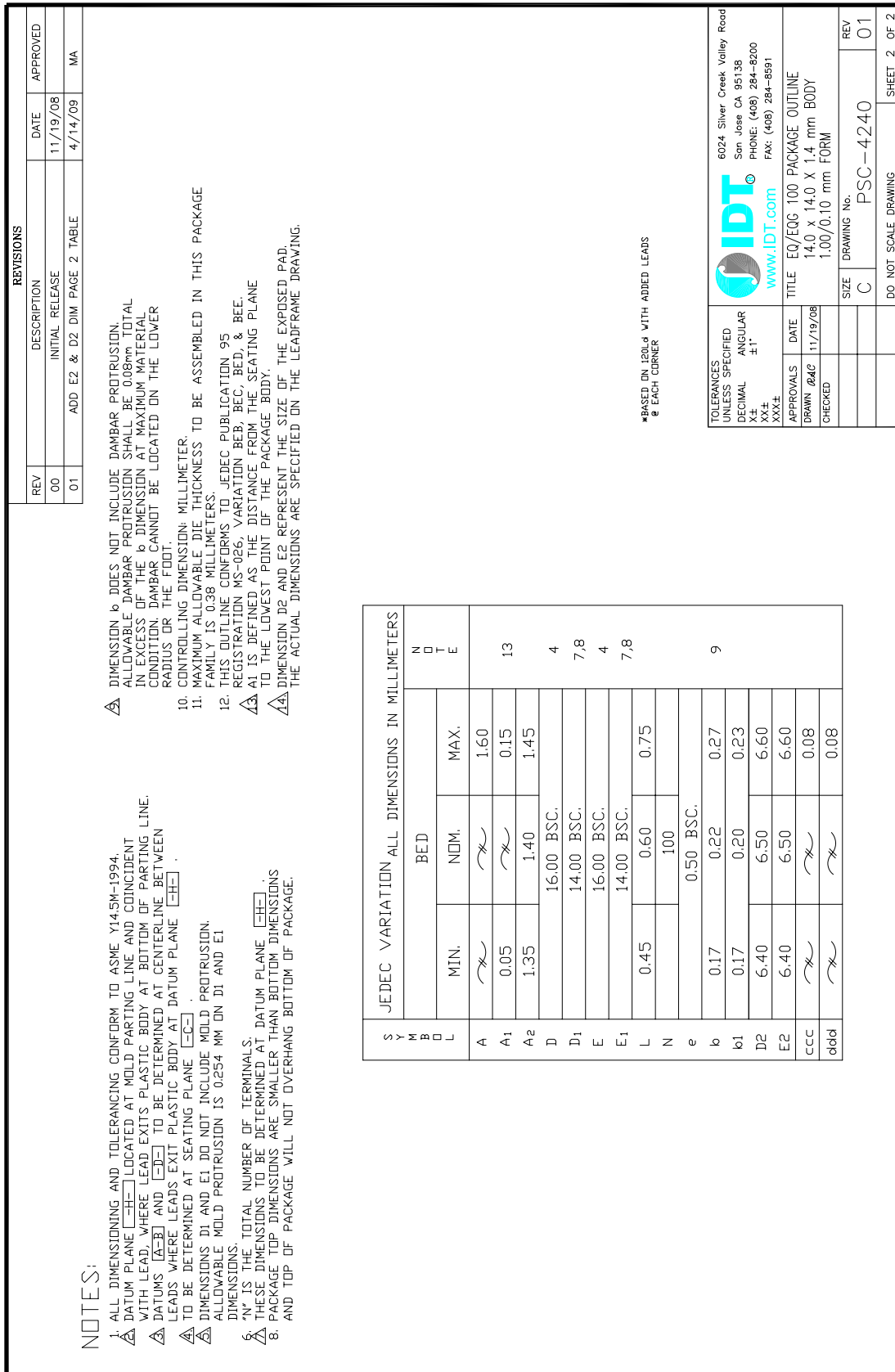


Figure 47. 100-Pin EQG Package Dimensions (b) (in Millimeters)

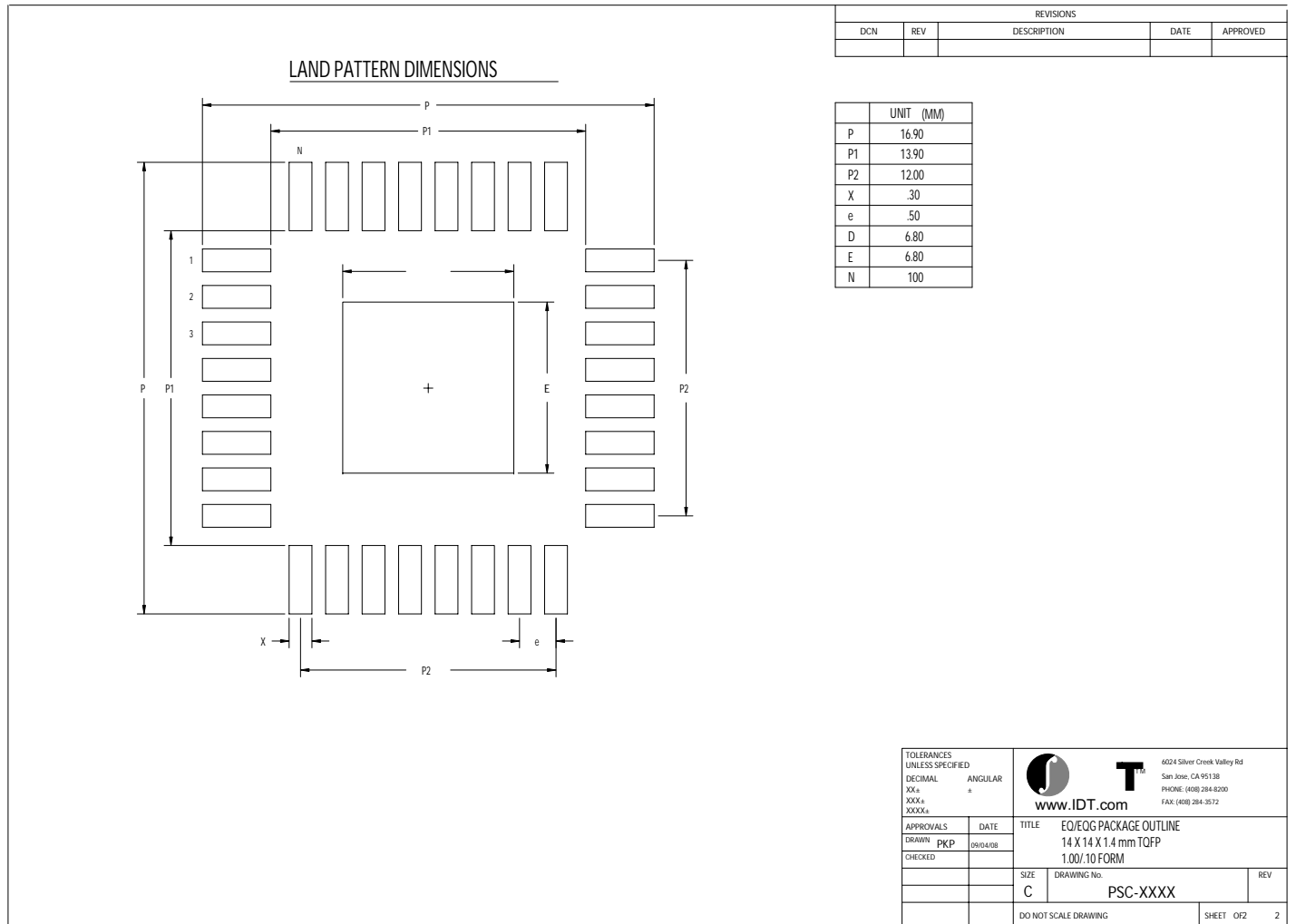
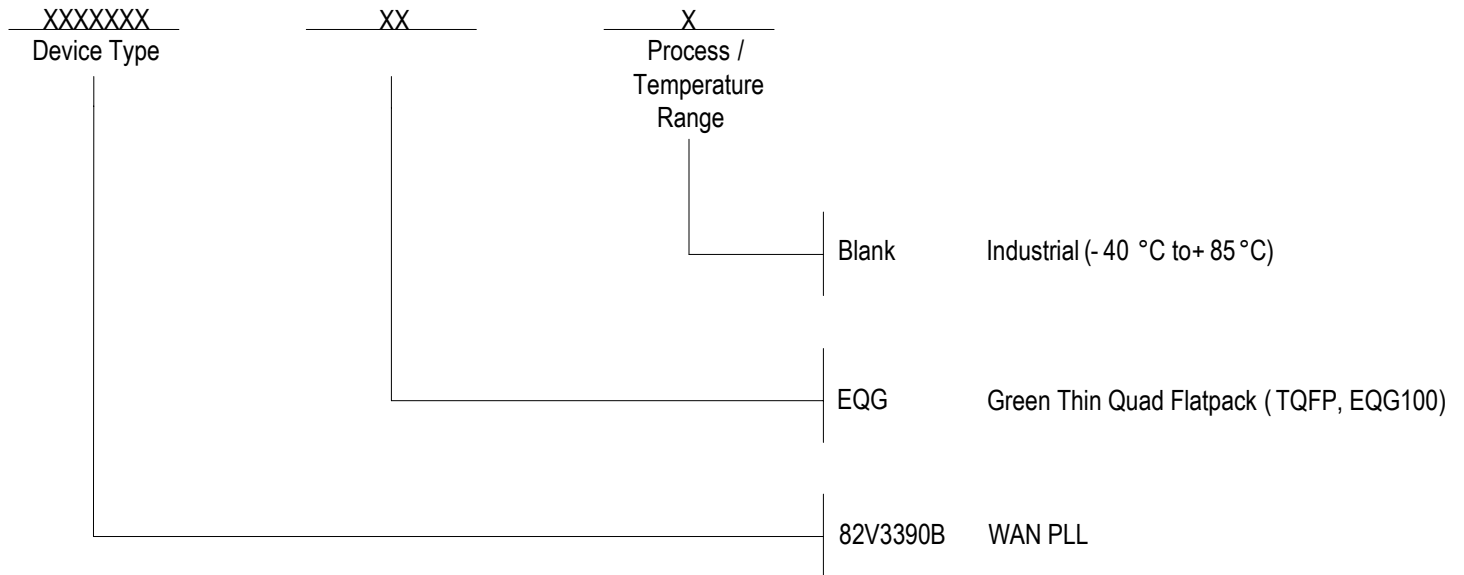


Figure 48. EQG100 Recommended Land Pattern with Exposed Pad (in Millimeters)

ORDERING INFORMATION



REVISION HISTORY

- April 15, 2011 Initial Revision
- April 28, 2011 Cover Page, deleted the word "Preliminary"
- July 14, 2011 pgs 9 - 11, 13 - 15, 17, 19 - 21, 24 - 28, 31, 35, 38 - 41, 45 - 46, 48, 62, 65, 70, 72 - 73, 76, 85 - 86, 88 - 97, 99, 115, 140 - 141, 154-156, 166, 169

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