## GENERAL DESCRIPTION

The 83908I-02 is a low skew, high performance 1-to-8 Crystal Oscillator//Crystal-to-LVCMOS fanout buffer from IDT. The 83908I-02 has selectable single-ended clock or two crystal-oscillator inputs. There is an output enable to disable the outputs by placing them into a high-impedance state.

Guaranteed output and part-to-part skew characteristics make the 83908I-02 ideal for those applications demanding well defined performance and repeatability.

## FEATURES

- Eight LVCMOS/LVTTL outputs ,
  $19\Omega$ typical output impedance @ $V_{DD} = V_{DDO} = 3.3V$

- Two Crystal oscillator input pairs
  One LVCMOS/LVTTL clock input

- Crystal input frequency range:  10MHz - 40MHz

- Output frequency:  200MHz (typical)

- Output Skew: 70ps (maximum) @ $V_{DD} = V_{DDO} = 3.3V$

- Part-to-part skew:  700ps (maximum) @ $V_{DD} = V_{DDO} = 3.3V$

- RMS phase jitter @ 25MHz output using a 25MHz crystal
  (12kHz - 10MHz): 0.39ps (typical) @ $V_{DD} = V_{DDO} = 3.3V$

  | Offset | Noise Power |
  |--------|-------------|
  | 100Hz | -111.4 dBc/Hz |
  | 1kHz | -139.9 dBc/Hz |
  | 10kHz | -157.3 dBc/Hz |
  | 100kHz | -157.5 dBc/Hz |

- Supply Voltage Modes:
  (Core/Output)
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/2.5V
  2.5V/1.8V

- -40°C to 85°C ambient operating temperature

- Available in lead-free (RoHS 6) package

## BLOCK DIAGRAM
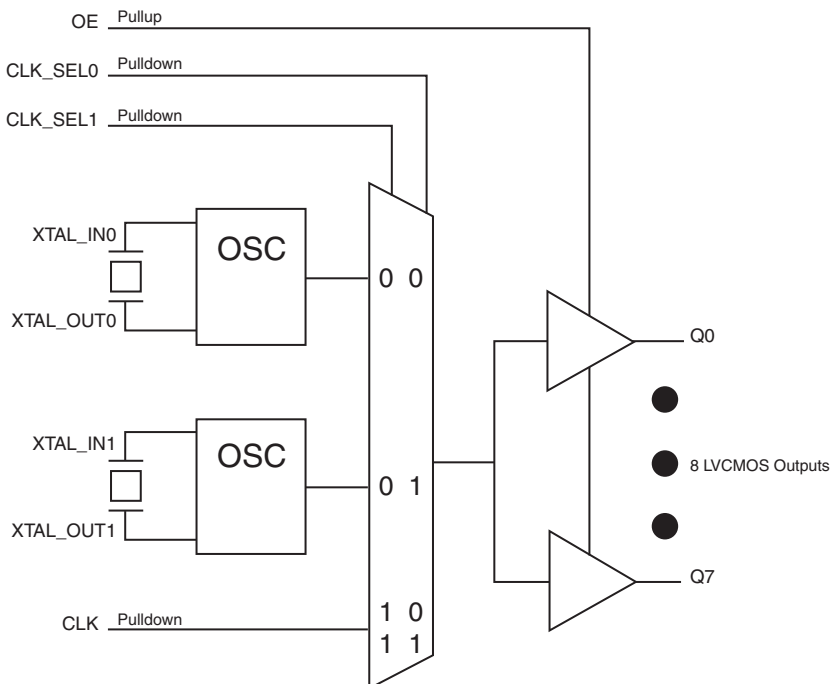


## PIN ASSIGNMENT



### 83908I-02
**24-Lead, 173-MIL TSSOP**
4.4mm x 7.8mm x 0.925mm
body package
**G Package**
Top View

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | V$_{DD}$ | Power | | Power supply pin. |
| 2, 3 | XTAL_IN0, XTAL_OUT0 | Input | | Crystal oscillator interface. XTAL_IN0 is the input. XTAL_OUT0 is the output. |
| 4, 10, 15, 21 | V$_{DDO}$ | Power | | Output supply pins. |
| 5, 6, 8, 9, 16, 17, 19, 20 | Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7 | Output | | Single-ended clock outputs. LVCMOS/LVTTL interface levels. |
| 7, 18, 24 | GND | Power | | Power supply ground. |
| 11, 14 | CLK_SEL0, CLK_SEL1 | Input | Pulldown | Clock select inputs. See Table 3, Input Reference Function Table. LVCMOS / LVTTL interface levels. |
| 12 | CLK | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 13 | OE | Input | Pullup | Output enable. When LOW, outputs are in HIGH impedance state. When HIGH, outputs are active. LVCMOS / LVTTL interface levels. |
| 22, 23 | XTAL_OUT1, XTAL_IN1 | Input | | Crystal oscillator interface. XTAL_IN1 is the input. XTAL_OUT1 is the output. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| C$_{IN}$ | Input Capacitance | | | 4 | | pF |
| R$_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| R$_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |
| C$_{PD}$ | Power Dissipation Capacitance (per output) | V$_{DDO}$ = 3.465V | | 7 | | pF |
| | | V$_{DDO}$ = 2.625V | | 7 | | pF |
| | | V$_{DDO}$ = 2V | | 6 | | pF |
| R$_{OUT}$ | Output Impedance | V$_{DDO}$ = 3.3V ± 5% | | 19 | | Ω |
| | | V$_{DDO}$ = 2.5V ± 5% | | 21 | | Ω |
| | | V$_{DDO}$ = 1.8V ± 0.2V | | 32 | | Ω |

TABLE 3. INPUT REFERENCE FUNCTION TABLE

| Control Inputs | | Reference | |
|---|---|---|---|
| CLK_SEL1 | CLK_SEL0 | | |
| 0 | 0 | XTAL0 enabled (default) | XTAL1 disabled |
| 0 | 1 | XTAL1 enabled | XTAL0 disabled |
| 1 | 0 | CLK enabled | XTAL0 and XTAL1 disabled |
| 1 | 1 | CLK enabled | XTAL0 and XTAL1 disabled |

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD}$      4.6V

Inputs, $V_I$      -0.5V to $V_{DD}$ + 0.5 V

Outputs, $V_O$      -0.5V to $V_{DDO}$ + 0.5V

Package Thermal Impedance, $\theta_{JA}$      87.8°C/W (0 mps)

Storage Temperature, $T_{STG}$      -65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,** $V_{DD} = V_{DDO} = 3.3V\pm5\%$, $T_A = -40°C$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDO}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | No Load & XTALx selected | | | 30 | mA |
| | | No Load & CLK selected | | | 1 | mA |
| $I_{DDO}$ | Output Supply Current | No Load & CLK selected | | | 1 | mA |

**TABLE 4B. POWER SUPPLY DC CHARACTERISTICS,** $V_{DD} = 3.3V\pm5\%$, $V_{DDO} = 2.5V\pm5\%$, $T_A = -40°C$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDO}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD}$ | Power Supply Current | No Load & XTALx selected | | | 30 | mA |
| | | No Load & CLK selected | | | 1 | mA |
| $I_{DDO}$ | Output Supply Current | No Load & CLK selected | | | 1 | mA |

**TABLE 4C. POWER SUPPLY DC CHARACTERISTICS,** $V_{DD} = 3.3V\pm5\%$, $V_{DDO} = 1.8V\pm0.2V$, $T_A = -40°C$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDO}$ | Output Supply Voltage | | 1.6 | 1.8 | 2.0 | V |
| $I_{DD}$ | Power Supply Current | No Load & XTALx selected | | | 30 | mA |
| | | No Load & CLK selected | | | 1 | mA |
| $I_{DDO}$ | Output Supply Current | No Load & CLK selected | | | 1 | mA |

**TABLE 4D. POWER SUPPLY DC CHARACTERISTICS,** $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ TO $85°C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{DDO}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD}$ | Power Supply Current | No Load & XTALx selected | | | 20 | mA |
| | | No Load & CLK selected | | | 1 | mA |
| $I_{DDO}$ | Output Supply Current | No Load & CLK selected | | | 1 | mA |

**TABLE 4E. POWER SUPPLY DC CHARACTERISTICS,** $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40°C$ TO $85°C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{DDO}$ | Output Supply Voltage | | 1.6 | 1.8 | 2.0 | V |
| $I_{DD}$ | Power Supply Current | No Load & XTALx selected | | | 20 | mA |
| | | No Load & CLK selected | | | 1 | mA |
| $I_{DDO}$ | Output Supply Current | No Load & CLK selected | | | 1 | mA |

**TABLE 4F. DC CHARACTERISTICS,** $T_A = -40°C$ TO $85°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | $V_{DD} = 3.3V \pm 5\%$ | 2.2 | | $V_{DD} + 0.3$ | V |
| | | | $V_{DD} = 2.5V \pm 5\%$ | 1.6 | | $V_{DD} + 0.3$ | V |
| $V_{IL}$ | Input Low Voltage | | $V_{DD} = 3.3V \pm 5\%$ | -0.3 | | 1.3 | V |
| | | | $V_{DD} = 2.5V \pm 5\%$ | -0.3 | | 0.9 | V |
| $I_{IH}$ | Input High Current | CLK, CLK_SEL[0:1] | $V_{DD} = 3.3V$ or $2.5V \pm 5\%$ | | | 150 | µA |
| | | OE | $V_{DD} = 3.3V$ or $2.5V \pm 5\%$ | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK, CLK_SEL[0:1] | $V_{DD} = 3.3V$ or $2.5V \pm 5\%$ | -5 | | | µA |
| | | OE | $V_{DD} = 3.3V$ or $2.5V \pm 5\%$ | -150 | | | µA |
| $V_{OH}$ | Output HighVoltage | | $V_{DDO} = 3.3V \pm 5\%$; NOTE 1 | 2.6 | | | V |
| | | | $V_{DDO} = 2.5V \pm 5\%$; NOTE 1 | 1.8 | | | V |
| | | | $V_{DDO} = 1.8V \pm 0.2V$; NOTE 1 | 1.2 | | | V |
| $V_{OL}$ | Output Low Voltage | | $V_{DDO} = 3.3V \pm 5\%$; NOTE 1 | | | 0.6 | V |
| | | | $V_{DDO} = 2.5V \pm 5\%$; NOTE 1 | | | 0.5 | V |
| | | | $V_{DDO} = 1.8V \pm 0.2V$; NOTE 1 | | | 0.4 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement section, "Load Test Circuit" diagrams.

**TABLE 5. CRYSTAL CHARACTERISTICS**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation / cut | | | Fundamental | | |
| Frequency | | 10 | | 40 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Drive Level | | | | 1 | mW |

**TABLE 6A. AC CHARACTERISTICS,** $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ TO $85°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | w/external XTAL | | 10 | | 40 | MHz |
| | | w/external CLK | | | | 200 | MHz |
| $tp_{LH}$ | Propagation Delay, Low-to-High; NOTE 1 | | | 1.4 | 2.0 | 2.6 | ns |
| $t$sk(o) | Output Skew; NOTE 2 | | | | | 70 | ps |
| $t$sk(pp) | Part-to-Part Skew; NOTE 2, 3 | | | | | 700 | ps |
| $t$jit(Ø) | RMS Phase Jitter, Random; NOTE 4 | | 25MHz XTAL, (12kHz-10MHz) | | 0.39 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | | 20% to 80% | 200 | | 800 | ps |
| odc | Output Duty Cycle | w/external XTAL | $f \leq 38.88MHz$ | 45 | | 55 | % |
| | | w/external CLK | $f \leq 133MHz$ | 47 | | 53 | % |
| $t_{EN}$ | Output Enable Time; NOTE 5 | | | | | 10 | ns |
| $t_{DIS}$ | Output Disable Time; NOTE 5 | | | | | 10 | ns |

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

**TABLE 6B. AC CHARACTERISTICS,** $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ TO $85°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | w/external XTAL | | 10 | | 40 | MHz |
| | | w/external CLK | | | | 200 | MHz |
| $tp_{LH}$ | Propagation Delay, Low-to-High; NOTE 1 | | | 1.5 | 2.1 | 2.7 | ns |
| $t$sk(o) | Output Skew; NOTE 2 | | | | | 70 | ps |
| $t$sk(pp) | Part-to-Part Skew; NOTE 2, 3 | | | | | 700 | ps |
| $t$jit(Ø) | RMS Phase Jitter, Random; NOTE 4 | | 25MHz XTAL, (12kHz-10MHz) | | 0.42 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | | 20% to 80% | 200 | | 800 | ps |
| odc | Output Duty Cycle | w/external XTAL | $f \leq 38.88MHz$ | 45 | | 55 | % |
| | | w/external CLK | $f \leq 133MHz$ | 47 | | 53 | % |
| $t_{EN}$ | Output Enable Time; NOTE 5 | | | | | 10 | ns |
| $t_{DIS}$ | Output Disable Time; NOTE 5 | | | | | 10 | ns |

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

**TABLE 6C. AC CHARACTERISTICS,** $V_{DD}$ = 3.3V ± 5%, $V_{DDO}$ = 1.8V±0.2V, T$_A$ = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | w/external XTAL | | 10 | | 40 | MHz |
| | | w/external CLK | | | | 200 | MHz |
| tp$_{LH}$ | Propagation Delay, Low-to-High; NOTE 1 | | | 1.6 | 2.4 | 3.2 | ns |
| $t$sk(o) | Output Skew; NOTE 2 | | | | | 70 | ps |
| $t$sk(pp) | Part-to-Part Skew; NOTE 2, 3 | | | | | 700 | ps |
| $t$jit(Ø) | RMS Phase Jitter, Random; NOTE 4 | | 25MHz XTAL, (12kHz-10MHz) | | 0.43 | | ps |
| t$_R$ / t$_F$ | Output Rise/Fall Time | | 20% to 80% | 200 | | 800 | ps |
| odc | Output Duty Cycle | w/external XTAL | $f \leq 38.88$MHz | 45 | | 55 | % |
| | | w/external CLK | $f \leq 133$MHz | 47 | | 53 | % |
| t$_{EN}$ | Output Enable Time; NOTE 5 | | | | | 10 | ns |
| t$_{DIS}$ | Output Disable Time; NOTE 5 | | | | | 10 | ns |

NOTE 1: Measured from $V_{DD}$/2 of the input to $V_{DDO}$/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}$/2.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.


**TABLE 6D. AC CHARACTERISTICS,** $V_{DD}$ = $V_{DDO}$ = 2.5V ± 5%, T$_A$ = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | w/external XTAL | | 10 | | 40 | MHz |
| | | w/external CLK | | | | 200 | MHz |
| tp$_{LH}$ | Propagation Delay, Low-to-High; NOTE 1 | | | 1.7 | 2.4 | 3.1 | ns |
| $t$sk(o) | Output Skew; NOTE 2 | | | | | 70 | ps |
| $t$sk(pp) | Part-to-Part Skew; NOTE 2, 3 | | | | | 700 | ps |
| $t$jit(Ø) | RMS Phase Jitter, Random; NOTE 4 | | 25MHz XTAL, (12kHz-10MHz) | | 0.44 | | ps |
| t$_R$ / t$_F$ | Output Rise/Fall Time | | 20% to 80% | 200 | | 800 | ps |
| odc | Output Duty Cycle | w/external XTAL | $f \leq 38.88$MHz | 45 | | 55 | % |
| | | w/external CLK | $f \leq 133$MHz | 47 | | 53 | % |
| t$_{EN}$ | Output Enable Time; NOTE 5 | | | | | 10 | ns |
| t$_{DIS}$ | Output Disable Time; NOTE 5 | | | | | 10 | ns |

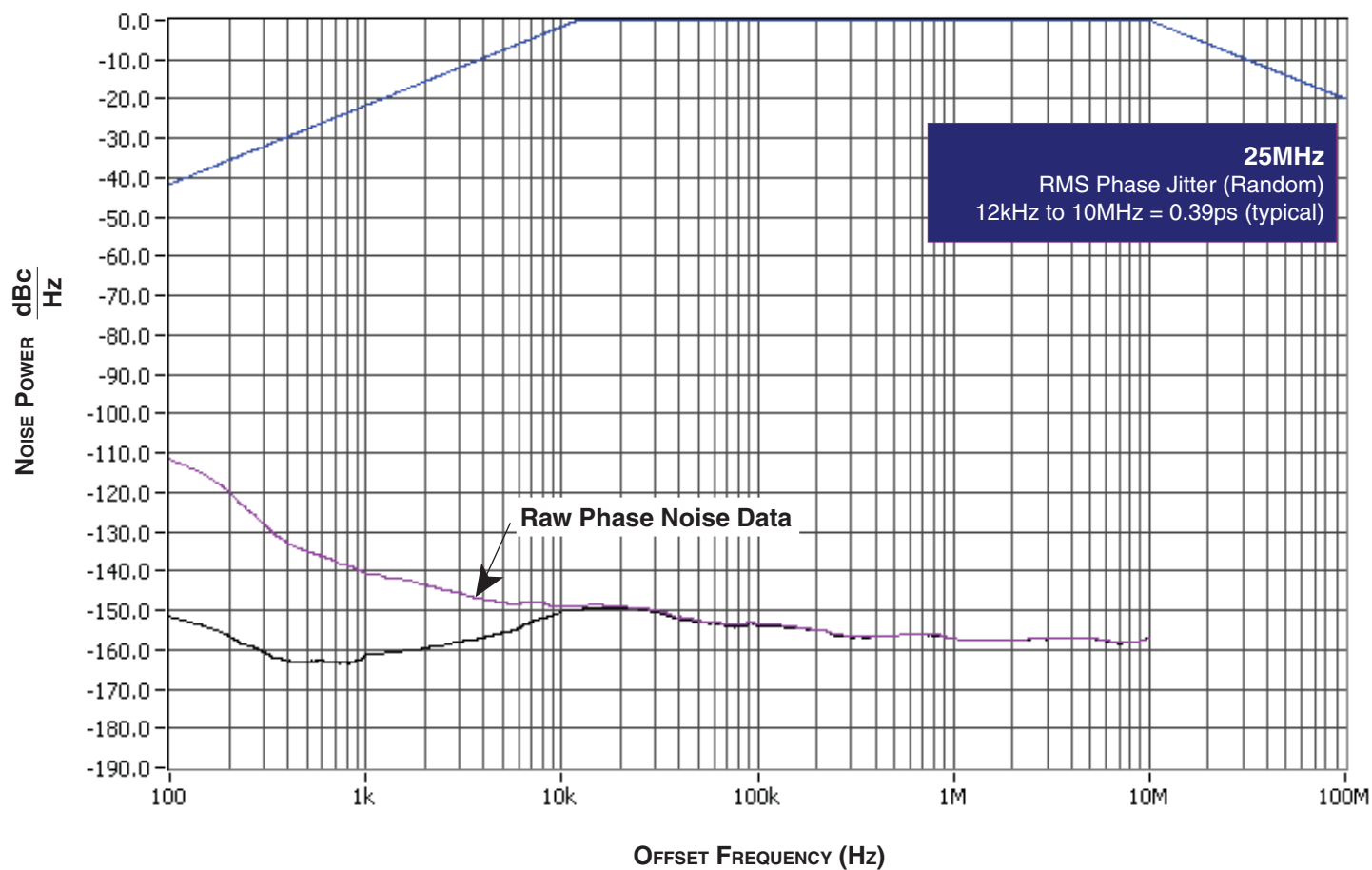NOTE 1: Measured from $V_{DD}$/2 of the input to $V_{DDO}$/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}$/2.
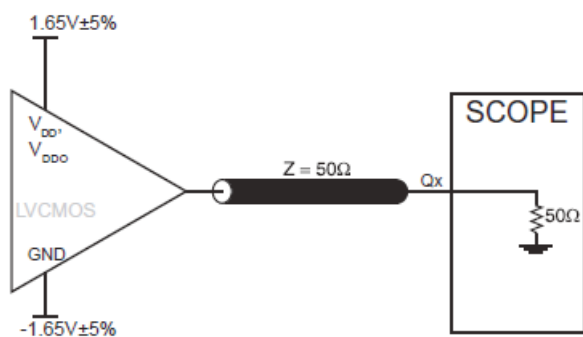NOTE 4: Phase jitter is dependent on the input source used.
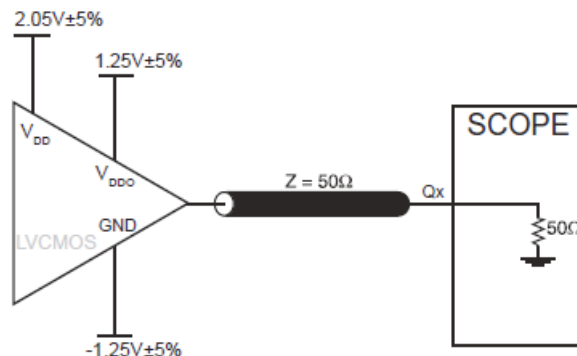NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

TABLE 6E. AC CHARACTERISTICS, $V_{DD}$ = 2.5V ± 5%, $V_{DDO}$ = 1.8V±0.2V, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | w/external XTAL | | 10 | | 40 | MHz |
| | | w/external CLK | | | | 200 | MHz |
| $tp_{LH}$ | Propagation Delay, Low-to-High; NOTE 1 | | | 1.7 | 2.6 | 3.5 | ns |
| $t$sk(o) | Output Skew; NOTE 2 | | | | | 70 | ps |
| $t$sk(pp) | Part-to-Part Skew; NOTE 2, 3 | | | | | 700 | ps |
| $t$jit(Ø) | RMS Phase Jitter, Random; NOTE 4 | | 25MHz XTAL, (12kHz-10MHz) | | 0.37 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | | 20% to 80% | 200 | | 800 | ps |
| odc | Output Duty Cycle | w/external XTAL | $f \leq 38.88$MHz | 45 | | 55 | % |
| | | w/external CLK | $f \leq 133$MHz | 47 | | 53 | % |
| $t_{EN}$ | Output Enable Time; NOTE 5 | | | | | 10 | ns |
| $t_{DIS}$ | Output Disable Time; NOTE 5 | | | | | 10 | ns |

NOTE 1: Measured from $V_{DD}$/2 of the input to $V_{DDO}$/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}$/2.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
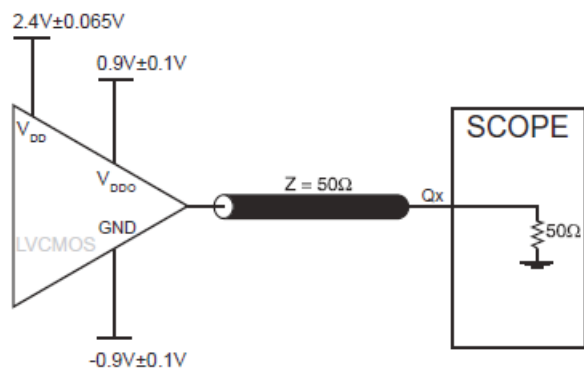
## TYPICAL PHASE NOISE AT 25MHz @ 3.3V/3.3V



**25MHz**
RMS Phase Jitter (Random)
12kHz to 10MHz = 0.39ps (typical)

Raw Phase Noise Data

**OFFSET FREQUENCY (Hz)**

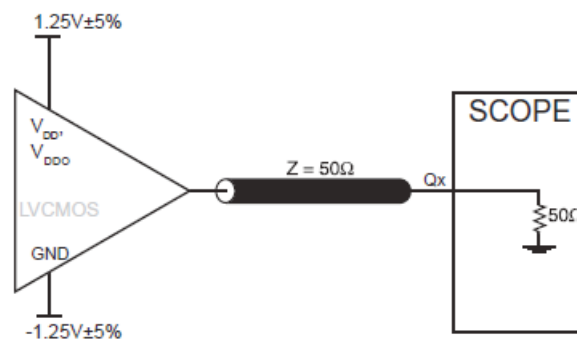# PARAMETER MEASUREMENT INFORMATION



**3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT**
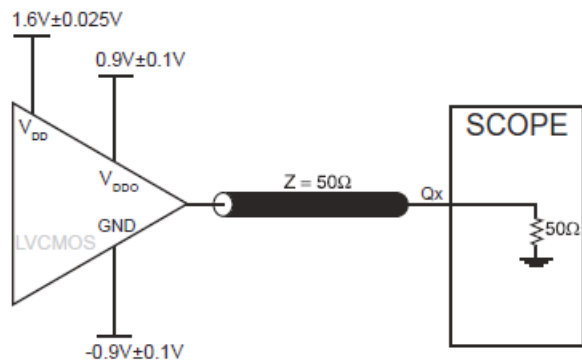


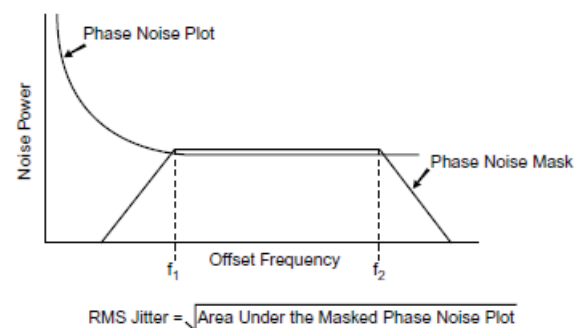**3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT**



**3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT**

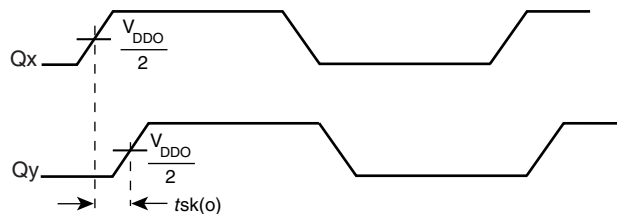

**2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT**



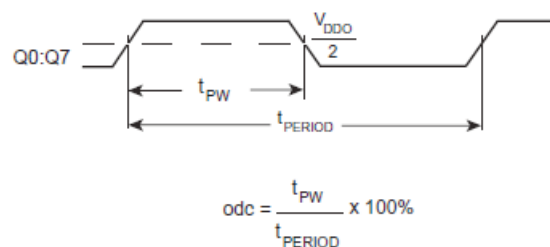**2.5V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT**



$$RMS \ Jitter = \sqrt{Area \ Under \ the \ Masked \ Phase \ Noise \ Plot}$$

**RMS PHASE JITTER**

**OUTPUT SKEW**

$Qx$ — $\dfrac{V_{DDO}}{2}$

$Qy$ — $\dfrac{V_{DDO}}{2}$

$t_{sk(o)}$

**PART-TO-PART SKEW**

PART 1 $Qx$ — $\dfrac{V_{DDO}}{2}$

PART 2 $Qy$ — $\dfrac{V_{DDO}}{2}$

$t_{sk(pp)}$

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

$Q0:Q7$ — $\dfrac{V_{DDO}}{2}$

$t_{PW}$

$t_{PERIOD}$

$$odc = \dfrac{t_{PW}}{t_{PERIOD}} \times 100\%$$

**OUTPUT RISE/FALL TIME**

Clock Outputs

80%   80%

20%   20%

$t_R$   $t_F$

**PROPAGATION DELAY**

CLK — $\dfrac{V_{DD}}{2}$

$Q0:Q7$ — $\dfrac{V_{DDO}}{2}$

$t_{PD}$
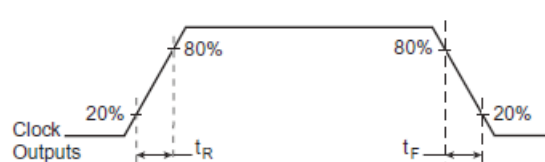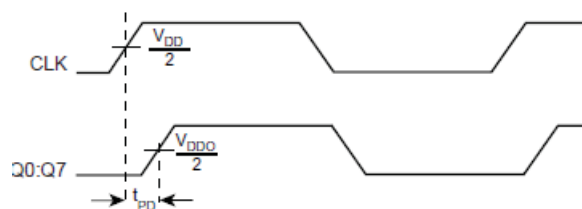
# APPLICATION INFORMATION

## CRYSTAL INPUT INTERFACE

*Figure 1* shows an example of 83908I-02 crystal interface with a parallel resonant crystal. The frequency accuracy can be fine tuned by adjusting the C1 and C2 values. For a parallel crystal with loading capacitance CL = 18pF, we suggest C1 and C2 = 15pF to start with. These values may be slightly fine tuned further to optimize the frequency accuracy for different board layouts. Slightly increasing the C1 and C2 values will slightly reduce the frequency. Slightly decreasing the C1 and C2 values will slightly increase the frequency. For the oscillator circuit below, R1 can be used, but is not required. For new designs, it is recommended that R1 not be used.
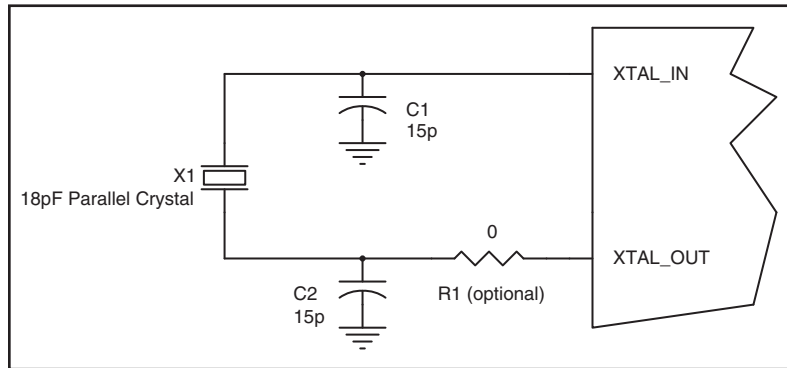


**FIGURE 1. Crystal Input Interface**

## LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 2.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.
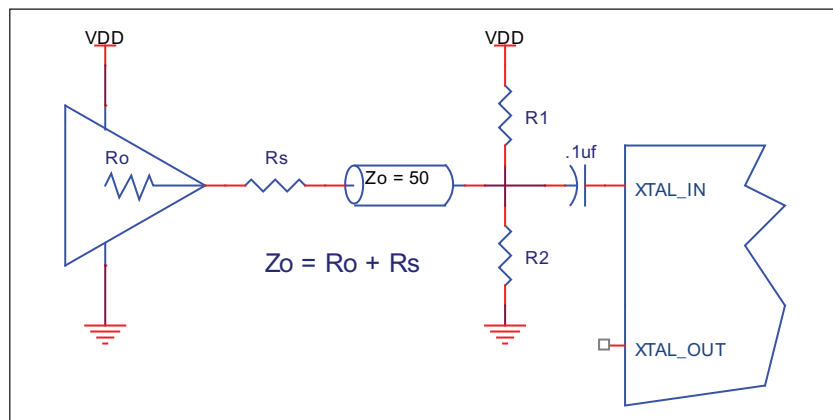


**FIGURE 2. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE**

## RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

### INPUTS:

**CLK INPUT**
For applications not requiring the use of the clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

**CRYSTAL INPUTS**
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT should be tied to ground. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground and from XTAL_OUT to ground.

**LVCMOS CONTROL PINS**
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### OUTPUTS:

**LVCMOS OUTPUTS**
All unused LVCMOS output can be left floating. There should be no trace attached.

# RELIABILITY INFORMATION

**TABLE 7. θ$_{JA}$ VS. AIR FLOW TABLE FOR 24 LEAD TSSOP**

| | | | |
|---|---|---|---|
| **θ$_{JA}$ by Velocity (Meters per Second)** | | | |
| | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 87.8°C/W | 83.5°C/W | 81.3°C/W |

**TRANSISTOR COUNT**

The transistor count for 83908I-02 is: 277

# PACKAGE OUTLINE AND DIMENSIONS
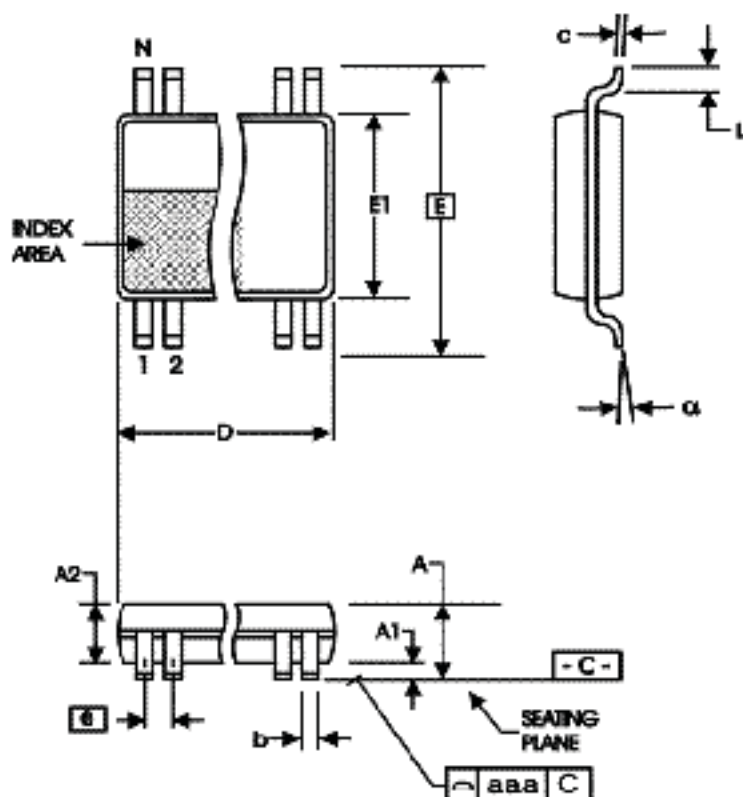
**PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP**



**TABLE 8. PACKAGE DIMENSIONS**

| SYMBOL | Millimeters | |
|---|---|---|
| | **Minimum** | **Maximum** |
| N | 24 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 7.70 | 7.90 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MO-153

### TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 83908AGI-02LF | ICS83908AI02L | 24 lead "Lead Free" TSSOP | Tube | -40°C to +85°C |
| 83908AGI-02LFT | ICS83908AI02L | 24 lead "Lead Free" TSSOP | Tape and Reel | -40°C to +85°C |

REVISION HISTORY SHEET

| Rev | Table | Page | Description of Change | Date |
|------|-------|------|-----------------------|------|
| A | T9 | 14 | Ordering Information - removed leaded devices.<br><br>Updated datasheet format. | 3/27/15 |
| A | T9 | 14 | Ordering Information - Deleted LF note below table.<br>Updated header and footer | 3/17/16 |

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