FemtoClock® NG Crystal-to-LVCMOS/ LVTTL Clock Synthesizer

ICS840N011I

DATASHEET

General Description

The ICS840N011I is an LVCMOS/LVTTL clock synthesizer designed for Fibre Channel applications. The device generates a 106.25MHz clock signal from a 26.5625MHz crystal or a 100MHz clock signal from a 25MHz crystal with excellent phase jitter performance. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency, low phase noise performance and low power consumption and high power supply noise rejection.The device supports 2.5V or 3.3V voltage supply and is packaged in a small, lead-free (RoHS 6) 8-lead TSSOP package. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

Frequency Table

f_{XTAL} (MHz)	Output Frequency (MHz)
25	100
26.5625	106.25
30.72	122.88
31.25	125

Function Table

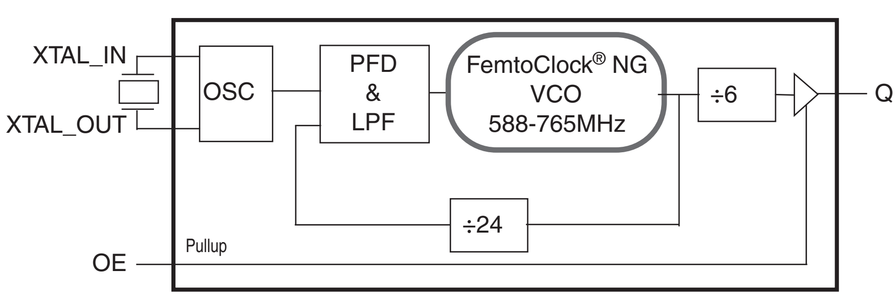
Input	
OE	Output Enable
0	Output Q is disabled in high-impedance state
1 (default)	Output Q is enabled.

NOTE: OE is an asynchronous control.

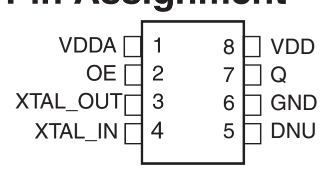
Features

- Fourth generation FemtoClock® NG technology
- 106.25MHz output clock synthesized from a 26.5625MHz fundamental mode crystal
- One 2.5V or 3.3V LVCMOS/LVTTL clock output
- Crystal interface designed for a 12pF parallel resonant crystal
- RMS phase jitter @ 100MHz, using a 25MHz crystal (637kHz - 10MHz): 0.185ps (maximum)
- LVCMOS/LVTTL interface level for the output enable input
- Full 2.5V or 3.3V supply voltage
- Lead-free (RoHS 6) packaging
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



ICS840N011I
8-lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DDA}	Power		Analog power supply.
2	OE	Input	Pullup	Output enable pin. LVCMOS interface levels.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	DNU			Do not use. Do not connect.
6	GND	Power		Power supply ground.
7	Q	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
8	V_{DD}	Power		Core supply pin.

NOTE: *Pullup* refers to an internal input resistor. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	OE		3.5		pF
C_{PD}	Power Dissipation Capacitance	V_{DD} = 3.465V		11		pF
		V_{DD} = 2.625V		9		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
R_{OUT}	Output Impedance	V_{DD} = 3.3V		15		Ω
		V_{DD} =2.5V		19		Ω

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	3.63V
Inputs, V_I XTAL_IN Other Inputs	 0V to 2V -0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	117°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.18	3.3	V_{DD}	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.18	2.5	V_{DD}	V
I_{DDA}	Analog Supply Current				18	mA
I_{DD}	Power Supply Current				67	mA

Table 3B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	OE	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	OE	V_{DD} = 3.465V 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1	Q	V_{DD} = 3.465V	2.6			V
			V_{DD} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	Q	V_{DD} = 3.465V or 2.625V			0.5	V

NOTE 1: Output terminated with 50Ω to V_{DD} / 2. See Parameter Measurement Information Section, *LVCMOS Output Load Test Circuit Diagrams.*

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		24.50	26.5625	31.88	MHz
Equivalent Series Resistance (ESR)				80	Ω
Shunt Capacitance				7	pF
Capacitive Load (C_L)			12		pF

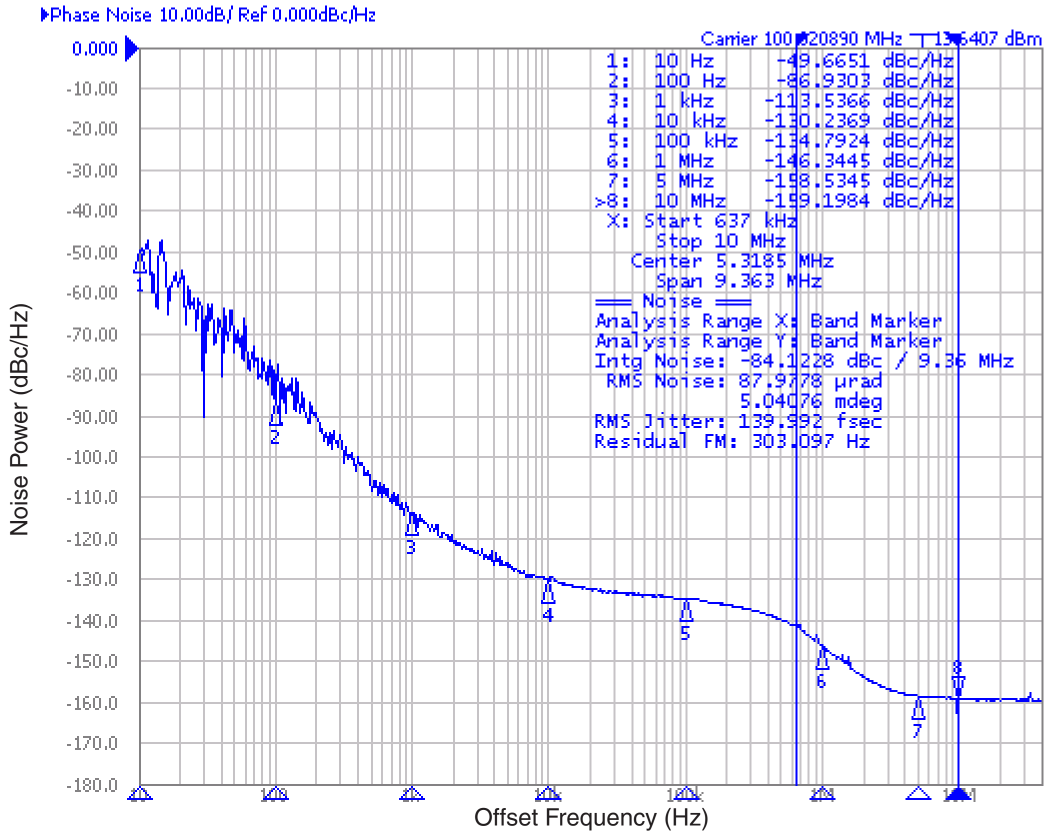
AC Characteristics

Table 5. AC Characteristics, V_{DD} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

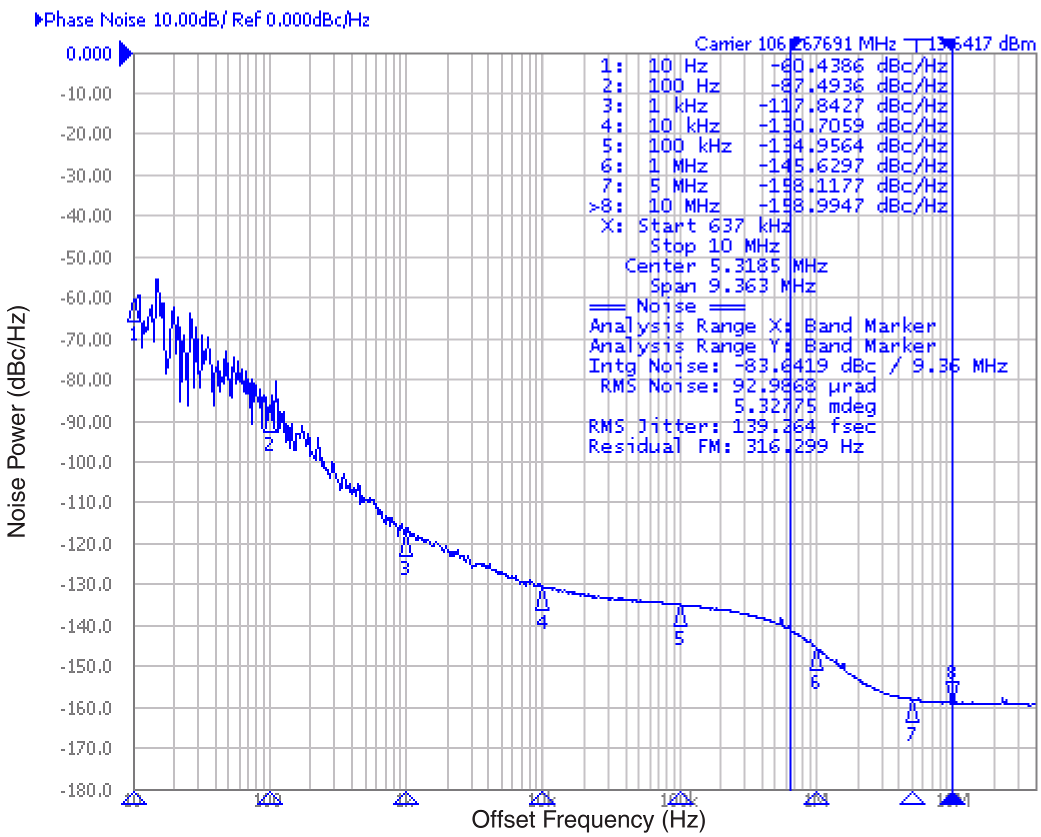
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		98.00	106.25	127.52	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	f_{OUT} = 100MHz, 25MHz Crystal, Integration Range: 637kHz – 10MHz		0.140	0.185	ps
		f_{OUT} = 106.25MHz, 26.5625MHz Crystal, Integration Range: 637kHz – 10MHz		0.139	0.177	ps
Φ_N	Single-Side Band Noise Power	f_{OUT} = 106.25MHz, Offset: 10Hz		-60.4		dBc/Hz
		f_{OUT} = 106.25MHz, Offset: 100Hz		-87.4		dBc/Hz
		f_{OUT} = 106.25MHz, Offset: 1kHz		-117.8		dBc/Hz
		f_{OUT} = 106.25MHz, Offset: 10kHz		-130.7		dBc/Hz
		f_{OUT} = 106.25MHz, Offset: 100kHz		-134.9		dBc/Hz
		f_{OUT} = 106.25MHz, Offset: 1MHz		-145.6		dBc/Hz
		f_{OUT} = 106.25MHz, Offset: 10MHz		-158.9		dBc/Hz
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		600	ps
odc	Output Duty Cycle		48		52	%

NOTE: Characterized with 25MHz, 26.5625MHz, 30.72MHz and 31.25MHz crystals.
NOTE 1: Please refer to the phase noise plots.

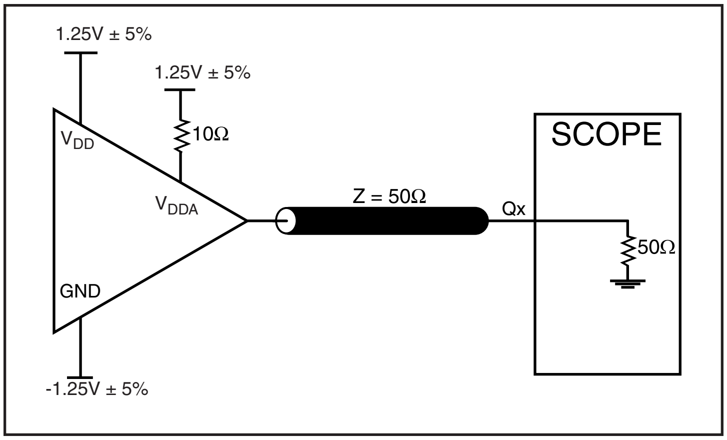
Typical Phase Noise at 100MHz (637kHz - 10MHz)



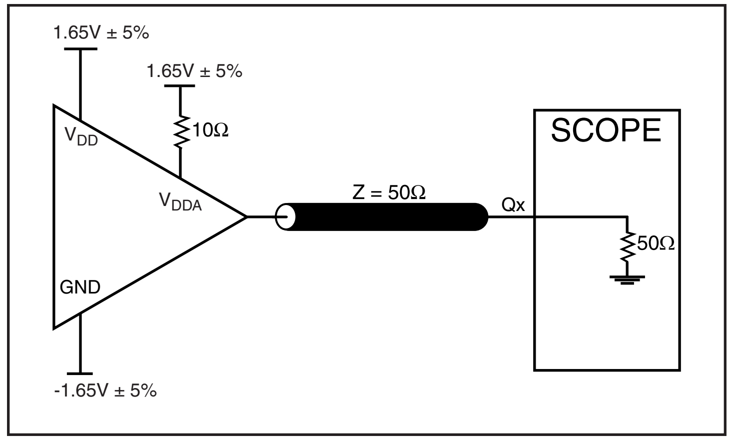
Typical Phase Noise at 106.25MHz (637kHz - 10MHz)



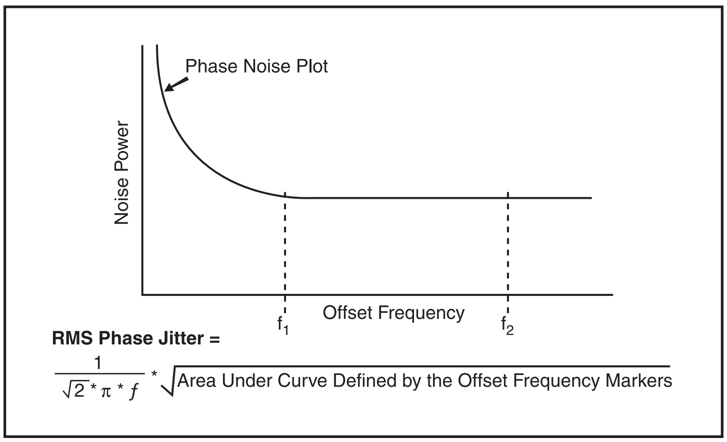
Parameter Measurement Information



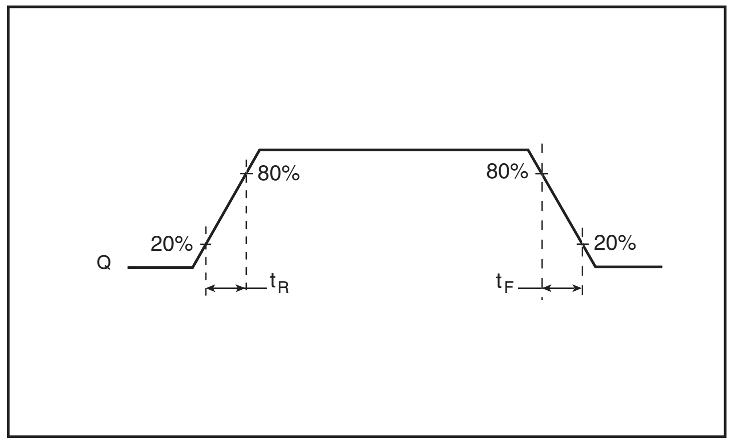
2.5V LVCMOS/LVTTL Output Load AC Test Circuit



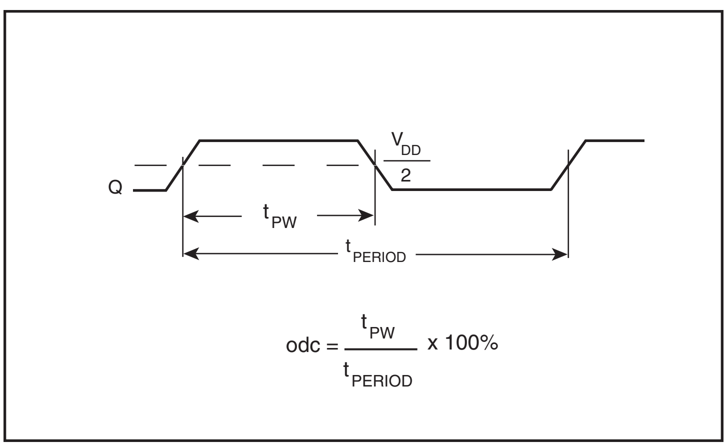
3.3V LVCMOS/LVTTL Output Load AC Test Circuit



RMS Phase Jitter



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Applications Information

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

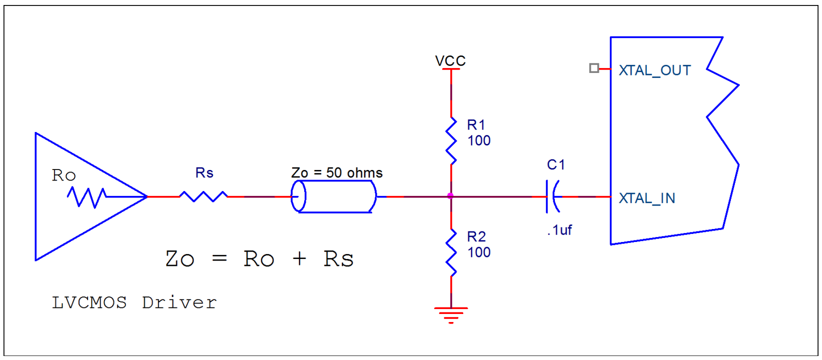


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

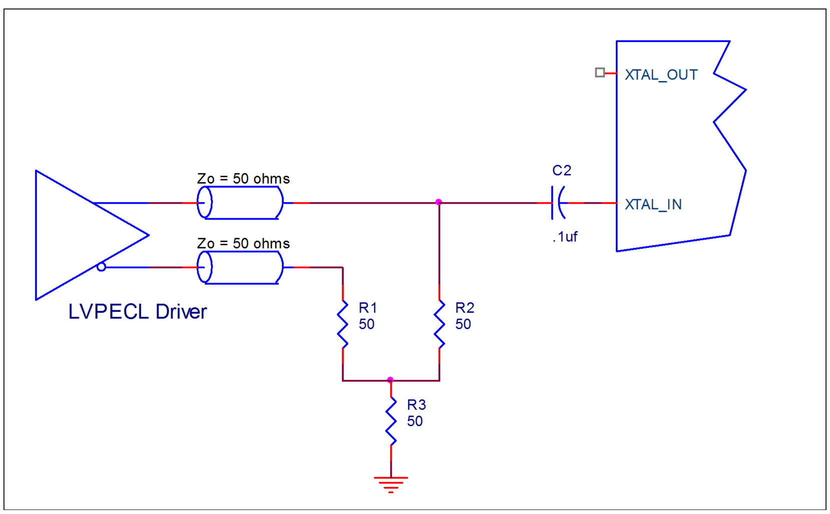


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

Schematic Layout

Figure 2 shows an example ICS840N011I application schematic in which the device is operated at $V_{DD} = V_{DDA} = +3.3V$. The schematic example focuses on functional connections and is intended as an example only and may not represent the exact user configuration. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. For example OE can be configured from an FPGA instead of set with pull up and pull down resistors as shown.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise, so to achieve optimum jitter performance isolation of the V_{DD} pin from power supply is required. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor on the V_{DD} pin must be placed on the device side with direct return to the ground plane though vias. The remaining filter components can be on the opposite side of the PCB.

Power supply filter component recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

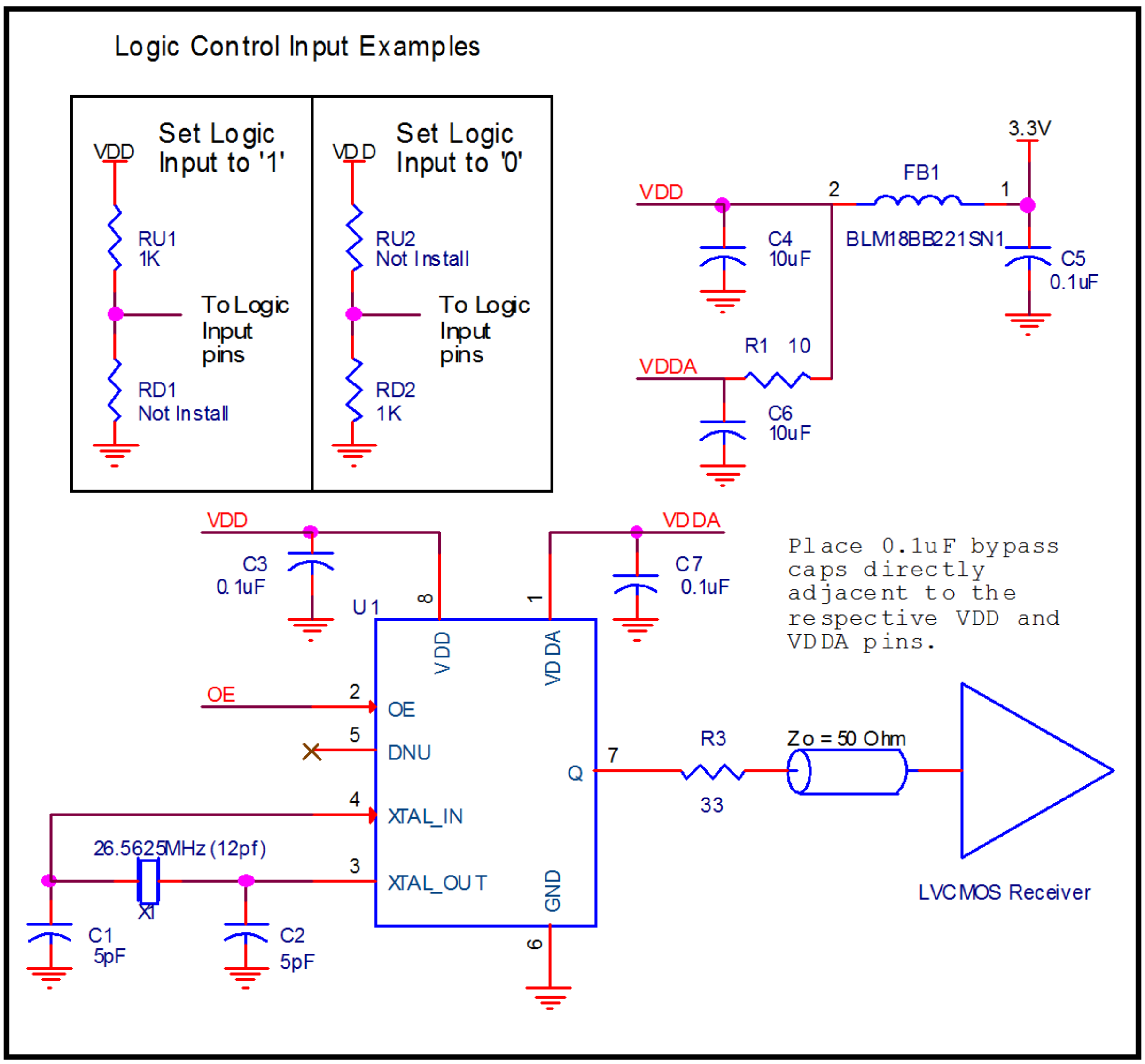


Figure 2. ICS840N011I Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS840N011I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS840N011I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX}$ = V_{DD_MAX} * (I_{DD} + I_{DDA}) = 3.465V *(67mA + 18mA) = **294.53mW**
- Output Impedance R_{OUT} Current due to Loading 50Ω to $V_{DD}/2$
  Output Current I_{OUT} = V_{DD_MAX} / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 15Ω)] = **26.7mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * $(I_{OUT})^2$ = 15Ω * $(26.7mA)^2$ = **10.7mW**
- Total Power (R_{OUT}) = 10.7mW * 1 = **10.7mW**

Dynamic Power Dissipation at 125MHz

Power (125MHz) = C_{PD} * Frequency * $(V_{DD})^2$ = 11pF * 125MHz * $(3.465V)^2$ = **16.51mW**

Total Power (125MHz) = 16.51mW * 1 = **16.51mW**

Total Power Dissipation

- **Total Power**
  = Power $(core)_{MAX}$ + Power (R_{OUT}) + Power (125MHz)
  = 294.53mW + 10.7mW + 16.51mW
  = 321.74mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance q_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 117°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.322W *117°C/W = 122.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} by Velocity	
Meters per Second	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	117°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 8-lead TSSOP

θ_{JA} vs. Air Flow	
Meters per Second	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	117°C/W

Transistor Count

The transistor count for ICS840N011I is: 24,811

Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

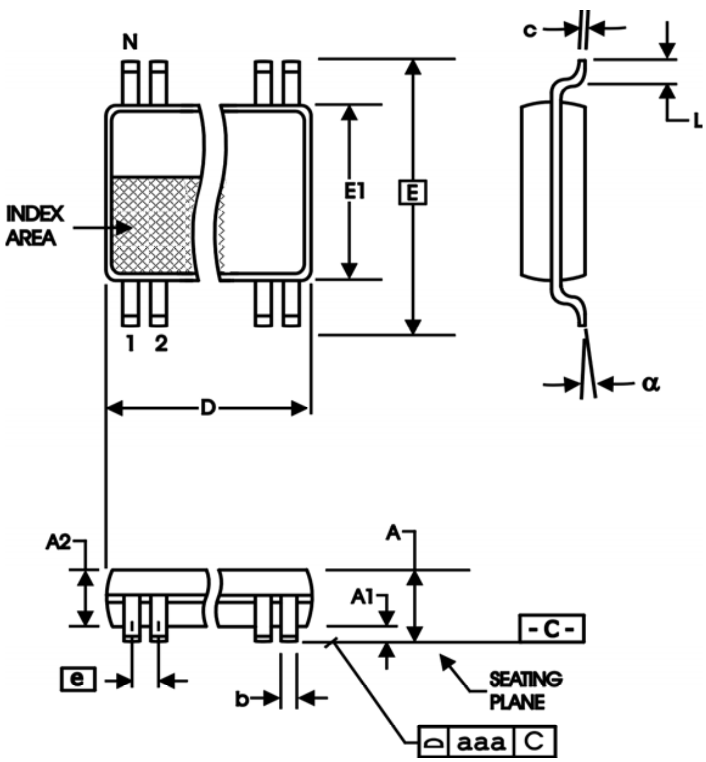


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840N011BGILF	11BIL	Lead-Free, 8-lead TSSOP	Tube	-40°C to 85°C
840N011BGILFT	11BIL	Lead-Free, 8-lead TSSOP	Tape & Reel	-40°C to 85°C

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