

General Description

The 840NT4 is a PLL-based clock generator designed to interface with Freescale B4/T4 Processor systems. The clock generator offers low jitter, low-skew clock outputs, frequency margining (0.025 - 0.312MHz step granularity), and spread spectrum clocking that meets the ever-growing demands of Freescale's next generation processors.

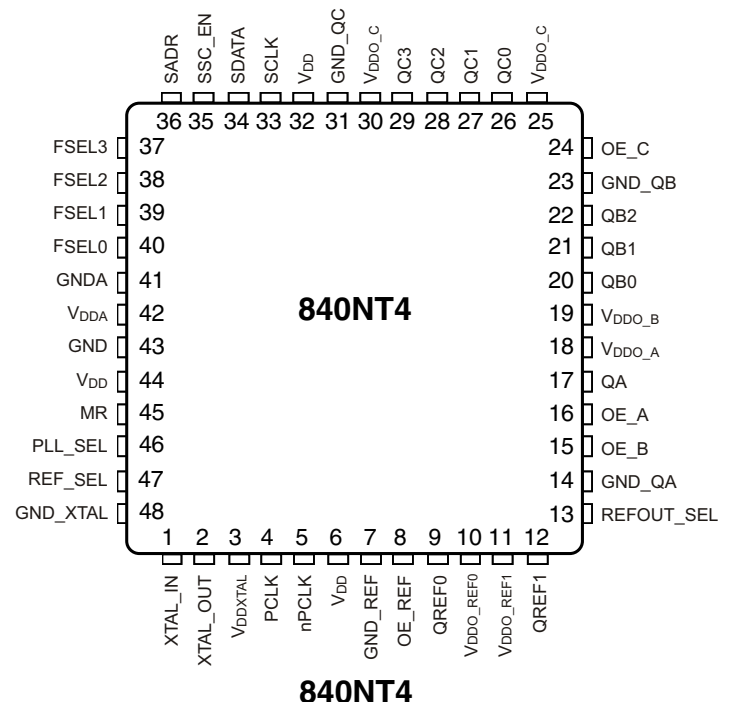
Features

- Ten LVCMOS clock outputs: four system clocks, four DDR clocks, one RTC output, and one 25MHz reference clock
- Selectable input reference: crystal oscillator interface or differential LVPECL input
- Output Frequency Range: 25MHz - 200MHz
- Serial Interface: I²C programmable
- Frequency Margining in <0.312MHz steps
- Spread spectrum for EMI reduction
- VCO range: 2GHz – 2.4GHz
- Voltage supply modes:
Core (V_{DD}, V_{DDXTAL}, V_{DDA}) all core voltages must be identical
Output (V_{DDO_A}, V_{DDO_B}, V_{DDO_C}, V_{DDO_REF0}, V_{DDO_REF1})
Core / Output
3.3V / 3.3V
3.3V / 2.5V
3.3V / 1.8V
2.5V / 2.5V
2.5V / 1.8V
- Output voltage levels are independently selectable
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

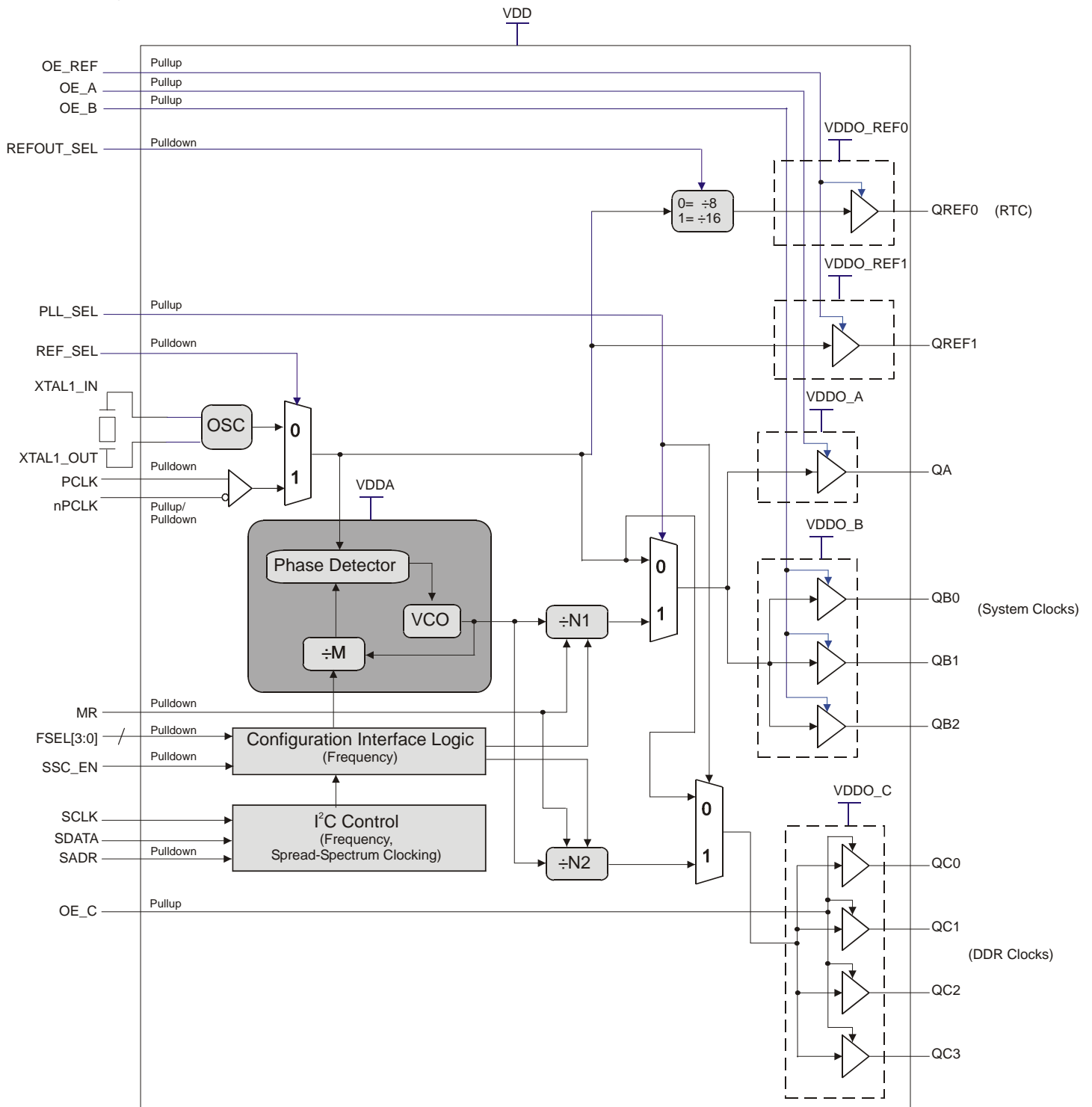
Output Frequency Reference Table

| XTAL (MHz) | FSEL[3:0] | SYSCLK QA & QB (MHz) | DDRCLK QC (MHz) |
|------------|-----------|----------------------|-----------------|
| 25 | 0000 | 66.67 | 66.67 |
| 25 | 0001 | 66.67 | 100 |
| 25 | 0010 | 66.67 | 125 |
| 25 | 0011 | 66.67 | 133.33 |
| 25 | 0100 | 100 | 66.67 |
| 25 | 0101 | 100 | 100 |
| 25 | 0110 | 100 | 125 |
| 25 | 0111 | 100 | 133.33 |
| 25 | 1000 | 125 | 66.67 |
| 25 | 1001 | 125 | 100 |
| 25 | 1010 | 125 | 125 |
| 25 | 1011 | 125 | 133.33 |
| 25 | 1100 | 133.33 | 66.67 |
| 25 | 1101 | 133.33 | 100 |
| 25 | 1110 | 133.33 | 125 |
| 25 | 1111 | 133.33 | 133.33 |

Pin Assignment



Block Diagram



Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|----------------|--|--------|---------------------|---|
| 1, 2 | XTAL_IN XTAL_OUT | Input | | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. |
| 6, 32, 44 | V _{DD} | Power | | Core supply pins. |
| 3 | V _{DDXTAL} | Power | | Power supply pin for crystal oscillator. |
| 4 | PCLK | Input | Pulldown | Non-inverting external 25MHz differential LVPECL reference input. LVPECL input levels. |
| 5 | nPCLK | Input | Pullup/ Pulldown | Inverting external 25MHz differential LVPECL reference input. LVPECL input levels. |
| 7 | GND_REF | Power | | Power supply ground for QREF clock outputs. |
| 8 | OE_REF | Input | Pullup | Output enable for QREFx clock outputs. The QREFx outputs are placed in a high-impedance mode on disable. LVCMOS/LVTTL interface levels. |
| 9 | QREF0 | Output | | Single-ended RTC clock output. LVCMOS/LVTTL interface levels. |
| 10, 11 | V _{DDO_REF0} , V _{DDO_REF1} | Power | | Output power supply for QREF0 and QREF1 outputs. |
| 12 | QREF1 | Output | | Single-ended reference clock output. LVCMOS/LVTTL interface levels. |
| 13 | REFOUT_SEL | Input | Pulldown | Selects the real-time clock output frequency as defined in Table 3B. LVCMOS/LVTTL interface levels. |
| 14 | GND_QA | Power | | Power supply ground for QA outputs. |
| 15 | OE_B | Input | Pullup | Output enable for Bank QBx clock outputs. The output bank is placed in a high-impedance mode on disable. LVCMOS/LVTTL interface levels. |
| 16 | OE_A | Input | Pullup | Output enable for QA clock output. The QA output is placed in a high-impedance mode on disable. LVCMOS/LVTTL interface levels. |
| 17 | QA | Output | | Single-ended system clock output. LVCMOS interface levels. |
| 18 | V _{DDO_A} | Power | | Output power supply for QA clock output. |
| 19 | V _{DDO_B} | Power | | Output power supply for Bank QBx clock outputs. |
| 20, 21, 22 | QB0, QB1, QB2 | Output | | Single-ended system clock outputs. LVCMOS/ LVTL interface levels. |
| 23 | GND_QB | Power | | Power supply ground for QB outputs. |
| 24 | OE_C | Input | Pullup | Output enable for Bank C outputs. The output bank is placed in a high-impedance mode on disable. LVCMOS/LVTTL interface levels. |
| 25, 30 | V _{DDO_C} | Power | | Output power supply for Bank QCx outputs. |
| 26, 27, 28, 29 | QC0, QC1, QC2, QC3 | Output | | Single-ended DDR clock outputs. LVCMOS/ LVTL interface levels. |
| 31 | GND_QC | Power | | Power supply ground for QC outputs. |
| 33 | SCLK | Input | | I ² C clock input. LVCMOS/LVTTL interface levels. |
| 34 | SDATA | Input | | I ² C data input/ output. Input: LVCMOS/ LVTL interface levels. Output: open drain. |
| 35 | SSC_EN | Input | Pulldown | SSC control pin. SSC is enabled when SSC_EN is HIGH. LOW disables SSC. See Table 3C. LVCMOS/LVTTL interface levels. |
| 36 | SADR | Input | Pulldown | I ² C unique address select pin. LVCMOS/LVTTL interface levels. |

Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|----------------|----------------------------|-------|----------|--|
| 37, 38, 39, 40 | FSEL3, FSEL2, FSEL1, FSEL0 | Input | Pulldown | Selects the System and DDR clock output frequencies as defined in Table 3A. LVCMOS/LVTTL interface levels. Overridden when in Frequency Margining mode (I ² C). |
| 41 | GND _A | Power | | Power supply ground for PLL analog. |
| 42 | V _{DDA} | Power | | Analog supply pin. |
| 43 | GND | Power | | Power supply ground. |
| 45 | MR | Input | Pulldown | Master Reset. Forces QA, Bank B and Bank C outputs to a logic low. Does not affect REF_OUT. LVCMOS/LVTTL interface levels. |
| 46 | PLL_SEL | Input | Pullup | Selects the clock signal that drives the output banks. When LOW, deselects the PLL (PLL Bypass). When HIGH, selects the PLL (PLL enable). LVCMOS/LVTTL interface levels. |
| 47 | REF_SEL | Input | Pulldown | Select input for XTAL (LOW) or PCLK, nPCLK (HIGH). LVCMOS/LVTTL interface levels. |
| 48 | GND_XTAL | Power | | Power supply ground for XTAL. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|--|---|------------------------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | SSC_EN, SADR, MR, REFOUT_SEL, OE_REF, FSEL[3:0], REF_SEL, PLL_SEL, OE_A, OE_B, OE_C | | | 4 | | pF |
| C _{PD} | Power Dissipation Capacitance (per output) | | V _{DDO_X} = 3.465V | | 15 | | pF |
| | | | V _{DDO_X} = 2.625V | | 14 | | pF |
| | | | V _{DDO_X} = 1.89V | | 14 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | | 51 | | kΩ |
| R _{OUT} | Output Impedance | | V _{DDO_X} = 3.3V±5% | | 15 | | Ω |
| | | | V _{DDO_X} = 2.5V±5% | | 19 | | Ω |
| | | | V _{DDO_X} = 1.8V±5% | | 28 | | Ω |

NOTE: V_{DDO_X} denotes, V_{DDO_A}, V_{DDO_B}, V_{DDO_C}, V_{DDO_REF0}, V_{DDO_REF1}.

Function Tables

Table 3A. System & DDR Clock Output Frequency Select Table, FM_EN = "0"

| XTAL (MHz) | FSEL[3:0] | System Clocks (MHz) QA & QB[2:0] | DDR Clocks (MHz) QC[3:0] |
|------------|----------------|-------------------------------------|-----------------------------|
| 25 | 0000 (default) | 66.67 | 66.67 |
| 25 | 0001 | 66.67 | 100 |
| 25 | 0010 | 66.67 | 125 |
| 25 | 0011 | 66.67 | 133.33 |
| 25 | 0100 | 100 | 66.67 |
| 25 | 0101 | 100 | 100 |
| 25 | 0110 | 100 | 125 |
| 25 | 0111 | 100 | 133.33 |
| 25 | 1000 | 125 | 66.67 |
| 25 | 1001 | 125 | 100 |
| 25 | 1010 | 125 | 125 |
| 25 | 1011 | 125 | 133.33 |
| 25 | 1100 | 133.33 | 66.67 |
| 25 | 1101 | 133.33 | 100 |
| 25 | 1110 | 133.33 | 125 |
| 25 | 1111 | 133.33 | 133.33 |

Table 3B. RTC Output Frequency Select Table

| XTAL (MHz) | REFOUT_SEL | Output Divider | QREF0 (MHz) | QREF1 (MHz) |
|------------|-------------|----------------|-------------|-------------|
| 25 | 0 (default) | ÷8 | 3.125 | 25 |
| 25 | 1 | ÷16 | 1.5625 | 25 |

Table 3C. SSC Control Settings

| XTAL (MHz) | SSC_EN | SSC Profile |
|------------|-------------|---|
| 25 | 0 (default) | SSC Off |
| 25 | 1* | Typical -0.5% down-spread, 30kHz – 32kHz, triangular waveform |

NOTE: *SSC_EN = 1. Disables M divider programming when frequency margining is also enabled. N divider programming is still available.

Principles of Operation

Output frequencies are synthesized from an external 25MHz LVPECL or crystal (f_{XTAL}) input. The device contains a 11-bit PLL feedback divider (M) with a prescaler (P) and an 7-bit output divider (N). The output frequency f_{OUT} is calculated using the following equation:

$$f_{OUT} = f_{XTAL} \cdot \frac{M}{P \cdot N}$$

or

$$f_{OUT} = PCLK \cdot \frac{M}{P \cdot N}$$

The M and N PLL-dividers have corresponding I²C registers. These registers can be directly programmed to allow for frequency margining. (See Tables 4E, 4F, 4G, & 4H).

Each I²C configuration register has a default setting determined by the FSEL[3:0] strap pins. The default setting is automatically loaded into the registers (defined in Table 4D) at power up and with the release of MR.

Frequency Margining

The M and N registers are normally configured at power up by the state of the FSEL[3:0] pins. These registers can be overwritten by setting the FM_EN bit to a 1 and then directly writing desired values to the M and N registers. Frequency margining is only allowed with SSC disabled. Enabling SSC will block direct user programming of the M and N registers. See Tables 4F, 4G and 4H for M and N divider coding.

Register Settings

Table 4A. I²C Device Slave Address

| | | | | | | | |
|---|---|---|---|---|---|------|-----|
| 1 | 1 | 0 | 0 | 0 | 0 | SADR | R/W |
|---|---|---|---|---|---|------|-----|

Table 4B. Block Write Operation

| Description | START | Slave Address | Write Bit R/W(0) | ACK | Register Byte Pointer (BP) | ACK | Data Byte (for Register BP) | ACK | Data Byte (for Register BP+1) | ACK | Data Byte (for Register BP+...) | ACK | STOP |
|---------------|-------|---------------|------------------|-----|----------------------------|-----|-----------------------------|-----|-------------------------------|-----|---------------------------------|-----|------|
| Length (bits) | 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |

Table 4C. Block Read Operation

| Description | START | Slave Address | Read Bit R/W(1) | ACK | Register Byte Pointer (BP) | ACK | Data Byte (for Register BP) | ACK | Data Byte (for Register BP+1) | ACK | Data Byte (for Register BP+...) | ACK | STOP |
|---------------|-------|---------------|-----------------|-----|----------------------------|-----|-----------------------------|-----|-------------------------------|-----|---------------------------------|-----|------|
| Length (bits) | 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |

Table 4D. I²C Register Map

| Register Byte | Binary Register Address | Power Up Default D[7:0] | | Register Bit | | | | | | | |
|---------------|-------------------------|-------------------------|---------|--------------|--------------|--------------|--------------|----------|----------|----------------|----------------|
| | | Binary | Decimal | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 00000000 | 00011110 | N1 = 30 | Reserved | N1[6] | N1[5] | N1[4] | N1[3] | N1[2] | N1[1] | Reserved |
| 1 | 00000001 | 00011110 | N2 = 30 | Reserved | N2[6] | N2[5] | N2[4] | N2[3] | N2[2] | N2[1] | Reserved |
| 2 | 00000010 | 01010000 | M = 640 | M[10] | M[9] | M[8] | M[7] | M[6] | M[5] | M[4] | M[3] |
| 3 | 00000011 | 00000000 | | M[2] | M[1] | M[0] | FM_EN | Reserved | Reserved | QREF1 Disabled | QREF0 Disabled |
| 4 | 00000100 | 00001011 | 11 | QC3 Disabled | QC2 Disabled | QC1 Disabled | QC0 Disabled | Reserved | Reserved | Reserved | Reserved |

NOTE: The QREF[0:1], QCx disable bits can be programmed at any time to override and disable the OE_REF and OE_QC per individual outputs. This can be done whether SSC_OFF frequency margining is enabled or disabled. If the OE_REF or OE_QC are set to disable their respective outputs, the I²C bits cannot enable their respective outputs.

Table 4E. I²C Register Function Descriptions

| Bits | Name | Function |
|---------|-----------------------------------|---|
| M[10:0] | Integer Feedback Divider Register | Sets the feedback divider value. Can be set to a value of 4 to 1023. The minimum feedback value is 4. Programming 0x04 would yield a feedback divider of ÷4, 0x05 = ÷5, etc. It should also be noted that with a reference of 25MHz and internally fixed Pre-divider of 8, the values loaded into this register should be between 640 and 768 inclusively in order to remain at or above the minimum VCO frequency of 2.0GHz and at or below the maximum VCO frequency of 2.4GHz. |
| N1[7:0] | Output Divider Register | Sets the output divider for output banks A and B. See Tables 4G and 4H for the output divider coding. |
| N2[7:0] | Output Divider Register | Sets the output divider for output bank C. See Table 4G and 4H for the output divider coding. |
| FM_EN | Frequency Margin Enable Bit | This bit must be set to "1" in order to enable frequency margining using Bytes [3:0]. Spread spectrum must also be OFF in order to use frequency margining. |

Table 4F. PLL Feedback (M) Divider Coding for frequency margin mode, FM_EN = "1"

| Register Bit M[10:0] | |
|----------------------|-------------------------|
| Binary | Decimal |
| 01100000000 | 768 |
| 01011111111 | 767 |
| 01011111110 | 766 |
| | <M, M+/-1, M+/-2,> |
| 01010000010 | 642 |
| 01010000001 | 641 |
| 01010000000 | 640 |

Table 4G. PLL Feedback (M) and Output (N) Divider Coding for frequency margin mode, FM_EN = "1"

| XTAL or PCLK (MHz) | Pre-scaler (P) | Register Bit | | M Divider | Nx Divider | fVCO (MHz) | f _{OUT} (MHz) |
|-----------------------|-------------------|--------------|---------|-----------|------------|------------|------------------------|
| | | M[10:0] | Nx[6:0] | | | | |
| 25 | 8 | 0110000000 | 0001100 | 768 | 12 | 2400 | 200.00 |
| 25 | 8 | 0101000000 | 0001100 | 640 | 12 | 2000 | 166.67 |
| 25 | 8 | 0110000000 | 0001110 | 768 | 14 | 2400 | 171.43 |
| 25 | 8 | 0101000000 | 0001110 | 640 | 14 | 2000 | 142.86 |
| 25 | 8 | 0110000000 | 0010000 | 768 | 16 | 2400 | 150.00 |
| 25 | 8 | 0101000000 | 0010000 | 640 | 16 | 2000 | 125.00 |
| 25 | 8 | 0110000000 | 0010010 | 768 | 18 | 2400 | 133.33 |
| 25 | 8 | 0101000000 | 0010010 | 640 | 18 | 2000 | 111.11 |
| 25 | 8 | 0110000000 | 0010100 | 768 | 20 | 2400 | 120.00 |
| 25 | 8 | 0101000000 | 0010100 | 640 | 20 | 2000 | 100.00 |
| 25 | 8 | 0110000000 | 0011000 | 768 | 24 | 2400 | 100.00 |
| 25 | 8 | 0101000000 | 0011000 | 640 | 24 | 2000 | 83.33 |
| 25 | 8 | 0110000000 | 0011100 | 768 | 28 | 2400 | 85.71 |
| 25 | 8 | 0101000000 | 0011100 | 640 | 28 | 2000 | 71.43 |
| 25 | 8 | 0110000000 | 0100000 | 768 | 32 | 2400 | 75.00 |
| 25 | 8 | 0101000000 | 0100000 | 640 | 32 | 2000 | 62.50 |
| 25 | 8 | 0110000000 | 0100110 | 768 | 38 | 2400 | 63.16 |
| 25 | 8 | 0101000000 | 0100110 | 640 | 38 | 2000 | 52.63 |
| 25 | 8 | 0110000000 | 0101100 | 768 | 44 | 2400 | 54.55 |
| 25 | 8 | 0101000000 | 0101100 | 640 | 44 | 2000 | 45.45 |
| 25 | 8 | 0110000000 | 0110100 | 768 | 52 | 2400 | 46.15 |
| 25 | 8 | 0101000000 | 0110100 | 640 | 52 | 2000 | 38.46 |
| 25 | 8 | 0110000000 | 0111110 | 768 | 62 | 2400 | 38.71 |
| 25 | 8 | 0101000000 | 0111110 | 640 | 62 | 2000 | 32.26 |
| 25 | 8 | 0110000000 | 1001000 | 768 | 72 | 2400 | 33.33 |
| 25 | 8 | 0101000000 | 1001000 | 640 | 72 | 2000 | 27.78 |
| 25 | 8 | 0110000000 | 1010000 | 768 | 80 | 2400 | 30.00 |
| 25 | 8 | 0101000000 | 1010000 | 640 | 80 | 2000 | 25.00 |

NOTE: x = 1 or 2.

NOTE: Nx Divider can only be even numbers 10 through 126.

NOTE: M and Nx dividers can be programmed to achieve granularity of 0.312MHz or finer.

Table 4H. PLL Output Divider (N) Coding for frequency margin mode, FM_EN = "1"

| Register Bit Nx[6:0] | Nx Divider | Output Frequency Range | |
|-------------------------|------------|----------------------------|----------------------------|
| | | f _{OUT,MIN} (MHz) | f _{OUT,MAX} (MHz) |
| 0001100 | 12 | 166.67 | 200.00 |
| 0001110 | 14 | 142.86 | 171.43 |
| 0010000 | 16 | 125.00 | 150.00 |
| 0010010 | 18 | 111.11 | 133.33 |
| 0010100 | 20 | 100.00 | 120.00 |
| 0011000 | 24 | 83.33 | 100.00 |
| 0011100 | 28 | 71.43 | 85.71 |
| 0100000 | 32 | 62.50 | 75.00 |
| 0100110 | 38 | 52.63 | 63.16 |
| 0101100 | 44 | 45.45 | 54.55 |
| 0110100 | 52 | 38.46 | 46.15 |
| 0111110 | 62 | 32.26 | 38.71 |
| 1001000 | 72 | 27.78 | 33.33 |
| 1010000 | 80 | 25.00 | 30.00 |

NOTE: x = 1 or 2.

NOTE: Nx Divider can only be even numbers 10 through 126.

NOTE: M and Nx dividers can be programmed to achieve granularity of 0.312MHz or finer.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|--|--------------------------------------|
| Supply Voltage, V_{DD} | 3.63V |
| Inputs, V_I XTAL_IN Other Inputs | 0V to 2V -0.5V to $V_{DD} + 0.5V$ |
| Outputs, V_O | -0.5V to $V_{DDO_X} + 0.5V$ |
| Junction Temperature, T_J | 125°C |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: V_{DDO_X} denotes, V_{DDO_A} , V_{DDO_B} , V_{DDO_C} , V_{DDO_REF0} , V_{DDO_REF1} .

DC Electrical Characteristics

Table 5A. Power Supply DC Characteristics, $V_{DD} = V_{DDXTAL} = 3.3V \pm 5\%$, $V_{DDO_X} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|---------------------------|---------------------------|------------------|---------|----------|-------|
| V_{DD} | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDXTAL} | XTAL Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | $V_{DD} - 0.064$ | 3.3 | V_{DD} | V |
| V_{DDO_X} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Power Supply Current | | | 136 | 149 | mA |
| I_{DDXTAL} | XTAL Power Supply Current | | | 40 | 44 | mA |
| I_{DDA} | Analog Supply Current | | | 27 | 32 | mA |
| I_{DDO_X} | Output Supply Current | Outputs in High-Impedance | | 1 | 3 | mA |

NOTE: V_{DDO_X} denotes, V_{DDO_A} , V_{DDO_B} , V_{DDO_C} , V_{DDO_REF0} , V_{DDO_REF1} .

NOTE: I_{DDO_X} denotes, $I_{DDO_A} + I_{DDO_B} + I_{DDO_C} + I_{DDO_REF0} + I_{DDO_REF1}$.

Table 5B. Power Supply DC Characteristics, $V_{DD} = V_{DDXTAL} = 3.3V \pm 5\%$, $V_{DDO_X} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|---------------------------|---------------------------|------------------|---------|----------|-------|
| V_{DD} | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDXTAL} | XTAL Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | $V_{DD} - 0.064$ | 3.3 | V_{DD} | V |
| V_{DDO_X} | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | | | 136 | 149 | mA |
| I_{DDXTAL} | XTAL Power Supply Current | | | 40 | 44 | mA |
| I_{DDA} | Analog Supply Current | | | 27 | 32 | mA |
| I_{DDO_X} | Output Supply Current | Outputs in High-Impedance | | 1 | 3 | mA |

NOTE: V_{DDO_X} denotes, V_{DDO_A} , V_{DDO_B} , V_{DDO_C} , V_{DDO_REF0} , V_{DDO_REF1} .

NOTE: I_{DDO_X} denotes, $I_{DDO_A} + I_{DDO_B} + I_{DDO_C} + I_{DDO_REF0} + I_{DDO_REF1}$.

Table 5C. Power Supply DC Characteristics, $V_{DD} = V_{DDXTAL} = 3.3V \pm 5\%$, $V_{DDO_X} = 1.8V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|---------------------------|---------------------------|------------------|---------|----------|-------|
| V_{DD} | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDXTAL} | XTAL Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | $V_{DD} - 0.064$ | 3.3 | V_{DD} | V |
| V_{DDO_X} | Output Supply Voltage | | 1.71 | 1.8 | 1.89 | V |
| I_{DD} | Power Supply Current | | | 136 | 149 | mA |
| I_{DDXTAL} | XTAL Power Supply Current | | | 40 | 44 | mA |
| I_{DDA} | Analog Supply Current | | | 27 | 32 | mA |
| I_{DDO_X} | Output Supply Current | Outputs in High-Impedance | | 1 | 2 | mA |

NOTE: V_{DDO_X} denotes, V_{DDO_A} , V_{DDO_B} , V_{DDO_C} , V_{DDO_REF0} , V_{DDO_REF1} .

NOTE: I_{DDO_X} denotes, $I_{DDO_A} + I_{DDO_B} + I_{DDO_C} + I_{DDO_REF0} + I_{DDO_REF1}$

Table 5D. Power Supply DC Characteristics, $V_{DD} = V_{DDXTAL} = V_{DDO_X} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|---------------------------|---------------------------|------------------|---------|----------|-------|
| V_{DD} | Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{DDXTAL} | XTAL Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{DDA} | Analog Supply Voltage | | $V_{DD} - 0.056$ | 2.5 | V_{DD} | V |
| V_{DDO_X} | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | | | 135 | 147 | mA |
| I_{DDXTAL} | XTAL Power Supply Current | | | 39 | 43 | mA |
| I_{DDA} | Analog Supply Current | | | 24 | 28 | mA |
| I_{DDO_X} | Output Supply Current | Outputs in High-Impedance | | 1 | 3 | mA |

NOTE: V_{DDO_X} denotes, V_{DDO_A} , V_{DDO_B} , V_{DDO_C} , V_{DDO_REF0} , V_{DDO_REF1} .

NOTE: I_{DDO_X} denotes, $I_{DDO_A} + I_{DDO_B} + I_{DDO_C} + I_{DDO_REF0} + I_{DDO_REF1}$.

Table 5E. Power Supply DC Characteristics, $V_{DD} = V_{DDXTAL} = 2.5V \pm 5\%$, $V_{DDO_X} = 1.8V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|---------------------------|---------------------------|------------------|---------|----------|-------|
| V_{DD} | Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{DDXTAL} | XTAL Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{DDA} | Analog Supply Voltage | | $V_{DD} - 0.056$ | 2.5 | V_{DD} | V |
| V_{DDO_X} | Output Supply Voltage | | 1.71 | 1.8 | 1.89 | V |
| I_{DD} | Power Supply Current | | | 135 | 147 | mA |
| I_{DDXTAL} | XTAL Power Supply Current | | | 39 | 43 | mA |
| I_{DDA} | Analog Supply Current | | | 24 | 28 | mA |
| I_{DDO_X} | Output Supply Current | Outputs in High-Impedance | | 1 | 2 | mA |

NOTE: V_{DDO_X} denotes, V_{DDO_A} , V_{DDO_B} , V_{DDO_C} , V_{DDO_REF0} , V_{DDO_REF1} .

NOTE: I_{DDO_X} denotes, $I_{DDO_A} + I_{DDO_B} + I_{DDO_C} + I_{DDO_REF0} + I_{DDO_REF1}$.

Table 5F. LVCMOS/LVTTL DC Characteristics, $T_A = -40^{\circ}\text{C}$ to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|---------------------|--|---|---------|---------|----------------|---------------|
| V_{IH} | Input High Voltage | | $V_{DD} = 3.3\text{V} \pm 5\%$ | 2 | | $V_{DD} + 0.3$ | V |
| | | | $V_{DD} = 2.5\text{V} \pm 5\%$ | 1.7 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | $V_{DD} = 3.3\text{V} \pm 5\%$ | -0.3 | | 0.8 | V |
| | | | $V_{DD} = 2.5\text{V} \pm 5\%$ | -0.3 | | 0.7 | V |
| I_{IH} | Input High Current | REF_SEL, MR, FSEL[3:0], SSC_EN, REFOUT_SEL, SADR | $V_{DD} = V_{IN} = 3.465\text{V}$ or 2.625V | | | 150 | μA |
| | | OE_A, OE_B, OE_C, OE_REF, PLL_SEL | $V_{DD} = V_{IN} = 3.465\text{V}$ or 2.625V | | | 5 | μA |
| I_{IL} | Input Low Current | REF_SEL, MR, FSEL[3:0], SSC_EN, REFOUT_SEL, SADR | $V_{DD} = 3.465\text{V}$ or 2.625V , $V_{IN} = 0\text{V}$ | -5 | | | μA |
| | | OE_A, OE_B, OE_C, OE_REF, PLL_SEL | $V_{DD} = 3.465\text{V}$ or 2.625V , $V_{IN} = 0\text{V}$ | -150 | | | μA |
| V_{OH} | Output High Voltage | | $V_{DDO_X} = 3.3\text{V} \pm 5\%$; $I_{OH} = -12\text{mA}$ | 2.6 | | | V |
| | | | $V_{DDO_X} = 2.5\text{V} \pm 5\%$; $I_{OH} = -12\text{mA}$ | 1.8 | | | V |
| | | | $V_{DDO_X} = 1.8\text{V} \pm 5\%$; $I_{OH} = -8\text{mA}$ | 1.3 | | | V |
| V_{OL} | Output Low Voltage; | | $V_{DDO_X} = 3.3\text{V} \pm 5\%$ or $2.5\text{V} \pm 5\%$, $I_{OL} = 12\text{mA}$ | | | 0.5 | V |
| | | | $V_{DDO_X} = 1.8\text{V} \pm 5\%$, $I_{OL} = 8\text{mA}$ | | | 0.4 | V |

NOTE: V_{DDO_X} denotes, V_{DDO_A} , V_{DDO_B} , V_{DDO_C} , V_{DDO_REF0} , V_{DDO_REF1} .

Table 5G. LVPECL DC Characteristics, $V_{DD} = V_{DDXTAL} = 3.3\text{V} \pm 5\%$ or $2.5\text{V} \pm 5\%$, $T_A = -40^{\circ}\text{C}$ to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------------------|-------------|---|-----------|---------|----------|---------------|
| I_{IH} | Input High Current | PCLK, nPCLK | $V_{DD} = V_{IN} = 3.465\text{V}$ | | | 150 | μA |
| I_{IL} | Input Low Current | PCLK | $V_{DD} = 3.465\text{V}$, $V_{IN} = 0\text{V}$ | -5 | | | μA |
| | | nPCLK | $V_{DD} = 3.465\text{V}$, $V_{IN} = 0\text{V}$ | -150 | | | μA |
| V_{PP} | Peak-to-Peak Voltage; NOTE 2 | | | 0.3 | | 1.0 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | | GND + 1.5 | | V_{DD} | V |

NOTE 1: Common mode voltage is defined as V_{IH} .

NOTE 2: V_{IL} should not be less than -0.3V and V_{IH} should not be greater than V_{DD} .

Table 6. Input Frequency Characteristics, $V_{DD} = V_{DDXTAL} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-----------------|-------------------|-----------------|---------|---------|---------|-------|
| f_{IN} | Input Frequency | XTAL_IN, XTAL_OUT | | | 25 | | MHz |
| | | PCLK, nPCLK | PLL Bypass | | 25 | 150 | MHz |

Table 7. Crystal Characteristics

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Capacitive Loading (C_L) | | | 12 | 18 | pF |

AC Electrical Characteristics

Table 8A. AC Characteristics (QA, QBx, QCx), $V_{DD} = V_{DDXTAL} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, V_{DDO_A} , V_{DDO_B} , $V_{DDO_C} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$ or $1.8V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|--|--------------------------------------|-------------------------|--|---------|---------|---------|-------|
| f _{OUT} | Output Frequency | | | 25 | | 200 | MHz |
| tsk(b) | Bank Skew; NOTE 1, 2, 4 | | | | | 70 | ps |
| (Φ) _N | Single Side-Band Phase Noise; NOTE 4 | | Offset from Carrier: 500kHz | | -140 | | dBc |
| f _{jit(cc)} | Cycle-to-Cycle Jitter; NOTE 1, 3, 4 | V _{DDO} = 3.3V | FSEL[3:0] = 0000, 0010, 0011, 0100, 0101, 0110, 1001, 1010, 1101, 1111 | | 90 | 300 | ps |
| | | | FSEL[3:0] = 0001, 0111, 1000, 1011, 1100, 1110 | | 260 | 530 | ps |
| | | V _{DDO} = 2.5V | FSEL[3:0] = 0000, 0010, 0011, 0100, 0101, 0110, 1001, 1010, 1101, 1111 | | 60 | 250 | ps |
| | | | FSEL[3:0] = 0001, 0111, 1000, 1011, 1100, 1110 | | 200 | 400 | ps |
| | | V _{DDO} = 1.8V | FSEL[3:0] = 0000, 0010, 0011, 0100, 0101, 0110, 1001, 1010, 1101, 1111 | | 60 | 200 | ps |
| | | | FSEL[3:0] = 0001, 0111, 1000, 1011, 1100, 1110 | | 175 | 350 | ps |
| f _{jit(per)} | Period Jitter, Peak; NOTE 1, 3, 4 | V _{DDO} = 3.3V | FSEL[3:0] = 0000, 0010, 0011, 0100, 0101, 0110, 1001, 1010, 1101, 1111 | | | ±150 | ps |
| | | | FSEL[3:0] = 0001, 0111, 1000, 1011, 1100, 1110 | | | ±265 | ps |
| | | V _{DDO} = 2.5V | FSEL[3:0] = 0000, 0010, 0011, 0100, 0101, 0110, 1001, 1010, 1101, 1111 | | | ±125 | ps |
| | | | FSEL[3:0] = 0001, 0111, 1000, 1011, 1100, 1110 | | | ±200 | ps |
| | | V _{DDO} = 1.8V | FSEL[3:0] = 0000, 0010, 0011, 0100, 0101, 0110, 1001, 1010, 1101, 1111 | | | ±100 | ps |
| | | | FSEL[3:0] = 0001, 0111, 1000, 1011, 1100, 1110 | | | ±175 | ps |
| t _L | PLL Lock Time; NOTE 4 | | | | | 50 | ms |
| odc | Output Duty Cycle; NOTE 4 | | | 40 | | 60 | % |
| tsl(o) | Slew Rate; NOTE 4 | | V _{DDO} = 3.3V; 0.35V _{DDO} – 0.65V _{DDO} | 2.0 | 4.4 | 7.0 | V/ns |
| V _{DDO} = 2.5V; 0.35V _{DDO} – 0.65V _{DDO} | | | 1.0 | 2.9 | 4.0 | V/ns | |
| V _{DDO} = 1.8V; 0.35V _{DDO} – 0.65V _{DDO} | | | 0.7 | 1.5 | 2.2 | V/ns | |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: $V_{DDO} \leq V_{DD}$.

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 2: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

NOTE 3: Jitter performance using XTAL inputs.

NOTE 4: Characterized for frequencies in Table 3A.

Table 8B. AC Characteristics (QREF[0:1]), $V_{DD} = V_{DDXTAL} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, V_{DDO_REF0} , $V_{DDO_REF1} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$ or $1.8V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|---|------------------------------------|--|---------|---------|---------|-------|
| f_{OUT} | Output Frequency; NOTE 1 | QREF0 | | 1.5625 | | 3.125 | MHz |
| | | QREF1 | | | 25 | | MHz |
| $\text{jit}(\theta)$ | RMS Phase Jitter (Random); NOTE 1, 2 | QREF1 | $f_{OUT} = 25\text{MHz}$, Integration Range: 12kHz to 5MHz | | 0.218 | 0.312 | ps |
| odc | Output Duty Cycle; NOTE 3 | | | 40 | | 60 | % |
| $\text{tsl}(o)$ | Slew Rate | QREF1, $f_{OUT} = 25\text{MHz}$ | $V_{DDO} = 3.3V; 0.35V_{DDO} - 0.65V_{DDO}$ | 2.0 | 5.4 | 8.0 | V/ns |
| | | | $V_{DDO} = 2.5V; 0.35V_{DDO} - 0.65V_{DDO}$ | 2.0 | 3.5 | 5.0 | V/ns |
| | | | $V_{DDO} = 1.8V; 0.35V_{DDO} - 0.65V_{DDO}$ | 1.0 | 1.7 | 3.0 | V/ns |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

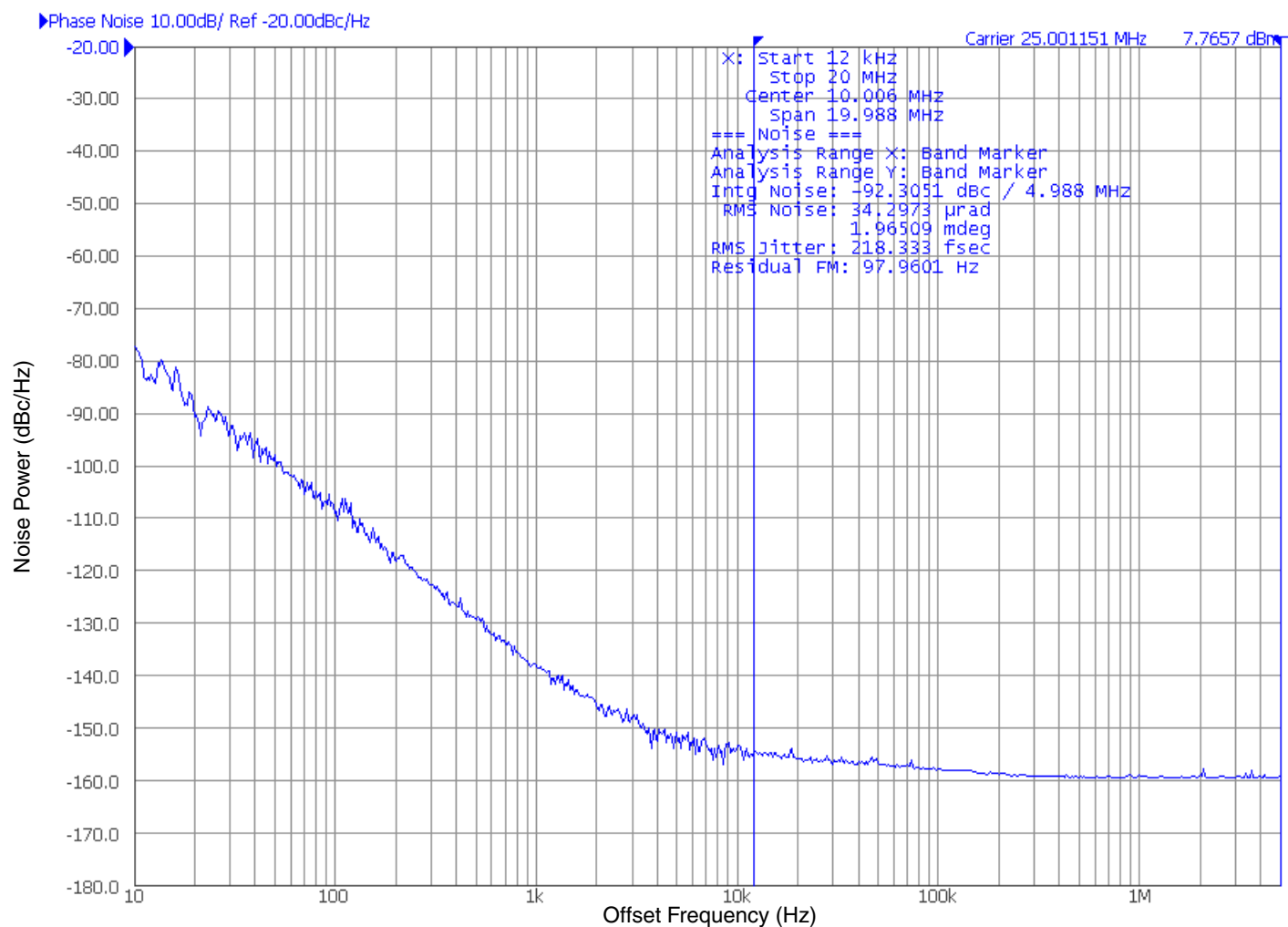
NOTE: $V_{DDO} \leq V_{DD}$.

NOTE 1: Crystal oscillator selected as frequency source.

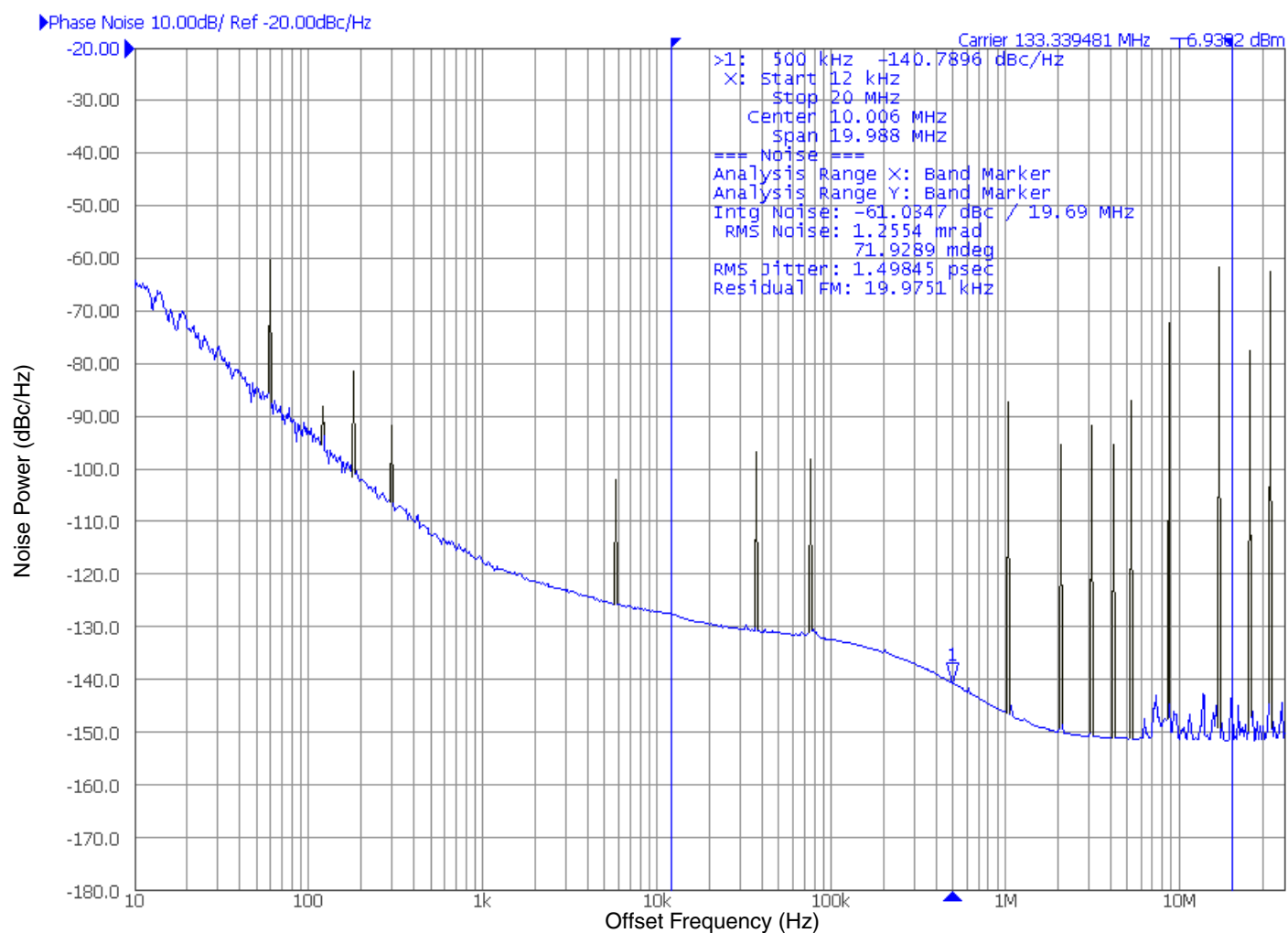
NOTE 2: Refer to phase noise plot. Only applies to QREF1.

NOTE 3: Input duty cycle must be 50%.

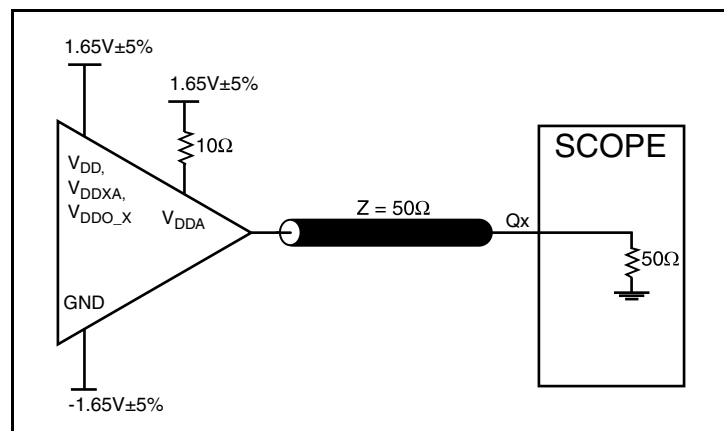
Typical Phase Noise at 25MHz (QREF1 output at 3.3V)



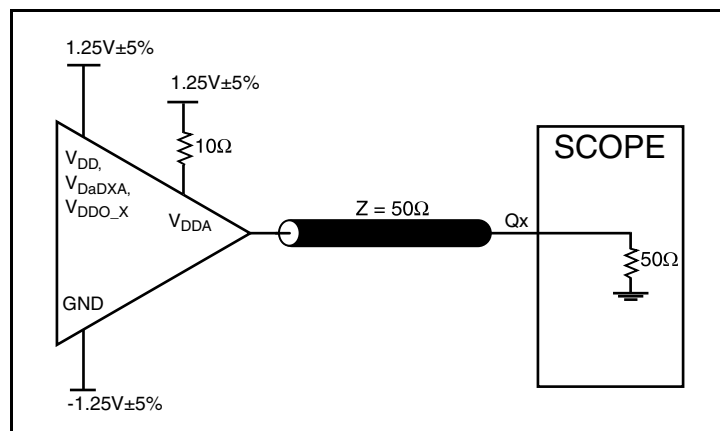
Typical Single-side Band Phase Noise (QB output at 3.3V)



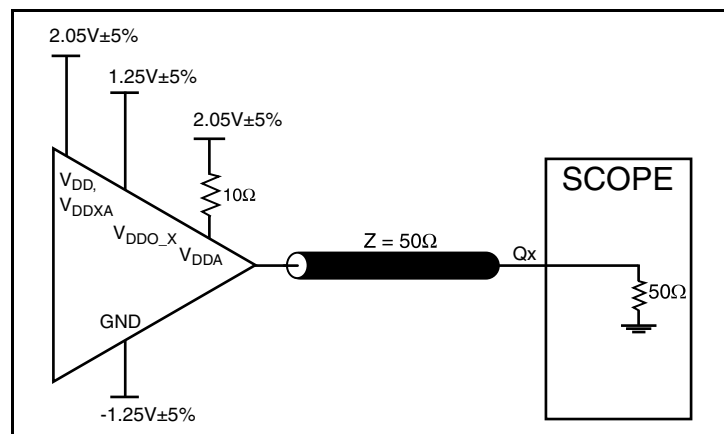
Parameter Measurement Information



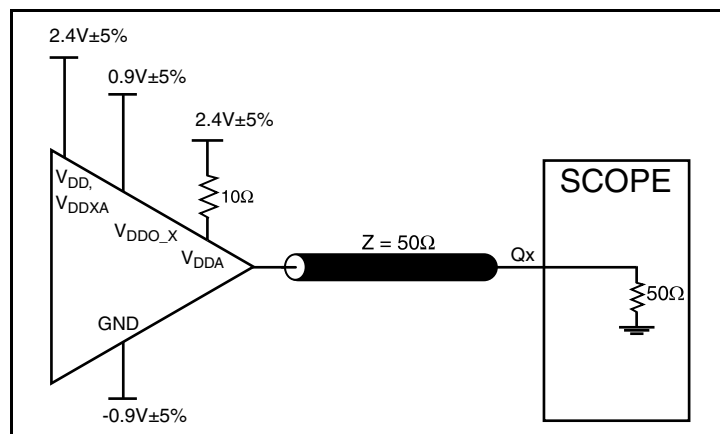
3.3V Core/3.3V LVCMOS Output Load Test Circuit



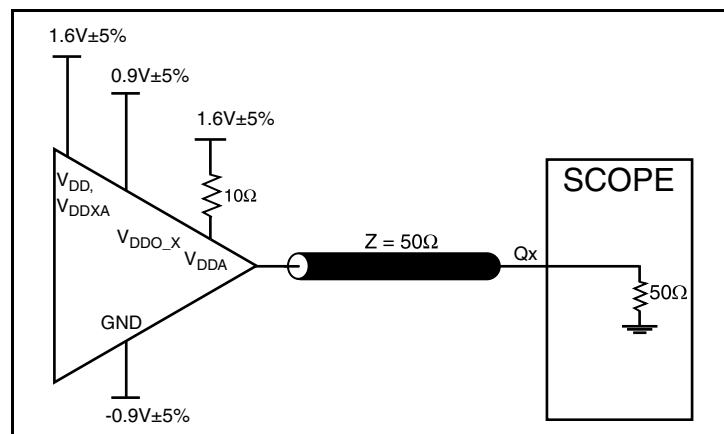
2.5V Core/2.5V LVCMOS Output Load Test Circuit



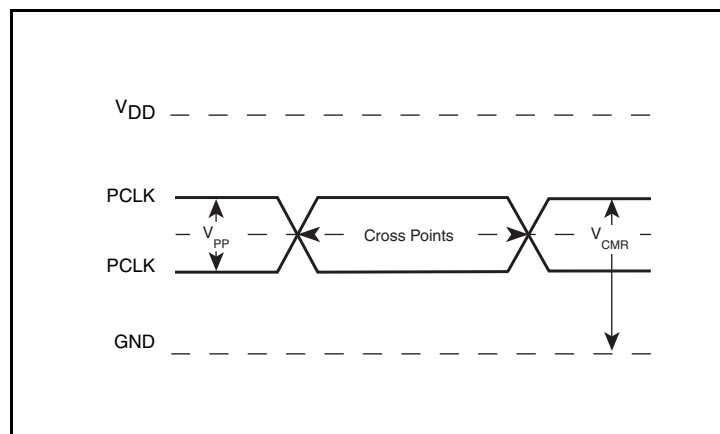
3.3V Core/2.5V LVCMOS Output Load Test Circuit



3.3V Core/1.8V LVCMOS Output Load Test Circuit

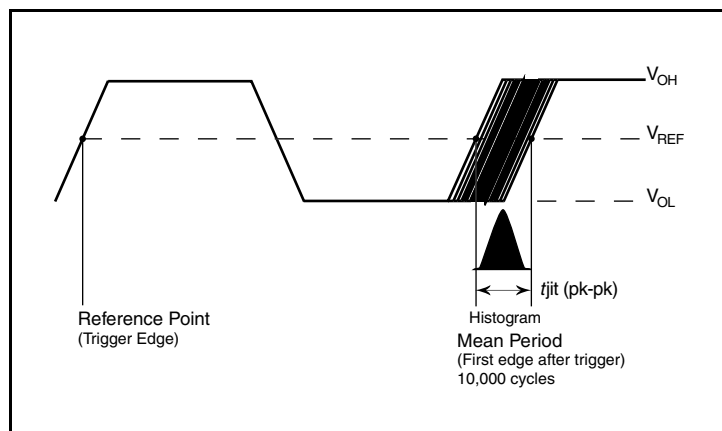


2.5V Core/1.8V LVCMOS Output Load Test Circuit

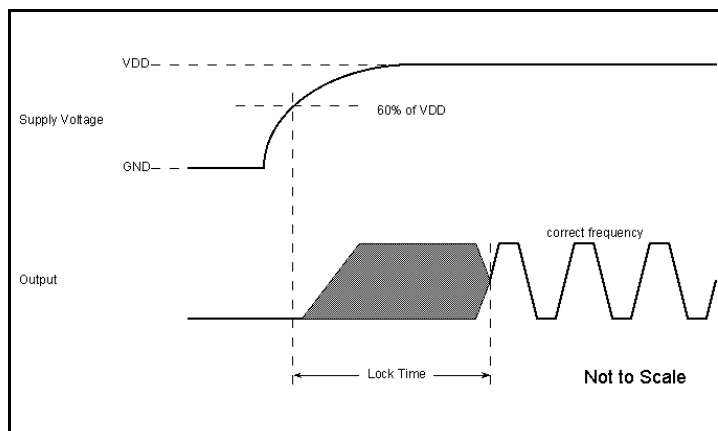


Differential Input Level

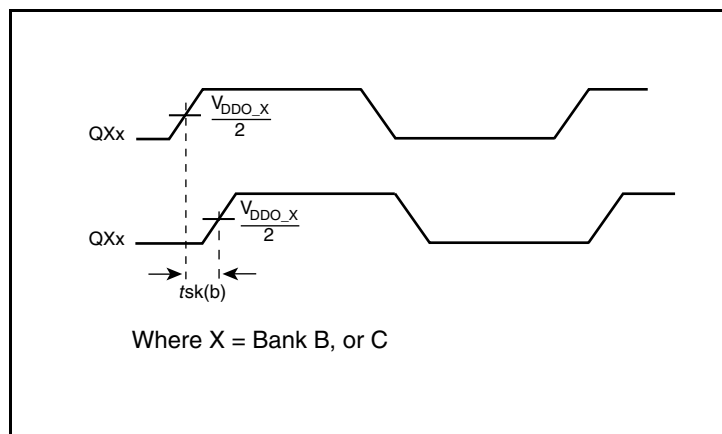
Parameter Measurement Information, continued



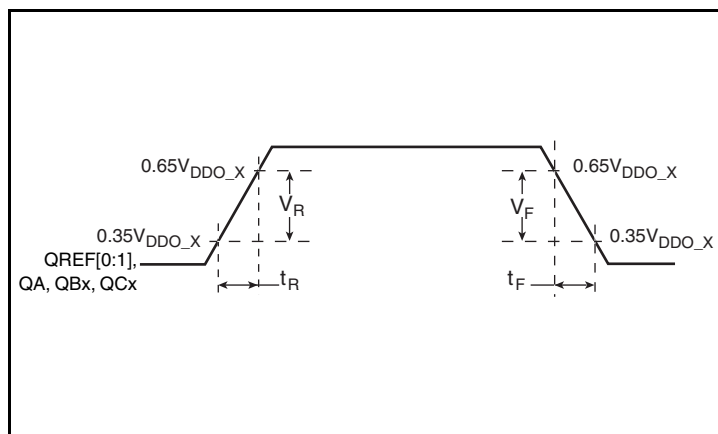
RMS Period Jitter, Peak-to-Peak



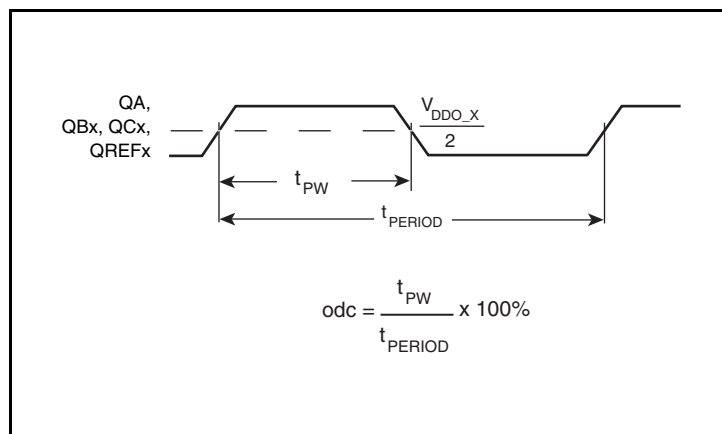
PLL Lock Time



Bank Skew



Slew Rate



Output Duty Cycle/Pulse Width/Period

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

PCLK/nPCLK Inputs

For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from PCLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from XTAL_IN to ground.

Outputs:

LVC MOS Outputs

All unused LVC MOS outputs can be left floating. There should be no trace attached.

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω. This can also be accomplished by removing R_1 and changing R_2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

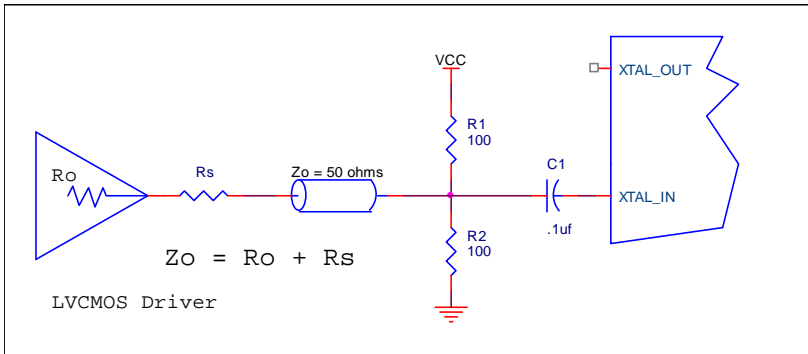


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

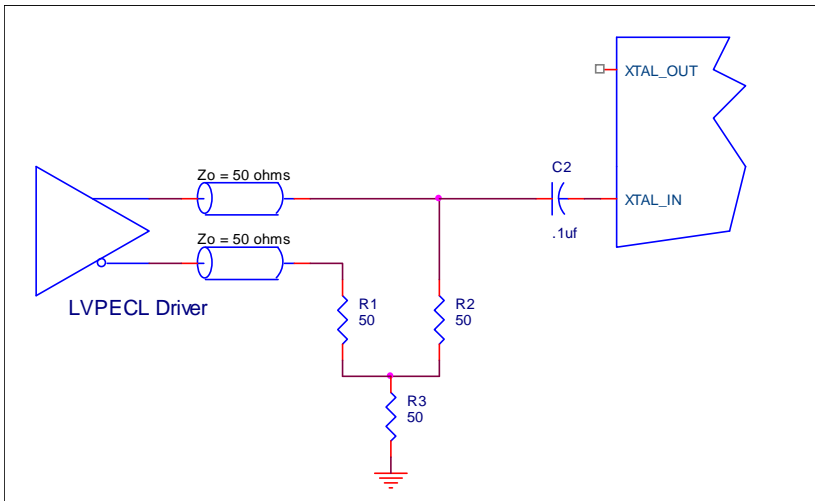


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

LVPECL Clock Input Interface

The PCLK/nPCLK accepts LVPECL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2B show interface examples for the PCLK/nPCLK input driven by the most common driver types. The

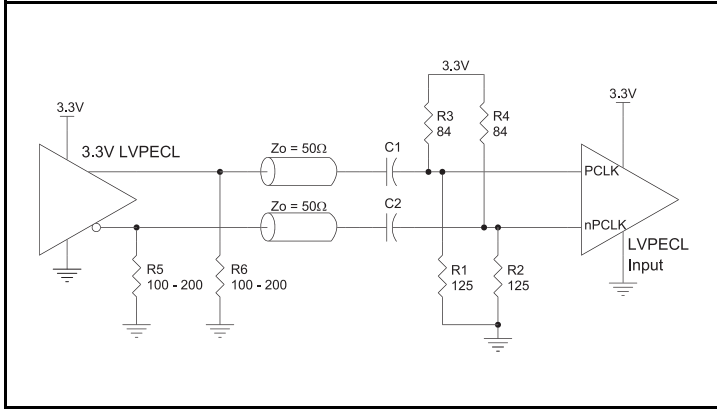


Figure 2A. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

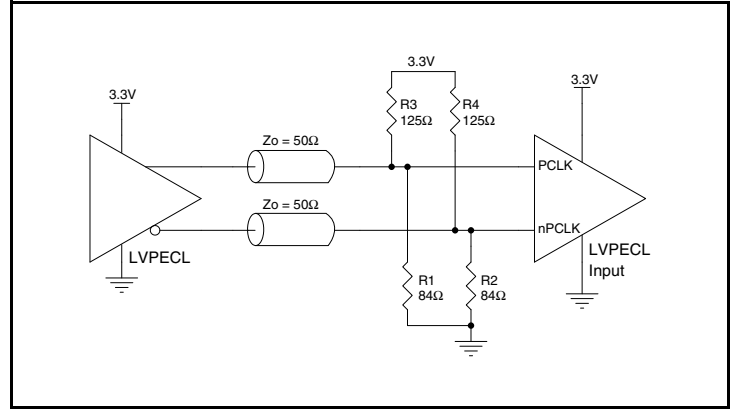


Figure 2B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

2.5V LVPECL Clock Input Interface

The PCLK/nPCLK accepts LVPECL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3B show interface examples for the PCLK/nPCLK input driven by the most common driver types. The

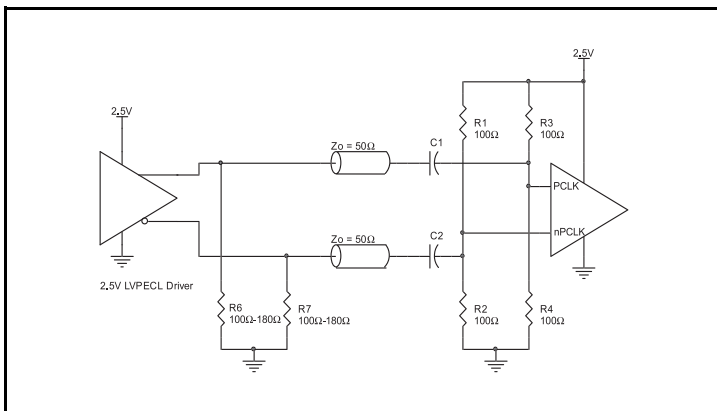


Figure 3A. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

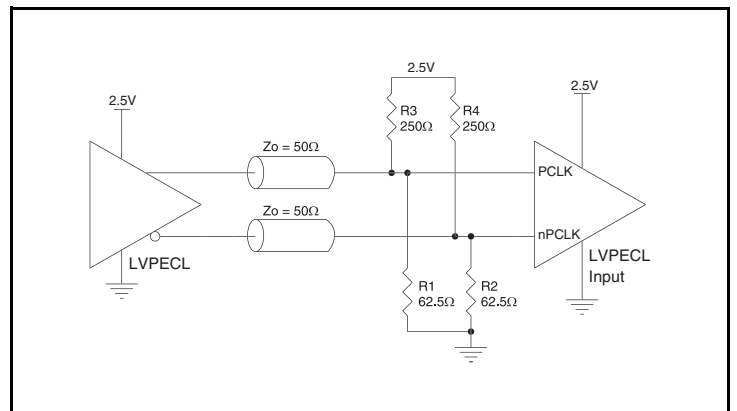


Figure 3B. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

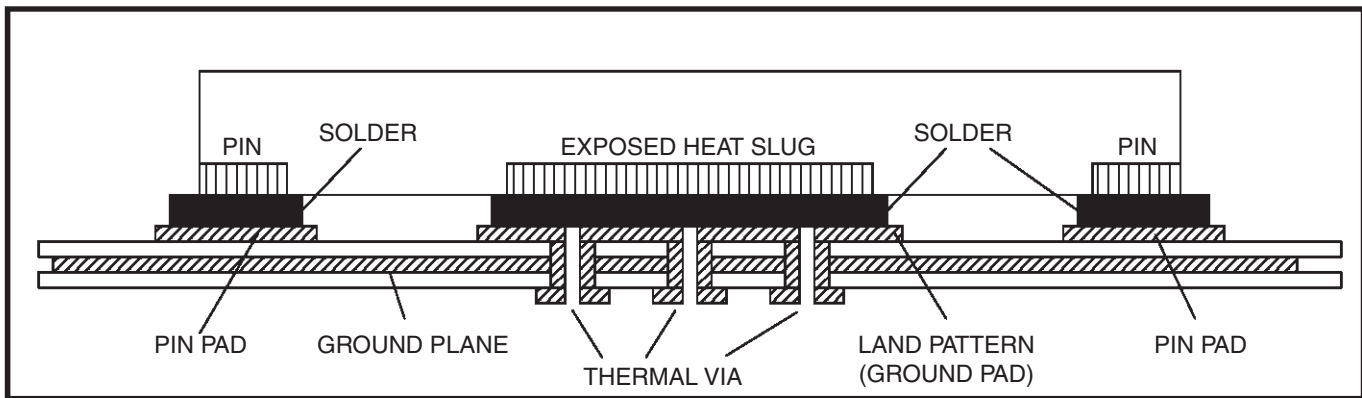


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Layout

Figure 5 shows an example 840NT4 application schematic. This schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

In this schematic, the device is operated at $V_{DD} = V_{DDA} = 2.5V$ and V_{DDO_A} , V_{DDO_B} , V_{DDO_C} and $V_{DDO_REFx} = 1.8V$.

A 12pF parallel resonant 25MHz crystal is used with the recommended load capacitors $C1 = C2 = 3.3pF$ for frequency accuracy. Depending on the parasitic capacity on the crystal terminals of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting $C1$ and $C2$. For this device, the crystal load capacitors are required for proper operation.

Crystal layout is very important to minimize capacitive coupling between the crystal pads and leads and other metal in the circuit board. Capacitive coupling to other conductors has two adverse effects; it reduces the oscillator frequency leaving less tuning margin and noise coupling from power planes and logic transitions on signal traces can pull the phase of the crystal resonance, inducing jitter. Routing I²C under the crystal is a very common layout error, based on the assumption that it is a low frequency signal and will not affect the crystal oscillation. In fact, I²C transition times are short enough to capacitively couple into the crystal if they are routed close enough to the crystal traces.

In layout, all capacitive coupling to the crystal from any signal trace is to be minimized, that is to the XTAL_IN and XTAL_OUT pins, traces to the crystal pads, the crystal pads and the tuning capacitors. Using a crystal on the top layer as an example, void all signal and power layers under the crystal connections between the top layer and the ground plane used by the 840NT4. Then calculate the parasitic capacity to the ground and determine if it is large enough to preclude tuning the oscillator. If the coupling is excessive, particularly if the first

layer under the crystal is a ground plane, a layout option is to void the ground plane and all deeper layers until the next ground plane is reached. The ground connection of the tuning capacitors should first be made between the capacitors on the top layer, then a single ground via is dropped to connect the tuning cap ground to the ground plane as close to the 840NT4 as possible as shown in the schematic.

This device package has an ePAD that is connected to ground internally. The ePAD is to be connected to V_{EE}/GND through vias in order to improve heat dissipation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 840NT4 provides separate power supply pins to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

For additional layout recommendations and guidelines, contact clocks@idt.com.

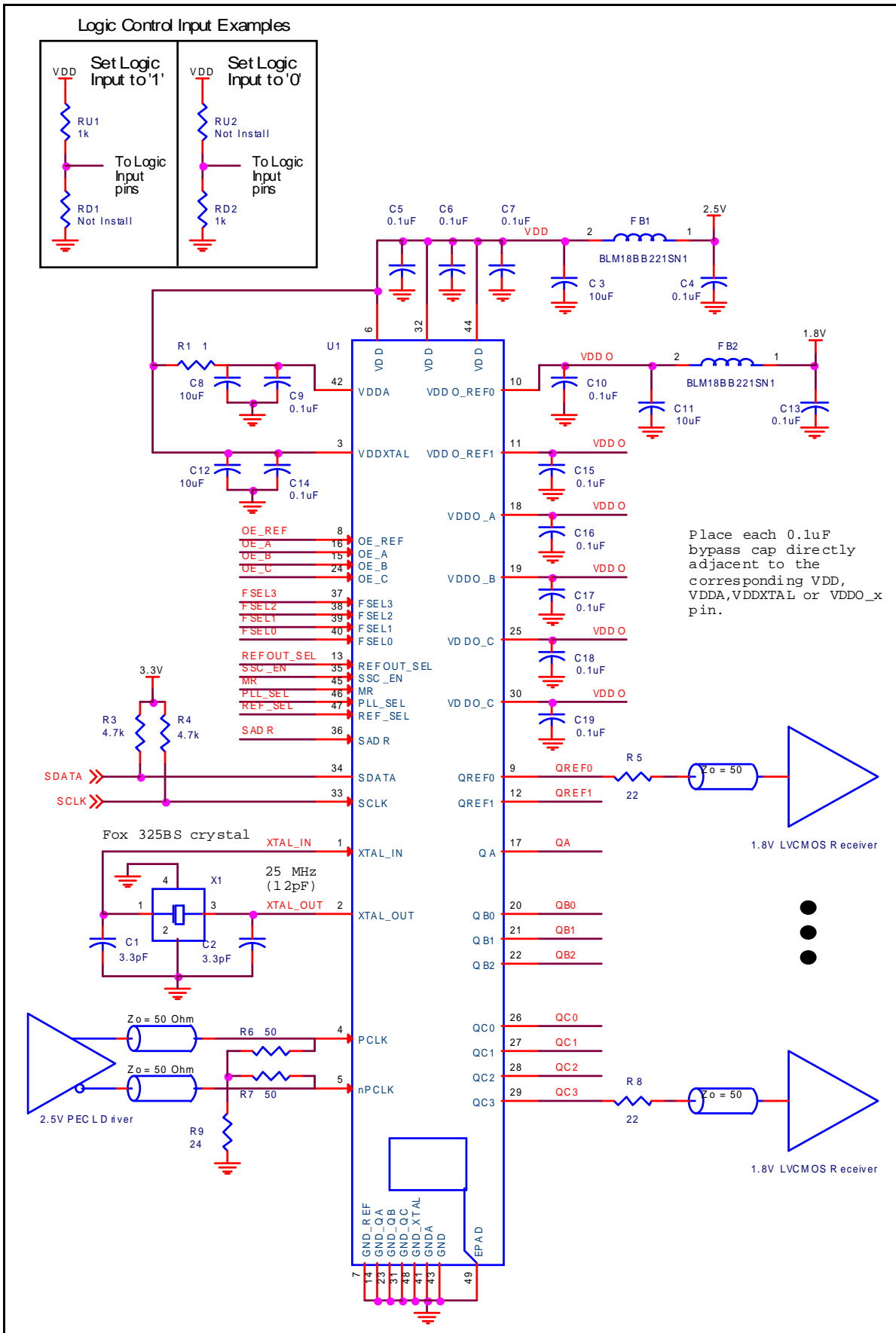


Figure 5. 840NT4 Schematic Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the 840NT4. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 840NT4 is the sum of the core power plus the analog power plus the power dissipation due to loading. The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

- $$\begin{aligned} \text{Power (Static)}_{MAX} &= [V_{DD_MAX} * (I_{DD_MAX} + I_{DD_XTAL} + I_{DDA} + I_{DDO_X})] \\ &= [3.465V * (149mA + 44mA + 32mA + 3mA)] \\ &= \mathbf{790.02mW} \end{aligned}$$

Dynamic Power Dissipation (max)

- $$\begin{aligned} \text{Power (F}_{OUT_MAX}) &= [C_{PD} * (8 * F_{MAX_Qa,b,c} + F_{MAX_QREF1} + F_{MAX_QREF0}) * (V_{DDO})^2] \\ &= [15pF * (8 * 200MHz + 25MHz + 3.125MHz) * (3.465V)^2] \\ &= \mathbf{293.2mW} \end{aligned}$$

Total Power

$$\begin{aligned} &= (\text{Static Power} + \text{Dynamic Power Dissipation}) \\ &= (790.02mW + 293.2mW) \\ &= \mathbf{1083.22mW} \end{aligned}$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 29°C/W per Table 9 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 1.083W * 29^\circ\text{C/W} = 116.4^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 9. Thermal Resistance θ_{JA} for a 48 Lead VFQFN Package, Forced Convection

| θ_{JA} by Velocity | | | |
|---|----------|-----------|-----------|
| Meters per Second | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 29.0°C/W | 22.88°C/W | 20.62°C/W |

Reliability Information

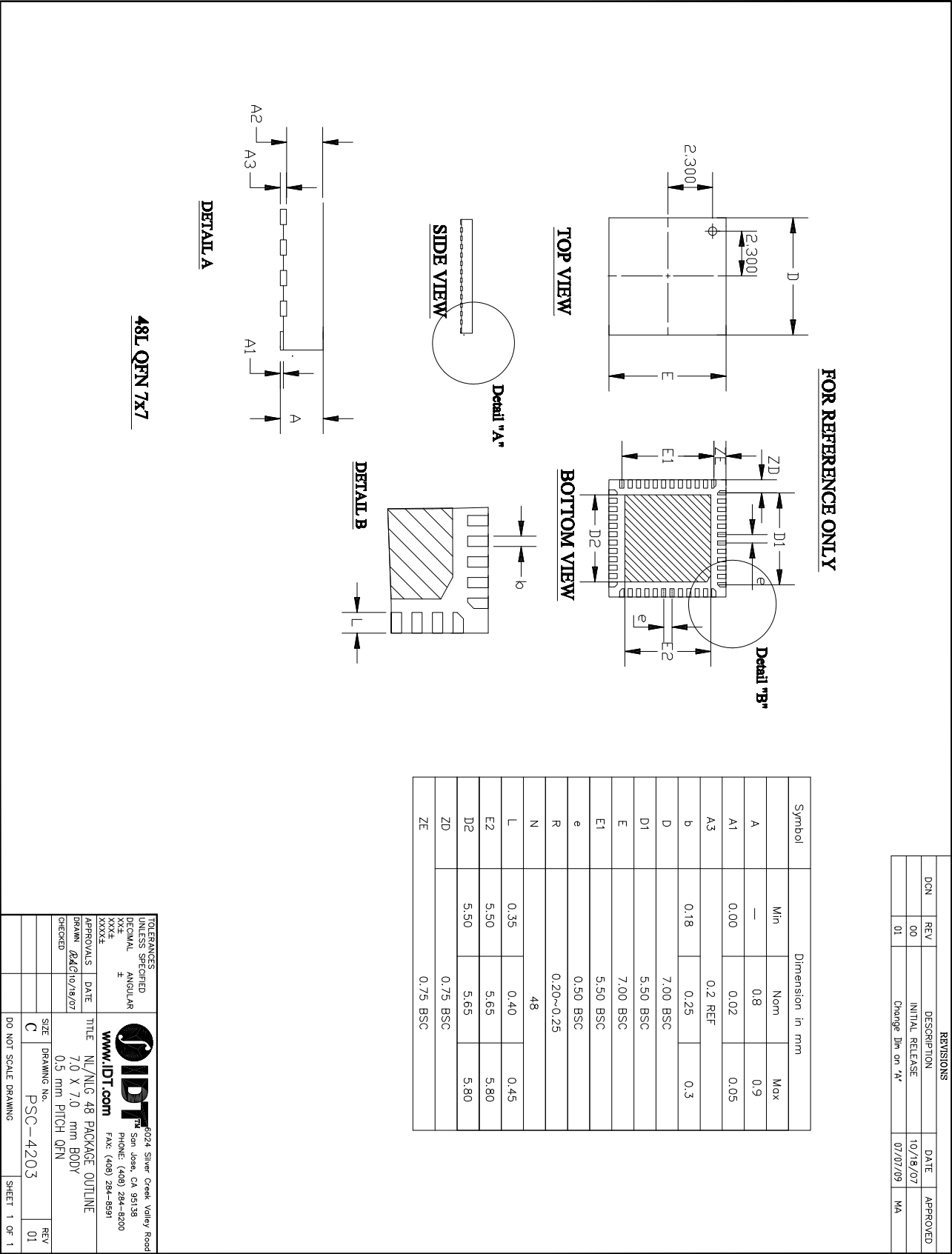
Table 10. θ_{JA} vs. Air Flow Table for a 48 Lead VFQFN

| θ_{JA} vs. Air Flow | | | |
|---|----------|-----------|-----------|
| Meters per Second | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 29.0°C/W | 22.88°C/W | 20.62°C/W |

Transistor Count

840NT4 transistor count 27,463

48 Lead VFQFN Package Outline and Package Dimensions



Ordering Information

Table 11. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|---------------|--------------------------|--------------------|---------------|
| 840NT4NLGI | IDT840NT4NLGI | 48 Lead VFQFN, Lead-Free | Tray | -40°C to 85°C |
| 840NT4NLGI8 | IDT840NT4NLGI | 48 Lead VFQFN, Lead-Free | Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "G" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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