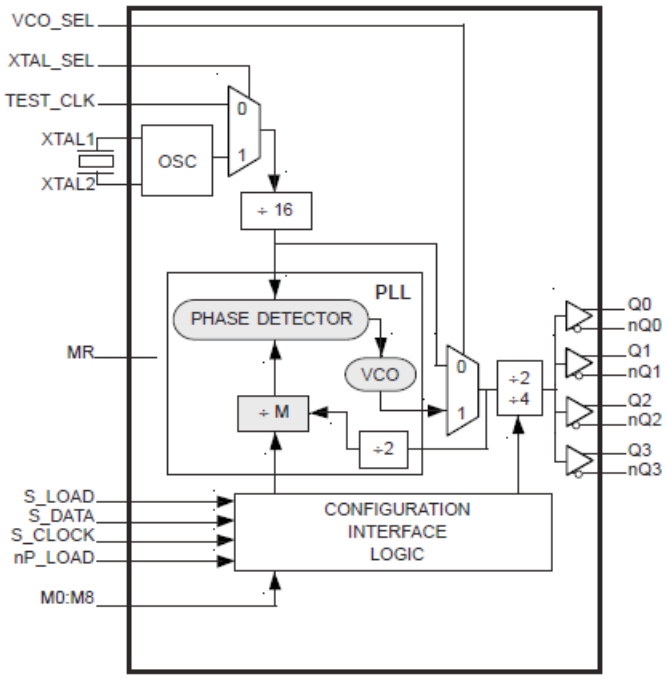
General Description

The 84314 is a general purpose quad output frequency synthesizer and a member of the family of High Performance Clock Solutions from IDT. When the device uses parallel loading, the M bits are programmable and the output divider is hard-wired for divide by 2 thus providing a frequency range of 125MHz to 350MHz. In serial programming mode, the M bits are programmable and the output divider can be set for either divide by 2 or divide by 4, providing a frequency range of 62.5MHz to 350MHz. The low cycle-cycle jitter and broad frequency range of the 84314 make it an ideal clock generator for a variety of demanding applications which require high performance.

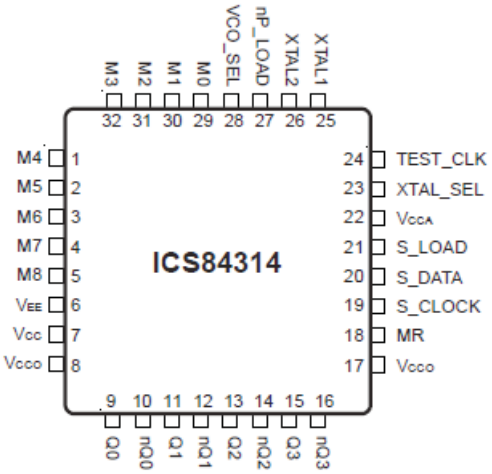
Features

- Fully integrated PLL
- 4 differential 3.3V or 2.5V LVPECL outputs
- Selectable crystal oscillator interface or LVCMOS TEST_CLK input
- Output frequency range: 62.5MHz to 350MHz
- VCO range: 250MHz to 700MHz
- Parallel interface for programming counter and output dividers during power-up
- Serial 3 wire interface
- Cycle-to-cycle jitter: 23ps (typical)
- Output skew: 16ps (typical)
- Output duty cycle: 49% < odc < 51%, fout ≤ 125MHz
- Full 3.3V or mixed 3.3V core, 2.5V operating supply
- 0°C to 85°C ambient operating temperature
- Lead-Free package available

Block Diagram



Pin Assignment



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Functional Description

NOTE: The functional description that follows describes operation using a 16MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.

The 84314 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A parallel-resonant, fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is divided by 16 prior to the phase detector. With a 16MHz crystal, this provides a 1MHz reference frequency. The VCO of the PLL operates over a range of 250MHz to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be 2M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the 84314 support two input modes to program the M divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode, the nP_LOAD input is initially LOW. The data on inputs M0 through M8 is passed directly to the M divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result, the M bits can be hardwired to set the M divider to a specific default state that will automatically occur during power-up. In parallel mode, the N output divider is set to 2. In serial mode, the N output divider can be set for either ÷2 or ÷4. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:

$$fVCO = \frac{fxtal}{16} \times 2M$$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 16MHz reference are defined as $125 \leq M \leq 350$. The frequency out is defined as follows: $fout = fVCO \times \frac{1}{N} = \frac{fxtal}{16} \times 2M \times \frac{1}{N}$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and N output divider on each rising edge of S_CLOCK.

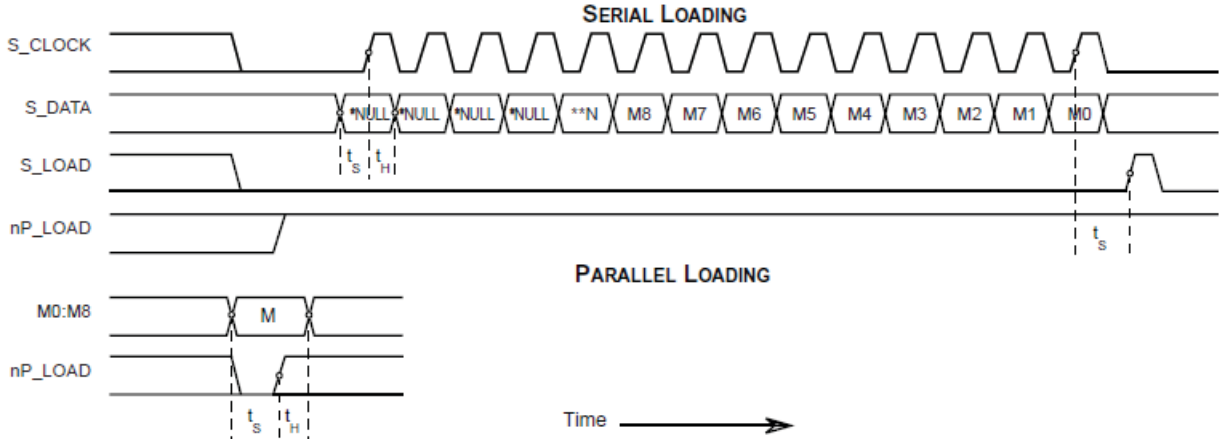


Figure 1. Parallel & Serial Load Operations

Table 1. N Output Divider Function Table (Serial Load)

N Logic Value	Output Divide
0	÷2
1	÷4

***NOTE:** The NULL timing slot must be observed.
****NOTE:** "N" can only be controlled through serial loading.

Table 2. Pin Descriptions

Number	Name	Type		Description
1, 2, 3, 4, 29, 30, 31, 32	M4, M5, M6, M7, M0, M1, M2, M3	Input	Pulldown	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS / LVTTL interface levels.
5	M8	Input	Pullup	
6	V_{EE}	Power		Negative supply pin.
7	V_{CC}	Power		Core power supply pin.
8, 17	V_{CCO}	Power		Output supply pins.
9, 10	Q0, nQ0	Output		Differential output for the synthesizer. LVPECL interface levels.
11, 12	Q1, nQ1	Output		Differential output for the synthesizer. LVPECL interface levels.
13, 14	Q2, nQ2	Output		Differential output for the synthesizer. LVPECL interface levels.
15, 16	Q3, nQ3	Output		Differential output for the synthesizer. LVPECL interface levels.
18	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not affect loaded M values. LVCMOS / LVTTL interface levels.
19	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
20	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
21	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS / LVTTL interface levels.
22	V_{CCA}	Power		Analog supply pin.
23	XTAL_SEL	Input	Pullup	Selects between the crystal oscillator or test clock as the PLL reference source. Selects XTAL inputs when HIGH. Selects TEST_CLK when LOW. LVCMOS / LVTTL interface levels.
24	TEST_CLK	Input	Pulldown	Test clock input. LVCMOS interface levels.
25, 26	XTAL1, XTAL2	Input		Crystal oscillator interface. XTAL1 is the input. XTAL2 is the output.
27	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into the M divider. LVCMOS / LVTTL interface levels.
28	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 3. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 4A. PARALLEL AND SERIAL MODE FUNCTION TABLE

Inputs						Conditions
MR	nP_LOAD	M	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	Reset. Forces outputs LOW.
L	L	Data	X	X	X	Data on M inputs passed directly to the M divider.
L	↑	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	L	X	X	Parallel or serial input do not affect shift registers.
L	H	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

TABLE 4B. PROGRAMMABLE VCO FREQUENCY FUNCTION TABLE (NOTE 1)

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	125	0	0	1	1	1	1	1	0	1
252	126	0	0	1	1	1	1	1	1	0
254	127	0	0	1	1	1	1	1	1	1
256	128	0	1	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
696	348	1	0	1	0	1	1	1	0	0
698	349	1	0	1	0	1	1	1	0	1
700	350	1	0	1	0	1	1	1	1	0

NOTE 1: These M divide values and the resulting frequencies correspond to crystal or TEST_CLK input frequency of 16MHz.

TABLE 4C. PROGRAMMABLE OUTPUT DIVIDER FUNCTION TABLE (SERIAL PROGRAMMING MODE ONLY)

Input		Output Frequency (MHz)	
N Logic	N Divide	Qx, nQx	
		Minimum	Maximum
0	2	125	350
1	4	62.5	175

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 5A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO} = 3.3V±5\%$ or $2.5V±5\%$, $T_A = 0°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{EE}	Power Supply Current				150	mA
I_{CCA}	Analog Supply Current				17	mA

Table 5B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO} = 3.3V±5\%$ or $2.5V±5\%$, $T_A = 0°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	TEST_CLK; NOTE 1		2.35		V_{CC} + 0.3	V
		VCO_SEL, XTAL_SEL, nP_LOAD, MR, M0:M8, S_LOAD, S_DATA, S_CLOCK		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	TEST_CLK; NOTE 1		-0.3		0.95	V
		VCO_SEL, XTAL_SEL, nP_LOAD, MR, M0:M8, S_LOAD, S_DATA, S_CLOCK		-0.3		0.8	V
I_{IH}	Input High Current	M0:M7, MR, nP_LOAD, S_CLOCK, S_DATA, S_LOAD	$V_{CC} = V_{IN} = 3.465V$			150	µA
		M8, XTAL_SEL, VCO_SEL	$V_{CC} = V_{IN} = 3.465V$			5	µA
		TEST_CLK	$V_{CC} = V_{IN} = 3.465V$			200	µA
I_{IL}	Input Low Current	M0:M7, MR, nP_LOAD, S_CLOCK, S_DATA, S_LOAD	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		M8, XTAL_SEL, VCO_SEL	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA

NOTE:1 Characterized with 1ns input edge rate.

Table 5C. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO} = 3.3V±5\%$ or $2.5V±5\%$, $T_A = 0°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V. See “Parameter Measurement Information” section, “3.3V Output Load Test Circuit”.

Table 6. Input Frequency Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $T_A = 0°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	TEST_CLK; NOTE 1		10		40	MHz
		XTAL1, XTAL2; NOTE 1		12		40	MHz
		S_CLOCK				50	MHz

NOTE 1: For the input crystal and reference frequency range, the M value must be set for the VCO to operate within the 250MHz to 700MHz range. Using the minimum input frequency of 12MHz, valid values of M are $167 \le M \le 466$. Using the maximum frequency of 40MHz, valid values of M are $50 \le M \le 140$.

Table 7. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

TABLE 8A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{MAX}	Output Frequency					350	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 3				23	35	ps
*t*jit(per)	Period Jitter, RMS; NOTE 1					8	ps
*t*sk(o)	Output Skew; NOTE 2, 3				16	30	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		700	ps
t_S	Setup Time	M to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
t_H	Hold Time	M to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
odc	Output Duty Cycle		f_{OUT} > 125MHz	48	50	52	%
			$f_{OUT} \leq$ 125MHz	49	50	51	%
t_{LOCK}	PLL Lock Time					1	ms

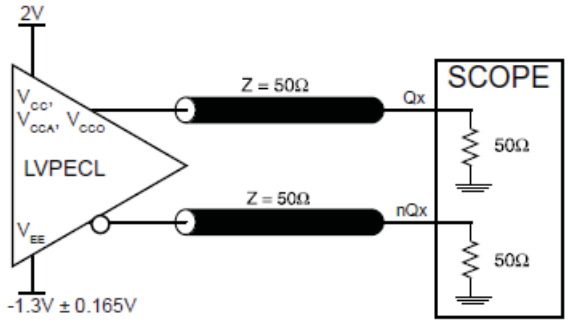
See Parameter Measurement Information section.
NOTE 1: Jitter performance using XTAL inputs.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 8B. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $V_{CCO} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $85°C$

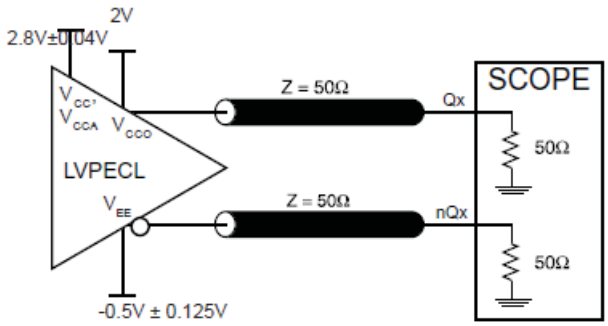
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{MAX}	Output Frequency					350	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 3				23	35	ps
*t*jit(per)	Period Jitter, RMS; NOTE 1					7	ps
*t*sk(o)	Output Skew; NOTE 2, 3				16	35	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		700	ps
t_S	Setup Time	M to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
t_H	Hold Time	M to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
odc	Output Duty Cycle		f_{OUT} > 125MHz	48	50	52	%
			$f_{OUT} \leq$ 125MHz	49	50	51	%
t_{LOCK}	PLL Lock Time					1	ms

See Parameter Measurement Information section.
NOTE 1: Jitter performance using XTAL inputs.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

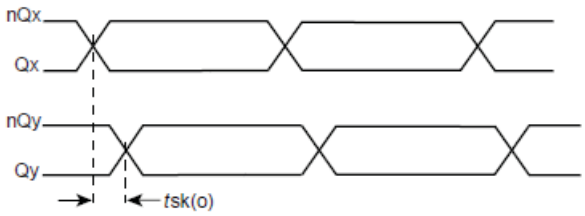
PARAMETER MEASUREMENT INFORMATION



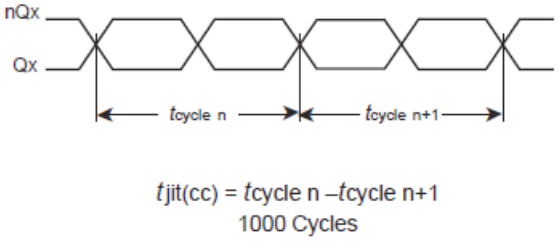
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT

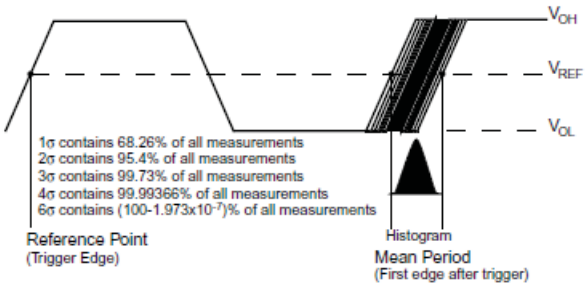


OUTPUT SKEW

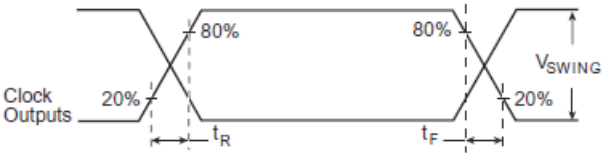


$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$
1000 Cycles

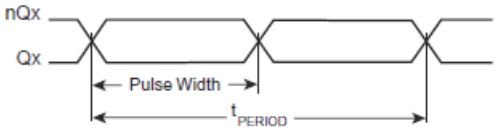
CYCLE-TO-CYCLE JITTER



PERIOD JITTER



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 84314 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

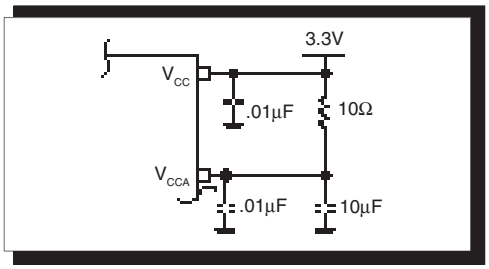


FIGURE 2. POWER SUPPLY FILTERING

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

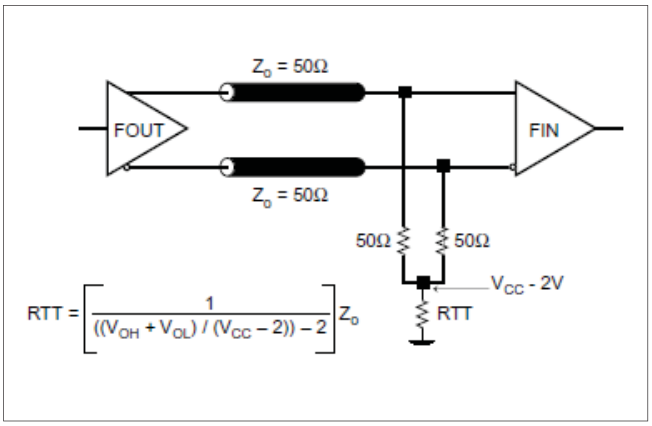


FIGURE 3A. LVPECL OUTPUT TERMINATION

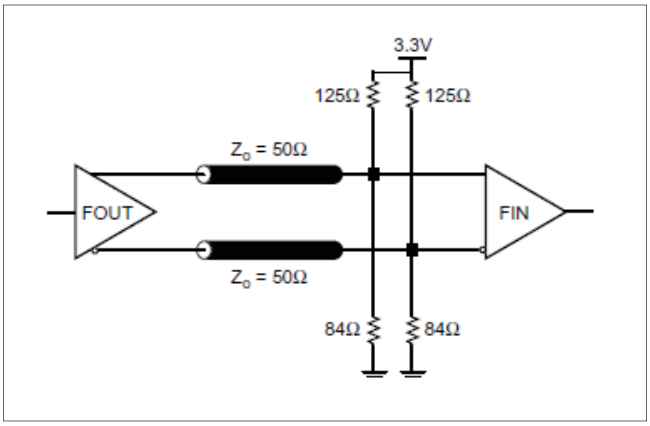


FIGURE 3B. LVPECL OUTPUT TERMINATION

Termination for 2.5V LVPECL Output

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 4A can be eliminated and the termination is shown in *Figure 4C.*

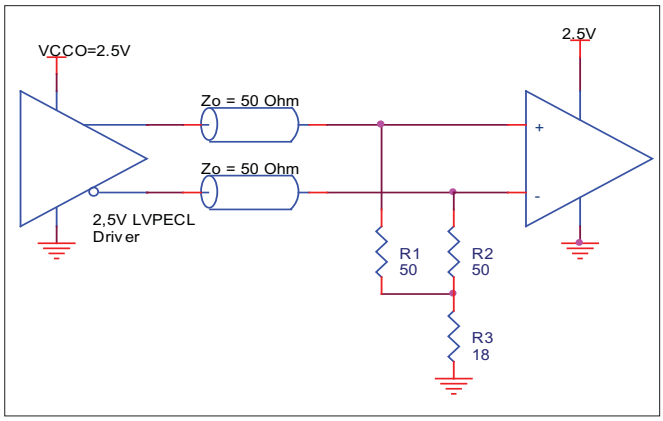


Figure 4A. 2.5V LVPECL Driver Termination Example

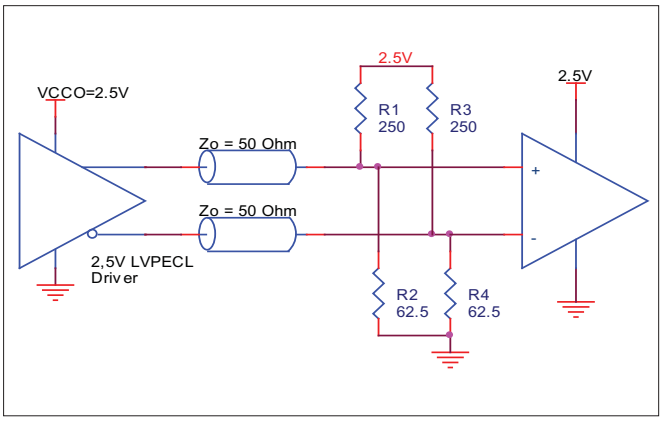


Figure 4B. 2.5V LVPECL Driver Termination Example

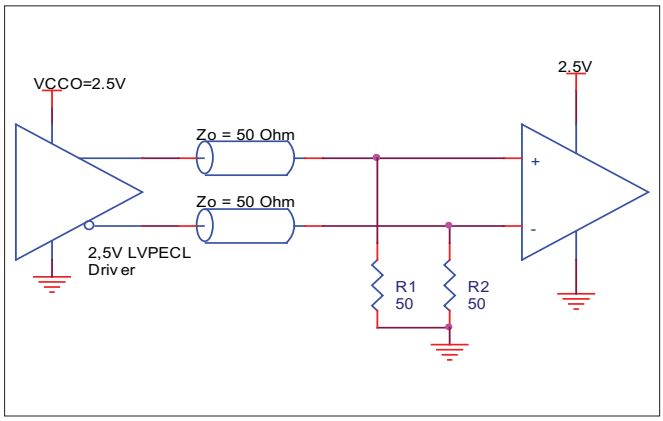


Figure 4C. 2.5V LVPECL Termination Example

Crystal Input Interface

The 84314 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 5* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

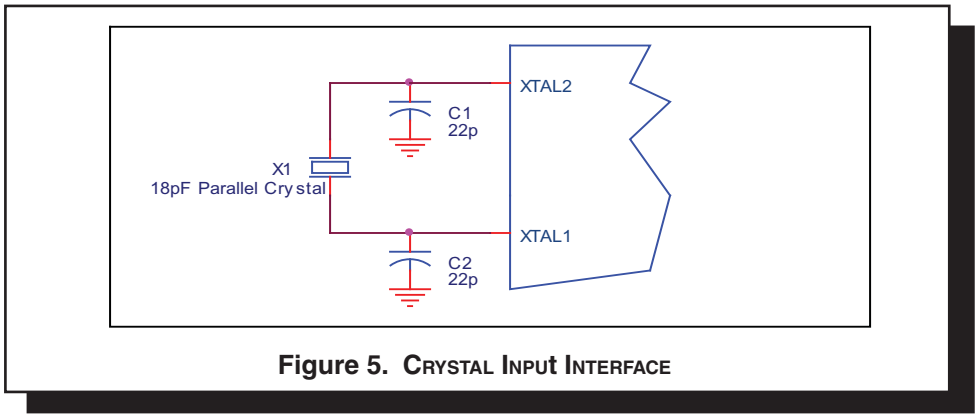


Figure 5. Crystal Input Interface

Layout Guideline

The schematic of the 84314 layout example used in this layout guideline is shown in *Figure 6A.* The 84314 recommended PCB board layout for this example is shown in *Figure 6B.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

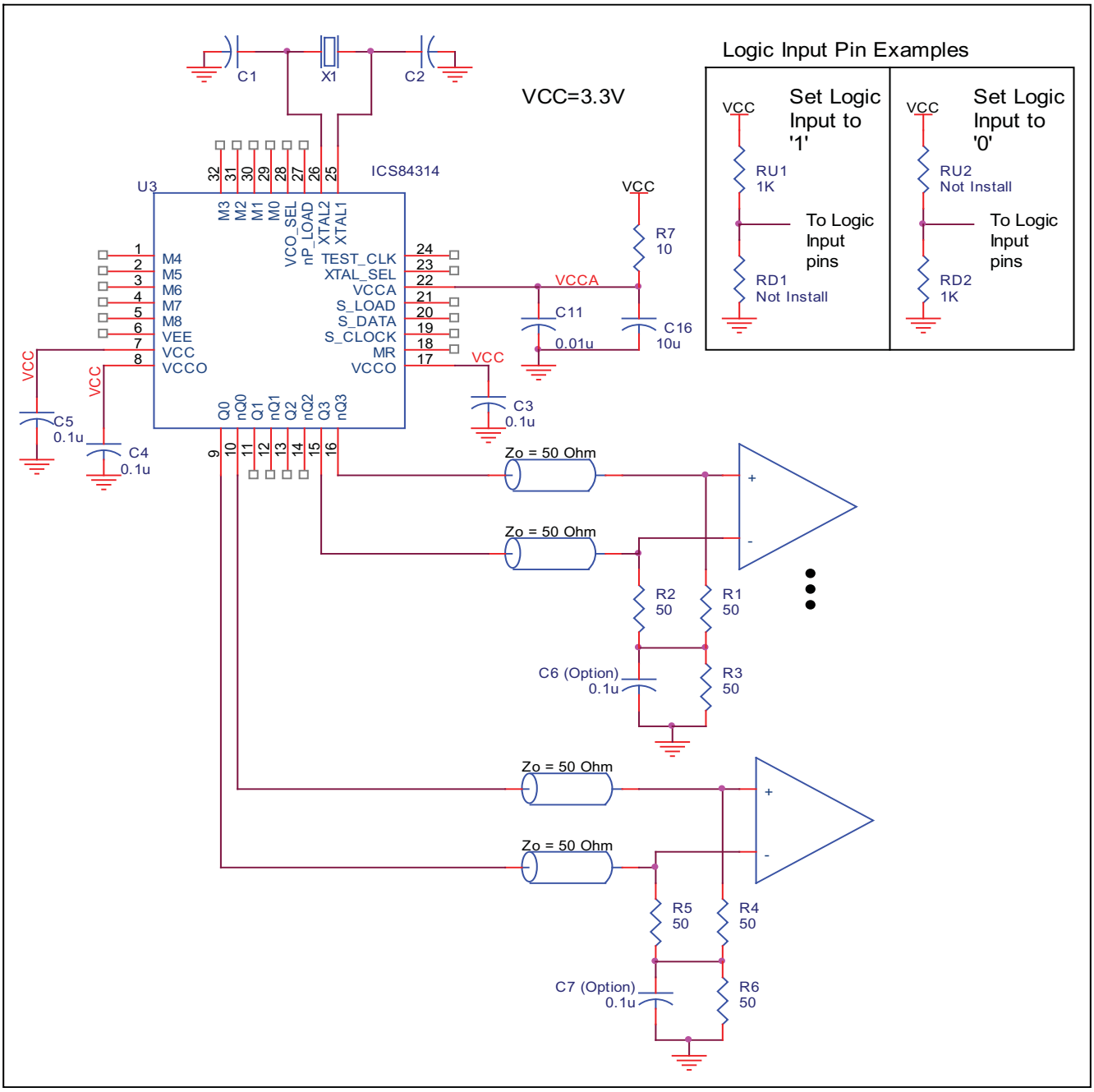


Figure 6A. Schematic of 3.3V/3.3V Recommended Layout

The following component footprints are used in this layout example: All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors C14 and C15 as close as possible to the power pins. If space allows, placing the decoupling capacitor at the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin generated by the via.

Maximize the pad size of the power (ground) at the decoupling capacitor. Maximize the number of vias between power (ground) and the pads. This can reduce the inductance between the power (ground) plane and the component power (ground) pins.

If V_{CCA} shares the same power supply with V_{CC}, insert the RC filter R7, C11, and C16 in between. Place this RC filter as close to the V_{CCA} as possible.

Clock Traces and Termination

The component placements, locations and orientations should be arranged to achieve the best clock signal quality. Poor clock signal quality can degrade the system performance or cause system failure. In the synchronous high-speed digital system, the clock signal is less tolerable to poor signal quality than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The trace shape and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The traces with 50Ω transmission lines TL1 and TL2 at FOUT and nFOUT should have equal delay and run adjacent to each other. Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock trace on the same layer. Whenever possible, avoid any vias on the clock traces. Any via on the trace can affect the trace characteristic impedance and hence degrade signal quality.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow more space between the clock trace and the other signal trace.
- Make sure no other signal trace is routed between th clock trace pair.

The matching termination resistors R1, R2, R3 and R4 should be located as close to the receiver input pins as possible. Other termination schemes can also be used but are not shown in this example.

Crystal

The crystal X1 should be located as close as possible to the pins 25 (XTAL1) and 26 (XTAL2). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

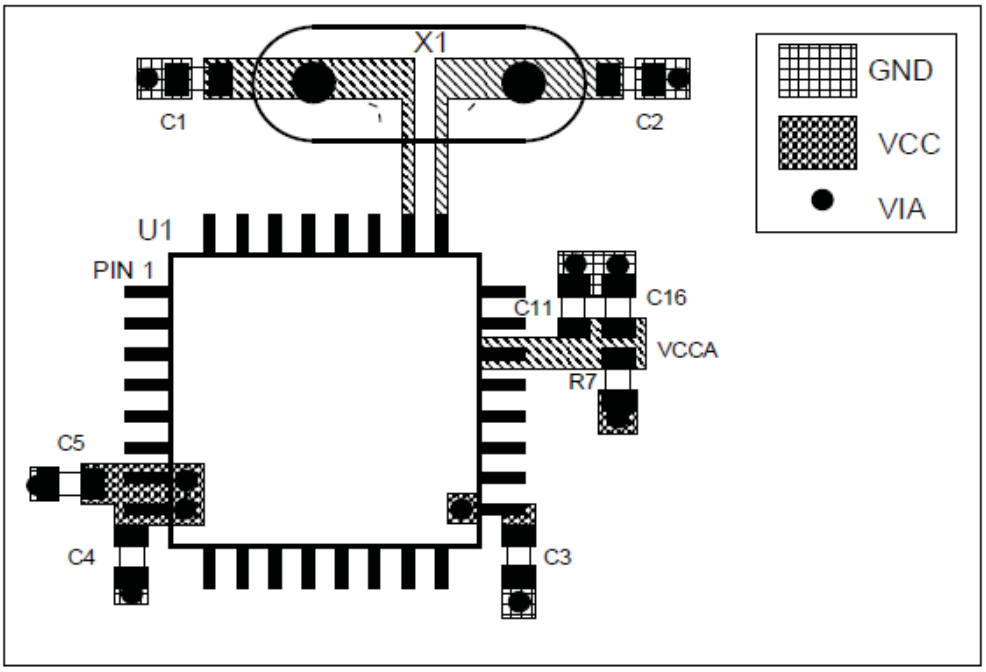


Figure 6B. PCB Board Layout for 84314

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 84314.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 84314 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 150mA = **519.7mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30mW = **120mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 519.7mW + 120mW = **639.7mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 9 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.640W * 42.1°C/W = 111.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 9. THERMAL RESISTANCE θ_{JA} FOR 32-PIN LQFP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

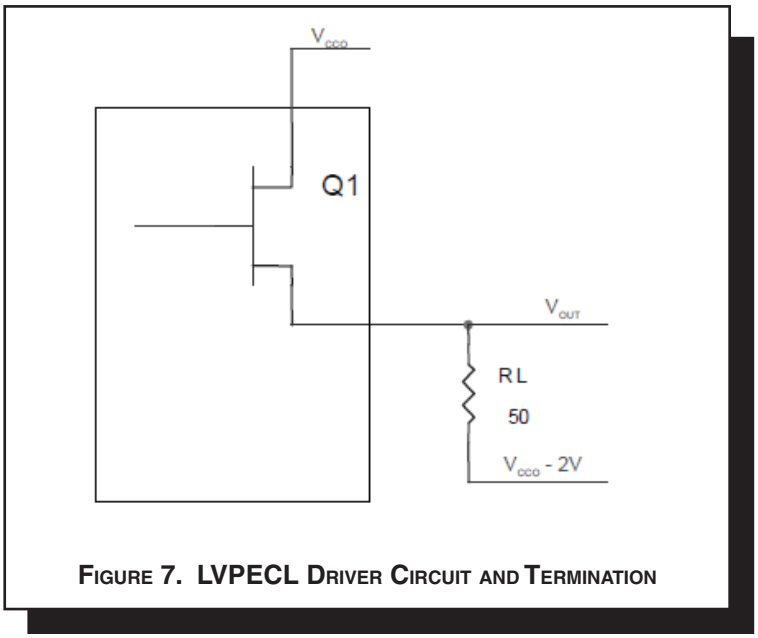


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination
voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} – 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 10. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 84314 is: 3509

Package Outline - Y Suffix for 32 Lead LQFP

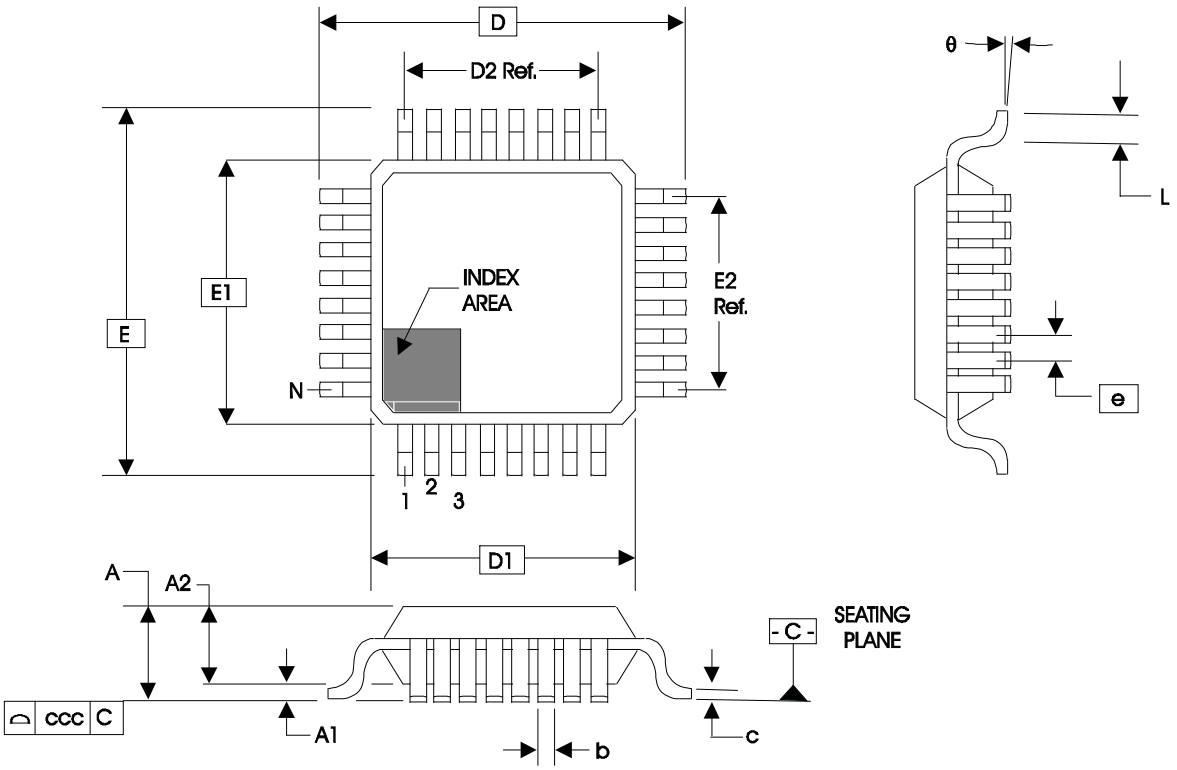


Table 11. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 12. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
84314AYLF	ICS84314AYLF	32 lead “Lead Free” LQFP	Tray	0°C to +85°C
84314AYLF	ICS84314AYLF	32 lead “Lead Free” LQFP	Tape and Reel	0°C to +85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T5C	6 13 - 14	LVPECL table - changed V_{OH} max. from V_{CC} - 1.0V to V_{CC} - 0.9V. Changed equations in Power Considerations to correlate with Table 5C.	2/4/04
C	T1 T5B T12	1 3 5 17	LVCMOS/LVTTL TEST_CLK changed to LVCMOS TEST_CLK. Added Lead-Free bullet . Pin Descriptions Table - Pin 24, TEST_CLK, description changed from LVCMOS/LVTTL interface levels to LVCMOS interface levels. LVCMOS DC Characteristics - TEST_CLK V_{IH} (min.) changed from 2V to 2.35V; V_{IL} (max.) changed from 1.3V to 0.95V. Added Lead-Free part number to Ordering Information Table.	11/5/04
C	T5B	5	LVCMOS DC Characteristics Table - added V_{IH}/V_{IL} NOTE 1.	1/27/05
C	T12	1 17	General Description - Removed ICS Chip and Hiperclocks. Ordering Information - Removed leaded parts, removed 1000 from tape and reel, and removed the LF note below the table. Added contacts page. Updated data sheet header and footer.	1/8/16

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