General Description

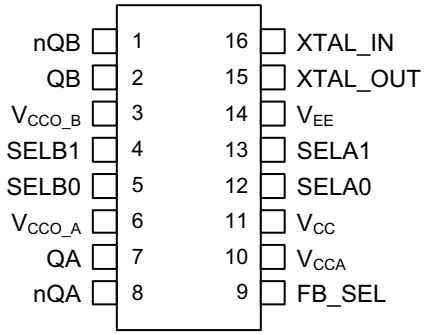
The 843242 is a two differential output LVPECL Synthesizer designed to generate Ethernet reference clock frequencies. Using a 31.25MHz or 26.041666MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the settings of 4 frequency select pins (SELA[1:0], SELB[1:0]): 625MHz, 312.5MHz, 156.25MHz, and 125MHz.

The two banks have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The 843242 IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The 843242 is packaged in a small 16-pin TSSOP package.

Features

- Two differential LVPECL output pairs
- Using a 31.25MHz or 26.041666MHz crystal, the two output banks can be independently set for 625MHz, 312.5MHz, 156.25MHz or 125MHz
- Crystal oscillator interface
- RMS Phase Jitter @ 625MHz, (1.875MHz – 20MHz) using a 25MHz crystal: 0.4ps (typical)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Lead-free (RoHS 6) packaging

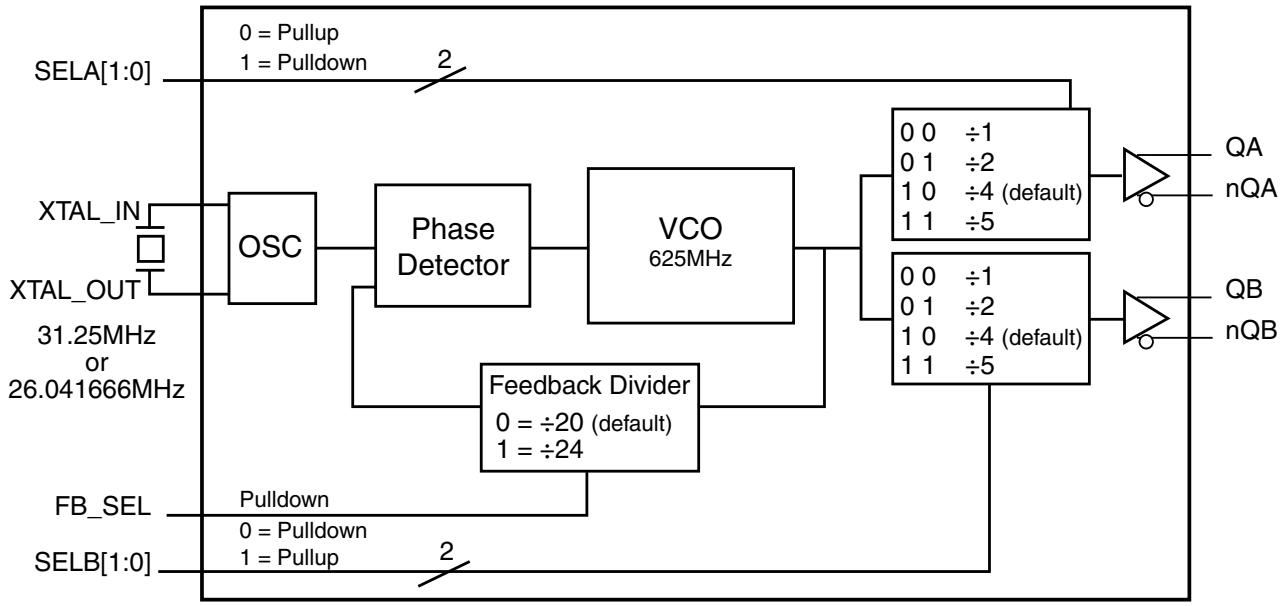
Pin Assignment



843242

16-pin, 4.4mm x 5.0mm TSSOP Package (173 mil)

Block Diagram



Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	nQB	Output		Differential clock outputs. LVPECL interface levels.
2	QB	Output		Differential clock outputs. LVPECL interface levels.
3	V_{CCO_B}	Power		Output supply pin for QB, nQB outputs.
4	SELB1	Input	Pullup	Division select pin for Bank B. Default = High. LVCMOS/LVTTL interface levels.
5	SELB0	Input	Pulldown	Division select pins for Bank B. Default = Low. LVCMOS/LVTTL interface levels.
6	V_{CCO_A}	Power		Output supply pin for QA, nQA outputs.
7	QA	Output		Differential clock outputs. LVPECL interface levels.
8	nQA	Output		Differential clock outputs. LVPECL interface levels.
9	FB_SEL	Input	Pulldown	Feedback divide select. When LOW (default), the feedback divider is set for ÷20. When HIGH, the feedback divider is set for ÷24. LVCMOS/LVTTL interface levels.
10	V_{CCA}	Power		Analog supply pin.
11	V_{CC}	Power		Core supply pin.
12	SELA0	Input	Pullup	Division select pin for Bank A. Default = High. LVCMOS/LVTTL interface levels.
13	SELA1	Input	Pulldown	Division select pin for Bank A. Default = Low. LVCMOS/LVTTL interface levels.
14	V_{EE}	Power		Negative supply pin.
15	XTAL_OUT	Input		Crystal oscillator interface XTAL_IN is the input, XTAL_OUT is the output.
16	XTAL_IN	Input		Crystal oscillator interface XTAL_IN is the input, XTAL_OUT is the output.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	SELA[1:0], SELB[1:0], FB_SEL		4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Bank A Frequency Table

Inputs				Feedback Divider	Bank A Output Divider	M/N Multiplication Factor	QA, nQA Output Frequency (MHz)
Crystal Frequency (MHz)	SELA1	SELA0	FB_SEL				
31.25	0	0	0	20	1	20	625
31.25	0	1	0	20	2	10	312.5
31.25	1	0	0	20	4	5	156.25
31.25	1	1	0	20	5	4	125
26.041666	0	0	1	24	1	24	625
26.041666	0	1	1	24	2	12	312.5
26.041666	1	0	1	24	4	6	156.25
26.041666	1	1	1	24	5	4.8	125

Table 3B. Bank B Frequency Table

Inputs				Feedback Divider	Bank B Output Divider	M/N Multiplication Factor	QB, nQB Output Frequency (MHz)
Crystal Frequency (MHz)	SELB1	SELB0	FB_SEL				
31.25	0	0	0	20	1	20	625
31.25	0	1	0	20	2	10	312.5
31.25	1	0	0	20	4	5	156.25
31.25	1	1	0	20	5	4	125
26.041666	0	0	1	24	1	24	625
26.041666	0	1	1	24	2	12	312.5
26.041666	1	0	1	24	4	6	156.25
26.041666	1	1	1	24	5	4.8	125

Table 3C. Output Bank Configuration Select Function Table

Inputs		Outputs
SELA1	SELA0	QA
0	0	÷1
0	1	÷2 (default)
1	0	÷4
1	1	÷5

Inputs		Outputs
SELB1	SELB0	QB
0	0	÷1
0	1	÷2
1	0	÷4 (default)
1	1	÷5

Table 3D. Feedback Divider Configuration Select Function Table

Inputs	
FB_DIV	Feedback Divide
0	÷20 (default)
1	÷24

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V ±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.15	3.3	V_{CC}	V
V_{CCO_A}, V_{CCO_B}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				158	mA
I_{CCA}	Analog Supply Current				15	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V ±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	FB_SEL, SELA1, SELB0	$V_{CC} = V_{IN}$ = 3.465V			150	µA
		SELA0, SELB1	$V_{CC} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	FB_SEL, SELA1, SELB0	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		SELA0, SELB1	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO\_X} - 1.4$		$V_{CCO\_X} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO\_X} - 2.0$		$V_{CCO\_X} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Output termination with 50Ω to $V_{CCO\_A, \_B} - 2V$.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		26.04166		31.25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Load Capacitance			12	18	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

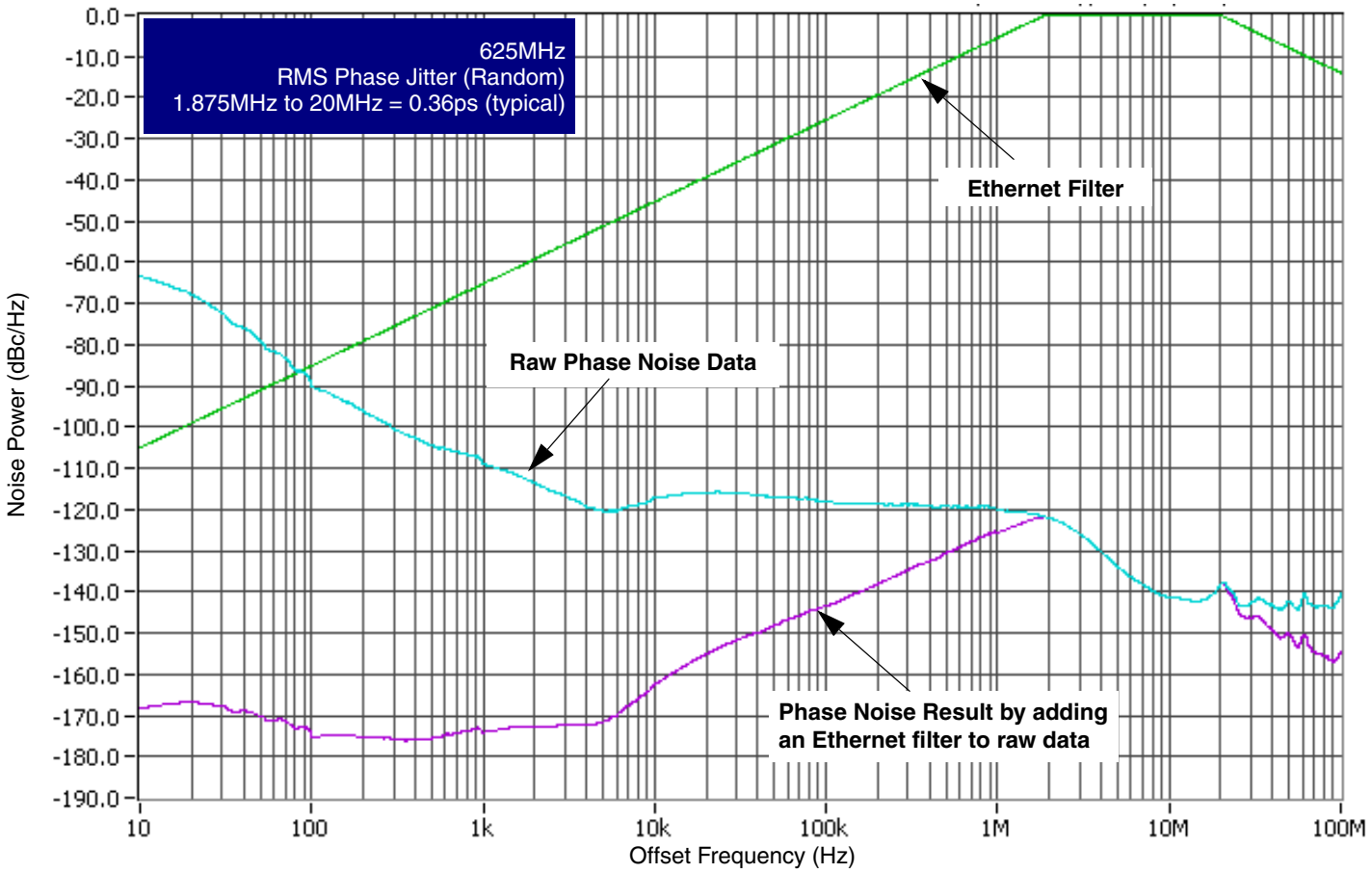
AC Electrical Characteristics

Table 6. AC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

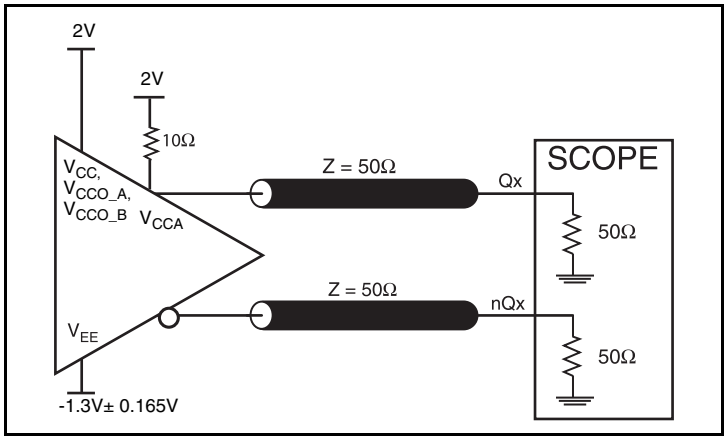
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	VCO = 625MHz	Output Divider = ÷ 1		625		MHz
			Output Divider = ÷ 2		312.5		MHz
			Output Divider = ÷ 4		156.25		MHz
			Output Divider = ÷ 5		125		MHz
*t*sk(o)	Output Skew; NOTE 1, 2		Outputs @ Same Frequency			45	ps
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 3		625MHz, (1.875MHz – 20MHz)		0.4		ps
			312.5MHz, (1.875MHz – 20MHz)		0.5		ps
			156.25MHz, (1.875MHz – 20MHz)		0.5		ps
			125MHz, (1.875MHz – 20MHz)		0.6		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	250		650	ps
odc	Output Duty Cycle		SELx[1:0] = 00	40		60	%
			SELx[1:0] ≠ 00	45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential crosspoint.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plots.

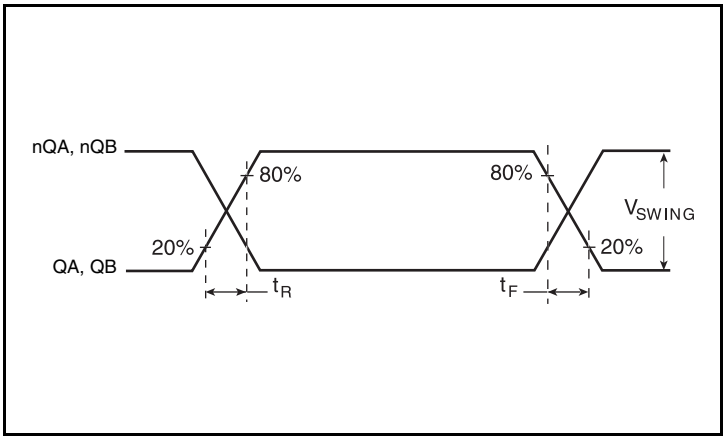
Typical Phase Noise at 625MHz



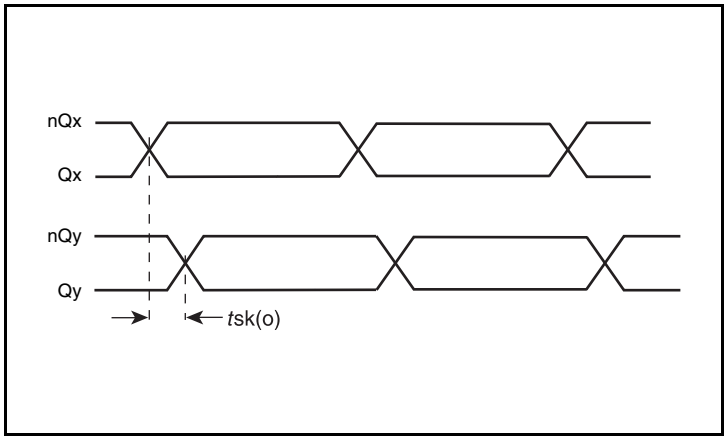
Parameter Measurement Information



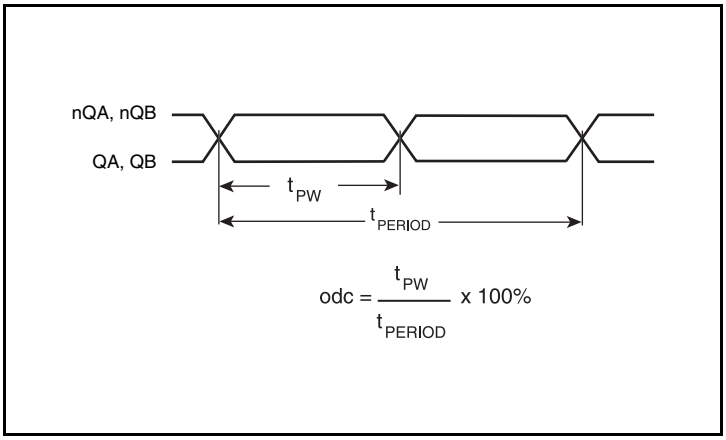
3.3V LVPECL Output Load AC Test Circuit



Output Rise/Fall Time



Output Skew



Output Duty Cycle/Pulse Width/Period

Application Information

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups and pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

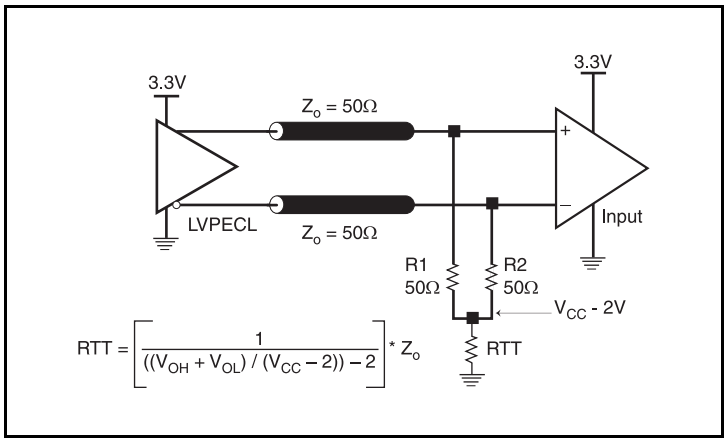


Figure 5A. 3.3V LVPECL Output Termination

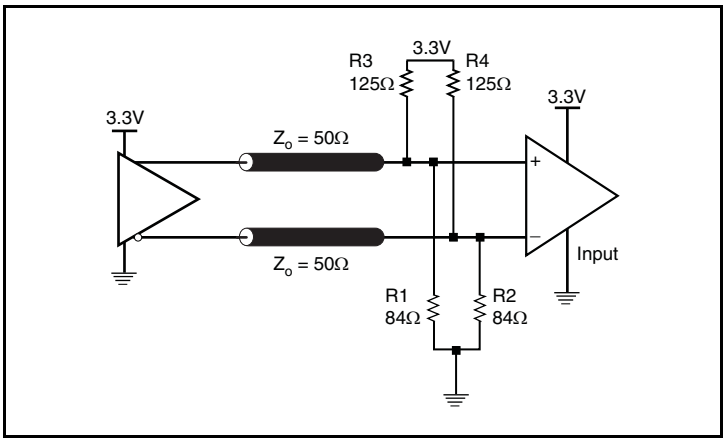


Figure 5B. 3.3V LVPECL Output Termination

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

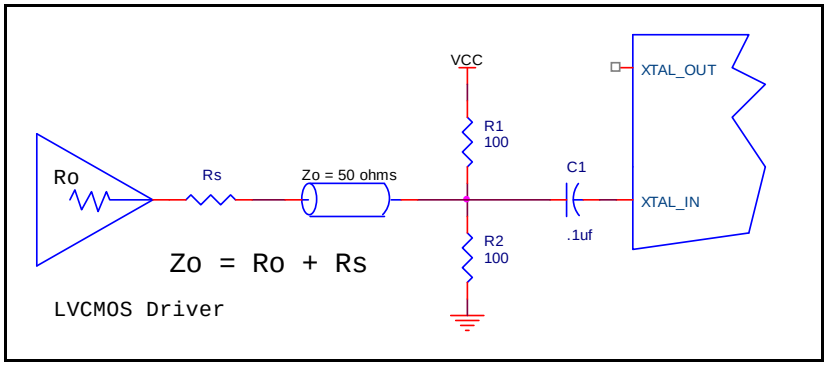


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

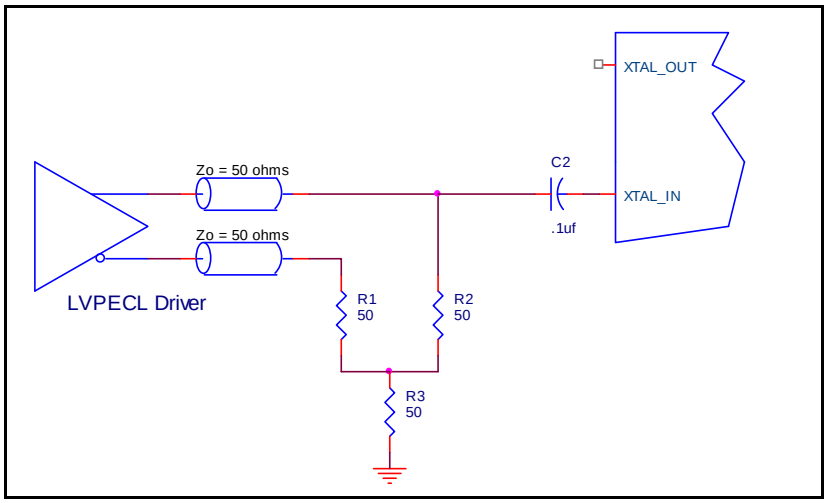


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Schematic Example

Figure 6 (next page) shows an example 843242 application schematic in which the device is operated at V_{CC} = 3.3V.

This example focuses on functional connections and is not configuration specific, particularly in the selection of 31.25MHz crystals instead of 26.041666MHz. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set for the application.

The 12pF parallel resonant Fox FX325BS 31.25MHz crystal is used with tuning capacitors C1 = 15pF and C2 = 21pF, which are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2. For this device, the crystal tuning capacitors are required for proper operation. As an alternate choice, a CL= 18pF HC-49/U crystal is shown with the appropriate tuning capacitors. These values may also require a slight adjustment depending on the parasitic capacity of the layout.

Crystal layout is very important to minimize capacitive coupling between the crystal pads and leads and other metal in the circuit board. Capacitive coupling to other conductors has two adverse effects; it reduces the oscillator frequency leaving less tuning margin and noise coupling from power planes and logic transitions on signal traces can pull the phase of the crystal resonance, inducing jitter. Routing I^2C under the crystal is a very common layout error, based on the assumption that it is a low frequency signal and will not affect the crystal oscillation. In fact, I^2C transition times are short enough to capacitively couple into the crystal if they are routed close enough to the crystal traces.

In layout, all capacitive coupling to the crystal from any signal trace is to be minimized, that is to the XTAL_IN and XTAL_OUT pins, traces to the crystal pads, the crystal pads and the tuning capacitors. Using a crystal on the top layer as an example, void all signal and power layers under the crystal connections between the top layer and the ground plane used by the 843242. Then calculate the parasitic capacity to the ground and determine if it is large enough to preclude tuning the oscillator. If the coupling is excessive, particularly if the first layer under the crystal is a ground plane, a layout option is to void the ground plane and all deeper layers until the next ground plane is reached. The ground connection of the tuning capacitors should first be made between the capacitors on the top layer, then a single ground via is dropped to connect the tuning cap ground to the ground plane as close to the 843242 as possible as shown in the schematic.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843242 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 10Ω V_{CCA} resistor and the 0.1µF capacitors in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB. Pull up and pull down resistors to set configuration pins can all be placed on the PCB side opposite to the device side to free up device side area if necessary.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

For additional layout recommendations and guidelines, contact clocks@idt.com.

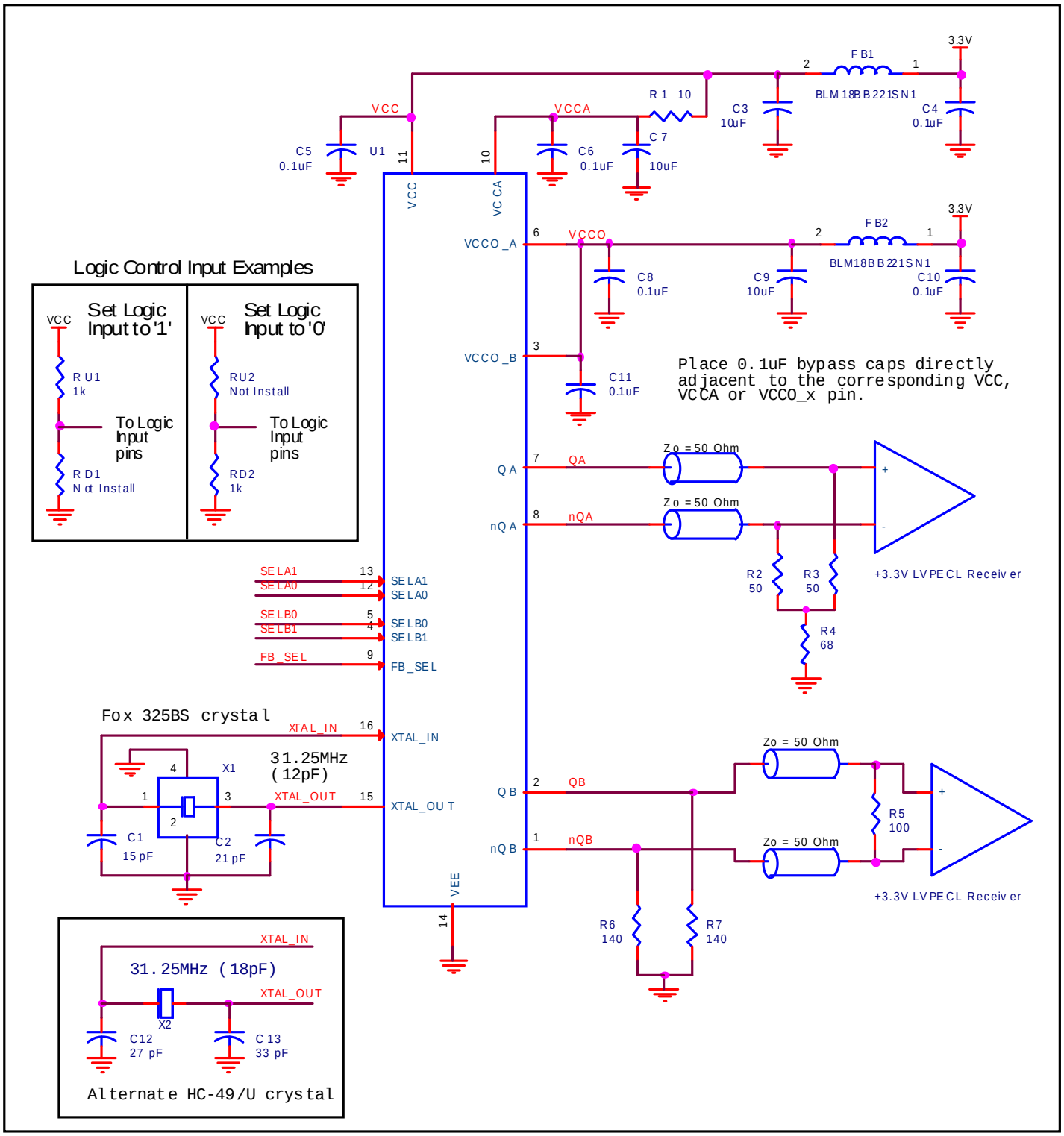


Figure 6. 843242 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 843242.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843242 is the sum of the core power plus the power dissipated due to the load.
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 158mA = **547.47mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 547.47mW + 60mW = **607.47mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 81.2°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.60747W * 81.2°C/W = 119.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 16-Lead TSSOP, Forced Convection

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	81.2°C/W	73.9°C/W	70.2°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 8.*

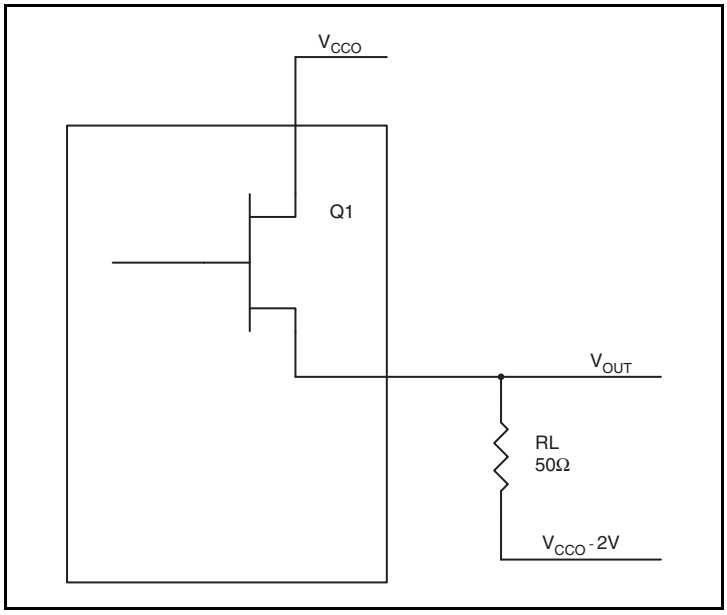


Figure 8. LVPECL Driver Circuit and Termination

To calculate power dissipation due to the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} – 0.9V$
  $(V_{CCO\_MAX} – V_{OH\_MAX}) =$ **0.9V**
- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} – 1.7V$
  $(V_{CCO\_MAX} – V_{OL\_MAX}) =$ **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 16-Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	81.2°C/W	73.9°C/W	70.2°C/W

Transistor Count

The transistor count for 843242 is: 3767

Package Outline and Package Dimensions

Package Outline - G Suffix for 16-Lead TSSOP

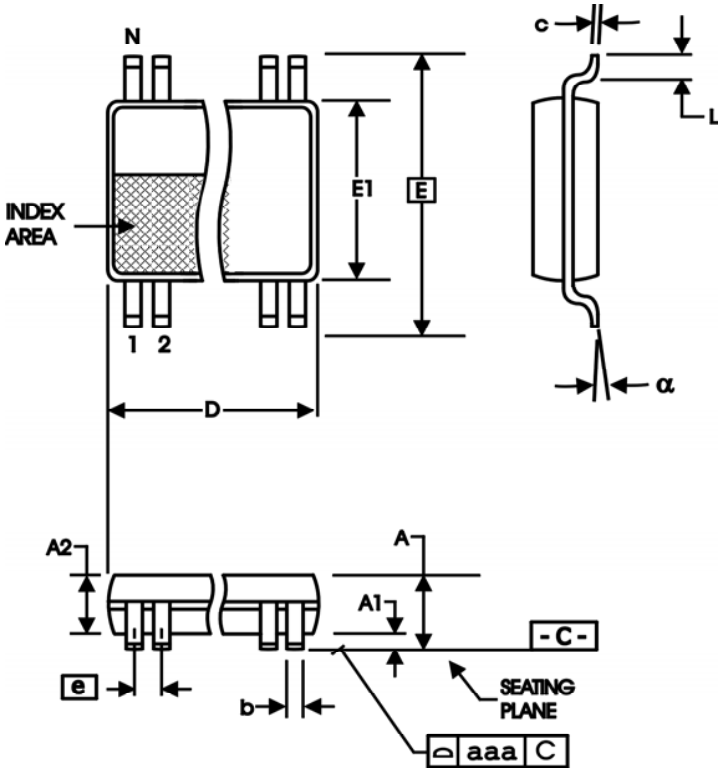


Table 9. Package Dimensions for 16-Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843242AGLF	843242AL	16-Lead TSSOP, Lead-Free	Tube	0°C to 70°C
843242AGLFT	843242AL	16-Lead TSSOP, Lead-Free	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an “G” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
1	T10	1 16	Block Diagram - added output clock lables. Ordering Information table - added note. Deleted “ICS” prefix from part number throughout the datasheet. Updated datasheet header/footer.	1/30/15

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