

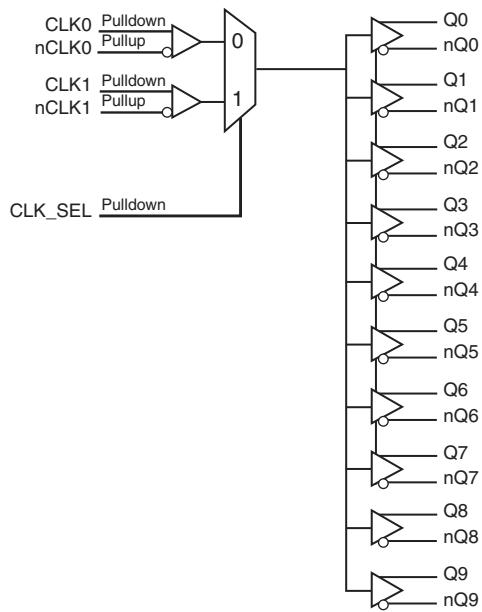
General Description

The 85310I-01 is a low skew, high performance 1-to-10 Differential-to-2.5V/3.3V ECL/LVPECL Fanout Buffer. The CLKx, nCLKx pairs can accept most standard differential input levels. The 85310I-01 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the 85310I-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

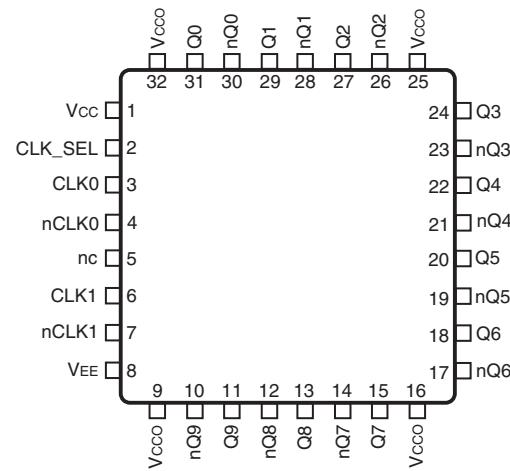
Features

- Ten differential 2.5V, 3.3V LVPECL/ECL output pair
- Two selectable differential input pairs
- Differential CLKx/nCLKx pairs can accept the following interface levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 700MHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Output skew: 30ps (typical)
- Part-to-part skew: 140ps (typical)
- Propagation delay: 2ns (typical)
- Additive phase jitter, RMS: <0.13ps (typical)
- LVPECL mode operating voltage supply range: $V_{CC} = 2.375V$ to $3.8V$, $V_{EE} = 0V$
- ECL mode operating voltage supply range: $V_{CC} = 0V$, $V_{EE} = -3.8V$ to $-2.375V$
- -40°C to 85°C ambient operating temperature
- Available in lead-free RoHS compliant package

Block Diagram



Pin Assignment



85310I-01
32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Table 1. Pin Descriptions

| Number | Name | Type | Description |
|---------------|------------------|--------|---|
| 1 | V _{CC} | Power | Positive supply pin. |
| 2 | CLK_SEL | Input | Pulldown |
| | | | Clock select input. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0, nCLK0 inputs. LVCMOS / LVTTL interface levels. |
| 3 | CLK0 | Input | Pulldown |
| 4 | nCLK0 | Input | Pullup |
| | | | Inverting differential clock input. |
| 5 | nc | Unused | |
| 6 | CLK1 | Input | Pulldown |
| | | | Non-inverting differential clock input. |
| 7 | nCLK1 | Input | Pullup |
| | | | Inverting differential clock input. |
| 8 | V _{EE} | Power | Negative supply pin. |
| 9, 16, 25, 32 | V _{CC0} | Power | Output supply pins. |
| 10, 11 | nQ9, Q9 | Output | Differential output pair. LVPECL interface levels. |
| 12, 13 | nQ8, Q8 | Output | Differential output pair. LVPECL interface levels. |
| 14, 15 | nQ7, Q7 | Output | Differential output pair. LVPECL interface levels. |
| 17, 18 | nQ6, Q6 | Output | Differential output pair. LVPECL interface levels. |
| 19, 20 | nQ5, Q5 | Output | Differential output pair. LVPECL interface levels. |
| 21, 22 | nQ4, Q4 | Output | Differential output pair. LVPECL interface levels. |
| 23, 24 | nQ3, Q3 | Output | Differential output pair. LVPECL interface levels. |
| 26, 27 | nQ2, Q2 | Output | Differential output pair. LVPECL interface levels. |
| 28, 29 | nQ1, Q1 | Output | Differential output pair. LVPECL interface levels. |
| 30, 31 | nQ0, Q0 | Output | Differential output pair. LVPECL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|--------------------------|
| Supply Voltage, V_{CC} | 4.6V |
| Inputs, V_I | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, I_O Continuous Current Surge Current | 50mA 100mA |
| Package Thermal Impedance, θ_{JA} | 47.9°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 2.375V$ to 3.8V; $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{CC} | Positive Supply Voltage | | 2.375 | 3.3 | 3.8 | V |
| V_{CCO} | Output Supply Voltage | | 2.375 | 3.3 | 3.8 | V |
| I_{EE} | Power Supply Current | | | | 120 | mA |

Table 3B. LVCMS/LVTTL DC Characteristics, $V_{CC} = V_{CCO} = 2.375V$ to 3.8V; $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|-----------------|---------------------------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | $V_{CC} = 3.3V$ | 2 | | $V_{CC} + 0.3$ | V |
| | | $V_{CC} = 2.5V$ | 1.7 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | $V_{CC} = 3.3V$ | -0.3 | | 0.8 | V |
| | | $V_{CC} = 2.5V$ | -0.3 | | 0.7 | V |
| I_{IH} | Input High Current | CLK_SEL | $V_{CC} = V_{IN} = 3.8V$ | | 150 | μA |
| I_{IL} | Input Low Current | CLK_SEL | $V_{CC} = 3.8V$, $V_{IN} = 0V$ | -5 | | μA |

Table 3C. DC Characteristics, $V_{CC} = V_{CCO} = 2.375V$ to $3.8V$; $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | | Minimum | Typical | Maximum | Units |
|-----------|------------------------------|-----------------|--|----------------|---------|-----------------|---------|
| I_{IH} | Input High Current | CLK[0:1], | $V_{CC} = V_{IN} = 3.8V$ or $2.625V$ | | | 150 | μA |
| | | nCLK[0:1] | $V_{CC} = V_{IN} = 3.8V$ or $2.625V$ | | | 5 | μA |
| I_{IL} | Input Low Current | CLK[0:1] | $V_{CC} = 3.8V$ or $2.625V$, $V_{IN} = 0V$ | -5 | | | μA |
| | | nCLK[0:1] | $V_{CC} = 3.8V$ or $2.625V$, $V_{IN} = 0V$ | -150 | | | μA |
| V_{PP} | Peak-to-Peak Voltage; NOTE 1 | | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Range; NOTE 1, 2 | | | $V_{EE} + 0.5$ | | $V_{CC} - 0.85$ | V |

NOTE 1: V_{IL} should not be less than $-0.3V$.NOTE 2: Common mode voltage is defined as V_{IH} .**Table 3D. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 2.375V$ to $3.8V$; $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{CCO} - 1.4$ | | $V_{CCO} - 0.9$ | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{CCO} - 2.0$ | | $V_{CCO} - 1.7$ | V |
| V_{swing} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} - 2V$.

AC Electrical Characteristics

Table 4. AC Characteristics, $V_{CC} = V_{CCO} = 2.375V$ to $3.8V$; $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------------------|--|-----------------|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 700 | MHz |
| f_{jit} | Additive Phase Jitter, RMS; refer to Additive Phase Jitter section | | | <0.13 | | ps |
| t_{PD} | Propagation Delay; NOTE 1 | | | 2 | 2.5 | ns |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 2, 3 | | | 140 | 340 | ps |
| $t_{sk(o)}$ | Output Skew; NOTE 3, 4 | | | 30 | 55 | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 200 | | 700 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at $500MHz$, unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

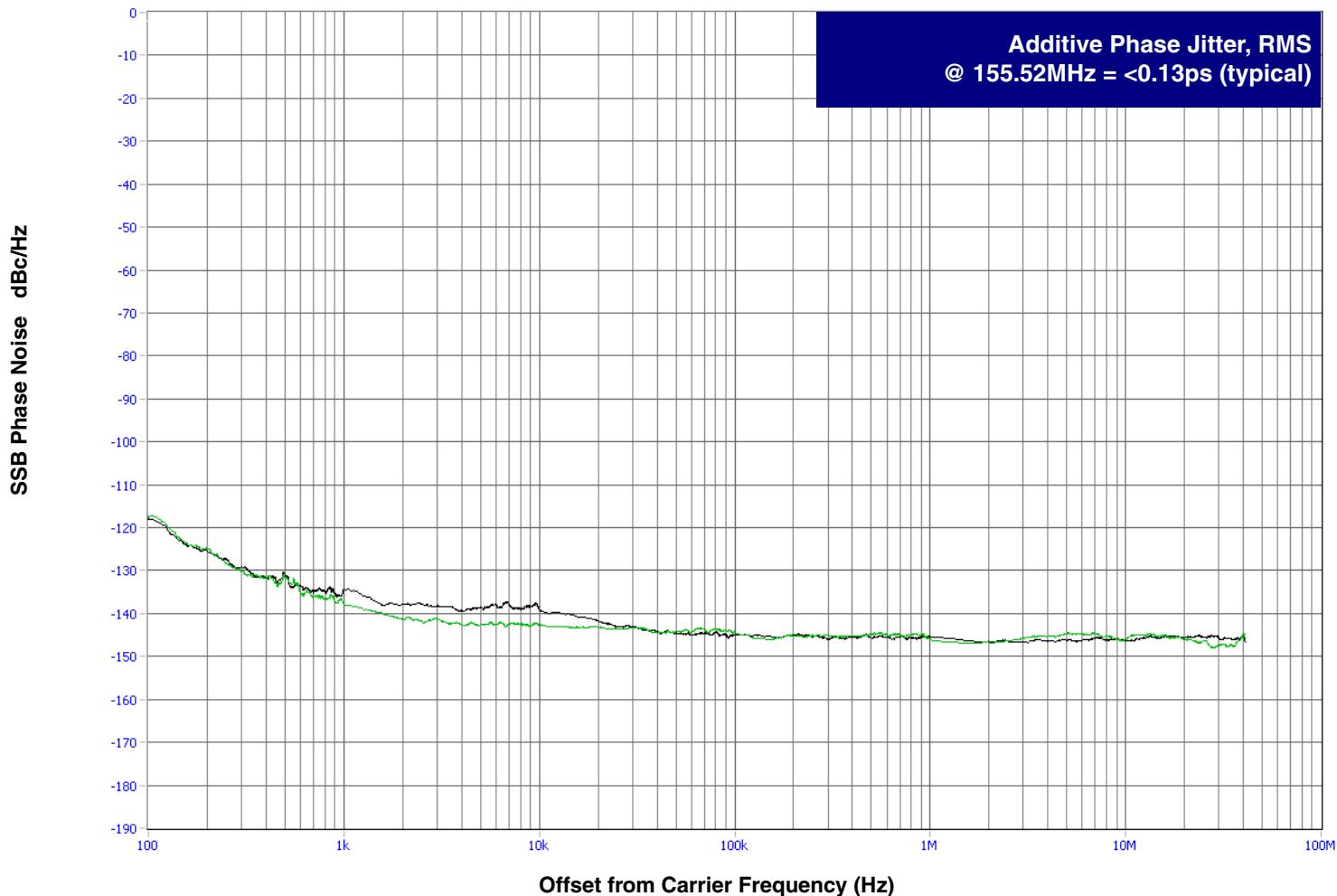
NOTE 3: This parameter is defined according with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

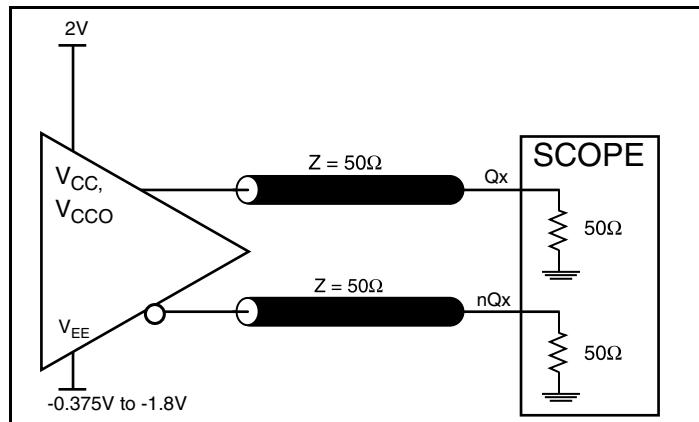
of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



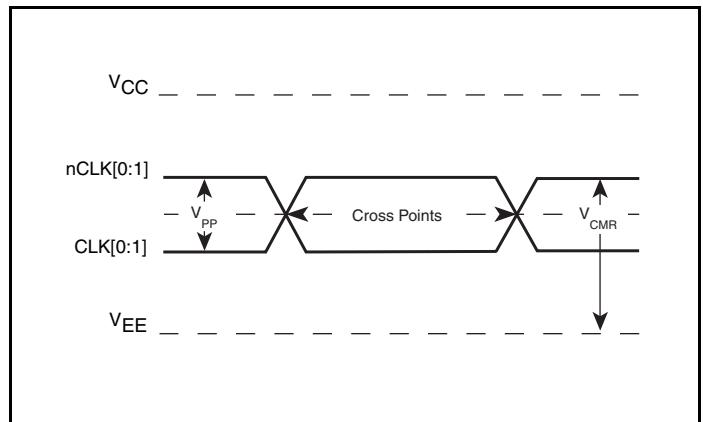
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This

is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

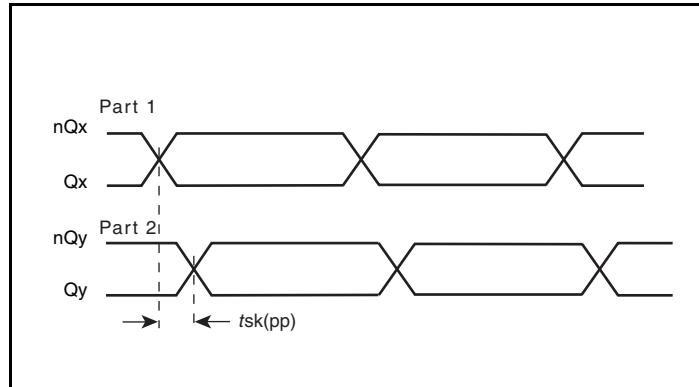
Parameter Measurement Information



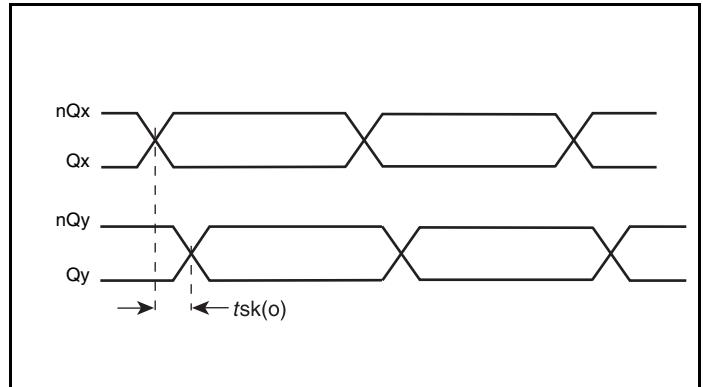
LVPECL Output Load AC Test Circuit



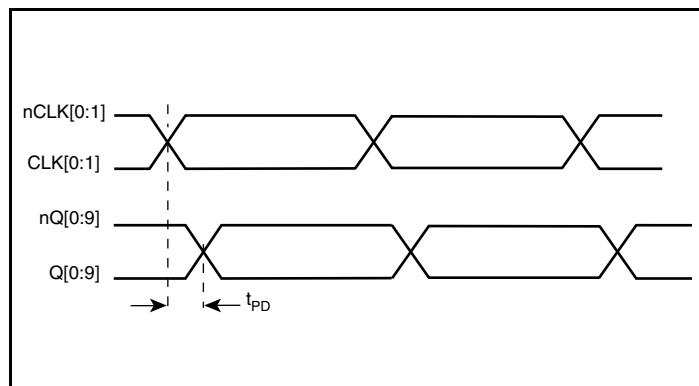
Differential Input Level



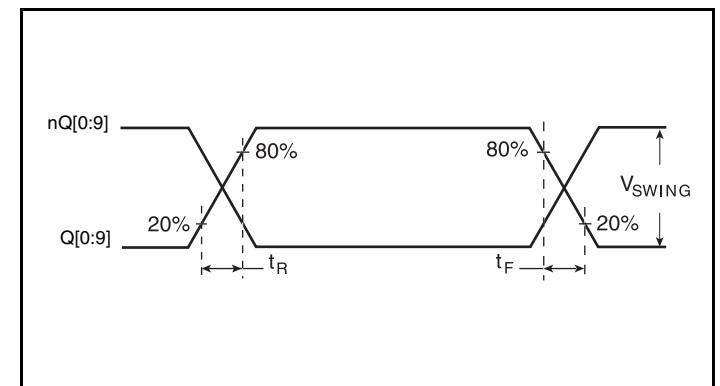
Part-to-Part Skew



Output Skew

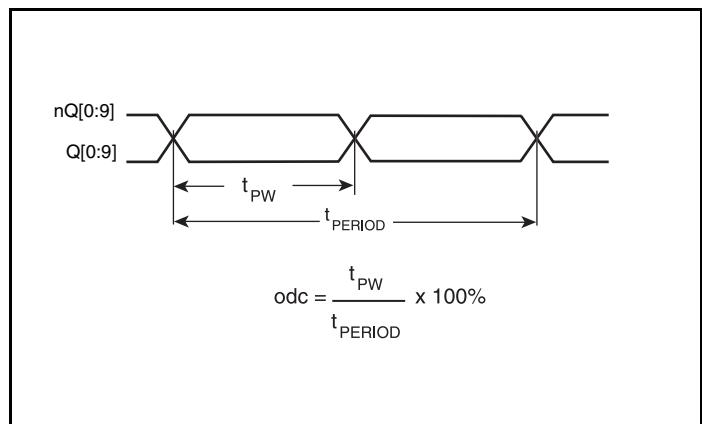


Propagation Delay



Output Rise/Fall Time

Parameter Measurement Information



Output Duty Cycle/Pulse Width/Period

Application Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

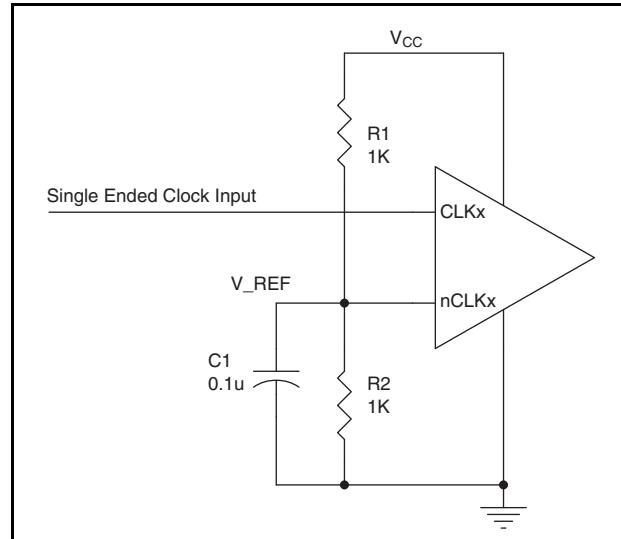


Figure 1. Single-Ended Signal Driving Differential Input

Recommendations for Unused Input Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from CLK to ground.

Single-ended LVPECL Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2F show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

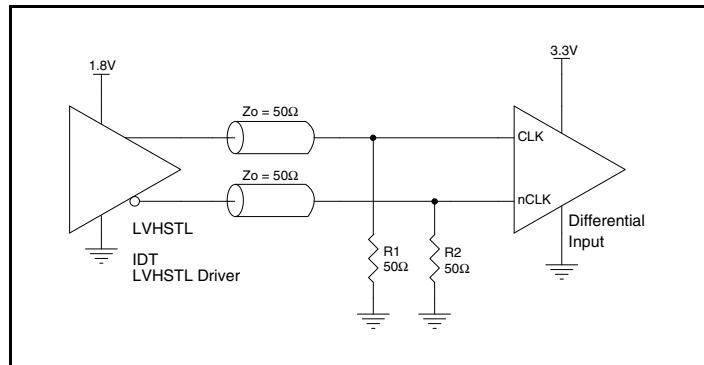


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

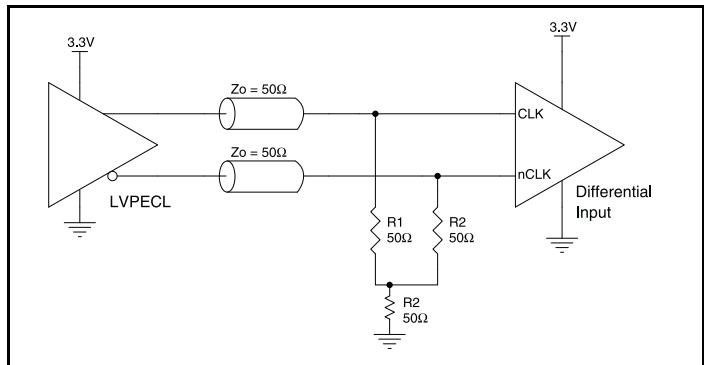


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

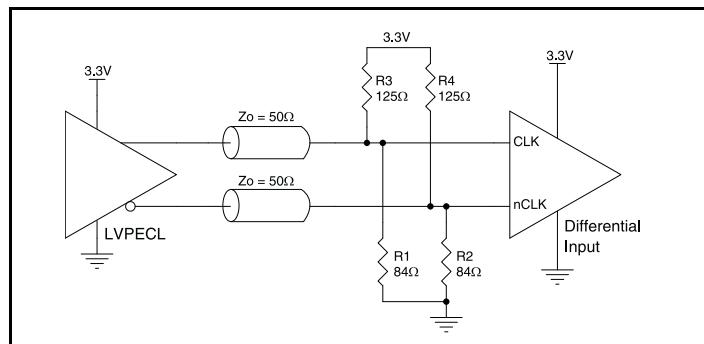


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

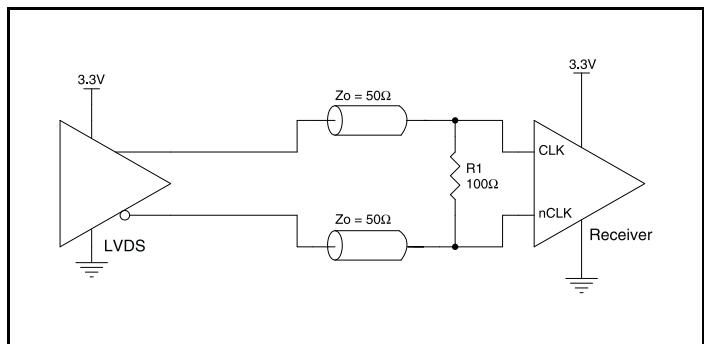


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

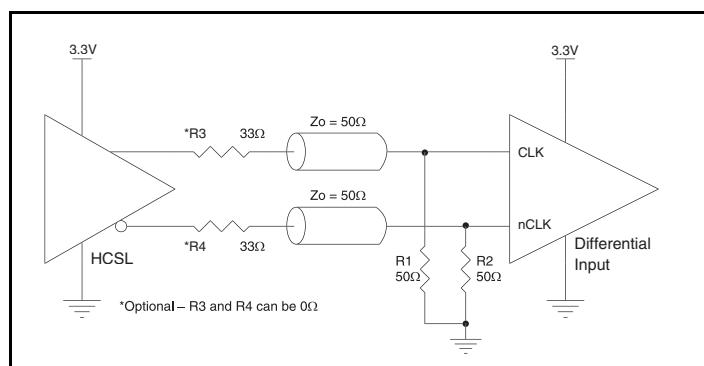


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

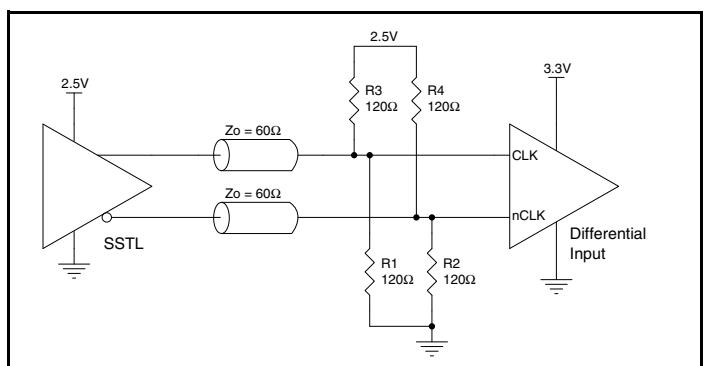


Figure 2F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

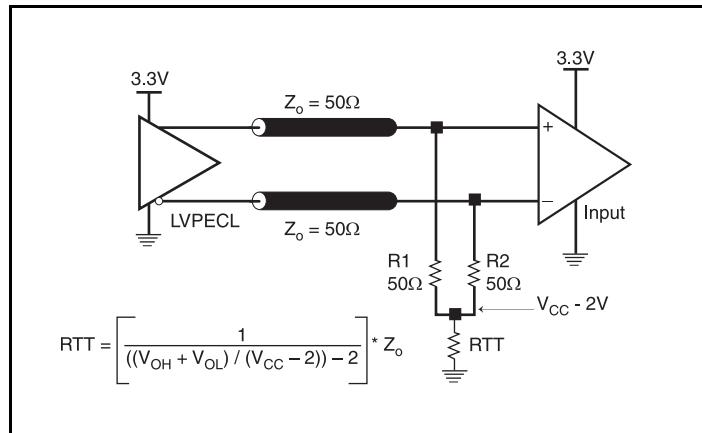


Figure 3A. 3.3V LVPECL Output Termination

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figures 3A and 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

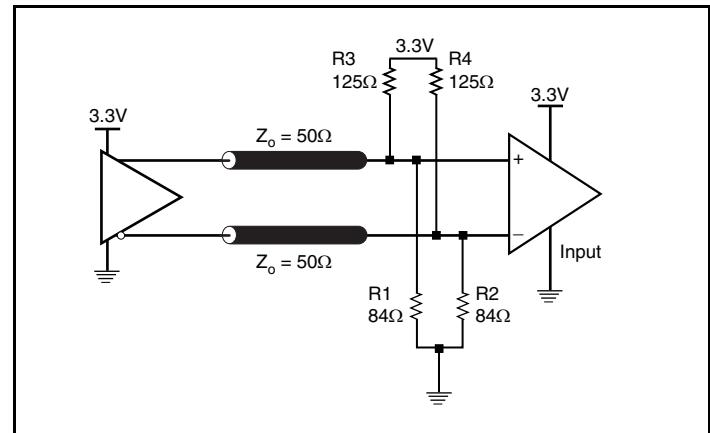


Figure 3B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CC} = 2.5V$, the $V_{CC} - 2V$ is very close to ground

level. The $R3$ in Figure 4B can be eliminated and the termination is shown in Figure 4C.

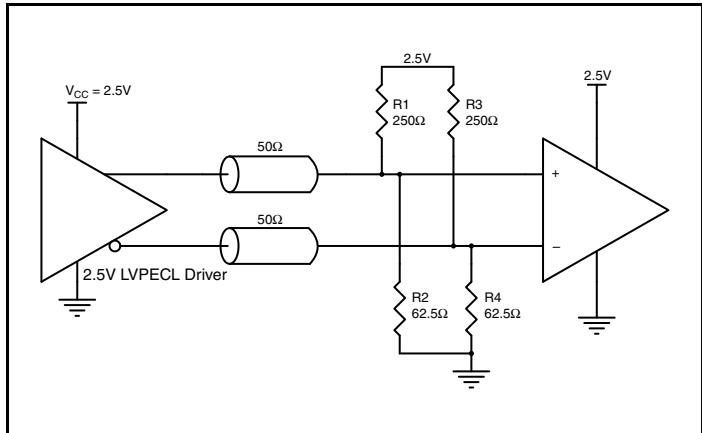


Figure 4A. 2.5V LVPECL Driver Termination Example

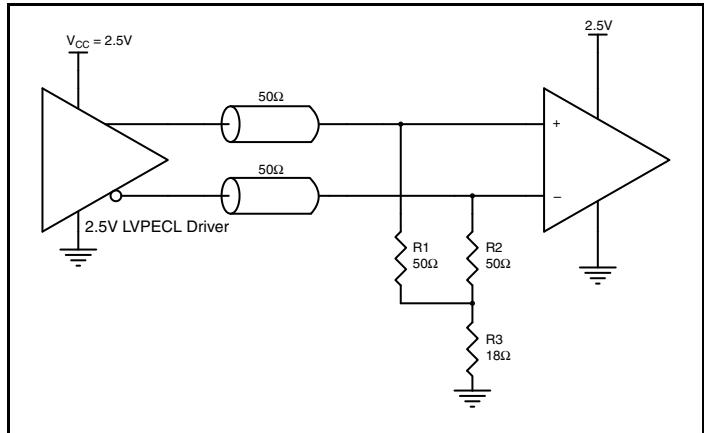


Figure 4B. 2.5V LVPECL Driver Termination Example

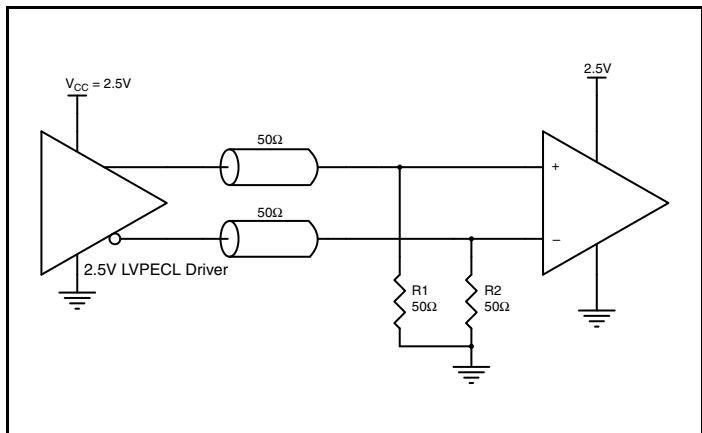


Figure 4C. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS5310I-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS5310I-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.8V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.8V * 120mA = 456mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is $10 * 30mW = 300mW$

Total Power_{MAX} (3.8V, with all outputs switching) = $456mW + 300mW = 756mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is $125^\circ C$. Limiting the internal transistor junction temperature, T_j , to $125^\circ C$ ensures that the bond wire and bond pad temperature remains below $125^\circ C$.

The equation for T_j is as follows: $T_j = \theta_{JA} * P_{d_total} + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

P_{d_total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is $42.1^\circ C/W$ per Table 5 below.

Therefore, T_j for an ambient temperature of $85^\circ C$ with all outputs switching is:

$85^\circ C + 0.756W * 42.1^\circ C/W = 116.8^\circ C$. This is well below the limit of $125^\circ C$.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 5. Thermal Resistance θ_{JA} for 32 Lead LQFP, Forced Convection

| θ_{JA} by Velocity | | | |
|---|----------|----------|----------|
| Linear Feet per Minute | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |
| NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. | | | |

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 5*.

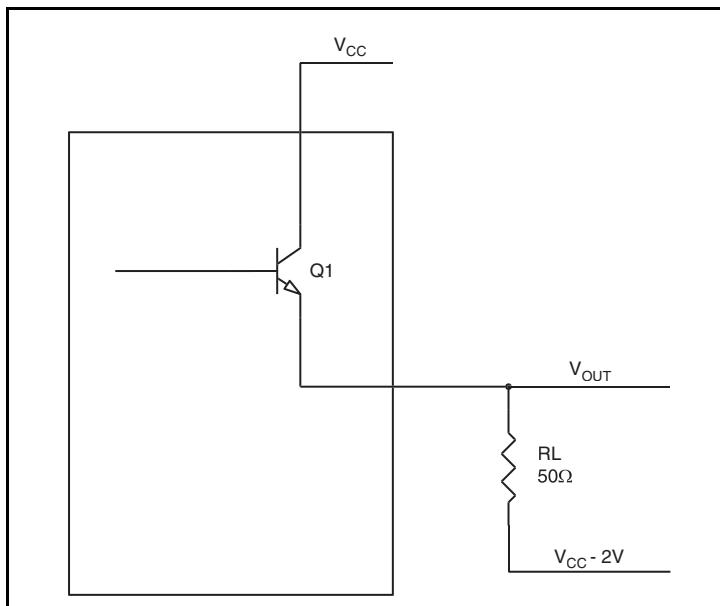


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 0.935V$
 $(V_{CCO_MAX} - V_{OH_MAX}) = 0.935V$
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.67V$
 $(V_{CCO_MAX} - V_{OL_MAX}) = 1.67V$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = $Pd_H + Pd_L = 30mW$

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 32 Lead LQFP

| θ_{JA} by Velocity | | | |
|---|----------|----------|----------|
| Linear Feet per Minute | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |
| NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. | | | |

Transistor Count

The transistor count for 85310I-01 is: 1034

Pin compatible with MC100LVEP111

Package Outline and Package Dimensions

Package Outline - Y Suffix for 32 Lead LQFP

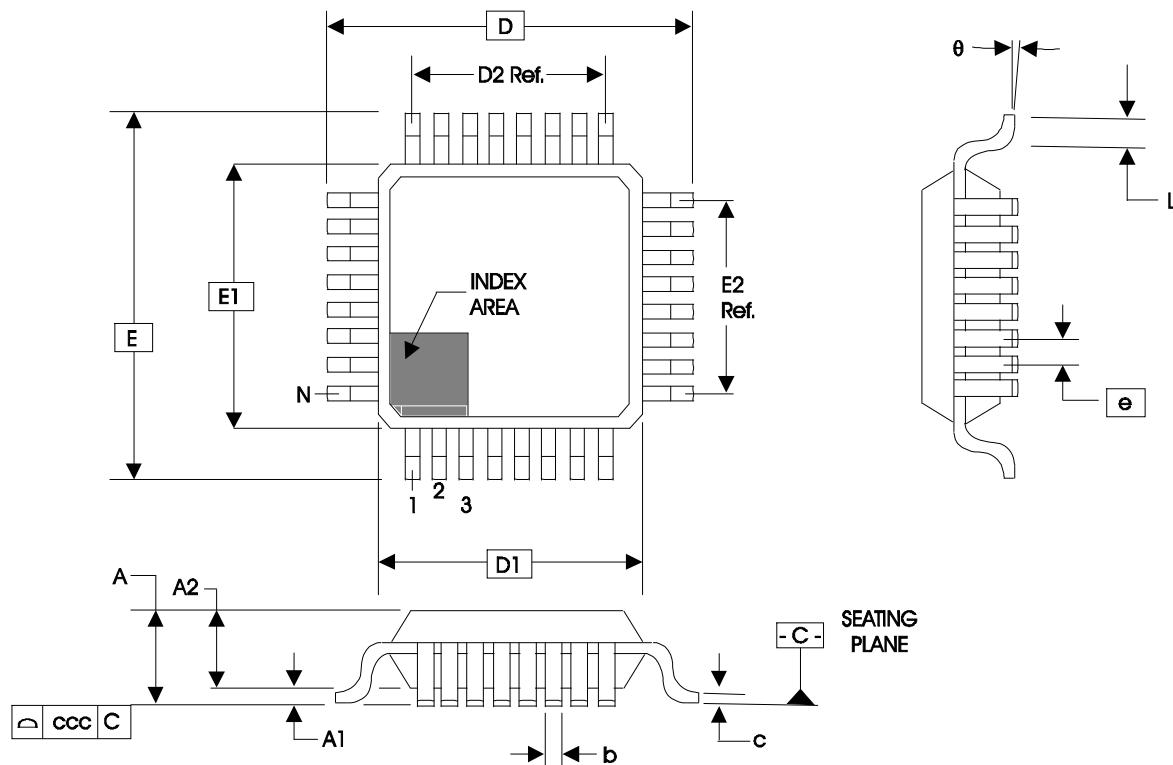


Table 7. Package Dimensions for 32 Lead LQFP

| JEDEC Variation: BBA All Dimensions in Millimeters | | | |
|---|------------|---------|---------|
| Symbol | Minimum | Nominal | Maximum |
| N | 32 | | |
| A | | | 1.60 |
| A1 | 0.05 | | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.45 |
| c | 0.09 | | 0.20 |
| D & E | 9.00 Basic | | |
| D1 & E1 | 7.00 Basic | | |
| D2 & E2 | 5.60 Ref. | | |
| e | 0.80 Basic | | |
| L | 0.45 | 0.60 | 0.75 |
| θ | 0° | | 7° |
| ccc | | | 0.10 |

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 8. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|--------------|---------------------------------|--------------------|---------------|
| 85310AYI-01LF | ICS5310AI01L | “Lead-Free” 32 Lead LQFP | Tray | -40°C to 85°C |
| 85310AYI-01LFT | ICS5310AI01L | “Lead-Free” 32 Lead LQFP | Tape & Reel | -40°C to 85°C |
| 85310AYI-01LN | ICS5310AI01N | Lead-Free/Annealed 32 Lead LQFP | Tray | -40°C to 85°C |
| 85310AYI-01LNT | ICS5310AI01N | Lead-Free/Annealed 32 Lead LQFP | Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" and "LN" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|-----|------------|------------------------|--|----------|
| B | T4 | 4 | AC Characteristics table - t_{PD} row, revised value from 2.25ns Max. to 2.5ns Max. | 4/29/02 |
| B | | 8 | Added <i>Termination for LVPECL Outputs</i> . | 5/29/02 |
| C | T3D | 4 | Added <i>LVPECL DC Characteristics table</i> . Changed part number from ICS85310-01 to 85310I-01 in title and all subsequent areas throughout the datasheet. | 7/26/02 |
| D | T3A | 3 7 | Power Supply table - increased max. value for I_{EE} to 120mA from 30mA max. Power Considerations have re-adjusted to the increased I_{EE} value. | 10/22/02 |
| E | T2 | 2 3 6 7 12 | Pin Characteristics - changed C_{IN} 4pF max. to 4pF typical. Absolute Maximum Ratings - updated Outputs. Updated <i>Single Ended Signal Driving Differential Input</i> drawing and <i>LVPECL Output Termination</i> drawings. Added <i>Differential Clock Input Interface</i> section. Added Lead Free/A annealed part number. | 6/14/04 |
| F | T8 | 1 5 13 | Features Section - added Additive Phase Jitter bullet. Added <i>Additive Phase Jitter</i> Section. Ordering Information Table - added Lead-Free Note. | 6/22/05 |
| F | T8 | 7 14 | Added <i>Recommendations for Unused Input and Output Pins</i> . Ordering Information Table - added lead-free part number and marking. | 1/16/06 |
| G | T3D | 4 10 - 11 | LVPECL DC Characteristics Table - corrected V_{OH} max. from V_{CCO} - 1.0V to V_{CCO} - 0.9V; and V_{SWING} max. from 0.85V to 1.0V. Power Considerations - corrected power dissipation to reflect V_{OH} max in Table 3D. | 4/11/07 |
| H | T3B T3D | 3 4 9 11 | LVCMOS DC Characteristics Table - corrected I_{IH}/I_{IL} specs. Added missing V_{IH}/V_{IL} 2.5V specs. LVPECL DC Characteristics Table - corrected V_{OH} max. from 0.9V to V_{CCO} - 0.9V. Updated <i>Differential Clock Input Interface</i> section. Added <i>Termination for 2.5V LVPECL Outputs</i> section. Converted datasheet format. | 4/23/09 |
| I | | 1 10 | Pin Assignment - corrected typo on pin 16 from "cco" to "Vcco". Termination for 3.3V LVPECL Outputs - updated Diagrams 3A & 3B. Updated Header/Footer of datasheet. | 1/15/10 |
| I | T8 | 16 | Ordering Information Table - add "T" at end of Part/Order Number for 85310AYI-01LN. | 1/25/10 |
| I | T8 | 16 | Ordering Information Table - Removed leaded devices. Updated data sheet format. | 7/8/15 |



Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com

Tech Support
email: clocks@idt.com

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications, such as those requiring extended temperature ranges, high reliability or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Product specification subject to change without notice. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.

Copyright ©2015 Integrated Device Technology, Inc.. All rights reserved.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.