

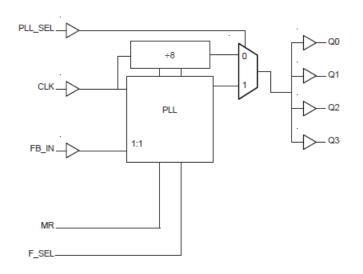
GENERAL DESCRIPTION

The 86004-01 is a high performance 1-to-4 LVCMOS/LVTTL Clock Buffer and a member of the family of High Performance Clock Solutions from IDT. The 86004-01 has a fully integrated PLL and can be configured as zero delay buffer and has an input and output frequency range of 62.5MHz to 250MHz. The external feedback allows the device to achieve "zero delay" between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output divider.

CONTROL INPUT FUNCTION TABLE

Input	Input/Output Frequency Range (MHz)		
F_SEL	Minimum	Maximum	
0	125	250	
1	62.5	125	

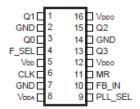
BLOCK DIAGRAM



FEATURES

- Four LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Single LVCMOS/LVTTL clock input
- · CLK accepts the following input levels: LVCMOS or LVTTL
- Output frequency range: 62.5MHz to 250MHz
- Input frequency range: 62.5MHz to 250MHz
- External feedback for "zero delay" clock regeneration with configurable frequencies
- · Fully integrated PLL
- Cycle-to-cycle jitter, (F_SEL = 1): 45ps (maximum)
- · Output skew: 60ps (maximum)
- Supply Voltage Modes: (Core/Output) 3.3V/3.3V 3.3V/2.5V 2.5V/2.5V
- · 5V tolerant input
- -40°C to 70°C ambient operating temperature
- · Available in lead-free (RoHS 6) package

PIN ASSIGNMENT



86004-01 16-Lead TSSOP4.4mm x 5.0mm x 0.925mm package body **G Package**Top View



TABLE 1. PIN DESCRIPTIONS

Number	Name	Т	уре	Description
1, 3, 13, 15	Q1, Q0, Q3, Q2	Output		Clock outputs. 7Ω typical output impedance. LVCMOS/LVTTL interface levels.
2, 7, 14	GND	Power		Power supply ground.
4	F_SEL	Input	Pulldown	Frequency range select input. When LOW, I/O frequency range is from 125MHz to 250Mz. When HIGH, I/O frequency range is from 62.5MHz to 125MHz. LVCMOS/LVTTL interface levels.
5	V _{DD}	Power		Core supply pin.
6	CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
8	V _{DDA}	Power		Analog supply pin.
9	PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as input to the dividers. When LOW, selects the reference clock (PLL Bypass). When HIGH, selects PLL (PLL Enabled). LVCMOS/LVTTL interface levels.
10	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with "zero delay". Connect to one of the outputs. LVCMOS/LVTTL interface levels.
11	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
12, 16	V _{DDO}	Power		Output supply pins.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R	Input Pullup Resistor			51		kΩ
R	Input Pulldown Resistor			51		kΩ
	Power Dissipation Capacitance	$V_{_{DD}}, V_{_{DDO}} = 3.465V$			23	pF
PD	(per output)	$V_{_{DD}}, V_{_{DDO}} = 2.625V$			17	pF
R _{OUT}	Output Impedance	3.3V ± 5%	5	7	12	Ω

TABLE 3. CONTROL INPUT FUNCTION TABLE

Input	Input/Output Frequency Range (MHz)			
F_SEL	Minimum	Maximum		
0	125	250		
1	62.5	125		



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} 4.6V

Inputs, V -0.5V to +5.0V

Outputs, V_{o} -0.5V to V_{dd} + 0.5V

Package Thermal Impedance, $\theta_{\text{\tiny IA}}$ 89°C/W (0 Ifpm)

Storage Temperature, T_{STG} -65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, Ta = -40°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V _{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V _{DDA}	Analog Supply Voltage		3.135	3.3	V	V
V _{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I _{DD}	Power Supply Current				100	mA
DDA	Analog Supply Current				16	mA
I _{DDO}	Output Supply Current				6	mA

NOTE: Special thermal handling maybe required in some configurations.

Table 4B. Power Supply DC Characteristics, $V_{_{DD}} = 3.3V \pm 5\%$, $V_{_{DDO}} = 2.5V \pm 5\%$, Ta = -40°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V _{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V	Analog Supply Voltage		3.135	3.3	V	V
V _{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I _{DD}	Power Supply Current				100	mA
DDA	Analog Supply Current				16	mA
 DDO	Output Supply Current				6	mA

Table 4C. Power Supply DC Characteristics, $V_{DD} = V_{DDD} = 2.5V \pm 5\%$, Ta = -40°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V _{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V _{DDA}	Analog Supply Voltage		2.375	2.5	V	V
V _{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I _{DD}	Power Supply Current				96	mA
 DDA	Analog Supply Current				15	mA
DDO	Output Supply Current				6	mA

NOTE: Special thermal handling maybe required in some configurations.



Table 4D. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, Ta = -40°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V	Input High Voltage		V _{DD} = 3.465V	2.0		5.0	V
V _{IH}	Imput riigh voltage		V _{DD} = 2.625V	1.7		5.0	V
V	Input Low Voltage		V _{DD} = 3.465V	-0.3		0.8	V
V	Imput Low voltage		$V_{_{DD}} = 2.625V$	-0.3		0.7	V
I	Input High Current	CLK, MR, FB_IN, F_SEL	$V_{DD} = V_{IN} = 3.465 V \text{ or } 2.625 V$			150	μΑ
"		PLL_SEL	$V_{DD} = V_{IN} = 3.465 V \text{ or } 2.625 V$			5	μA
	Input Low Current	CLK, MR, FB_IN, F_SEL	$V_{DD} = 3.465V \text{ or } 2.625V,$ $V_{IN} = 0V$	-5			μА
' _{IL}	Imput Low Guiterit	PLL_SEL	$V_{DD} = 3.465V \text{ or } 2.625V,$ $V_{IN} = 0V$	-150			μА
\ <u></u>	Output High Voltage; NOTE 1		$V_{_{DDO}} = 3.465V$	2.6			V
V _{OH}			V _{DDO} = 2.625V	1.8			V
V _{OL}	Output Low Voltage;	NOTE 1	$V_{DDO} = 3.465 \text{V} \text{ or } 2.625 \text{V}$			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{ppo}/2$. See Parameter Measurement Information Section, Output Load Test Circuit diagrams.

Table 5A. AC Characteristics, $V_{DD} = V_{DDD} = 3.3V \pm 5\%$, Ta = -40°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f	Output Fraguency	F_SEL = 0	125		250	MHz
MAX	Output Frequency	F_SEL = 1	62.5		125	MHz
tp _{LH}	Propagation Delay, Low-to-High; NOTE 1	PLL_SEL = 0V, Bypass Mode	4.1	5.1	6.1	ns
t(Ø)	Static Phase Offset; NOTE 2, 4	PLL_SEL = 3.3V	-75	50	175	ps
tsk(o)	Output Skew; NOTE 3, 4	PLL_SEL = 0V			60	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 4	F_SEL = 0			65	ps
	Cycle-to-Cycle Sitter, NOTE 4	F_SEL = 1			45	ps
t_	PLL Lock Time				1	mS
t _R / t _F	Output Rise/Fall Time		300		750	ps
	Output Duty Cycle	F_SEL = 0	44	50	56	%
odc	Output Duty Cycle	F_SEL = 1	47	50	53	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. All parameters measured at f noted otherwise.

All parameters measured at f $_{\text{\tiny MAX}}$ unless noted otherwise. NOTE 1: Measured from the differential input crossing point to the output at V $_{\text{\tiny DDO}}/2$.

NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions.

Measured at V_{DDO}/2.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



Table 5B. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDD} = 2.5V \pm 5\%$, $TA = -40^{\circ}C$ to $70^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f	Output Fraguenay	F_SEL = 0	125		250	MHz
MAX	Output Frequency	F_SEL = 1	62.5		125	MHz
tp _{LH}	Propagation Delay, Low-to-High; NOTE 1	PLL_SEL = 0V, Bypass Mode	4.25	5.25	6.25	ns
t(Ø)	Static Phase Offset; NOTE 2, 4	PLL_SEL = 3.3V	-300		0	ps
tsk(o)	Output Skew; NOTE 3, 4	PLL_SEL = 0V			60	ps
tiit(co)	Cycle-to-Cycle Jitter; NOTE 4	F_SEL = 0			65	ps
tjit(cc)	Cycle-to-Cycle Sitter, NOTE 4	F_SEL = 1			45	ps
t	PLL Lock Time				1	mS
t _R / t _F	Output Rise/Fall Time		300		700	ps
odc	Output Duty Cycle		45	50	55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. All parameters measured at f_{MAX} unless noted otherwise.

All parameters measured at $f_{_{\text{\scriptsize MAX}}}$ unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output at V___/2.

NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions.

Measured at V_{pp}/2.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

Table 5C. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, Ta = -40°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f	Output Fraguenay	F_SEL = 0	125		250	MHz
f _{MAX}	Output Frequency	F_SEL = 1	62.5		125	MHz
tp _{LH}	Propagation Delay, Low-to-High; NOTE 1	PLL_SEL = 0V, Bypass Mode	4.5	5.5	6.5	ns
t(Ø)	Static Phase Offset; NOTE 2, 4	PLL_SEL = 3.3V	-100		250	ps
tsk(o)	Output Skew; NOTE 3, 4	PLL_SEL = 0V			55	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 4	F_SEL = 0			65	ps
ווו(ככ)	Cycle-to-Cycle Sitter, NOTE 4	F_SEL = 1			45	ps
t_	PLL Lock Time				1	mS
t _r / t _r	Output Rise/Fall Time		300		700	ps
odc	Output Duty Cycle		45	50	55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. All parameters measured at f unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output at $V_{pool}/2$.

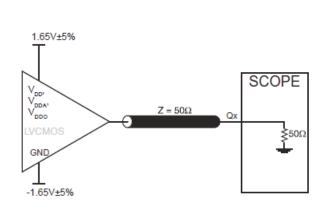
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

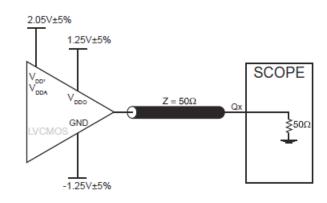
NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{poo}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



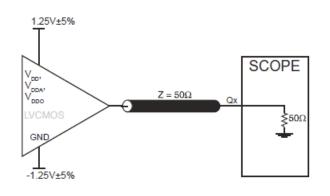
PARAMETER MEASUREMENT INFORMATION

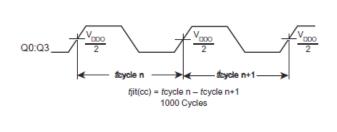




3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT

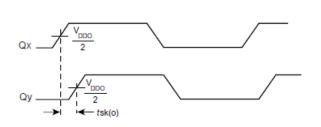
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT

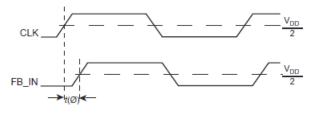




2.5VCore/ 2.5V OUTPUT LOAD AC TEST CIRCUIT

CYCLE-TO-CYCLE JITTER



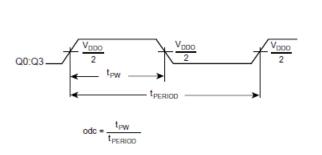


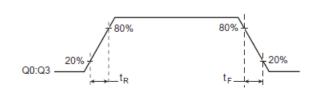
 $t(\emptyset)$ mean = Static Phase Offset (where $t(\emptyset)$ is any random sample, and $t(\emptyset)$ mean is the average of the sampled cycles measured on controlled edges)

OUTPUT SKEW

STATIC PHASE OFFSET

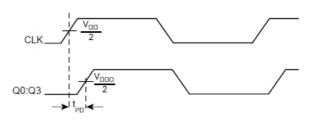






OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

OUTPUT RISE/FALL TIME



PROPAGATION DELAY



APPLICATION INFORMATION

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 86004-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{\scriptscriptstyle DD}$, $V_{\scriptscriptstyle DDA}$ and $V_{\scriptscriptstyle DDO}$ should be individually connected to the power supply plane through vias, and $0.01\mu F$ bypass capacitors should be used for each pin. Figure 1 illustrates this for a generic $V_{\scriptscriptstyle DD}$ pin and also shows that $V_{\scriptscriptstyle DDA}$ requires that an additional 10Ω resistor along with a $10\mu F$ bypass capacitor be connected to the $V_{\scriptscriptstyle DDA}$ pin.

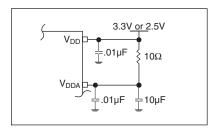


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS:

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A $1k\Omega$ resistor can be used.

OUTPUTS:

LVCMOS OUTPUTS:

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

SCHEMATIC EXAMPLE

Figure 2 shows a schematic example of using an 86004-01. It is recommended to have one decouple capacitor per power pin. Each decoupling capacitor should be located as close as

possible to the power pin. The low pass filter R7, C11 and C16 for clean analog supply should also be located as close to the $V_{\tiny DDA}$ pin as possible.

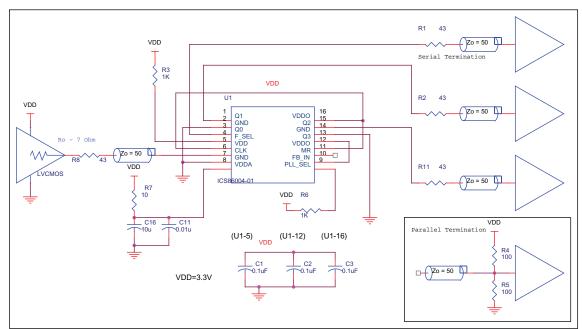


FIGURE 2. 86004-01 SCHEMATIC EXAMPLE



RELIABILITY INFORMATION

Table 6. $\theta_{_{JA}} \text{vs. Air Flow Table for 16 Lead TSSOP}$

θ_{JA} by Velocity (Linear Feet per Minute)

0200500Single-Layer PCB, JEDEC Standard Test Boards137.1°C/W118.2°C/W106.8°C/WMulti-Layer PCB, JEDEC Standard Test Boards89.0°C/W81.8°C/W78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 86004-01 is: 2496

PACKAGE OUTLINE AND DIMENSIONS

PACKAGE OUTLINE - G SUFFIX 16 LEAD TSSOP

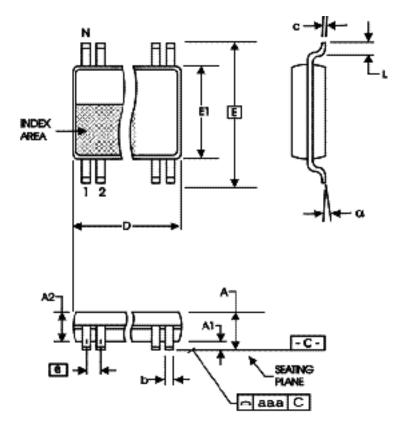


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millim	neters
STWIDOL	Minimum	Maximum
N	1	6
Α		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
С	0.09	0.20
D	4.90	5.10
Е	6.40 E	BASIC
E1	4.30	4.50
е	0.65 E	BASIC
L	0.45	0.75
α	0° 8°	
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153



Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
86004BG-01LF	6004B01L	16 lead "Lead Free" TSSOP	Tube	0°C to +70°C
86004BG-01LFT	6004B01L	16 lead "Lead Free" TSSOP	Tape and Reel	0°C to +70°C



REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	
Α			Throughout data sheet, changed part number from ICS86004I-01 to ICS86004-01.	
Α	T7	1 11	Features section - added Lead-Free bullet. Ordering Information table - added Lead Free part number.	
А			Changed temperature range throughout the data sheet from "-40°C - 85°C" to "0°C - 70°C".	
В	T4A T4B T4C T7	1 3 3 3 11	Features section - changed Ambient Operating Temperature from 0°C to -40°C and throughout the datasheet. 3.3V Power Supply Table - changed V max. from 3.465V to V Added note. 3.3V/2.5V Power Supply Table - changed V max. from 3.465V to V Added note. 2.5V Power Supply Table - changed V max. from 3.465V to V Added note. Ordering Information Table - added lead-free note.	
С	T4D	4	LVCMOS DC Characteristics Table - defined 2.5V V pp v specs.	
D	T4B T4D T5A - T5C	3 3 4 5 - 6	Absolute Maximum Ratings - Inputs, V _I changed from -0.5V to V _{DD} + 0.5V to -0.5V to 5.0V. Mix Power Supply Table - corrected V _{DD} and V _{DDA} from 2.5V± to 3.3V±. LVCMOS DC Characteristics Table - V _{IH} rows - changed max. from V _{DD} + 0.3V to 5.0V. AC Tables - added ambient temperature note.	1/19/09
D	Т8	1 1 10	Removed ICS from the part number where needed. General Description - Deleted ICS Chip and HiPerClockS. Features Section - removed reference to leaded package. Ordering Information - removed quantity for tape and reel. Deleted LF note below the table. Updated header and footer.	1/21/16





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