1:2 LVCMOS/LVTTL-to-LVCMOS/LVTTL Zero Delay Buffer for Audio

ICS87002-05

DATA SHEET

General Description

The ICS87002-05 is a 1:2 LVCMOS/LVTTL low phase noise Zero Delay Buffer and is optimized for audio frequencies.

The device uses third generation FemtoClock® Technology for an optimum of high frequency and excellent phase jitter performance, combined with a low power consumption.

The device utilizes an internal feedback loop therefore eliminating the complexity of an external feedback loop.

The device utilizes a 3.3V supply and is packaged in a small, lead-free (RoHS 6) 8-lead SOIC package.

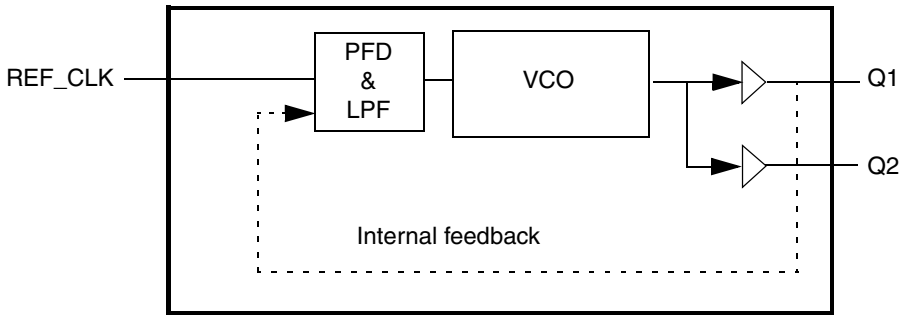
Features

- Third generation FemtoClock® technology
- Low phase noise zero delay buffer
- Low skew outputs
- One LVCMOS/LVTTL clock input
- Two LVCMOS/LVTTL outputs
- Phase noise: -125dBc/Hz @1kHz offset; -130dBc/Hz @100kHz offset
- Cycle-to-cycle jitter: 60ps (maximum)
- 0°C to 70°C ambient operating temperature
- Full 3.3V supply voltage

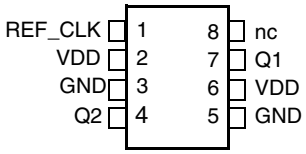
Supported Input Reference Clock Frequencies

REF_CLK Frequencies
11.2896MHz
12.288MHz
16.384MHz
16.9344MHz
18.432MHz
22.5792MHz
24.576MHz

Block Diagram



Pin Assignment



ICS87002-05
8-lead SOIC
3.8mm x 4.8mm x 1.47mm
M Package
Top View

Table 1. Pin Descriptions

Number	Name	Type	Description
1	REF_CLK	Input	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
2, 6	V_{DD}	Power	Power supply pin.
3, 5	GND	Power	Power supply ground.
4, 7	Q2, Q1	Output	Single-ended clock outputs. 15Ω typical output impedance. LVCMOS/LVTTL interface level.
8	nc	Unused	No connect.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DD} = 3.6V		8		pF
R_{OUT}	Output Impedance	V_{DD} = 3.3V ± 0.3V		15		Ω

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	96°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V±0.3V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current	No load			85	mA

.

Table 3B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V±0.3V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		(V_{DD}/2) + 1			V
V_{IL}	Input Low Voltage				(V_{DD}/2) - 1	V
I_{IH}	Input High Current	V_{DD} = 3.6V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.6V	-150			µA
V_{OH}	Output High Voltage	I_{OH} = -25mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 25mA			0.4	V

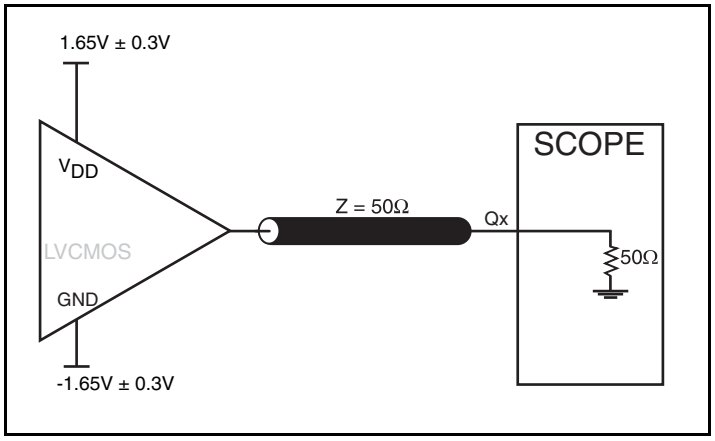
AC Characteristics

Table 4. AC Characteristics, V_{DD} = 3.3V±0.3V, T_A = 0°C to 70°C

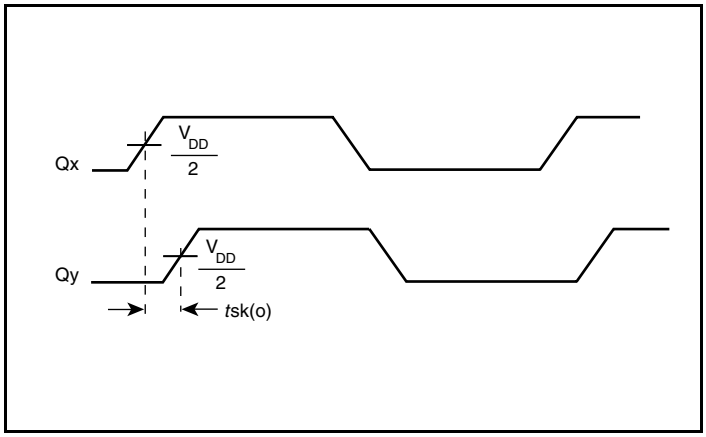
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency; NOTE 1		11.2783		24.6005	MHz
*t*sk(o)	Output Skew				20	ps
t_{PD}	Propagation Delay		200		1150	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	425		1450	ps
idc	Input Duty Cycle	f_{IN} = 24.576MHz	30		70	%
odc	Output Duty Cycle	At V_{DD}/2	48		52	%
*t*jit(cc)	Cycle-to-cycle Jitter, NOTE 2, 3				60	ps
*t*jit(per)	Period Jitter (pk-pk), NOTE 2, 3			50	75	ps
	Long Term Jitter, NOTE 4	N = 512 Cycles		100	300	ps
	Phase Noise, Relative to Carrier; NOTE 5	1kHz offset		-125		dBc/Hz
		100kHz offset		-130		dBc/Hz

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Device operation is guaranteed for the standard audio reference frequencies of 11.2896MHz, 12.288MHz, 16.384MHz, 16.9344MHz, 18.432MHz, 22.5792MHz and 24.576MHz. A variation of up to ±1000ppm in reference clock is acceptable at these frequencies.
NOTE 2: Measured at 22.5792MHz and 24.576MHz input clock.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Measured at 24.576MHz input clock and cycle N = 512.
NOTE 5: Measured at 24.576MHz input clock from 100Hz to 5MHz.

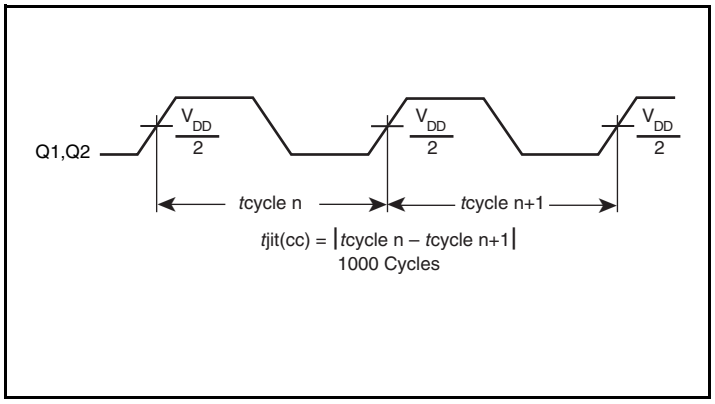
Parameter Measurement Information



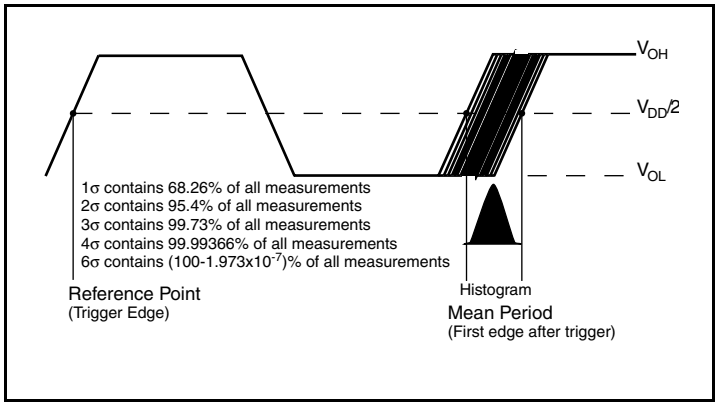
LVCMOS/LVTTL Output Load AC Test Circuit



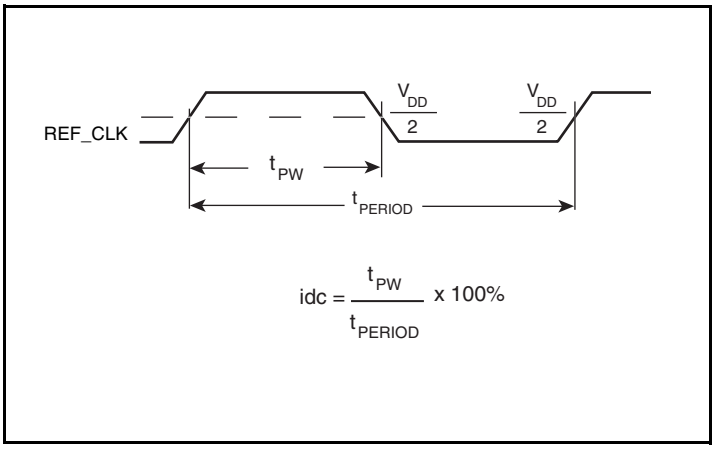
Output Skew



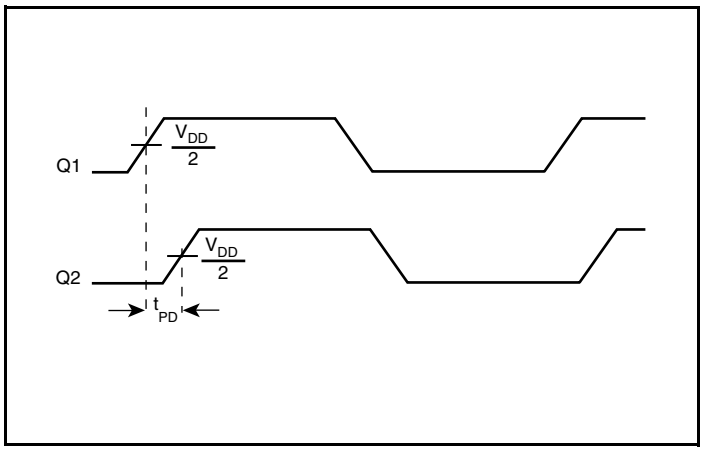
Cycle-to-Cycle Jitter



Period Jitter

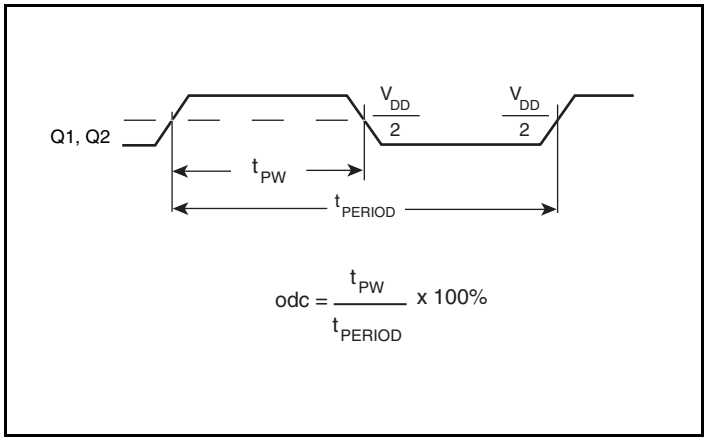


Input Duty Cycle

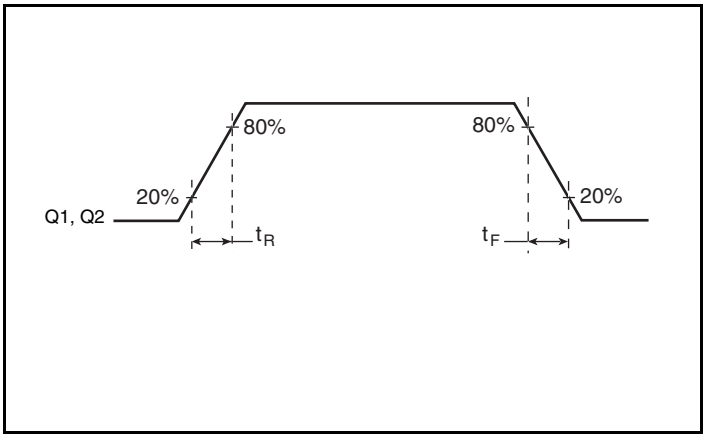


Propagation Delay

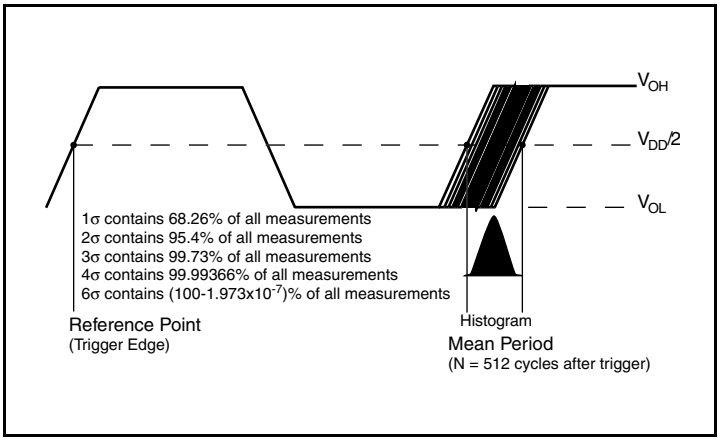
Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time



Long Term Jitter

Applications Information

Recommendations for Unused Output Pins

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Schematic Example

Figure 1 shows an example of ICS87002-05 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The input is driven by a 3.3V LVCMOS driver. One example of an LVCMOS termination is shown in this schematic. The decoupling capacitors should be located as close as possible to the power pin.

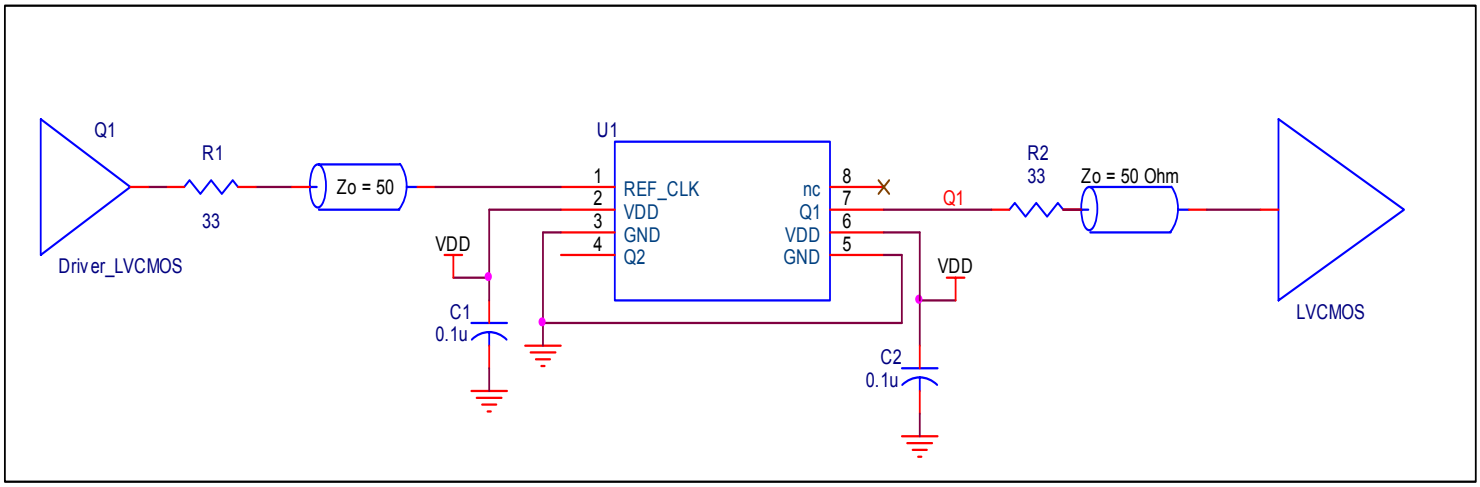


Figure 1. ICS87002-05 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS87002-05.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS87002-05 is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 0.3V = 3.6V, which gives worst case results.

Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD}$ = 3.6V *85mA = **306mW**

Total Static Power:

= Power $(core)_{MAX}$ = **306mW**

Dynamic Power Dissipation at F_{OUT_MAX} (24.576MHz)

Total Power $(F_{OUT\_MAX}) = [(C_{PD} * N) * Frequency * (V_{DDO})^2]$ = [(8pF *2) * 24.576MHz * $(3.6V)^2$] = **5.1mW per output**
N = number of outputs

Total Power

= Static Power + Dynamic Power Dissipation
= 306mW + 5.1mW
= 311mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 96°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.311W *96°C/W = 99.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 5. Thermal Resistance θ_{JA} for 8 Lead SOIC, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	96.0°C/W	87°C/W	82.0°C/W

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for an 8-lead SOIC

θ_{JA} vs. Air Flow			
Linear Feet per Minute			
Multi-Layer PCB, JEDEC Standard Test Boards	96°C/W	87°C/W	82°C/W

Transistor Count

The transistor count for ICS87002-05 is: 2267

Package Outline and Package Dimensions

Package Outline - M Suffix for 8 Lead SOIC

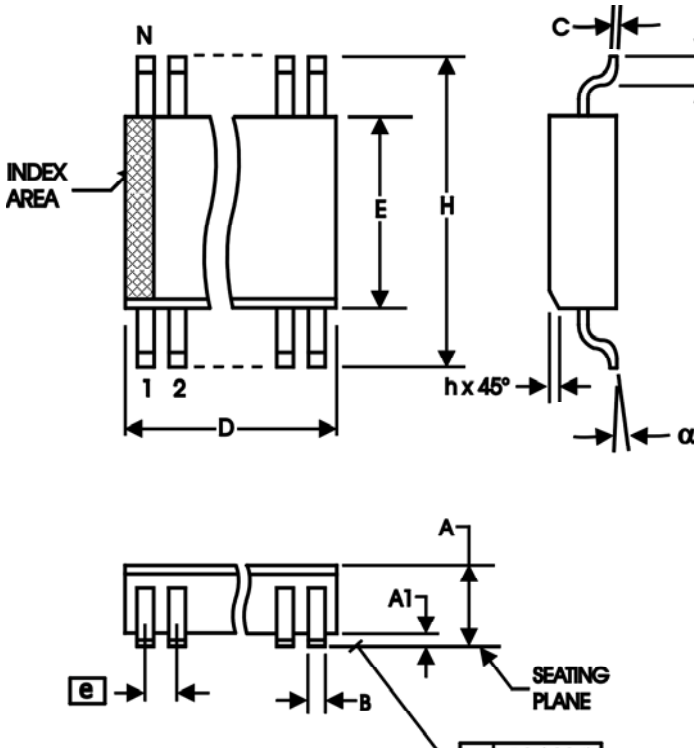


Table 7. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 Basic	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87002BM-05LF	P0003	Lead-Free, 8-lead SOIC	Tube	0°C to 70°C
87002BM-05LFT	P0003	Lead-Free, 8-lead SOIC	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	4	4	AC Characteristics Table - changed Min. and Max. f_{OUT} values. NOTE 1 - changed ±100pm to ±1000ppm.	4/16/10

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.