

### General Description

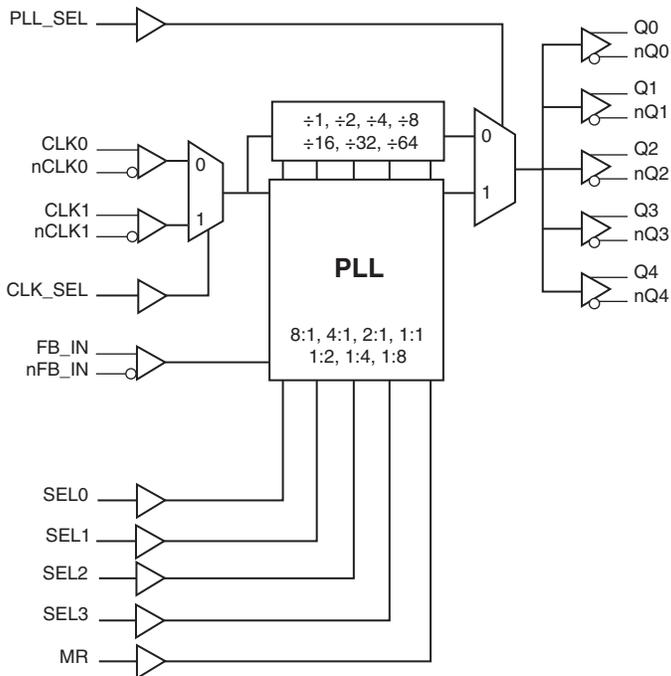


The ICS8725B-01 is a highly versatile 1:5 Differential-to-HSTL clock generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8725B-01 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider, and has an output frequency range of 31.25MHz to 700MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL\_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

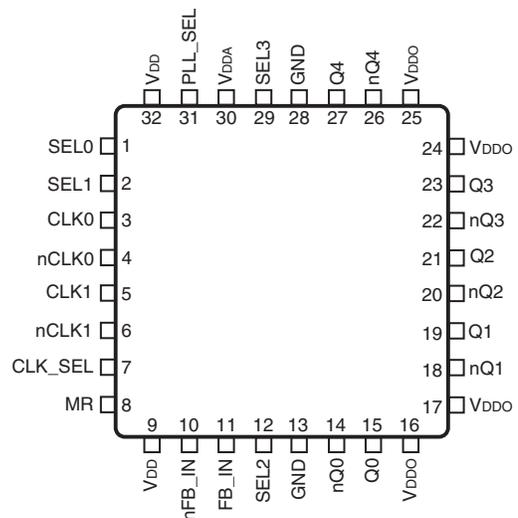
### Features

- Five differential HSTL output pairs
- Selectable differential CLKx/nCLKx input pairs
- CLKx/nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, HSTL, HCSSL, SSTL
- Output frequency range: 31.25MHz to 700MHz
- Input frequency range: 31.25MHz to 700MHz
- VCO range: 250MHz to 700MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Static phase offset: 15ps ± 135ps
- Cycle-to-cycle jitter: 25ps (maximum)
- Output skew: 45ps (maximum)
- 3.3V core, 1.8V output operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

### Block Diagram



### Pin Assignment



**ICS8725B-01**

**32-Lead LQFP**

**7mm x 7mm x 1.4mm package body**

**Y Package**

**Top View**

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 2, 12, 29	SEL0, SEL1, SEL2, SEL3	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTTL interface levels.
3	CLK0	Input	Pulldown	Non-inverting differential clock input.
4	nCLK0	Input	Pullup	Inverting differential clock input.
5	CLK1	Input	Pulldown	Non-inverting differential clock input.
6	nCLK1	Input	Pullup	Inverting differential clock input.
7	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1. When LOW, selects CLK0, nCLK0. LVCMOS/LVTTTL interface levels.
8	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels.
9, 32	V <sub>DD</sub>	Power		Core supply pins.
10	nFB_IN	Input	Pullup	Inverting differential feedback input to phase detector for regenerating clocks with "Zero Delay."
11	FB_IN	Input	Pulldown	Non-inverted differential feedback input to phase detector for regenerating clocks with "Zero Delay."
13, 28	GND	Power		Power supply ground.
14, 15	nQ0, Q0	Output		Differential output pair. HSTL interface levels.
16, 17, 24, 25	V <sub>DDO</sub>	Power		Output supply pins.
18, 19	nQ1, Q1	Output		Differential output pair. HSTL interface levels.
20, 21	nQ2, Q2	Output		Differential output pair. HSTL interface levels.
22, 23	nQ3, Q3	Output		Differential output pair. HSTL interface levels.
26, 27	nQ4, Q4	Output		Differential output pair. HSTL interface levels.
30	V <sub>DDA</sub>	Power		Analog supply pin.
31	PLL_SEL	Input	Pullup	PLL select. Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS/LVTTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			2		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Function Tables

Table 3A. Control Input Function Table

Inputs					Outputs PLL_SEL = 1 PLL Enable Mode
SEL3	SEL2	SEL1	SEL0	Reference Frequency Range (MHz)*	Q[0:4], nQ[0:4]
0	0	0	0	250 - 700	÷1
0	0	0	1	125 - 350	÷1
0	0	1	0	62.5 - 175	÷1
0	0	1	1	31.25 - 87.5	÷1
0	1	0	0	250 - 700	÷2
0	1	0	1	125 - 350	÷2
0	1	1	0	62.5 - 175	÷2
0	1	1	1	250 - 700	÷4
1	0	0	0	125 - 350	÷4
1	0	0	1	250 - 700	÷8
1	0	1	0	125 - 350	x2
1	0	1	1	62.5 - 175	x2
1	1	0	0	31.25 - 87.5	x2
1	1	0	1	62.5 - 175	x4
1	1	1	0	31.25 - 87.5	x4
1	1	1	1	31.25 - 87.5	x8

\*NOTE: VCO frequency range for all configurations above is 250MHz to 700MHz.

**Table 3B. PLL Bypass Function Table**

Inputs				Outputs PLL_SEL = 0 PLL Bypass Mode
SEL3	SEL2	SEL1	SEL0	Q[0:4], nQ[0:4]
0	0	0	0	÷4
0	0	0	1	÷4
0	0	1	0	÷4
0	0	1	1	÷8
0	1	0	0	÷8
0	1	0	1	÷8
0	1	1	0	÷16
0	1	1	1	÷16
1	0	0	0	÷32
1	0	0	1	÷64
1	0	1	0	÷2
1	0	1	1	÷2
1	1	0	0	÷4
1	1	0	1	÷1
1	1	1	0	÷2
1	1	1	1	÷1

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	47.9°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		1.6	1.8	2.0	V
$I_{DD}$	Power Supply Current				135	mA
$I_{DDA}$	Analog Supply Current				16	mA
$I_{DDO}$	Output Supply Current			0		mA

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	CLK_SEL, SEL[0:3], MR	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		PLL_SEL	$V_{DD} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	CLK_SEL, SEL[0:3], MR	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		PLL_SEL	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu A$

**Table 4C. Differential DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	FB_IN, CLK0, CLK1	$V_{DD} = V_{IN} = 3.465V$			150	$\mu A$
		nFB_IN, nCLK0, nCLK1	$V_{DD} = V_{IN} = 3.465V$			5	$\mu A$
$I_{IL}$	Input Low Current	FB_IN, CLK0, CLK1	$V_{DD} = 3.465V, V_{IN} = 0V$	-5			$\mu A$
		nFB_IN, nCLK0, nCLK1	$V_{DD} = 3.465V, V_{IN} = 0V$	-150			$\mu A$
$V_{PP}$	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2			0.5		$V_{DD} - 0.85$	V

NOTE 1:  $V_{IL}$  should not be less than  $-0.3V$ .

NOTE 2: Common mode input voltage is defined as  $V_{IH}$ .

**Table 4D. HSTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		1.0		1.4	V
$V_{OL}$	Output Low Voltage; NOTE 1		0		0.4	V
$V_{OX}$	Output Crossover Voltage; NOTE 2		40		60	%
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

NOTE 1: Outputs terminated with  $50\Omega$  to ground.

NOTE 2: Defined with respect to output voltage swing at a given condition.

**Table 5. Input Frequency Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$F_{IN}$	Input Frequency	CLK0, nCLK0, CLK1, nCLK1	PLL_SEL = 1	31.25		700	MHz
			PLL_SEL = 0			700	MHz

## AC Electrical Characteristics

**Table 6. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				700	MHz
$t_{PD}$	Propagation Delay; NOTE 1	PLL_SEL = 0V, $f \leq 700MHz$	3.2		4.4	ns
$t_{sk}(\emptyset)$	Static Phase Offset; NOTE 2, 5	PLL_SEL = 3.3V	-120	15	150	ps
$t_{sk}(o)$	Output Skew; NOTE 3, 5	PLL_SEL = 0V			45	ps
$f_{jit}(cc)$	Cycle-to-Cycle Jitter; NOTE 5, 6				25	ps
$f_{jit}(\theta)$	Phase Jitter; NOTE 4, 5, 6				$\pm 50$	ps
$t_L$	PLL Lock Time				1	ms
$t_R / t_F$	Output Rise/Fall Time	20% to 80% @ 50MHz	300		700	ps
$t_{PW}$	Output Pulse Width		$t_{PERIOD}/2 - 85$	$t_{PERIOD}/2$	$t_{PERIOD}/2 + 85$	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal across all conditions, when the PLL is locked and the input reference frequency is stable.

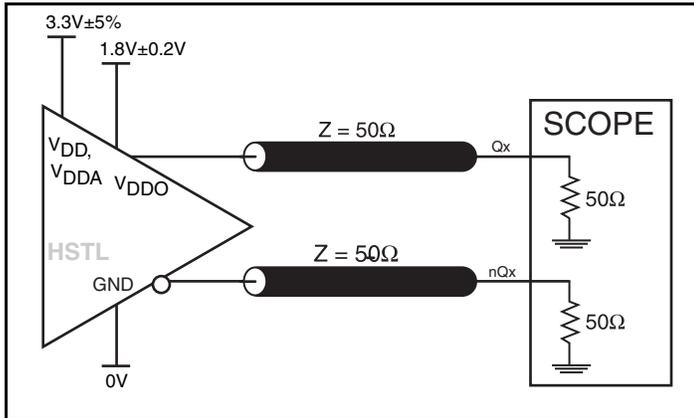
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 4: Phase jitter is dependent on the input source used.

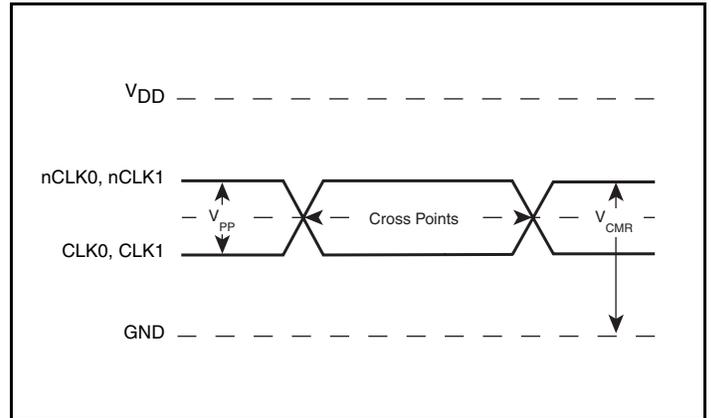
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Characterized at VCO frequency of 622MHz.

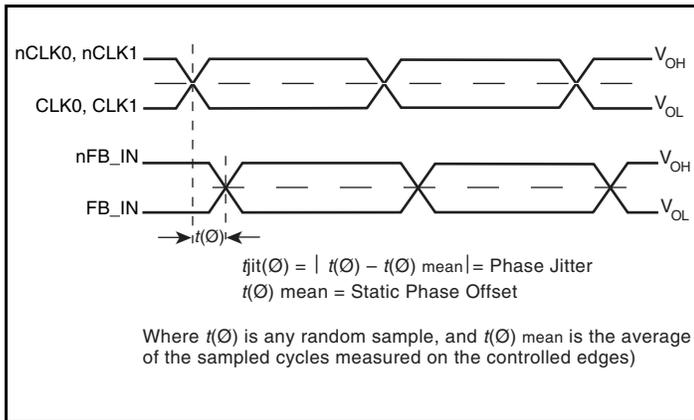
## Parameter Measurement Information



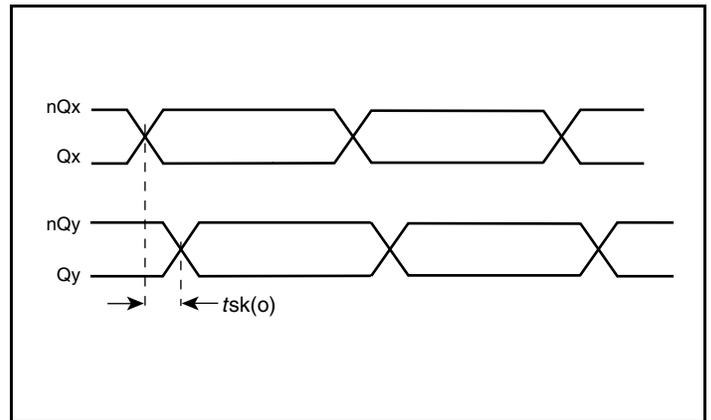
3.3V Core/1.8V Output Load AC Test Circuit



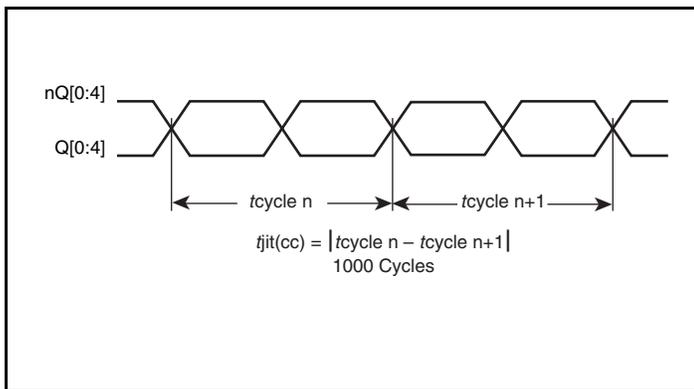
Differential Input Level



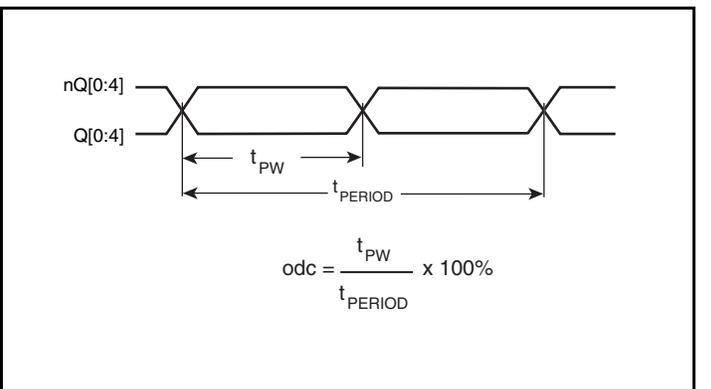
Phase Jitter and Static Phase Offset



Output Skew

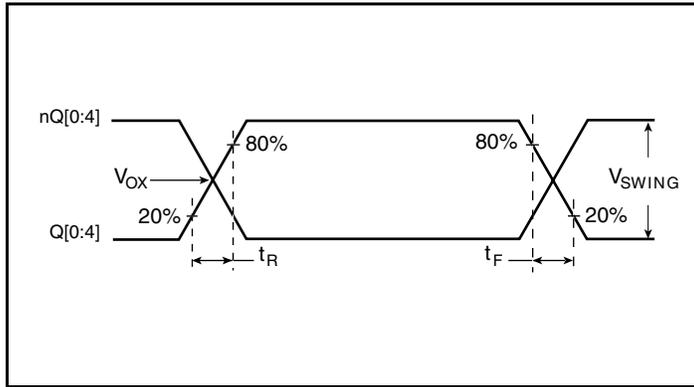


Cycle-to-Cycle Jitter

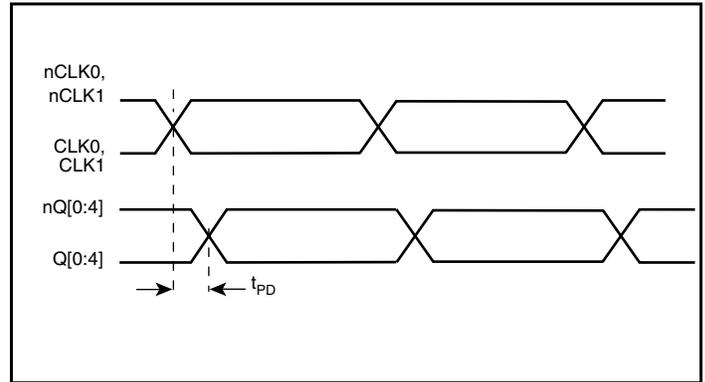


Output Duty Cycle/Pulse Width/Period

## Parameter Measurement Information, continued



Output Rise/Fall Time



Propagation Delay

## Application Information

### Power Supply Filtering Technique

To achieve optimum jitter performance, power supply isolation is required. To achieve optimum jitter performance, power supply isolation is required. The ICS8725B-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$  and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{DDA}$  pin. The  $10\Omega$  resistor can also be replaced by a ferrite bead.

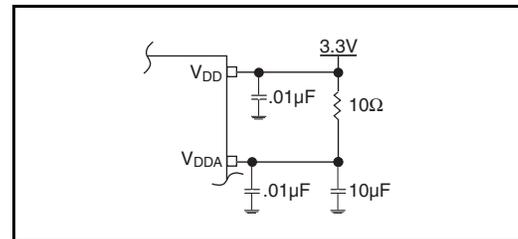


Figure 1. Power Supply Filtering

## Recommendations for Unused Input Pins

### Inputs:

#### LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

### Outputs:

#### HSTL OUTPUTS

All unused HSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

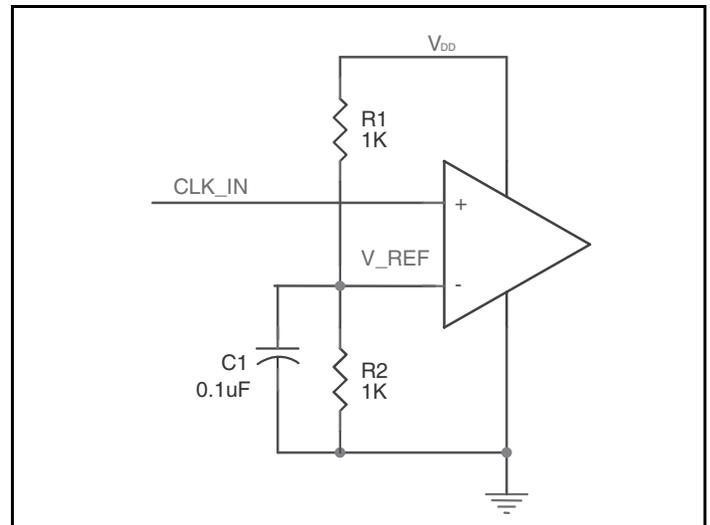
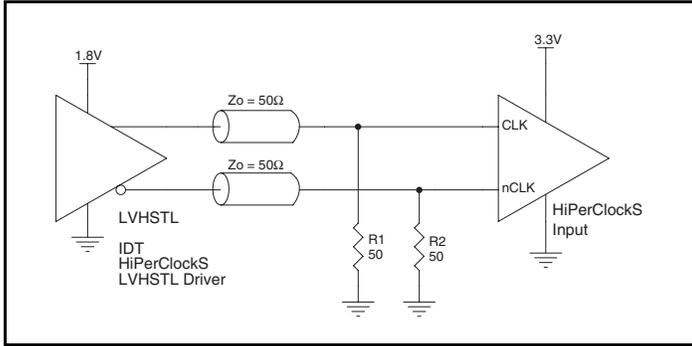


Figure 2. Single-Ended Signal Driving Differential Input

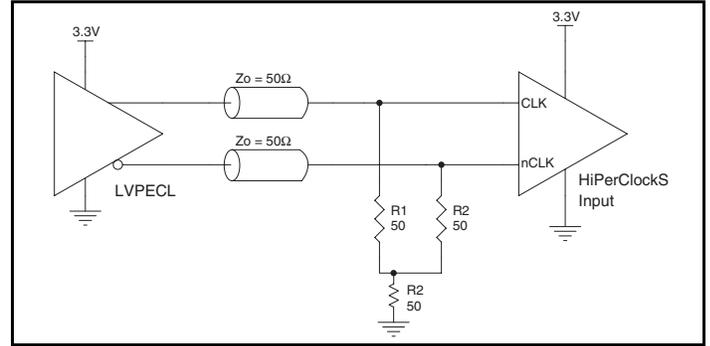
## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3F show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver

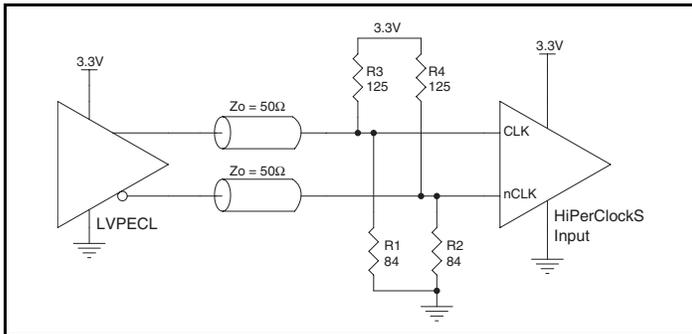
component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



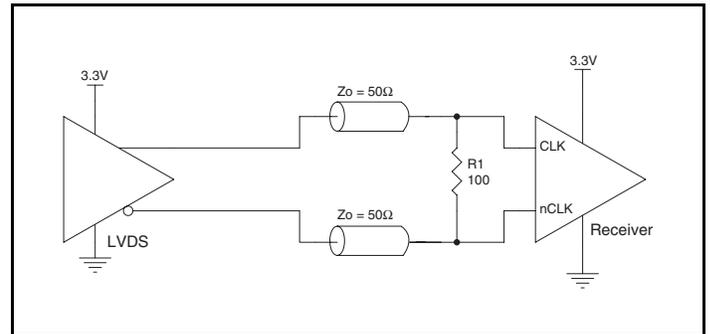
**Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver**



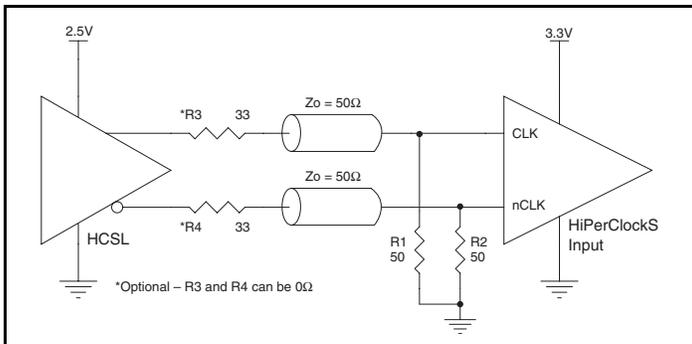
**Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



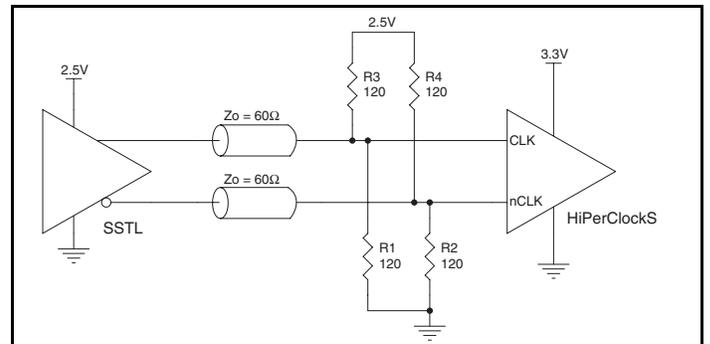
**Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver**



**Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver**



**Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver**

## Schematic Example

The schematic of the ICS8725B-01 layout example is shown in Figure 4A. The ICS8725B-01 recommended PCB board layout for this example is shown in Figure 4B. This layout example is used as a

general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stacking of the P.C. board.

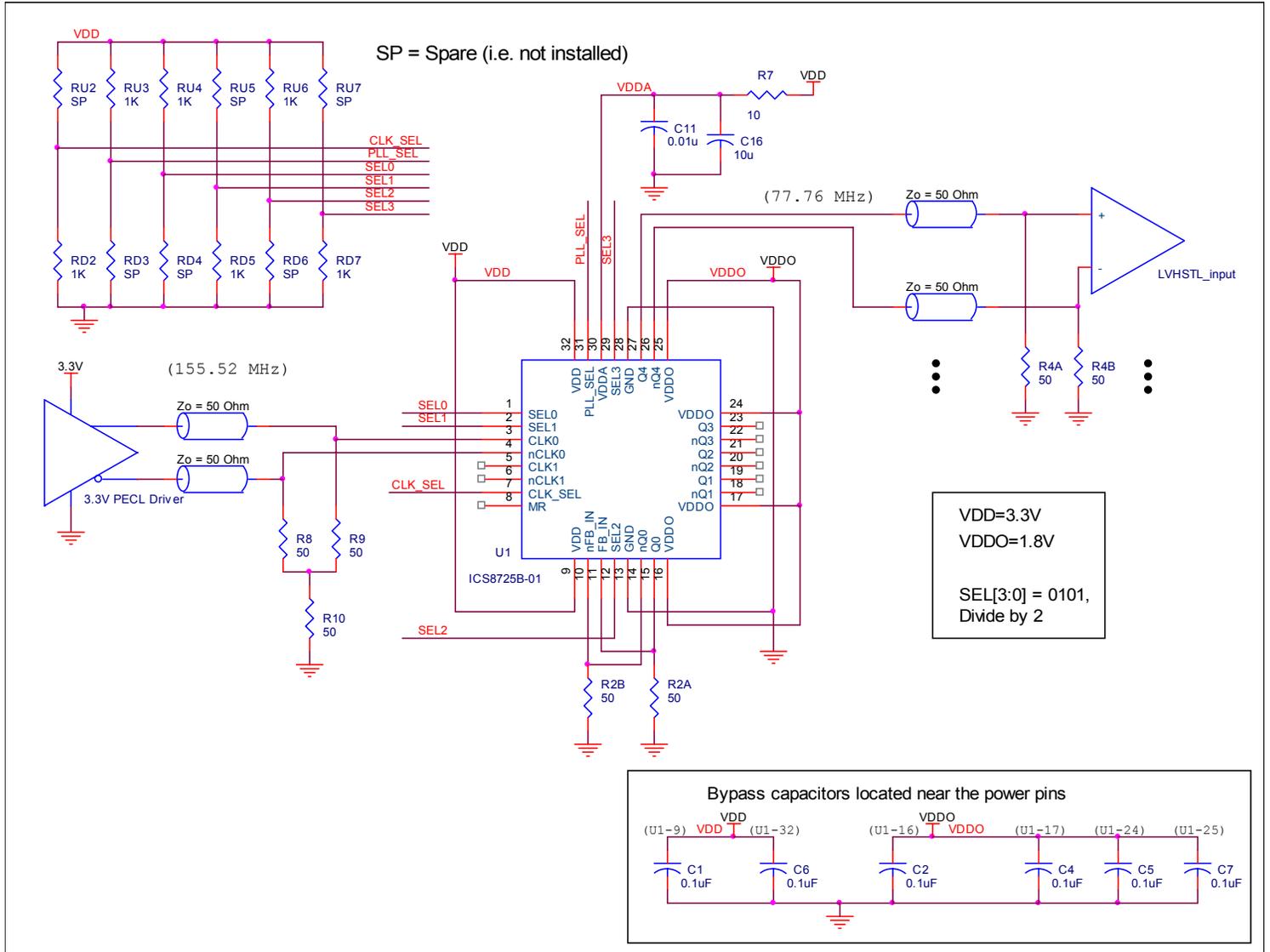


Figure 4. ICS8725B-01 HSTL Zero Delay Buffer Schematic Example

The following component footprints are used in this layout example: All the resistors and capacitors are size 0603.

**Power and Grounding**

Place the decoupling capacitors C1, C6, C2, C4, C5, and C7 as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V<sub>DDA</sub> pin as possible.

**Clock Traces and Termination**

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component

location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.

The matching termination resistors should be located as close to the receiver input pins as possible.

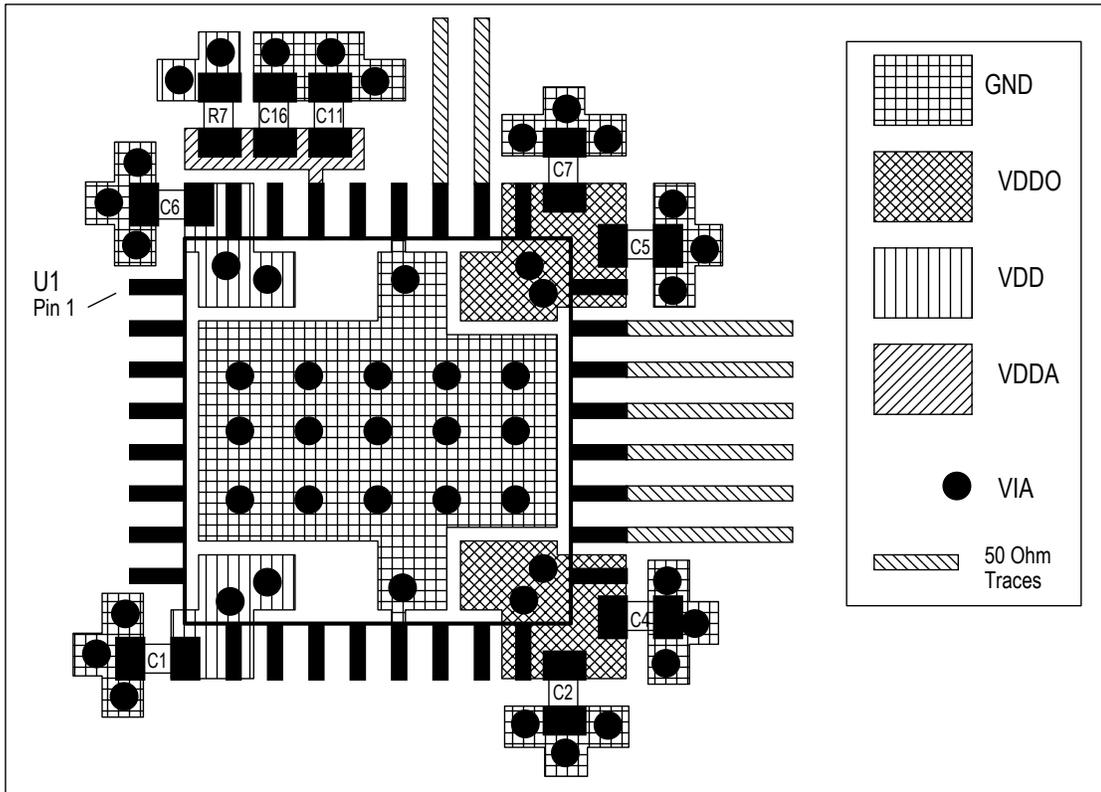


Figure 4B. PCB Board Layout for ICS8725B-01

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8725B-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8725B-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (135mA + 16mA) = 523.215mW$
- Power (outputs)<sub>MAX</sub> = **32.8mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $5 * 32.8mW = 164mW$

**Total Power<sub>MAX</sub>** (3.465V, with all outputs switching) =  $523.215mW + 164mW = 687.215mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 47.9°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.687\text{W} * 47.9^\circ\text{C}/\text{W} = 102.9^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance  $\theta_{JA}$  for 32 Lead LQFP, Forced Convection**

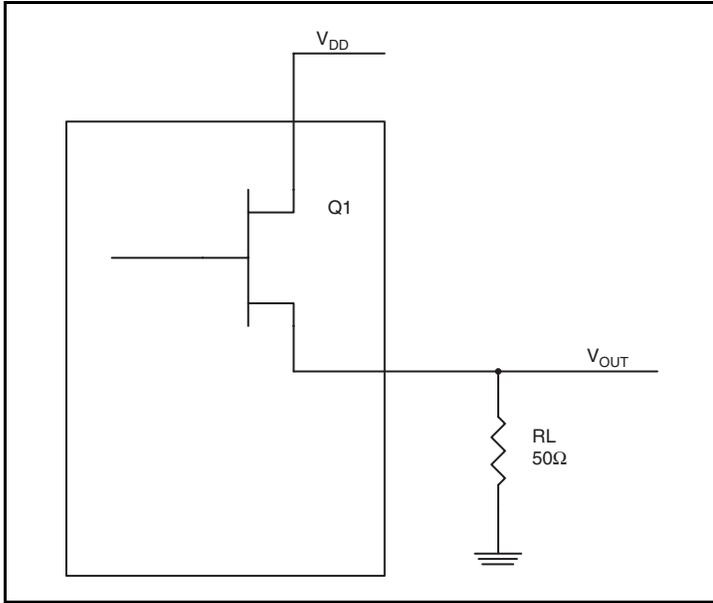
$\theta_{JA}$ vs. Air Flow			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 5*.



**Figure 5. HSTL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd\_H is power dissipation when the output drives high.

Pd\_L is the power dissipation when the output drives low.

$$Pd_H = (V_{OH\_MAX} / R_L) * (V_{DDO\_MAX} - V_{OH\_MAX})$$

$$Pd_L = (V_{OL\_MAX} / R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$$

$$Pd_H = (1.0V / 50\Omega) * (2V - 1.0V) = \mathbf{20mW}$$

$$Pd_L = (0.4V / 50\Omega) * (2V - 0.4V) = \mathbf{12.8mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{32.8mW}$$

## Reliability Information

**Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 32 Lead LQFP**

$\theta_{JA}$ vs. Air Flow			
Linear Feet per Minute	<b>0</b>	<b>200</b>	<b>500</b>
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

## Transistor Count

The transistor count for ICS8725B-01 is: 2969

## Package Outline and Dimensions

### Package Outline - Y Suffix for 32 Lead LQFP

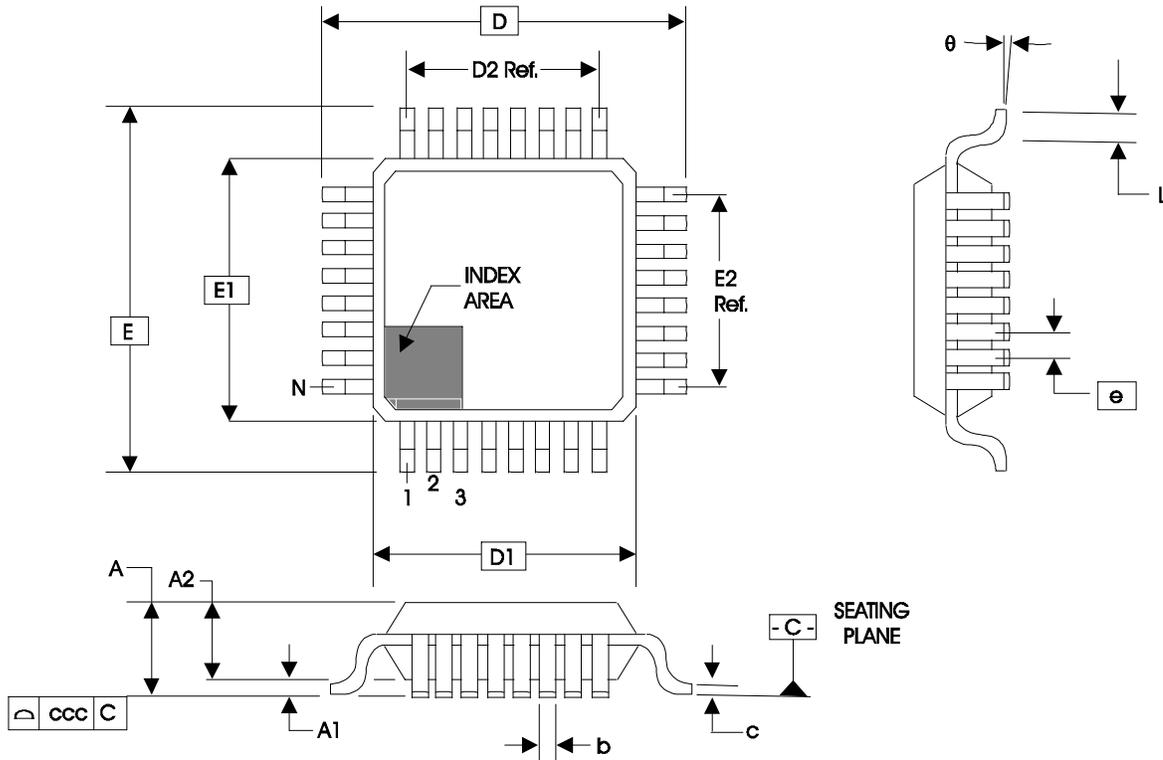


Table 9. Package Dimensions for 32 Lead LQFP

JEDEC Variation: BBA			
All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N	32		
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E	9.00 Basic		
D1 & E1	7.00 Basic		
D2 & E2	5.60 Ref.		
e	0.80 Basic		
L	0.45	0.60	0.75
$\theta$	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

## Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8725BY-01	ICS8725BY-01	32 Lead LQFP	Tray	0°C to 70°C
8725BY-01T	ICS8725BY-01	32 Lead LQFP	1000 Tape & Reel	0°C to 70°C
8725BY-01LF	ICS8725BY01L	“Lead-Free” 32 Lead LQFP	Tray	0°C to 70°C
8725BY-01LFT	ICS8725BY01L	“Lead-Free” 32 Lead LQFP	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).