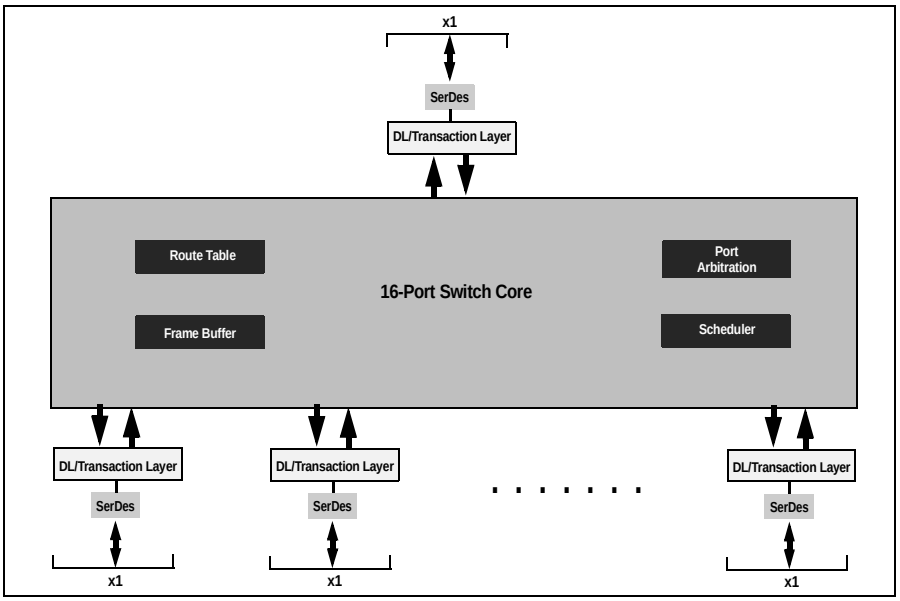
Device Overview

The 89HPES16H16 is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES16H16 is a 16-lane, 16-port peripheral chip that performs PCI Express packet switching with a feature set optimized for high-performance applications such as servers, storage, and communications/networking. It provides connectivity and switching functions between a PCI Express upstream port and up to fifteen downstream ports and supports switching between downstream ports.

Features

- **High Performance PCI Express Switch**
  - *Sixteen maximum switch ports*
    - Sixteen x1 ports
  - *Sixteen 2.5 Gbps embedded SerDes*
    - Supports pre-emphasis and receive equalization on per-port basis
  - *Delivers 64 Gbps (8 GBps) of aggregate switching capacity*
  - *Low-latency cut-through switch architecture*
  - *Support for Max Payload Size up to 2048 bytes*
  - *Supports two virtual channels and eight traffic classes*
  - *PCI Express Base Specification Revision 1.1 compliant*
- **Flexible Architecture with Numerous Configuration Options**
  - *Port arbitration schemes utilizing round robin algorithms*
  - *Virtual channels arbitration based on priority*
  - *Automatic polarity inversion on all lanes*
  - *Supports locked transactions, allowing use with legacy software*
  - *Ability to load device configuration from serial EEPROM*
  - *Ability to control device via SMBus*
- **Highly Integrated Solution**
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates sixteen 2.5 Gbps embedded full duplex SerDes, 8B/10B encoder/decoder (no separate transceivers needed)*
- **Reliability, Availability, and Serviceability (RAS) Features**
  - *Redundant upstream port failover capability*
  - *Supports optional PCI Express end-to-end CRC checking*
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports optional PCI Express Advanced Error Reporting*

Block Diagram



16 PCI Express Lanes
16 x1 Ports

Figure 1 Internal Block Diagram

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  - *Supports PCI Express Hot-Plug*
    - *Compatible with Hot-Plug I/O expanders used on PC motherboards*
  - *Supports Hot-Swap*
- **Power Management**
  - *Supports PCI Power Management Interface specification, Revision 1.1 (PCI-PM)*
    - Supports powerdown modes at the link level (L0, L0s, L1, L2/L3 Ready and L3) and at the device level (D0, $D3_{hot}$)
  - *Unused SerDes disabled*
- **Testability and Debug Features**
  - *Built in SerDes Pseudo-Random Bit Stream (PRBS) generator*
  - *Ability to read and write any internal register via the SMBus*
  - *Ability to bypass link training and force any link into any mode*
  - *Provides statistics and performance counters*
- **Thirty-two General Purpose Input/Output pins**
  - *Each pin may be individually configured as an input or output*
  - *Each pin may be individually configured as an interrupt input*
  - *Some pins have selectable alternate functions*
- **Packaged in a 23mm x 23mm 484-ball Flip Chip BGA with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect, the PES16H16 provides the most efficient I/O connectivity for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 64 Gbps of aggregated, full-duplex switching capacity through 16 integrated serial lanes, using proven and robust IDT technology. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.1.

The PES16H16 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers. The PES16H16 can operate either as a store and forward switch or a cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and two Virtual Channels (VCs) with sophisticated resource management to enable efficient switching and I/O connectivity.

SMBus Interface

The PES16H16 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES16H16, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES16H16 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 3, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 3(a), the master and slave SMBuses are tied together and the PES16H16 acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES16H16 registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES16H16 may be configured to operate in a split configuration as shown in Figure 3(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES16H16 supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

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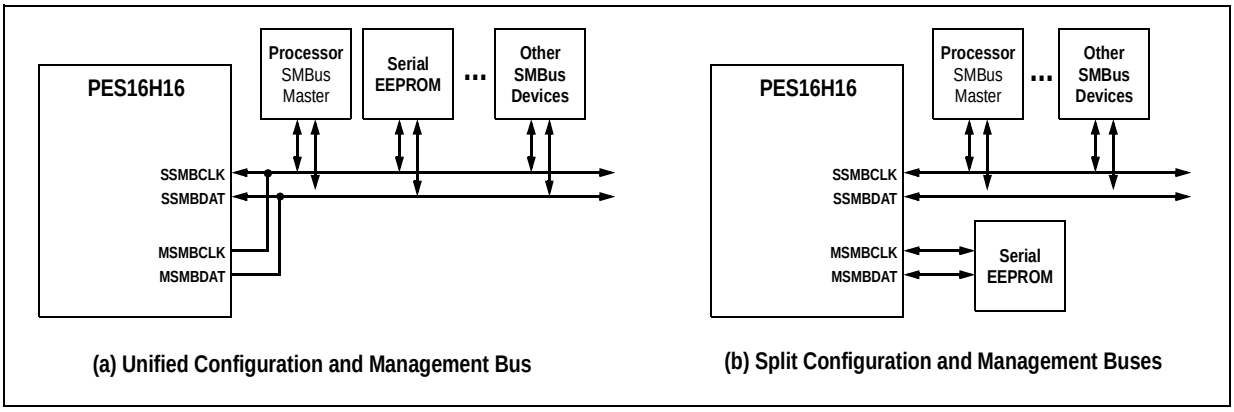

Figure 3 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES16H16 supports PCI Express Hot-Plug on each downstream port (ports 1 through 15). To reduce the number of pins required on the device, the PES16H16 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES16H16 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES16H16. In response to an I/O expander interrupt, the PES16H16 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES16H16 provides 32 General Purpose I/O (GPIO) pins that may be individually configured as general purpose inputs, general purpose outputs, or alternate functions. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables lists the functions of the pins provided on the PES16H16. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level. Differential signals end with a suffix “N” or “P.” The differential signal ending in “P” is the positive portion of the differential pair and the differential signal ending in “N” is the negative portion of the differential pair.

Signal	Type	Name/Description
PE0RP[0] PE0RN[0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pair for port 0. Port 0 is the upstream port.
PE0TP[0] PE0TN[0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pair for port 0. Port 0 is the upstream port.
PE1RP[0] PE1RN[0]	I	**PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pair for port 1.
PE1TP[0] PE1TN[0]	O	**PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pair for port 1.
PE2RP[0] PE2RN[0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pair for port 2.
PE2TP[0] PE2TN[0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pair for port 2.

Table 2 PCI Express Interface Pins (Part 1 of 3)

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Signal	Type	Name/Description
PE3RP[0] PE3RN[0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pair for port 3.
PE3TP[0] PE3TN[0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pair for port 3.
PE4RP[0] PE4RN[0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pair for port 4.
PE4TP[0] PE4TN[0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pair for port 4.
PE5RP[0] PE5RN[0]	I	**PCI Express Port 5 Serial Data Receive.** Differential PCI Express receive pair for port 5.
PE5TP[0] PE5TN[0]	O	**PCI Express Port 5 Serial Data Transmit.** Differential PCI Express transmit pair for port 5.
PE6RP[0] PE6RN[0]	I	**PCI Express Port 6 Serial Data Receive.** Differential PCI Express receive pair for port 6.
PE6TP[0] PE6TN[0]	O	**PCI Express Port 6 Serial Data Transmit.** Differential PCI Express transmit pair for port 6.
PE7RP[0] PE7RN[0]	I	**PCI Express Port 7 Serial Data Receive.** Differential PCI Express receive pair for port 7.
PE7TP[0] PE7TN[0]	O	**PCI Express Port 7 Serial Data Transmit.** Differential PCI Express transmit pair for port 7.
PE8RP[0] PE8RN[0]	I	**PCI Express Port 8 Serial Data Receive.** Differential PCI Express receive pair for port 8.
PE8TP[0] PE8TN[0]	O	**PCI Express Port 8 Serial Data Transmit.** Differential PCI Express transmit pair for port 8.
PE9RP[0] PE9RN[0]	I	**PCI Express Port 9 Serial Data Receive.** Differential PCI Express receive pair for port 9.
PE9TP[[0] PE9TN[0]	O	**PCI Express Port 9 Serial Data Transmit.** Differential PCI Express transmit pair for port 9.
PE10RP[0] PE10RN[0]	I	**PCI Express Port 10 Serial Data Receive.** Differential PCI Express receive pair for port 10.
PE10TP[0] PE10TN[0]	O	**PCI Express Port 10 Serial Data Transmit.** Differential PCI Express transmit pair for port 10.
PE11RP[0] PE11RN[0]	I	**PCI Express Port 11 Serial Data Receive.** Differential PCI Express receive pair for port 11.
PE11TP[0] PE11TN[0]	O	**PCI Express Port 11 Serial Data Transmit.** Differential PCI Express transmit pair for port 11.
PE12RP[0] PE12RN[0]	I	**PCI Express Port 12 Serial Data Receive.** Differential PCI Express receive pair for port 12.
PE12TP[0] PE12TN[0]	O	**PCI Express Port 12 Serial Data Transmit.** Differential PCI Express transmit pair for port 12.
PE13RP[0] PE13RN[0]	I	**PCI Express Port 13 Serial Data Receive.** Differential PCI Express receive pair for port 13.
PE13TP[0] PE13TN[0]	O	**PCI Express Port 13 Serial Data Transmit.** Differential PCI Express transmit pair for port 13. W

Table 2 PCI Express Interface Pins (Part 2 of 3)

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Signal	Type	Name/Description
PE14RP[0] PE14RN[0]	I	**PCI Express Port 14 Serial Data Receive.** Differential PCI Express receive pair for port 14.
PE14TP[0] PE14TN[0]	O	**PCI Express Port 14 Serial Data Transmit.** Differential PCI Express transmit pair for port 14.
PE15RP[0] PE15RN[0]	I	**PCI Express Port 15 Serial Data Receive.** Differential PCI Express receive pair for port 15.
PE15TP[0] PE15TN[0]	O	**PCI Express Port 15 Serial Data Transmit.** Differential PCI Express transmit pair for port 15.
REFCLKM	I	**PCI Express Reference Clock Mode Select.** This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz
PEREFCLKP[3:0] PEREFCLKN[3:0]	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.

Table 2 PCI Express Interface Pins (Part 3 of 3)

Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.

Table 4 General Purpose I/O Pins (Part 1 of 4)

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Signal	Type	Name/Description
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P1RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 1
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2
GPIO[8]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P3RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 3
GPIO[9]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4
GPIO[10]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P5RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 5
GPIO[11]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P6RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 6
GPIO[12]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P7RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 7
GPIO[13]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P8RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 8

Table 4 General Purpose I/O Pins (Part 2 of 4)

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Signal	Type	Name/Description
GPIO[14]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P9RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 9
GPIO[15]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P10RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 10
GPIO[16]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P11RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 11
GPIO[17]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P12RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 12
GPIO[18]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P13RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 13
GPIO[19]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P14RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 14
GPIO[20]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P15RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 15
GPIO[21]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 0
GPIO[22][1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN1 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 1
GPIO[23]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 2

Table 4 General Purpose I/O Pins (Part 3 of 4)

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Signal	Type	Name/Description
GPIO[24]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN3 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 3
GPIO[25][1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN4 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 4
GPIO[26]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN5 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 5
GPIO[27]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN6 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 6
GPIO[28]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN7 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 7
GPIO[29]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[30]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[31]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN10 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 10

Table 4 General Purpose I/O Pins (Part 4 of 4)

1. GPIO pins 22 and 25 are not available in the 23x23mm package.

Signal	Type	Name/Description
CCLKDS	I	**Common Clock Downstream.** When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port.
CCLKUS	I	**Common Clock Upstream.** When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port.
MSMBSMODE	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.

Table 5 System Pins (Part 1 of 2)

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Signal	Type	Name/Description
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside the PES16H16 and initiates a PCI Express fundamental reset.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, the PES16H16 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register by an SMBus master.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the PES16H16 switch operating mode. These pins should be static and not change following the negation of PERSTN. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 through 0x7 - Reserved 0x8 - Normal switch mode with upstream port failover (port 0 selected as the upstream port) 0x9 - Normal switch mode with upstream port failover (port 2 selected as the upstream port) 0xA - Normal switch mode with Serial EEPROM initialization and upstream port failover (port 0 selected as the upstream port) 0xB - Normal switch mode with Serial EEPROM initialization and upstream port failover (port 2 selected as the upstream port) 0xC through 0xF - Reserved

Table 5 System Pins (Part 2 of 2)

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins

Signal	Type	Name/Description
V_{DD}CORE	I	**Core VDD.** Power supply for core logic.
V_{DD}I/O	I	**I/O VDD.** LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power.** PCI Express digital power used by the digital power of the SerDes.

Table 7 Power and Ground Pins

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Signal	Type	Name/Description
$V_{DD}PEA$	I	**PCI Express Analog Power.** PCI Express analog power used by the PLL and bias generator.
V_{SS}	I	Ground.
$V_{TT}PE$		**PCI Express Serial Data Transmit Termination Voltage.** This pin allows the driver termination voltage to be set, enabling the system designer to control the Common Mode Voltage and output voltage swing of the corresponding PCI Serial Data Transmit differential pair.

Table 7 Power and Ground Pins

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Pin Characteristics

Note: Some input pads of the PES16H16 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
PCI Express Interface	PE0RN[0]	I	CML	Serial Link		
	PE0RP[0]	I				
	PE0TN[0]	O				
	PE0TP[0]	O				
	PE1RN[0]	I				
	PE1RP[0]	I				
	PE1TN[0]	O				
	PE1TP[0]	O				
	PE2RN[0]	I				
	PE2RP[0]	I				
	PE2TN[0]	O				
	PE2TP[0]	O				
	PE3RN[0]	I				
	PE3RP[0]	I				
	PE3TN[0]	O				
	PE3TP[0]	O				
	PE4RN[0]	I				
	PE4RP[0]	I				
	PE4TN[0]	O				
	PE4TP[0]	O				
	PE5RN[0]	I				
	PE5RP[0]	I				
	PE5TN[0]	O				
	PE5TP[0]	O				
	PE6RN[0]	I				
	PE6RP[0]	I				
	PE6TN[0]	O				
	PE6TP[0]	O				
	PE7RN[0]	I				
	PE7RP[0]	I				
	PE7TN[0]	O				
	PE7TP[0]	O				
	PE8RN[0]	I				

Table 8 Pin Characteristics (Part 1 of 3)

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Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
PCI Express Interface (cont.)	PE8RP[0]	I	CML	Serial Link		
	PE8TN[0]	O				
	PE8TP[0]	O				
	PE9RN[0]	I				
	PE9RP[0]	I				
	PE9TN[0]	O				
	PE9TP[0]	O				
	PE10RN[0]	I				
	PE10RP[0]	I				
	PE10TN[0]	O				
	PE10TP[0]	O				
	PE11RN[0]	I				
	PE11RP[0]	I				
	PE11TN[0]	O				
	PE11TP[0]	O				
	PE12RN[0]	I				
	PE12RP[0]	I				
	PE12TN[0]	O				
	PE12TP[0]	O				
	PE13RN[0]	I				
	PE13RP[0]	I				
	PE13TN[0]	O				
	PE13TP[0]	O				
	PE14RN[0]	I				
	PE14RP[0]	I				
	PE14TN[0]	O				
	PE14TP[0]	O				
	PE15RN[0]	I				
	PE15RP[0]	I				
	PE15TN[0]	O				
	PE15TP[0]	O				
	PEREFCLKN[3:0]	I	LVPECL/ CML	Diff. Clock Input		Refer to Table 9
	PEREFCLKP[3:0]	I				
	REFCLKM	I	LVTTL	Input	pull-down	

Table 8 Pin Characteristics (Part 2 of 3)

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Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
SMBus	MSMBADDR[4:1]	I	LVTTL		pull-up	
	MSMBCLK	I/O		STI[1]		
	MSMBDAT	I/O		STI		
	SSMBADDR[5,3:1]	I			pull-up	
	SSMBCLK	I/O		STI		
	SSMBDAT	I/O		STI		
General Purpose I/O	GPIO[31:0]	I/O	LVTTL		pull-up	
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	PERSTN	I				
	RSTHALT	I			pull-down	
	SWMODE[3:0]	I			pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	External pull-down

Table 8 Pin Characteristics (Part 3 of 3)

1. Schmitt Trigger Input (STI).

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Logic Diagram — PES16H16

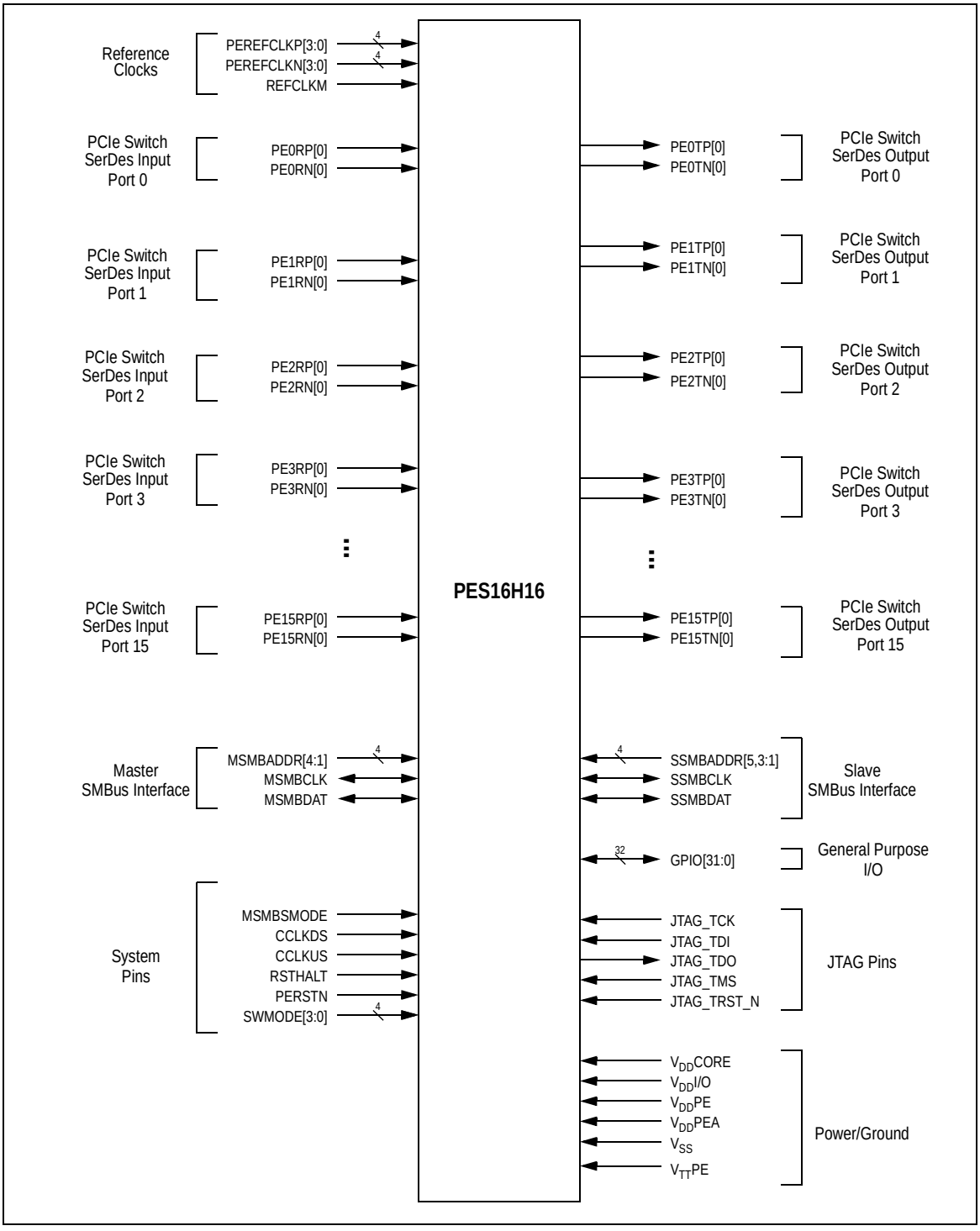

Figure 4 PES16H16 Logic Diagram

Note: GPIO pins 22 and 25 are not available in the 23x23mm package.

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System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 15.

Parameter	Description	Min	Typical	Max	Unit
PEREFCLK					
$Refclk_{FREQ}$	Input reference clock frequency range	100		125[1]	MHz
$Refclk_{DC}$[2]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[3]
V_{SW}	Differential input voltage swing[4]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps
R_T	Termination Resistor		110		Ohms

Table 9 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.
2. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
4. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
PCIe Transmit					
UI	Unit Interval	399.88	400	400.12	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.7	.9		UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+ / D- Tx output rise/fall time	50	90		ps
$T_{TX- IDLE-MIN}$	Minimum time in idle	50			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			20	UI
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
PCIe Receive					
UI	Unit Interval	399.88	400	400.12	ps
$T_{RX-EYE (with jitter)}$	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI
$T_{RX-EYE-MEDIUM TO MAX JITTER}$	Max time between jitter median & max deviation			0.3	UI
$T_{RX-IDLE-DET-DIFF-ENTER TIME}$	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
$T_{RX-SKEW}$	Lane to lane input skew			20	ns

Table 10 PCIe AC Timing Characteristics

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1

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Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[31:0][1]	Tpw_13b[2]	None	50	—	ns	See Figure 5.

Table 11 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.
2. The values for this symbol were determined by calculation, not by testing.

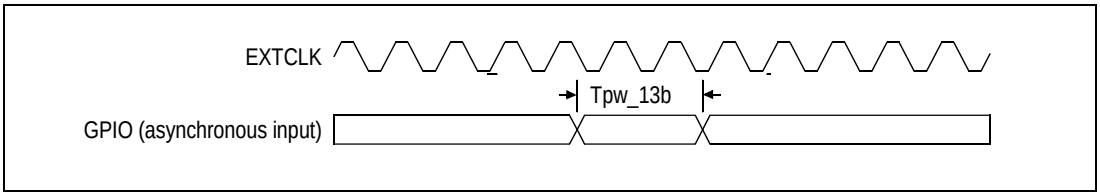

Figure 5 GPIO AC Timing Waveform

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 6.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.
2. The values for this symbol were determined by calculation, not by testing.

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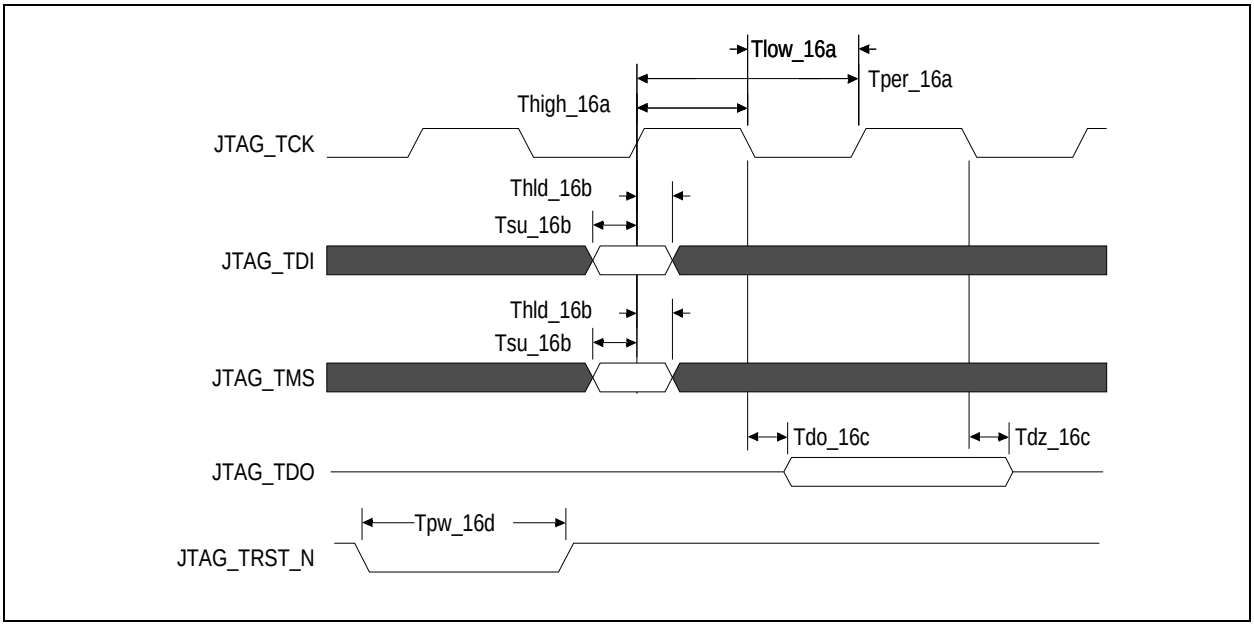

Figure 6 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.0	3.3	3.6	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}PEA	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES16H16 Operating Voltages

Absolute Maximum Voltage Rating

V_{DD}Core	V_{DD}PE	V_{DD}APE	V_{TT}PE	V_{DD}I/O
1.5V	1.5V	1.5V	2.5V	5.0V

Table 14 PES16H16 Absolute Maximum Voltage Rating

Warning: For proper and reliable operation in adherence with this data sheet, the device should not exceed the recommended operating voltages in Table 13. The absolute maximum operating voltages in Table 14 are offered to provide guidelines for voltage excursions outside the recommended voltage ranges. Device functionality is not guaranteed at these conditions and sustained operation at these values or any exposure to voltages outside the maximum range may adversely affect device functionality and reliability.

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Power-Up Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES16H16, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}PEA — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels. The power-down sequence must be in the reverse order of the power-up sequence.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 15 PES16H16 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Digital Supply		PCIe Analog Supply		PCIe Termination Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.5V	Max 1.575V	Typ 3.3V	Max 3.6V	Typ Power	Max Power
Sixteen x1	**mA**	2320	2880	723	867.5	1157	1500	370.5	500	5	5		
	Watts	2.32	3.17	0.72	0.95	1.16	1.65	0.56	0.79	0.017	0.018	4.77	6.58

Table 16 PES16H16 Power Consumption

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Thermal Considerations

This section describes thermal considerations for the PES16H16 ($23mm^2$ FCBGA484 package). The data in Table 17 below contains information that is relevant to the thermal performance of the PES16H16 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	^{0}C	Maximum
$T_{A(max)}$	Ambient Temperature	70	^{0}C	Maximum for commercial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	13.4	^{0}C/W	Zero air flow
		7.2	^{0}C/W	1 m/S air flow
		6.2	^{0}C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	2.5	^{0}C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.1	^{0}C/W	
P	Power Dissipation of the Device	6.58	Watts	Maximum

Table 17 Thermal Specifications for PES16H16, 23x23mm FCBGA484 Package

Note: The parameter $\theta_{JA(eff)}$ is not the *absolute* thermal resistance for the package as defined by JEDEC (JESD-51). Because resistance can vary with the number of board layers, size of the board, and airflow, $\theta_{JA(eff)}$ is the *effective* thermal resistance. The values for effective θ_{JA} given above are based on a 10-layer, standard height, full length (4.3"x12.2") PCIe add-in card.

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DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	**PCIe Transmit**						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	
	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
	PCIe Receive						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	

Table 18 DC Electrical Characteristics (Part 1 of 2)

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I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	V_{DD}I/O (max)

Table 18 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.0a.

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Option A Package — 484-BGA Signal Pinout for PES16H16

The following table lists the pin numbers and signal names for the PES16H16 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{DD}I/O		B13	V_{SS}		D3	GPIO_27		E15	V_{SS}	
A2	GPIO_16		B14	NC		D4	GPIO_23		E16	V_{DD}PE	
A3	V_{SS}		B15	NC		D5	GPIO_20		E17	V_{DD}PE	
A4	PE9TN00		B16	V_{SS}		D6	V_{SS}		E18	JTAG_TRST_N	
A5	PE8TN00		B17	NC		D7	PE9RP00		E19	SSMBCLK	
A6	V_{SS}		B18	PE2TN00		D8	PE9RN00		E20	SSMBADDR_2	
A7	PE3RP00		B19	MSMBADDR_3		D9	PE8RP00		E21	PE1TP00	
A8	NC		B20	JTAG_TDO		D10	PE8RN00		E22	PE1TN00	
A9	V_{SS}		B21	PERSTN		D11	V_{SS}		F1	PE10RP00	
A10	PEREFCLKN1		B22	JTAG_TDI		D12	NC		F2	PE10RN00	
A11	V_{SS}		C1	V_{DD}I/O		D13	NC		F3	V_{SS}	
A12	PE3TN00		C2	GPIO_21		D14	NC		F4	GPIO_30	
A13	V_{SS}		C3	GPIO_19		D15	NC		F5	V_{DD}I/O	
A14	NC		C4	V_{SS}		D16	PE2RP00		F6	V_{DD}I/O	
A15	NC		C5	V_{SS}		D17	PE2RN00		F7	V_{DD}PE	
A16	V_{SS}		C6	V_{SS}		D18	MSMBADDR_1		F8	V_{DD}PE	
A17	NC		C7	V_{SS}		D19	V_{DD}I/O		F9	V_{DD}PE	
A18	PE2TP00		C8	V_{SS}		D20	CCLKDS		F10	V_{DD}CORE	
A19	MSMBSMODE		C9	V_{SS}		D21	SSMBADDR_1		F11	V_{DD}CORE	
A20	MSMBDAT		C10	V_{SS}		D22	SSMBADDR_3		F12	V_{DD}CORE	
A21	JTAG_TMS		C11	V_{SS}		E1	V_{SS}		F13	V_{DD}CORE	
A22	V_{SS}		C12	V_{SS}		E2	V_{SS}		F14	V_{DD}PE	
B1	V_{SS}		C13	V_{SS}		E3	GPIO_31		F15	V_{DD}PE	
B2	GPIO_18		C14	V_{SS}		E4	GPIO_28		F16	V_{DD}I/O	
B3	V_{SS}		C15	V_{SS}		E5	GPIO_26		F17	V_{DD}I/O	
B4	PE9TP00		C16	V_{SS}		E6	GPIO_17		F18	SSMBADDR_5	
B5	PE8TP00		C17	V_{SS}		E7	V_{DD}PE		F19	V_{SS}	
B6	V_{SS}		C18	MSMBADDR_4		E8	V_{SS}		F20	V_{SS}	
B7	PE3RN00		C19	MSMBADDR_2		E9	V_{TT}PE		F21	NC	
B8	NC		C20	MSMBCLK		E10	V_{TT}PE		F22	NC	
B9	V_{SS}		C21	SSMBDAT		E11	V_{DD}PEA		G1	PE11RP00	
B10	PEREFCLKP1		C22	JTAG_TCK		E12	V_{DD}PEA		G2	PE11RN00	
B11	V_{SS}		D1	GPIO_29		E13	V_{TT}PE		G3	V_{SS}	
B12	PE3TP00		D2	GPIO_24		E14	V_{TT}PE		G4	V_{SS}	

Table 19 PES16H16 Signal Pin-Out (Part 1 of 4)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
G5	V_{DD}I/O		H20	V_{SS}		K13	V_{SS}		M6	V_{SS}	
G6	V_{DD}PE		H21	NC		K14	V_{DD}CORE		M7	V_{SS}	
G7	V_{SS}		H22	NC		K15	V_{DD}CORE		M8	V_{DD}CORE	
G8	V_{DD}CORE		J1	PE10TN00		K16	V_{SS}		M9	V_{DD}CORE	
G9	V_{DD}CORE		J2	PE10TP00		K17	V_{DD}PE		M10	V_{SS}	
G10	V_{SS}		J3	V_{SS}		K18	V_{TT}PE		M11	V_{DD}CORE	
G11	V_{DD}CORE		J4	V_{SS}		K19	NC		M12	V_{DD}CORE	
G12	V_{DD}CORE		J5	V_{TT}PE		K20	V_{SS}		M13	V_{SS}	
G13	V_{SS}		J6	V_{DD}PE		K21	V_{SS}		M14	V_{DD}CORE	
G14	V_{DD}CORE		J7	V_{SS}		K22	V_{SS}		M15	V_{DD}CORE	
G15	V_{DD}CORE		J8	V_{DD}CORE		L1	V_{SS}		M16	V_{SS}	
G16	V_{SS}		J9	V_{DD}CORE		L2	V_{SS}		M17	V_{SS}	
G17	V_{DD}I/O		J10	V_{SS}		L3	V_{SS}		M18	V_{DD}PEA	
G18	V_{SS}		J11	V_{DD}CORE		L4	V_{SS}		M19	NC	
G19	PE1RN00		J12	V_{DD}CORE		L5	V_{DD}PEA		M20	V_{SS}	
G20	V_{SS}		J13	V_{SS}		L6	V_{SS}		M21	V_{SS}	
G21	V_{SS}		J14	V_{DD}CORE		L7	V_{SS}		M22	V_{SS}	
G22	V_{SS}		J15	V_{DD}CORE		L8	V_{DD}CORE		N1	V_{SS}	
H1	V_{SS}		J16	V_{SS}		L9	V_{DD}CORE		N2	V_{SS}	
H2	V_{SS}		J17	V_{DD}PE		L10	V_{SS}		N3	V_{SS}	
H3	V_{SS}		J18	V_{TT}PE		L11	V_{DD}CORE		N4	V_{SS}	
H4	V_{SS}		J19	NC		L12	V_{DD}CORE		N5	V_{TT}PE	
H5	V_{DD}PE		J20	V_{SS}		L13	V_{SS}		N6	V_{SS}	
H6	V_{DD}PE		J21	NC		L14	V_{DD}CORE		N7	V_{SS}	
H7	V_{SS}		J22	NC		L15	V_{DD}CORE		N8	V_{DD}CORE	
H8	V_{DD}CORE		K1	PE11TN00		L16	V_{SS}		N9	V_{DD}CORE	
H9	V_{DD}CORE		K2	PE11TP00		L17	V_{SS}		N10	V_{SS}	
H10	V_{SS}		K3	V_{SS}		L18	V_{DD}PEA		N11	V_{DD}CORE	
H11	V_{DD}CORE		K4	V_{SS}		L19	NC		N12	V_{DD}CORE	
H12	V_{DD}CORE		K5	V_{TT}PE		L20	V_{SS}		N13	V_{SS}	
H13	V_{SS}		K6	V_{SS}		L21	PE0TP00		N14	V_{DD}CORE	
H14	V_{DD}CORE		K7	V_{SS}		L22	PE0TN00		N15	V_{DD}CORE	
H15	V_{DD}CORE		K8	V_{DD}CORE		M1	PEREFCLKN2		N16	V_{SS}	
H16	V_{SS}		K9	V_{DD}CORE		M2	PEREFCLKP2		N17	V_{SS}	
H17	V_{DD}PE		K10	V_{SS}		M3	V_{SS}		N18	V_{TT}PE	
H18	V_{DD}PE		K11	V_{DD}CORE		M4	V_{SS}		N19	V_{SS}	
H19	PE1RP00		K12	V_{DD}CORE		M5	V_{DD}PEA		N20	V_{SS}	

Table 19 PES16H16 Signal Pin-Out (Part 2 of 4)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
N21	PEREFCLKN0		R14	V_{DD}CORE		U7	V_{DD}PE		V22	PE15TP00	
N22	PEREFCLKP0		R15	V_{DD}CORE		U8	V_{DD}PE		W1	V_{SS}	
P1	PE4TN00		R16	V_{SS}		U9	V_{DD}PE		W2	V_{SS}	
P2	PE4TP00		R17	V_{DD}PE		U10	V_{DD}CORE		W3	V_{SS}	
P3	V_{SS}		R18	V_{SS}		U11	V_{DD}CORE		W4	REFCLKM	
P4	V_{SS}		R19	PE15RN00		U12	V_{DD}CORE		W5	RSTHALT	
P5	V_{TT}PE		R20	V_{SS}		U13	V_{DD}CORE		W6	SWMODE_1	
P6	V_{DD}PE		R21	NC		U14	V_{DD}PE		W7	V_{SS}	
P7	V_{SS}		R22	NC		U15	V_{DD}PE		W8	V_{SS}	
P8	V_{DD}CORE		T1	V_{SS}		U16	V_{DD}I/O		W9	V_{SS}	
P9	V_{DD}CORE		T2	V_{SS}		U17	V_{DD}I/O		W10	V_{SS}	
P10	V_{SS}		T3	V_{SS}		U18	V_{SS}		W11	V_{DD}PEA	
P11	V_{DD}CORE		T4	V_{SS}		U19	PE14RN00		W12	V_{SS}	
P12	V_{DD}CORE		T5	V_{SS}		U20	V_{SS}		W13	V_{SS}	
P13	V_{SS}		T6	V_{DD}PE		U21	V_{SS}		W14	V_{SS}	
P14	V_{DD}CORE		T7	V_{SS}		U22	V_{SS}		W15	V_{DD}I/O	
P15	V_{DD}CORE		T8	V_{DD}CORE		V1	PE5RP00		W16	GPIO_01	
P16	V_{SS}		T9	V_{DD}CORE		V2	PE5RN00		W17	GPIO_03	
P17	V_{DD}PE		T10	V_{SS}		V3	V_{SS}		W18	GPIO_04	
P18	V_{TT}PE		T11	V_{DD}CORE		V4	V_{SS}		W19	GPIO_08	
P19	PE15RP00		T12	V_{DD}CORE		V5	V_{DD}I/O		W20	V_{SS}	
P20	V_{SS}		T13	V_{SS}		V6	V_{DD}I/O		W21	PE14TN00	
P21	V_{SS}		T14	V_{DD}CORE		V7	V_{SS}		W22	PE14TP00	
P22	V_{SS}		T15	V_{DD}CORE		V8	V_{DD}PE		Y1	V_{DD}I/O	
R1	PE5TN00		T16	V_{SS}		V9	V_{TT}PE		Y2	CCLKUS	
R2	PE5TP00		T17	V_{DD}PE		V10	V_{TT}PE		Y3	V_{DD}I/O	
R3	V_{SS}		T18	V_{DD}PE		V11	V_{DD}PEA		Y4	SWMODE_0	
R4	V_{SS}		T19	PE14RP00		V12	V_{TT}PE		Y5	V_{SS}	
R5	V_{DD}PE		T20	V_{SS}		V13	V_{TT}PE		Y6	V_{SS}	
R6	V_{DD}PE		T21	PE0RN00		V14	V_{DD}PE		Y7	V_{SS}	
R7	V_{SS}		T22	PE0RP00		V15	V_{DD}PE		Y8	V_{SS}	
R8	V_{DD}CORE		U1	PE4RP00		V16	V_{DD}I/O		Y9	V_{SS}	
R9	V_{DD}CORE		U2	PE4RN00		V17	GPIO_06		Y10	V_{SS}	
R10	V_{SS}		U3	V_{SS}		V18	GPIO_11		Y11	V_{SS}	
R11	V_{DD}CORE		U4	V_{SS}		V19	V_{SS}		Y12	V_{SS}	
R12	V_{DD}CORE		U5	V_{SS}		V20	V_{SS}		Y13	V_{SS}	
R13	V_{SS}		U6	V_{DD}I/O		V21	PE15TN00		Y14	V_{SS}	

Table 19 PES16H16 Signal Pin-Out (Part 3 of 4)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
Y15	V_{SS}		AA6	PE7RN00		AA19	GPIO_05		AB10	V_{SS}	
Y16	V_{SS}		AA7	V_{SS}		AA20	V_{DD}I/O		AB11	PEREFCLKN3	
Y17	V_{SS}		AA8	PE6TP00		AA21	GPIO_12		AB12	V_{SS}	
Y18	GPIO_00		AA9	PE7TP00		AA22	GPIO_14		AB13	PE12TN00	
Y19	GPIO_07		AA10	V_{SS}		AB1	V_{DD}I/O		AB14	PE13TN00	
Y20	GPIO_09		AA11	PEREFCLKP3		AB2	V_{SS}		AB15	V_{SS}	
Y21	V_{SS}		AA12	V_{SS}		AB3	SWMODE_02		AB16	PE12RP00	
Y22	V_{SS}		AA13	PE12TP00		AB4	V_{SS}		AB17	PE13RP00	
AA1	V_{SS}		AA14	PE13TP00		AB5	PE6RP00		AB18	V_{SS}	
AA2	V_{DD}I/O		AA15	V_{SS}		AB6	PE7RP00		AB19	GPIO_02	
AA3	SWMODE_3		AA16	PE12RN00		AB7	V_{SS}		AB20	GPIO_10	
AA4	V_{SS}		AA17	PE13RN00		AB8	PE6TN00		AB21	GPIO_13	
AA5	PE6RN00		AA18	V_{SS}		AB9	PE7TN00		AB22	GPIO_15	

Table 19 PES16H16 Signal Pin-Out (Part 4 of 4)

Alternate Signal Functions

Pin	GPIO	Alternate	Pin	GPIO	Alternate
AA19	GPIO_05	GPEN	E6	GPIO_17	P12RSTN
V17	GPIO_06	P1RSTN	B2	GPIO_18	P13RSTN
Y19	GPIO_07	P2RSTN	C3	GPIO_19	P14RSTN
W19	GPIO_08	P3RSTN	D5	GPIO_20	P15RSTN
Y20	GPIO_09	P4RSTN	C2	GPIO_21	IOEXPINTN0
AB20	GPIO_10	P5RSTN	D4	GPIO_23	IOEXPINTN2
V18	GPIO_11	P6RSTN	D2	GPIO_24	IOEXPINTN3
AA21	GPIO_12	P7RSTN	E5	GPIO_26	IOEXPINTN5
AB21	GPIO_13	P8RSTN	D3	GPIO_27	IOEXPINTN6
AA22	GPIO_14	P9RSTN	E4	GPIO_28	IOEXPINTN7
AB22	GPIO_15	P10RSTN	E3	GPIO_31	IOEXPINTN10
A2	GPIO_16	P11RSTN	—	—	—

Table 20 PES16H16 Alternate Signal Functions

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No Connection Pins

No Connection			
A8	B15	F21	J22
A14	B17	F22	K19
A15	D12	H21	L19
A17	D13	H22	M19
B8	D14	J19	R21
B14	D15	J21	R22

Table 21 PES16H16 No Connection Pins

Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}IO	V_{DD}PE	V_{DD}PE	V_{DD}PEA	V_{TT}PE
F10	K9	P8	A1	E7	P6	E11	E9
F11	K11	P9	C1	E16	P17	E12	E10
F12	K12	P11	D19	E17	R5	L5	E13
F13	K14	P12	F5	F7	R6	L18	E14
G8	K15	P14	F6	F8	R17	M5	J5
G9	L8	P15	F16	F9	T6	M18	J18
G11	L9	R8	F17	F14	T17	V11	K5
G12	L11	R9	G5	F15	T18	W11	K18
G14	L12	R11	G17	G6	U7		N5
G15	L14	R12	U6	H5	U8		N18
H8	L15	R14	U16	H6	U9		P5
H9	M8	R15	U17	H17	U14		P18
H11	M9	T8	V5	H18	U15		V9
H12	M11	T9	V6	J6	V8		V10
H14	M12	T11	V16	J17	V14		V12
H15	M14	T12	W15	K17	V15		V13
J8	M15	T14	Y1				
J9	N8	T15	Y3				
J11	N9	U10	AA2				
J12	N11	U11	AA20				
J14	N12	U12	AB01				
J15	N14	U13					
K8	N15	—					

Table 22 PES16H16 Power Pins

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Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A3	C17	H16	L16	P4	U4	Y10
A6	D6	H20	L17	P7	U5	Y11
A9	D11	J3	L20	P10	U18	Y12
A11	E1	J4	M3	P13	U20	Y13
A13	E2	J7	M4	P16	U21	Y14
A16	E8	J10	M6	P20	U22	Y15
A22	E15	J13	M7	P21	V3	Y16
B1	F3	J16	M10	P22	V4	Y17
B3	F19	J20	M13	R3	V7	Y21
B6	F20	K3	M16	R4	V19	Y22
B9	G3	K4	M17	R7	V20	AA1
B11	G4	K6	M20	R10	W1	AA4
B13	G7	K7	M21	R13	W2	AA7
B16	G10	K10	M22	R16	W3	AA10
C4	G13	K13	N1	R18	W7	AA12
C5	G16	K16	N2	R20	W8	AA15
C6	G18	K20	N3	T1	W9	AA18
C7	G20	K21	N4	T2	W10	AB2
C8	G21	K22	N6	T3	W12	AB4
C9	G22	L1	N7	T4	W13	AB7
C10	H1	L2	N10	T5	W14	AB10
C11	H2	L3	N13	T7	W20	AB12
C12	H3	L4	N16	T10	Y5	AB15
C13	H4	L6	N17	T13	Y6	AB18
C14	H7	L7	N19	T16	Y7	
C15	H10	L10	N20	T20	Y8	
C16	H13	L13	P3	U3	Y9	

Table 23 PES16H16 Ground Pins

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Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	D20	System
CCLKUS	I	Y2	
GPIO_00	I/O	Y18	General Purpose Input/Output
GPIO_01	I/O	W16	
GPIO_02	I/O	AB19	
GPIO_03	I/O	W17	
GPIO_04	I/O	W18	
GPIO_05	I/O	AA19	
GPIO_06	I/O	V17	
GPIO_07	I/O	Y19	
GPIO_08	I/O	W19	
GPIO_09	I/O	Y20	
GPIO_10	I/O	AB20	
GPIO_11	I/O	V18	
GPIO_12	I/O	AA21	
GPIO_13	I/O	AB21	
GPIO_14	I/O	AA22	
GPIO_15	I/O	AB22	
GPIO_16	I/O	A2	
GPIO_17	I/O	E6	
GPIO_18	I/O	B2	
GPIO_19	I/O	C3	
GPIO_20	I/O	D5	
GPIO_21	I/O	C2	
GPIO_23	I/O	D4	
GPIO_24	I/O	D2	
GPIO_26	I/O	E5	
GPIO_27	I/O	D3	
GPIO_28	I/O	E4	
GPIO_29	I/O	D1	
GPIO_30	I/O	F4	
GPIO_31	I/O	E3	

Table 24 89PES16H16 Alphabetical Signal List (Part 1 of 4)

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Signal Name	I/O Type	Location	Signal Category
JTAG_TCK	I	C22	JTAG
JTAG_TDI	I	B22	
JTAG_TDO	O	B20	
JTAG_TMS	I	A21	
JTAG_TRST_N	I	E18	
MSMBADDR_1	I	D18	SMBus
MSMBADDR_2	I	C19	
MSMBADDR_3	I	B19	
MSMBADDR_4	I	C18	
MSMBCLK	I/O	C20	
MSMBDAT	I/O	A20	
MSMBSMODE	I	A19	System
NO CONNECTION	See Table 21 for a listing of No Connection pins.		
PE0RN00	I	T21	PCI Express
PE0RP00	I	T22	
PE0TN00	O	L22	
PE0TP00	O	L21	
PE1RN00	I	G19	
PE1RP00	I	H19	
PE1TN00	O	E22	
PE1TP00	O	E21	
PE2RN00	I	D17	
PE2RP00	I	D16	
PE2TN00	O	B18	
PE2TP00	O	A18	
PE3RN00	I	B7	
PE3RP00	I	A7	
PE3TN00	O	A12	
PE3TP00	O	B12	
PE4RN00	I	U2	
PE4RP00	I	U1	
PE4TN00	O	P1	
PE4TP00	O	P2	
PE5RN00	I	V2	
PE5RP00	I	V1	
PE5TN00	O	R1	

Table 24 89PES16H16 Alphabetical Signal List (Part 2 of 4)

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Signal Name	I/O Type	Location	Signal Category
PE5TP00	O	R2	PCI Express (Cont.)
PE6RN00	I	AA5	
PE6RP00	I	AB5	
PE6TN00	O	AB8	
PE6TP00	O	AA8	
PE7RN00	I	AA6	
PE7RP00	I	AB6	
PE7TN00	O	AB9	
PE7TP00	O	AA9	
PE8RN00	I	D10	
PE8RP00	I	D9	
PE8TN00	O	A5	
PE8TP00	O	B5	
PE9RN00	I	D8	
PE9RP00	I	D7	
PE9TN00	O	A4	
PE9TP00	O	B4	
PE10RN00	I	F2	
PE10RP00	I	F1	
PE10TN00	O	J1	
PE10TP00	O	J2	
PE11RN00	I	G2	
PE11RP00	I	G1	
PE11TN00	O	K1	
PE11TP00	O	K2	
PE12RN00	I	AA16	
PE12RP00	I	AB16	
PE12TN00	O	AB13	
PE12TP00	O	AA13	
PE13RN00	I	AA17	
PE13RP00	I	AB17	
PE13TN00	O	AB14	
PE13TP00	O	AA14	
PE14RN00	I	U19	
PE14RP00	I	T19	
PE14TN00	O	W21	

Table 24 89PES16H16 Alphabetical Signal List (Part 3 of 4)

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Signal Name	I/O Type	Location	Signal Category
PE14TP00	O	W22	PCI Express (Cont.)
PE15RN00	I	R19	
PE15RP00	I	P19	
PE15TN00	O	V21	
PE15TP00	O	V22	
PEREFCLKN0	I	N21	
PEREFCLKN1	I	A10	
PEREFCLKN2	I	M1	
PEREFCLKN3	I	AB11	
PEREFCLKP0	I	N22	
PEREFCLKP1	I	B10	
PEREFCLKP2	I	M2	
PEREFCLKP3	I	AA11	
PERSTN	I	B21	System
REFCLKM	I	W4	PCI Express
RSTHALT	I	W5	System
SSMBADDR_1	I	D21	SMBus
SSMBADDR_2	I	E20	
SSMBADDR_3	I	D22	
SSMBADDR_5	I	F18	
SSMBCLK	I/O	E19	
SSMBDAT	I/O	C21	
SWMODE_0	I	Y4	System
SWMODE_1	I	W6	
SWMODE_2	I	AB3	
SWMODE_3	I	AA3	
V_{DD}CORE, V_{DD}PEA, V_{DD}IO, V_{DD}PE, V_{TT}PE	See Table 22 for a listing of power pins.		
V_{SS}	See Table 23 for a listing of ground pins.		

Table 24 89PES16H16 Alphabetical Signal List (Part 4 of 4)

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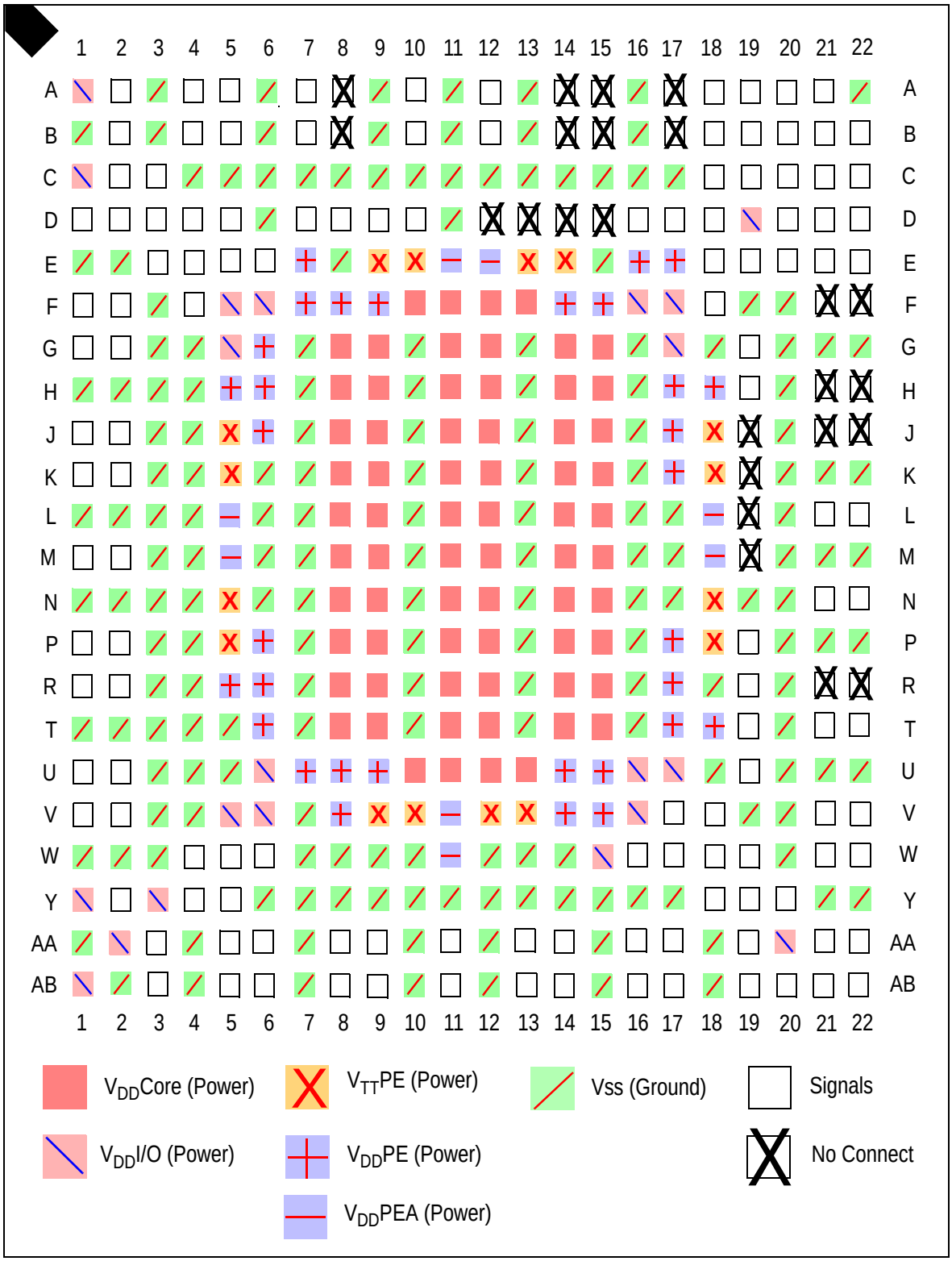
PES16H16 Pinout — Top View



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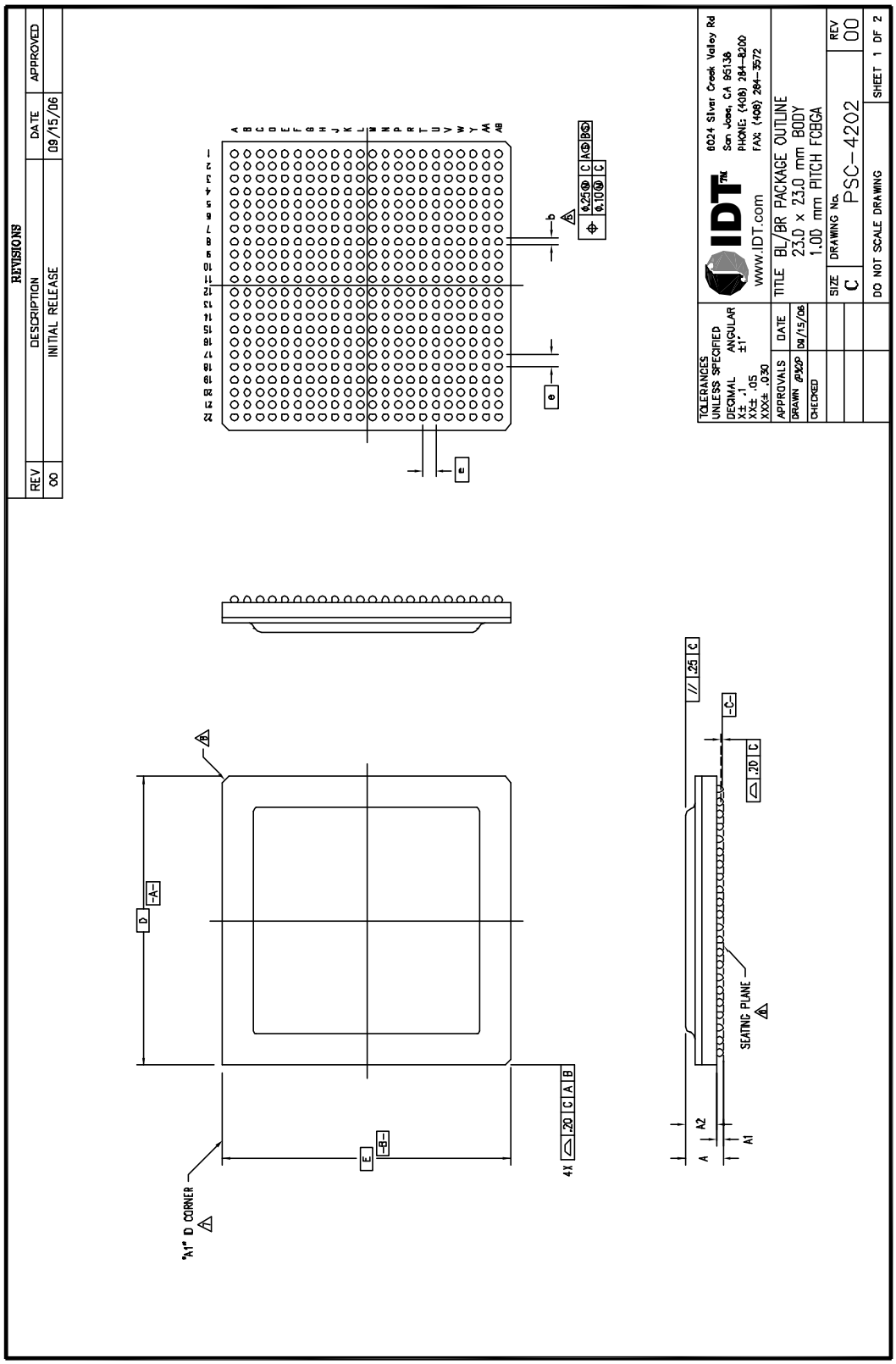
PES16H16 Package Drawing — 484-Pin BL484/BR484



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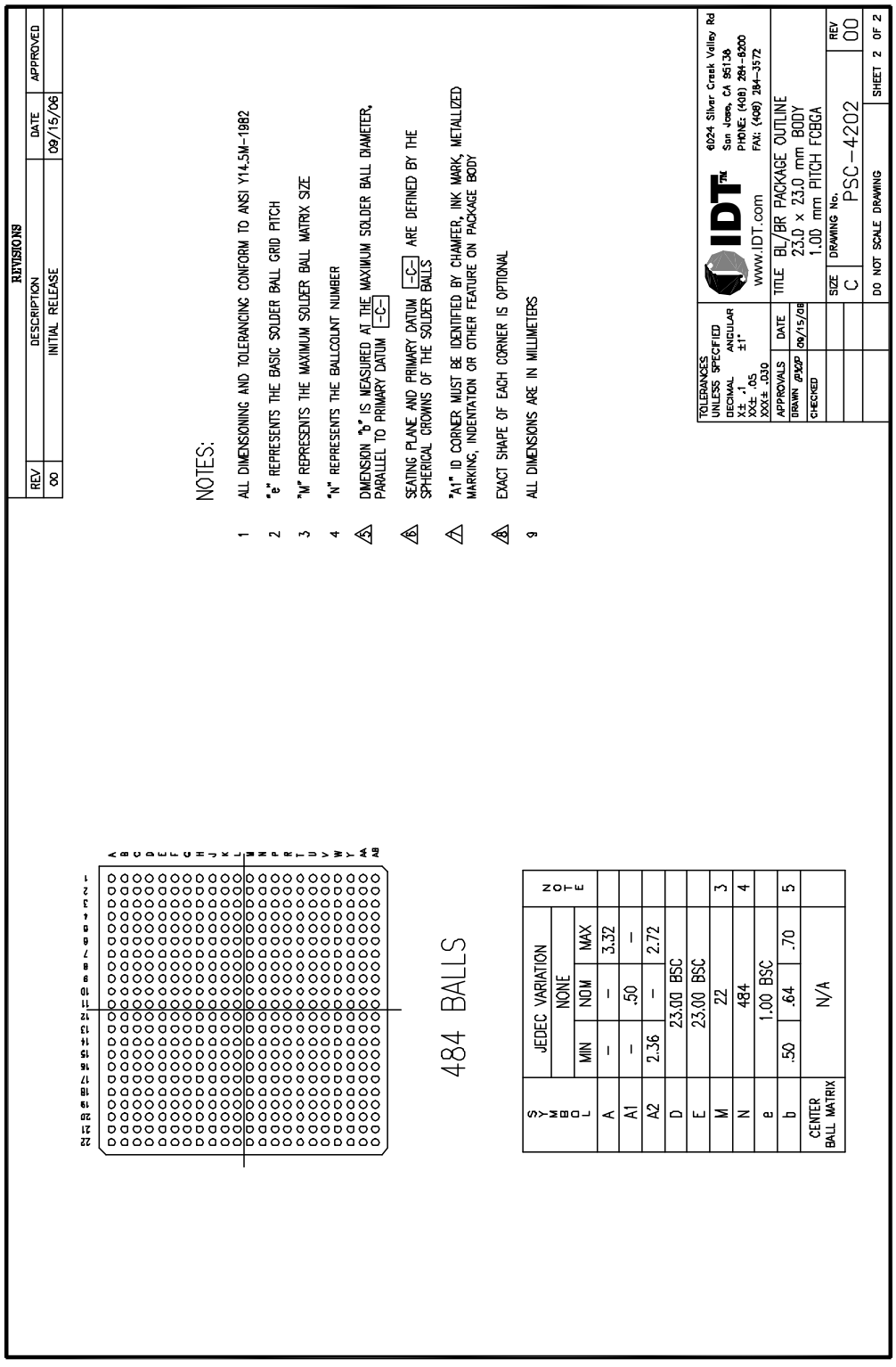
PES16H16 Package Drawing — Page Two



REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	09/15/06	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE
4. "N" REPRESENTS THE BALLCOUNT NUMBER
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-
6. SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
7. "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. ALL DIMENSIONS ARE IN MILLIMETERS

484 BALLS

SYMBOL	JEDEC VARIATION NONE MIN	NOM	MAX	NOTE
A	–	–	3.32	
A1	–	.50	–	
A2	2.36	–	2.72	
D		23.00 BSC		
E		23.00 BSC		
M		22		3
N		484		4
e		1.00 BSC		
b	.50	.64	.70	5
CENTER BALL MATRIX		N/A		

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± .1 ±1°
XX± .05
XXX± .030

APPROVALS DATE
DRAWN JPK/JP 09/15/06
CHECKED

IDT™
www.IDT.com

6024 Silver Creek Valley Rd
San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-3572

TITLE BL/BR PACKAGE OUTLINE
23.0 x 23.0 mm BODY
1.00 mm PITCH FCBGA

SIZE C | DRAWING No. PSC-4202 | REV 00

DO NOT SCALE DRAWING | SHEET 2 OF 2

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Revision History

April 7, 2008: Publication of Preliminary data sheet with 23x23mm FCBGA package option.

April 16, 2008: In Table 16, Thermal Specifications, revised values for θ_{JA}, θ_{JB}, and θ_{JC}..

October 21, 2009: Added Industrial temperature to ordering codes on page 35.

October 3, 2011: Added new Table 14, PES16H16 Absolute Maximum Voltage Rating.

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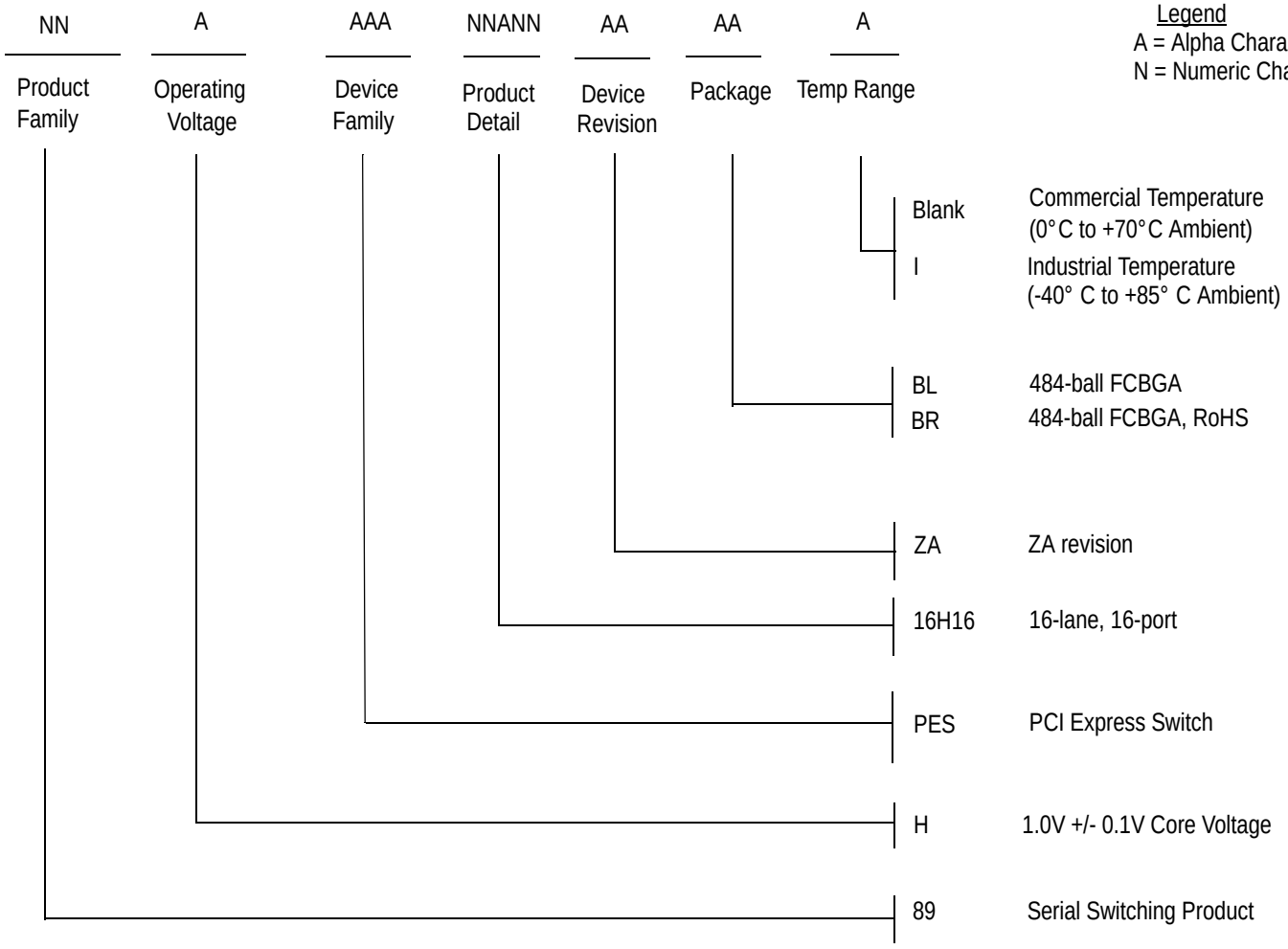
Ordering Information



Valid Combinations

89HPES16H16ZABL	484-ball FCBGA package, Commercial Temperature
89HPES16H16ZABR	484-ball RoHS FCBGA package, Commercial Temperature
89HPES16H16ZABLI	484-ball FCBGA package, Industrial Temperature
89HPES16H16ZABRI	484-ball RoHS FCBGA package, Industrial Temperature

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