

8P34S1208-1

2:8 LVDS 1.8V / 2.5V Fanout Buffer for 1PPS and High-Speed Clocks with Individual OE Control

The 8P34S1208-1 is a high-performance differential LVDS fanout buffer. The device is designed for the fanout of 1PPS signals or high-frequency, very low additive phase-noise clock and data signals.

The 8P34S1208-1 supports fail-safe operation and is characterized to operate from a 1.8V or 2.5V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the device ideal for clock distribution applications that demand well-defined performance and repeatability.

Two selectable differential inputs and eight low skew outputs are available. The integrated bias voltage reference enables easy interfacing of single-ended signals to the device inputs. The device is optimized for low power consumption and low additive phase noise.

The 8P34S1208-1 uses AMP_SEL to control the Output Swing control by output bank, and uses individual OE pins to control output enable/disable, which allows for excellent control over both swing and output enable functions.

Features

- Eight low skew, low additive jitter LVDS output pairs in two output banks (Q0 to Q3, Q4 to Q7)
- Individual OE control pin for each output
- Bank-selectable pin for bank swing output (Q0 to Q3 as bank 0, Q4 to Q7 as bank 1)
- Two selectable, differential clock input pairs
- Differential CLK, nCLK pairs can accept LVDS and CML differential input levels
- Maximum input clock frequency of 2GHz
- LVCMOS/LVTTL interface levels for the control input-select pin
- Output skew of 20ps (typical)
- Propagation delay of 450ps (maximum)
- Low propagation delay variation across temperature for 1PPS applications
- Low additive phase jitter, RMS; $f_{REF} = 156.25\text{MHz}$, $V_{PP} = 1\text{V}$
- 12kHz to 20MHz: 50fs (typical)
- Device current consumption (I_{DD}): 225mA
- Full 1.8V or 2.5V supply voltage
- Lead-free (RoHS 6), 40-VFQFPN packaging
- -40°C to +85°C ambient operating temperature
- Supports case temperature up to +105°C

Applications

- 4G and 5G RU and DU system
- Ethernet switches / routers
- Medical imaging
- Professional audio and video
- Data center and server

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1. Overview

1.1 Block Diagram

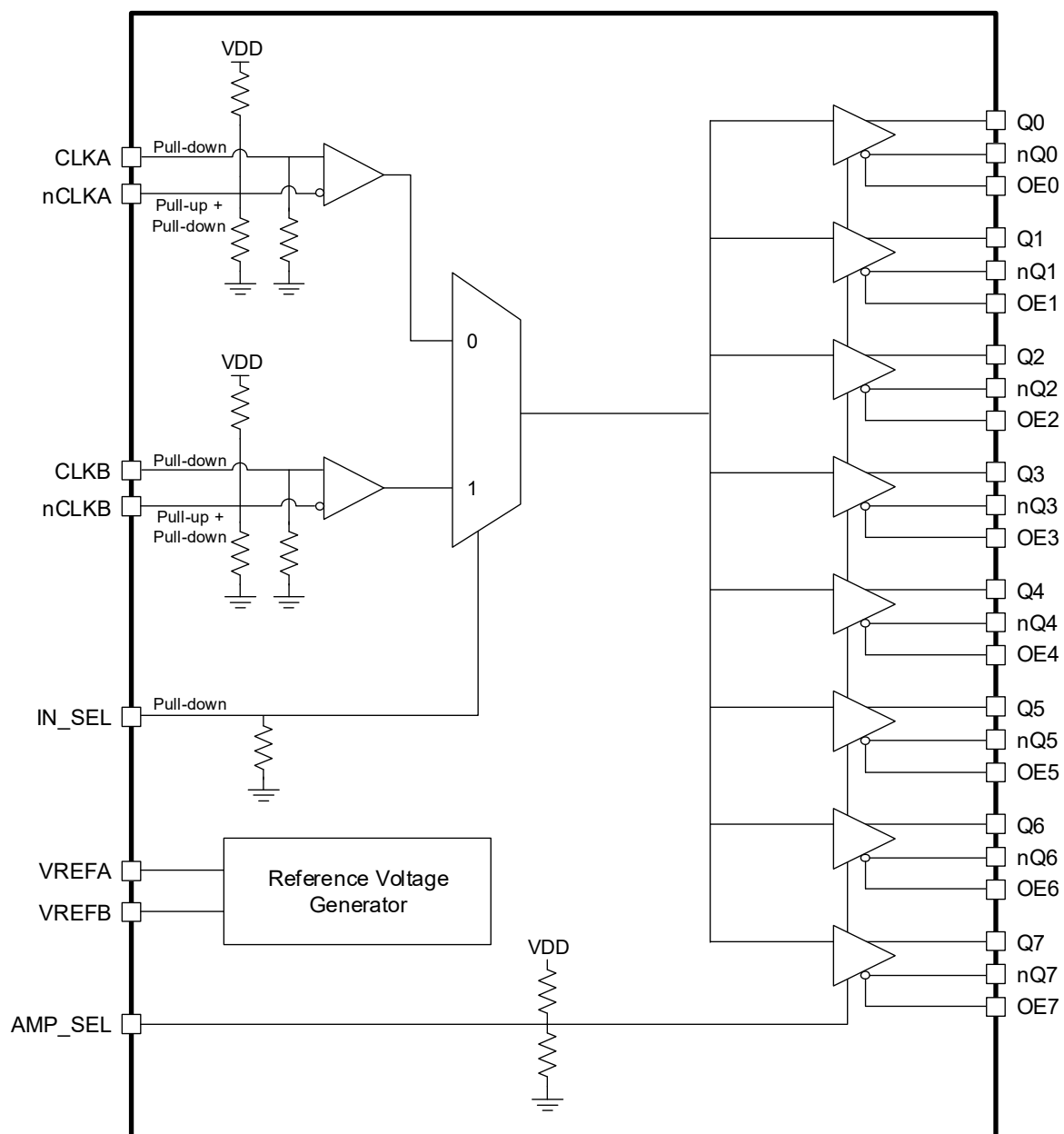


Figure 1. Block Diagram

2. Pin Information

2.1 Pin Assignments

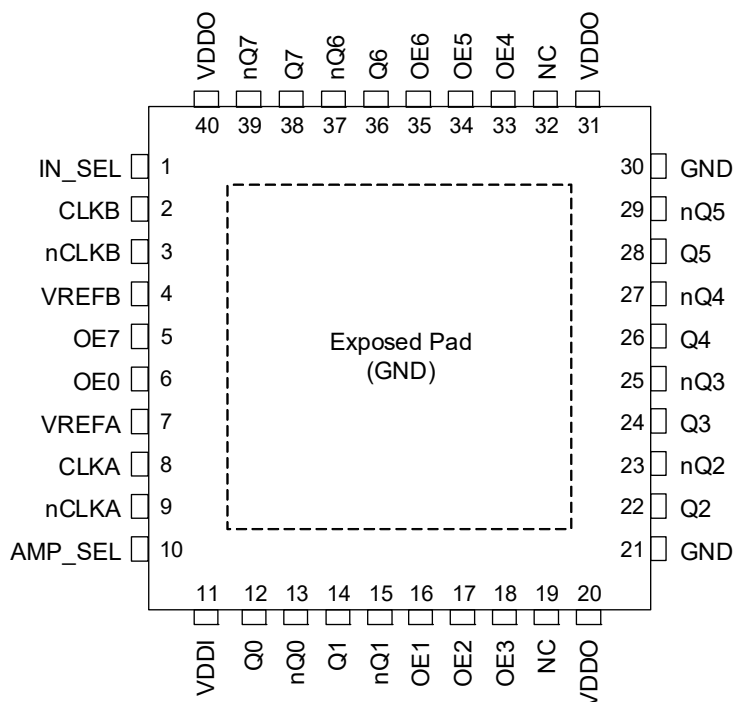


Figure 2. Pin Assignments – Top View

2.2 Pin Descriptions

Table 1. Pin Descriptions

| Pin Number | Pin Name | Type | Description |
|------------|----------|--------|---|
| 1 | IN_SEL | Input | Reference selects control pin. LVCMOS/LVTTL interface levels. |
| 2 | CLKB | Input | Non-inverting differential clock/data input B. |
| 3 | nCLKB | Input | Inverting differential clock/data input B. VDD/2 default when left floating. |
| 4 | VREFB | Power | Bias voltage reference. Provides an input bias voltage for the CLKB, nCLKB input pair in AC-coupled applications. |
| 5 | OE7 | Input | Control output enable function for Q7. LVCMOS/TTL input levels. |
| 6 | OE0 | Input | Control output enable function for Q0. LVCMOS/TTL input levels. |
| 7 | VREFA | Power | Bias voltage reference. Provides an input bias voltage for the CLKA, nCLKA input pair in AC-coupled applications. |
| 8 | CLKA | Input | Non-inverting differential clock/data input A. |
| 9 | nCLKA | Input | Inverting differential clock/data input A. VDD/2 default when left floating. |
| 10 | AMP_SEL | Input | Output swing control pin. |
| 11 | VDDI | Power | Power supply input pin. |
| 12 | Q0 | Output | Differential output pair Q0. LVDS interface levels |
| 13 | nQ0 | Output | Differential output pair Q0. LVDS interface levels. |

Table 1. Pin Descriptions (Cont.)

| Pin Number | Pin Name | Type | Description |
|------------|----------|--------|---|
| 14 | Q1 | Output | Differential output pair Q1. LVDS interface levels. |
| 15 | nQ1 | Output | Differential output pair Q1. LVDS interface levels. |
| 16 | OE1 | Input | Control output enable function for Q1. LVCMOS/TTL input levels. |
| 17 | OE2 | Input | Control output enable function for Q2. LVCMOS/TTL input levels. |
| 18 | OE3 | Input | Control output enable function for Q3. LVCMOS/TTL input levels. |
| 19 | NC | - | Not connected. |
| 20 | VDDO | Power | Power supply pin. |
| 21 | GND | Power | Ground pin. |
| 22 | Q2 | Output | Differential output pair Q2. LVDS interface levels. |
| 23 | nQ2 | Output | Differential output pair Q2. LVDS interface levels. |
| 24 | Q3 | Output | Differential output pair Q3. LVDS interface levels. |
| 25 | nQ3 | Output | Differential output pair Q3. LVDS interface levels. |
| 26 | Q4 | Output | Differential output pair Q4. LVDS interface levels. |
| 27 | nQ4 | Output | Differential output pair Q4. LVDS interface levels. |
| 28 | Q5 | Output | Differential output pair Q6. LVDS interface levels. |
| 29 | nQ5 | Output | Differential output pair Q5. LVDS interface levels. |
| 30 | GND | Power | Ground pin. |
| 31 | VDDO | Power | Power supply pin. |
| 32 | NC | - | Not connected. |
| 33 | OE4 | Input | Control output enable function for Q4. LVCMOS/TTL input levels. |
| 34 | OE5 | Input | Control output enable function for Q5. LVCMOS/TTL input levels. |
| 35 | OE6 | Input | Control output enable function for Q6. LVCMOS/TTL input levels. |
| 36 | Q6 | Output | Differential output pair Q6. LVDS interface levels. |
| 37 | nQ6 | Output | Differential output pair Q6. LVDS interface levels. |
| 38 | Q7 | Output | Differential output pair Q7. LVDS interface levels. |
| 39 | nQ7 | Output | Differential output pair Q7. LVDS interface levels. |
| 40 | VDDO | Power | Power supply pin. |
| - | ePAD | Power | EPAD connect to GND. |

2.3 IN_SEL Input Functions

| IN_SEL Input [1] | Operation |
|------------------|---|
| 0 | CLKA, nCLKA is the selected differential clock input. |
| 1 | CLKB, nCLKB is the selected differential clock input. |

1. IN_SEL is an asynchronous control.

2.4 AMP_SEL Functions

| AMP_SEL | Output |
|---------|----------------------------------|
| Low | Q0 – Q3 = 500mV, Q4 – Q7 = 350mV |
| Middle | Q0 – Q7 = 350mV |
| High | Q0 – Q7 = 500mV |

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Figure 3. Absolute Maximum Ratings

| Parameter | Minimum | Maximum | Unit |
|---|---------|---------|------|
| Supply Voltage, V_{DD} | - | 4.6 | V |
| Input, V_I | -0.5 | 4.6 | V |
| Input, I_I | - | 20 | mA |
| Outputs, I_O | | | |
| Continuous Current | - | 10 | mA |
| Surge Current | - | 15 | |
| Input Sink/Source, I_{REF} | - | ±2 | mA |
| Maximum Junction Temperature, $T_{J,MAX}$ | - | 125 | °C |
| Storage Temperature, T_{STG} | -65 | 150 | °C |
| ESD – Human Body Model | - | 2000 | V |
| ESD – Charged Device Model | - | 1500 | V |

3.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions [1][2]

| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Unit |
|-----------|---------------------------------------|-------------------------------|---------|---------|---------|------|
| T_J | Maximum Junction Temperature | - | - | - | 125 | °C |
| T_A | Ambient Operating Temperature | - | -40 | - | 85 | °C |
| V_{DDx} | Supply Voltage with Respect to Ground | Any V_{DD} pin, 1.8V supply | 1.71 | 1.8 | 1.89 | V |
| | | Any V_{DD} pin, 2.5V supply | 2.1 | 2.5 | 2.7 | V |

1. All electrical characteristics are specified over Recommended Operating Conditions unless noted otherwise.
2. All conditions in this table must be met to guarantee device functionality and performance.

3.3 Thermal Specifications

| Parameter | Package | Symbol | Conditions | Typical Value | Unit |
|--------------------|-------------------------|----------------|-------------------------------------|---------------|------|
| Thermal Resistance | 40-VFQFPN, 6.0 × 6.0 mm | θ_{JA0} | Junction to ambient, still air | 24 | °C/W |
| | | θ_{JA1} | Junction to ambient, 1 m/s air flow | 21 | °C/W |
| | | θ_{JA2} | Junction to ambient, 2 m/s air flow | 19 | °C/W |
| | | θ_{JB} | Junction to board | 1.4 | °C/W |
| | | θ_{JC} | Junction to case | 19.2 | °C/W |

3.4 DC Input Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|----------------|--------------------------|-----------------|---------|---------|---------|--------|
| C_{IN} | Input Capacitance | - | - | 2 | - | pF |
| $R_{PULLDOWN}$ | Input Pull-down Resistor | - | - | 51 | - | k ohms |
| R_{PULLUP} | Input Pull-up Resistor | - | - | 51 | - | k ohms |

3.5 Power Supply Characteristics

$V_{DD} = 1.8V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|----------|----------------------|-----------------|---------|---------|---------|------|
| V_{DD} | Power Supply Voltage | - | 1.71 | 1.8 | 1.89 | V |
| I_{DD} | Power Supply Current | AMP_SEL = 500mV | - | 215.0 | 270.0 | mA |

3.6 Power Supply Characteristics

$V_{DD} = 2.1V, 2.5V$, and $2.7V$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$.

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|----------|----------------------|-----------------|---------|---------|---------|------|
| V_{DD} | Power Supply Voltage | - | 2.1 | 2.5 | 2.7 | V |
| I_{DD} | Power Supply Current | AMP_SEL = 500mV | - | 225.0 | 280.0 | mA |

3.7 LVCMOS/LVTTL Input DC Characteristics

$V_{DD} = 1.8V \pm 5\%$, $2.1V$ to $2.7V$, $T_A = -40^\circ C$ to $85^\circ C$.

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|------------|-----------------------------------|---|----------------------|---------|----------------------|---------|
| V_{IH} | Input High Voltage | $V_{DD} = 1.89V, 2.7V$ | $0.75 \times V_{DD}$ | - | $V_{DD} + 0.3$ | V |
| V_{IM} | Input Middle Voltage | $V_{DD} = 1.89V, 2.7V$ | $0.45 \times V_{DD}$ | - | $0.55 \times V_{DD}$ | V |
| V_{IL} | Input Low Voltage | $V_{DD} = 1.89V, 2.7V$ | -0.3 | - | $0.25 \times V_{DD}$ | V |
| I_{IH} | Input High Current, AMP_SEL | $V_{DD} = V_{IN} = 1.89V, 2.7V$ | - | - | 150 | μA |
| I_{IL} | Input Low Current, AMP_SEL | $V_{DD} = 1.89V, 2.7V$, $V_{IN} = 0V$ | -150 | - | - | μA |
| I_{LEAK} | Input Leakage Current, AMP_SEL | $V_{IN} = 2.7V, V_{DD} = 0V$ | - | - | 250 | μA |

3.8 LVCMOS/LVTTL Input DC Characteristics

$V_{DD} = 1.8V \pm 5\%$, 2.1V to 2.7V, $T_A = -40^\circ\text{C}$ to 85°C .

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|------------|---|---|----------------------|---------|----------------------|---------------|
| V_{IH} | Input High Voltage | $V_{DD} = 1.89V, 2.7V$ | $0.65 \times V_{DD}$ | - | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | $V_{DD} = 1.89V, 2.7V$ | -0.3 | - | $0.35 \times V_{DD}$ | V |
| I_{IH} | Input High Current, IN_SEL, OE0 to OE7 | $V_{DD} = V_{IN} = 1.89V, 2.7V$ | - | - | 150 | μA |
| I_{IL} | Input High Current, IN_SEL, OE0 to OE7 | $V_{DD} = 1.89V, 2.7V$, $V_{IN} = 0V$ | -150 | - | - | μA |
| I_{LEAK} | Input Leakage Current, IN_SEL, OE0 to OE7 | $V_{IN} = 2.7V, V_{DD} = 0V$ | - | - | 250 | μA |

3.9 Differential Input Characteristics

$V_{DD} = 1.8V \pm 5\%$, 2.1V to 2.7V, $T_A = -40^\circ\text{C}$ to 85°C .

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|------------|---|--|---------------------|---------|-----------------------|---------------|
| I_{IH} | Input High Current CLKA, nCLKA; CLKB, nCLKB | $V_{DD} = V_{IN} = 1.89V, 2.7V$ | - | - | 150 | μA |
| I_{IL} | Input Low Current CLKA, CLKB | $V_{IN} = 0V, V_{DD} = 1.89V, 2.7V$ | -150 | - | - | μA |
| | Input Low Current nCLKA, nCLKB | $V_{IN} = 0V, V_{DD} = 1.89V, 2.7V$ | -150 | - | - | μA |
| I_{LEAK} | Input Leakage Current | $V_{IN} = 2.7V, V_{DD} = 0V$ | - | - | 250 | μA |
| V_{REF} | Reference Voltage for Input Bias | $I_{REF} = -100\mu\text{A}$; $V_{DD} = 1.8V, 2.5V$ | $0.7 \times V_{DD}$ | - | $0.85 \times V_{DD}$ | V |
| V_{PP} | Peak-to-Peak Voltage | $V_{DD} = 1.89V, 2.7V$ | 0.2 | - | 1 | V |
| V_{CMR} | Common Mode Input Voltage | - | 0.9 | - | $V_{DD} - (V_{PP}/2)$ | V |

3.10 LVDS AC and DC Characteristics

$V_{DD} = 1.8V \pm 5\%$, 2.1V to 2.7V, $T_A = -40^\circ\text{C}$ to 85°C .

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|-----------------|----------------------|-----------------|---------|---------|---------|------|
| ΔV_{OD} | VOD Magnitude Change | - | - | - | 50 | mV |
| ΔV_{OD} | VOD Magnitude Change | - | - | - | 50 | mV |

3.11 AC Characteristics

$V_{DD} = V_{DDA} = V_{DDB} = V_{DDQB} = V_{DDQA} = 1.8V \pm 5\%$ or $2.1V, 2.5V, 2.7V$, $V_{EE} = 0V$, $T_A = -40^\circ\text{C}$ to 85°C

Table 3. AC Characteristics [1]

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|-------------------|-----------------------------------|---|---------|---------|---------|--------|
| f_{REF} | Input Frequency | - | 0 | - | 2 | GHz |
| dV/dt | Input Edge Rate | - | 1.5 | - | - | V/ns |
| t_{PD} | Propagation Delay | CLK[0:1], nCLK[0:1] to any Qx, nQx $V_{DD} = 1.8V$ $V_{DD} = 2.5V$ | 100 | 350 | 450 | ps |
| $tsk(o)$ | Output Skew | Qx, nQx $V_{DD} = 1.8V$ $V_{DD} = 2.5V$ | - | 20 | 40 | ps |
| $tsk(p)$ | Pulse Skew | $f_{REF} = 100\text{MHz}$ $V_{DD} = 1.8V$ $V_{DD} = 2.5V$ | - | 5 | 25 | ps |
| $tsk(i)$ | Input Skew | - $V_{DD} = 1.8V \pm 5\%$ $V_{DD} = 2.5V \pm 5\%$ | - | - | 60.0 | ps |
| $tsk(pp)$ | Part-to-part Skew | $f_{REF} = 100\text{MHz}$ $V_{DD} = 1.8V$ $V_{DD} = 2.5V$ | - | - | 200 | ps |
| t_{jit} | Buffer Additive Phase Jitter, RMS | $f_{REF} = 122.88\text{MHz}$ Square Wave, $V_{PP} = 1V$, Integration Range: 12kHz to 20MHz | - | 50 | - | fs |
| | | $f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 1V$, Integration Range: 12kHz to 20MHz | - | 50 | - | fs |
| | | $f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 0.5V$, Integration Range: 12kHz to 20MHz | - | 50 | - | fs |
| PNF | Phase noise floor | Phase noise floor carrier frequency at 122.88MHz at 20MHz offset | - | -160 | - | dBc/Hz |
| t_R / t_F | Output Rise/ Fall Time | $V_{DD} = 1.8V \pm 5\%$ 10% to 90% | - | 150 | 400 | ps |
| | | $V_{DD} = 1.8V \pm 5\%$ 20% to 80% | - | 90 | 160 | ps |
| | | $V_{DD} = 2.1V, 2.5V, 2.7V$ 10% to 90% | - | 200 | 420 | ps |
| | | $V_{DD} = 2.1V, 2.5V, 2.7V$ 20% to 80% | - | 110 | 190 | ps |
| $MUX_{isolation}$ | Mux Isolation | $f_{REF} = 100\text{MHz}$ | - | 80 | - | dB |
| V_{OD} | Differential Output Voltage | Output = 350mV, $R_{OUT} = 100\Omega$ $f_{REF} < 2\text{GHz}$ | 247 | 350 | 454 | mV |
| | | Output = 350mV, $R_{OUT} = 100\Omega$ $f_{REF} < 500\text{MHz}$ | 305 | 385 | 454 | mV |
| | | Output = 500mV, $R_{OUT} = 100\Omega$ $f_{REF} < 2\text{GHz}$ | 350 | 500 | 650 | mV |
| | | Output = 500mV, $R_{OUT} = 100\Omega$ $f_{REF} < 500\text{MHz}$ | 450 | 550 | 650 | mV |

Table 3. AC Characteristics ^[1] (Cont.)

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|-----------------|--|-----------------|---------|---------|---------|------|
| V _{OS} | Offset Voltage, V _{DD} ^[2] = 1.8V ±5% | Output = 350mV | 0.61 | 0.77 | 0.91 | V |
| | | Output = 500mV | 0.53 | 0.68 | 0.82 | V |
| | Offset Voltage, V _{DD} ^[2] = 2.1V | Output = 350mV | 0.80 | 1.01 | 1.20 | V |
| | | Output = 500mV | 0.74 | 0.95 | 1.15 | V |
| | Offset Voltage, V _{DD} ^[2] = 2.3V | Output = 350mV | 1.00 | 1.21 | 1.42 | V |
| | | Output = 500mV | 0.95 | 1.15 | 1.36 | V |
| | Offset Voltage, V _{DD} ^[2] = 2.5V | Output = 350mV | 1.30 | 1.45 | 1.62 | V |
| | | Output = 500mV | 1.20 | 1.35 | 1.55 | V |
| | Offset Voltage, V _{DD} ^[2] = 2.7V | Output = 350mV | 1.40 | 1.61 | 1.82 | V |
| | | Output = 500mV | 1.34 | 1.55 | 1.75 | V |

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Input V_{PP} = 400mV.

4. Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise*. This value is normally expressed using a phase noise plot, and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm), or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

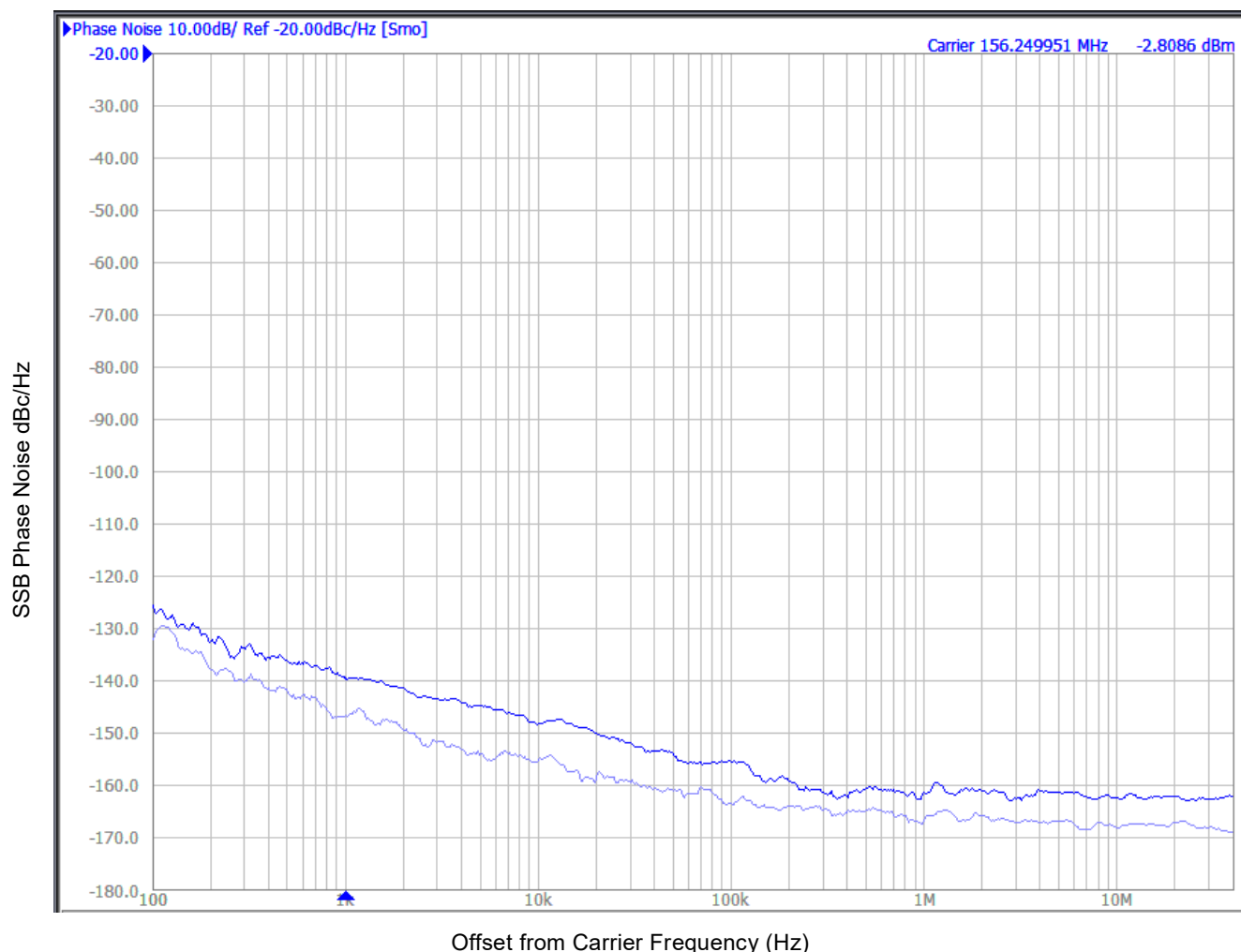


Figure 4. Additive Phase Jitter. Frequency: 156.25MHz, Integration Range: 12kHz to 20MHz = 45fs Typical

As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

Note: The phase noise plot was measured using a Wenzel 156.25MHz Oscillator as the input source.

5. Applications Information

5.1 Fail-Safe Operation

All clock inputs support fail-safe operation. That is, when the device is powered down, the clock inputs can be held at a DC voltage of up to 4.6V without damaging the device or the input pins.

5.2 Recommendations for Unused Input and Output Pins

5.2.1 Inputs

5.2.1.1 CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from CLK to ground.

5.2.2 Outputs

5.2.2.1 LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 Ω across. If they are left floating there should be no trace attached.

5.2.2.2 VREFX

The unused VREFA and VREFB pins can be left floating. We recommend that there is no trace attached.

5.3 Wiring the Differential Input to Accept Single-Ended Levels

Figure 5 shows an example of how a differential input can be wired to accept single-ended levels. To satisfy the V_{CMR} requirement, the reference voltage V1 is set to 1.2V which is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V1 to meet the V_{CMR} requirement. For example, if the input clock swing is 1.8V and $V_{DD} = 1.8V$, the R1 and R2 values should be adjusted to set V1 at 1.2V in this example.

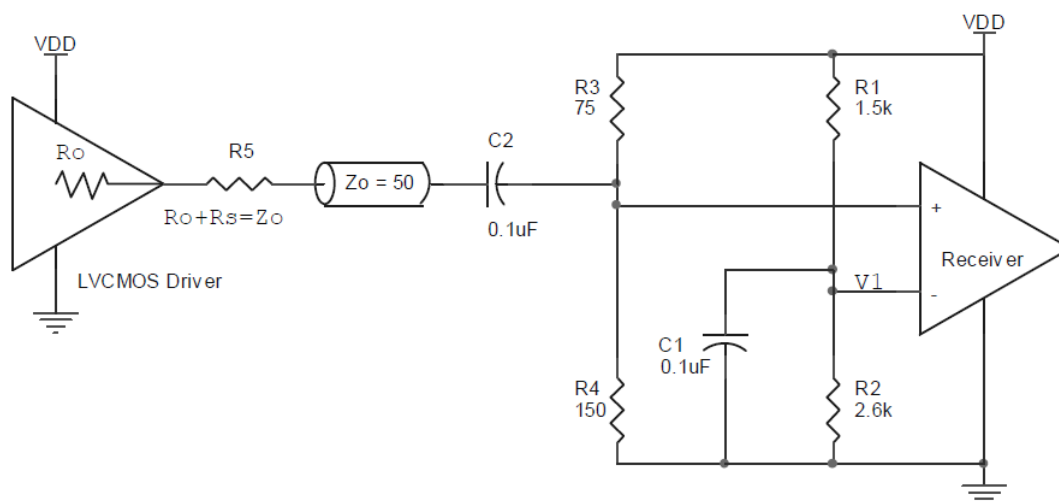


Figure 5. Example Schematic for Wiring a Differential Input to Accept Single-ended Levels

The values in the figure are for when both the single-ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R_3 and R_4 in parallel should equal the transmission line impedance and the signal DC offset after AC coupling should be equal to V_1 (in other words, 1.2V in this example). For most $Z_o = 50\Omega$ applications, $R_3 = 75\Omega$ and R_4 can be 130Ω . By keeping the same R_3/R_4 ratio, the values of the resistors can be increased to reduce the loading for a slower or weaker LVCMOS driver.

When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the input can handle larger amplitude signaling, it is recommended that the amplitude be reduced. For single-ended applications, the swing can be larger. Make sure the single-ended logic high and logic low signal operates within the specification limit. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be used for debugging purposes. The datasheet specifications are characterized and confirmed by using a differential signal.

5.4 1.8V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, and other differential signals. The differential input signal must meet both the V_{PP} and V_{CMR} input requirements. Figure 6 to Figure 8 show interface examples for the CLK /nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

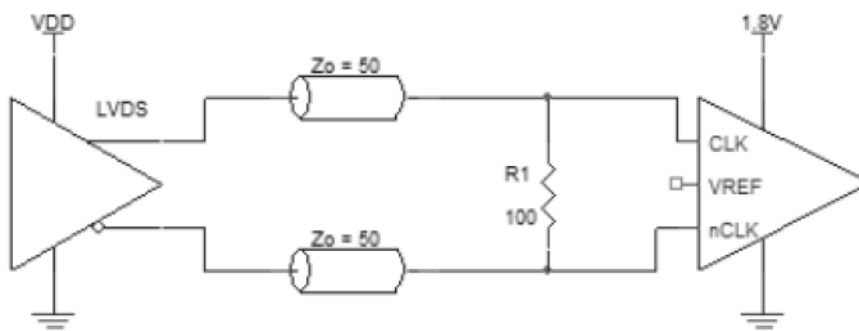


Figure 6. Differential Input Driven by an LVDS Driver – DC Coupling

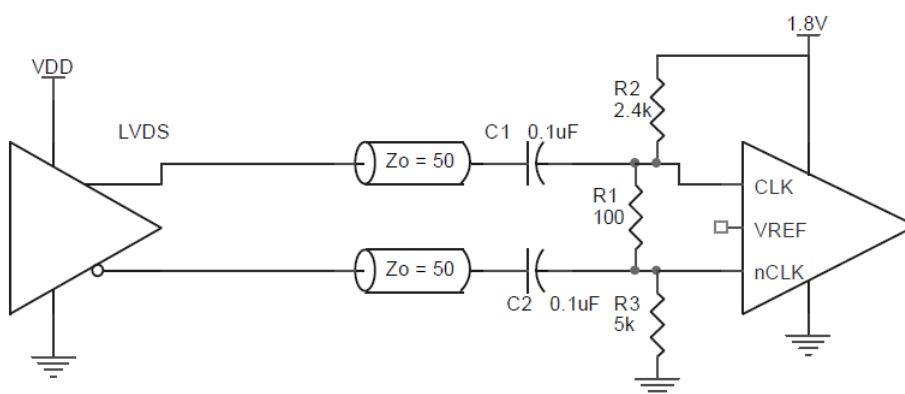


Figure 7. Differential Input Driven by an LVDS Driver – AC Coupling

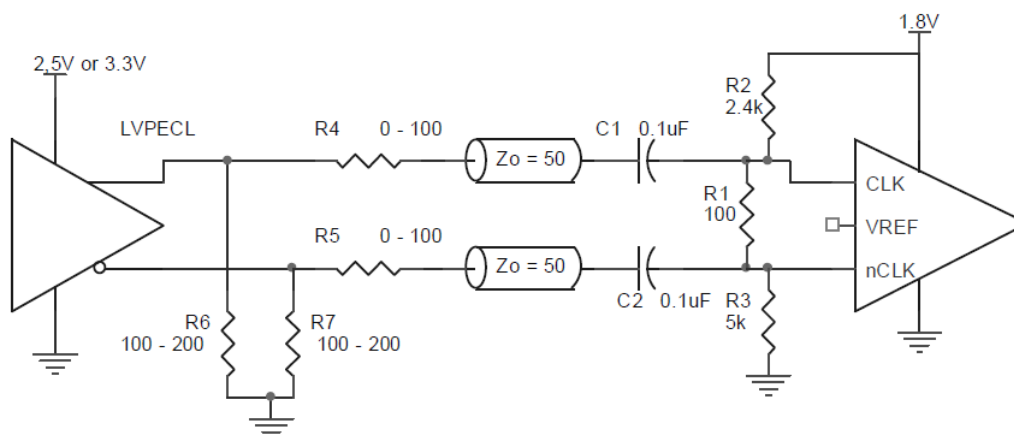


Figure 8. Differential Input Driven by an LVPECL Driver – AC Coupling

5.5 LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_O) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface-mounted and must be placed as close to the receiver as possible. Renesas offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source.

The standard termination schematic as shown in Figure 9 can be used with either type of output structure. Figure 10, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF . If using a non-standard termination, it is recommended to contact Renesas and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

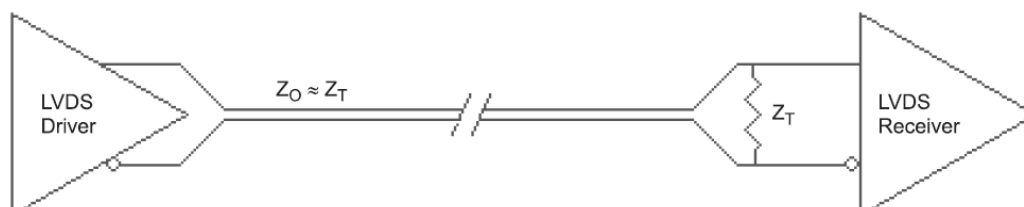


Figure 9. Standard LVDS Termination

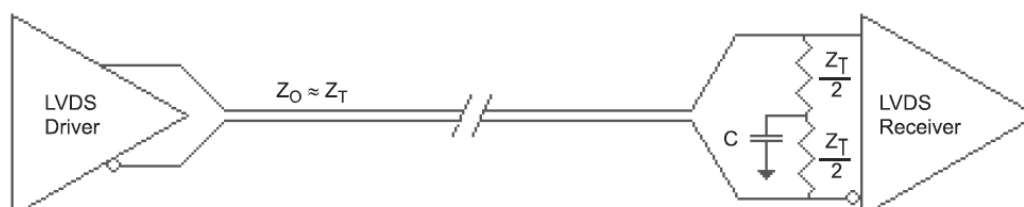
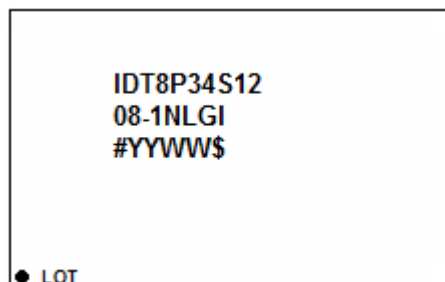


Figure 10. Optional LVDS Termination

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

7. Marking Diagram



- Lines 1 and 2: part number.
- Line 3:
 - “#” denotes stepping number.
 - “YYWW” denotes the last two digits of the year and work week that the part was assembled.
 - “\$” denotes the mark code.

8. Ordering Information

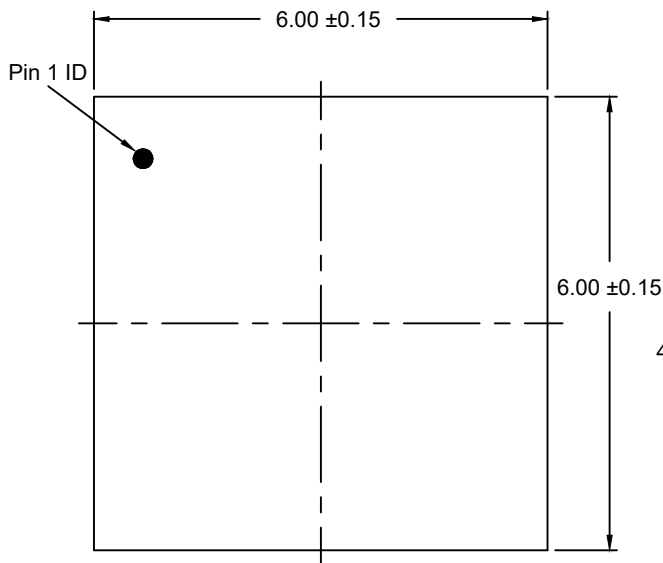
| Part Number | Package Description | Carrier Type | Temperature Range |
|-------------------|---|---|-------------------|
| 8P34S1208-1NLGI | 6.0 × 6.0 × 0.90 mm 40-VFQFPN | Tray | -40 to +85°C |
| 8P34S1208-1NLGI8 | | Tape and Reel, Pin 1 Orientation: EIA-481-C (see Table 4) | |
| 8P34S1208-1NLGI/W | | Tape & Reel, Pin 1 Orientation: EIA-481-D/E (see Table 4) | |

Table 4. Pin 1 Orientation in Tape and Reel Packaging

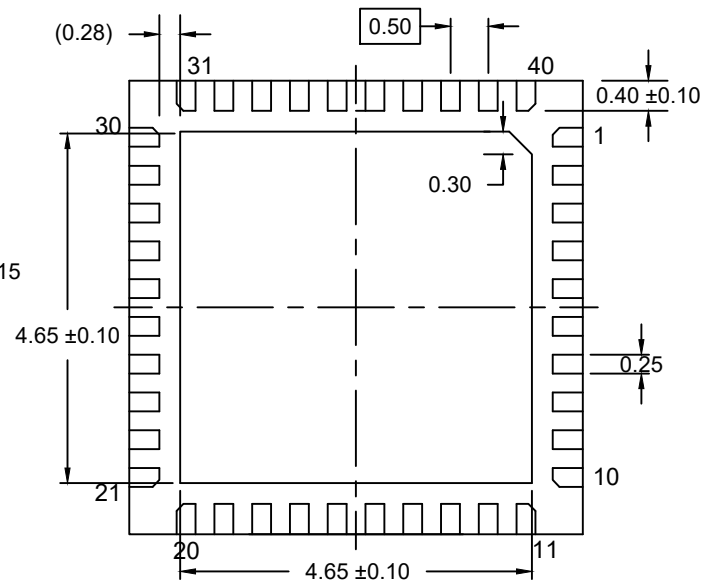
| Part Number Suffix | Pin 1 Orientation | Illustration |
|--------------------|--------------------------|---|
| 8 | Quadrant 1 (EIA-481-C) | <p>Correct PIN 1 ORIENTATION</p> <p>CARRIER TAPE TOPSIDE (Round Sprocket Holes)</p> <p>USER DIRECTION OF FEED</p> |
| /W | Quadrant 2 (EIA-481-D/E) | <p>Correct PIN 1 ORIENTATION</p> <p>CARRIER TAPE TOPSIDE (Round Sprocket Holes)</p> <p>USER DIRECTION OF FEED</p> |

9. Revision History

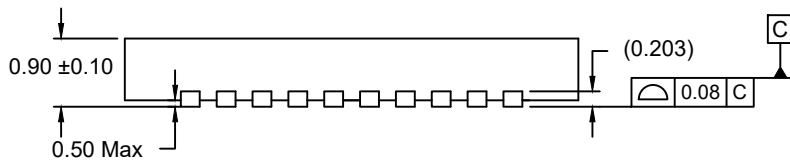
| Revision | Date | Description |
|----------|--------------|------------------|
| 1.00 | Jul 17, 2024 | Initial release. |



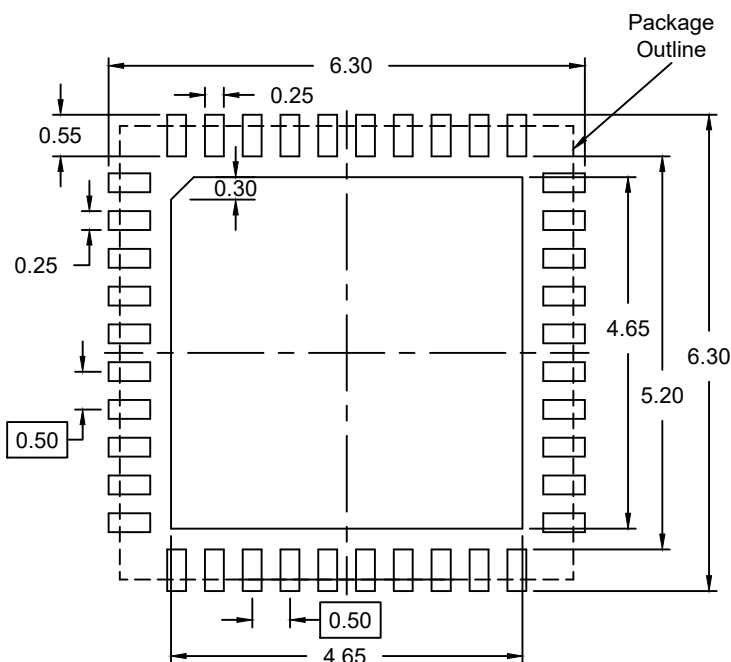
Top View



Bottom View



Side View



Recommended Land Pattern
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Number in () are for references only.

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