8P34S2108-1

Dual 1:8 LVDS Output 1.8V / 2.5V Fanout Buffer with OE/Swing Control

The 8P34S2108-1 is a differential dual 1:8 LVDS output 1.8V/2.5V fanout buffer that boasts high performance and low power consumption. It is engineered to support fail-safe operation and specifically designed for the fanout of high-frequency clock and data signals with very low additive phase-noise. The device comprises two independent buffer channels, and each of these channels has eight outputs with low skew. High isolation between the channels ensures minimal noise coupling.

The 8P34S2108-1 shines in clock distribution applications that require well-defined performance and repeatability due to its guaranteed output-to-output and part-to-part skew characteristics. The device can operate using a 1.8V or 2.5V power supply. Its integrated bias voltage references allow for the easy interfacing of AC-coupled signals with the device's inputs.

The 8P34S2108-1 had the individual OE / Swing control pin for each output, which provides the excellent control over both swing and output enable functions.

Features

- Dual 1:8 low skew, low additive jitter LVDS fanout buffers
- Individual OE / swing control pin for each output.
- Matched AC characteristics across both channels
- High isolation between channels
- Both differential CLKA, nCLKA and CLKB, nCLKB inputs accept LVDS, LVPECL, and single-ended LVCMOS levels
- Maximum input clock frequency of 2GHz
- Output amplitudes: 350mV, 500mV, or disable (selectable)
- Output skew: 20ps typical
- Low additive phase jitter, RMS: 50fs typical (f_{REF} = 156.25MHz, 12kHz–20MHz)
- Full 1.8V and 2.5V supply voltage mode
- Lead-free (RoHS 6), 64-lead VFQFPN packaging
- -40°C to +85°C ambient operating temperature
- Supports case temperature up to +105°C

Applications

- 4G and 5G RU and DU system
- Ethernet switches / routers
- Medical imaging
- Professional audio and video
- Data center and server

Contents

1. Overview

1.1 Block Diagram

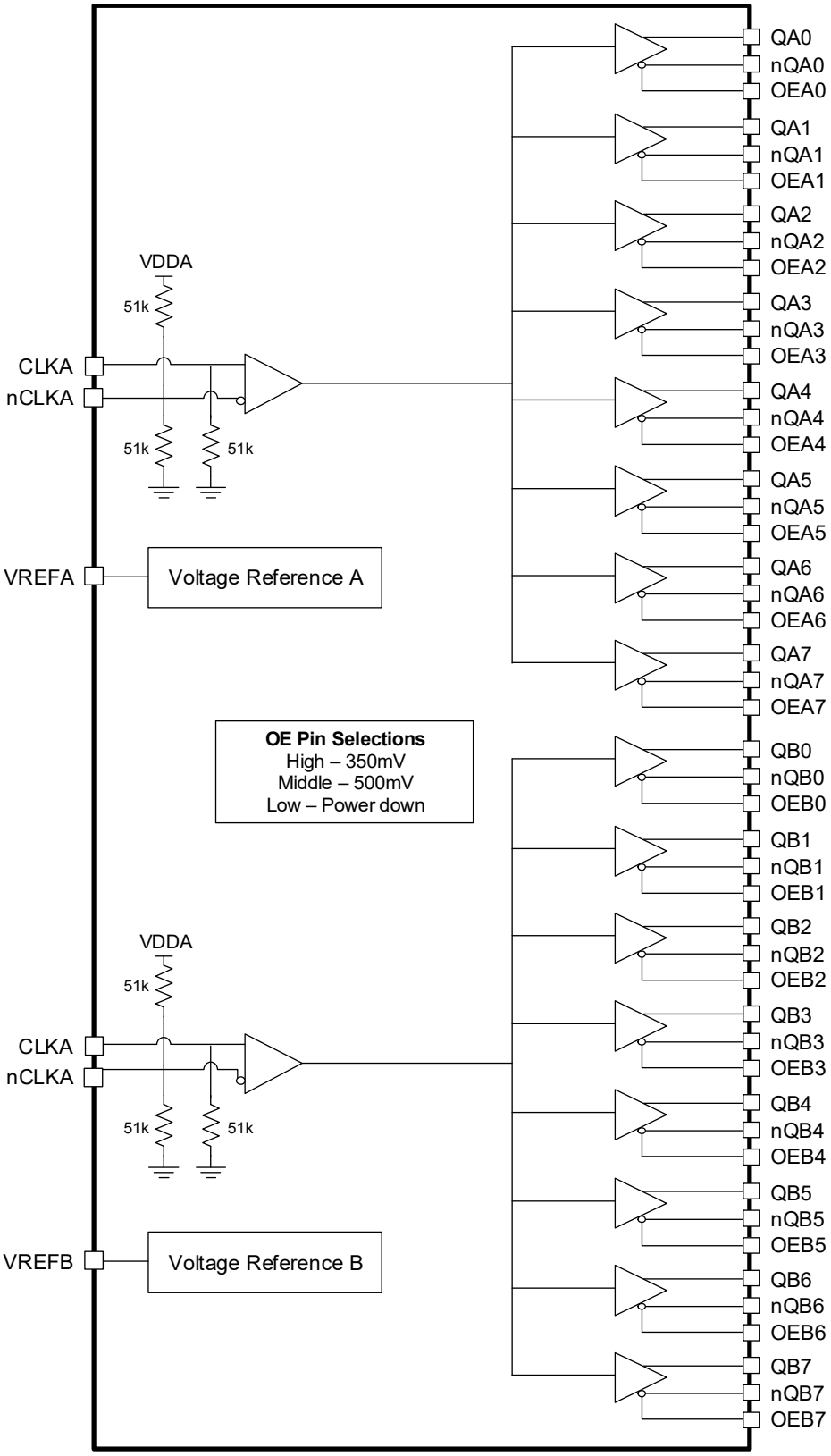


Figure 1. Block Diagram

2. Pin Information

2.1 Pin Assignments

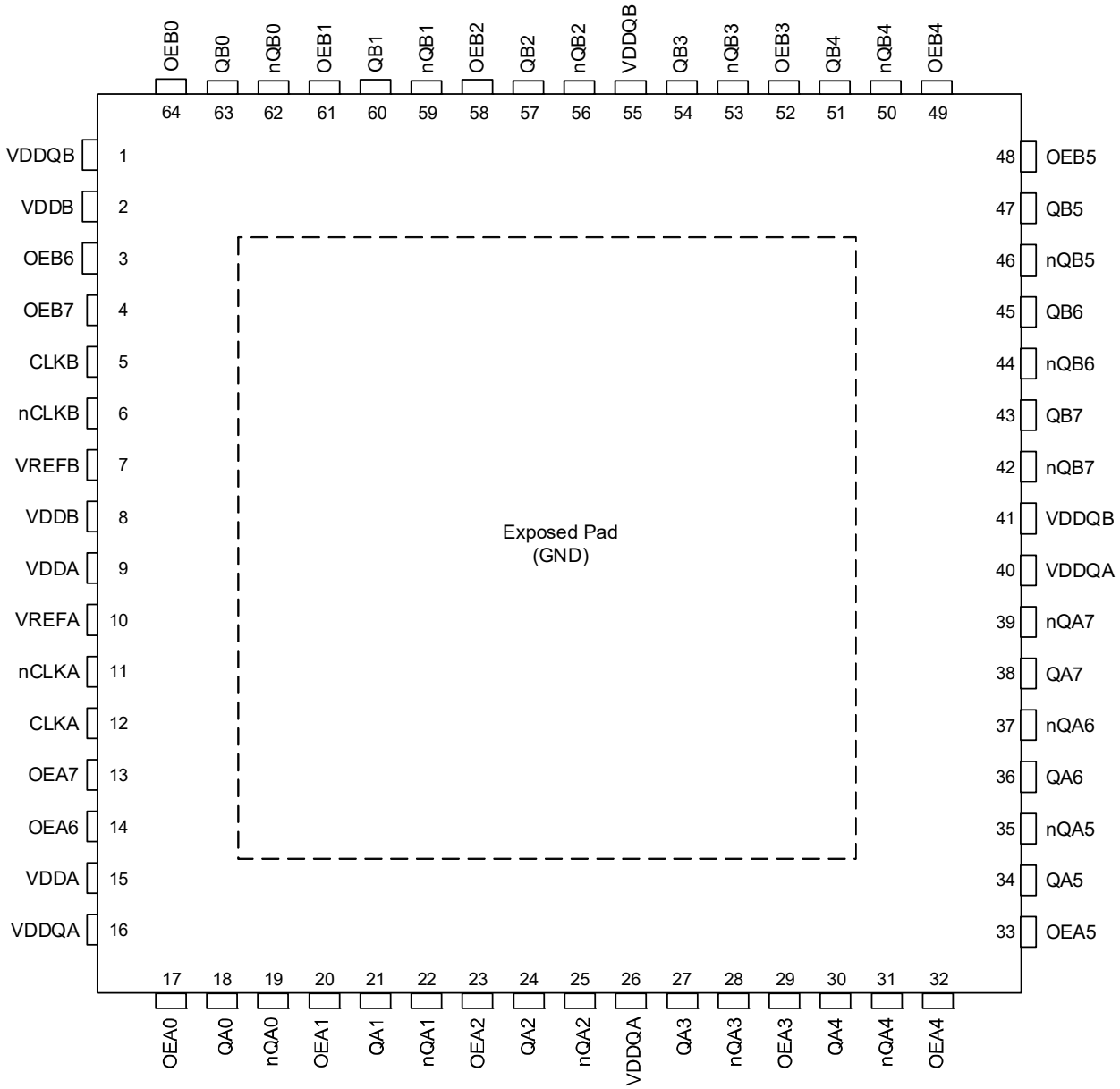


Figure 2. Pin Assignments – Top View

2.2 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Type	Description
1	VDDQB	Power	Power supply pin for the channel B outputs QB[0:7].
2	VDDB	Power	Power supply pins for the core and inputs of channel B.
3	OEB6	Input	Control output enables and swing for QB6. LVCMOS/TTL input levels.
4	OEB7	Input	Control output enables and swing for QB7. LVCMOS/TTL input levels.

Table 1. Pin Descriptions (Cont.)

Pin Number	Pin Name	Type	Description
5	CLKB	Input (PD)	Non-inverting differential clock/data input for channel B.
6	nCLKB	Input (PD/PU)	Inverting differential clock/data input for channel B.
7	VREFB	Power	Bias voltage reference for the CLKB, nCLKB input pairs.
8	VDDB	Power	Power supply pins for the core and inputs of channel B.
9	VDDA	Power	Power supply pins for the core and inputs of channel A.
10	VREFA	Power	Bias voltage reference for the CLKA, nCLKA input pairs.
11	nCLKA	Input (PD/PU)	Inverting differential clock/data input for channel A.
12	CLKA	Input (PD)	Non-inverting differential clock/data input for channel A.
13	OEA7	Input	Control output enables and swing for QA7. LVCMOS/TTL input levels.
14	OEA6	Input	Control output enables and swing for QA6. LVCMOS/TTL input levels.
15	VDDA	Power	Power supply pins for the core and inputs of channel A.
16	VDDQA	Power	Power supply pin for the channel A outputs QA[0:7].
17	OEA0	Input	Control output enables and swing for QA0. LVCMOS/TTL input levels.
18	QA0	Output	Differential output pair A0. LVDS interface levels.
19	nQA0	Output	Differential output pair A0. LVDS interface levels.
20	OEA1	Input	Control output enables and swing for QA1. LVCMOS/TTL input levels.
21	QA1	Output	Differential output pair A1. LVDS interface levels.
22	nQA1	Output	Differential output pair A1. LVDS interface levels.
23	OEA2	Input	Control output enables and swing for QA2. LVCMOS/TTL input levels.
24	QA2	Output	Differential output pair A2. LVDS interface levels.
25	nQA2	Output	Differential output pair A2. LVDS interface levels.
26	VDDQA	Power	Power supply pin for the channel A outputs QA[0:7].
27	QA3	Output	Differential output pair A3. LVDS interface levels.
28	nQA3	Output	Differential output pair A3. LVDS interface levels.
29	OEA3	Input	Control output enables and swing for QA3. LVCMOS/TTL input levels.
30	QA4	Output	Differential output pair A4. LVDS interface levels.
31	nQA4	Output	Differential output pair A4. LVDS interface levels.
32	OEA4	Input	Control output enables and swing for QA4. LVCMOS/TTL input levels.
33	OEA5	Input	Control output enables and swing for QA5. LVCMOS/TTL input levels.
34	QA5	Output	Differential output pair A5. LVDS interface levels.
35	nQA5	Output	Differential output pair A5. LVDS interface levels.
36	QA6	Output	Differential output pair A6. LVDS interface levels.
37	nQA6	Output	Differential output pair A6. LVDS interface levels.
38	QA7	Output	Differential output pair A7. LVDS interface levels.
39	nQA7	Output	Differential output pair A7. LVDS interface levels.
40	VDDQA	Power	Power supply pin for the channel A outputs QA[0:7].
41	VDDQB	Power	Power supply pin for the channel B outputs QB[0:7].

Table 1. Pin Descriptions (Cont.)

Pin Number	Pin Name	Type	Description
42	nQB7	Output	Differential output pair B7. LVDS interface levels.
43	QB7	Output	Differential output pair B7. LVDS interface levels.
44	nQB6	Output	Differential output pair B6. LVDS interface levels.
45	QB6	Output	Differential output pair B6. LVDS interface levels.
46	nQB5	Output	Differential output pair B5. LVDS interface levels.
47	QB5	Output	Differential output pair B5. LVDS interface levels.
48	OEB5	Input	Control output enables and swing for QB5. LVCMOS/TTL input levels.
49	OEB4	Input	Control output enables and swing for QB4. LVCMOS/TTL input levels.
50	nQB4	Output	Differential output pair B4. LVDS interface levels.
51	QB4	Output	Differential output pair B4. LVDS interface levels.
52	OEB3	Input	Control output enables and swing for QB3. LVCMOS/TTL input levels.
53	nQB3	Output	Differential output pair B3. LVDS interface levels.
54	QB3	Output	Differential output pair B3. LVDS interface levels.
55	VDDQB	Power	Power supply pin for the channel B outputs QB[0:7].
56	nQB2	Output	Differential output pair B2. LVDS interface levels.
57	QB2	Output	Differential output pair B2. LVDS interface levels.
58	OEB2	Input	Control output enables and swing for QB2. LVCMOS/TTL input levels.
59	nQB1	Output	Differential output pair B1. LVDS interface levels.
60	QB1	Output	Differential output pair B1. LVDS interface levels.
61	OEB1	Input	Control output enables and swing for QB1. LVCMOS/TTL input levels.
62	nQB0	Output	Differential output pair B0. LVDS interface levels.
63	QB0	Output	Differential output pair B0. LVDS interface levels.
64	OEB0	Input	Control output enables and swing for QB0. LVCMOS/TTL input levels.
-	ePAD	Power	EPAD connect to GND.

2.3 OE Output Amplitude Selection (Static Control)

Table 2. OE Output Amplitude Selection (Static Control)

OE Pin	QA and QB Output Amplitude (mV)
1	350
Float (default)	500
0	Disable (power-down)

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Figure 3. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{DD}	-	4.6	V
Input, V_I	-0.5	4.6	V
Input, I_I	-	20m	A
Outputs, I_O Continuous Current Surge Current	 - -	 10 15	mA
Input Sink/Source, I_{REF}	-	±2	mA
Maximum Junction Temperature, T_{JMAX}	-	125	°C
Storage Temperature, T_{STG}	-65	150	°C
ESD - Human Body Model	-	2000	V
ESD - Charged Device Model	-	1500	V

3.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions [1][2]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T_J	Maximum Junction Temperature	-	-	-	125	°C
T_A	Ambient Operating Temperature	-	-40	-	85	°C
V_{DDx}	Supply Voltage with Respect to Ground	Any V_{DD} pin, 1.8V supply	1.71	1.8	1.89	V
		Any V_{DD} pin, 2.5V supply	2.1	2.5	2.7	V

1. All electrical characteristics are specified over Recommended Operating Conditions unless noted otherwise.
2. All conditions in this table must be met to guarantee device functionality and performance.

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	64-VFQFPN, 9.0 × 9.0 mm	θ_{JA0}	Junction to ambient, still air	22	°C/W
		θ_{JA1}	Junction to ambient, 1 m/s air flow	19	°C/W
		θ_{JA2}	Junction to ambient, 2 m/s air flow	17	°C/W
		θ_{JB}	Junction to board	1.4	°C/W
		θ_{JC}	Junction to case	12.8	°C/W

3.4 DC Input Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
C_{IN}	Input Capacitance	-	-	2	-	pF
$R_{PULLDOWN}$	Input Pull-down Resistor	-	-	51	-	k ohms
R_{PULLUP}	Input Pull-up Resistor	-	-	51	-	k ohms

3.5 Power Supply DC Characteristics

V_{DD} = 1.8V ± 5%, T_A = -40ºC to 85ºC

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{DD}	Power Supply Voltage	-	1.71	1.8	1.89	V
I_{DD}	Power Supply Current	All QA, QB output terminated 100 ohm. Output swing is 500mV	-	404	515	mA
I_{DD}	Power Supply Current	All QA, QB output terminated 100 ohm. Output swing is 350mV	-	300	380	mA
I_{DD}	Power Supply Current	All QA, QB output disabled.	-	95	125	mA

3.6 Power Supply DC Characteristics

V_{DD} = 2.1V to 2.7V, T_A = -40ºC to 85ºC

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{DD}	Power Supply Voltage	-	2.1	2.5	2.7	V
I_{DD}	Power Supply Current	All QA, QB output terminated 100 ohm. Output swing is 500mV	-	420	530	mA
I_{DD}	Power Supply Current	All QA, QB output terminated 100 ohm. Output swing is 350mV	-	310	390	mA
I_{DD}	Power Supply Current	All QA, QB output disabled.	-	113	145	mA

3.7 LVCMOS/LVTTL Input DC Characteristics

V_{DD} = 1.8V ± 5%, 2.1V to 2.7V, T_A = -40ºC to 85ºC.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage	V_{DD} = 1.89V, 2.7V	0.75 × V_{DD}	-	V_{DD}+ 0.3	V
V_{IM}	Input Middle Voltage	V_{DD} = 1.89V, 2.7V	0.45 × V_{DD}	-	0.55 × V_{DD}	V
V_{IL}	Input Low Voltage	V_{DD} = 1.89V, 2.7V	-0.3	-	0.25 × V_{DD}	V
I_{IH}	Input High Current, OEx	V_{DD} = V_{IN} = 1.89V, 2.7V	-	-	150	µA
I_{IL}	Input Low Current, OEx	V_{DD} = 1.89V, 2.7V, V_{IN} = 0V	-10	-	-	µA
I_{LEAK}	Input Leakage Current, OEx	V_{IN} = 2.7V, V_{DD} = 0V	-	-	250	µA

3.8 Differential Input Characteristics

V_{DD} = 1.8V ± 5%, 2.1V to 2.7V, T_A = -40ºC to 85ºC.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_{IH}	Input High Current CLKA, nCLKA; CLKB, nCLKB	$V_{DD} = V_{IN}$ = 1.89V, 2.7V	-	-	150	µA
I_{IL}	Input Low Current CLKA, CLKB	V_{IN} = 0V, V_{DD} = 1.89V, 2.7V	-150	-	-	µA
	Input Low Current nCLKA, nCLKB	V_{IN} = 0V, V_{DD} = 1.89V, 2.7V	-150	-	-	µA
I_{LEAK}	Input Leakage Current	V_{IN} = 2.7V, V_{DD} = 0V	-	-	250	µA
V_{REF}	Reference Voltage for Input Bias	I_{REF} = -100µA; V_{DD} = 1.8V, 2.5V	0.7 × V_{DD}	-	0.85 × V_{DD}	V
V_{PP}	Peak-to-peak Voltage	V_{DD} = 1.89V, 2.7V	0.2	-	1	V
V_{CMR}	Common Mode Input Voltage	-	0.9	-	V_{DD} -($V_{PP/2}$)	V

3.9 LVDS AC and DC Characteristics

V_{DD} = 1.8V ± 5%, 2.1V to 2.7V, T_A = -40ºC to 85ºC.

Symbol	Parameter [1]	Test Conditions	Minimum	Typical	Maximum	Unit
deltaV_{OD}	VOD Magnitude Change	-	-	-	50	mV
deltaV_{OD}	VOD Magnitude Change	-	-	-	50	mV
V_{OD}	Differential Output Voltage	Output = 350mV, f_{REF} < 1.5GHz	247	350	454	mV
		Output = 500mV, f_{REF} < 1.5GHz	350	500	650	mV

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

3.10 AC Characteristics

V_{DD} = 1.8V ± 5% or 2.1 to 2.7V, T_A = -40ºC to 85ºC

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Unit
F_{REF}	Input Frequency	-		0	-	2	GHz
dV/dt	Input Edge Rate	-		1.5	-	-	V/ns
t_{PD}	Propagation Delay	CLK[0:1], nCLK[0:1] to any Qx, nQx		100	300	425	ps
tsk(o)	Output Skew	-		-	20	45	ps
tsk(p)	Pulse Skew	f_{REF} = 100MHz		-	-	30	ps
tsk(pp)	Part-to-part Skew	-		-	-	200	ps
t_{jit}	Buffer Additive Phase Jitter, RMS	f_{REF} = 122.88MHz Square Wave, V_{PP} = 1V, Integration Range: 12kHz to 20MHz		-	50	-	fs
		f_{REF} = 156.25MHz Square Wave, V_{PP} = 1V, Integration Range: 12kHz to 20MHz		-	50	-	fs
		f_{REF} = 156.25MHz Square Wave, V_{PP} = 0.5V, Integration Range: 12kHz to 20MHz		-	50	-	fs
PNF	Phase noise floor	Phase noise floor carrier frequency at 122.88MHz at 20MHz offset		-	-160	-	dBc/Hz
t_R / t_F	Output Rise/ Fall Time	V_{DD} = 1.8V ±5%, outputs loaded with 100ohm	10% to 90%	-	150	400	ps
			20% to 80%	-	90	160	ps
		V_{DD} = 2.1V, 2.5V, 2.7V, outputs loaded with 100ohm	10% to 90%	-	200	420	ps
			20% to 80%	-	110	190	ps
$MUX_{isolation}$	Mux Isolation	f_{REF} = 100MHz		-	80	-	dB

4. Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise.* This value is normally expressed using a phase noise plot, and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm), or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

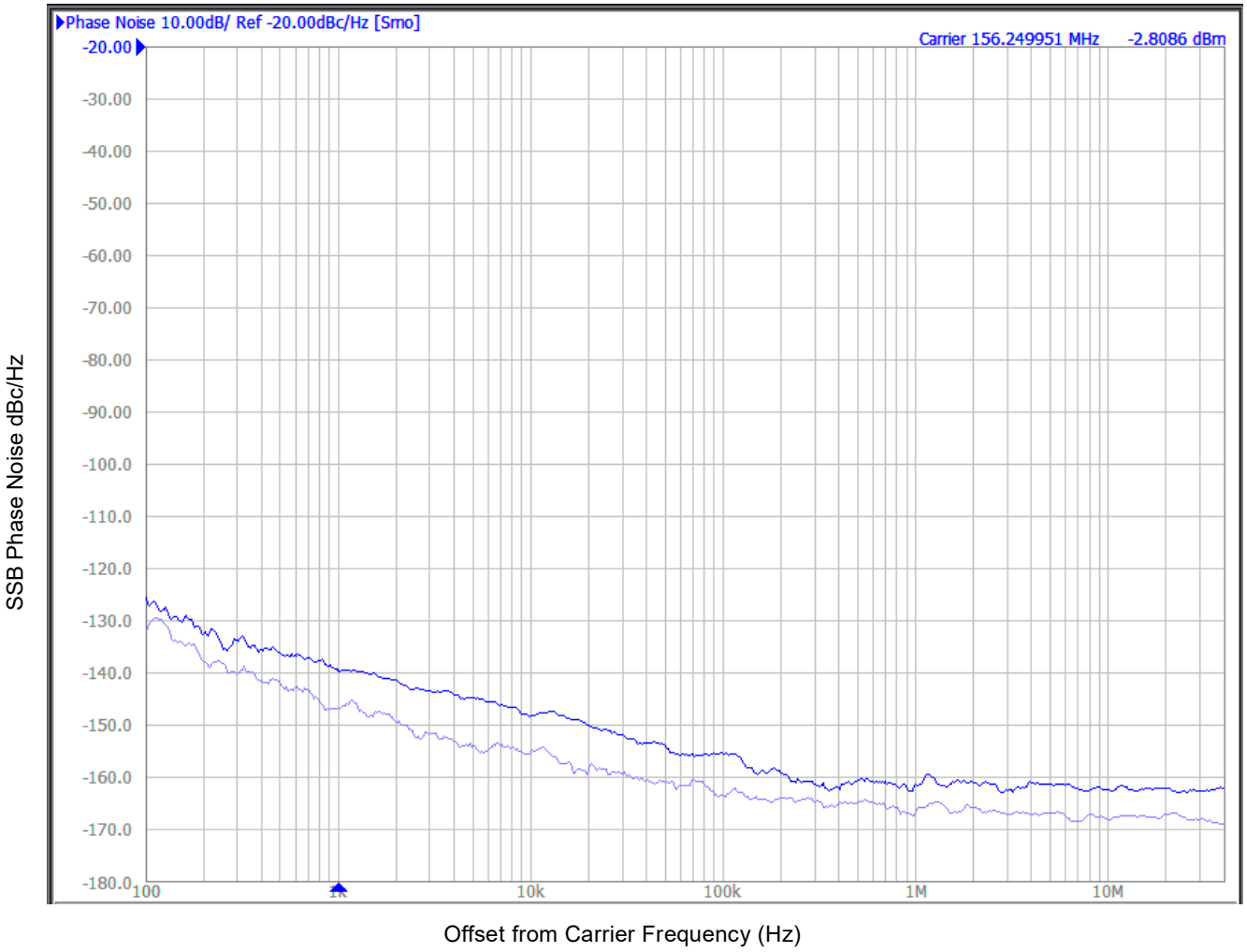


Figure 4. Additive Phase Jitter. Frequency: 156.25MHz, Integration Range: 12kHz to 20MHz = 45fs Typical

As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

Note: The phase noise plot was measured using a Wenzel 156.25MHz Oscillator as the input source.

5. Applications Information

5.1 Fail-Safe Operation

All clock inputs support fail-safe operation. That is, when the device is powered down, the clock inputs can be held at a DC voltage of up to 4.6V without damaging the device or the input pins.

5.2 Recommendations for Unused Input and Output Pins

5.2.1 Inputs

5.2.1.1 CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

5.2.2 Outputs

5.2.2.1 LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

5.2.2.2 VREFX

The unused VREFA and VREFB pins can be left floating. We recommend that there is no trace attached.

5.3 Wiring the Differential Input to Accept Single-Ended Levels

Figure 5 shows an example of how a differential input can be wired to accept single-ended levels. To satisfy the V_{CMR} requirement, the reference voltage V1 is set to 1.2V which is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V1 to meet the V_{CMR} requirement. For example, if the input clock swing is 1.8V and V_{DD} = 1.8V, the R1 and R2 values should be adjusted to set V1 at 1.2V in this example.

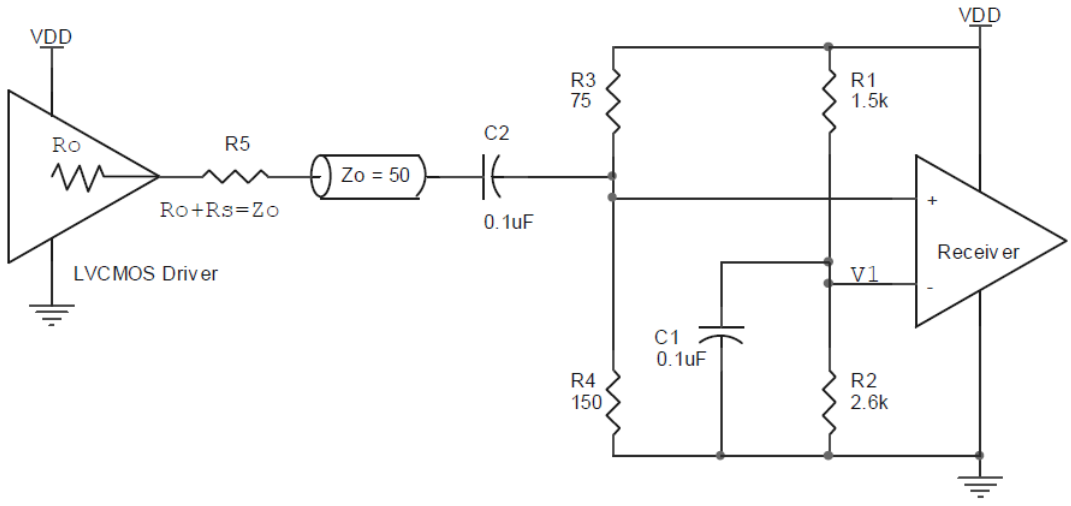


Figure 5. Example Schematic for Wiring a Differential Input to Accept Single-ended Levels

The values in the figure are for when both the single-ended swing and VDD are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_O) and the series resistance (R_S) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line

impedance and the signal DC offset after AC coupling should be equal to V1 (in other words, 1.2V in this example). For most Z_O = 50Ω applications, R3 = 75Ω and R4 can be 130Ω. By keeping the same R3/R4 ratio, the values of the resistors can be increased to reduce the loading for a slower or weaker LVCMOS driver.

When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the input can handle larger amplitude signaling, it is recommended that the amplitude be reduced. For single-ended applications, the swing can be larger. Make sure the single-ended logic high and logic low signal operates within the specification limit. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be used for debugging purposes. The datasheet specifications are characterized and confirmed by using a differential signal.

5.4 1.8V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, and other differential signals. The differential input signal must meet both the V_{PP} and V_{CMR} input requirements. Figure 6 to Figure 8 show interface examples for the CLK /nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Consult with the vendor of the driver component to confirm the driver termination requirements.

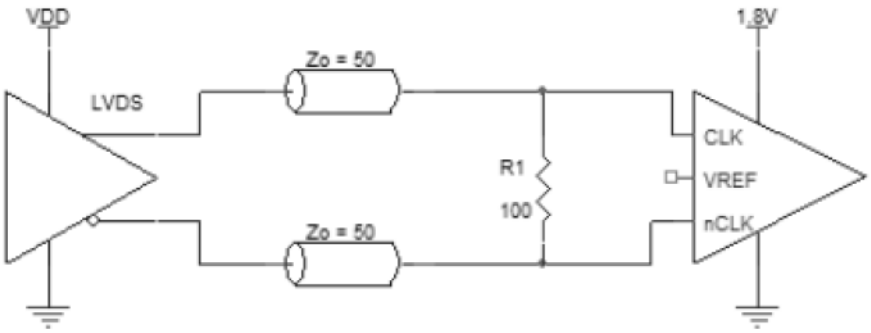


Figure 6. Differential Input Driven by an LVDS Driver – DC Coupling

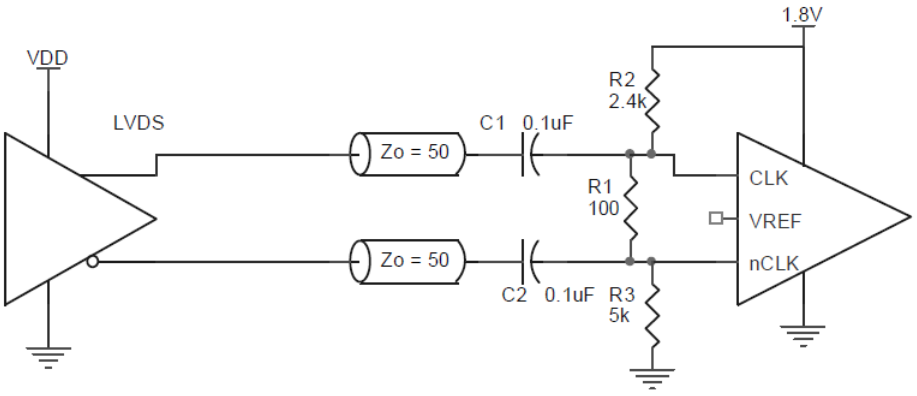


Figure 7. Differential Input Driven by an LVDS Driver – AC Coupling

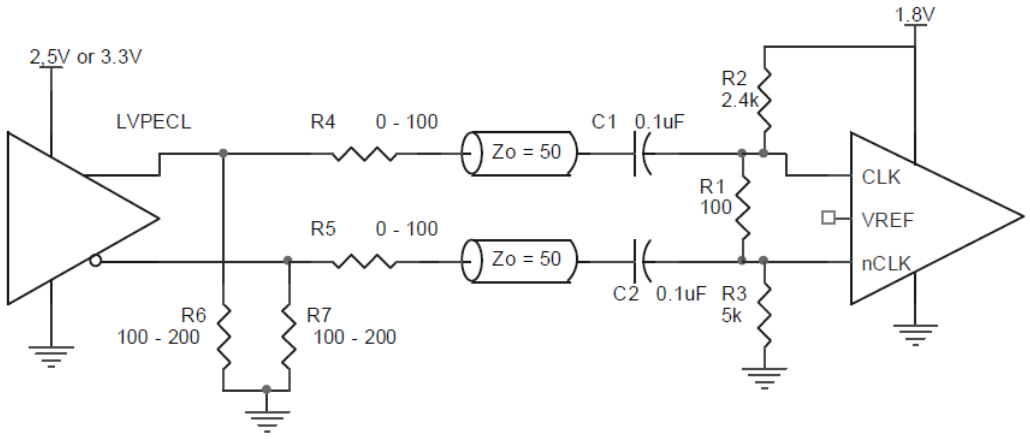


Figure 8. Differential Input Driven by an LVPECL Driver – AC Coupling

5.5 LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_O) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface-mounted and must be placed as close to the receiver as possible. Renesas offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source.

The standard termination schematic as shown in Figure 9 can be used with either type of output structure. Figure 10, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact Renesas and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

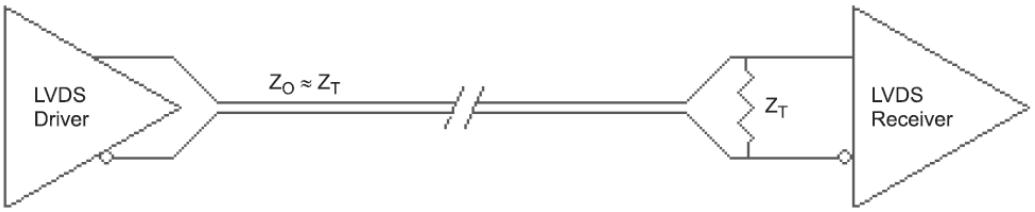


Figure 9. Standard LVDS Termination

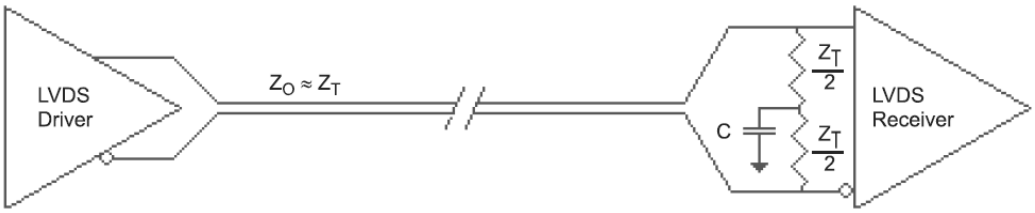
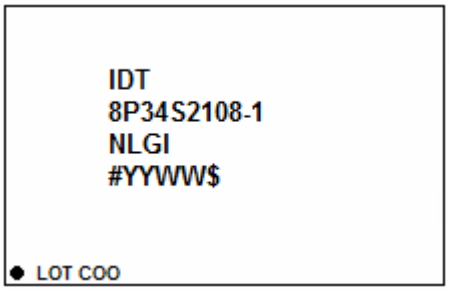


Figure 10. Optional LVDS Termination

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

7. Marking Diagram

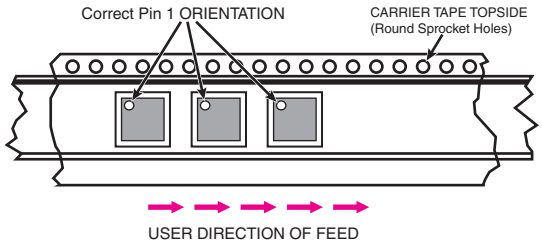
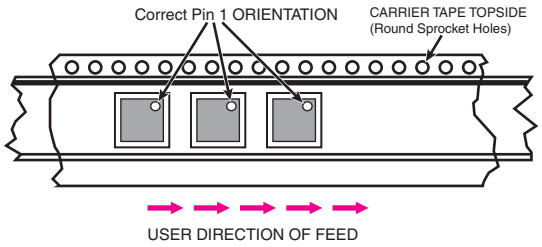


- Lines 2 and 3: part number.
- Line 4:
  - "#" denotes the stepping number.
  - "YYWW" denotes the last two digits of the year and workweek that the part was assembled.
  - "$" denotes the lot sequence.
- "LOT" denotes the lot number.
- "COO" denotes country of origin.

8. Ordering Information

Part Number	Package Description	Carrier Type	Temperature Range
8P34S2108-1NLGI	9.0 × 9.0 × 0.9 mm 64-VFQFPN	Tray	-40 to +85°C
8P34S2108-1NLGI8		Tape and Reel, Pin 1 Orientation: EIA-481-C (see Table 4)	-40 to +85°C
8P34S2108-1NLGI/W	9.0 × 9.0 × 0.9 mm 64-VFQFPN	Tape and Reel, Pin 1 Orientation: EIA-481-D (see Table 4)	-40 to +85°C

Table 4. Pin 1 Orientation in Tape and Reel Packaging

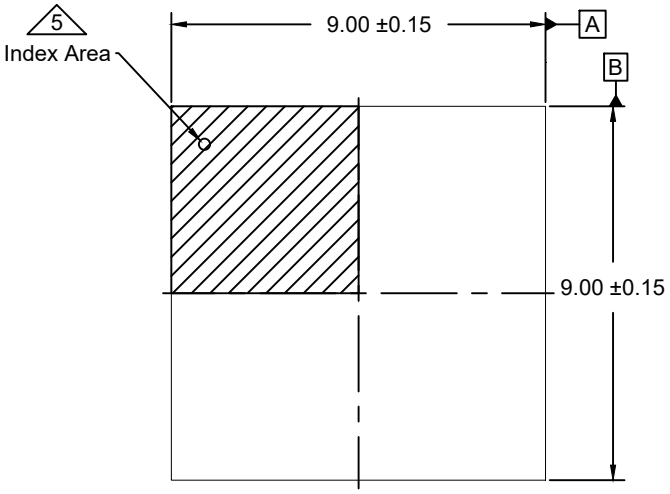
Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

9. Revision History

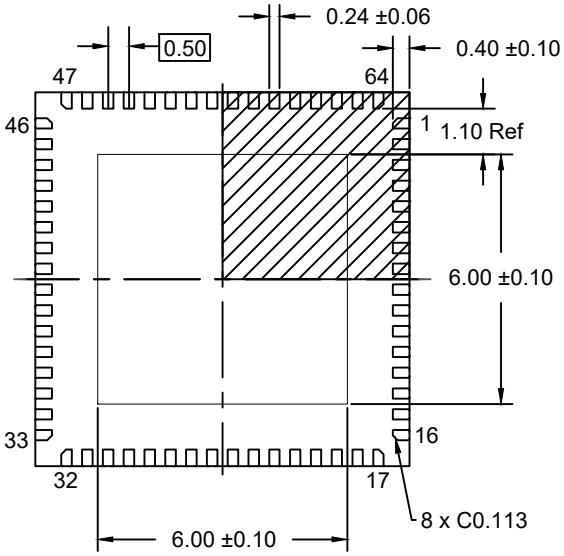
Revision	Date	Description
1.00	Jul 31, 2024	Initial release.

Package Outline Drawing

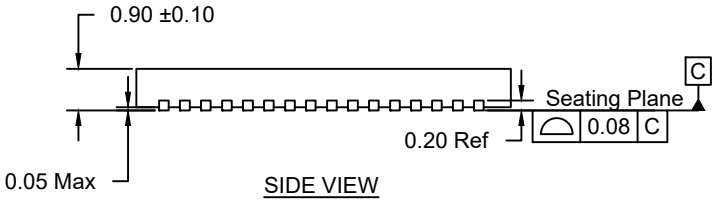
PSC-4147-05
NLG64P5
64-VFQFPN 9.0 x 9.0 x 0.9 mm Body, 0.50mm Pitch
Rev.07, Nov 24, 2025



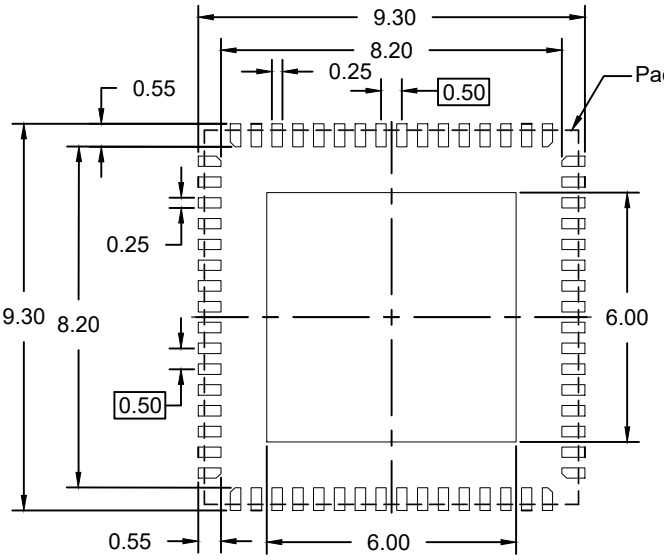
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Pin 1 Index ID is indicated with either exposed pad corner chamfer or half circled cut near the exposed pad corner.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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