

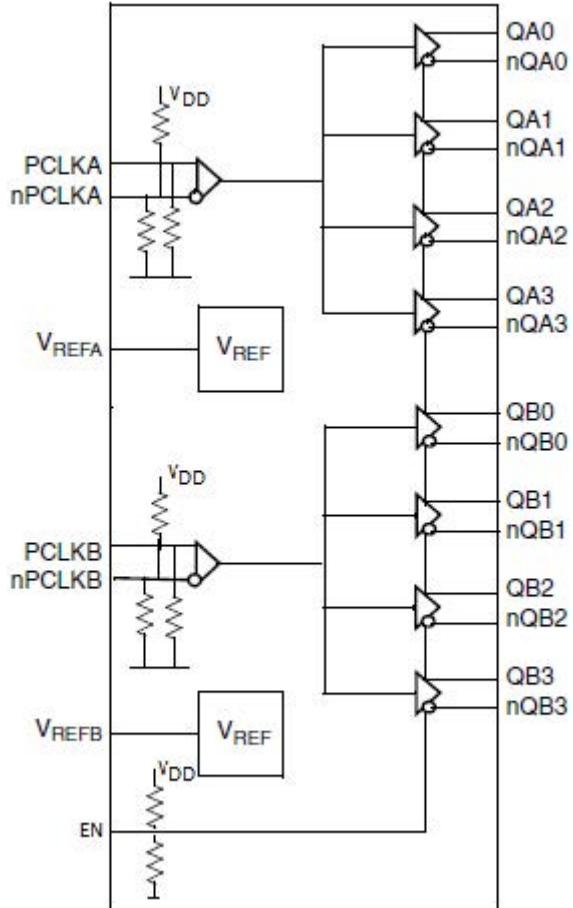
General Description

The 8SLVD2104 is a high-performance differential dual 1:4 LVDS fanout buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. The 8SLVD2104 is characterized to operate from a 2.5V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the 8SLVD2104 ideal for those clock distribution applications demanding well-defined performance and repeatability. Two independent buffers with four low skew outputs each are available. The integrated bias voltage generators enables easy interfacing of single-ended signals to the device inputs. The device is optimized for low power consumption and low additive phase noise.

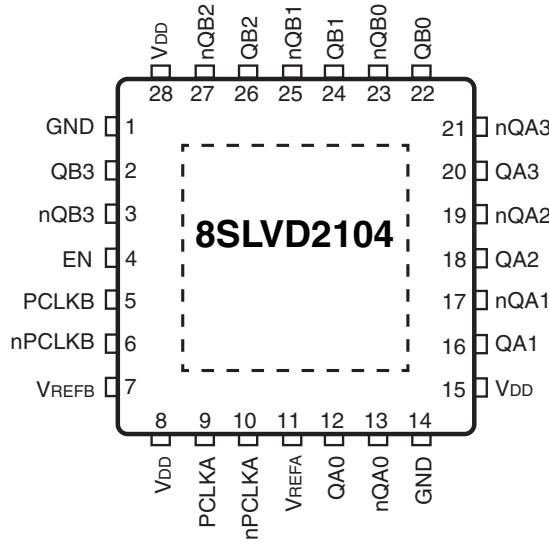
Features

- Two 1:4, low skew, low additive jitter LVDS fanout buffers
- Two differential clock inputs
- Differential pairs can accept the following differential input levels: LVDS and LVPECL
- Maximum input clock frequency: 2GHz
- Output bank skew: 35ps, (maximum)
- Propagation delay: 300ps, (maximum)
- Low additive RMS phase jitter, 156.25MHz (10kHz - 20MHz): 105fs, (maximum)
- 2.5V supply voltage
- Lead-free (RoHS 6) 28-Lead VFQFN package
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



28-Lead, 5mm x 5mm VFQFN

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions¹

| Number | Name | Type | | Description |
|--------|------------|--------|---------------------|---|
| 1 | GND | Power | | Power supply ground. |
| 2 | QB3 | Output | | Differential output pair B3. LVDS interface levels. |
| 3 | nQB3 | Output | | |
| 4 | EN | Input | Pullup/ Pulldown | Output enable pin. $V_{DD}/2$ default when left floating. |
| 5 | PCLKB | Input | Pulldown | Non-inverting differential clock/data input. |
| 6 | nPCLKB | Input | Pullup/ Pulldown | Inverting differential clock/data input. $V_{DD}/2$ default when left floating. |
| 7 | V_{REFB} | Output | | Bias voltage reference for the PCLKB, nPCLKB input pair. |
| 8 | V_{DD} | Power | | Power supply pin. |
| 9 | PCLKA | Input | Pulldown | Non-inverting differential clock/data input. |
| 10 | nPCLKA | Input | Pullup/ Pulldown | Inverting differential clock/data input. $V_{DD}/2$ default when left floating. |
| 11 | V_{REFA} | Output | | Bias voltage reference for the PCLKA, nPCLKA input pair. |
| 12 | QA0 | Output | | Differential output pair A0. LVDS interface levels. |
| 13 | nQA0 | Output | | |
| 14 | GND | Power | | Power supply ground. |
| 15 | V_{DD} | Power | | Power supply pin. |
| 16 | QA1 | Output | | Differential output pair A1. LVDS interface levels. |
| 17 | nQA1 | Output | | |
| 18 | QA2 | Output | | Differential output pair A2. LVDS interface levels. |
| 19 | nQA2 | Output | | |
| 20 | QA3 | Output | | Differential output pair A3. LVDS interface levels. |
| 21 | nQA3 | Output | | |
| 22 | QB0 | Output | | Differential output pair B0. LVDS interface levels. |
| 23 | nQB0 | Output | | |
| 24 | QB1 | Output | | Differential output pair B1. LVDS interface levels. |
| 25 | nQB1 | Output | | |
| 26 | QB2 | Output | | Differential output pair B2. LVDS interface levels. |
| 27 | nQB2 | Output | | |
| 28 | V_{DD} | Power | | Power supply pin. |
| | ePAD | | | Thermal pad. Connect to ground. |

NOTE 1: *Pulldown* and *Pullup* refer to internal input resistors. See [Table 2, Pin Characteristics](#), for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------|-------------------------|---------------------------------|---------|---------|---------|------------|
| C_{IN} | Input Capacitance | | | 2 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | EN, PCLK[A:B], nPCLK[A:B] | | 51 | | k Ω |
| R_{PULLUP} | Input Pullup Resistor | EN, nPCLK[A:B] | | 51 | | k Ω |

Function Table**Table 3. EN Input Selection Function Table¹**

| Input | Operation |
|----------|--|
| EN | |
| 0 (Low) | Outputs are disabled and static at $Q_x = 0$ (low level) and $nQ_x = 1$ (high level). |
| 1 (High) | Bank A outputs are enabled and Bank B outputs are disabled at the following static levels: $QB_x = 0$ (low level) and $nQB_x = 1$ (high level). |
| Open | All outputs enabled. |

NOTE 1: EN is an asynchronous control input pin.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the [DC Electrical Characteristics](#) or [AC Electrical Characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|--|--------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, I_O (LVDS) Continuous Current Surge Current | 10mA 15mA |
| Maximum Junction Temperature, $T_{J,MAX}$ | 125°C |
| Storage Temperature, T_{STG} | -65°C to 150°C |
| ESD - Human Body Model ¹ | 2000V |
| ESD - Charged Device Model ¹ | 1500V |

NOTE 1: According to JEDEC/JESD JS-001-2012/22-C101E.

DC Electrical Characteristics

Table 4A. Power Supply Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$ ¹

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|----------------------|--|---------|---------|---------|-------|
| V_{DD} | Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | All outputs terminated with 100Ω in between nQ_x , Q_x ; DC to 2GHz | | 145 | 170 | mA |

NOTE 1: Q_x , nQ_x denotes $QA[3:0]$, $nQA[3:30]$, and $QB[3:0]$, $nQB[3:0]$.

Table 4B. LVC MOS/LV TTL Input Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------|-----------------|-----------------------------------|----------------|----------------|---------|
| V_{MID} | Input Voltage - Open Pin | EN | Open | | $V_{DD} / 2$ | V |
| V_{IH} | Input High Voltage | EN | | $0.7 * V_{DD}$ | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | EN | | -0.3 | $0.2 * V_{DD}$ | V |
| I_{IH} | Input High Current | EN | $V_{DD} = V_{IN} = 2.625V$ | | 150 | μA |
| I_{IL} | Input Low Current | EN | $V_{DD} = 2.625V$, $V_{IN} = 0V$ | -150 | | μA |

Table 4C. Differential Input Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|---|------------------------------------|--------------------------------------|---------|---------------------|---------------|
| I_{IH} | Input High Current | $PCLKA, nPCLKA$ $PCLKB, nPCLKB$ | $V_{DD} = V_{IN} = 2.625V$ | | | 150 μA |
| I_{IL} | Input Low Current | $PCLKA, PCLKB$ | $V_{DD} = 2.625V, V_{IN} = 0V$ | -10 | | μA |
| | | $nPCLKA, nPCLKB$ | $V_{DD} = 2.625V, V_{IN} = 0V$ | -150 | | μA |
| V_{REFA}, V_{REFB} | Reference Voltages for Input Bias | | $V_{DD} = 2.5V; I_{REF} = +100\mu A$ | 1.0 | | 1.35 V |
| V_{PP} | Peak-to-Peak Voltage ¹ | $f_{REF} < 1.5$ GHz | 0.15 | | 1.6 | V |
| | | $f_{REF} > 1.5$ GHz | 0.2 | | 1.6 | V |
| V_{CMR} | Common Mode Input Voltage ^{1, 2} | | 1.0 | | $V_{DD} - V_{PP}/2$ | V |

NOTE 1: V_{IL} should not be less than -0.3V.

NOTE 2: Common mode input voltage is defined at the crosspoint.

Table 4D. LVDS Output DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$ ^{1, 2}

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| V_{OD} | Differential Output Voltage | | 247 | | 454 | mV |
| ΔV_{OD} | V_{OD} Magnitude Change | | | | 50 | mV |
| V_{OS} | Offset Voltage | | 1.0 | | 1.4 | V |
| ΔV_{OS} | V_{OS} Magnitude Change | | | | 50 | mV |

NOTE 1: Qx, nQx denotes QA[3:0], nQA[3:30], and QB[3:0], nQB[3:0].

NOTE 2: 100 Ω termination across differential outputs.

AC Electrical Characteristics

Table 5. AC Electrical Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$ ¹

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------|---|---|---------|---------|---------|-------|
| f_{REF} | Input Frequency | | | | 2 | GHz |
| $\Delta V/\Delta t$ | Input Edge Rate | | 0.75 | | | V/ns |
| t_{PD} | Propagation Delay ² | PCLKA, nPCLKA to QA[3:0], nQA[3:0] PCLKB, nPCLKB to QB[3:0], nQB[3:0] | 100 | 196 | 300 | ps |
| | Channel Isolation | NOTE ³ | | 65 | | dB |
| $t_{SK(o)}$ | Output Skew ^{4, 5, 6} | Any Output | | 20 | 40 | ps |
| $t_{SK(b)}$ | Output Bank Skew ^{4, 5} | Within QA[3:0] or QB[3:0] Outputs | | 17 | 35 | ps |
| $t_{SK(p)}$ | Pulse Skew | $f_{REF} = 100MHz$ | -50 | | 50 | ps |
| $t_{SK(pp)}$ | Part-to-Part Skew ^{5, 7} | | | | 200 | ps |
| t_{JIT} | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | $f_{REF} = 156.25MHz$ Square Wave, $V_{PP} = 1V$, Integration Range: 1kHz – 40MHz | | 90 | 125 | fs |
| | | $f_{REF} = 156.25MHz$ Square Wave, $V_{PP} = 1V$, Integration Range: 10kHz – 20MHz | | 70 | 105 | fs |
| | | $f_{REF} = 156.25MHz$ Square Wave, $V_{PP} = 1V$, Integration Range: 12kHz – 20MHz | | 70 | 105 | fs |
| | | $f_{REF} = 156.25MHz$ Square Wave, $V_{PP} = 0.5V$, Integration Range: 1kHz – 40MHz | | 100 | 165 | fs |
| | | $f_{REF} = 156.25MHz$ Square Wave, $V_{PP} = 0.5V$, Integration Range: 10kHz – 20MHz | | 72 | 130 | fs |
| | | $f_{REF} = 156.25MHz$ Square Wave, $V_{PP} = 0.5V$, Integration Range: 12kHz – 20MHz | | 72 | 130 | fs |
| $t_{JIT, SP}$ | Spurious suppression, coupling from QA3 to QB0 | $f_{QB0} = 500MHz$, $V_{PP(PCLKB)} = 0.15V$, $V_{CMR(PCLKB)} = 1V$ and $f_{QA1} = 62.5MHz$, $V_{PP(PCLKA)} = 1.0V$, $V_{CMR(PCLKA)} = 1V$ | | 67 | | dB |
| | | $f_{QB0} = 500MHz$, $V_{PP(PCLKB)} = 0.15V$, $V_{CMR(PCLKB)} = 1V$ and $f_{QA1} = 15.625MHz$, $V_{PP(PCLKA)} = 1.0V$, $V_{CMR(PCLKA)} = 1V$ | | 80 | | dB |
| t_R / t_F | Output Rise/ Fall Time | 20% to 80% | | 120 | 225 | ps |

NOTE 1: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2: Measured from the differential input crossing point to the differential output crossing point.

NOTE 3: Channel Isolation is defined as the output amplitude delta between the measured output with active input and the same output with inactive input when the other channel is active.

NOTE 4: Defined as skew among outputs at the same supply voltage and with equal load conditions. Measured at the differential cross point.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

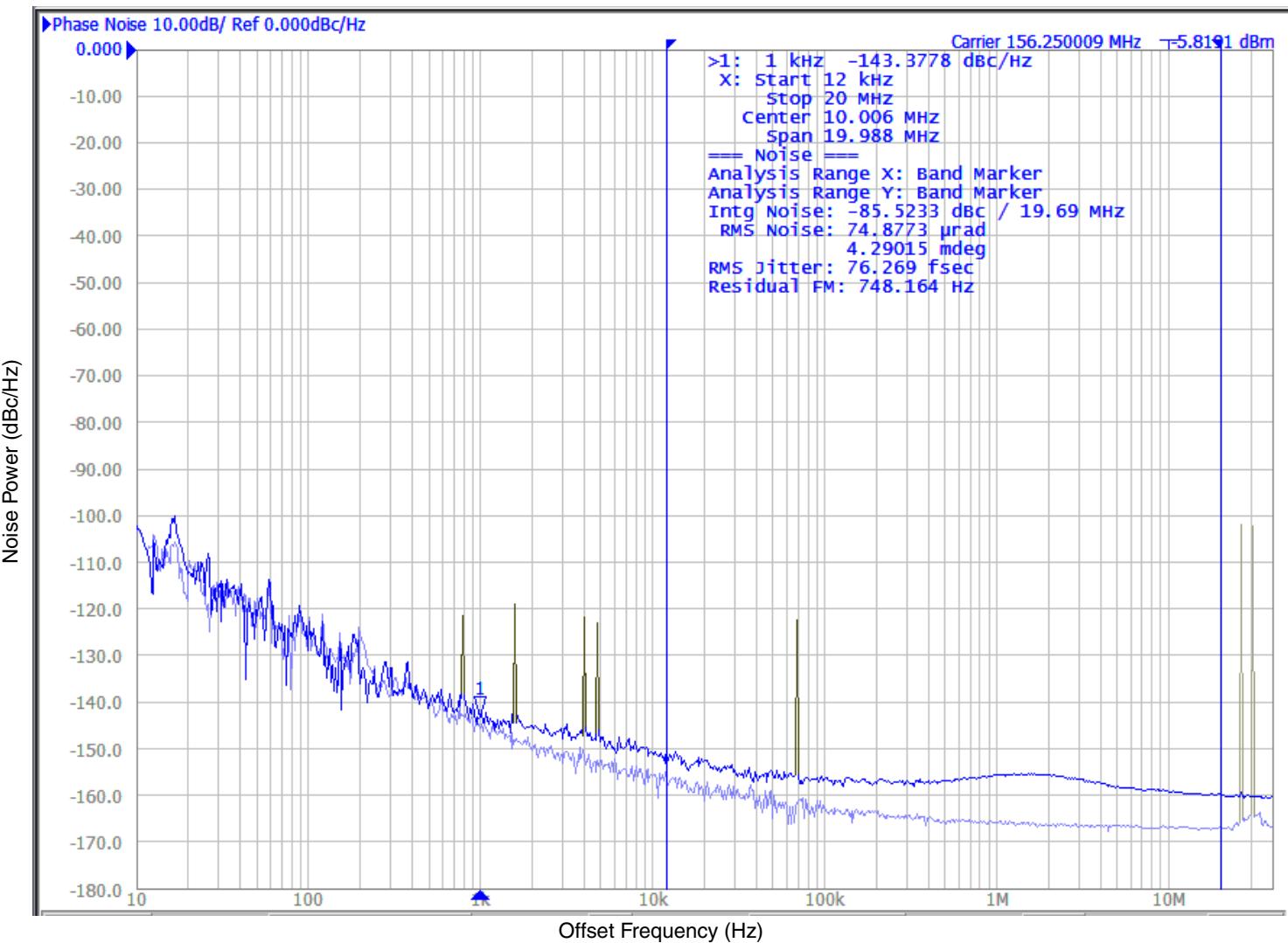
NOTE 6: Both PCLKA, nPCLKA and PCLKB, nPCLKB inputs are phase aligned.

NOTE 7: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross point.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

Additive phase jitter was measured with a Wenzel 156.25MHz oscillator as the input source.

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from PCLK to ground.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

V_{REFX}

Unused V_{REFA} and V_{REFB} pins can be left floating. We recommend that there is no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock is driven from a single-ended 2.5V LVCMS driver and the DC offset (or swing center) of this signal is 1.25V, the R1 and R2 values should be adjusted to set the V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R_3 and R_4 in parallel should

equal the transmission line impedance. For most 50Ω applications, R_3 and R_4 can be 100Ω . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMS signaling, it is recommended that the amplitude be reduced while maintaining an edge rate faster than 1V/ns . The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than $V_{DD} + 0.3\text{V}$. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

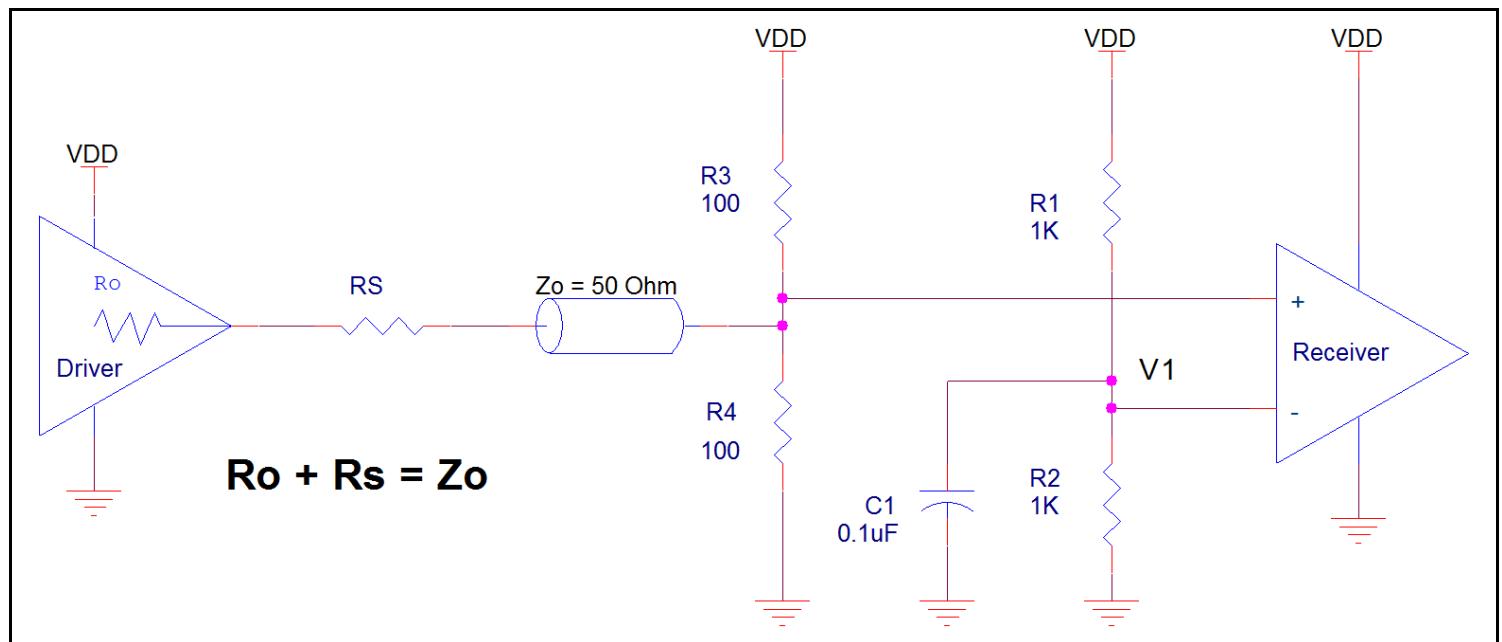


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

2.5V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. [Figure 2A](#) to [Figure 2D](#) show interface examples for the PCLK /nPCLK input driven by the most common driver types. The

input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

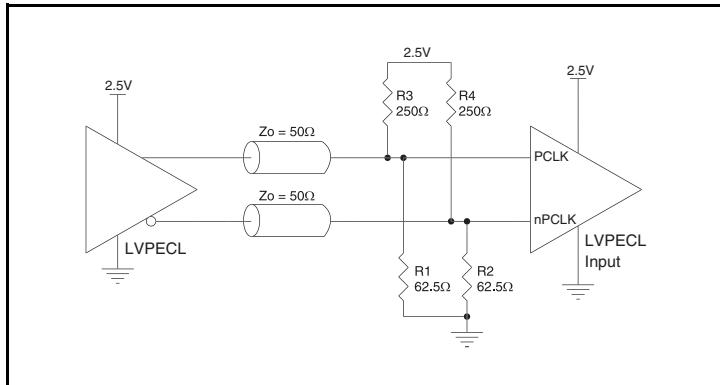


Figure 2A. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

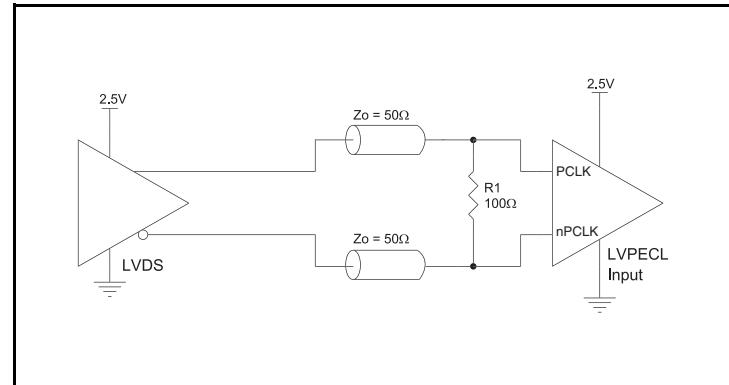


Figure 2C. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver

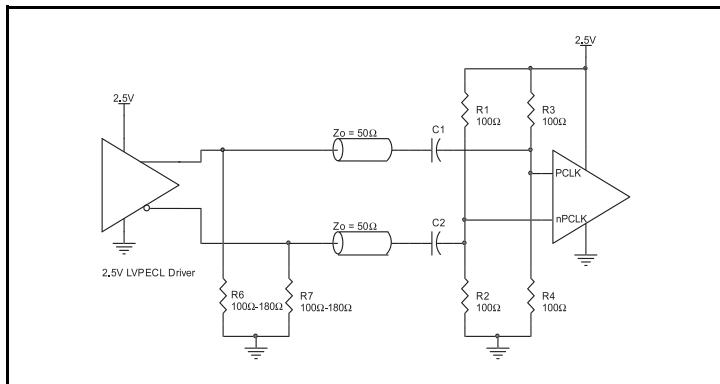


Figure 2B. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

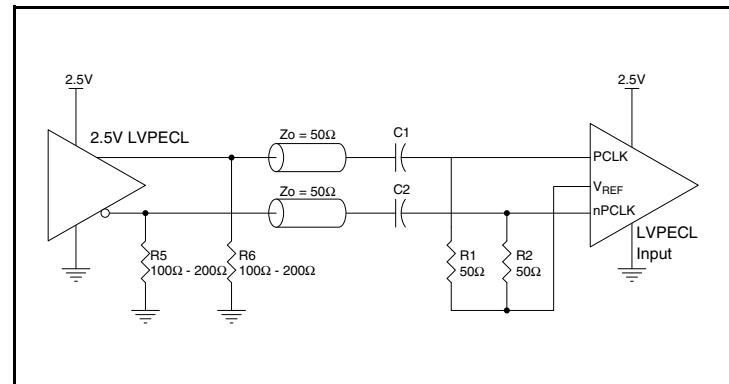


Figure 2D. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver AC Couple with V_{REF} bias

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The

standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

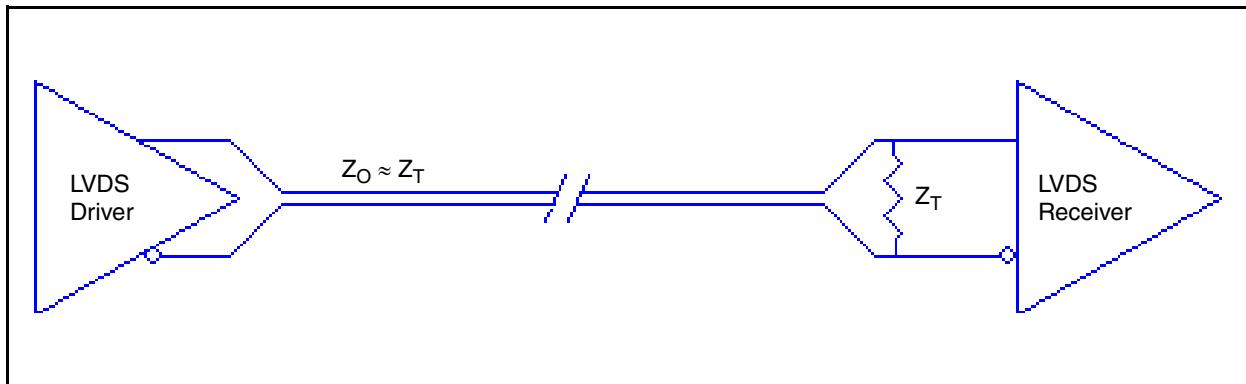


Figure 3A. Standard LVDS Termination

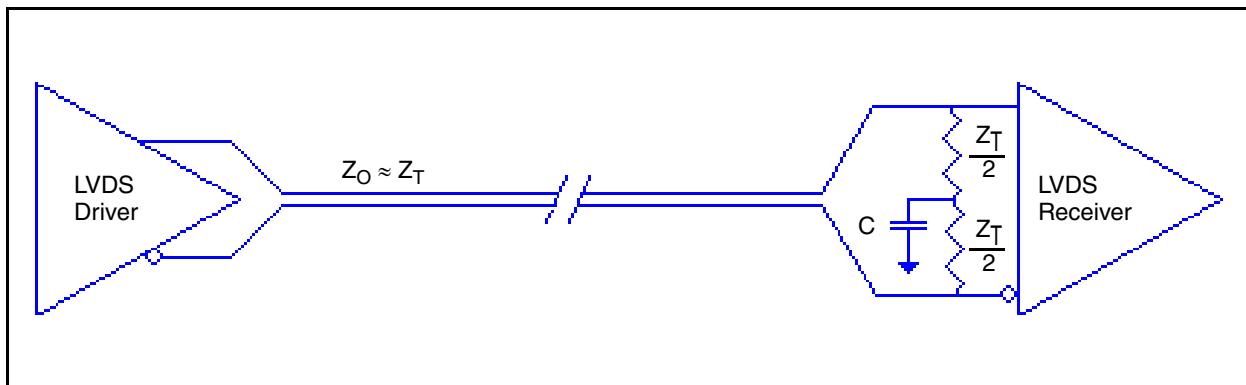


Figure 3B. Optional LVDS Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in [Figure 4](#). The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

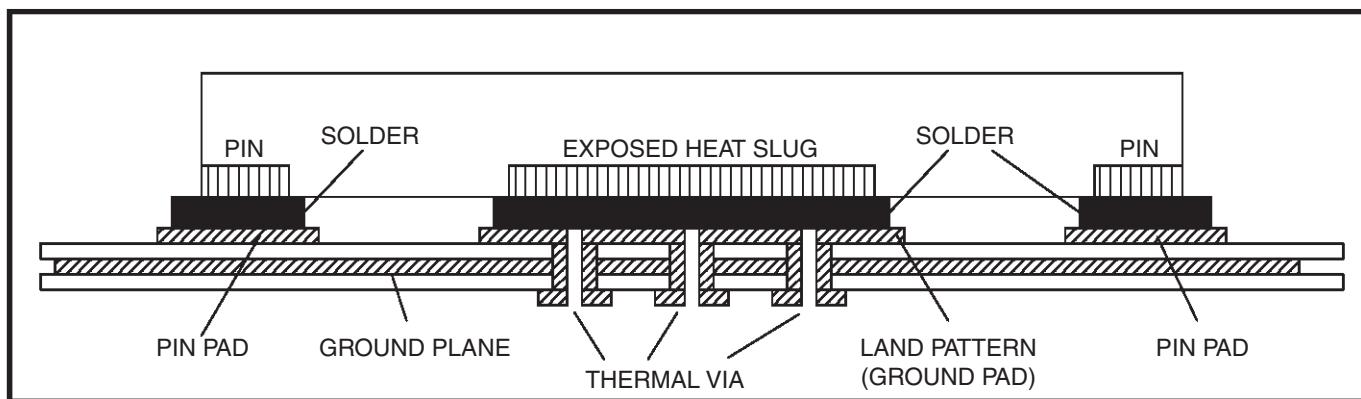


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the 8SLVD2104. Equations and example calculations are also provided.

1. Power Dissipation.

The following is the power dissipation for $V_{DD} = 2.5V + 5\% = 2.625V$, which gives worst case results.

Maximum current at 85°C: $I_{DD_MAX} = 156mA$

- $Power_MAX = V_{DD_MAX} * I_{DD_MAX} = 2.625V * 156mA = 409.5mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * P_{d_total} + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

P_{d_total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 46.2°C/W per [Table 6](#) below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.4095W * 46.2^\circ C/W = 103.9^\circ C$. This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 28 Lead VFQFN, Forced Convection

| θ_{JA} at 0 Air Flow | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 46.2°C/W | 39.4°C/W | 37.1°C/W |

Reliability Information

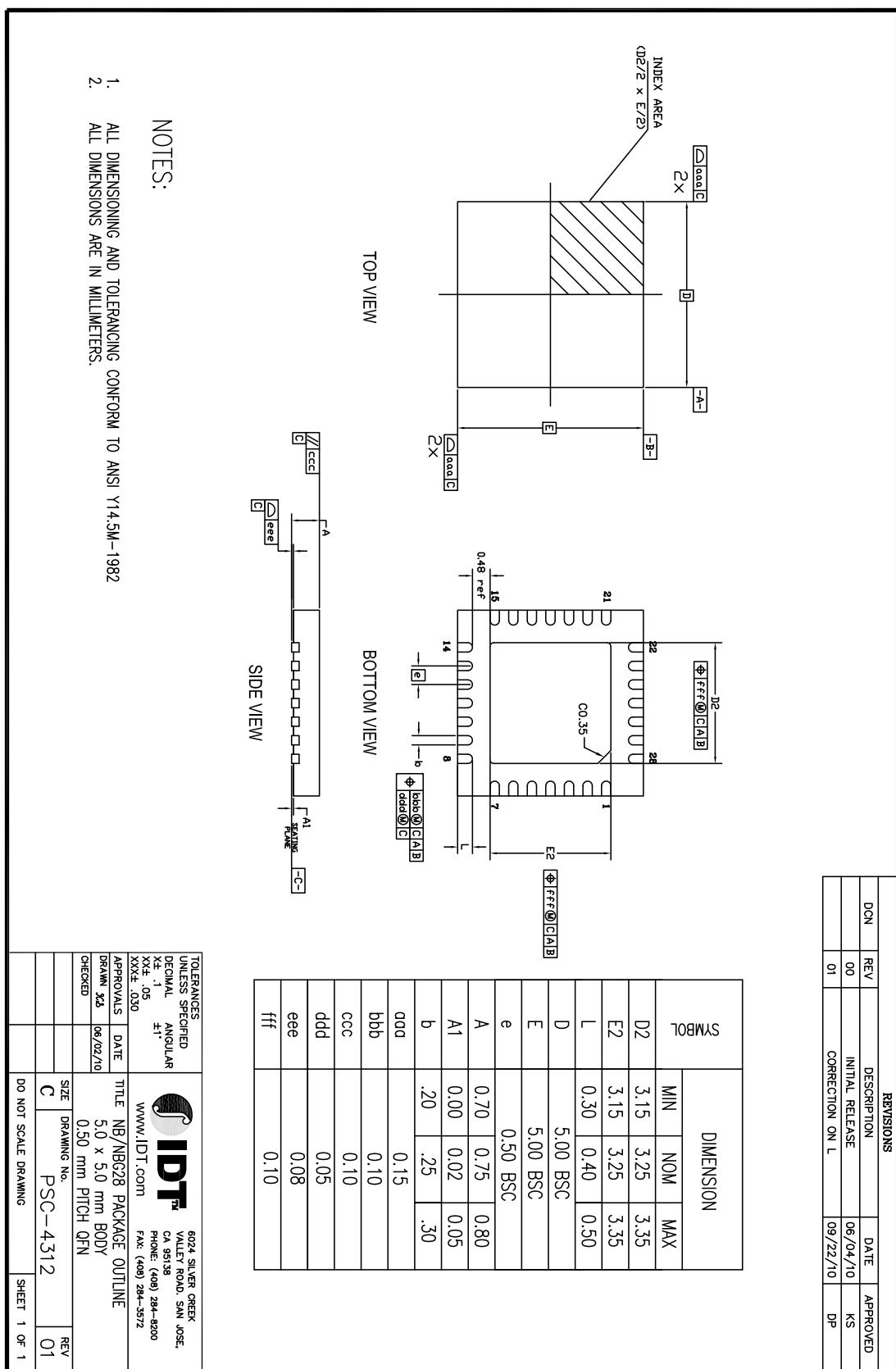
Table 7. θ_{JA} vs. Air Flow Table for a 28-Lead VFQFN

| θ_{JA} at 0 Air Flow | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 46.2°C/W | 39.4°C/W | 37.1°C/W |

Transistor Count

The transistor count for the 8SLVD2104 is: 394

28-Lead VFQFN Package Outline and Package Dimensions



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

DUAL 1:4, LVDS OUTPUT FANOUT BUFFER

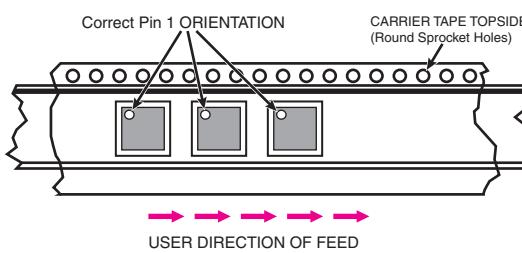
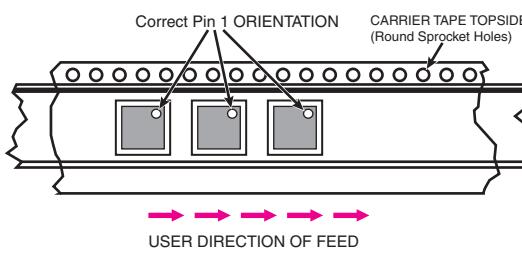
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Ordering Information

Table 8. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|--------------|--------------------------|---|---------------|
| 8SLVD2104NBGI | SLVD2104NBGI | 28 Lead VFQFN, Lead-Free | Tray | -40°C to 85°C |
| 8SLVD2104NBGI8 | SLVD2104NBGI | 28 Lead VFQFN, Lead-Free | Tape & Reel pin 1 orientation: EIA-481-C | -40°C to 85°C |
| 8SLVD2104NBGI/W | SLVD2104NBGI | 28 Lead VFQFN, Lead-Free | Tape & Reel pin 1 orientation: EIA-481-D | -40°C to 85°C |

Table 9. Pin 1 Orientation in Tape and Reel Packaging

| Part Number Suffix | Pin 1 Orientation | Illustration |
|--------------------|------------------------|--|
| 8 | Quadrant 1 (EIA-481-C) |  |
| /W | Quadrant 2 (EIA-481-D) |  |

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