General Description

The 8T33FS6222 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the 8T33FS6222 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

Functional Description

The 8T33FS6222 is designed for low skew clock distribution systems and supports clock frequencies up to 2GHz. The CLK0 and CLK1 inputs can be driven by PECL compatible signals. Each of the four output banks of two, three, four and six differential clock output pairs can be independently configured to distribute the input frequency or 2 of the input frequency. The FSELA, FSELB, FSELC, FSELD, and CLK_SEL are asychronous control inputs. Any changes of the control inputs require a MR pulse for resynchronization of the 2 outputs. For the functionality of the MR control input, see Figure 4.Functional Diagram.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The 8T33FS6222 can be operated from a single 3.3V or 2.5V supply.

Features

- Fifteen differential PECL outputs (four output banks)
- Two selectable differential PECL inputs
- Selectable ÷1 or ÷2 frequency divider
- Supports DC to 2GHz input frequency
- Single 3.3V or 2.5V supply
- Standard 52-Lead TQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Lead-free RoHS 6 packaging

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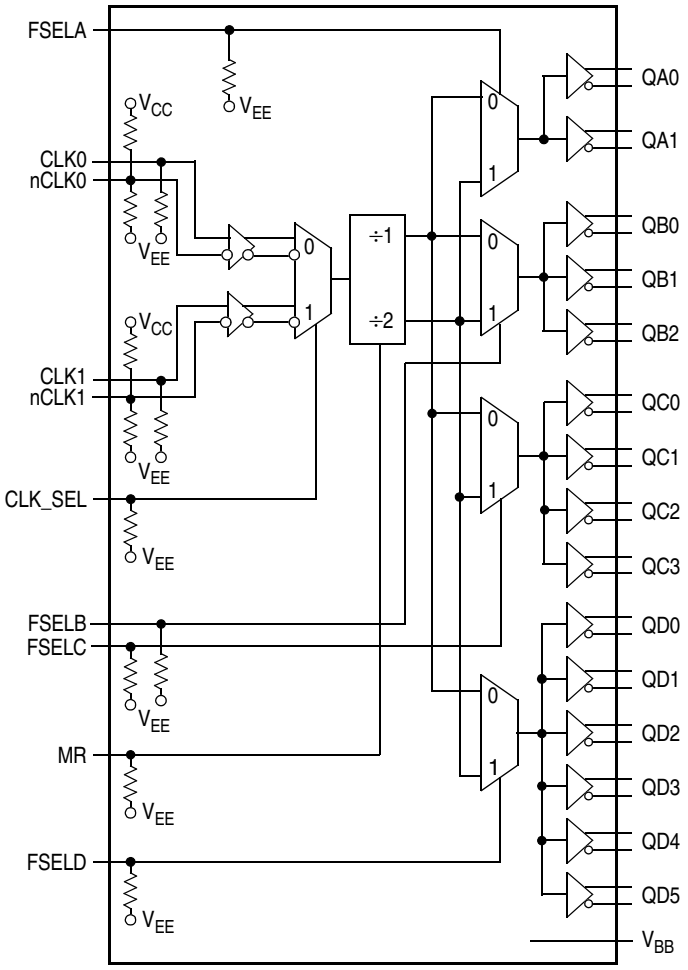
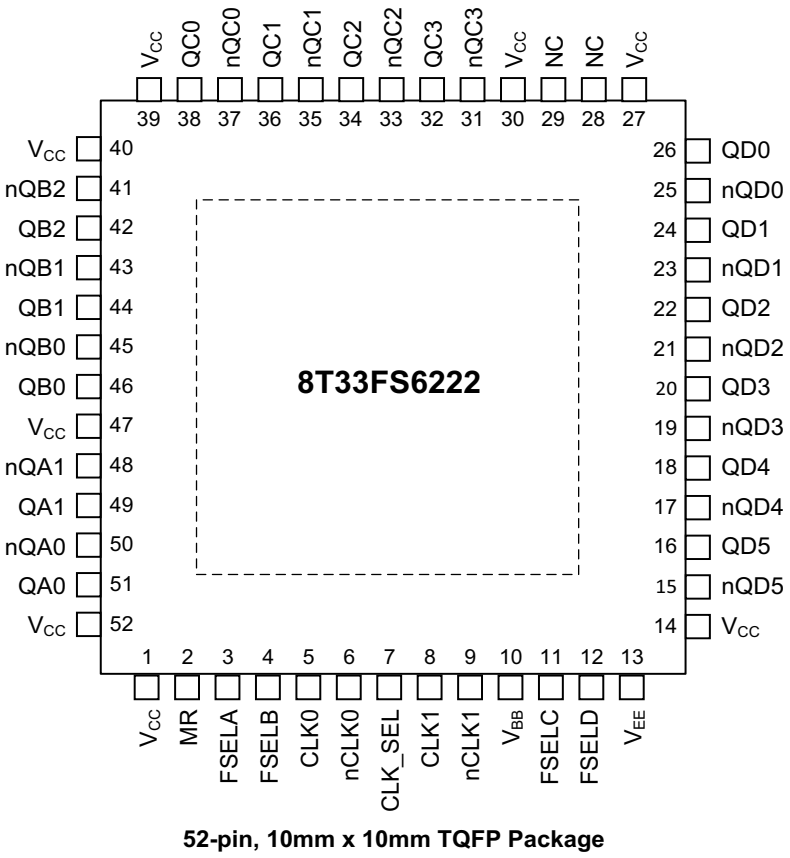


Figure 1. 8T33FS6222 Logic Diagram



52-pin, 10mm x 10mm TQFP Package

Figure 2. 52-Lead Package Pin Assignment

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Pin Description and Characteristics

Table 1. Pin Description Table

Number	Name	Type		Description
1	V_{CC}	Power		Power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
2	MR	Input		Reset.
3	FSELA	Input		Selection output frequency divider for Bank A.
4	FSELB	Input		Selection output frequency divider for Bank B.
5	CLK0	Input	PECL	Differential reference clock signal input.
6	nCLK0	Input	PECL	Differential reference clock signal input.
7	CLK_SEL	Input		Clock reference select input.
8	CLK1	Input	PECL	Alternative differential reference clock signal input.
9	nCLK1	Input	PECL	Alternative differential reference clock signal input.
10	V_{BB}	Output		Reference voltage output for single ended PECL operation.
11	FSELC	Input		Selection output frequency divider for Bank C.
12	FSELD	Input		Selection output frequency divider for Bank D.
13	V_{EE}[1]	Power		Negative power supply.
14	V_{CC}	Power		Power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
15	nQD5	Output	PECL	Bank D differential output.
16	QD5	Output	PECL	Bank D differential output.
17	nQD4	Output	PECL	Bank D differential output.
18	QD4	Output	PECL	Bank D differential output.
19	nQD3	Output	PECL	Bank D differential output.
20	QD3	Output	PECL	Bank D differential output.
21	nQD2	Output	PECL	Bank D differential output.
22	QD2	Output	PECL	Bank D differential output.
23	nQD1	Output	PECL	Bank D differential output.
24	QD1	Output	PECL	Bank D differential output.
25	nQD0	Output	PECL	Bank D differential output.
26	QD0	Output	PECL	Bank D differential output.
27	V_{CC}	Power		Power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
28	NC	Unused		No internal connection.
29	NC	Unused		No internal connection.
30	V_{CC}	Power		Power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
31	nQC3	Output	PECL	Bank C differential output.
32	QC3	Output	PECL	Bank C differential output.

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Table 1. Pin Description Table

Number	Name	Type		Description
33	nQC2	Output	PECL	Bank C differential output.
34	QC2	Output	PECL	Bank C differential output.
35	nQC1	Output	PECL	Bank C differential output.
36	QC1	Output	PECL	Bank C differential output.
37	nQC0	Output	PECL	Bank C differential output.
38	QC0	Output	PECL	Bank C differential output.
39	V_{CC}	Power		Power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
40	V_{CC}	Power		Power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
41	nQB2	Output	PECL	Bank B differential output.
42	QB2	Output	PECL	Bank B differential output.
43	nQB1	Output	PECL	Bank B differential output.
44	QB1	Output	PECL	Bank B differential output.
45	nQB0	Output	PECL	Bank B differential output.
46	QB0	Output	PECL	Bank B differential output.
47	V_{CC}	Power		Power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
48	nQA1	Output	PECL	Bank A differential output.
49	QA1	Output	PECL	Bank A differential output.
50	nQA0	Output	PECL	Bank A differential output.
51	QA0			Bank A differential output.
52	V_{CC}	Power		Power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
ePAD	V_{EE_EP}	Power		Exposed pad of package. Connect to ground.

NOTE 1. In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either +3.3 V or +2.5 V. The input and output levels are referenced to the most positive supply (V_{CC}).

Table 2. Function Table

Control Pin	0	1
FSELA (asynchronous)	÷1	÷2
FSELB (asynchronous)	÷1	÷2
FSELC (asynchronous)	÷1	÷2
FSELD (asynchronous)	÷1	÷2
CLK_SEL (asynchronous)	CLK0	CLK1
MR (asynchronous)	Active	Reset. Qx = L and nQx = H

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability

Table 3. Absolute Maximum Ratings

Symbol	Characteristics		Min	Max	Unit
V_{CC}	Supply Voltage		-0.3	3.6	V
V_{IN}	DC Input Voltage		-0.3	V_{CC} + 0.3	V
V_{OUT}	DC Output Voltage		-0.3	V_{CC} + 0.3	V
I_{IN}	DC Input Current			±20	mA
I_{OUT}	DC Output Current			±50	mA
T_S	Storage Temperature		-65	125	°C
T_{FUNC}	Functional Temperature Range		T_A = -40	T_A = +85	°C
T_J	Operating Junction Temperature			125	°C
HBM	ESD Human Body Model[1]			2000	V
CDM	ESD Charged Device Model[1]			500	V

NOTE 1. According to JEDEC/JS-001-2012/JESD22-C101E.

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DC Electrical Characteristics

Table 4. PECL DC Characteristics, V_{CC} = 2.5V ±5% or V_{CC} = 3.3V ±5%, V_{EE} = GND, T_A = -40°C to +85°C

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
Clock Input Pair CLK0, nCLK0, CLK1, nCLK1 (PECL differential signals)						
V_{PP}	Differential Input Voltage[1]	Differential operation	0.2		1.3	V
V_{CMR}	Differential Cross Point Voltage[2]	Differential operation	1.0		$V_{CC} – V_{PP}/2$	V
I_{IN}	Input Current[1]	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$			±150	µA
Clock Inputs MR, CLK_SEL, FSELA, FSELB, FSELC, FSELD						
V_{IH}	Input Voltage High		$V_{CC} – 1.165$		V_{CC}	V
V_{IL}	Input Voltage Low		V_{EE}		$V_{CC} – 1.475$	V
I_{IN}	Input Current[3]	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$			±150	µA
PECL Clock Outputs (QA[0:1], nQA[0:1], QB[0:2], nQB[0:2], QC[0:3], nQC[0:3], QD[0:5], nQD[0:5]						
V_{OH}	Output High Voltage	I_{OH} = –30mA[4]	$V_{CC} – 1.1$		$V_{CC} – 0.7$	V
V_{OL}	Output Low Voltage	I_{OL} = –5mA[4]	$V_{CC} – 1.9$		$V_{CC} – 1.4$	V
Supply Current and V_{BB}						
I_{EE}[5]	Maximum Quiescent Supply Current without Output Termination Current	V_{EE} pins			145	mA
V_{BB}	Output Reference Voltage	I_{BB} = 0.4mA	$V_{CC} – 1.38$		$V_{CC} – 1.2$	V

NOTE 1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality. V_{IL} should not be less than -0.3V. V_{IH} should not be greater than V_{CC}.

NOTE 2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

NOTE 3. Input have internal pullup/pulldown resistors which affect the input current.

NOTE 4. Equivalent to a termination of 50Ω to V_{TT}.

NOTE 5. I_{CC} calculation:I_{CC} = (number of differential output used) x (I_{OH} + I_{OL}) + I_{EE}
I_{CC} = (number of differential output used) x ($V_{OH} – V_{TT}$)/R_{load} + ($V_{OL} – V_{TT}$)/R_{load} + I_{EE}.

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AC Electrical Characteristics

Table 5. AC Characteristics, PECL: V_{CC} = 3.3V ±5% or V_{CC} = 2.5V ±5%, V_{EE} = GND, T_A = -40°C to +85°C[1] [2]

Symbol	Characteristics		Condition	Min	Typ	Max	Unit
Clock Input Pair CLK0, nCLK0, CLK1, nCLK1 (PECL Differential Signals)							
f_{CLK}	Input Frequency		Differential	0		2000	MHz
PECL Clock Outputs (QA[0:1], nQA[0:1], QB[0:2], nQB[0:2], QC[0:3], nQC[0:3], QD[0:5], nQD[0:5]							
t_{PD}	Propagation Delay	CLK0 or CLK1 to Qx	Differential	350		800	ps
$V_{O(P-P)}$	Output Voltage (peak-to-peak)	f_O < 1.0GHz			0.7		V
		f_O < 2.0GHz			0.7		V
$t_{sk(O)}$	Output-to-Output Skew	within QA[0:1]	Differential			35	ps
		within QB[0:2]	Differential			35	ps
		within QC[0:3]	Differential			50	ps
		within QD[0:5]	Differential			60	ps
		any Output	Differential			130	ps
$t_{sk(PP)}$	Part-to-Part Skew		Differential			300	ps
t_{JIT}	Buffer additive Phase Jitter, RMS. Refer to the Additive section		F_{OUT} =156.25MHz, Integration Range: 12k–20M		127	186	fs
odc	Output Duty Cycle	f_{REF} < 0.1GHz	DC_{REF} = 50%	48		52	%
		f_{REF} < 1.0GHz	DC_{REF} = 50%	45		55	%
		f_{REF} < 2.0GHz	DC_{REF} = 50%	40		60	%
t_r, t_f	Output Rise/Fall Time		20% to 80%			300	ps

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.

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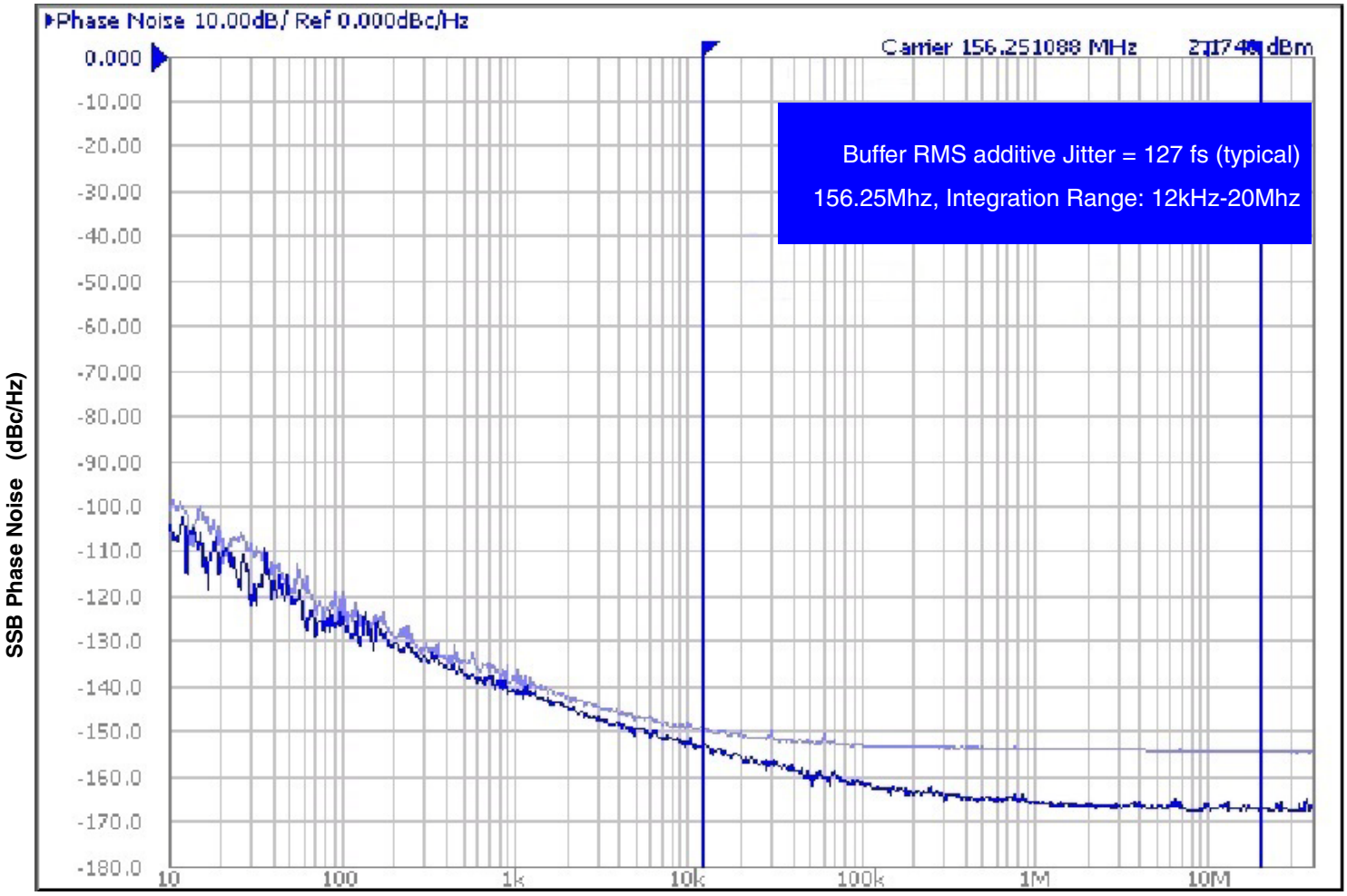
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise.** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Wenzel, 156.25MHz Oscillator as the input source.

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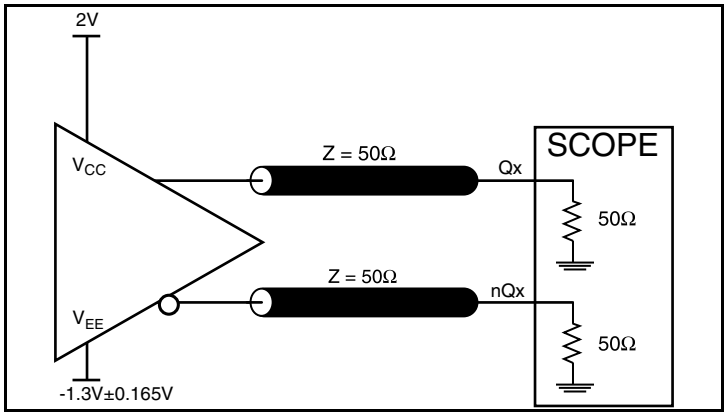
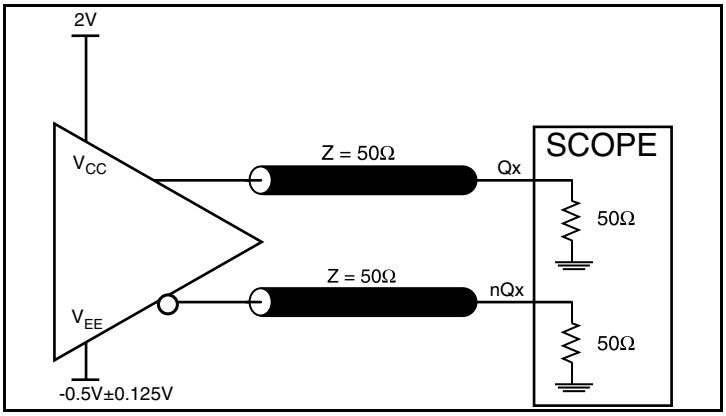
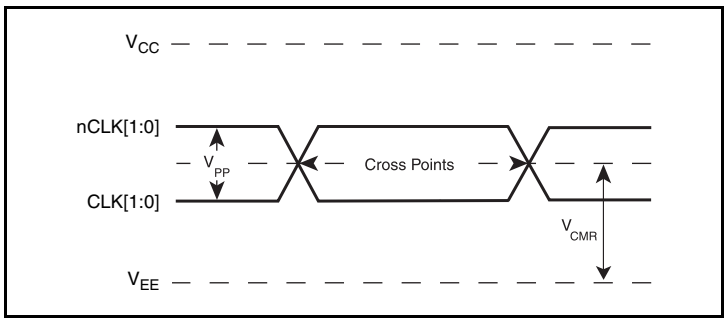
Parameter Measurement Information



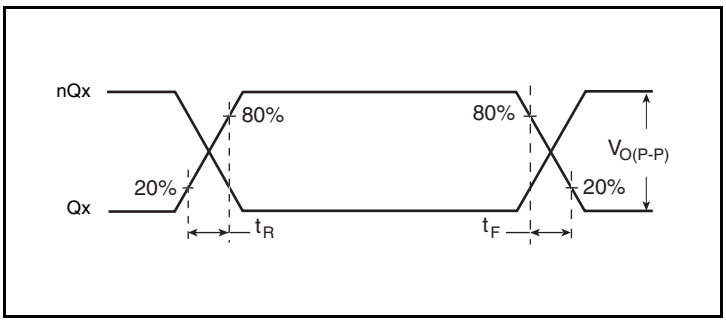
3.3V LVPECL Output Load AC Test Circuit



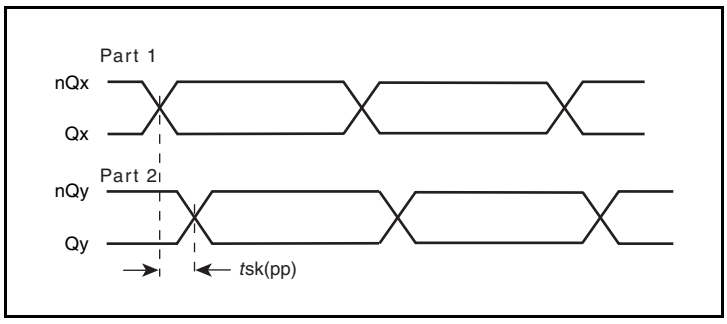
2.5V LVPECL Output Load AC Test Circuit



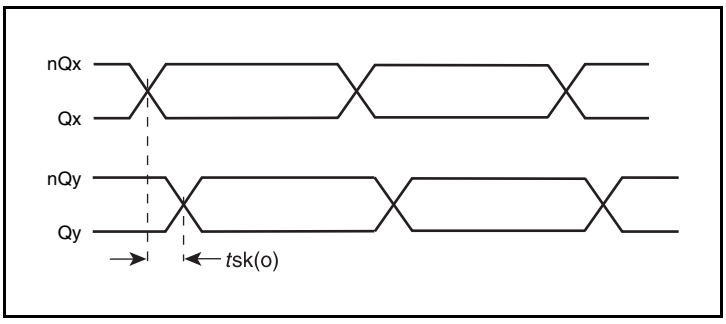
Differential Input Level



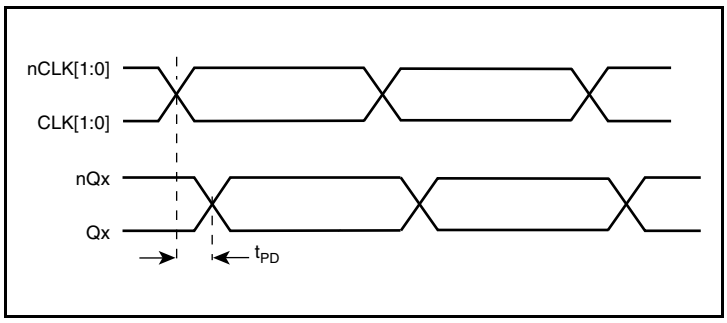
Output Rise/Fall Time



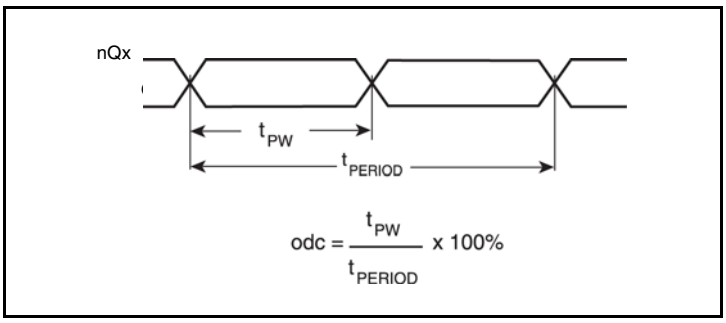
Part-to-Part Skew



Output Skew



Propagation Delay



Output Duty Cycle/Pulse Width

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Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 3 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

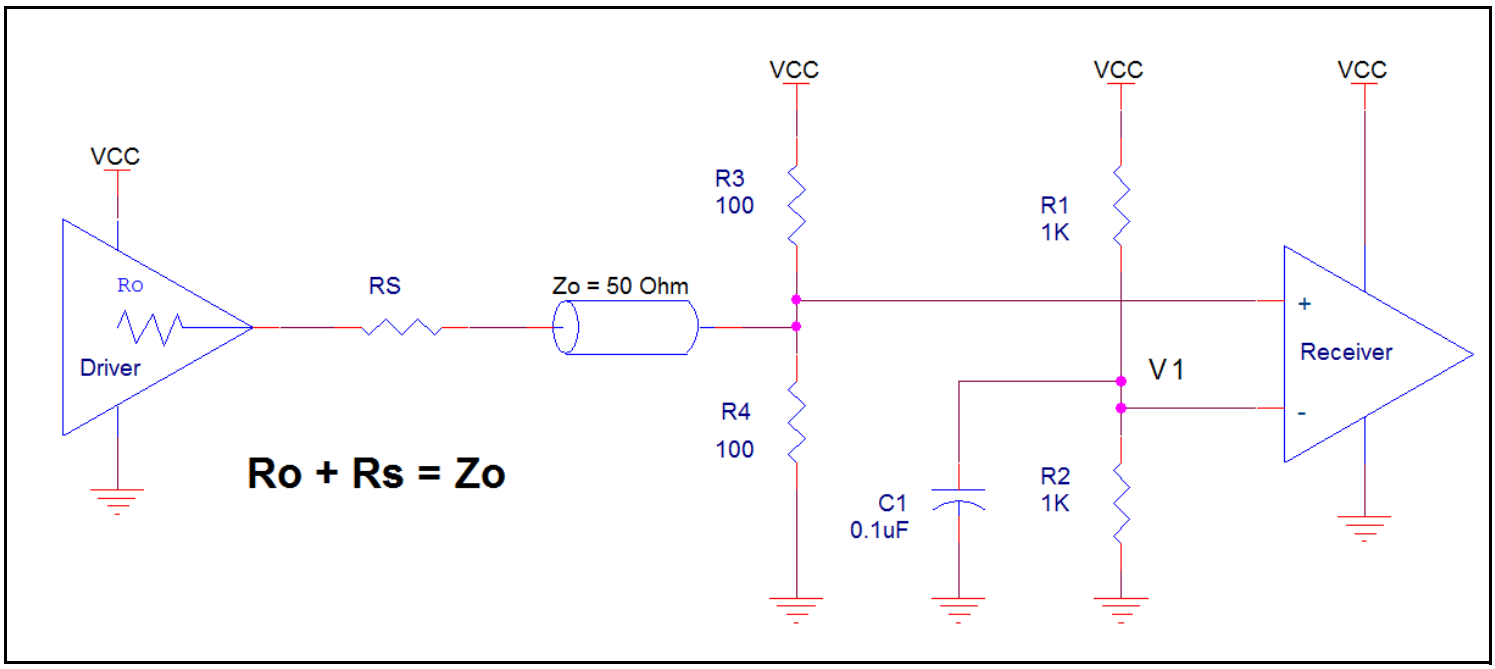

Figure 3. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Recommendations for Unused Input and Output Pins

Inputs:

CLKx/nCLKx Inputs

For applications not requiring the use of a differential input, both the CLKx and nCLKx pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLKx to ground. For applications

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

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Applications Information

Asynchronous Reset Functional Diagram

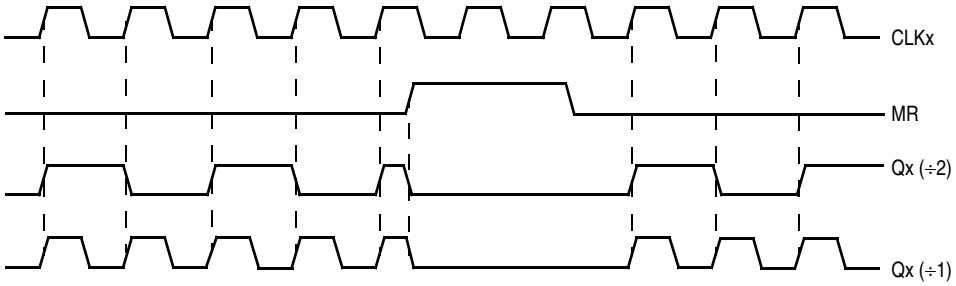

Figure 4. Functional Diagram

Maintaining Lowest Device Skew

The 8T33FS6222 guarantees low output-to-output bank skew of 130ps and a part-to-part skew of max. 300ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The 8T33FS6222 is a mixed analog/digital product. The differential architecture of the 8T33FS6222 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

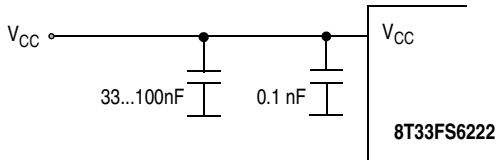

Figure 5. V_{CC} Power Supply Bypass

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EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Lead frame Base Package, Amkor Technology.

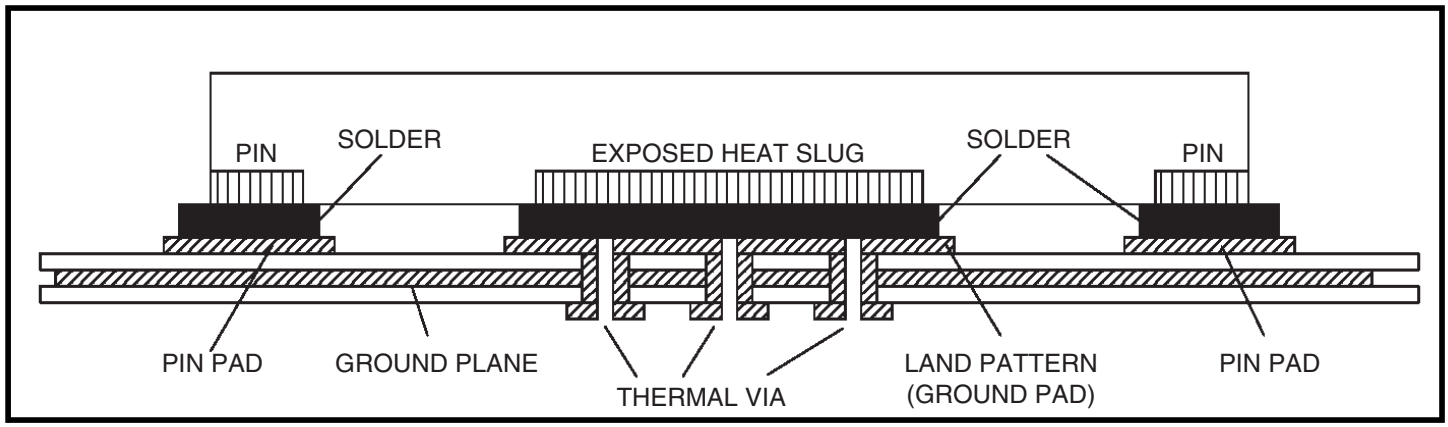

Figure 6. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

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3.3V LVPECL Clock Input Interface

The CLK /nCLK accepts LVPECL, LVDS, CML and other differential signals. Both differential outputs must meet the V_{PP} and V_{CMR} input requirements. *Figures 7A* to *7E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

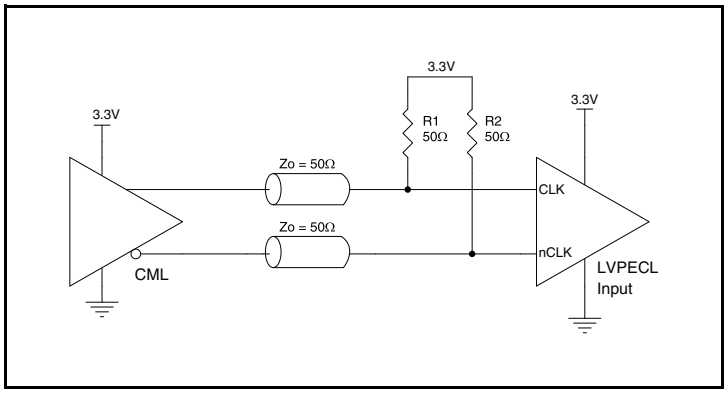

Figure 7A. CLK/nCLK Input Driven by a CML Driver

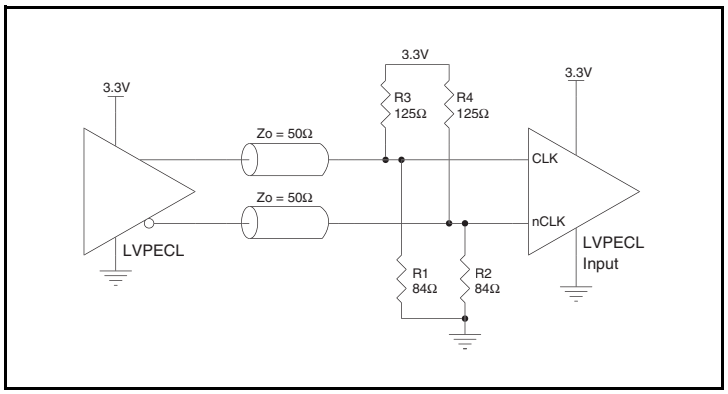

Figure 7B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

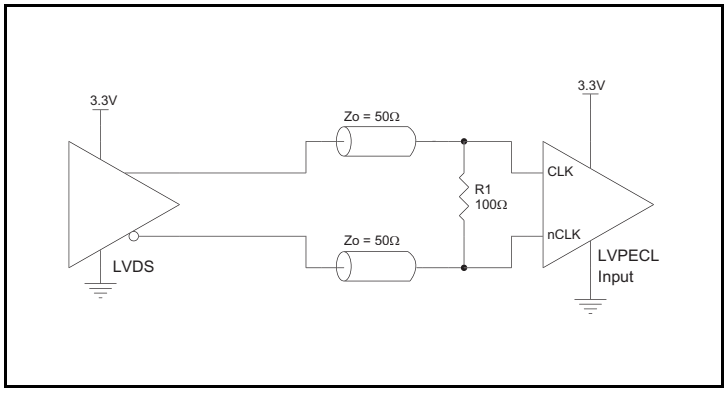

Figure 7C. CLK/nCLK Input Driven by a 3.3V LVDS Driver

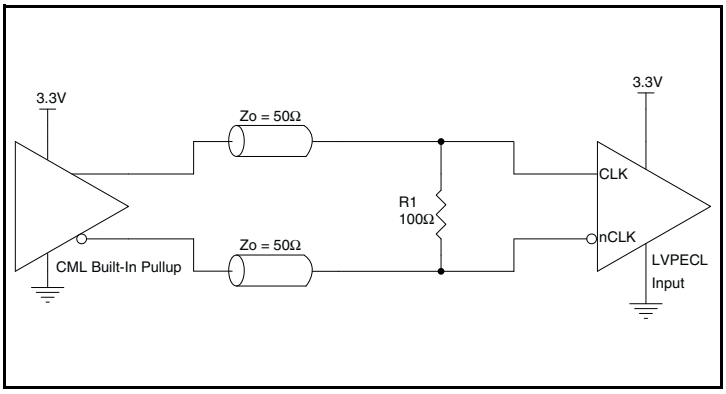

Figure 7D. CLK/nCLK Input Driven by a Built-In Pullup CML Driver

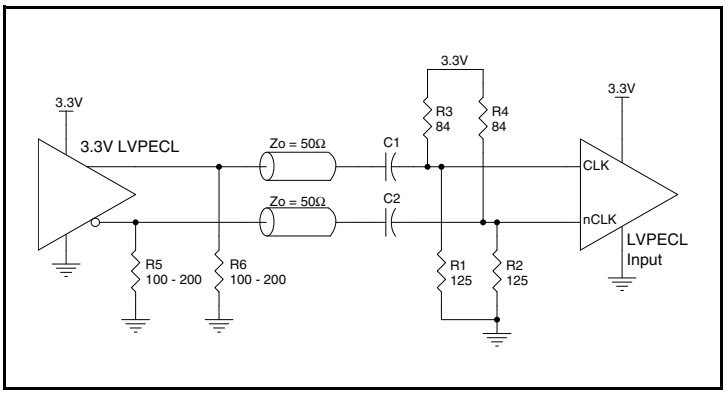

Figure 7E. CLK/nCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

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2.5V LVPECL Clock Input Interface

The CLK /nCLK accepts LVPECL, LVDS, CML and other differential signals. Both differential outputs must meet the V_{PP} and V_{CMR} input requirements. *Figures 8A* to *8E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

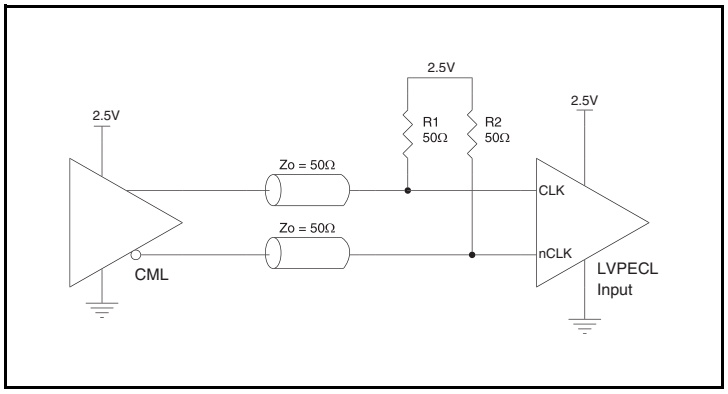

Figure 8A. CLK/nCLK Input Driven by a CML Driver

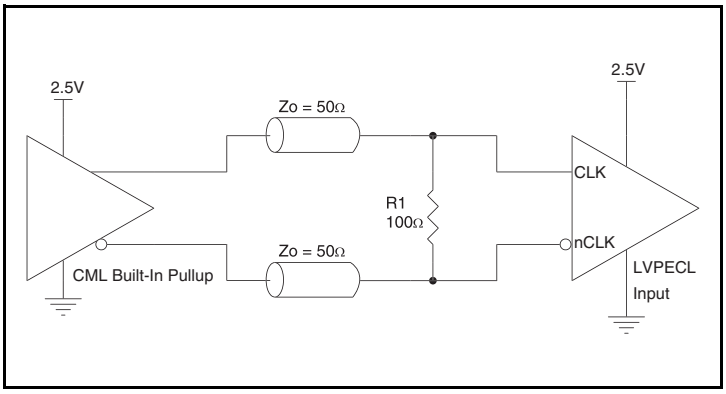

Figure 8D. CLK/nCLK Input Driven by a Built-In Pullup CML Driver

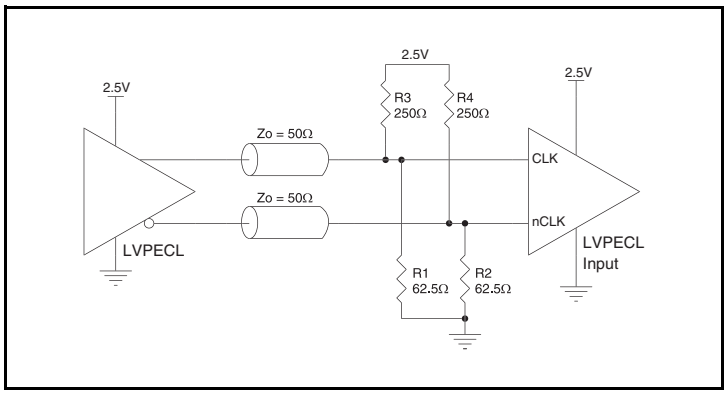

Figure 8B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

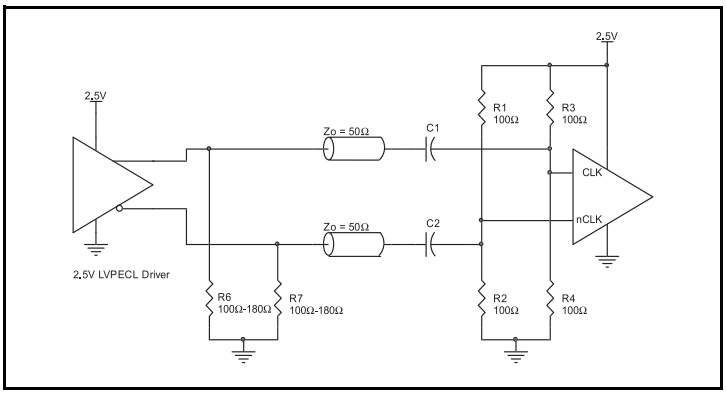

Figure 8E. CLK/nCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

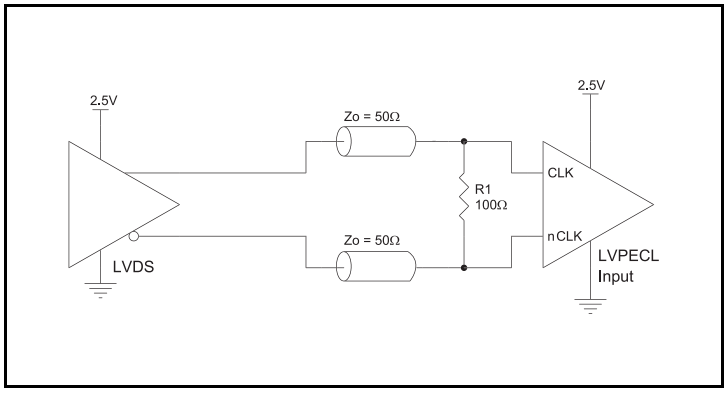

Figure 8C. CLK/nCLK Input Driven by a 2.5V LVDS Driver

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Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 9A* and *9B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

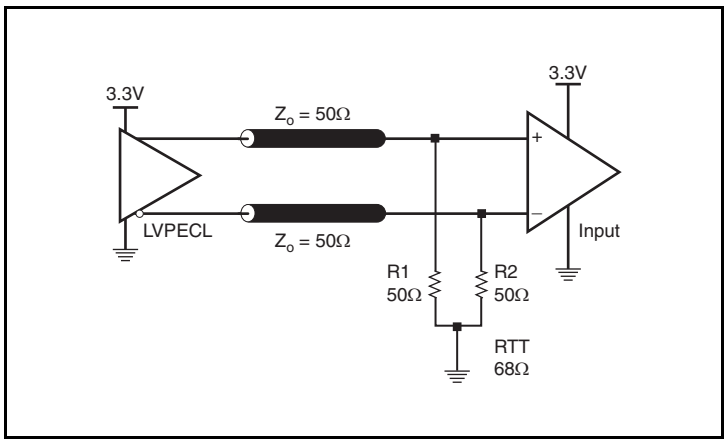

Figure 9A. 3.3V LVPECL Output Termination

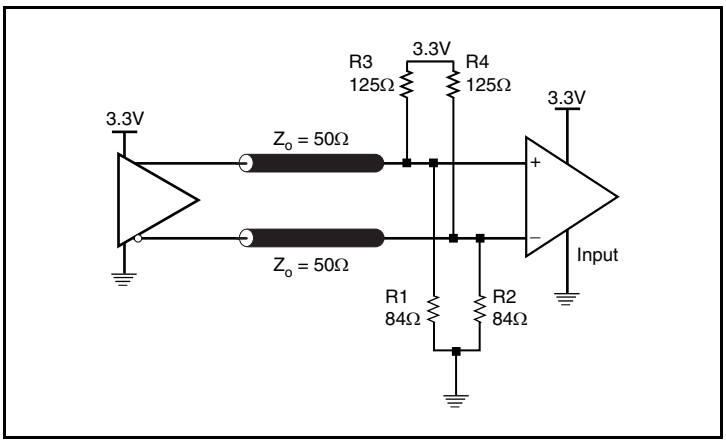

Figure 9B. 3.3V LVPECL Output Termination

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Termination for 2.5V LVPECL Outputs

Figure 10A and *Figure 10B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 10B can be eliminated and the termination is shown in *Figure 10C.*

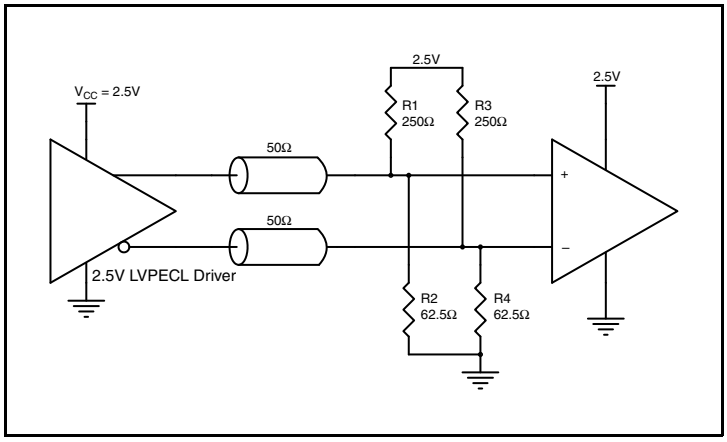

Figure 10A. 2.5V LVPECL Driver Termination Example

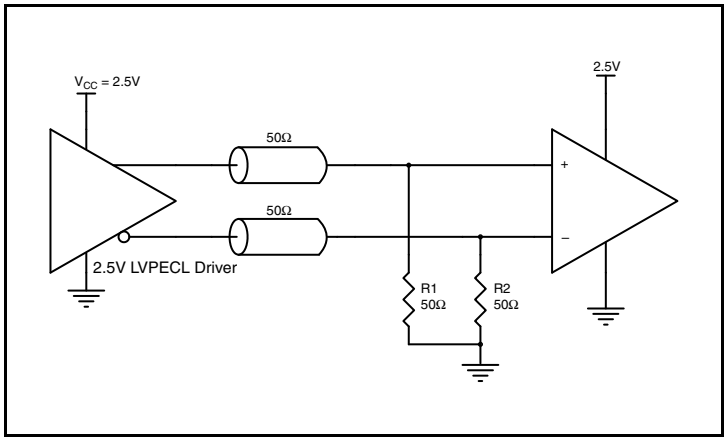

Figure 10B. 2.5V LVPECL Driver Termination Example

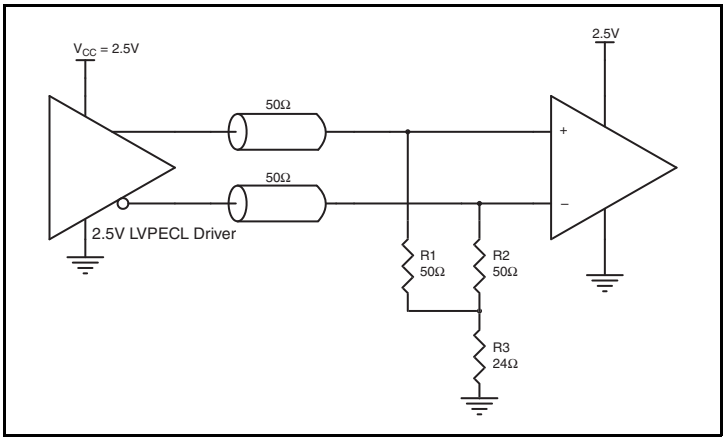

Figure 10C. 2.5V LVPECL Driver Termination Example

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Power Considerations

This section provides information on power dissipation and junction temperature for the 8T33FS6222.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8T33FS6222 is the sum of the core power plus the power dissipated due to the load.
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- The maximum current at 85C is: I_{EE_max} = **145mA**
- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 145mA = **502.4mW**
- Power (outputs)$_{MAX}$ = **35mW/Loaded Output pair**
  If all outputs are loaded, the total power is 15 * 35mW = **525mW**

  Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 502.4mW + 525mW = **1027mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 26.84°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.027W * 26.84°C/W = 112.5°C. This is within the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 52-Lead TQFP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	26.84°C/W	22.08°C/W	20.54°C/W

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3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 11.*

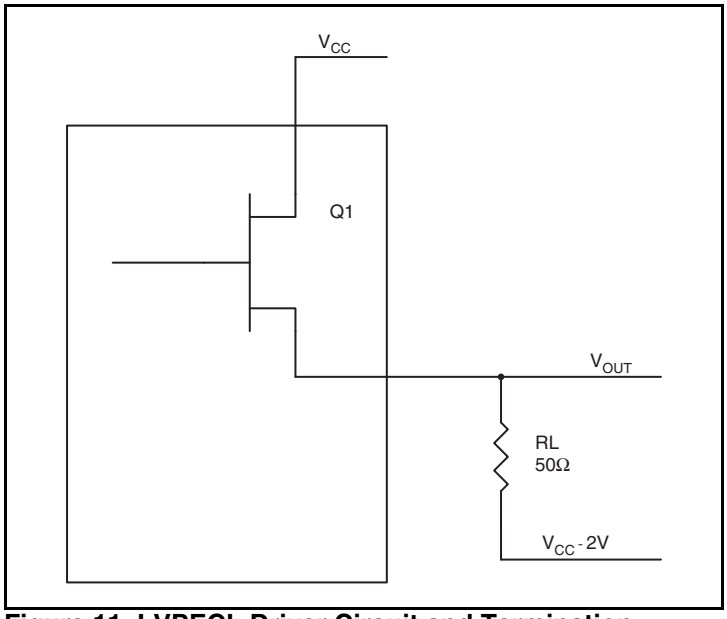

Figure 11. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} =$ **V_{CC_MAX} – 0.7V**
  ($V_{CC_MAX} - V_{OH_MAX}$) = **0.7V**
- For logic low, $V_{OUT} = V_{OL_MAX} =$ **V_{CC_MAX} – 1.4V**
  ($V_{CC_MAX} - V_{OL_MAX}$) = **1.4V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) =$
$[(2V - 0.7V)/50\Omega] * 0.7V =$ **18.2mW**

$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) =$
$[(2V - 1.4V)/50\Omega] * 1.4V =$ **16.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **35mW**

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 52-Lead TQFP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	26.84°C/W	22.08°C/W	20.54°C/W

Transistor Count

The transistor count for 8T33FS6222 is: 1959

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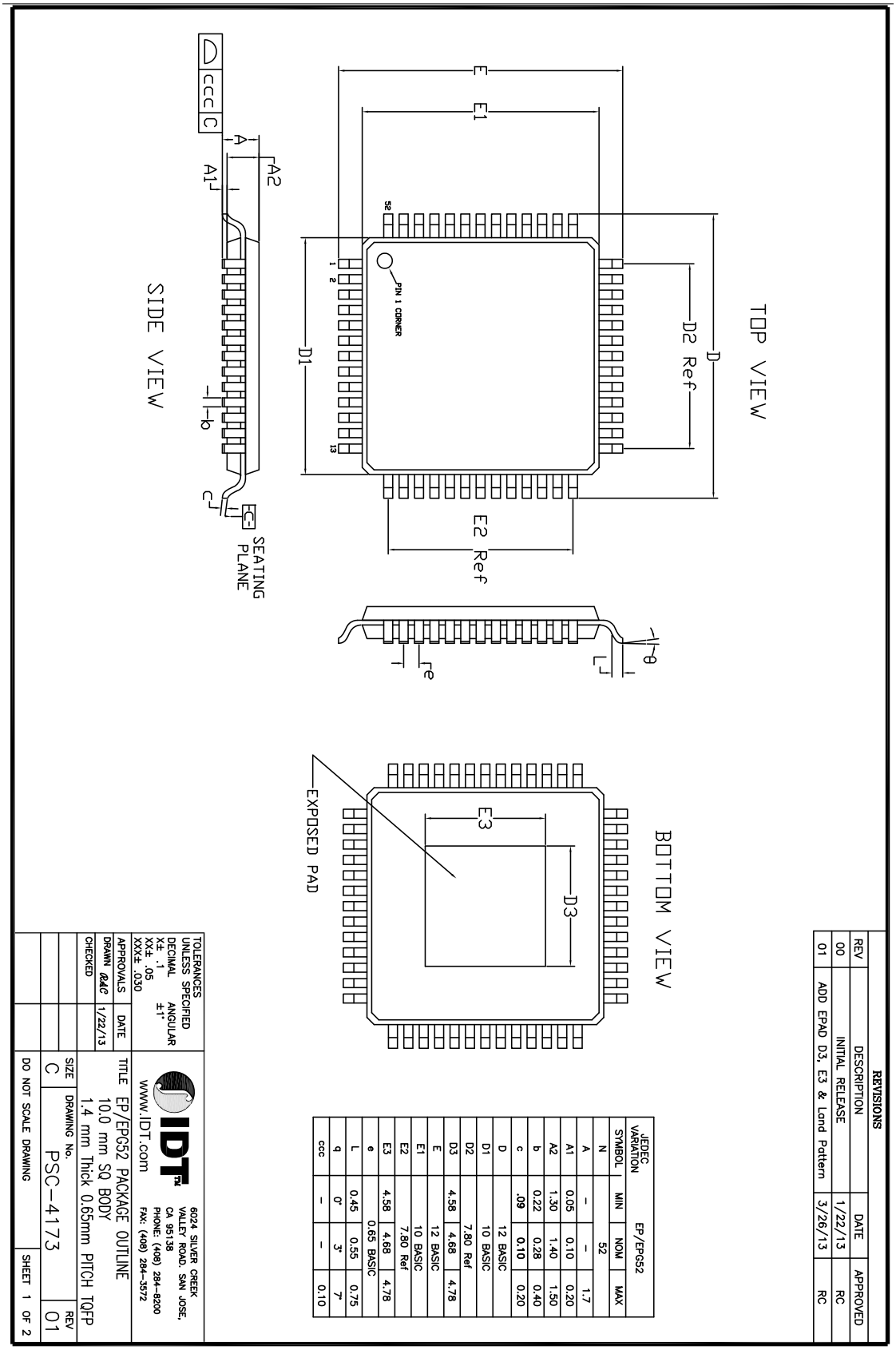
52-Lead TQFP Package Outline and Dimensions



REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	1/22/13	RC
01	ADD EPAD D3, E3 & Land Pattern	3/26/13	RC

JEDEC VARIATION	EP/EPG52		
SYMBOL	MIN	NOM	MAX
N		52	
A	–	–	1.7
A1	0.05	0.10	0.20
A2	1.30	1.40	1.50
b	0.22	0.28	0.40
c	.09	0.10	0.20
D		12 BASIC	
D1		10 BASIC	
D2		7.80 Ref	
D3	4.58	4.68	4.78
E		12 BASIC	
E1		10 BASIC	
E2		7.80 Ref	
E3	4.58	4.68	4.78
e		0.65 BASIC	
L	0.45	0.55	0.75
q	0°	3°	7°
ccc	–	–	0.10

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
X± .1 ±1°
XX± .05
XXX± .030

APPROVALS DATE
DRAWN 1/22/13
CHECKED

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6024 SILVER CREEK VALLEY ROAD, SAN JOSE, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-3572
www.IDT.com

TITLE EP/EPG52 PACKAGE OUTLINE
10.0 mm SQ BODY
1.4 mm Thick 0.65mm PITCH TQFP

SIZE C | DRAWING No. PSC-4173 | REV 01

DO NOT SCALE DRAWING | SHEET 1 OF 2

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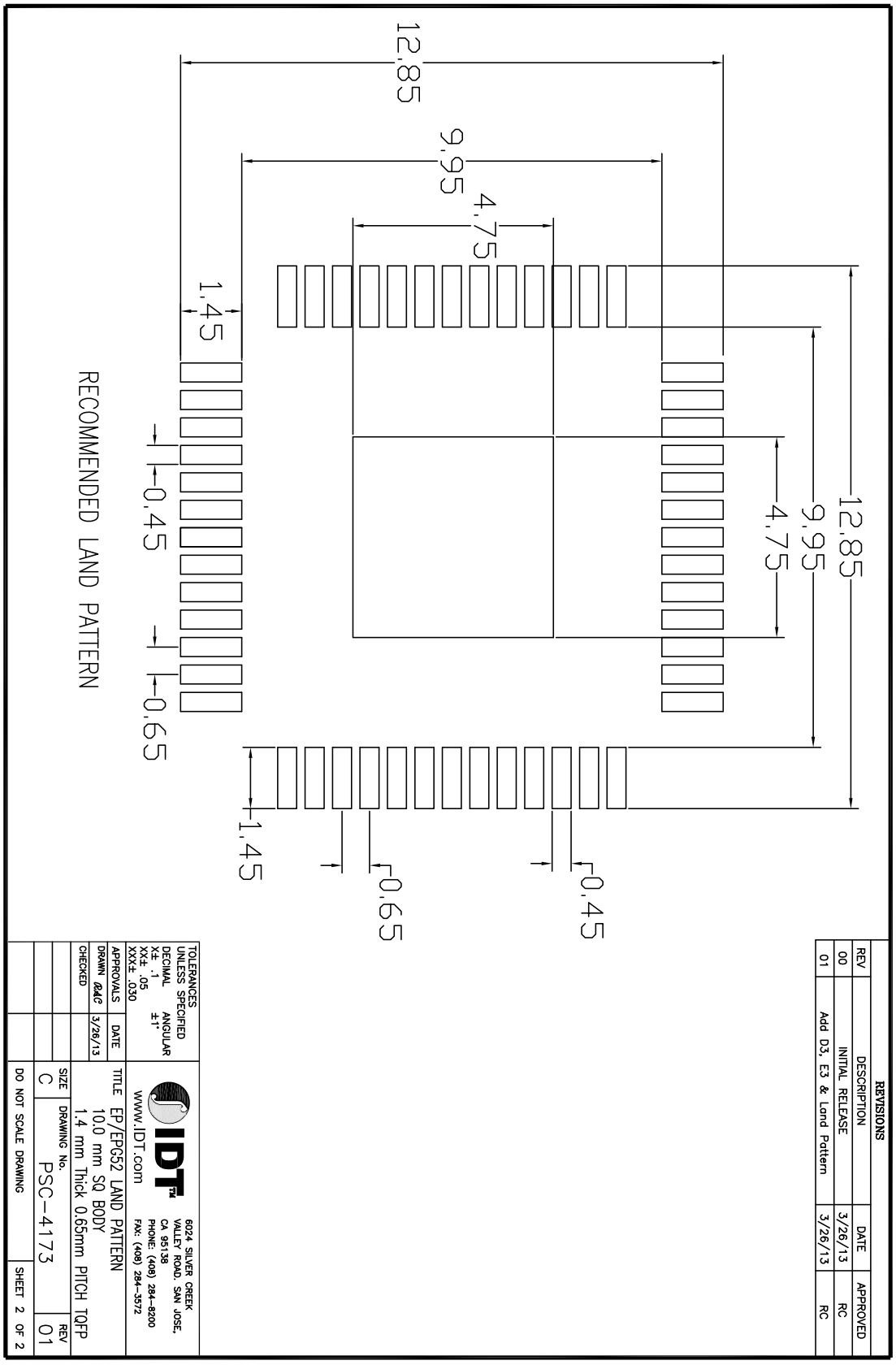
52-Lead TQFP Package Outline and Dimensions



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ORDERING INFORMATION

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T33FS6222EPGI	IDT8T33FS6222EPGI	52-Lead TQFP, Lead-Free	Tray	-40°C to 85°C
8T33FS6222EPGI8	IDT8T33FS6222EPGI	52-Lead TQFP, Lead-Free	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “G” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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