Description

The 8V19N491-36 is a fully integrated FemtoClock® NG jitter attenuator and clock synthesizer. The device is designed as a high-performance clock solution for conditioning and frequency/phase management of wireless base station radio equipment boards. The device is optimized to deliver excellent phase noise performance as required in GSM, WCDMA, LTE, and LTE-A radio board implementations. The device supports JESD204B subclass 0 and 1 clocks.

A two-stage PLL architecture supports both jitter attenuation and frequency multiplication. The first stage PLL is the jitter attenuator and uses an external VCXO for best possible phase noise characteristics. The second stage PLL locks on the VCXO-PLL output signal and synthesizes the target frequency.

The 8V19N491-36 supports the clock generation of high-frequency clocks from the selected VCO and low-frequency synchronization signals (SYSREF). SYSREF signals are internally synchronized to the clock signals. Delay functions exist for achieving alignment and controlled phase delay between system reference and clock signals and to align/delay individual output signals. The four redundant inputs are monitored for activity. Four selectable clock switching modes are provided to handle clock input failure scenarios. Auto-lock, individually programmable output frequency dividers, and phase adjustment capabilities are added for flexibility.

The device is configured through a 3/4-wire SPI interface and reports lock and signal loss status in internal registers and via a lock detect (LOCK) output. Internal status bit changes can also be reported via the nINT output. The 8V19N491-36 is ideal for driving converter circuits in wireless infrastructure, radar/imaging, and instrumentation/medical applications. The device is a member of the high-performance clock family from Renesas.

Typical Applications

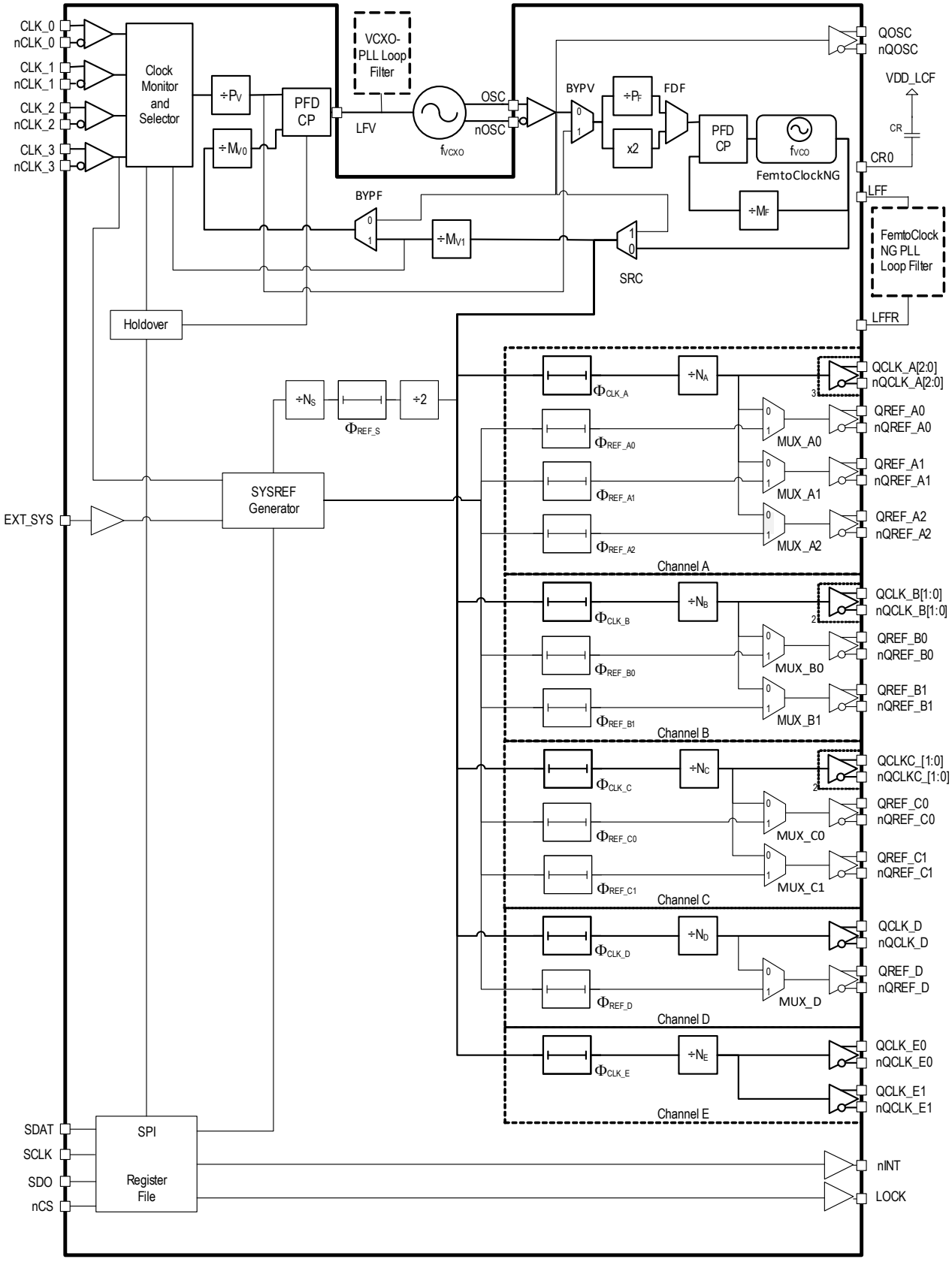
- Wireless infrastructure applications: GSM, WCDMA, LTE, and LTE-A
- Ideal clock driver for jitter-sensitive ADC and DAC circuits
- Low-phase noise clock generation
- Ethernet line cards
- Radar and imaging
- Instrumentation and medical

Features

- High-performance clock RF-PLL with support for JESD204B
- Optimized for low phase noise: -152.5dBc/Hz (800kHz offset; 245.76MHz clock)
- Integrated phase noise of 65fs RMS typical (12kHz–20MHz) at 737.28MHz
- Dual-PLL architecture
- First PLL stage with external VCXO for clock jitter attenuation
- Second PLL with internal FemtoClock NG PLL: 3686.4MHz
- Six output channels with a total of 19 outputs, organized in:
  - Four JESD204B channels (device clock and SYSREF output) with two, four, and six outputs
  - One clock channel with two outputs
  - One VCXO output
- Configurable integer clock frequency dividers
- Supported clock output frequencies include: 3686.4, 1843.2, 1228.8, 737.28, 614.4, 368.4, 307.2, 245.76, 153.6, 122.88, and 61.44MHz
- Low-power LVPECL/LVDS outputs support configurable signal amplitude, DC and AC coupling, and LVPECL, LVDS line terminations techniques
- Phase delay circuits
  - Clock phase delay with 256 steps of 271ps and a range of 0 to 69.173ns
  - Individual SYSREF phase delay with 8 steps of 271ps
  - Additional individual SYSREF fine phase delay with eight 25ps steps
  - Global SYSREF signal delay with 256 steps of 543ps and a range of 0 to 138.346ns
- Redundant input clock architecture with four inputs including:
  - Input activity monitoring
  - Manual and automatic, fault-triggered clock selection modes
  - Priority controlled clock selection
  - Digital holdover and hitless switching
  - Differential inputs accept LVDS and LVPECL signals
- SYSREF generation modes include internal and external trigger mode for JESD204B
- Supply voltage: 3.3V
- SPI Interface, 3/4 wire configurable
- SPI and control I/O voltage: 1.8V/3.3V (selectable)
- Package: 11 × 11 mm, 100-CABGA
- Temperature range: -40°C to +85°C

Block Diagram

Figure 1. Block Diagram (f_{VCO} = 3686.4MHz)



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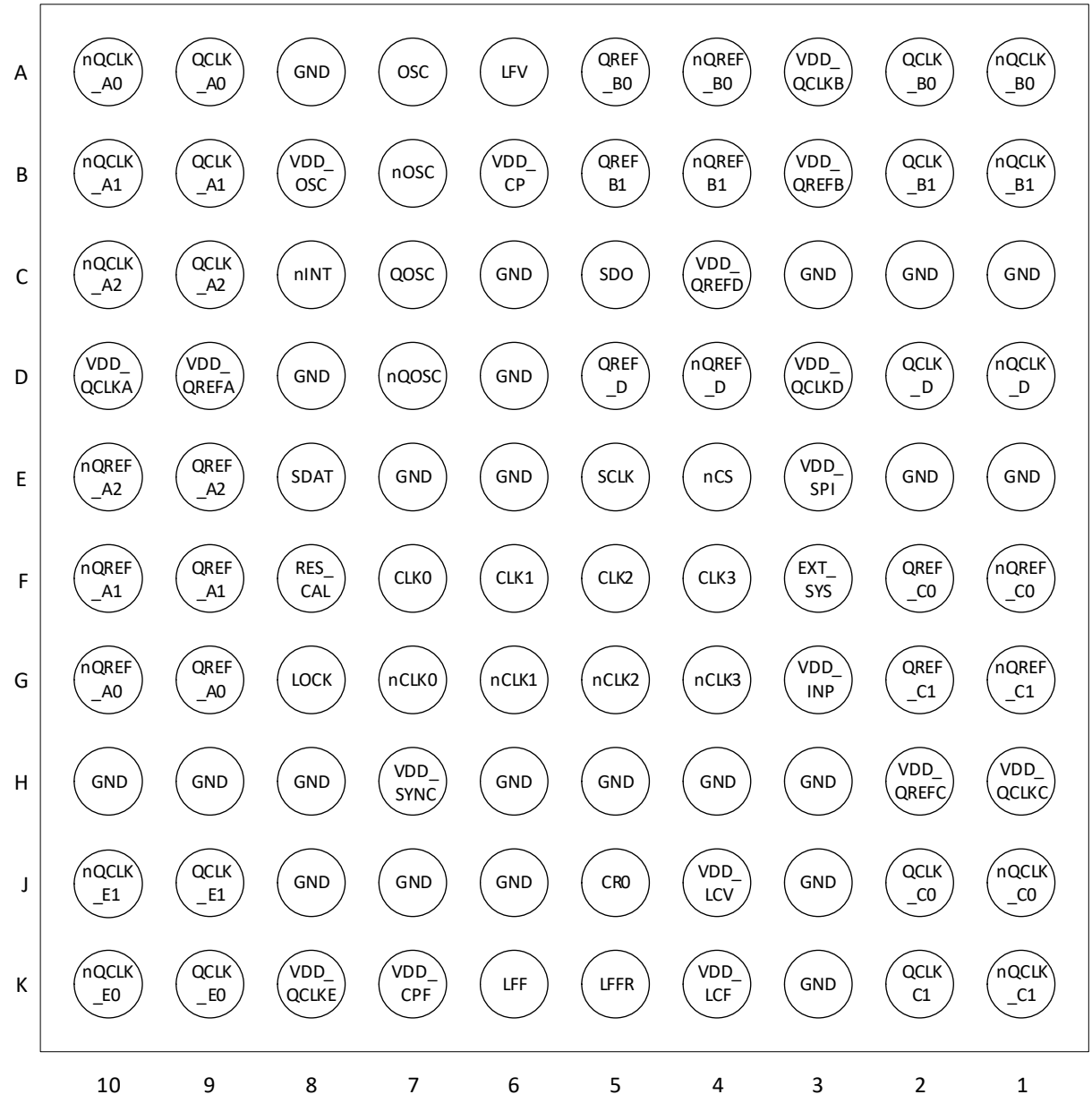
Ball Map

Figure 2. Ball Map for 100-CABGA, 1mm Ball Pitch 11 × 11 × 1.1 mm Package (Bottom View)



Pin Descriptions

Table 1. Pin Descriptions[a]

Ball	Name	Type[b]		Description
F7	CLK_0	Input	PD	Device clock 0 inverting and non-inverting differential clock input. Inverting input is biased to V_{DD_V} /2 by default when left floating. Compatible with LVPECL, LVDS, and LVCMOS signals.
G7	nCLK_0		PD/PU	
F6	CLK_1	Input	PD	Device clock 1 inverting and non-inverting differential clock input. Inverting input is biased to V_{DD_V} /2 by default when left floating. Compatible with LVPECL, LVDS, and LVCMOS signals.
G6	nCLK_1		PD/PU	
F5	CLK_2	Input	PD	Device clock 2 inverting and non-inverting differential clock input. Inverting input is biased to V_{DD_V} /2 by default when left floating. Compatible with LVPECL, LVDS, and LVCMOS signals.
G5	nCLK_2		PD/PU	
F4	CLK_3	Input	PD	Device clock 3 inverting and non-inverting differential clock/SYSREF input. Inverting input is biased to V_{DD_V} /2 by default when left floating. Compatible with LVPECL, LVDS, and LVCMOS signals. See SR_INSEL register bit for input selection.
G4	nCLK_3		PD/PU	
A9, A10	QCLK_A0, nQCLK_A0	Output	-	Differential clock output A0 (Channel A). Configurable LVPECL/LVDS style and amplitude.
B9, B10	QCLK_A1, nQCLK_A1	Output	-	Differential clock output A1 (Channel A). Configurable LVPECL/LVDS style and amplitude.
C9, C10	QCLK_A2, nQCLK_A2	Output	-	Differential clock output A2 (Channel A). Configurable LVPECL/LVDS style and amplitude.
G9, G10	QREF_A0, nQREF_A0	Output	-	Differential SYSREF/clock output REF_A0 (Channel A). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style, and amplitude for clock operation.
F9, F10	QREF_A1, nQREF_A1	Output	-	Differential SYSREF/clock output REF_A1 (Channel A). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style, and amplitude for clock operation.
E9, E10	QREF_A2, nQREF_A2	Output	-	Differential SYSREF/clock output REF_A2 (Channel A). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style, and amplitude for clock operation.
A2, A1	QCLK_B0, nQCLK_B0	Output	-	Differential clock output B0 (Channel B). Configurable LVPECL/LVDS style and amplitude.
B2, B1	QCLK_B1, nQCLK_B1	Output	-	Differential clock output B1 (Channel B). Configurable LVPECL/LVDS style and amplitude.
A5, A4	QREF_B0, nQREF_B0	Output	-	Differential SYSREF/clock output REF_B0 (Channel B). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style, and amplitude for clock operation.
B5, B4	QREF_B1, nQREF_B1	Output	-	Differential SYSREF/clock output REF_B1 (Channel B). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style, and amplitude for clock operation.
J2, J1	QCLK_C0, nQCLK_C0	Output	-	Differential clock output C0 (Channel C). Configurable LVPECL/LVDS style and amplitude.
K2, K1	QCLK_C1, nQCLK_C1	Output	-	Differential clock output C1 (Channel C). Configurable LVPECL/LVDS style and amplitude.

Table 1. Pin Descriptions[a] (Cont.)

Ball	Name	Type[b]		Description
F2, F1	QREF_C0, nQREF_C0	Output	-	Differential SYSREF/clock output REF_C0 (Channel C). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style, and amplitude for clock operation.
G2, G1	QREF_C1, nQREF_C1	Output	-	Differential SYSREF/clock output REF_C1 (Channel C). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style, and amplitude for clock operation.
D2, D1	QCLK_D, nQCLK_D	Output	-	Differential clock output D (Channel D). Configurable LVPECL/LVDS style and amplitude.
D5, D4	QREF_D, nQREF_D	Output	-	Differential SYSREF/clock output REF_D (Channel D). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
K9, K10	QCLK_E0, nQCLK_E0	Output	-	Differential clock output E0. Configurable LVPECL/LVDS style and amplitude.
J9, J10	QCLK_E1, nQCLK_E1	Output	-	Differential clock output E1. Configurable LVPECL/LVDS style and amplitude.
C7, D7	QOSC, nQOSC	Output	-	Differential VCXO-PLL clock outputs. Configurable LVPECL/LVDS style and amplitude.
C8	nINT	Output	-	Status output pin for signaling internal changed conditions. Selectable 1.8/3.3V LVCMOS interface levels.
G8	LOCK	Output	-	PLL lock detect status output for both PLLs. Selectable 1.8/3.3V LVCMOS interface levels.
F3	EXT_SYS	Input	PD	External SYSREF pulse trigger input. 1.8 LVCMOS interface levels.
E8	SDAT	Input/ Output	PU	Serial Control Port SPI Mode Data Input and Output (3-wire mode) and Data Input (4-wire mode). Register-selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V and set to input.
E5	SCLK	Input	PD	Serial Control Port SPI Mode Clock Input. Register-selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V.
E4	nCS	Input	PU	Serial Control Port SPI Chip Select Input. Register-selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V.
C5	SDO	Output	-	Serial Control Port SPI Mode Data Output (4-wire mode). Pin is not used in SPI 3-wire mode. Register-selectable 1.8V/3.3V LVCMOS interface levels.
J5	CR0	Analog	-	Internal VCO regulator bypass capacitor. Use a 4.7 µF capacitor between the CR0 and the VDD_LCF terminals.
A6	LFV	Output	-	VCXO-PLL charge pump output. Connect to the loop filter for the external VCXO.
A7	OSC	Input	PD	VCXO non-inverting and inverting differential clock input. Inverting input is biased to V_{DD_V} /2 by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
B7	nOSC		PD/PU	
K6	LFF	Output	-	Loop filter/charge pump output for the FemtoClock NG PLL. Connect to the external loop filter.
K5	LFFR	Analog	-	Ground return path pin for the VCO loop filter.
F8	RES_CAL	Analog	-	Connect a 2.8 kΩ (1%) resistor to GND for output current calibration.

Table 1. Pin Descriptions[a] (Cont.)

Ball	Name	Type[b]		Description
A8, C1, C2, C3, C6, D6, D8, E1, E2, E6, E7, H3, H4, H5, H6, H8, H9, H10, J3, J6, J7, J8, K3	GND	Power	-	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
D10	VDD_QCLKA	Power	-	Positive supply voltage (3.3V) for the QCLK_A[2:0] outputs.
D9	VDD_QREFA	Power	-	Positive supply voltage (3.3V) for the QREF_A[2:0] outputs.
A3	VDD_QCLKB	Power	-	Positive supply voltage (3.3V) for the QCLK_B[2:0] outputs.
B3	VDD_QREFB	Power	-	Positive supply voltage (3.3V) for the QREF_B[2:0] outputs.
H1	VDD_QCLKC	Power	-	Positive supply voltage (3.3V) for the QCLK_C[1:0] outputs.
H2	VDD_QREFC	Power	-	Positive supply voltage (3.3V) for the QREF_C[1:0] outputs.
D3	VDD_QCLKD	Power	-	Positive supply voltage (3.3V) for the QCLK_D outputs.
C4	VDD_QREFD	Power	-	Positive supply voltage (3.3V) for the QREF_D outputs.
K8	VDD_QCLKE	Power	-	Positive supply voltage (3.3V) for the QCLK_E[1:0] outputs.
E3	VDD_SPI	Power	-	Positive supply voltage (3.3V) for the SPI interface.
G3	VDD_INP	Power	-	Positive supply voltage (3.3V) for the differential inputs (CLK_0 to CLK_3).
J4	VDD_LCV	Power	-	Positive supply voltage (3.3V).
K4	VDD_LCF	Power	-	Positive supply voltage (3.3V).
K7	VDD_CPF	Power	-	Positive supply voltage (3.3V) for internal FemtoClock NG circuits.
B8	VDD_OSC	Power	-	Positive supply voltage (3.3V) for OSC, nOSC input and QOSC, nQOSC output.
B6	VDD_CP	Power	-	Positive supply voltage (3.3V) for internal VCXO_PLL circuits.
H7	VDD_SYNC	Power	-	Positive supply voltage (3.3V).

[a] See Application Information for important information on power supply filtering.

[b] PU (pull-up) and PD (pull-down) indicate internal input resistors. See Figure 46 for values.

Principles of Operation

Overview

The 8V19N491-36 generates low-phase noise, synchronized clock and SYSREF output signals locked to an input reference frequency. The device contains two PLLs with configurable frequency dividers. The first PLL (VCXO-PLL, suffix V) uses an external VCXO as the oscillator and provides jitter attenuation. The external loop filter is used to set the VCXO-PLL bandwidth frequency in conjunction with internal parameters. The second, low-phase noise PLL (FemtoClock NG, suffix F) multiplies the VCXO-PLL frequency to 3686.4MHz. The FemtoClock NG PLL is completely internal and provides a central timing reference point for all output signals. From this point, fully synchronous dividers generate the output frequencies and the internal timing references for JESD204B support. The device supports the generation of SYSREF pulses synchronous to the clock signals.

There are five channels consisting of clock and/or SYSREF outputs. The clock outputs are configurable with support for LVPECL or LVDS formats and a variable output amplitude. Clock and SYSREF offer adjustable phase delay functionality. Individual output channels and unused circuit blocks support user-configurable powered-down states for operating with lower power consumption. The register map, accessible through SPI interface with read-back capability controls the main device settings and delivers device status information. For redundancy purpose, there are four selectable reference frequency inputs and a configurable switch logic with priority-controlled auto-selection and holdover support.

Phase-Locked Loop Operation

Frequency Generation

Table 2 displays the available frequency dividers for clock generation. The dividers must be set by the user to match input, VCXO and VCO frequency to achieve frequency and phase lock on both PLLs. The frequency of the external VCXO is selected by the user; the internal VCO frequency is set to 3686.4MHz. Table 3 shows example divider configurations for typical wireless infrastructure applications.

Table 2. PLL Operation and Divider Values

MUX and Divider Setting	Range	Operation for f_{VCO} = 3686.4MHz			Frequency Synthesis FemtoClock NG Bypassed
		Jitter Attenuation, Dual-PLL with Deterministic Input-to-Output Delay	Jitter Attenuation, Dual-PLL	Frequency Synthesis VCXO-PLL Bypassed	
SRC	0, 1	0	0	0	1
BYPV	0, 1	0	0	1	0
BYPF	0, 1	1	0	X	X
VCXO-PLL Pre-Divider P_V	÷1…÷4095: (12 bit)	Input frequency $f_{CLK} = P_V \cdot \frac{f_{VCXO}}{P_F} \cdot \frac{M_F}{M_{V0} \cdot M_{V1}}$	Input frequency $f_{CLK} = f_{VCXO} \cdot \frac{P_V}{M_{V0}}$	Input frequency $f_{CLK} = f_{VCO} \cdot \frac{P_V \cdot P_F}{M_F}$	Input frequency $f_{CLK} = f_{VCXO} \cdot \frac{P_V}{M_{V0}}$
VCXO-PLL Feedback Divider M_{V0}	÷1…÷4095: (12 bit)		M_{V1} setting is not applicable to PLL operation	M_{V0} and M_{V1} settings are not applicable to the PLL operation.	M_{V1}, P_F and M_F settings are not applicable to VCXO-PLL operation
PLL Feedback Divider[a] M_{V1}	÷4…÷511: (9 bit)			P_F: Set P_F to 0.5 in above equation if the frequency doubler is engaged by setting FDF = 1	
FemtoClock NG Pre-Divider P_F	÷1…÷63: (6 bit)	VCXO frequency: $f_{VCXO} = f_{VCO} \cdot \frac{P_F}{M_F}$ P_F: Set P_F to 0.5 in above equation if the frequency doubler is engaged by setting FDF = 1			
FemtoClock NG Feedback Dividers M_F	÷8 …÷511 (9 bit)				

Table 2. PLL Operation and Divider Values (Cont.)

MUX and Divider Setting	Range	Operation for f_{VCO} = 3686.4MHz			Frequency Synthesis FemtoClock NG Bypassed
		Jitter Attenuation, Dual-PLL with Deterministic Input-to-Output Delay	Jitter Attenuation, Dual-PLL	Frequency Synthesis VCXO-PLL Bypassed	
Output Divider N*x* (x = A, B, C, D, E)	÷1…÷200:	Output frequency $f_{OUT} = \frac{f_{VCO}}{N_X}$			Output frequency $f_{OUT} = \frac{f_{VCXO}}{N_X}$
SYSREF Divider[b] N_S	÷64…÷12800: 2 × {2,4,8,16} × {2,3,4,5} × {2,4} × {2,4} × {2,3,4,5}	SYSREF frequency/rate $f_{SYSREF} = \frac{f_{VCO}}{2N_S}$			SYSREF frequency/rate $f_{SYSREF} = \frac{f_{VCXO}}{2N_S}$

[a] For input monitoring, configure MV1 as described in Monitoring and LOS of Input Signal.

[b] For SYSREF operation, configure SYNC[5:0] as described in Synchronizing SYSREF and Clock Output Dividers.

VCXO-PLL

The prescaler P_V and the VCXO-PLLs feedback divider M_{V0} and M_{V1} require configuration to match the input frequency to the VCXO-frequency. The BYPF setting allows to route the VCXO-PLLs feedback path through the M_{V0} divider. Alternatively, the feedback path is routed through the second PLL and both the M_{V0} and M_{V1} feedback divider. M_{V0} has a divider value range of 12 bit; M_{V1} has 9 bit. The feedback path through the second PLL, in combination with the divider setting P_F = ÷1, is the preferred setting for achieving deterministic delay from the clock input to the outputs.

Multiple divider settings are available to enable support input frequencies of 245.76, 122.88, 61.44, and 30.72MHz and the VCXO-frequencies of 61.44, 38.4, 30.72, 122.88, and 245.76MHz. In addition, the range of available input and feedback dividers allows to adjust the phase detector frequency independent on the input and VCXO frequencies. In general, the phase detector can be set into the range from 120kHz to the input reference frequency. The VCXO-PLL charge pump current is controllable via a register and can be set in 50µA steps from 50µA to 1.6mA. The VCXO-PLL can be bypassed: the FemtoClock NG PLL locks to the pre-divider input frequency.

Table 3. Example Configurations for f_{VCXO} = 122.88MHz[a]

Input Frequency (MHz)	VCXO-PLL Divider Settings		f_{PFD} (MHz)
	P_V	M_{V0}	
245.76	2	1	122.88
	32	16	7.68
	256	128	0.96
	2048	1024	0.12
122.88	1	1	122.88
	16	16	7.68
	128	128	0.96
	1024	1024	0.12

[a] BYPF = 0

Table 4. Example Configurations for f_{VCXO} = 38.4MHz[a]

Input Frequency (MHz)	VCXO- PLL Divider Settings		f_{PFD} (MHz)
	P_V	M_{V0}	
245.76	32	5	7.68
	128	20	1.92
	512	80	0.48
	2048	320	0.12
122.88	16	5	7.68
	64	20	1.92
	256	80	0.48
	1024	320	0.12

[a] BYPF = 0

Table 5. VCXO-PLL Bypass Settings

BYPV	Operation
0	VCXO-PLL operation.
1	VCXO-PLL bypassed and disabled. The reference clock for the FemtoClock NG PLL is the input clock divided by the pre-divider P_V. The input clock selection must be set to manual by the user. Clock switching and holdover are not defined. The device will not attenuate input jitter. No external VCXO component and loop filter required.

Table 6. PLL Feedback Path Settings

BYPF	Operation[a]
0	VCXO-PLL feedback path through the M_{V0} divider. FemtoClock NG feedback path uses the M_F divider.
1	VCXO-PLL feedback path through the $M_{V1} \times M_{V0}$ dividers. FemtoClock NG feedback path uses the M_F divider. Preferred setting for achieving deterministic delay from input to the outputs.

[a] Regardless of the selected internal feedback path, the MV1 divider should be set to match its internal output frequency to the input reference frequency: the MV1 output signal is the internal reference for input loss-of-signal detect.

FemtoClock NG PLL

This PLL locks to the output signal of the VCXO-PLL (BYPV = 0). It requires configuration of the frequency doubler FDF or the pre-divider PF and the feedback divider MF to match the VCXO-PLL frequency to the VCO frequency of 3686.4MHz. This PLL is internally configured to high bandwidth. Best phase noise is typically achieved by engaging the internal frequency doubler (FDF = 1). If engaged, the signal from the first PLL stage is doubled in frequency, increasing the phase detector frequency of the FemtoClock NG PLL. Enabling the frequency doubler disables the frequency pre-divider PF. If the frequency doubler is not used (FDF = 0), the PF pre-divider must be configured. Typically, PF is set to ÷1 to keep the phase detector frequency as high as possible. Set PF to other divider values to achieve specific frequency ratios (1 to 19.2, 1 to 76.8, etc.) between first and second PLL stage.

Table 7. Frequency Doubler

FDF	Operation
0	Frequency doubler off. PF divides clock signal from VCXO-PLL or input (in bypass)
1	Frequency doubler on. Signal from VCXO-PLL or input (in bypass) is doubled in frequency. PF divider has no effect.

Table 8. Output Divider Source Signal

SRC	Operation
0	The output divider input signal is the FemtoClock NG PLL.
1	The output divider input signal is the VCXO-PLL output signal. The FemtoClock NG PLL is bypassed.

Table 9. Example PLL Configurations

VCXO-Frequency (MHz)	FemtoClock NG Divider Settings				Output Frequency (MHz)
	FDF	PF	MF	Nx[a]	
122.88	x2	–	15	10	368.64
122.88	–	1	30	12	307.2
				15	245.76
				30	122.88
				60	61.44

[a] *x* = A to E

Channel Frequency Divider

The device supports five independent channels, A to E. Each channel has a frequency divider N*x* (*x* = A to E) that divides the VCO frequency to the output frequency. Each divider be individually set to a value in the range of ÷1 to ÷200. See Table 10 for typical divider values and Table 30 for the complete set of supported divider values.

Table 10. Integer Frequency Divider Settings

Channel Divider N*x*[a]	Output Clock Frequency (MHz)
	f_{VCO} = 3686.4MHz
÷1	3686.4
÷2	1843.2
÷3	1228.8
÷4	921.6
÷5	737.28
÷6	614.4
÷8	460.8
÷10	368.64
÷12	307.2
÷15	245.76
÷16	230.4
÷18	204.8
÷20	184.32
÷24	153.6
÷30	122.88
÷32	115.2
÷36	102.4
÷40	92.4
÷48	76.8
÷50	73.728
÷60	61.44
÷72	51.2
÷80	46.08
÷96	38.4
÷100	36.864
÷120	30.72
÷128	28.8
÷150	24.576
÷160	23.04
÷200	18.432

[a] *x* = A to E

Redundant Inputs

The four inputs are compatible with LVDS, LVPECL, and single-ended LVCMOS signal formats. For applicable input interface circuits, see Application Information.

Monitoring and LOS of Input Signal

The device's four inputs are individually monitored for activity. Inactivity is defined by a static input signal.

The clock input monitors compare the device input frequency (f_{CLK}) to the frequency of the VCO divided by M_{V1} (regardless of the internal feedback path using or not using M_{V1}). A clock input is declared invalid with the corresponding LOS (Loss-of-input-signal) indicator bit set after three consecutive missing clock edges. For correct operation of the LOS detect circuit, M_{V1} must be powered on by setting PD_MV1 = 0. The MV1 divider must be set so that the LOS detect reference frequency matches the input frequency. For instance, if the input frequency is 245.76MHz, M_{V1} should be set to ÷15: The VCO frequency of 3686.4MHz divided by 15 equals the input frequency of 245.76MHz. For an input frequency of 122.88MHz, set M_{V1} to ÷30. Failure to set M_{V1} to match the input frequency will result in added latency to the LOS circuit (if $f_{VCO} \div M_{V1} < f_{CLK}$) or false LOS indication (if $f_{VCO} \div M_{V1} > f_{CLK}$).

The minimum frequency that the circuit can monitor is: $f_{VCO} / M_{V1(MAX)}$ = 7.21MHz. In applications with an input frequency lower than 7.21MHz, disable the monitor to trigger the status flags by setting BLOCK_LOR = 1.

If differential input signals are applied, the input will also detect an LOS condition in case of a zero differential input voltage.

Input Re-Validation

A clock input is declared valid and the corresponding LOS status bit is reset after the clock input signal returns for user-configurable number of consecutive input periods. This re-validation of the selected input clock is controlled by the CNTV setting (verification pulse counter).

Clock Selection

The 8V19N491-36 supports four input selection modes: manual, short-term holdover, and two automatic switch modes. The modes are described in the following table.

Table 11. Clock Selection Settings

Mode	Description	Application
Manual nM/A[1:0] = 00	Input selection follows user-configuration of SEL[1:0]. Selection is *never* changed by the internal state machine. A failing reference clock will cause an LOS event and the PLL will unlock if the failing clock is selected. Re-validation of the selected input clock will result in the PLL to re-lock on that input clock.	Startup and external selection control
Automatic nM/A[1:0] = 01	Input selection follows LOS status by user preset input switch priorities. A failing input clock will cause an LOS event for that clock input. If the selected clock has an LOS event, the device will immediately initiate a clock fail-over switch. The switch target is determined by pre-set input priorities. No valid clock scenario: If no valid input clocks exist, the device will not attempt to switch and will not enter the holdover state. The PLL is not locked. Re-validation of any input clock that is not the selected clock will result in the PLL to attempt to lock on that input clock. For more information Revertive Switching	Multiple inputs with qualified clock signals
Shot-term Holdover nM/A[1:0] = 10	Input selection follows user-configuration of SEL[1:0]. Selection is never changed by the internal state machine. A failing reference clock will cause an LOS event. If the selected reference fails, the device will enter holdover *immediately*. Re-validation of the selected input clock is controlled by the CNTV setting. A successful re-validation will result in the PLL to re-lock on that input clock. For more information Short-Term Holdover	Single reference

Table 11. Clock Selection Settings (Cont.)

Mode	Description	Application
Automatic with holdover nM/A[1:0] = 11	Input selection follows LOS status by user preset input priorities. Each failing input clock will cause an LOS event for that clock input. If the *selected* clock detects an LOS event, the device will go into holdover and the hold-off down-counter (CNTH) starts. The device initiates a clock fail-over switch *after* expiration of the hold-off counter. The switch target is determined by the preset input priorities. *No valid clock scenario:* If no valid input clocks exist, the device will not attempt to switch and will remain in the holdover state. Re-validation of any input clock will result in the PLL to attempt to lock on that input clock. For more information Automatic with Holdover (nM/A[1:0] = 11) and Revertive Switching	Multiple inputs

Holdover

In holdover state, the output frequency and phase is derived from an internal, digital value based on previous frequency and phase information. Holdover characteristics are defined in Table 53.

Input Priorities

Configurable settings encompass four selectable priorities with the range 0 (lowest priority) to 3 (highest priority). The user can change the input priorities at any time. In the automatic switch modes, input priority changes may cause immediate input selection changes.

Hold-off Counter

A configurable down-counter applicable to the “Automatic with holdover” selection mode. The purpose of this counter is a deferred, user-configurable, input switch after an LOS event. The hold-off counter is triggered by a transition of ST_REF upon detection of an LOS event. The counter expires when a zero-transition occurs – this triggers a new reference clock selection. The counter is clocked by the frequency-divided VCXO-PLL signal. The CNTR setting determines the hold-off counter frequency divider and the CNTH setting the start value of the hold-off counter. For instance, set CNTR to a value of ÷131072 to achieve 937.5 Hz (or a period of 1.066 ms at f_{VCXO} = 122.88MHz): the 8-bit CNTH counter is clocked by 937.5Hz and the user-configurable hold-off period range is 0ms (CNTH = 0x00) to 272ms (CNTH = 0xFF). After the counter expires, it reloads automatically from the CNTH SPI register. After the LOS status bit (LS_CLK_*n*) for the corresponding input CLK_*n* has been cleared by the user, the input is enabled for generating a new LOS event.

The CNTR counter is only clocked if the device is configured in the clock selection mode “Automatic with holdover” *AND* the *selected* reference clock experiences an LOS event. Otherwise, the counter is automatically disabled (not clocked).

Revertive Switching

Revertive switching: is only applicable to the two automatic switch modes shown in Table 11. Revertive switching enabled: Re-validation of any non-selected input clock(s) will cause a new input selection according to the user-preset input priorities (revertive switch). An input switch is only done if the re-validated input has a higher priority than the currently selected reference clock.

Revertive switching disabled: Re-validation of a non-selected input clock has no impact on the clock selection. Default setting is revertive switching disabled.

Short-Term Holdover

If an LOS event is detected on the reference clock designated by the SEL[1:0] bits:

- Holdover begins immediately
- ST_REF, LS_REF go low immediately
- No transitions will occur of the active REF clock; ST_SEL[1:0] does not change
- The hold-off countdown is not active

When the designated reference clock resumes and has met the programmed validation count of consecutive rising edges:

- Holdover turns off
- ST_SEL[1:0] does not change
- ST_REF returns to 1

LS_REF can be cleared by an SPI write of 1 to that register

Automatic with Holdover (nM/A[1:0] = 11)

If an LOS event is detected on the active reference clock:

- Holdover begins immediately
- Corresponding ST_REF and LS_REF go low immediately
- Hold-off countdown begins immediately.

During this time, all clocks continue to be monitored and their respective ST_CLK, LS_CLK flags are active. LOS events will be indicated on ST_CLK, LS_CLK when they occur.

If the active reference clock resumes and is validated during the hold-off countdown:

- Its ST_CLK status flag will return high and the LS_CLK is available to be cleared by an SPI write of 1 to that register bit.
- No transitions will occur of the active REF clock; ST_SEL[1:0] does not change. LS_REF can be cleared by an SPI write of 1 to that register.
- Revertive bit has no effect during this time (whether 0 or 1)

When the hold-off countdown reaches zero:

If the active reference has resumed and has been validated during the countdown, it will maintain being the active reference clock

- ST_SEL1:0 does not change
- ST_REF returns to 1
- LS_REF can be cleared by an SPI write of 1 to that register
- Holdover turns off and the VCXO-PLL attempts to lock to the active reference clock

If the active reference has not resumed, but another (sorted by next priority) clock input CLK_*n* is validated, then

- ST_SEL1:0 changes to the new active reference
- ST_REF returns to 1
- LS_REF can be cleared by an SPI write of 1 to that register
- Holdover turns off

If there is no validated CLK:

- ST_SEL1:0 does not change
- ST_REF remains low
- LS_REF cannot be cleared by an SPI write of 1 to that register
- Holdover remains active

Revertive capability returns if REVS = 1.

VCXO-PLL Lock Detect (LOLV)

The VCXO-PLL lock detect circuit uses the signal phase difference at the phase detector as loss-of-lock criteria. Loss-of-lock is reported if the actual phase difference is larger than a configurable phase window set by the Φ_{MV0} and Φ_{PV} configuration bits. Configuration of the width window allows for an application-specific loss of lock reporting. A loss-of-lock state is reported through the nST_LOLV and nLS_LOLV status bit, see Table 23.

Setting the BLOCK_LOLV register bit will block the VCXO-PLL lock status from being reported to the LOCK pin (see Table 33).

Loss-of-Lock Window Description

The selected clock input signal is the reference signal (CLK) for lock detection. The rising edge of CLK defines the reference point t_0. Φ_{PV} configures the start of the lock window t_B (which occurs before t_0) and Φ_{MV0} configures the end of the window t_E (which occurs after t_0). The width of the lock window is defined by t_E - t_B. The VCXO-PLL declares lock when the rising edge of the feedback signal (FB) is within this window; otherwise, the PLL reports loss-of-lock.

Figure 3. Lock Detect Window

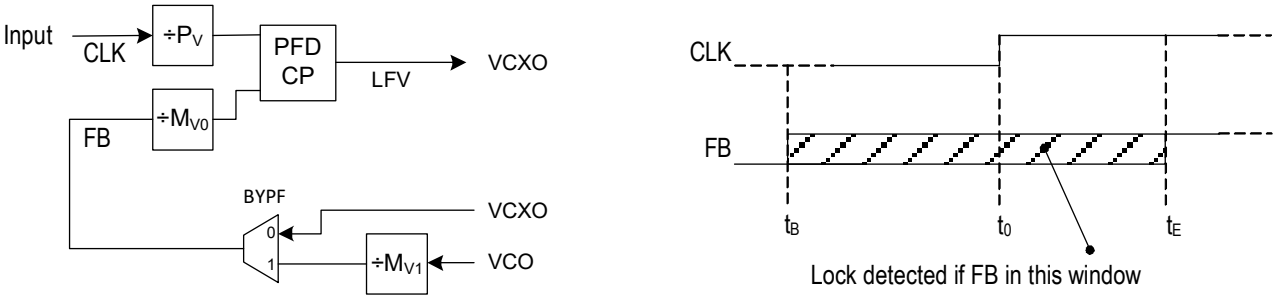


Table 12. t_B and t_E Calculation

Operation	Jitter Attenuation, Dual-PLL with Deterministic Input-to-Output Delay (BYPV = 0, BYPF = 1)	Jitter Attenuation, Dual-PLL (BYPV = 0, BYPF = 0)
t_B	$t_B = -\frac{2^{\Phi PV} - 1}{f_{CLK}}$	
t_E	$t_E = \frac{(2^{\Phi MV0} - 1) \cdot M_{V1}}{f_{VCO}}$	$t_E = \frac{2^{\Phi MV0} - 1}{f_{VCXO}}$

Figure 3 shows that Φ_{PV} configures the start and ΦM_{V0} the end of the window in integer multiples of PLL input and feedback periods. Both Φ_{PV} and Φ_{MV0} use three configuration bits with valid settings from 010 to 111 (2 to 7, decimal). This range allows configuring both t_S and t_E from 3 to 127 periods of the input signal (T_{IN}) and the feedback signal (T_{FB}), respectively, is implied.

Loss-of-Lock Window Configuration Example

With given P_V, M_{V0} and M_{V1} divider values, select the corresponding Φ_{PV} and Φ_{MV0} settings from Table 13 and apply the Φ_{PV} and Φ_{MV0} values to the ΦPV[1:0] and ΦMV0[1:0] registers. Table 12 shows the lock window calculation formulas. For instance, if an input frequency of 245.76MHz and a P_V divider of 128 is desired, set ΦPV[1:0] to a binary value of 100 (decimal 4). This results in t_B = -61.035ns (15 periods of 4.069ns). With a VCXO-PLL (BYPF = 0) and a VCXO frequency of 122.88MHz and M_{V0} = 64, select 011 (decimal 3) resulting in t_E = 56.96ns (7 periods of 8.138ns) and an overall lock detect window of t_E - t_B = 56.96ns + 61.035ns = 118.001ns. The user can select a smaller lock detect window. For instance, a P_V divider of 128 allows to set ΦPV[1:0] to 010, 011 or 100 (decimal 2 to 4). Correspondingly, a M_{V0} divider of 64 allows ΦMV0[1:0] settings from 010 to 011 (decimal 2 to 3). With smaller settings, the lock detect window size is reduced exponentially.

ΦPV[1:0] = 010 will set t_B to 3 × T_{CLK} and ΦPV[1:0] = 110 will set t_B to 63 × T_{CLK}. ΦMV0[1:0] = 010 will set t_E to 3 × T_{VCXO} and ΦMV0[1:0] = 110 will set t_E to 63 × T_{VCXO}.

Table 13. Recommended Lock Detector Phase Window Settings

P_V Divider Value	ΦPV[1:0] Setting	M_{V0} Divider Value	ΦMV0[1:0] Setting
1–31[a]	N/A	1–31[a]	N/A
32–63	010	32–63	010
64–127	≤ 011	64–127	≤ 011
128–255	≤ 100	128–255	≤ 100
256–511	≤ 101	256–511	≤ 101
512–1023	≤ 110	512–1023	≤ 110
1024 and higher	≤ 111	1024 and higher	≤ 111

[a] The PLL will be locked with these values but the PLL Lock Status bit and pin will not respond correctly.

FemtoClock NG Loss-of-Lock (LOLF)

FemtoClock NG-PLL loss-of-lock is signaled through the nST_LOLF (momentary) and nLS_LOLF (sticky, resettable) status bits, and can reported as hardware signal on the LOCK output as well as an interrupt signal on the nINT output.

Channel, Output, and JESD204B Logic

Channel

Each of the four channels A to D consists of one to three clock outputs and one associated to three SYSREF outputs. Each SYSREF output in a channel can be individually configured to generate JESD204B (SYSREF) signals or copy the clock signal of that channel. The fifth channel (E) consists of two clock outputs without SYSREF support in that channel.

If JESD204B/SYSREF operation is assigned to a QREF output, the channel logic controls the outputs: outputs automatically turn on and off in a SYSREF sequence. QREF outputs configured to clock operation can have individually configured output states.

Table 14. Channel Configuration[a]

MUX_*r*	0	1
Description	Clock configuration	JESD204B
QCLK_*y*	Clock signal	Clock signal
QREF_*r*		SYSREF/JESD204B
Frequency Divider	QCLK_*y* and QREF_*r*: N_x	QCLK_*y*: N_x QREF_*r*: N_S (Global to all QREF_*r*)
Phase Delay	QCLK_*y* and QREF_*r*: Φ_{CLK_x} Φ_{REF_r} settings do not apply	QCLK_*y*: Φ_{CLK_x} QREF_*r*: Φ_{REF_r}
Power Down	Per output	Per channel
Output Enable	Per output	Per output

[a] *x* = A to E. *y* = A0, A1, A2, B0, B1, C0, C1, D, E0, E1; *r* = A0, A1, A2, B0, B1, C0, C1, D

Differential Outputs

Table 15. Output Features

Output	Style	Amplitude[a]	Disable	Power Down	Termination
QCLK_*y*, QREF_*r* (Clock)	LVPECL	250-1000mV 4 steps	Yes	Yes	50Ω to V_T
	LVDS				100Ω differential[b]
QREF_*r* (SYSREF)	LVDS	500mV A[1:0] = 01	Controlled by SYSREF[c]		100Ω differential[b]
QOSC	LVPECL	250-750mV 3 steps	Yes	Yes	50Ω to V_T
	LVDS				100Ω differential[b]

[a] Amplitudes are measured single-endedly. Differential amplitudes supported are 500, 1000, 1500, and 2000mV.

[b] AC coupling and DC coupling supported.

[c] State of SYSREF outputs is controlled by an internal SYSREF state machine.

Table 16. Individual Clock Output Settings[a]

PD[b]	STYLE	EN[c]	A[1:0][d]	Output Power	Termination	State	Amplitude (mV)
1	X	X	X	Off	100Ω differential or no termination	Off	X
0	0	0	XX	On	100Ω differential (LVDS)	Disable (logic low)	X
		1	00			Enable	250
			01				500
			10				750
			11				1000
	1	0	XX		50Ω to V_T (LVPECL)	Disable (logic low)	X
		1	00		50Ω to V_T = V_{DD_V} - 1.50V (LVPECL)	Enable	250
			01		50Ω to V_T = V_{DD_V} - 1.75V (LVPECL)		500
			10		50Ω to V_T = V_{DD_V} - 2.00V (LVPECL)		750
			11		50Ω to V_T = V_{DD_V} - 2.25V (LVPECL)	Enable	1000

[a] Applicable to clock outputs: QCLK_*y* and QREF_*r* outputs in clock mode (MUX_*r* = 0).

[b] Power-down modes are available for the individual channels A-E and the outputs QCLK_y (A0 to E1) and QREF_*r*.

[c] Output enable is supported on each individual QCLK_*y* and QREF_*r* output.

[d] Output amplitude control is supported on each individual QCLK_*y* and QREF_*r* output.

Table 17. Individual SYSREF Output Settings[a]

PD	STYLE	EN	nBIAS	A[1:0]	Output Power	Termination	State	Amplitude (mV)
1	X	X	X	X	Off	100Ω differential or no termination	Off	X
0	0	0	0	01	On[b]	100Ω differential (LVDS)	Disable (logic low)	X
		1					Enable	500
		X	1	XX			Line bias[c]	XX
	1	0	0	01		50Ω to V_T = V_{DD_V} - 1.75V (LVPECL)	Disable (logic low)	X
		1					Enable	500

[a] Applicable QREF_r outputs when configured as SYSREF output (MUX_*r* = 1).

[b] Output amplitude should be set to a 500mV swing (A[1:0] to 01) by SPI. SYSREF output states are controlled by an internal state machine. An internal SYSREF event will automatically turn SYSREF outputs on. After the event, outputs are automatically turned off. Setting nBIAS = 1 will bias powered-off outputs to the LVDS midpoint voltage.

[c] Output (both Q, and nQ) bias the line to the differential signal cross-point voltage. Available if output is AC-coupled and set to LVDS style.

nPD	STYLE	A[1:0]	Output Power	Termination	Amplitude (mV)
0	X	X	Off	100Ω differential (LVDS) or no termination	X
1	0	00	On	100Ω differential (LVDS)	250
		01			500
		10			
		11			750
	1	00		50Ω to V_T = V_{DD_V} - 1.50V (LVPECL)	250
		01		50Ω to V_T = V_{DD_V} - 1.75V (LVPECL)	500
		10			
		11		50Ω to V_T = V_{DD_V} - 2.00V (LVPECL)	750

Table 18. QREF_r Setting for JESD204B Applications

BIAS_TYPE	nBIAS_*r*	QREF_r Outputs (LVDS, 500mV Amplitude)			Application
		Initial	During SYSREF Event	SYSREF Completed	
0	0	Static low (QREF = L, nQREF_*r* = H)	Start switching for the number of configured SYSREF pulses	Released to static low (QREF = L, nQREF_*r* = H)	QREF_*r* DC coupled
	1	Static low (QREF = L, nQREF_*r* = H)			
1	0	Static LVDS crosspoint level (QREF = nQREF_*r* = VOS)	Start switching for the number of configured SYSREF pulses	Released to static LVDS crosspoint level (QREF = nQREF_*r* = VOS)	QREF_*r* AC coupled
	1	Static LVDS crosspoint level (QREF = nQREF_*r* = VOS)			

Output Phase Delay

Output phase delay is independently supported on both clock and SYSREF outputs.

The phase delay on clock outputs Φ_{CLK_x}, SYSREF outputs coarse delay Φ_{REF_r} and global delay Φ_{REF_S} is derived from the internal VCO frequency of the second PLL (FemtoClock NG PLL). In configurations bypassing the second PLL by setting SRC = 1, the delay unit is derived from the frequency of the external VCXO: use f_{VCXO} instead of f_{VCO} in Table 19.

Table 19. Delay Circuit Settings[a]

Delay Circuit	Unit	Steps	Range (ns)	Alignment[b]
Clock[c] Φ_{CLK_x}	$\frac{1}{f_{VCO}} = 271ps$	256	0–69.173[d]	Incident rising clock edges are aligned, independent on the divider N_*x* across channels
SYSREF Φ_{REF_r}	Coarse delay: $\frac{1}{f_{VCO}} = 271ps$	8	0–1.899ns[d]	SYSREF rising edge is aligned to the incident rising clock edge across channels
	Fine delay: 0, 25, 50, 75, 85, 110, 135, 160ps	8	0–0.160[e]	
SYSREF (Global) Φ_{REF_S}	$\frac{2}{f_{VCO}} = 543ps$	256	0–138.346[d]	Global alignment of SYSREF signals

[a] Supports ≥ 12 SYSREF rising edge stops within a device clock period of 4.096ns (245.76MHz) and 8.137 ns (122.88MHz), respectively

[b] Default configuration (all delay settings = 0)

[c] Clock output inversion supported by setting phase delay to 180° setting

[d] Exact delay value

[e] ±20% delay variation over PVT

Configuration for JESD204B Operation

Synchronizing SYSREF and Clock Output Dividers

The SYNC[5:0] divider controls the release of SYSREF pulses at coincident QCLK_y clock edges. For SYSREF operation, set the SYNC divider value to half of the least common multiple of the clock divider values Nx (x = A to E). For example, if NA = NB = ÷2, NC = ND = ÷3, NE = ÷4, set the SYNC divider to ÷6.

SYSREF Generation

A SYSREF event is the generation of one or more consecutive pulses on the QREF outputs. An event can be triggered by SPI commands or by a signal-transition on the EXT_SYS or CLK_3 input. The number of SYSREF pulses generated is programmable from 1 to 255. The SYSREF signal can also be programmed to be continuous. The SYSREF pulse rate is configurable to the frequencies shown in Table 20. SYSREF output pulses are aligned to coincident rising clock edges of the clock outputs QCLK_*y*. Device settings for phase alignment between QCLK_*y* and QREF_*r* outputs is discussed in QCLK to QREF Phase Alignment. The following SYSREF pulse generation modes are available and configurable by SPI:

- Counted pulse mode – 1 to 255 pulses are generated by the device. SYSREF activity stops automatically after the transmission of the selected number of pulses and the QREF output becomes disabled.
- Continuous mode – The SYSREF signal is a clock signal.

The generation of SYSREF pulses is configured by SPI commands and is available after the initial setup of output clock divider and QREF phase delay stages. A SYSREF event will automatically turn on the SYSREF outputs. After the event, SYSREF outputs are automatically turned off. SYSREF outputs with the nBIAS bit set high will bias the outputs at the LVDS crosspoint voltage level (requires BIAS_TYPE = 1).

Table 20. SYSREF Generation[a]

N_S	SYSREF Operation (f_{SYSREF})
	f_{VCO} = 3686.4MHz
÷80, ÷160, ÷320, ÷640, ÷1280, ÷2560, ÷5120	46.08, 23.04, 11.52, 5.76, 2.88, 1.44, 0.72
÷96, ÷192, ÷288, ÷384, ÷480, ÷576, ÷768, ÷1536, ÷3072	38.4, 19.2, 12.8, 9.6, 6.4, 4.8, 2.4, 1.2
÷120, ÷240, ÷480, ÷960, ÷1440, ÷1920, ÷2400, ÷2880, ÷3840	30.72, 15.36, 7.68, 3.84, 2.56, 1.92, 1.536, 1.28, 0.96
÷128, ÷256, ÷512, ÷1024, ÷2048, ÷4096	28.8, 14.4, 7.2, 3.6, 1.8, 0.9

[a] Example frequencies

Internal SYSREF Generation

SYSREF generation is set to internal (SRG = 0). The SRO setting defines if SYSREF pulses are counted or continuous and the NS[7:0] divider sets the frequency. In counted pulse mode, the SRPC register contains the number of pulses to generate. Any number from 1 to 255 pulses can be generated. SYSREF pulses are generated upon completion of the SPI command RS (SYSREF release). Setting RS activates the SYSREF outputs, loads the number of pulses from the SRPC register, and starts the generation of SYSREF pulses synchronized to the incident edge of the clock signals. After the programmed number of pulses are generated, SYSREF outputs will go into logic low state or bias the output voltage to the static LVDS crosspoint level (see Table 18 for settings and details). In continuous mode, SYSREF is a clock signal and the content of the SRPC signal is ignored. For proper operation of this mode, set SR_INSEL bit to 0.

External SYSREF Generation

SYSREF generation is set to external (SRG = 1): SYSREF pulses are generated in response to the detection of a rising edge at the EXT_SYS or CLK_3 input (see Table 21 for selection of the active, external SYSREF input). The EXT_SYS (or CLK_3) input rising edge releases SYSREF pulses. Both SRO and SRPC register settings apply as in internal SYSREF generation mode for generating single shot and repetitive SYSREF output signals. Set RS = 1 to prepare for SYSREF generation; the generation of SYSRE pulses is triggered by a rising edge at EXT_SYS or CLK_3 input.

Table 21. External SYSREF Input

SR_INSEL	Operation
0 (Default)	EXT_SYS (single-ended) is the external SYSREF input
1	CLK_3 (differential) is the external SYSREF input. CLK_3 is not available as clock input to drive the first-stage PLL.

QCLK to QREF (SYSREF) Phase Alignment

Figure 4 and Table 22 show how to achieve output phase alignment between the QCLK_*y* clock and the QREF_*r* SYSREF outputs. The output phase will be different for different N_x dividers. For a given example in Figure 4, the closest (smallest phase error) output alignment is achieved by setting the clock phase delay register Φ_{QCLK_Y} to 0x00, the coarse SYSREF output phase delay register Φ_{REF_r} to 0x01, fine SYSREF delay to ΦREF_F_*r* = *1,* and the global Φ_{REF_S} delay register to 0x30.

With the manipulation of the phase delays, the QREF_*r* output phase can be in advance or delay of the QCLK_y phase, which is applicable in JESD204B application. Phase delay settings and propagation delays are dependent on the clock and SYSREF frequency dividers, but independent of the SYSREF generation mode (SRG = 0 or SRG = 1). Recommended phase delay setting for several device configurations are shown in Table 22.

Figure 4. QCLK to QREF Phase Alignment

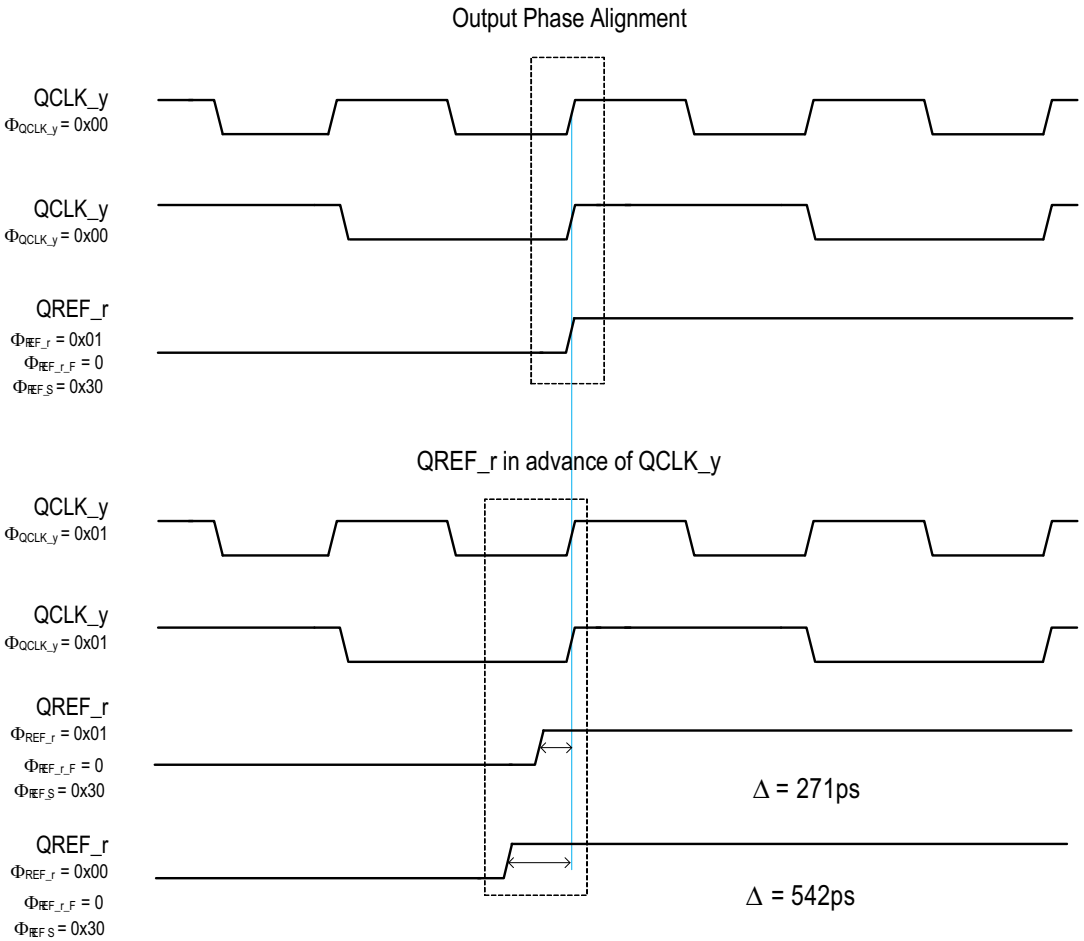


Table 22. Recommended Delay Settings for Closest Clock-SYSREF Output Phase Alignment[a]

Divider Configuration	Φ_{CLK_y}	Φ_{REF_r}	$\Phi_{REF\_r\_F}$	Φ_{REF_S}
N_{A-E} = ÷3 N_S = ÷480	0x00	0x01	0	0x00
N_A = N_B = ÷120 N_C = ÷15 N_D = ÷30 N_E = ÷3 N_S = ÷240 $_{SYNC}$ = ÷120	0x00	0x01	1	0x30

[a] QCLK and QREF outputs are aligned on the incident edge.

Deterministic Phase Relationship and Phase Alignment

Input to output delay is deterministic when the device is configured as dual PLL with the BYPV = 0, BYPF = 1 (PLL feedback path through $M_{V0} \times M_{V1}$). For more information on phase alignment, termination, and coupling techniques, see *AN-952: 8V19N480/490 Design Guide for JESD204B Output Phase Alignment and Termination*.

Status Conditions and Interrupts

The 8V19N491-36 has an interrupt output to signal changes in status conditions. The device has several conditions that can indicate faults and status changes in the operation of the device. These are shown in Table 23 and can be monitored directly in the status registers. Status bits (named ST_*condition*) are read-only and reflect the momentary device status at the time of read-access. Several status bits are also copied into latched bit positions (named LS_*condition*).

The latched version is controlled by the corresponding fault and status conditions and remains set (sticky) until reset by the user by writing 1 to the status register bit. The reset of the status condition only has an effect if the corresponding fault condition is removed, otherwise, the status bit will set again. Setting a status bit on several latched registers can be programmed to generate an interrupt signal (nINT) via settings in the Interrupt Enable bits (named IE_*condition*). A setting of 0 in any of these bits will mask the corresponding latched status bit from affecting the interrupt status pin. Setting all IE bits to 0 has the effect of disabling interrupts from the device. Interrupts are cleared by resetting the appropriate bit(s) in the latched register after the underlying fault condition has been resolved. When all valid interrupt sources have been cleared in this manner, this will release the nINT output until the next unmasked fault.

Table 23. Status Bit Functions

Status Bit		Function			
			Status if Bit is:		
Momentary	Latched	Description	1	0	Interrupt Enable Bit
ST_CLK_0	LS_CLK_0	CLK_0 input status	Active	LOS	IE_CLK_0
ST_CLK_1	LS_CLK_1	CLK_1 input status	Active	LOS	IE_CLK_1
ST_CLK_2	LS_CLK_2	CLK_2 input status	Active	LOS	IE_CLK_2
ST_CLK_3	LS_CLK_3	CLK_3 input status	Active	LOS	IE_CLK_3
nST_LOLV[a]	nLS_LOLV	VCXO-PLL loss of lock	Locked	Loss of lock	IE_LOLV
nST_LOLF[b]	nLS_LOLF	FemtoClock NG-PLL loss of lock	Locked	Loss of lock	IE_LOLF
nST_HOLD	nLS_HOLD	Holdover	Not in holdover	Device in holdover	IE_HOLD

Table 23. Status Bit Functions (Cont.)

Status Bit		Function			
			Status if Bit is:		Interrupt Enable Bit
Momentary	Latched	Description	1	0	
ST_VCOF	—	FemtoClock NG VCO calibration	Not completed	Completed	—
ST_SEL[1:0]	—	Clock input selection	00 = CLK_0 01 = CLK_1 10 = CLK_2 11 = CLK_3		—
ST_REF	LS_REF	PLL reference status	Valid reference	Reference lost[c]	IE_REF

[a] Setting the BLOCK_LOLV register bit will block the LOLV status bit from affecting the LOCK pin.

[b] If the VCXO-PLL is bypassed by setting BYPV = 1, VCXO-PLL lock status is blocked from affecting the LOCK pin.

[c] Manual and short-term holdover mode: 0 indicates if the reference selected by SEL[1:0] is lost, 1 if not lost.
Automatic with holdover mode: 0 indicates the reference is lost and while still in holdover, or no valid CLK_0 to CLK_3.
Automatic mode: 0 indicates no valid CLK_0 to CLK_3.

Table 24. LOCK Function

Status Bit (PLL)		Status Reported on LOCK Output
nST_LOLV[a] (VCXO-PLL)	nST_LOLF (FemtoClock NG)	
Locked[b]	Locked	1
	Not locked	0
Not locked	Locked	0
	Not locked	0

[a] The LOCK pin will only report the FemtoClockNG PLL status on the LOCK pin if BLOCK_LOLV = 0.

[b] If the VCXO-PLL is bypassed by setting BYPV = 1, VCXO-PLL lock status is blocked from affecting the LOCK pin.

Device Startup, Reset, and Synchronization

At startup, an internal POR (power-on reset) resets the device and sets all register bits to their default value. The device forces the VCXO control voltage at the LFV pin to half of the power supply voltage to center the VCXO-frequency. In the default configuration the QCLK_*y* and QREF_*r* outputs are disabled at startup.

Recommended Configuration Sequence

1. (Optional) Set the value of the CPOL and (optional) SDO_ACT register bits to define the SPI read mode and the SPI 3/4-wire mode. If SDO_ACT is not set, the device will be in 3-wire mode with the SDAT pin as SPI I/O.
2. Configure all PLL settings, output divider, and delay circuits as well as other device configurations:
   a. BYPF and BYPV for the desired PLL operation mode and configure the PLL dividers P_V, M_{V0}, M_{V1}, M_F, and P_F as required to achieve PLL lock (see Table 2).
   b. VCXO-PLL lock detect window by configuring the phase settings ΦM_{V0} and ΦP_V.
   c. Charge pump currents for both PLLs (CPV[4:0] and CPF[4:0]) and POLV for the desired VCXO polarity.
   d. (Optional) OSVEN and OFFSET[4:0] for the VCXO-PLL static phase offset.
   e. Channel dividers (see Table 9).
   f. MUX_*r* for the desired operation of the QREF_*r* outputs.
   g. QCLK_y, QREF_r, and QOSC output features such as desired output power-down state, style, and amplitude. QCLK_y, QREF_r and QOSC output features such as desired output power-down state, style and amplitude. Use the EN_QOSC_MOD register to make QOSC register changes effective.
   h. Desired input selection and monitoring modes: this involves nM/A[1:0] and SEL[1:0] for input selection. In any of the automatic modes, configure PRIO[1:0]_*n*, and REVS. Configure the CNTH[7:0], CNTR[1:0] counters for the desired holdover characteristics and DIV4_VAL, CNTV[1:0] for input revalidation if applicable to the operation mode.
   i. Individual Φ_{CLK_X} and Φ_{REF_r} registers and the global delay Φ_{REF_S} register for the desired phase delay between clock and SYSREF outputs (see QCLK to QREF (SYSREF) Phase Alignment).
   j. Interrupt enable configuration bits IE_*status_condition*, as desired for fault reporting on the nINT output.
3. For SYSREF operation:
   a. Configure the N_S and SYNC divider as described in Synchronizing SYSREF and Clock Output Dividers.
   b. Configure the SYSREF registers SRG, SRO, and SRPC[7:0] according to the desired SYSREF operation.
   c. Configure the SR_INSEL register bit if external SYSREF operation is desired.
4. Set the initialization bit INIT_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT_CLK bit will self-clear.
5. Set both the RELOCK bit and PB_CAL bit. This step should not be combined with the previous step (setting INIT_CLK) in a multi SPI-byte register access. Both bits will self-clear.
6. Clear the FVCV bit to release the VCXO control voltage; VCXO-PLL will attempt to lock to the input clock signal starting from its center frequency.
7. Clear the status flags.
8. At this point, the basic configuration of the registers 0x00 to 0x73 should be completed and the SPI transfer ended (set nCS to high level).
9. In a separate SPI write access, enable the outputs as desired by accessing the output-enable registers 0x74 and 0x76.
10. For SYSREF operation, see step 9 of SYSREF Frequency Divider, Delay and Starting/Re-Starting SYSREF Pulse Sequences.

Reserved registers and registers in the address range 0x78 to 0xFF should not be used. Do not write into any registers in this range.

Changing Frequency Dividers and Phase Delay Values

Clock Frequency Divider and Delay

The following procedure must be applied for a change of a clock divider and phase delay value N_{A-E}, and Φ_{CLKA-E}:

1. (Optional) Set the value of the CPOL register to define the SPI read mode. This is required so that the SPI settings can be validated by subsequent SPI read accesses.
2. (Optional) Disable the outputs whose frequency divider or delay value is changed.
3. Configure the N_{A-E} dividers and the delay circuits Φ_{CLKA-E} to the desired new values.
4. (Optional) Configure the SYNC divider if required for synchronization between clock and SYSREF signals.
5. Set the initialization bit INIT_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT_CLK bit will self-clear. During this initialization step, all QCLK_y and QREF_*r* outputs are reset to the logic low state.
6. Set the RELOCK bit. This step should not be combined with the setting INIT_CLK in a multi SPI-byte register access. The bit will self-clear.
7. (Optional) Enable the outputs whose frequency divider was changed.

SYSREF Frequency Divider, Delay and Starting/Re-Starting SYSREF Pulse Sequences

The following procedure must be applied for a change of a SYSREF divider and phase delay value N_S and Φ_{REF_S}:

1. (Optional) Set the value of the CPOL register to define the SPI read mode. This is required so that the SPI settings can be validated by subsequent SPI read accesses.
2. (Optional) Disable the outputs whose frequency divider or delay value is changed.
3. Configure any N_S divider and any delay circuits Φ_{REF_S} to their desired new values.
4. Configure the SYNC divider if required for synchronization between clock and SYSREF signals.
5. Set the initialization bit INIT_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT_CLK bit will self-clear. During this initialization step, all QCLK_y and QREF_*r* outputs are reset to the logic low state.
6. Set the RELOCK bit. This step should not be combined with the setting INIT_CLK in a multi SPI-byte register access. The bit will self-clear.
7. Set the SRO bit to counted pulse mode or to continue pulse mode, as desired.
8. (Optional) Enable the outputs whose frequency divider was changed.
9. For SYSREF operation, set the RS bit to start (or re-start) generating the configured number of SYSREF pulses.
   a. In internal SYSREF generation mode (SRG = 0), the SYSREF pulses are generated as a result of setting the RS bit. Set RS for each repeated SYSREF generation (set SR_INSEL bit to 0 for this mode).
   b. In external SYSREF mode, the SYSREF pulses are generated at the next rising edge of the EXT_SYS or CLK_3 input. Set RS before each rising edge at the EXT_SYS or CLK_3 input.

SPI Interface

The 8V19N491-36 has a configurable 3-wire/4-wire serial control port that can respond as a slave in an SPI configuration to allow read and write access to any of the internal registers for device programming or read back. The SPI interface consists of the SCLK (clock), SDAT (serial data input and output in 3-wire mode, input in 4-wire mode), SDO (serial data output in 4-wire mode) and nCS (chip select) pins. After power-up, the SPI interface is in 3-wire mode. The SDO_ACT register bit controls the SPI 3/4 wire configuration. SDO_ACT should be set after startup if 4-wire operation is required. A data transfer consists any integer multiple of 8 bits and is always initiated by the SPI master on the bus. Internal register data is organized in SPI bytes of 8 bits each.

If nCS is at logic high, the SDAT data I/O is in high-impedance state and the SPI interface of the device is disabled.

In a write operation, data on SDAT will be clocked in on the rising edge of SCLK. In a read operation, data on SDAT / SDO will be clocked out on the falling or rising edge of SCLK depending on the CPOL setting (CPOL = 0: output data changes on the falling edge, CPOL = 1: output data changes on the rising edge).

Starting a data transfer requires nCS to set and hold at logic low level during the entire transfer. Setting nCS = 0 will enable the SPI interface with SDAT in data input mode. The master must initiate the first 8-bit transfer. The first bit presented to the slave is the direction bit R/nW (1 = Read, 0 = Write) and the following 7 bits are the address bits, A[0:6], pointing to an internal register in the address space 0 to 127. Data is presented with the LSB (least significant bit) first.

Read operation from an internal register: A read operation starts with an 8-bit transfer from the master to the slave: SDAT is clocked on the *rising* edge of SCLK. The first bit is the direction bit, R/nW, which must be to 1 to indicate a read transfer, followed by 7 address bits, A[0:6]. After the first 8 bits are clocked into SDAT (in SPI 3-wire mode), the SDAT I/O changes to output. The register content addressed by A[0:6] is loaded into the shift register and the next eight SCLK *falling* (CPOL = 1) clock cycles will then present the loaded register data on the SDAT output in 3-wire mode (SDO output in 4-wire mode) and transfer these to the master. Transfers must be completed by de-asserting nCS after any multiple 8 of SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined. SPI byte (8 bit) and back-to-back read transfers of multiple registers are supported with an address auto-increment. During multiple transfers, nCS must stay at logic low level and SDAT (SDO) will present multiple registers (A), (A +1), (A +2), etc. with each 8 SCLK cycles. During SPI read operations, the user can continue to hold nCS low and provide further bytes of data for up to a total of 127 bytes in a single block read.

Write operation to a device register: During a write transfer, an SPI master transfers one or more bytes of data into the internal registers of the device. A write transfer starts by asserting nCS to low logic level. The first bit presented by the master must set the direction bit R/nW to 0 (Write) and the 7 address bits, A[0:6], must contain the 7-bit register address. Bits D0 to D7 contain 8 bits of payload data, which is written into the register addressed by A[0:6] at the end of a 8-bit write transfer. Multiple, subsequent register transfers from the master to the slave are supported by holding nCS asserted at logic low level during write transfers. The 7-bit register address will auto-increment. Transfers must be completed by de-asserting nCS after any multiple 8 of SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined.

End of transfer: After nCS is de-asserted to logic 1, the SPI bus is available to transfers to other slaves on the SPI bus. The read diagram (Figure 5) and write diagram (Figure 6) display the transfer of two bytes of data from and into registers.

Registers 0x78 to 0xFF. Registers in the address range 0x78 to 0xFF should not be used. Do not write into any registers in the 0x78 to 0xFF range.

Figure 5. Logic Diagram: Read Data (SPI 3-wire) from Registers for CPOL = 0 and CPOL = 1

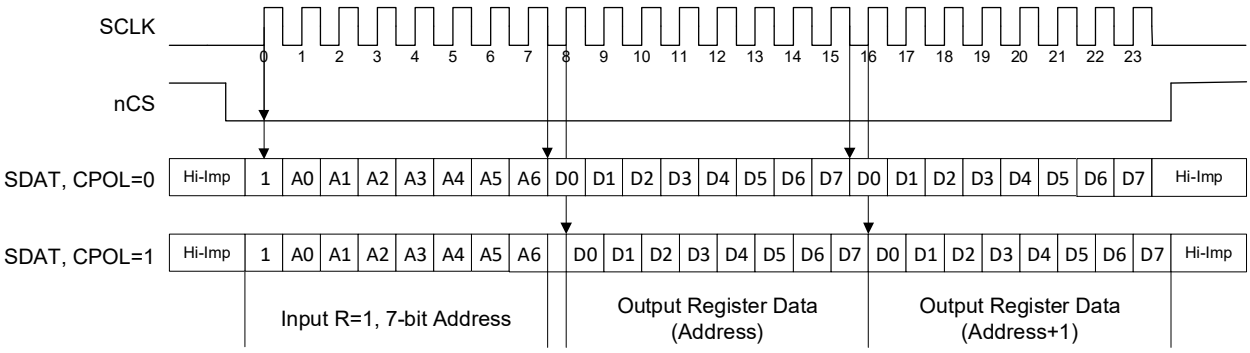


Figure 6. Logic Diagram: Write Data (SPI 3/4 wire) into Registers

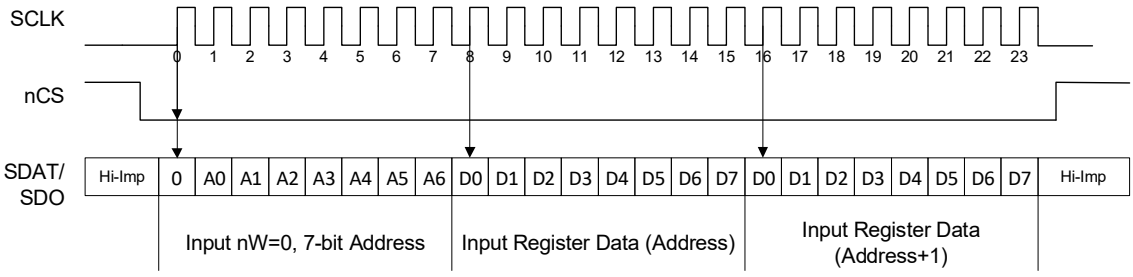


Table 25. SPI Read / Write Cycle Timing Parameters

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
f_{SCLK}	SCLK Frequency			20	MHz
t_{S1}	Setup Time, nCS (falling) to SCLK (rising)		5		ns
t_{S2}	Setup Time, SDAT (input) to SCLK (rising)		5		ns
t_{S3}	Setup Time, nCS (rising) to SCLK (rising)		5		ns
t_{H1}	Hold Time, SCLK (rising) to SDAT (input)		5		ns
t_{H2}	Hold Time, SCLK (falling) to nCS (rising)		5		ns
t_{PD1F}	Propagation Delay, SCLK (falling) to SDAT (3-wire) or to SDO (4-wire)	CPOL = 0		12	ns
t_{PD1R}	Propagation Delay, SCLK (rising) to SDAT (3-wire) or to SDO (4-wire)	CPOL = 1		12	ns
t_{PD2}	Propagation Delay, nCS to SDAT (disable)			12	ns

Figure 7. SPI Timing Diagram

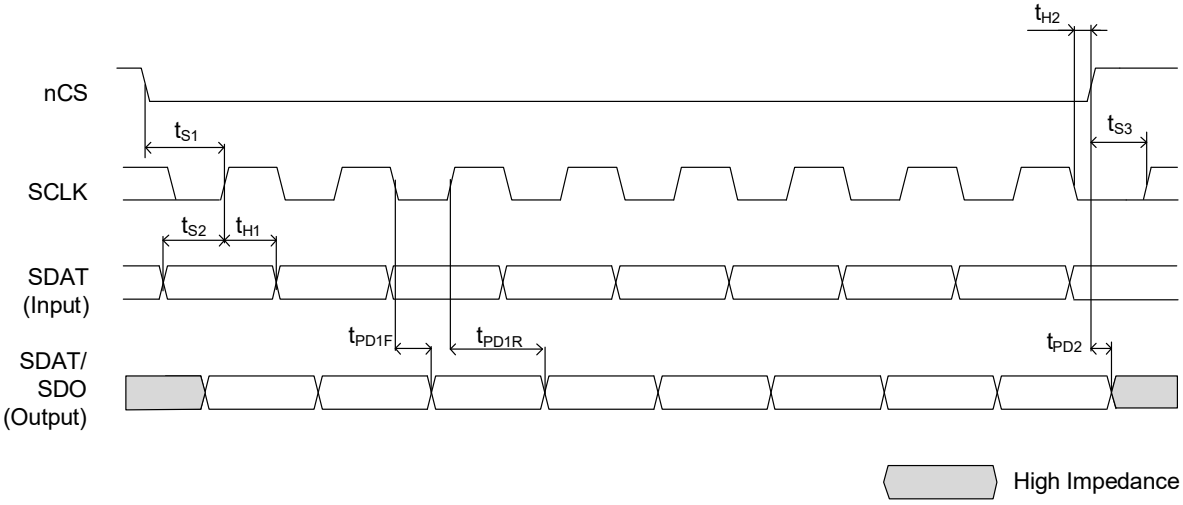


Table 26. Serial Interface Logic Voltage (SPI)[a]

SELSV0	SPI Interface (SDAT, SDO, SCLK, nCS) Logic Voltage
0 (default)	1.8V
1	3.3V

[a] SELV0 is in register 0x1F, bit D4

Table 27. Serial Interface Logic Voltage (Status Outputs)[a]

SELSV1	Status Output (nINT, LOCK) Logic Voltage
0 (default)	1.8V
1	3.3V

[a] SELV1 is in register 0x1F, bit D5

Configuration Registers

This section contains all addressable registers, sorted for function, followed for a detailed description of each bit field for each register. Several functional blocks with multiple instances in this device have individual registers controlling their settings, but since the registers have an identical format and bit meaning, they are described only once, with an additional table to indicate their addresses and default values. All writable register fields will come up with default values as indicated in the Defaults column.

Fixed read-only bits will have defaults as indicated in their specific register descriptions. Read-only status bits will reflect valid status of the conditions they are designed to monitor once the internal power-up reset has been released. Unused registers and bit positions are reserved. Reserved bit fields can be used for internal debug test and debug functions.

Table 28. Configuration Registers

Register Address	Register Description
0x00–0x01	PLL Frequency Divider: ΦMV, MV0
0x02–0x03	PLL Frequency Divider: MV1, BYPF
0x04–0x05	VCXO-PLL Control: ΦPV, PV
0x06–0x07	Reserved
0x08–0x09	PLL Frequency Divider: MF
0x0A	VCXO-PLL Control: BYPV
0x0B	Reserved
0x0C	PLL Frequency Divider: SRC, PF, FDF
0x0D–0x0F	Reserved
0x10–0x12	VCXO-PLL Control; Output state QOSC
0x13	Reserved
0x14	Input Selection Mode: Priority
0x15	Input Selection Mode: Switching
0x16	Input Selection Mode: CNTH
0x17	Input Selection Mode: CNTR, CNTV
0x18	SYSREF Control: Divider
0x19	SYSREF Control: SYNC, PD
0x1A	SYSREF Control: SRPC
0x1B	SYSREF Control: ΦREF_S
0x1C	SYSREF Control: SRG, SRO, SR_INSEL, EN_QCLK_MOD
0x1D–0x1E	Reserved
0x1F	PLL Control, SPI control, SPI/Status output control, EN_QCLKV_MOD
0x20–0x22	Channel A
0x23	Reserved
0x24	Output State QCLK_*A0*
0x25	Output State QCLK_*A1*
0x26	Output State QCLK_*A2*
0x27	Reserved

Table 28. Configuration Registers (Cont.)

Register Address	Register Description
0x28	QREF_A0 Delay, MUX
0x29	QREF_A1 Delay, MUX
0x2A	QREF_A2 Delay, MUX
0x2B	Reserved
0x2C	Output State QREF_*A0*
0x2D	Output State QREF_*A1*
0x2E	Output State QREF_*A2*
0x2F	Reserved
0x30–0x32	Channel B
0x33	Reserved
0x34	Output State QCLK_*B0*
0x35	Output State QCLK_*B1*
0x36–0x37	Reserved
0x38	QREF_B0 Delay, MUX
0x39	QREF_B1 Delay, MUX
0x3A–0x3B	Reserved
0x3C	Output State QREF_*B0*
0x3D	Output State QREF_*B1*
0x3E–0x3F	Reserved
0x40–0x42	Channel C
0x43	Reserved
0x44	Output State QCLK_*C0*
0x45	Output State QCLK_*C1*
0x46–0x47	Reserved
0x48	QREF_C0 Delay, MUX
0x49	QREF_C1 Delay, MUX
0x4A–0x4B	Reserved
0x4C	Output State QREF_*C0*
0x4D	Output State QREF_*C1*
0x4E–0x4F	Reserved
0x50–0x52	Channel D
0x53	Reserved
0x54	Output State QCLK_*D*
0x55–0x57	Reserved
0x58	QREF_D Delay, MUX
0x59–0x5B	Reserved

Table 28. Configuration Registers (Cont.)

Register Address	Register Description
0x5C	Output State QREF_*D*
0x5D–0x5F	Reserved
0x60–0x62	Channel E
0x63	Reserved
0x64	Output State QCLK_*E0*
0x65	Output State QCLK_*E1*
0x66–0x67	Reserved
0x68–0x69	Interrupt Enable
0x6A–0x6B	Reserved
0x6C	Status (Latched)
0x6D	Status (Momentary)
0x6E	Status (Latched)
0x6F	Status (Momentary)
0x70	SYSREF control: RS
0x71–0x73	General Control
0x74–0x75	Output Enable QCLK
0x76	Output Enable QREF
0x77	Reserved
0x78–0x7A	Reserved
0x7B	Reserved
0x7C–0x7F	Reserved
0x80–0xFF	Reserved

Channel and Clock Output Registers

The content of the channel register and clock output registers set the channel state, the clock divider, the QCLK output state, and clock phase delay.

Table 29. Channel and Clock Output Register Bit Field Locations

Bit Field Location								
Register Address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x20: Channel A 0x30: Channel B 0x40: Channel C 0x50: Channel D 0x60: Channel E	Reserved	Reserved	N_*A*[5:0] N_*B*[5:0] N_*C*[5:0] N_*D*[5:0] N_*E*[5:0]					
0x21: Channel A 0x31: Channel B 0x41: Channel C 0x51: Channel D 0x61: Channel E	ΦCLK_*A*[7:0] ΦCLK_*B*[7:0] ΦCLK_*C*[7:0] ΦCLK_*D*[7:0] ΦCLK_*E*[7:0]							
0x22: Channel A 0x32: Channel B 0x42: Channel C 0x52: Channel D 0x62: Channel E	PD_*A* PD_*B* PD_*C* PD_*D* PD_*E*	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x24: QCLK_A0 0x25: QCLK_A1 0x26: QCLK_A2	PD_*A0* PD_*A1* PD_*A2*	Reserved	Reserved	STYLE_*A0* STYLE_*A1* STYLE_*A2*	A_*A0*[1:0] A_*A1*[1:0] A_*A2*[1:0]		Reserved	
0x34: QCLK_B0 0x35: QCLK_B1	PD_*B0* PD_*B1*	Reserved	Reserved	STYLE_*B0* STYLE_*B1*	A_*B0*[1:0] A_*B1*[1:0]		Reserved	
0x44: QCLK_C0 0x45: QCLK_C1	PD_*C0* PD_*C1*	Reserved	Reserved	STYLE_*C0* STYLE_*C1*	A_*C0*[1:0] A_*C1*[1:0]		Reserved	
0x54: QCLK_D	PD_*D*	Reserved	Reserved	STYLE_*D*	A_*D*[1:0]		Reserved	
0x64: QCLK_E0 0x65: QCLK_E1	PD_*E0* PD_*E1*	Reserved	Reserved	STYLE_*E0* STYLE_*E1*	A_*E0*[1:0] A_*E1*[1:0]		Reserved	
0x74	EN_QCLK_A0	EN_QCLK_A1	EN_QCLK_A2	EN_QCLK_B0	EN_QCLK_B1	EN_QCLK_C0	EN_QCLK_C1	EN_QCLK_D
0x75	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EN_QCLK_E1	EN_QCLK_E0

Table 30. Channel and Clock Output Register Descriptions[a]

<table>
<tr><th colspan="6">Bit Field Location</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th colspan="3">Description</th></tr>
<tr><td rowspan="8">N_x[5:0]</td><td rowspan="8">R/W</td><td rowspan="8">01 0001

Value = ÷30</td><td colspan="3">Output Frequency Divider N
N_x[5:0]Divider Value</td></tr>
<tr><td>00 0001
00 0010
00 0011
00 0100
00 0101
00 0110
00 0111
00 1000</td><td>÷1
÷2
÷3
÷4
÷5
÷6
÷8
÷9</td><td>00 1001
00 1010
00 1011
00 1100
00 1101
00 1110
00 1111
01 0000</td><td>÷10
÷12
÷15
÷16
÷18
÷20
÷24
÷25</td></tr>
<tr><td>01 0001
01 0010
01 0011</td><td>÷30
÷32
÷36</td><td>01 0100
01 0101</td><td>÷40
÷48</td></tr>
<tr><td>01 0110</td><td>÷50</td><td>01 1000
01 1001</td><td>÷60
÷64</td></tr>
<tr><td>01 1010</td><td>÷72</td><td>01 1011</td><td>÷80</td></tr>
<tr><td>01 1101</td><td>÷96</td><td>01 1110
01 1111</td><td>÷100
÷120</td></tr>
<tr><td>10 0000
10 0001</td><td>÷128
÷150</td><td>10 0010
10 0011</td><td>÷160
÷200</td></tr>
<tr><td>PD_x</td><td>R/W</td><td>0</td><td colspan="3">0 = Channel x is powered up
1 = Channel x is powered down</td></tr>
<tr><td>PD_y</td><td>R/W</td><td>0</td><td colspan="3">0 = Output QCLK_y is powered up
1 = Output QCLK_y is powered down</td></tr>
<tr><td rowspan="2">ΦCLK_x[7:0]</td><td rowspan="2">R/W</td><td rowspan="2">0000 0000</td><td colspan="3">CLK_x phase delay
ΦCLK_x[7:0]</td></tr>
<tr><td colspan="3">Delay in ps = ΦCLK_x × 271ps (256 steps)
0000 0000 = 0ps
…
1111 1111 = 69.173ns</td></tr>
<tr><td rowspan="3">A_y[1:0]</td><td rowspan="3">R/W</td><td rowspan="3">00</td><td colspan="3">QCLK_y Output amplitude</td></tr>
<tr><td colspan="2">Setting for STYLE = 0 (LVDS)</td><td>Setting for STYLE = 1 (LVPECL)</td></tr>
<tr><td colspan="2">A[1:0] = 00: 250mV
A[1:0] = 01: 500mV
A[1:0] = 10: 750mV
A[1:0] = 11:1000mV
Termination: 100Ω across</td><td>A[1:0] = 00: 250mV
A[1:0] = 01: 500mV
A[1:0] = 10: 750mV
A[1:0] = 11:1000mV
Termination: 50Ω to VT</td></tr>
</table>

Table 30. Channel and Clock Output Register Descriptions[a]

Bit Field Location			
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**
STYLE_*y*	R/W	0	QCLK_*y* Output format 0 = Output is LVDS (Requires 100Ω output termination) 1 = Output is LVPECL (Requires 50Ω output termination of the specified recommended termination voltage)
EN_*y*	R/W	0	QCLK_*y* Output enable 0 = QCLK_*y* Output is disabled at the logic low state 1 = QCLK_*y* Output is enabled

[a] *x* = A, B, C, D, E; *y* = A0, A1, A2, B0, B1, C0, C1, D, E0, E1.

QREF Output State Registers

The content of the output registers set the output frequency and divider, several output states, the power state, the output style, and amplitude.

Table 31. QREF Output State Register Bit Field Locations

Bit Field Location								
Register Address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x28: QREF_A0 0x29: QREF_A1 0x2A:QREF_A2	Reserved	ΦREF_F[1:0]_*A0* ΦREF_F[1:0]_*A1* ΦREF_F[1:0]_*A2*		MUX_*A0* MUX_*A1* MUX_*A2*	ΦREF_*A0*[2:0] ΦREF_*A1*[2:0] ΦREF_*A2*[2:0]			ΦREF_F[2]_*A0* ΦREF_F[2]_*A1* ΦREF_F[2]_*A2*
0x38: QREF_B0 0x39: QREF_B1	Reserved	ΦREF_F[1:0]_*B0* ΦREF_F[1:0]_*B1*		MUX_*B0* MUX_*B1*	ΦREF_*B0*[2:0] ΦREF_*B1*[2:0]			ΦREF_F[2]_*B0* ΦREF_F[2]_*B1*
0x48: QREF_C0 0x49: QREF_C1	Reserved	ΦREF_F[1:0]_*C0* ΦREF_F[1:0]_*C1*		MUX_*C0* MUX_*C1*	ΦREF_*C0*[2:0] ΦREF_*C1*[2:0]			ΦREF_F[2]_*C0* ΦREF_F[2]_*C1*
0x58: QREF_D	Reserved	ΦREF_F[1:0]_*D*		MUX_*D*	ΦREF_*D*[2:0]			ΦREF_F[2]_*D*
0x2C: QREF_A0 0x2D: QREF_A1 0x2E: QREF_A2	PD_*A0* PD_*A1* PD_*A2*	Reserved	nBIAS_*A0* nBIAS_*A1* nBIAS_*A2*	STYLE_*A0* STYLE_*A1* STYLE_*A2*	A_*A0*[1:0] A_*A1*[1:0] A_*A2*[1:0]		Reserved	
0x3C: QREF_B0 0x3D: QREF_B1	PD_*B0* PD_*B1*	Reserved	nBIAS_*B0* nBIAS_*B1*	STYLE_*B0* STYLE_*B1*	A_*B0*[1:0] A_*B1*[1:0]		Reserved	
0x4C: QREF_C0 0x4D: QREF_C1	PD_*C0* PD_*C1*	Reserved	nBIAS_*C0* nBIAS_*C1*	STYLE_*C0* STYLE_*C1*	A_*C0*[1:0] A_*C1*[1:0]		Reserved	

Table 31. QREF Output State Register Bit Field Locations

Bit Field Location								
Register Address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x5C: QREF_D	PD_*D*	Reserved	nBIAS_*D*	STYLE_*D*	A_*D*[1:0]		Reserved	
0x76	EN_QREF_A0	EN_QREF_A1	EN_QREF_A2	EN_QREF_B0	EN_QREF_B1	EN_QREF_C0	EN_QREF_C1	EN_QREF_D

Table 32. QREF Output State Register Descriptions[a]

Bit Field Location			
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**
MUX_*r*	R/W	1	0 = QREF_*r* output signal source is the channel's clock signal 1 = QREF_*r* output signal source is the internally generated SYSREF signal
ΦREF_*r*[2:0]	R/W	000	SYSREF coarse phase delay ΦREF_*r*[2:0]
			Delay in ps = ΦREF_*r*[2:0] × 271ps (8 steps) 000 = 0ps … 111 = 1.899 ns
ΦREF_F[2:0]_*r*	R/W	000	SYSREF fine phase delay ΦREF_F[2:0]_*r*
			Insert a SYSREF fine phase delay in ps (8 steps) in addition to the delay value in ΦREF_*r*[2:0]. 000 = 0ps 001 = 25ps 010 = 50ps 011 = 75ps 100 = 85ps 101 = 110ps 110 = 135ps 111 = 160ps
nBIAS_*r*	R/W	0	QREF_*r* Output Bias Voltage 0 = Output is not voltage biased. 1 = Output is biased to the LVDS cross-point voltage if BIAS_TYPE (register 0x19, bit 7) is set to 1. Bit has no effect if BIAS_TYPE = 0. Output bias = 1 requires AC coupling and LVDS style on the corresponding output.

Table 32. QREF Output State Register Descriptions[a]

Bit Field Location				
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**	
A_*r*[1:0]	R/W	00	QREF_*r* Output amplitude	
			Setting for STYLE_*r* = 0 (LVDS)	Setting for STYLE_*r* = 1 (LVPECL)
			A[1:0] = 00: 250mV A[1:0] = 01: 500mV A[1:0] = 10: 750mV A[1:0] = 11:1000mV Termination: 100Ω across	A[1:0] = 00: 250mV A[1:0] = 01: 500mV A[1:0] = 10: 750mV A[1:0] = 11:1000mV Termination: 50Ω to VT
PD_*r*	R/W	0	QREF_*r* Output Power Down 0 = Output is powered up 1 = Output is powered down. STYLE, EN, and A[1:0] settings have no effect.	
STYLE_*r*	R/W	0	QREF_*r* Output format 0 = Output is LVDS (requires 100Ω output termination) 1 = Output is LVPECL (requires 50Ω output termination to the specified recommended termination voltage)	
EN_*r*	R/W	0	QREF_*r* Output enable 0 = Output is disabled at the logic low state 1 = Output is enabled	

[a] r = A0, A1, A2, B0, B1, C0, C1, and D

PLL Frequency Divider Registers

Table 33. PLL Frequency Divider Register Bit Field Locations

Bit Field Location								
Register Address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x00	ΦMV0[2:0]			PD_MV1	MV0[11:8]			
0x01	MV0[7:0]							
0x02	MV1[7:0]							
0x03	MV1[8]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BYPF
0x04	ΦPV[2:0]			Reserved	PV[11:8]			
0x05	PV[7:0]							
0x08	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MF[8]
0x09	MF[7:0]							
0x0C	FDF	SRC	PF[5:0]					
0x1F	BLOCK_LOLV	SDO_ACT	SELSV1	SELSV0	EN_QOSC_MOD[3:0]			

Table 34. PLL Frequency Divider Register Descriptions

Bit Field Location				
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**	
ΦMV0[2:0]	R/W	101	Phase of the M_{V0} feedback divider. Determines the PLL lock-detect phase window in conjunction with ΦPV[2:0]. Sampling clock phase is relative to the VCXO-PLL phase detector clock edge. Set ΦMV0[2:0] in relationship to M_{V0}:	
			M_{V0} Divider Value	ΦMV0[2:0] Setting
			1–31	
			32–63	010
			64–127	011
			128–255	100
			256–511	101
			512–1023	110
			1024+	111

Table 34. PLL Frequency Divider Register Descriptions (Cont.)

Bit Field Location			
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**
MV0[11:0]	R/W	1100 0000 0000 Value = ÷3072	VCXO-PLL Feedback-Divider The value of the frequency divider (binary coding). Range: ÷1 to ÷4095
MV1[8:0]	R/W	0 0001 1110 Value = ÷30	PLL Feedback-Divider. The value of the frequency divider (binary coding). Range: ÷4 to ÷511
PD_MV1	R/W	0 Value = MV1 enabled	PLL Feedback-Divider MV1 Power Down/Disabled. 0 = MV1 Divider is enabled 1 = MV1 Divider is powered down and disabled Disable MV1 to save power consumption in configurations that do not use the input clock monitors.
ΦPV[2:0]	R/W	101	Phase of the P_V input (reference) divider. Determines the PLL lock-detect phase window in conjunction with ΦMV0[2:0]. Sampling clock phase is relative to the VCXO-PLL phase detector clock edge. Set ΦPV[2:0] in relationship to P_V: P_V Divider Value — ΦPV[2:0] Setting 1–31 — 010 32–63 — 011 64–127 — 100 128–255 — 101 256–511 — 110 512–1023 — 111 1024+
PV[11:0]	R/W	1100 0000 0000 Value = ÷3072	VCXO-PLL Input Frequency Pre-Divider The value of the frequency divider (binary coding). Range: ÷1 to ÷4095
MF[8:0]	R/W	0 0001 1110 Value = ÷30	FemtoClock NG Pre-Divider The value of the frequency divider (binary coding). Range: ÷8 to ÷511
PF[5:0]	R/W	00 0000 Value = Bypass	FemtoClock NG Pre-Divider The value of the frequency divider (binary coding). Range: ÷1 to ÷63 00 0000: PF is bypassed

Table 34. PLL Frequency Divider Register Descriptions (Cont.)

Bit Field Location			
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**
FDF	R/W	0 Value = f_{VCXO} ÷ PF	Frequency Doubler The input frequency of the FemtoClock NG PLL (2nd stage) is: 0 = The output signal of the BYPV multiplexer, divided by the PF divider 1 = The output signal of the BYPV multiplexer, doubled in frequency. Use this setting to improve phase noise. The PF divider has no effect if FDF = 1.
SRC	R/W	0 PLL enabled	Output Divider Source Signal (FemtoClock NG PLL Bypass) 0 = FemtoClock NG PLL is enabled and feeds the output channel dividers. 1 = FemtoClock NG PLL is disabled and bypassed. The VCXO-PLL output signal is frequency divided by the channel dividers.
BLOCK_LOLV	R/W	0 Not blocked	Blocks the LOLV status condition from reporting to the LOCK pin. 0 = The LOLV (VCXO-PLL lock) condition is reported to the LOCK pin. 1 = The LOLV (VCXO-PLL lock) condition does not affect the LOCK pin.
SDO_ACT	R/W	0 Value: 3-wire SPI	SPI interface select 0 = 3-wire. SDAT is SPI input and output. SDO is in high-impedance state 1 = 4-wire. SDAT is SPI input, SDO pin is the SPI output
SELSV0	R/W	0 Value: 1.8V	SPI (SDO, SDAT, nCS, SCLK) Logic Voltage Select 0 = 1.8V 1 = 3.3V
SELSV1	R/W	0 Value: 1.8V	Status output (nINT, LOCK) Logic Voltage Select 0 = 1.8V 1 = 3.3V

VCXO-PLL Control Registers

Table 35. VCXO-PLL Control Register Bit Field Locations

Bit Field Location								
Register Address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x03	MV1[8]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BYPF
0x0A	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BYPV
0x10	POLV	FVCV	Reserved	CPV[4:0]				
0x11	nPD_QOSC	STYLE_QOSC	OSVEN	OFFSET[4:0]				
0x12	Reserved	A_QOSC[1:0]		CPF[4:0]				

Table 36. VCXO-PLL Control Register Descriptions

Bit Field Location			
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**
BYPF	R/W	0	PLL feedback Bypass 0 = VCXO-PLL feedback divider: M_{V0} 1 = VCXO-PLL feedback divider: $M_{V0} \times M_{V1}$
BYPV	R/W	0	VCXO-PLL Bypass 0 = VCXO-PLL is enabled. 1 = VCXO-PLL is disabled and bypassed.
POLV	R/W	0	VCXO Polarity 0 = Positive polarity. Use for an external VCXO with a positive f(V_C) characteristics. 1 = Negative polarity. Use for an external VCXO with a negative f(V_C) characteristics.
FVCV	R/W	1	VCXO-PLL Force VC control voltage 0 = Normal operation. 1 = Forces the voltage at the LFV control pin (VCXO input) to V_{DD_V} / 2. VCXO-PLL unlocks and the VCXO is forced to its mid-point frequency. FVCV = 1 is the default setting at startup to center the VCXO frequency. FVCV should be cleared after startup to enable the PLL to lock to the reference frequency.
CPV[4:0]	R/W	1 1000 Value: 1.25mA	VCXO-PLL Charge-Pump Current Controls the charge pump current I_{CPV} of the VCXO-PLL. Charge pump current is the binary value of this register plus one multiplied by 50µA. I_{CPV} = 50µA × (CPV[4:0] + 1). CPV[4:0] = 00000 sets ICPV to the min. current of 50µA. Max. charge pump current is 1.6mA. Default setting is 1.25mA: ((24 + 1) × 50µA).

Table 36. VCXO-PLL Control Register Descriptions (Cont.)

Bit Field Location				
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**	
nPD_QOSC	R/W	0	QOSC Power State 0 = Output QOSC is powered down 1 = Output QOSC is powered up	
STYLE_QOSC	R/W	0	QOSC Output format 0 = Output is LVDS (requires 100Ω output termination) 1 = Output is LVPECL (requires 50Ω output termination to the specified recommended termination voltage)	
OSVEN	R/W	0	VCXO-PLL Offset Enable 0 = No offset 1 = Offset enabled. A static phase offset of OFFSET[4:0] is applied to the PFD of the VCXO-PLL	
OFFSET[4:0]	R/W	0 0000 Value: 0°	VCXO-PLL Static Phase Offset Controls the static phase detector offset of the VCXO-PLL. Phase offset is the binary value of this register multiplied by 0.9° of the PFD input signal (OFFSET [4:0] × f_{PFD} ÷ 400). Maximum offset is 31 × 0.9° = 27.9°. Setting OFFSET to 0.0° eliminates the thermal noise of an offset current. If the VCXO-PLL input jitter period T_{JIT} exceeds the average input period: set OFFSET to a value larger than f_{PFD} × T_{JIT} × 400 to achieve a better charge pump linearity and lower in-band noise of the PLL.	
CPF[4:0]	R/W	1 1000 Value: 10mA	FemtoClock NG-PLL Charge-Pump Current Controls the charge pump current I_{CPF} of the FemtoClock NG PLL. Charge pump current is the binary value of this register plus one multiplied by 400µA. I_{CPF} = 400µA × (CPF[4:0] + 1). CPV[4:0] = 00000 sets I_{CPF} to the min. current of 400µA. Maximum charge pump current is 12.8mA. Default setting is 10.0mA: ((24+1) × 400µA).	
A_QOSC[1:0]	R/W	00 Value: 10mV	QOSC Output amplitude	
			Setting for STYLE_*r* = 0 (LVDS)	Setting for STYLE_*r* = 1 (LVPECL)
			A[1:0] = 00: 250mV A[1:0] = 01: 500mV A[1:0] = 10: 500mV A[1:0] = 11: 750mV Termination: 100Ω across	A[1:0] = 00: 250mV A[1:0] = 01: 500mV A[1:0] = 10: 500mV A[1:0] = 11: 750mV Termination: 50Ω to VT

Input Selection Mode Registers

Table 37. Input Selection Mode Register Bit Field Locations

Bit Field Location								
Register Address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x14	PRIO_0[1:0]		PRIO_1[1:0]		PRIO_2[1:0]		PRIO_3[1:0]	
0x15	Reserved	BLOCK_LOR	DIV4_VAL	REVS	nM/A[1:0]		SEL[1:0]	
0x16	CNTH[7:0]							
0x17	CNTR[1:0]		PD_CLK3	PD_CLK2	PD_CLK1	PD_CLK0	CNTV[1:0]	

Table 38. Input Selection Mode Register Descriptions

Bit Field Location			
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**
PRIO_*n*[1:0]	R/W	CLK_0: 11 CLK_1: 10 CLK_2: 01 CLK_3: 00	Controls the auto-selection priority of the clock input CLK_*n* (*n* = 0…3). If multiple inputs have equal priority, the order within that priority is from CLK_0 (highest) to CLK_3 (lowest). 00 = Priority 0 (lowest) 01 = Priority 1 10 = Priority 2 11 = Priority 3 (highest)
DIV4_VAL	R/W	0 Value: ÷1	Pre-divider for CNTV[1:0]. Use the ÷4 pre-divider for input frequencies > 250MHz. 0 = ÷1 1 = ÷4
REVS	R/W	0 (Value: off)	Revertive Switching. The revertive input switching setting is only applicable to the two automatic selection modes shown in Table 11. If nM/A[1:0] = X0, the REVS setting has no impact. 0 = Disabled: Re-validation of a non-selected input clock has no impact on the clock selection. 1 = Enabled: Re-validation of any non-selected input clock(s) will cause a new input selection according to the pre-set input priorities (revertive switch). An input switch is only done if the re-validated input has a higher priority than the current VCXO-PLL reference clock. Default setting is revertive switching turned off.

Table 38. Input Selection Mode Register Descriptions (Cont.)

Bit Field Location			
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**
nM/A[1:0]	R/W	00 Value: Manual Selection	Reference Input Selection Mode. In any of the manual selection modes (either nM/A[1:0] = 00 or 10), the VCXO-PLL reference input is selected by SEL[1:0]. In any of the automatic selection modes, the VCXO-PLL reference input is selected by an internal state machine according to the input LOS states and the priorities in the input priority registers 00 = Manual selection 01 = Automatic selection (no holdover) 10 = Short-term holdover 11 = Automatic selection with holdover
SEL[1:0]	R/W	00 Value: CLK_0 selected	VCXO-PLL Input Reference Selection Controls the selection of the VCXO-PLL reference input in the manual selection modes. In automatic selection modes (nM/A[1:0] = X1), SEL[1:0] has no meaning. 00 = CLK_0 01 = CLK_1 10 = CLK_2 11 = CLK_3
CNTH[7:0]	R/W	1000 0000 (value: 136ms)	nMA[1:0] = 11 Hold-off counter period for automatic with holdover mode. The device initiates a clock fail-over switch upon counter expiration (zero transition). The counters start to count backward after an LOS event is detected. The hold-off counter period is determined by the binary number of VCXO-PLL output pulses divided by CNTR[1:0]. With a VCXO frequency of 122.88MHz and CNTR[1:0] = 10, the counter has a period of (1.066ms × binary setting). After each zero-transition, the counter automatically re-loads to the setting in this register. The default setting is 136ms (VCXO = 122.88MHz: 1/122.88MHz × 2^{17} × 128)
CNTR[1:0]	R/W	10 (Value: 2^{17})	nMA[1:0] = 11 Automatic with holdover: Reference divider CNTR[1:0] / CNTH frequency (period; range): 122.88MHz VCXO / 38.4MHz VCXO 00 = $f_{VCXO} \div 2^{15}$ / 1171Hz (0.853ms; 0–217.6ms) 01 = $f_{VCXO} \div 2^{16}$ / 1875Hz (0.533ms; 0–136ms) 10 = $f_{VCXO} \div 2^{17}$ / 937.5Hz (1.066ms; 0–272ms)
CNTV[1:0]	R/W	10 (Value: 32)	Controls the number of required consecutive, valid input reference pulses for clock re-validation on CLK_*n* (n = 0…3), in number of input periods. At an LOS event, the re-validation counter loads this setting from the register and counts down by one with every valid, consecutive input signal period. Missing input edges (for one input period) will cause this counter to re-load its setting. An input is re-validated when the counter transitions to zero and the corresponding LOS flag is reset. DIV4_VAL = 0: 00 = 2 (shortest possible); 01 = 16; 10 = 32; 11 = 64 DIV4_VAL = 1: 00 = 8 (shortest possible); 01 = 64; 10 = 128; 11 = 256

Table 38. Input Selection Mode Register Descriptions (Cont.)

Bit Field Location			
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**
PD_CLK_*3* PD_CLK_*2* PD_CLK_*1* PD_CLK_*0*	R/W	0 Powered up/Enabled	Input CLK_*n* Power Down/Disable. 0 = Input CLK_*n* is enabled 1 = Input CLK_*n* is powered down and disabled Disable individual Input CLK_*n* input to save power consumption in configurations not using the respective input and in manual switching or short-term holdover mode. Enable inputs CLK_*n* in configurations with automatic switching.
BLOCK_LOR	R/W	0 Value: Not blocked	Block loss-of-reference (input activity) indicator VCXO-PLL loss of lock signals nST_LOLV and nLS_LOLV are triggered by: 0 = VCXO-PLL loss of lock or by inactivity of the selected reference clock 1 = Only VCXO-PLL loss of lock. BLOCK_LOR = 1 will also block loss-of-reference from triggering a failure on the LOCK output pin.

SYSREF Control Registers

Table 39. SYSREF Control Register Bit Field Locations

Bit Field Location								
Register Address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x18	NS[7:0]							
0x19	PD_S	BIAS_TYPE	SYNC[5:0]					
0x1A	SRPC[7:0]							
0x1B	ΦREF_*S*[7:0]							
0x1C	EN_QOSC_MOD[7:4]				Reserved	SR_INSEL	SRG	SRO
0x1F	BLOCK_LOLV	SDO_ACT	SELSV1	SELSV0	EN_QOSC_MOD[3:0]			
0x70	RS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 40. SYSREF Control Register Descriptions

<table>
<tr><th colspan="6">Bit Field Location</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th colspan="3">Description</th></tr>
<tr><td>PD_S</td><td>R/W</td><td>0</td><td colspan="3">SYSREF global power down (incl. global delay ΦS, SYSREF frequency divider NS)
0 = SYSREF functional blocks are powered up.
1 = SYSREF functional blocks are powered down.</td></tr>
<tr><td rowspan="3">NS[7:0]</td><td rowspan="3">R/W</td><td rowspan="3">00 00 00 00
Value = ÷64</td><td colspan="3">SYSREF Frequency Divider.
The value of the frequency divider is set by the product of 2 × NS[7] × NS[6] × NS[5:4] × NS[3] × NS[2] × NS[1:0]</td></tr>
<tr><td>NS[7:6]
00 =÷2
01 =÷4
10 =÷8
11 =÷16</td><td>NS[5:4]
00 =÷2
01 =÷3
10 =÷4
11 =÷5</td><td>NS[3]
0 =÷2
1 =÷4</td><td>NS[2]
0 =÷2
1 =÷4</td><td>NS[1:0]
00 =÷2
01 =÷3
10 =÷4
11 =÷5</td></tr>
<tr><td colspan="3">The SYSREF contains five serial dividers that can be individually controlled by NS[6], NS[5:4], NS[3], NS[2] and NS[1:0], respectively; and an additional divide-by-two. Example: to achieve a SYSREF divider value of ÷3840 = 2 × {16} × {3} × {4} × {2} × {5}: set NS[7:6] = 11, NS[5:4] = 01, NS[3] = 1, NS[2] = 0, and NS[1:0] = 11.
If a given output divider can be achieved by multiple NS[7:0] settings, use the highest possible divider in NS[7:6], then in NS[5:4], followed by NS[3], NS[2], and NS[1:0].</td></tr>
<tr><td>BIAS_TYPE</td><td>R/W</td><td>1</td><td colspan="3">SYSREF output voltage bias
0 = QREF_r outputs are in a low/high state when nBIAS_r is set to 1 or during a SYSREF event
1 = QREF_r outputs are in a cross-point biased state when nBIAS_r is set to 1 or during a SYSREF event.</td></tr>
</table>

Table 40. SYSREF Control Register Descriptions (Cont.)

<table>
<tr><th colspan="5">Bit Field Location</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th colspan="2">Description</th></tr>
<tr><td rowspan="8">SYNC[5:0]</td><td rowspan="8">R/W</td><td rowspan="8">010001
Value = ÷30</td><td colspan="2">SYSREF Synchronizer divider value. The SYNC[5:0] divider controls the release of SYSREF pulses at coincident QCLK_y clock edges. For SYSREF operation, set the SYNC divider value to half of the least common multiple of the clock divider values Nx (x = A to E). For example, if NA = NB = ÷2, NC = ND = ÷3, NE = ÷4, set the SYNC divider to ÷6.
SYNC Frequency Divider N
SYNC[5:0] Divider Value SYNC[5:0] Divider Value</td></tr>
<tr><td>00 0000
00 0001
00 0010
00 0011
00 0100
00 0101
00 0110
00 0111
00 1000</td><td>Do not use
Do not use
÷2
÷3
÷4
÷5
÷6
÷8
÷9</td><td>00 1001
00 1010
00 1011
00 1100
00 1101
00 1110
00 1111
01 0000</td><td>÷10
÷12
÷15
÷16
÷18
÷20
÷24
÷25</td></tr>
<tr><td>01 0001
01 0010
01 0011</td><td>÷30
÷32
÷36</td><td>01 0100
01 0101</td><td>÷40
÷48</td></tr>
<tr><td>01 0110</td><td>÷50</td><td>01 1000
01 1001</td><td>÷60
÷64</td></tr>
<tr><td>01 1010</td><td>÷72</td><td>01 1011</td><td>÷80</td></tr>
<tr><td>01 1101</td><td>÷96</td><td>01 1110
01 1111</td><td>÷100
÷120</td></tr>
<tr><td>10 0000
10 0001</td><td>÷128
÷150</td><td>10 0010
10 0011</td><td>÷160
÷200</td></tr>
<tr><td>SRPC[7:0]</td><td>R/W</td><td>0000 0010
(value: 2)</td><td colspan="2">SYSREF pulse count
Binary value of the SYSREF pulses generated and output at all enabled QREF outputs. Allows to generate 1 to 255 pulses after each write access. Requires setting SRO = 0.</td></tr>
<tr><td rowspan="2">ΦREF_S[7:0]</td><td rowspan="2">R/W</td><td rowspan="2">0000 0000</td><td colspan="2">ΦREF_S global SYSREF phase delay. This setting affects all QREF_r outputs configured as SYSREF.
ΦREF_S[7:0]</td></tr>
<tr><td colspan="2">Delay in ps = ΦREF_S × 543ps (256 steps)
0000 0000 = 0ps
…
1111 1111 = 138.346ns</td></tr>
<tr><td>SRG</td><td>R/W</td><td>0</td><td colspan="2">SYSREF pulse generation
0 = Internal, SPI controlled SYSREF generation using the RS bit (set SR_INSEL = 0).
1 = External controlled SYSREF generation using the EXT_SYS or CLK_3 input.</td></tr>
</table>

Table 40. SYSREF Control Register Descriptions (Cont.)

Bit Field Location			
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**
SRO	R/W	0	SYSREF pulse mode 0 = Counted SYSREF pulse generation mode. Number of pulses is controlled by SRPC[7:0]. 1 = Continuous SYSREF pulse generation.
SR_INSEL	R/W	0	SYSREF input select 0 = EXT_SYS is the SYSREF input (single-ended signal support) 1 = CLK_3 is the SYSREF input (differential signal support)
RS	W only Auto-Clear	X	Set RS = 1 to initiate the SYSREF pulse generation of continuous or SRPC of pulses. Powers up the SYSREF circuitry and releases the SYSREF pulse(s) as configured. SRG = 0; otherwise, no function. RS = 1 also phase-aligns the QREF outputs to the QCLK outputs and adds the programmed delay values into the QREF paths.
EN_QOSC_MOD[7:0]	R/W	0000 0000	Enable QOSC Configuration Modifications Set EN_QOSC_MODE[7:0] to the bit pattern 0100 1011 (0x4B) after QOSC configuration bits nPD_QOSC (0x11, D7), STYLE_QOSC (0x11, D6), and A_QOSC[1:0] (0x12, D6:5) have been written. Set EN_QOSC_MODE[7:4] to any other value (e.g., to 0x00) to prevent changes to the nPD_QOSC, STYLE_QOSC and A_QOSC[1:0] bits. If EN_QOSC_MODE[7:0] is not set to 0x4B, the QOSC output is set to its startup configuration (LVPECL, 750mV, power on).

Status Registers

Table 41. Status Register Bit Field Locations

Bit Field Location								
Register Address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x68	Reserved	Reserved	IE_LOLF	IE_LOLV	IE_CLK_3	IE_CLK_2	IE_CLK_1	IE_CLK_0
0x69	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IE_REF	IE_HOLD
0x6C	Reserved	Reserved	nLS_LOLF	nLS_LOLV	LS_CLK_3	LS_CLK_2	LS_CLK_1	LS_CLK_0
0x6D	ST_SEL[1:0]		nST_LOLF	nST_LOLV	ST_CLK_3	ST_CLK_2	ST_CLK_1	ST_CLK_0
0x6E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LS_REF	nLS_HOLD
0x6F	Reserved	Reserved	Reserved	Reserved	Reserved	ST_VCOF	ST_REF	nST_HOLD

Table 42. Status Register Descriptions[a]

Bit Field Location			
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**
IE_LOLF	R/W	0	Interrupt Enable for FemtoClock NG-PLL Loss-of-lock: 0 = Disabled: Setting nLS_LOLF will not cause an interrupt on nINT 1 = Enabled: Setting nLS_LOLF will assert the nINT output (nINT = 0, interrupt)
IE_LOLV	R/W	0	Interrupt Enable for VCXO-PLL Loss-of-lock: 0 = Disabled: setting nLS_LOLV will not cause an interrupt on nINT. 1 = Enabled: setting nLS_LOLV will assert the nINT output (nINT = 0, interrupt).
IE_CLK_*n*	R/W	0	Interrupt Enable for CLK_*n* input Loss-of-signal: 0 = Disabled: setting LS_CLK_*n* will not cause an interrupt on nINT. 1 = Enabled: setting LS_CLK_*n* will assert the nINT output (nINT = 0, interrupt).
IE_REF	R/W	0	Interrupt Enable for LS_REF: 0 = Disabled: Setting LS_REF will not cause an interrupt on nINT. 1 = Enabled: Setting LS_REF will assert the nINT output (nINT = 0, interrupt).
IE_HOLD	R/W	0	Interrupt Enable for Holdover: 0 = Disabled: setting nLS_HOLD will not cause an interrupt on nINT. 1 = Enabled: setting nLS_HOLD will assert the nINT output (nINT = 0, interrupt).
nLS_LOLF	R/W	—	FemtoClock NG-PLL Loss-of-lock (latched status of nST_LOLF): Read 0 = ≥1 Loss-of-lock events detected after the last nLS_LOLF status latch clear. Read 1 = No Loss-of-lock detected after the last nLS_LOLF status latch clear. Write 1 = Clear status latch (clears pending nLS_LOLF interrupt).
nLS_LOLV	R/W	—	VCXO-PLL Loss-of-lock (latched status of nST_LOLV): Read 0 = ≥1 Loss-of-lock events detected after the last nLS_LOLV status latch clear. Read 1 = No Loss-of-lock detected after the last nLS_LOLF status latch clear. Write 1 = Clear status latch (clears pending nLS_LOLV interrupt).
LS_CLK_*n*	R/W	—	Input CLK_*n* Status (latched status of ST_CLK_*n*): Read 0 = ≥ 1 LOS events detected on CLK_*n* after the last LS_CLK_n status latch clear. Read 1 = No Loss-of-signal detected on CLK_*n* input after the last LS_CLK_n status latch clear. Write 1 = Clear LS_CLK_*n* status latch (clears pending LS_CLK_*n* interrupts on nINT).
ST_SEL[1:0]	R	—	Input Selection (momentary): Reference Input Selection Status of the state machine. In any input selection mode, reflects the input selected by the state machine: 00 = CLK_0 01 = CLK_1 10 = CLK_2 11 = CLK_3
nST_LOLF	R	—	FemtoClock NG-PLL Loss-of-lock (momentary): Read 0 = Loss-of-lock event detected. Read 1 = No Loss-of-lock detected. A latched version of this status bit is available (nLS_LOLF).

Table 42. Status Register Descriptions[a]

Bit Field Location			
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**
nST_LOLV	R	—	VCXO-PLL Loss-of-lock (momentary): Read 0 = Loss-of-lock event detected. Read 1 = No Loss-of-lock detected. A latched version of this status bit is available (nLS_LOLV).
ST_CLK_*n*	R	—	Input CLK_*n* Status (momentary): 0 = LOS detected on CLK_*n.* 1 = No LOS detected, CLK_*n* input is active. Latched versions of these status bits are available (LS_CLK_*n*).
LS_REF	R/W	—	PLL Reference Status (latched status of ST_REF): Read 0 = Reference is lost after the last LS_REF status latch clear. Read 1 = Reference is valid after the last LS_REF status latch clear. Write 1 = Clear LS_REF status latch (clears pending LS_REF interrupts on nINT).
nLS_HOLD	R/W	—	Holdover Status Indicator (latched status of nST_HOLD): Read 0 = VCXO-PLL has entered holdover state at least 1 time after the last nLS_HOLD status latch clear. Read 1 = VCXO-PLL is (or attempts to) lock(ed) to an input clock. Write 1 = Clear status latch (clears pending nLS_HOLD interrupt).
ST_VCOF	R	—	FemtoClock NG-PLL Calibration Status (momentary): Read 0 = FemtoClock NG PLL auto-calibration is completed. Read 1 = FemtoClock NG PLL calibration is active (not completed).
ST_REF	R	—	Input Reference Status: A latched version of this status bit is available (LS_REF). 0 = No input reference present. 1 = Input reference is present.
nST_HOLD	R	—	Holdover Status Indicator (momentary): 0 = VCXO-PLL in holdover state, not locked to any input clock. 1 = VCXO-PLL is (or attempts to) lock(ed) to input clock. A latched version of this status bit is available (nLS_HOLD).

[a] CLK_*n* = CLK_0, CLK_1, CLK_2, CLK_3.

General Control Registers

Table 43. General Control Register Bit Field Locations

Bit Field Location								
Register Address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x71	INIT_CLK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x72	RELOCK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x73	PB_CAL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CPOL

Table 44. General Control Register Descriptions

Bit Field Location			
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**
INIT_CLK	W only Auto-Clear	X	Set INIT_CLK = 1 to initialize divider and delay functions. Required as part of the startup procedure.
RELOCK	W only Auto-Clear	X	Setting this bit to 1 will force the FemtoClock NG PLL to re-lock.
PB_CAL	W only Auto-Clear	X	Precision Bias Calibration Setting this bit to 1 will start the calibration of an internal precision bias current source. The bias current is used as reference for outputs configured as LVDS and for as reference for the charge pump currents. This bit will auto-clear after the calibration completed. Set as part of the startup procedure.
CPOL	R/W	0	SPI Read Operation SCLK Polarity 0 = Data bits on SDAT (SPI 3-wire) / SDO (SPI 4-wire) are output at the falling edge of SCLK edge. 1 = Data bits on SDAT (SPI 3-wire) / SDO (SPI 4-wire) are output at the rising edge of SCLK edge.

Electrical Characteristics

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8V19N491-36 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 45. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD_V}	3.6V
Inputs	-0.5V to V_{DD_V} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{DD_V}+ 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O (LVDS) Continuous Current Surge Current	 50mA 100mA
Input termination current, I_{VT}	±35mA
Operating Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model[a]	2000V
ESD - Charged Device Model[a]	500V

[a] According to JEDEC JS-001-2012/JESD22-C101

Pin Characteristics

Table 46. Pin Characteristics, V_{DD_V} = 3.3V ± 5%, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
C_{IN}[a]	Input Capacitance	OSC, nOSC		2	4	pF
		Other inputs		2	4	pF
R_{PU}	Input Pull-Up Resistor	SDAT, nCS, nCLK_0, nCLK_1, nCLK_2, nCLK_3, nOSC		51		kΩ
R_{PU}	Input Pull-Down Resistor	EXT_SYS, SCLK, CLK_0, nCLK_0, CLK_1, nCLK_1, CLK_2, nCLK_2, CLK_3, CLK_3, OSC		51		kΩ
R_{OUT}	LVCMOS Output Impedance	nINT, LOCK		25		Ω

[a] Guaranteed by design

DC Characteristics

Table 47. Power Supply DC Characteristics, V_{DD_V} = 3.3V ±5%, T_A = -40°C to +85°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{DD_V}	Core Supply Voltage		3.135	3.3	3.465	V
I_{DD_TOT}	Total Power Supply Current			1480		mA

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Table 48. Typical Power Supply DC Current Characteristics, V_{DD_V} = 3.3V[a][b]

Symbol	Supply Pin Current		Test Case 1	2	3[c]	4	5	6	Unit
	QCLK_*y* QOSC	Style	LVPECL	LVPECL	LVPECL	LVPECL	LVDS	LVDS	
		State	On	On	On	On	On	On	
		Amplitude	500	750	1000	250	500	750	mV
	QREF_*r*	Style	LVDS	LVDS	LVDS	LVDS	LVDS	LVDS	
		State	On	On	Off	On	Off	Off	
		Amplitude	500	500	–	250	–	–	mV
I_{DD_CA}	Current through VDD_QCLKA pin		133	152	169	118	92	112	mA
I_{DD_CB}	Current through VDD_QCLKB pin		92	103	112	80	64	78	mA
I_{DD_CC}	Current through VDD_QCLKC pin		92	104	113	81	65	79	mA
I_{DD_CD}	Current through VDD_QCLKD pin		59	65	70	54	47	54	mA
I_{DD_CE}	Current through VDD_QCLKE pin		95	106	117	84	68	81	mA
I_{DD_RA}	Current through VDD_QREFA pin		77	77	1.6	55	2.1	2.1	mA
I_{DD_RB}	Current through VDD_QREFB pin		51	51	1.2	37	1.2	1.2	mA
I_{DD_RC}	Current through VDD_QREFC pin		52	52	1.2	37	1.2	1.2	mA
I_{DD_RD}	Current through VDD_QREFD pin		26	26	0.6	18	0.6	0.6	mA
I_{DD_INP}	Current through VDD_INP pin		87	87	87	87	87	87	mA
I_{DD_SPI}	Current through VDD_SPI pin		7	7	7	7	7	7	mA
I_{DD_OSC}	Current through VDD_OSC and VDD_CP pins		57	66	28	52	44	53	mA
I_{DD_SYNC}	Current through VDD_SYNC pin		90	91	91	91	91	91	mA
I_{DD_CPF}	Current through VDD_CPF pin		87	87	87	87	87	87	mA
I_{DD_LCV}	Current through VDD_LCV pin		97	97	97	97	97	97	mA
I_{DD_LCF}	Current through VDD_LCF pin		55	55	55	55	55	55	mA
P_{TOT}	Total Device Power Consumption		3.55	3.71	3.06	3.28	2.67	2.93	W
$P_{TOT, SYS}$	Total System Power Consumption[d]		3.82	4.05	3.43	3.49	2.67	2.93	W

[a] f_{CLK} (input) = 122.88MHz, f_{SYSREF} = 0.96MHz, internal SYSREF generation (continuous). QA[2:0] = 245.76MHz, QB[1:0] = 368.64MHz, QC[1:0] = 122.88MHz, QD = 614.4MHz, QE[1:0] = 61.44MHz). QCLK_y outputs terminated according to amplitude settings. QREF_*r* outputs unterminated when SYSREF is turned off.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] QOSC is powered down.

[d] Includes total device power consumption and the power dissipated in external output termination components.

Table 49. LVCMOS DC Characteristics, V_{DD_V} = 3.3V ±5%, T_A = -40°C to +85°C[a]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
Control Input EXT_SYS (1.8V logic)							
V_{IH}	Input High Voltage			1.17		V_{DD_V}	V
V_{IL}	Input Low Voltage			-0.3		0.63	V
I_{IH}	Input High Current	Input with pull-down resistor	V_{DD_V} = 3.3V, V_{IN} = 3.3V			150	µA
I_{IL}	Input Low Current		V_{DD_V} = 3.3V, V_{IN} = 0V	-5			µA
SPI Inputs SDAT (when input), SCLK, nCS (1.8V/3.3V selectable logic with input hysteresis)							
V_I	Input Voltage			-0.3		V_{DD_V}	V
V_{T+}	Positive-going Input Threshold Voltage		1.8V logic (SELSVx = 0)	0.660		1.350	V
			3.3V logic (SELSVx = 1)		1.8-2.1		V
V_{T-}	Negative-going Input Threshold Voltage		1.8V logic (SELSVx = 0)	0.495		1.170	V
			3.3V logic (SELSVx = 1)		0.75-0.97		V
V_H	Hysteresis Voltage		V_{T+} - V_{T-}	0.165		0.780	V
SPI outputs DAT (when output), SDO, nINT, LOCK (1.8V/3.3V selectable logic)							
V_{OH}	Output High Voltage		1.8V logic (SELSVx = 0) I_{OH} = -4mA	1.35			V
			3.3V logic (SELSVx = 1) I_{OH} = -4mA	2.4			V
V_{OL}	Output Low Voltage		1.8V logic (SELSVx = 0) I_{OL} = 4mA			0.45	V
			3.3V logic (SELSVx = 1) I_{OL} = 4mA			0.4	V

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Table 50. Differential Input DC Characteristics, V_{DD_V} = 3.3V ±5%, T_A = -40°C to +85°C[a]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
I_{IH}	Input High Current	Inputs with pull-down resistor[b]	V_{DD_V} = V_{IN} = 3.465V			150	µA
		Input with pull-down/pull-up resistor[c]				150	µA
I_{IL}	Input Low Current	Input with pull-down/pull-up resistor[b]	V_{DD_V} = 3.465V, V_{IN} = 0V	-150			µA
		Pull-down/pull-up inputs[c]		-150			µA

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Non-Inverting inputs: CLK_n, OSC

[c] Inverting inputs: nCLK_n, nOSC

Table 51. LVPECL DC Characteristics (QCLK_y, QREF_r, STYLE = 1), V_{DD_V} = 3.3V ±5%, T_A = -40°C to +85°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage[b]	250mV Amplitude Setting	V_{DD_V} - 1.027	V_{DD_V} - 0.838	V_{DD_V} - 0.679	V
		500mV Amplitude Setting	V_{DD_V} - 1.041	V_{DD_V} - 0.857	V_{DD_V} - 0.708	V
		750mV Amplitude Setting	V_{DD_V} - 1.054	V_{DD_V} - 0.876	V_{DD_V} - 0.755	V
		1000mV Amplitude Setting	V_{DD_V} - 1.078	V_{DD_V} - 0.898	V_{DD_V} - 0.777	V
V_{OL}	Output Low Voltage[b]	250mV Amplitude Setting	V_{DD_V} - 1.311	V_{DD_V} - 1.138	V_{DD_V} - 0.949	V
		500mV Amplitude Setting	V_{DD_V} - 1.575	V_{DD_V} - 1.421	V_{DD_V} - 1.212	V
		750mV Amplitude Setting	V_{DD_V} - 1.842	V_{DD_V} - 1.703	V_{DD_V} - 1.493	V
		1000mV Amplitude Setting	V_{DD_V} - 2.119	V_{DD_V} - 1.983	V_{DD_V} - 1.746	V

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Outputs terminated with 50Ω to V_{DD_V} – 1.5V (250mV amplitude setting), V_{DD_V} – 1.75V (500mV amplitude setting), V_{DD_V} – 2.0V (750mV amplitude setting), V_{DD_V} – 2.25V (1000mV amplitude setting)

Table 52. LVDS DC Characteristics (QCLK_y, QREF_r, STYLE = 0), V_{DD_V} = 3.3V ±5%, T_A = -40°C to +85°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{OS}	Offset Voltage[b]	250mV Amplitude Setting	2.05	2.37	2.70	V
		500mV Amplitude Setting	1.90	2.21	2.55	V
		750mV Amplitude Setting	1.75	2.06	2.39	V
		1000mV Amplitude Setting	1.60	1.91	2.20	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] V_{OS} changes with V_{DD_V}

AC Characteristics

Table 53. AC Characteristics, V_{DD_V} = 3.3V ±5%, T_A = -40°C to +85°C[a][b]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
f_{OUT}	Output Frequency		QCLK_*y*, QREF_*r* (Clock), N = ÷1		3686.4		MHz
			QCLK_*y*, QREF_*r* (Clock), N = ÷2		1843.2		MHz
			QCLK_*y*, QREF_*r* (Clock), N = ÷3		1228.8		MHz
			QCLK_*y*, QREF_*r* (Clock), N = ÷4		921.6		MHz
			QCLK_*y*, QREF_*r* (Clock), N = ÷5		737.28		MHz
			QCLK_*y*, QREF_*r* (Clock), N = ÷6		614.4		MHz
			QCLK_*y*, QREF_*r* (Clock), N = ÷10		368.64		MHz
			QCLK_*y*, QREF_*r* (Clock), N = ÷12		307.2		MHz
			QCLK_*y*, QREF_*r* (Clock), N = ÷15		245.76		MHz
			QCLK_*y*, QREF_*r* (Clock), N = ÷30		122.88		MHz
			QREF_*r* (SYSREF)	0.288		57.6	MHz
f_{VCO}	VCO Frequency			3300	3686.4	3900	MHz
f_{CLK}	Input Frequency		CLK_*n*	30.72	245.76	2000	MHz
f_{VCXO}	VCXO Frequency			30.72	122.88	245.76	MHz
Δ_{fp}	Static Frequency Error		f_{CLK} = 0pbb frequency deviation			0	ppb
Δ_{frms}	Dynamic Frequency Error RMS[c]		f_{CLK} = 0ppb frequency deviation			0.5	ppb
V_{IN}	Input Voltage Amplitude[d]	CLK_*n*, OSC/nOSC		0.15		1.2	V
V_{DIFF_IN}	Differential Input Voltage Amplitude[d, e]	CLK_*n*, OSC/nOSC		0.3		2.4	V
V_{CMR}	Common Mode Input Voltage			1.0		V_{DD_V} – (V_{IN} / 2)	V

Table 53. AC Characteristics, V_{DD_V} = 3.3V ±5%, T_A = -40°C to +85°C[a][b] (Cont.)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
odc	Output Duty Cycle		QCLK_*y*, QREF_*r* (Clock)	45	50	55	%
t_R / t_F	Output Rise/Fall Time, Differential		QCLK_*y*, QREF_*r* (LVPECL), 20– 80%			250	ps
			QCLK_*y*, QREF_*r* (LVDS), 20–80%			250	ps
			QREF_*r* (SYSREF, LVDS), 20–80%			250	ps
	Output Rise/Fall Time		LVCMOS outputs, 20-80%			1	ns
$V_{O(PP)}$[f]	LVPECL Output Voltage Swing, Peak-to-peak (see Table 51)	250mV Amplitude	1843.2MHz 614.4MHz	225 240	280 270	335 315	mV
		500mV Amplitude	1843.2MHz 614.4MHz	430 450	515 515	600 580	mV
		750mV Amplitude	1843.2MHz 614.4MHz	625 670	730 760	840 850	mV
		1000mV Amplitude	1843.2MHz 614.4MHz	800 890	920 1000	1050 1100	mV
	LVPECL Differential Output Voltage Swing, Peak-to-peak (see Table 51)	250mV Amplitude	1843.2MHz 614.4MHz	450 480	560 550	670 630	mV
		500mV Amplitude	1843.2MHz 614.4MHz	860 900	1030 1030	1200 1160	mV
		750mV Amplitude	1843.2MHz 614.4MHz	1250 1340	1460 1520	1680 1700	mV
		1000mV Amplitude	1843.2MHz 614.4MHz	1600 1780	1840 2000	2100 2200	mV
V_{OD}[g]	LVDS Output Voltage Swing, Peak-to-peak (see Table 51)	250mV Amplitude	1843.2MHz 614.4MHz	144 194	181 222	220 250	mV
		500mV Amplitude	1843.2MHz 614.4MHz	319 409	377 456	435 503	mV
		750mV Amplitude	1843.2MHz 614.4MHz	475 623	567 694	658 765	mV
		1000mV Amplitude	1843.2MHz 614.4MHz	600 827	742 926	885 1024	mV
	LVDS Differential Output Voltage Swing, Peak-to-peak (see Table 51)	250mV Amplitude	1843.2MHz 614.4MHz	288 388	362 444	440 500	mV
		500mV Amplitude	1843.2MHz 614.4MHz	638 818	754 912	870 1006	mV
		750mV Amplitude	1843.2MHz 614.4MHz	950 1246	1134 1388	1316 1530	mV
		1000mV Amplitude	1843.2MHz 614.4MHz	1200 1654	1484 1852	1770 2048	mV

Table 53. AC Characteristics, V_{DD_V} = 3.3V ±5%, T_A = -40°C to +85°C[a][b] (Cont.)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
Δt_{PD}	Propagation delay variation between reference input and any QCLK_y output			-200		+200	ps
*t*sk(o)	Output Skew; NOTE[h] [i] All delays set to 0		QCLK_*y* (same N divider)		35	100	ps
			QCLK_*y* (any N divider, incident rising edge)		35	100	ps
			QREF_*r* (Clock)		100	150	ps
			QREF_*r* (SYSREF)		50	100	ps
			QREF_*r* (Clock) to QCLK_*y* (any divider, incident rising QCLK edge)		100	150	ps
			QREF_*r* (SYSREF) to QCLK_*y* (any divider, incident rising QCLK edge)		100	150	ps
ΔF	Output isolation between any neighboring clock output		f_{OUT} = 614.4MHz	65	70		dB
			f_{OUT} = 245.76MHz	70	80		dB
ΔF	Output isolation between any QCLK_*y*, QREF_*r* (SYSREF[j]) output		Both SYSREF and clock signals active	50	75		dB
$t_{D, LOS}$	LOS state detected (measured in input reference periods)		f_{CLK} = 122.88MHz or 245.76MHz			2	T_{IN}
$t_{D, LOCK}$	PLL lock detect		PLL re-lock time after a short-term holdover scenario. Measured from LOS to both PLLs lock-detect asserted; hold-off timer = TBD, VCXO-PLL bandwidth = 100Hz, initial frequency error < 200 ppm.			300	ms
$t_{D, RES}$	PLL lock residual time error		Refer to PLL lock detect $t_{D,LOCK}$. Reference point: final value of clock output phase after all phase transitions settled.			20	ns
Δf_{HOLD}	Holdover accuracy		Maximum frequency deviation during a holdover duration of 200ms and after the clock re-validate event		±0.5	±5	ppm
$t_{D, RES-H}$	Holdover residual error.		Measured 50ms after the reference clock re-appeared in a holdover scenario. Reference point: final value of clock output phase after all phase transitions settled.			±8.138	ns
t_{H_E}	Hold Time	EXT_SYS to CLK_n		1			ns
t_{S_E}	Setup Time	EXT_SYS to CLK_n		0			ns

Table 53. AC Characteristics, V_{DD_V} = 3.3V ±5%, T_A = -40°C to +85°C[a][b] (Cont.)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
t_{W_E}	Pulse Width	EXT_SYS		2			ns
t_{H_C}	Hold Time	CLK_3 to CLK_n		0			ns
t_{S_C}	Setup Time	CLK_3 to CLK_n		0			ns
t_{W_C}	Pulse Width	CLK_3		2			ns

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] VCXO-PLL bandwidth = 100Hz.

[c] RMS frequency error, measured at any QCLK_*y* output, caused by Gaussian noise. Weighted with a 1ms low pass time window filter.

[d] V_{IL} should not be less than -0.3V and V_{IH} should not be greater than V_{DD_V}

[e] Common Mode Input Voltage is defined as the cross-point voltage.

[f] LVPECL outputs terminated with 50Ω to V_{DD_V} – 1.5V (250mV amplitude setting), V_{DD_V} – 1.75V (500mV amplitude setting), V_{DD_V} – 2.0V (750mV amplitude setting), V_{DD_V} – 2.25V (1000mV amplitude setting)

[g] LVDS outputs terminated 100Ω across terminals.

[h] This parameter is defined in accordance with JEDEC standard 65.

[i] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.

[j] SYSREF frequencies: 15.36, 7.68, 3.84MHz.

Table 54. Clock Phase Noise Characteristics, V_{DD_V} = 3.3V ±5%, T_A = -40°C to +85°C[a][b][c]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
*t*jit(Ø)	Clock RMS Phase Jitter (Random), 737.28MHz		Integration Range: 1kHz–76.8MHz		81	107	fs
			Integration Range: 12kHz–20MHz		65	86	fs
Φ_N(10)	Clock Single-side Band Phase Noise	1843.2MHz	10Hz offset (determined by VCXO)		-61	-59	dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-82.5	-78.9	dBc/Hz
Φ_N(500)			500Hz offset from carrier		-98.6	-96.9	dBc/Hz
Φ_N(1k)			1kHz offset from carrier		-104	-103	dBc/Hz
Φ_N(10k)			10kHz offset from carrier		-117.6	-113.9	dBc/Hz
Φ_N(60k)			60kHz offset from carrier		-120	-114.4	dBc/Hz
Φ_N(100k)			100kHz offset from carrier		-121.6	-118.7	dBc/Hz
Φ_N(200k)			200kHz offset from carrier		-125	-122.3	dBc/Hz
Φ_N(800k)			800kHz offset from carrier		-135.7	-134.2	dBc/Hz
Φ_N(5M)			5MHz offset from carrier		-150	-145.4	dBc/Hz
Φ_N(≥10M)			≥ 10MHz offset from carrier and noise floor		-152	-147.9	dBc/Hz
Φ_N(10)	Clock Single-side Band Phase Noise	614.4MHz	10Hz offset (determined by VCXO)		-71	-67	dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-92	-89	dBc/Hz
Φ_N(500)			500Hz offset from carrier		-108.5	-105.7	dBc/Hz
Φ_N(1k)			1kHz offset from carrier		-114.2	-112.1	dBc/Hz
Φ_N(10k)			10kHz offset from carrier		-126.2	-122.2	dBc/Hz
Φ_N(60k)			60kHz offset from carrier		-128.8	-122.8	dBc/Hz
Φ_N(100k)			100kHz offset from carrier		-130.5	-127.8	dBc/Hz
Φ_N(200k)			200kHz offset from carrier		-133.9	-131.6	dBc/Hz
Φ_N(800k)			800kHz offset from carrier		-144.4	-143.7	dBc/Hz
Φ_N(5M)			5MHz offset from carrier		-155.4	-151.8	dBc/Hz
Φ_N(≥10M)			≥ 10MHz offset from carrier and noise floor		-156	-153	dBc/Hz

Table 54. Clock Phase Noise Characteristics, V_{DD_V} = 3.3V ±5%, T_A = -40°C to +85°C[a][b][c] (Cont.)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
$\Phi_N(10)$	Clock Single-side Band Phase Noise	307.2MHz	10Hz offset (determined by VCXO)		-74.5	-71.1	dBc/Hz
$\Phi_N(100)$			100Hz offset (determined by VCXO)		-100.9	-94.3	dBc/Hz
$\Phi_N(500)$			500Hz offset from carrier		-114.4	-112.2	dBc/Hz
$\Phi_N(1k)$			1kHz offset from carrier		-120.4	-117.9	dBc/Hz
$\Phi_N(10k)$			10kHz offset from carrier		-133.2	-129.3	dBc/Hz
$\Phi_N(60k)$			60kHz offset from carrier		-135.2	-127.9	dBc/Hz
$\Phi_N(100k)$			100kHz offset from carrier		-137	-133.8	dBc/Hz
$\Phi_N(200k)$			200kHz offset from carrier		-140.3	-137.5	dBc/Hz
$\Phi_N(800k)$			800kHz offset from carrier		-150.4	-149.1	dBc/Hz
$\Phi_N(5M)$			5MHz offset from carrier		-158.3	-152.8	dBc/Hz
$\Phi_N(\geq 10M)$			≥ 10MHz offset from carrier and noise floor		-159	-153	dBc/Hz
$\Phi_N(10)$	Clock Single-side Band Phase Noise	245.76MHz	10Hz offset (determined by VCXO)		-76.4	-73.7	dBc/Hz
$\Phi_N(100)$			100Hz offset (determined by VCXO)		-101.3	-96.4	dBc/Hz
$\Phi_N(500)$			500Hz offset from carrier		-115.8	-113.4	dBc/Hz
$\Phi_N(1k)$			1kHz offset from carrier		-121.9	-119.8	dBc/Hz
$\Phi_N(10k)$			10kHz offset from carrier		-135.1	-129.2	dBc/Hz
$\Phi_N(60k)$			60kHz offset from carrier		-137.5	-130.7	dBc/Hz
$\Phi_N(100k)$			100kHz offset from carrier		-139.3	-135.7	dBc/Hz
$\Phi_N(200k)$			200kHz offset from carrier		-142.6	-139.2	dBc/Hz
$\Phi_N(800k)$			800kHz offset from carrier		-152.5	-151.1	dBc/Hz
$\Phi_N(5M)$			5MHz offset from carrier		-160	-154.1	dBc/Hz
$\Phi_N(\geq 10M)$			≥10MHz offset from carrier and noise floor		-161	-154.2	dBc/Hz

Table 54. Clock Phase Noise Characteristics, V_{DD_V} = 3.3V ±5%, T_A = -40°C to +85°C[a][b][c] (Cont.)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
Φ	Spurious Signals (QCLK, QREF as clock)	614.4MHz	100Hz–300Hz		-83	-80	dBc
			300Hz–100kHz		-106	-103	dBc
			100kHz–100MHz		-90	-84	dBc
			307.2MHz spurious[d]		-92	-85	dBc
			153.6MHz spurious		-95	-86	dBc
			122.88MHz spurious[e]		-88	-83	dBc
		307.2MHz	100Hz–300Hz		-88	-83	dBc
			300Hz–100kHz		-111	-104	dBc
			100kHz–100MHz		-95	-91	dBc
			153.6MHz spurious		-110	-103	dBc
			122.88MHz spurious[f]		-103	-96	dBc
		245.76MHz	100Hz–300Hz		-90	-83	dBc
			300Hz–100kHz		-110	-106	dBc
			100kHz–100MHz		-96	-93	dBc
			122.88MHz spurious		-88	-83	dBc

[a] Phase noise and spurious specifications apply for device operation with QREF_*r* outputs inactive (no SYSREF pulses generated). Phase noise specifications are applicable for all outputs active, Nx not equal.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] Phase noise characteristics at lower frequency offsets (10Hz ~1kHz) is primarily a function of the VCXO phase noise: VCXO characteristics: f = 122.88MHz; phase noise: -80.9dBc/Hz(10Hz), -106.3dBc/Hz(100Hz), -128.8dBc/Hz(1kHz), -144.8dBc/Hz(10kHz), -150.9dBc/Hz(100kHz):.

[d] Measured at all offset frequencies except at f_{OFFSET} = 307.2MHz.

[e] Measured at all offset frequencies except at f_{OFFSET} = 122.88MHz.

[f] Measured at all offset frequencies except at f_{OFFSET} = 122.88MHz.

Table 55. SYSREF Phase Noise Characteristics, V_{DD_V} = 3.3V ±5%, T_A = -40°C to +85°C[a][b]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
$\Phi_N(500)$	SYSREF Single-side Band Phase Noise	30.72MHz	500Hz offset		-130.0	-129.0	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier		-150.7	-148.1	dBc/Hz
$\Phi_N(60k)$			60kHz offset from Carrier		-153.3	-150.2	dBc/Hz
$\Phi_N(800k)$			800kHz offset from Carrier		-156.7	-152.2	dBc/Hz
$\Phi_N(\geq 3M)$			≥ 3MHz offset from Carrier and Noise Floor		-158.2	-152.1	dBc/Hz
Φ	Spurious Signals[c]	3.84MHz	> 500Hz		-70.0	-66.0	dBc
		15.36MHz	> 500Hz		-70.0	-66.0	dBc
		7.68MHz	> 500Hz		-70.0	-66.0	dBc

[a] Phase noise is measured as additive phase noise contribution by the device on all SYSREF outputs, dividers and channel logic. SYSREF signals measured as continued clock signal. Clock signals (QCLK) are turned on.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] Measured as sum of all spurious amplitudes in one side band in the offset frequency range above 500Hz, excluding the harmonics of the fundamental frequency of n × f_{SYSREF} (e.g. n × 7.68MHz).

Table 56. AC Characteristics: Typical QCLK_y Output Amplitude, V_{DD_V} = 3.3V, T_A = 25°C[a]

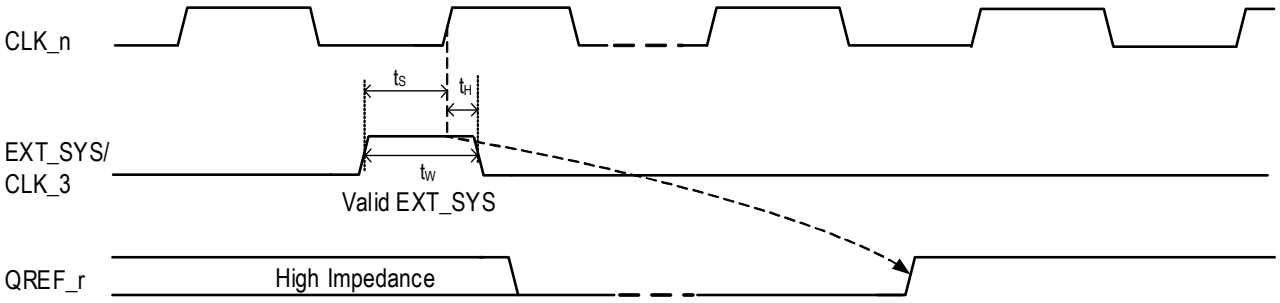
Symbol	Parameter	Test Conditions	QCLK_y Output Frequency in MHz						Unit
			3686.4	1843.2	1228.8	737.28	368.64	245.76	
$V_{O(PP)}$[b]	LVPECL Output Voltage Swing, Peak-to-peak	250mV Amplitude Setting	155	337	337	240	257	281	mV
		500mV Amplitude Setting	270	575	600	465	485	530	mV
		750mV Amplitude Setting	360	800	875	710	710	800	mV
		1000mV Amplitude Setting	450	920	1100	950	925	1040	mV
V_{OD}[c]	LVDS Output Voltage Swing, Peak-to-peak	250mV Amplitude Setting	117	210	216	196	225	250	mV
		500mV Amplitude Setting	240	435	455	405	445	500	mV
		750mV Amplitude Setting	342	670	675	610	665	750	mV
		1000mV Amplitude Setting	426	850	875	800	890	995	mV

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] LVPECL outputs terminated with 50Ω to V_{DD_V} – 1.5V (250mV amplitude setting), V_{DD_V} – 1.75V (500mV amplitude setting), V_{DD_V} – 2.0V (750mV amplitude setting), V_{DD_V} – 2.25V (1000mV amplitude setting)

[c] LVDS outputs terminated 100Ω across terminals

Figure 8. EXT_SYS Input Timing Diagram



Clock Phase Noise Characteristics

Measurement conditions for phase noise characteristics:

- VCXO characteristics: f = 122.88MHz; phase noise: -80.9dBc/Hz(10Hz), -106.3dBc/Hz(100Hz), -128.8dBc/Hz(1kHz), -144.8dBc/Hz(10kHz), -150.9dBc/Hz(100kHz):
- Input frequency: 122.88MHz
- I_{CPV} VCXO-PLL charge pump current: 0.55mA
- VCXO-PLL bandwidth: 6Hz
- I_{CPF} FemtoClock NG charge pump current: 2.0mA
- FemtoClock NG PLL bandwidth: 127kHz
- LVPECL output with 750 mV amplitude setting
- V_{DD_V} = 3.3V, T_A = 25°C

Figure 9. 1843.2MHz Output Phase Noise

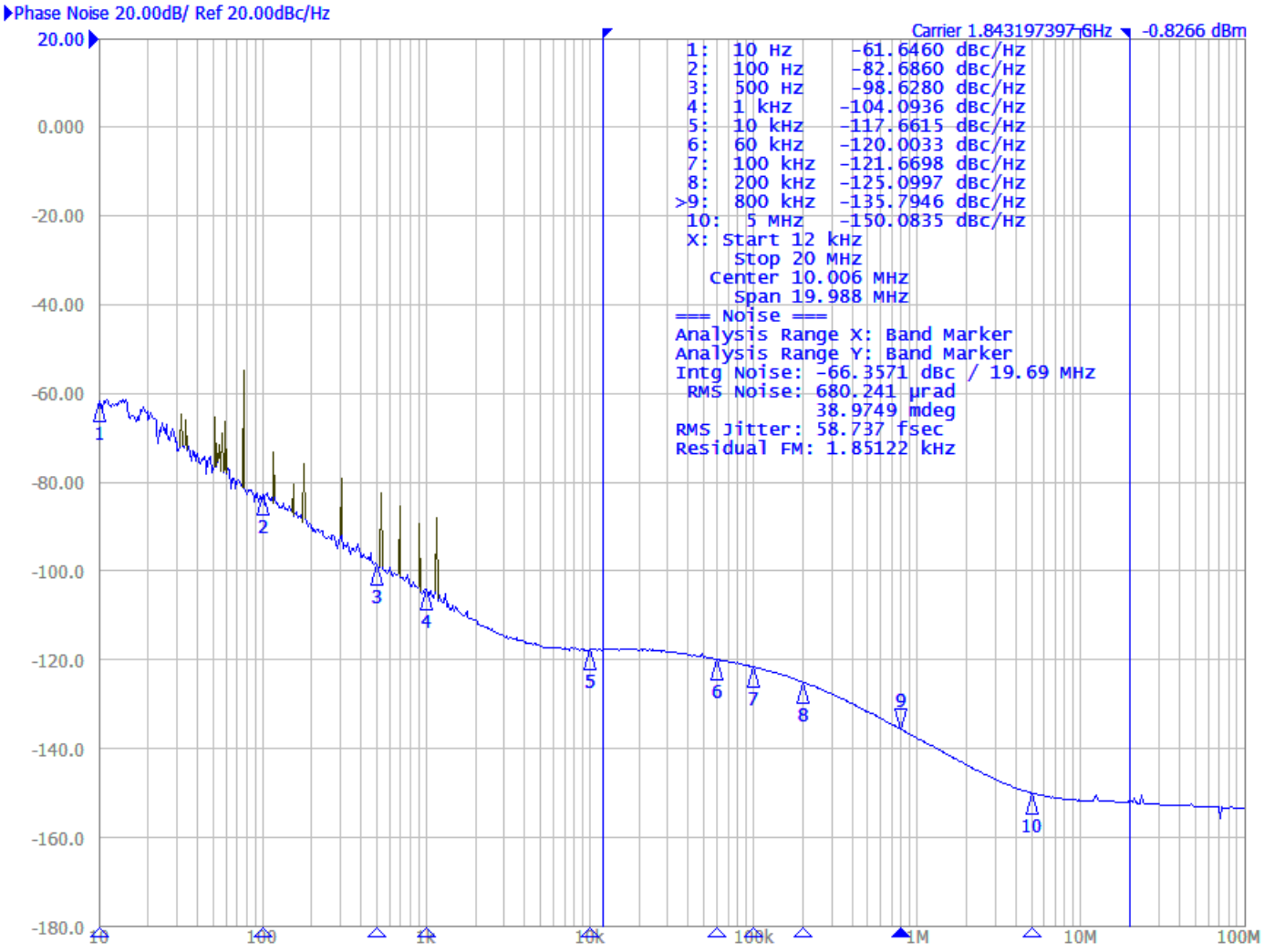


Figure 10. 614.4MHz Output Phase Noise

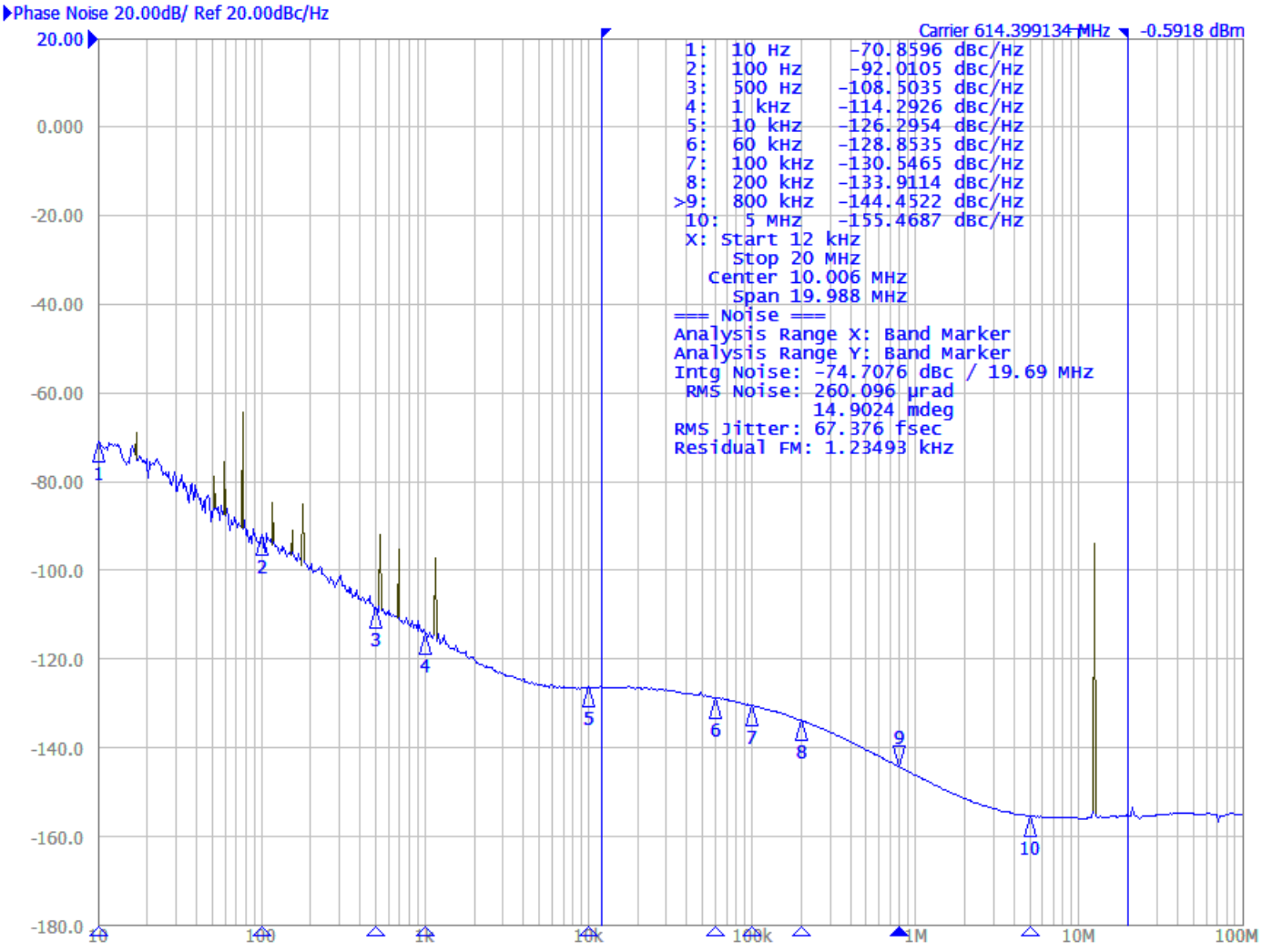


Figure 11. 307.2MHz Output Phase Noise

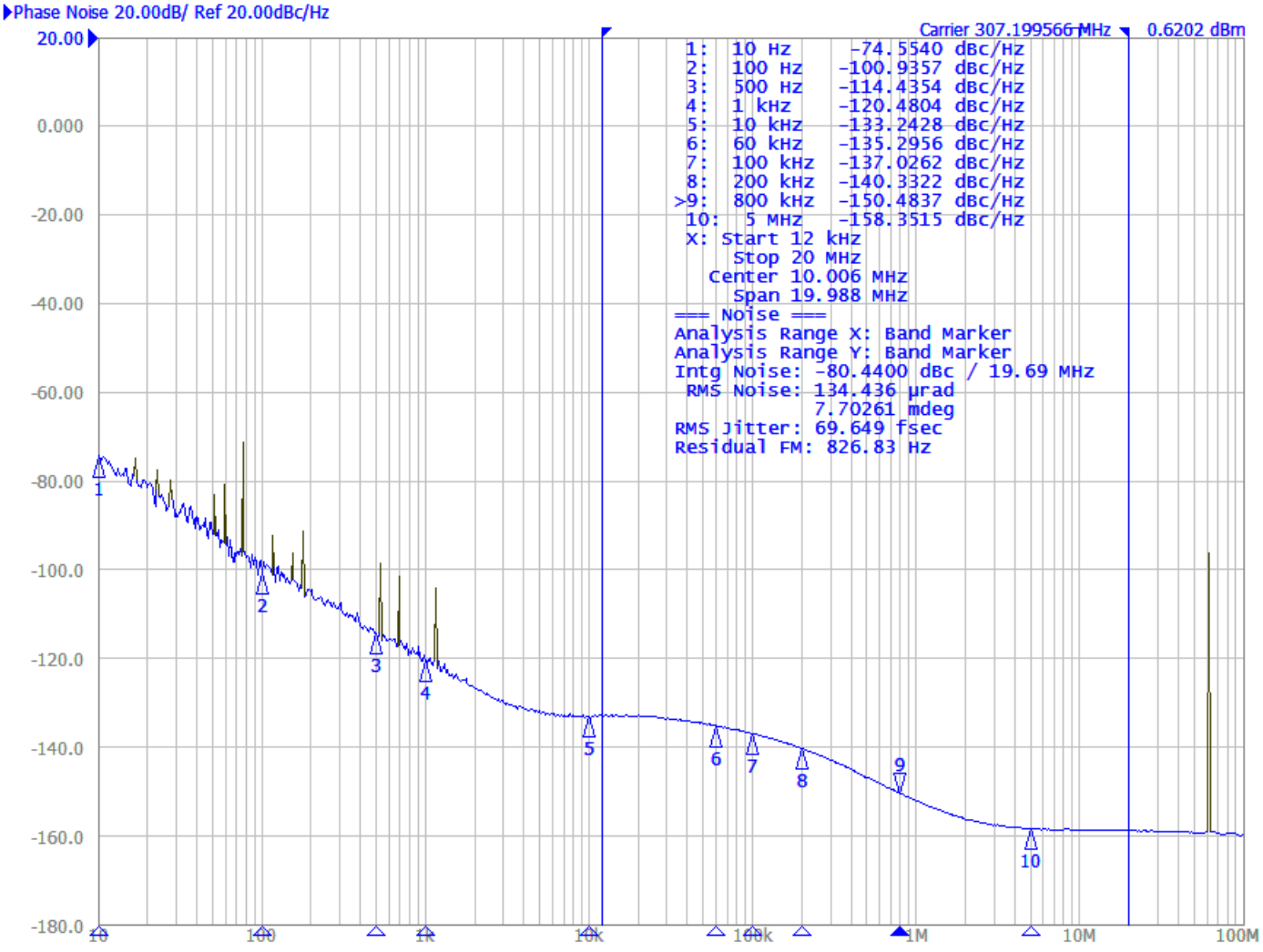
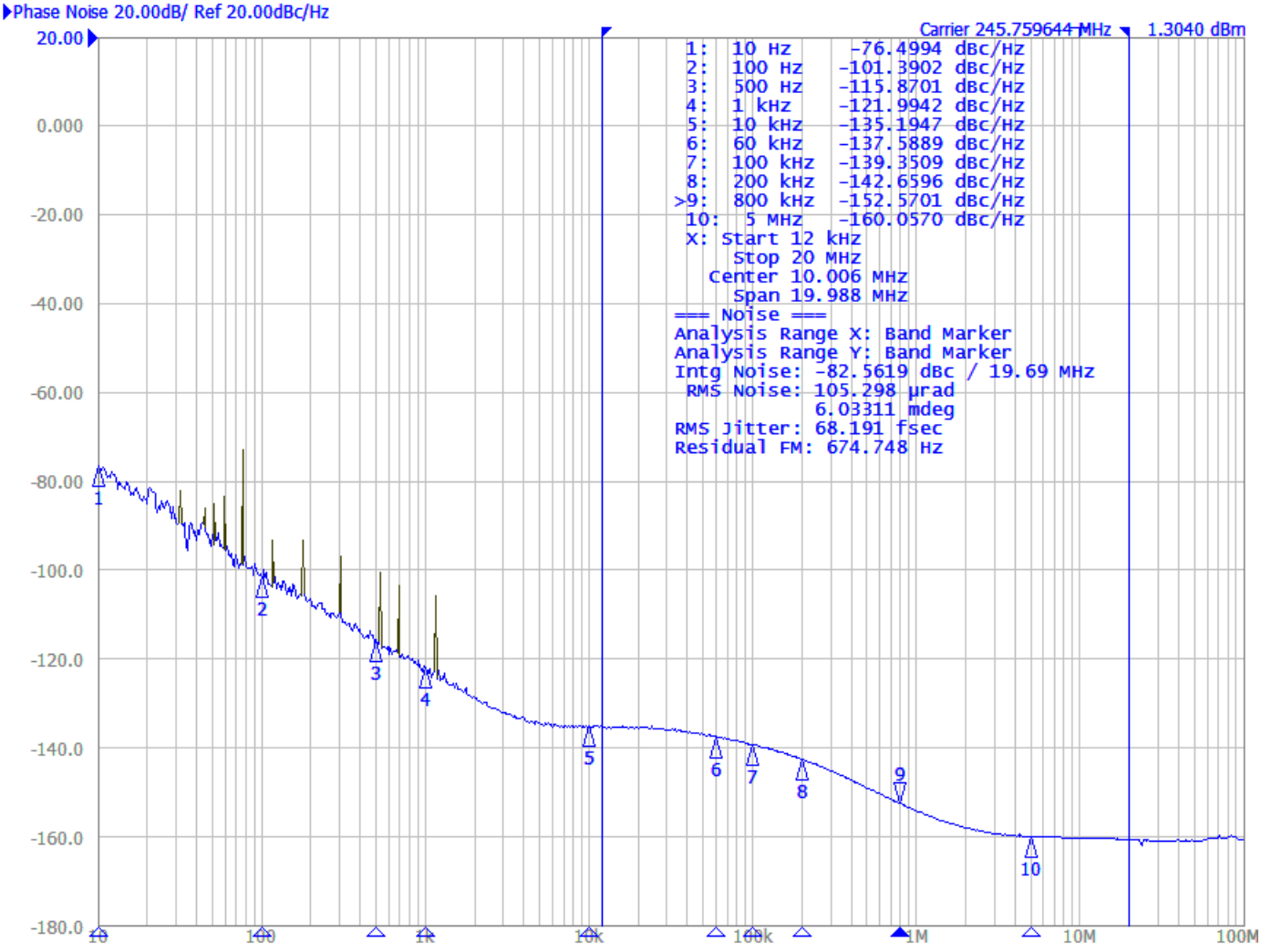


Figure 12. 245.76MHz Output Phase Noise

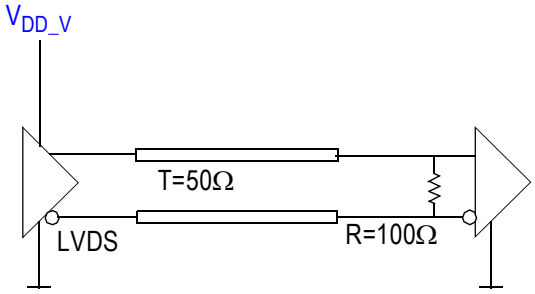


Application Information

Termination for QCLK_y, QREF_r LVDS Outputs (STYLE = 0)

Figure 13 shows an example termination for the QCLK_*y*, QREF_*r* LVDS outputs. In this example, the characteristic transmission line impedance is 50Ω. The termination resistor R (100Ω) is matched to the line impedance. The termination resistor must be placed at the line end. No external termination resistor is required if R is an internal part of the receiver circuit. The LVDS termination in the figure is applicable for any output amplitude setting specified in Table 16.

Figure 13. LVDS (STYLE = 0) Output Termination



AC Termination for QCLK_y, QREF_r LVDS Outputs (STYLE = 0)

Figure 14 and Figure 15 show example AC terminations for the QCLK_*y*, QREF_*r* LVDS outputs. In the examples, the characteristic transmission line impedance is 50Ω. In Figure 14, the termination resistor R (100Ω) is placed at the line end. No external termination resistor is required if R is an internal part of the receiver circuit. The LVDS terminations in both Figure 14 and Figure 15 are applicable for any output amplitude setting specified in Table 16. The receiver input should be re-biased according to its common mode range specifications.

Figure 14. LVDS (STYLE = 0) AC Output Termination

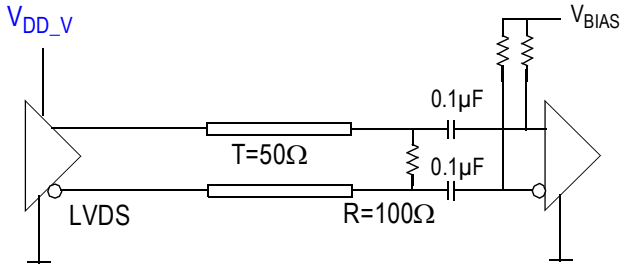
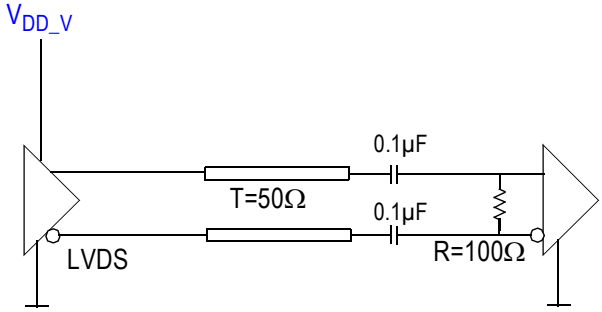


Figure 15. LVDS (STYLE = 0) AC Output Termination



Termination for QCLK_y, QREF_r LVPECL Outputs (STYLE = 1)

Figure 16 shows an example termination for the QCLK_*y*, QREF_*r* LVPECL outputs. In this example, the characteristic transmission line impedance is 50Ω. The R1 (50Ω) and R2 (50Ω) resistors are matched load terminations. The output is terminated to the termination voltage V_T. The V_T must be set according to the output amplitude setting defined in Table 16. The termination resistors must be placed close at the line end.

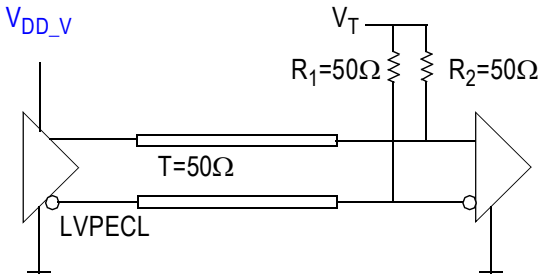
Figure 16. LVPECL (STYLE = 1) Output Termination

$V_T = V_{DD\_V}$ - 1.50V (250mV Amplitude)

$V_T = V_{DD\_V}$ - 1.75V (500mV Amplitude)

$V_T = V_{DD\_V}$ - 2.00V (750mV Amplitude)

$V_T = V_{DD\_V}$ - 2.25V (1000mV Amplitude)



Thermal Characteristics

Table 57. Thermal Characteristics for 100-CABGA Package[a]

Multi-Layer PCB, JEDEC Standard Test Board				
Symbol	**Thermal Parameter**	**Condition**	**Value**	**Unit**
Θ_{JA}	Junction to ambient	0 m/s air flow	24.06	°C/W
		1 m/s air flow	20.89	
		2 m/s air flow	19.07	
		3 m/s air flow	18.05	
		4 m/s air flow	17.46	
		5 m/s air flow	17.03	
Θ_{JC}	Junction to case	—	8.54	
Θ_{JB}	Junction to board	—	6.43	
Ψ_{JB}	Junction to board	—	4.15	

[a] Standard JEDEC 2S2P multilayer PCB

Temperature Considerations

The device supports applications in a natural convection environment as long as the junction temperature does not exceed the specified junction temperature T_J. In applications where the heat dissipates through the PCB, Θ_{JB} is the correct metric to calculate the junction temperature. Ψ_{JB} is the right metric in all other applications where the majority of the heat dissipates through the board (80%) and a minority (20%) through the top of the device. The following calculation uses the junction-to-board thermal characterization parameter Θ_{JB} to calculate the junction temperature (T_J). Care must be taken to not exceed the maximum allowed junction temperature T_J of 125 °C.

The junction temperature T_J is calculated using the following equation: $T_J = T_B + P_{TOT} \times \Psi_{JB}$

where:

- T_J is the junction temperature at steady state conditions in °C
- T_B is the board temperature at steady state condition in °C, measured on or near the component lead
- Ψ_{JB} is the thermal characterization parameter to report the difference between T_J and T_B
- P_{TOT} is the total device power dissipation

The 8V19N491-36 maximum power dissipation scenario: With the maximum allowed junction temperature and the maximum device power consumption and at the maximum supply voltage of 3.3V + 5%, the maximum supported board temperature can be determined. In the device configuration for the maximum power consumption, I_{DD_V} is 1480mA (see Table 47). In this configuration, all outputs are active and configured to LVDS, the output amplitude is set to 1000mV (QOSC: 750,V amplitude) and outputs use a 100Ω termination:

- Total system power dissipation (including termination resistor power): $P_{TOT} = V_{DD\_V, MAX} \times I_{DD\_V, MAX} = 3.465V \times 1480mA = 5.1282W$
- Total device power dissipation (excluding termination resistor power): $P_{TOT} = 5.1282W$

In this scenario and with the Ψ_{JB} thermal model, the maximum supported board temperature is:

- $T_{B, MAX} = T_{J, MAX} - \Psi_{JB} \times P_{TOT}$
- $T_{B, MAX} = 125°C - 6.43°C/W \times 5.1282W$
- $T_{B, MAX} = 92.0°C$

Application using the device at the maximum power dissipation must keep the board temperature below 92.0°C.

Application power dissipation scenarios: Applications may use device settings that result in a lower power dissipation than the maximum power scenario. The device is a multi-functional, high-speed device that targets a variety of applications. Since this device is highly programmable with a broad range of settings and configurations, the power consumption will vary as settings and configurations are changed. Table 47 shows the typical current consumption and total device power consumption along with the junction temperature for the 6 test cases shown in Table 48. The table also displays the maximum board temperature for the Θ_{JB} model.

Table 58. Typical Device Power Dissipation and Junction Temperature

Test Case[a]	Output Configuration	Device		Θ_{JB} Thermal Model	
		I_{DD_TOT}	P_{TOT}	T_J[b]	$T_{B, MAX}$[c]
		mA	W	°C	°C
1	QCLK: LVPECL, 500mV QREF: LVDS, 500mV	1155.7	3.55	107.8	102.2
2	QCLK: LVPECL, 750mV QREF: LVDS, 500mV	1223.4	3.71	108.9	101.1
3	QCLK: LVPECL, 1000mV QREF: LVDS (off)	1033.4	3.06	104.7	105.3
4	QCLK: LVPECL, 250mV QREF: LVDS, 250mV	1036.8	3.28	106.1	103.9
5	QCLK: LVDS, 500mV QREF: LVDS (off)	806.0	2.67	102.2	107.8
6	QCLK: LVDS, 750mV QREF: LVDS (off)	883.5	2.93	103.8	106.2

[a] For device settings (see Table 48).

[b] Junction temperature at board temperature T_B = 85°C.

[c] Maximum board temperature for junction temperature <125°C.

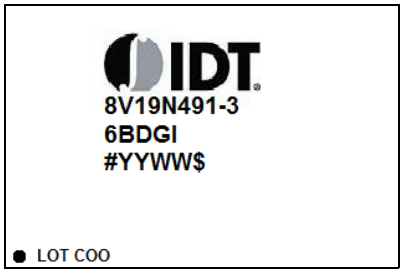
Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available and is subject to change without notice or revision of this document.

Ordering Information

Part Number	Package Description	Carrier	Temperature Range
8V19N491-36BDGI	RoHS 6/6 11 × 11 mm, 100-CABGA	Tray	-40°C to +85°C
8V19N491-36BDGI8		Tape and Reel	

Marking Diagram



- Lines 1 and 2 are the part number.
- Line 3:
  - "#" denotes stepping.
  - "YYWW" denotes: "YY" is the last two digits of the year, and "WW" is the work week number that the part was assembled.
  - "$" denotes the mark code.
- "LOT COO" denotes lot sequence number and country of origin.

Glossary

Abbreviation	Description
Index *n*	Denominates a clock input CLK_*n*. Range: 0 to 3
Index *x*	Denominates a channel, channel frequency divider and the associated configuration bits. Range: A, B, C, D, E
Index y	Denominates a QCLK output and associated configuration bits. Range: A0, A1, A2, B0, B1, C0, C1,D, E0,E1
Index *r*	Denominates a QREF output and associated configuration bits. Range: A0, A1, A2, B0, B1, C0, C1, D
V_{DD_V}	Denominates voltage supply pins. Range: VDD_QCLKA, VDD_QREFA, VDD_QCLKB, VDD_QREFB, VDD_QCLKC, VDD_QREFC, VDD_QCLKD, VDD_QREFD, VDD_QCLKE, VDD_SPI, VDD_INP, VDD_LCV, VDD_LCF, VDD_CP, VDD_SYNC, VDD_CPF,VDD_OSC
status_condition	Status conditions are: LOLV (Loss of VCXO-PLL lock), LOLF (Loss of FemtoClock NG PLL lock) and LOS (Loss of input signal)
[...]	Index brackets describe a group associated with a logical function or a bank of outputs.
{…}	List of discrete values
Suffix V	Denominates a function associated with the VCXO-PLL
Suffix F	Denominates a function associated with the 2nd stage PLL (FemtoClock NG)

Revision History

Date	Description of Change
November 20, 2023	Added “LVPECL” in Pin Descriptions for ball numbers G9/10, F9/10, E9/10, A5/4, B5/4, F2/1, G2/1, D5/4.
November 5, 2020	Updated Output Phase Delay
April 20, 2020	Corrected a typo in the description of pin J5 in Table 1
April 24, 2019	Updated the t_{H_E}, t_{S_E}, t_{W_E}, t_{H_C}, t_{S_C}, and t_{W_C} parameters in Table 53
April 2, 2019	Initial release.

CABGA-100, Package Outline Drawing

11.0 x 11.0 x 1.1 mm Body, 1.0mm Pitch

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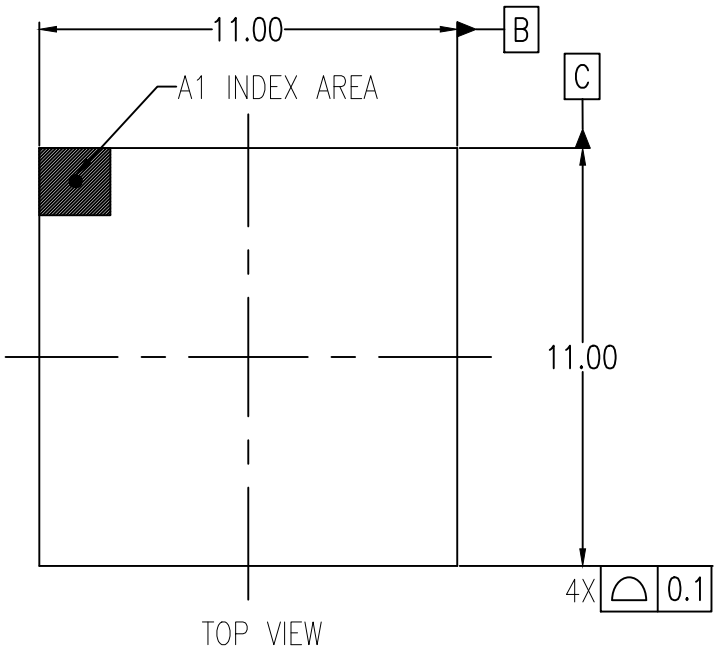
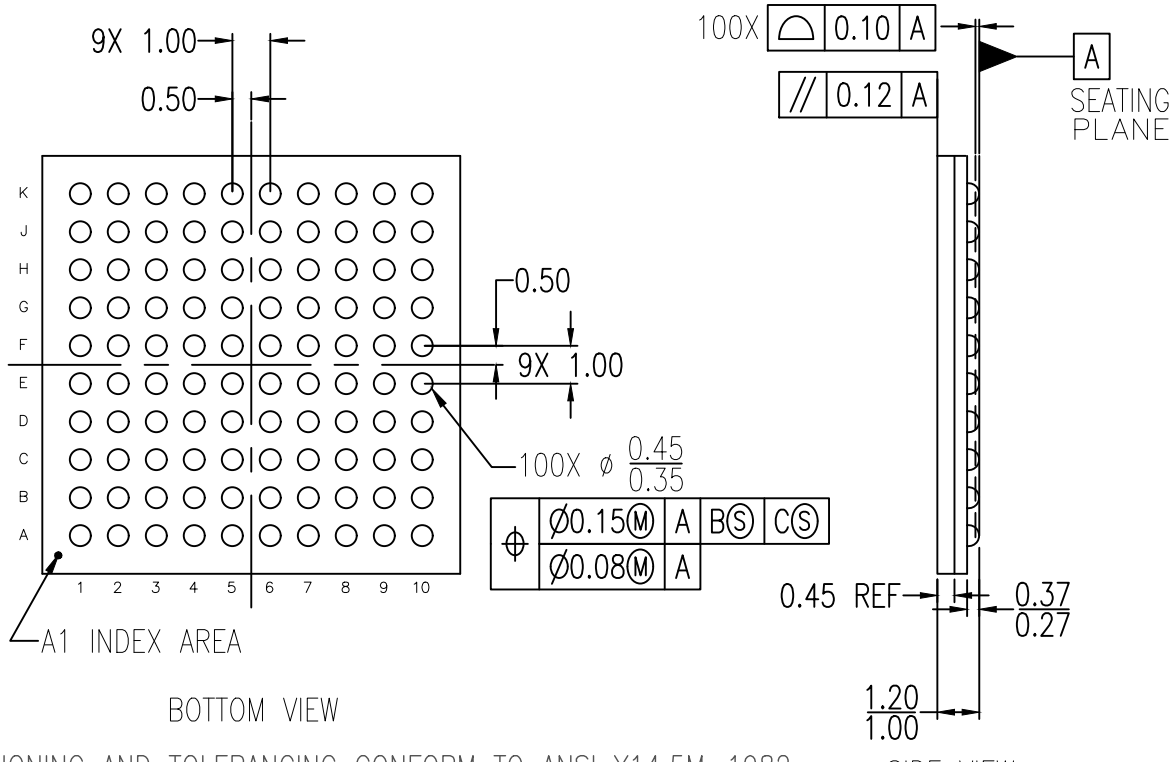


TOP VIEW

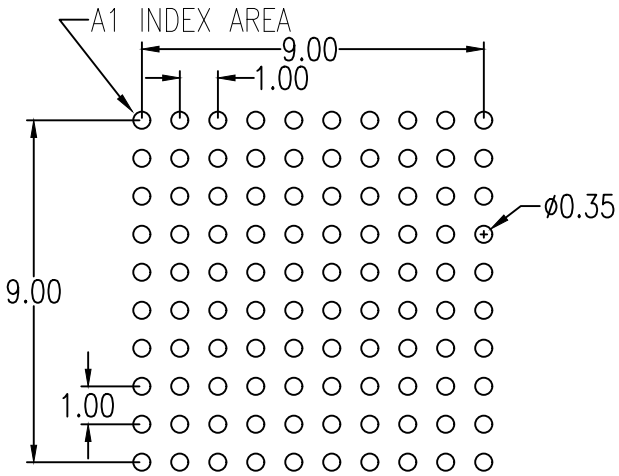


BOTTOM VIEW

SIDE VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSION ARE IN MILLIMETERS



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES
2. TOP DOWN VIEW ON PCB
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Oct 23, 2018	Rev 00	Initial Release

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