Programmable Timing Control Hub™ for P4™

Recommended Application:

CK-408 clock Intel® 845 with P4 processor.

Output Features:

- 3 Differential CPU Clock Pairs @ 3.3V
- 7 PCI (3.3V) @ 33.3MHz
- 3 PCI_F (3.3V) @ 33.3MHz
- 1 USB (3.3V) @ 48MHz
- 1 DOT (3.3V) @ 48MHz
- 1 REF (3.3V) @ 14.318MHz
- 5 3V66 (3.3V) @ 66.6MHz
- 1 VCH/3V66 (3.3V) @ 48MHz or 66.6MHz

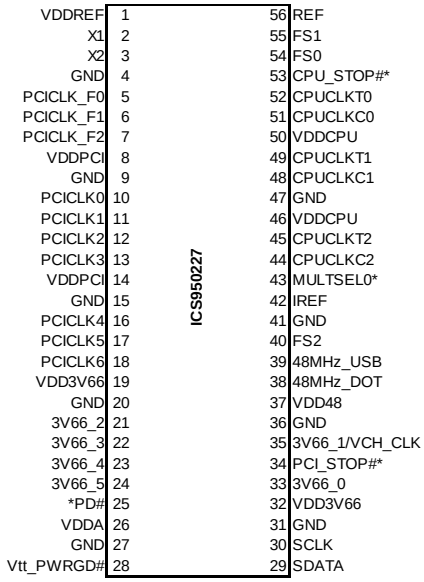
Features/Benefits:

- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I^2C Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.

Key Specifications:

- CPU Output Jitter <150ps
- 3V66 Output Jitter <250ps
- CPU Output Skew <100ps

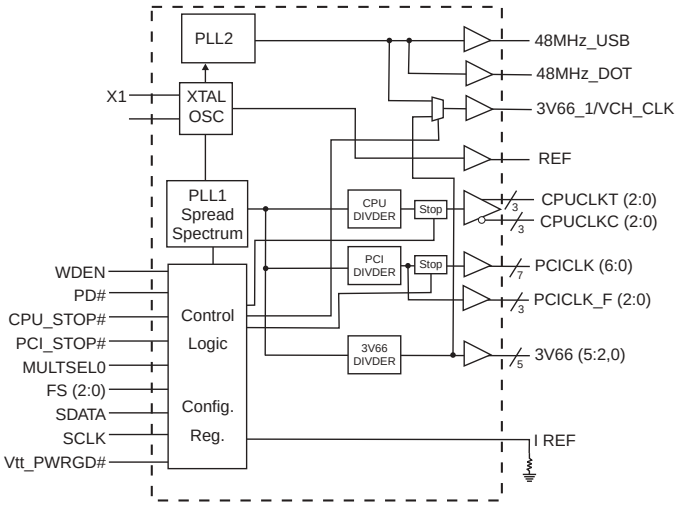
Pin Configuration



56-Pin 300-mil SSOP

* These inputs have 150K internal pull-up resistor to VDD.

Block Diagram



Frequency Table

FS2	FS1	FS0	CPU (MHz)	3V66 (MHz)	66Buff[2:0] 3V66[4:2] (MHz)	PCI_F PCI (MHz)
0	0	0	66.66	66.66	66.66	33.33
0	0	1	100.00	66.66	66.66	33.33
0	1	0	200.00	66.66	66.66	33.33
0	1	1	133.33	66.66	66.66	33.33
Mid	0	0	Tristate	Tristate	Tristate	Tristate
Mid	0	1	TCLK/2	TCLK/4	TCLK/4	TCLK/8
Mid	1	0	Reserved	Reserved	Reserved	Reserved
Mid	1	1	Reserved	Reserved	Reserved	Reserved

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Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 8, 14, 19, 26, 32, 37, 46, 50	VDD	PWR	3.3V power supply
2	X1	X2 Crystal Input	14.318MHz Crystal input
3	X2	X1 Crystal Output	14.318MHz Crystal output
7, 6, 5	PCICLK_F (2:0)	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
4, 9, 15, 20, 27, 31, 36, 41, 47	GND	PWR	Ground pins for 3.3V supply
18, 17, 16, 13, 12,11, 10	PCICLK (6:0)	OUT	PCI clock outputs
24, 23, 22, 21	3V66 (5:2)	OUT	66MHz reference clocks, from internal VCO
25	PD#	IN	Invokes power-down mode. Active Low.
28	Vtt_PWRGD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when FS(2:0) and MULTISEL0 inputs are valid and are ready to be sampled (active low)
29	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
30	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
33	3V66_0	OUT	66MHz reference clocks, from internal VCO
34	PCI_STOP#	IN	Halts PCICLK clocks at logic 0 level, when input low except PCICLK_F which are free running
35	3V66_1/VCH_CLK	OUT	3.3V output selectable through I^2C to be 66MHz from internal VCO or 48MHz (non-SSC)
38	48MHz_DOT	OUT	48MHz output clock for DOT
39	48MHz_USB	OUT	48MHz output clock for USB
40	FS2	IN	Special 3.3V input for Mode selection, cannot be logic 1
42	I REF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
43	MULTSEL0	IN	3.3V LVTTL input for selecting the current multiplier for CPU outputs
44, 48, 51	CPUCLKC (2:0)	OUT	"Complementory" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
45, 49, 52	CPUCLKT (2:0)	OUT	"True" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
53	CPU_STOP#	IN	Halts CPUCLK clocks at logic 0 level, when input low
55, 54	FS (1:0)	IN	Frequency select pins
56	REF	OUT	14.318MHz reference clock.

Power Groups

(Analog)

VDDA = Analog Core PLL1
VDDREF = REF, Xtal
VDD48 = 48MHz, PLL

(Digital)

VDDPCI
VDD3V66
VDDCPU

0641D—07/03/03

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Truth Table

FS2	FS1	FS0	CPU (MHz)	3V66 (5:0) (MHz)	PCI_F PCI (MHz)	REF0 (MHz)	USB/DOT (MHz)
0	0	0	66.66	66.66	33.33	14.318	48.00
0	0	1	100.00	66.66	33.33	14.318	48.00
0	1	0	200.00	66.66	33.33	14.318	48.00
0	1	1	133.33	66.66	33.33	14.318	48.00
Mid	0	0	Tristate	Tristate	Tristate	Tristate	Tristate
Mid	0	1	TCLK/2	TCLK/4	TCLK/8	TCLK	TCLK/2
Mid	1	0	Reserved	Reserved	Reserved	Reserved	Reserved
Mid	1	1	Reserved	Reserved	Reserved	Reserved	Reserved

Maximum Allowed Current

Condition	Max 3.3V supply consumption Max discrete cap loads, Vdd = 3.465V All static inputs = Vdd or GND
Powerdown Mode (PWRDWN# = 0)	40mA
Full Active	360mA

Host Swing Select Functions

MULTISEL0	Board Target Trace/Term Z	Reference R, Iref = V_{DD}/(3*Rr)	Output Current	Voh @ Z
1	50 ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6* I REF	0.7V @ 50

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General I²C serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	○		
	○		○
	○		○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address D3(H)			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			○
	○		○
	○		○
	○		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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I²C Table: Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SPREAD ENABLE	Frequency H/W IIC Select	RW	OFF	ON	0
Bit 6	-	CENTER/DOWNSPREAD SELECT	CENTER/DOWNSPREAD SELECT	RW	DOWN SPREAD	CENTER SPREAD	0
Bit 5	35	3V66/VCH SELECT	48MHz/66.66MHz SEL	RW	66.66MHz	48.00MHz	0
Bit 4	53	CPU_STOP#	CPU STOP Read Back	R	READBACK		X
Bit 3	34	PCI_STOP# HW/SW SELECT	Freq Select Bit 3	RW/R	PCI STOP	PCI RUNNING	1
Bit 2	40	FS2	Freq Select 2 Read Back	R	READBACK		X
Bit 1	55	FS1	Freq Select 1 Read Back	R			X
Bit 0	54	FS0	Freq Select 0 Read Back	R			X

I²C Table: Spreading and Device Behavior Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	43	MULTSEL0	MULTSEL0 READBACK	R	READBACK		X
Bit 6	-	WD ALARM	Watchdog Alarm Read Back	R	NO ALARM	ALARM SET	0
Bit 5	45, 44	CPU2/CPUC2	CPU FREE-RUN NING CONTROL	RW	STOPPABLE	FREE-RUN	0
Bit 4	49, 48	CPU1/CPUC1		RW	STOPPABLE	FREE-RUN	0
Bit 3	52, 51	CPU0/CPUC0		RW	STOPPABLE	FREE-RUN	0
Bit 2	45, 44	CPU2/CPUC2	Output Control	RW	Disable	Enable	1
Bit 1	49, 48	CPU1/CPUC1	Output Control	RW	Disable	Enable	1
Bit 0	52, 51	CPU0/CPUC0	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	18	PCICLK6	Output Control	RW	Disable	Enable	1
Bit 5	17	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 4	16	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 3	13	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 2	12	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 1	11	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 0	10	PCICLK0	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	38	48MHz_DOT	Output Control	RW	Disable	Enable	1
Bit 6	39	48MHz_USB	Output Control	RW	Disable	Enable	1
Bit 5	7	PCIF2	CPU FREE-RUN NING CONTROL	RW	FREE-RUN	STOPPABLE	0
Bit 4	6	PCIF1		RW	FREE-RUN	STOPPABLE	0
Bit 3	5	PCIF0		RW	FREE-RUN	STOPPABLE	0
Bit 2	7	PCICLK_F2	Output Control	RW	Disable	Enable	1
Bit 1	6	PCICLK_F1	Output Control	RW	Disable	Enable	1
Bit 0	5	PCICLK_F0	Output Control	RW	Disable	Enable	1

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I²C Table: Output Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RESERVED	RESERVED	-	-	-	0
Bit 6	-	RESERVED	RESERVED	`	-	-	0
Bit 5	33	3V66_0	Output Control	RW	Disable	Enable	1
Bit 4	35	3V66_1/VHC_CLK	Output Control	RW	Disable	Enable	1
Bit 3	24	3V66_5	Output Control	RW	Disable	Enable	1
Bit 2	23	3V66_4	Output Control	RW	Disable	Enable	1
Bit 1	22	3V66_3	Output Control	RW	Disable	Enable	1
Bit 0	21	3V66_2	Output Control	RW	Disable	Enable	1

I²C Table: Output Control and Fix Frequecy Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RESERVED	-	-	-	-	0
Bit 6	-	RESERVED	-	-	-	-	0
Bit 5	-	RESERVED	-	-	-	-	0
Bit 4	-	RESERVED	-	-	-	-	0
Bit 3	38	48MHz_DOT	DOT CLOCK EDGE RATE CONTROL	RW	00= MEDIUM (DEFAULT) 10= LOW 01= HIGH		0
Bit 2				RW			0
Bit 1	39	48MHz_USB	USB EDGE RATE CONTROL	RW	00= MEDIUM (DEFAULT) 01= LOW 10= HIGH		0
Bit 0				RW			0

I²C Table: Vendor & Revision ID Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	1
Bit 6	-	RID2		R	-	-	1
Bit 5	-	RID1		R	-	-	1
Bit 4	-	RID0		R	-	-	1
Bit 3	-	VID3	VENDOR ID	R	-	-	1
Bit 2	-	VID2		R	-	-	1
Bit 1	-	VID1		R	-	-	1
Bit 0	-	VID0		R	-	-	1

I²C Table: DEVICE ID

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-			R	-	-	0
Bit 6	-			R	-	-	0
Bit 5	-			R	-	-	0
Bit 4	-			R	-	-	0
Bit 3	-			R	-	-	0
Bit 2	-			R	-	-	0
Bit 1	-			R	-	-	0
Bit 0	-			R	-	-	1

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I²C Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	1
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

I²C Table: Watchdog Timer Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RESERVED	RESERVED	RW	-	-	0
Bit 6	-	RESERVED	RESERVED	RW	-	-	0
Bit 5	-	RESERVED	RESERVED	RW	-	-	0
Bit 4	-	WD4	These bits represent X*290ms the watchdog timer will wait before it goes to alarm mode. Default is10X 290ms =2.9seconds	RW	-	-	0
Bit 3	-	WD3		RW	-	-	1
Bit 2	-	WD2		RW	-	-	0
Bit 1	-	WD1		RW	-	-	1
Bit 0	-	WD0		RW	-	-	0

I²C Table: VCO Control Select Bit & WD Timer Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/NEN	M/N Programming Enable	RW	Latched Input	IIC Prog. B(11:17)	0
Bit 6	-	WDEN	Watchdog Enable	RW	OFF	ON	0
Bit 5	-	WDFSEN	WD Safe Frequency Mode	RW	Latched FS/Byte0	WD B10 b(4:0)	0
Bit 4	-	WD SS EN	Writing to these bit will configure the safe frequency configuration	RW	-	-	0
Bit 3	-	WD MultSEL		RW	-	-	0
Bit 2	-	WD FS2		RW	-	-	0
Bit 1	-	WD FS1		RW	-	-	0
Bit 0	-	WD FS0		RW	-	-	0

I²C Table: VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Bit 8	RW	-	-	X
Bit 6	-	M Div6	The decimal representation of M Div (6:0) is equal to reference divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 5	-	M Div5		RW	-	-	X
Bit 4	-	M Div4		RW	-	-	X
Bit 3	-	M Div3		RW	-	-	X
Bit 2	-	M Div2		RW	-	-	X
Bit 1	-	M Div1		RW	-	-	X
Bit 0	-	M Div0		RW	-	-	X

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I²C Table: VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	The decimal representation of N Div (8:0) is equal to VCO divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 6	-	N Div6		RW	-	-	X
Bit 5	-	N Div5		RW	-	-	X
Bit 4	-	N Div4		RW	-	-	X
Bit 3	-	N Div3		RW	-	-	X
Bit 2	-	N Div2		RW	-	-	X
Bit 1	-	N Div1		RW	-	-	X
Bit 0	-	N Div0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	These Spread Spectrum bits will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.	RW	-	-	X
Bit 6	-	SSP6		RW	-	-	X
Bit 5	-	SSP5		RW	-	-	X
Bit 4	-	SSP4		RW	-	-	X
Bit 3	-	SSP3		RW	-	-	X
Bit 2	-	SSP2		RW	-	-	X
Bit 1	-	SSP1		RW	-	-	X
Bit 0	-	SSP0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	SSP13	It is recommended to use ICS Spread % table for spread programming.	RW	-	-	X
Bit 4	-	SSP12		RW	-	-	X
Bit 3	-	SSP11		RW	-	-	X
Bit 2	-	SSP10		RW	-	-	X
Bit 1	-	SSP9		RW	-	-	X
Bit 0	-	SSP8		RW	-	-	X

I²C Table: Output Divider Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	CPU Div3	CPU divider ratio can be configured via these 4 bits individually.	RW	See Table 3: Divider Ratio Combination Table 2-3-5-7		X
Bit 2	-	CPU Div2		RW			X
Bit 1	-	CPU Div1		RW			X
Bit 0	-	CPU Div0		RW			X

I²C Table: Output Divider Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	3V66 Div3	3V66 divider ratio can be configured via these 4 bits individually.	RW	See Table 3: Divider Ratio Combination Table		X
Bit 2	-	3V66 Div2		RW			X
Bit 1	-	3V66 Div1		RW			X
Bit 0	-	3V66 Div0		RW			X

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I²C Table: Output Divider Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	CPUINV	CPU Phase Invert	RW	Default	Inverse	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Group Skew Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	CPUSkw1	CPUCLKT/C (2:0) Skew Control	RW	-	-	0
Bit 2	-	CPUSkw0		RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Group Skew Control Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	PCISkw3	PCI (6:1) AND PCIF(2:0) Skew Control	RW	16-Steps Skew Control. This byte will advance or delay the skew by 100ps per step		0
Bit 2	-	PCISkw2		RW			1
Bit 1	-	PCISkw1		RW			0
Bit 0	-	PCISkw0		RW			0

I²C Table: Slew Rate Control Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	3V66ISkw	3V66 (5:0) Skew Control	RW	Skew Control This byte will advance or delay the skew by 250 ps per step		0
Bit 6	-	3V66ISkw		RW			1
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	RESERVED	Reserved	-	-	-	0
Bit 2	-	RESERVED	Reserved	-	-	-	0
Bit 1	-	RESERVED	Reserved	-	-	-	0
Bit 0	-	RESERVED	Reserved	-	-	-	0

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I²C Table: Slew Rate Control Register

Byte 21	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCISlw	PCICLK_F2 Slew Rate Control	RW	10=STRONG 00= MEDIUM 01= WEAK		1
Bit 6	-			RW			0
Bit 5	-	PCISlw	PCICLK_F1:0 Slew Rate Control	RW	10=STRONG 00= MEDIUM 01= WEAK		1
Bit 4	-			RW			0
Bit 3	-	3V66SLW	3V66 (5:2) Slew Rate Control	RW	10=STRONG 00= MEDIUM 01= WEAK		1
Bit 2	-			RW			0
Bit 1	-	3V66SLW	3V66 (1:0) Slew Rate Control	RW	10=STRONG 00= MEDIUM 01= WEAK		1
Bit 0	-			RW			0

I²C Table: Slew Rate Control Register

Byte 22	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCISlw	REF Slew Rate Control	RW	10=STRONG 00= MEDIUM 01= WEAK		1
Bit 6	-			RW			0
Bit 5	-	PCISlw	PCICLK (6:4) Slew Rate Control	RW	10=STRONG 00= MEDIUM 01= WEAK		1
Bit 4	-			RW			0
Bit 3	-	PCISlw	PCICLK (3:1) Slew Rate Control	RW	10=STRONG 00= MEDIUM 01= WEAK		1
Bit 2	-			RW			0
Bit 1	-	PCISlw	PCICLK0 Slew Rate Control	RW	10=STRONG 00= MEDIUM 01= WEAK		1
Bit 0	-			RW			0

I²C Table: Slew Rate Control Register

Byte 23	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCISlw1	PCI (6:4) Slew Rate Control	RW	-	-	1
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	VCSLW	VCH Slew Rate Control	RW	10=STRONG 00= MEDIUM 01= WEAK		1
Bit 4	-			RW			0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

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Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Case Temperature . . . . . 115°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			
Operating Supply Current	$I_{DD3.3OP}$	C_L = Full load		283	360	mA
Powerdown Current	$I_{DD3.3PD}$	IREF=2.32 mA		23	25	mA
Input Frequency	F_i	V_{DD} = 3.3 V		14.32		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization[1,2]	T_{STAB}	From PowerUp or deassertion of PowerDown to 1st clock.			1.8	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns
	t_{PHZ},t_{PLZ}	Output disable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

[2]See timing diagrams for buffered and un-buffered timing requirements.

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Electrical Characteristics - CPU 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660	770	850	mV	1
Voltage Low	VLow		-150	5	150		1
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		756	1150	mV	1
Min Voltage	Vuds		-300	-7			1
Crossing Voltage (abs)	Vcross(abs)		250	350	550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		12	140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		5.4000	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T_{absmin}	200MHz nominal	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	332	700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175	344	700	ps	1
Rise Time Variation	d-t_r			30	125	ps	1
Fall Time Variation	d-t_f			30	125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45	49	55	%	1
Skew	t_{sk3}	V_T = 50%		8	100	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom		60	150	ps	1

[1]Guaranteed by design, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

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Electrical Characteristics - 3V66 [5:0]

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_O			66.66		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	V OH@MIN = 1.0 V,	-33	-110		
		$V_{OH@MAX}$ = 3.135 V		-20	-33	mA
Output Low Current	I_{OL}[1]	VOL @MIN = 1.95 V,	30	110		
		$V_{OL@MAX}$ = 0.4 V		37	38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.8	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.3	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51.2	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		136	250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 3V66		241	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_O			33.33		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4	3.28		V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA		0.08	0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V,	-33	-110		
		$V_{OH@MAX}$ = 3.135 V		-20	-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V,	30	110		
		$V_{OL@MAX}$ = 0.4 V		37	38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.51	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.32	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51.1	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		101	500	ps
Jitter,cycle to cyc	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		226	250	ps

[1]Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - VCH, 48MHz DOT, 48MHz, USB

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_O			48.008		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4	3.27		V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	V OH@MIN = 1.0 V,	-29	-61		
		$V_{OH@MAX}$ = 3.135 V		-12	-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
48DOT Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	0.84	1	ns
48DOT Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	0.92	1	ns
VCH 48 USB Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.74	2	ns
VCH 48 USB Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.84	2	ns
48 DOT Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	53.2	55	%
VCH 48 USB Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	52.5	55	%
48 DOT Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		151	350	ps
USB to DOT Skew	t_{sk1}[1]	V_T = 1.5 V (0 OR 180 degrees)		0.53	1	ns
VCH Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		187	350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

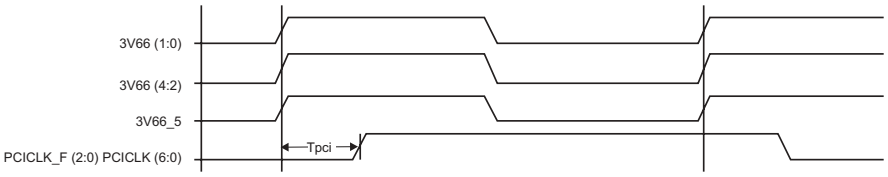
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			14.318		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4	3.28		V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	V OH@MIN = 1.0 V	-33	-110		
		$V_{OH@MAX}$ = 3.135 V		-20	-33	mA
Output Low Current	I_{OL}[1]	VOL @MIN = 1.95 V	30	110		
		$V_{OL@MAX}$ = 0.4 V		37	38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.38	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.31	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	54.7	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		276	1000	ps

[1]Guaranteed by design, not 100% tested in production.

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3V66 & PCI Phase Relationship

All 3V66 clocks are to be in pphase with each other. In the case where 3V66_1 is configured as 48MHz VCH clock, there is no defined phase relationship between 3V66_1/VCH and other 3V66 clocks. The PCI group should lag 3V66 by the standard skew described below as Tpci.



Group Skews at Common Transition Edges

GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3V66	3V66	3V66 (5:0) pin to pin skew	0	136	250	ps
PCI	PCI	PCI_F (2:0) and PCI (6:0) pin to pin skew	0	101	500	ps
3V66 to PCI	$S_{3V66-PCI}$	3V66 (5:0) leads 33MHz PCI	1.5	2.08	3.5	ns

[1]Guarenteed by design, not 100% tested in production.

PD# Functionality

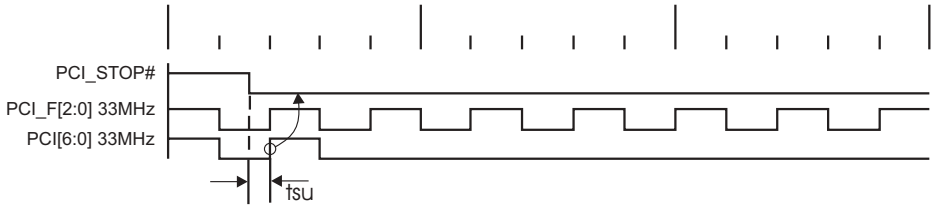
CPU_STOP#	CPUT	CPUC	3V66	66MHz_OUT	PCICLK_F PCICLK	PCICLK	USB/DOT 48MHz
1	Normal	Normal	66MHz	66MHz_IN	66MHz_IN	66MHz_IN	48MHz
0	iref * Mult	Float	Low	Low	Low	Low	Low

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PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCI[6:0] and stoppable PCI_F[2,0] clocks will latch low in their next high to low transition. The PCI_STOP# setup time tsu is 10 ns, for transitions to be recognized by the next rising edge.

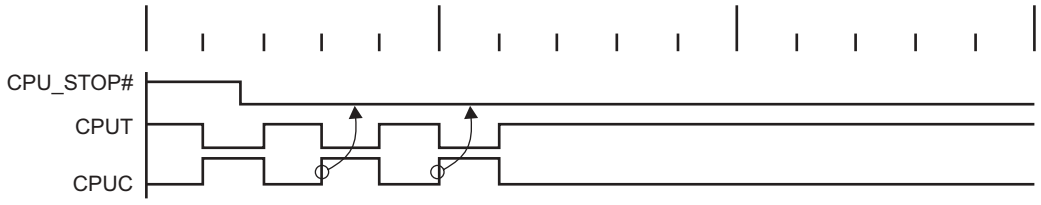
Assertion of PCI_STOP# Waveforms



CPU_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the CPU_STOP# pin is all CPU outputs that are set in the I^2C configuration to be stoppable via assertion of CPU_STOP# are to be stopped after their next transition following the two CPU clock edge sampling as shown. The final state of the stopped CPU signals is CPUT=High and CPUC=Low. There is to be no change to the output drive current values. The CPUT will be driven high with a current value equal to (MULTSEL0) X (I REF), the CPUC signal will not be driven.

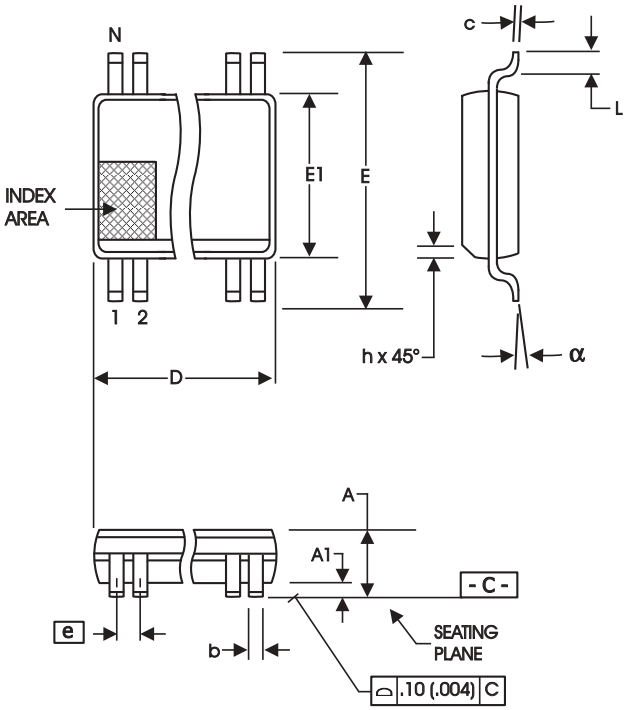
Assertion of CPU_STOP# Waveforms



CPU_STOP# Functionality

CPU_STOP#	CPUT	CPUC
1	Normal	Normal
0	iref * Mult	Float

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300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS950227yFT

Example:

ICS XXXXXX y F - T

- **Designation for tape and reel packaging**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0641D—07/03/03

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