PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES SEPTEMBER 7, 2016

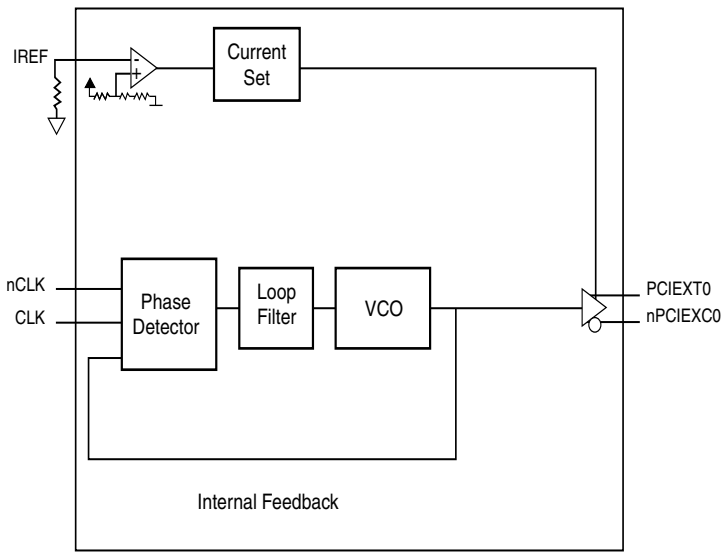
General Description

The 9DB202-01 is a high performance 1-to-1 Differential-to HCSL Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuating device may be necessary in order to reduce high frequency random and deterministic jitter com-ponents from the PLL synthesizer and from the system board.

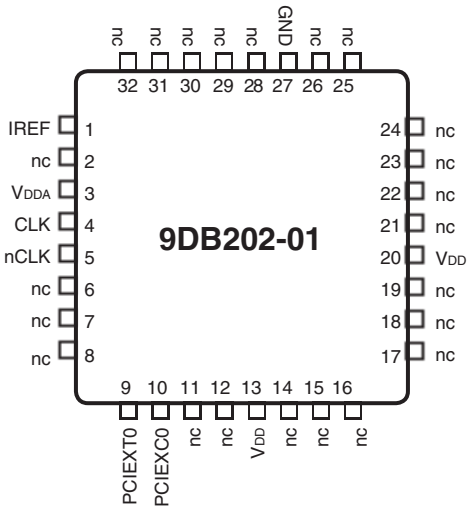
Features

- One 0.7V current mode differential HCSL output pair
- One differential clock input
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 140MHz
- Input frequency range: 90MHz - 140MHz
- VCO range: 450MHz - 700MHz
- Cycle-to-cycle jitter: 30ps (maximum)
- RMS phase jitter @ 100MHz, (1.5MHz - 22MHz): 2.31ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free RoHS compliant package
- Industrial temperature information available upon request
- For functional replacement use 8714004

Block Diagram



Pin Assignment



32-Lead VFQFN
5mm x 5mm x 0.925 package body
K Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	IREF	Input		A fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode PCIEX clock outputs.
2, 6, 7, 8, 11, 12, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 28, 29, 30, 31, 32	nc	Unused		No connect.
3	V_{DDA}	Power		Analog supply pin. Requires 24Ω series resistor.
4	CLK	Input	Pulldown	Non-inverting differential clock input.
5	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
9, 10	PCIEXT0, PCIEXC0	Output		Differential output pairs. HCSL interface levels.
13, 20	V_{DD}	Power		Core supply pins.
27	GND	Power		Power supply ground.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	34.8°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, TA = 0°C to 70°C, RREF = 475Ω

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				112	mA
I_{DDA}	Analog Supply Current				22	mA

Table 3B. Differential DC Characteristics, V_{DD} = 3.3V±5%, TA = 0°C to 70°C, RREF = 475Ω

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK, nCLK	V_{DD} = 3.465V, V_{IN} = 0V			150	µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

Table 3C. HCSL DC Characteristics, V_{DD} = 3.3V±5%, TA = 0°C to 70°C, RREF = 475Ω

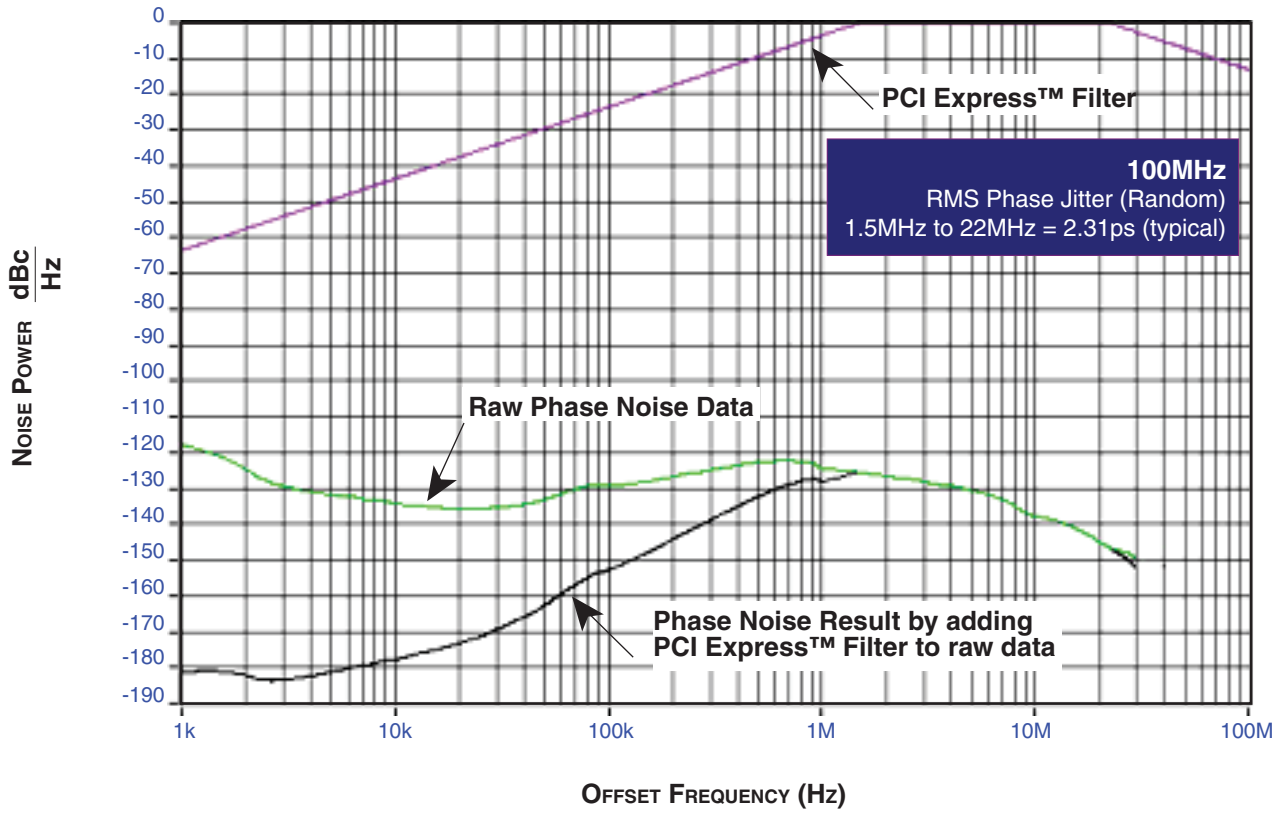
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{OH}	Output Current		12	14	16	mA
V_{OH}	Output High Voltage		610		780	mV
V_{OL}	Output Low Voltage				-5	mV
I_{OZ}	High Impedance Leakage Current		-10		10	µA
V_{OX}	Output Crossover Voltage		250		550	mV

Table 4. AC Characteristics, V_{DD} = 3.3V±5%, TA = 0°C to 70°C, RREF = 475Ω

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				140	MHz
$t_{jit(Ø)}$	RMS Phase Jitter (Random); NOTE 1	Integration Range: 1.5MHz - 22MHz		2.31		ps
$t_{jit(cc)}$	Cycle-to-Cycle Jitter				30	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to the Phase Noise Plot following this section.

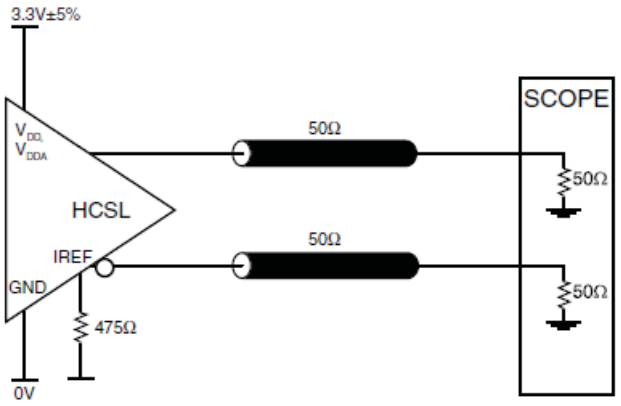
Typical Phase Noise at 100MHz



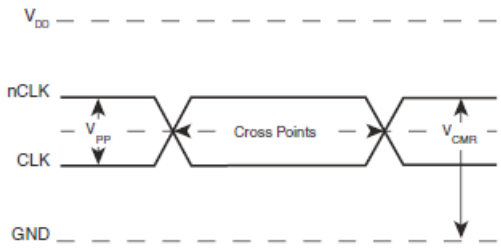
The illustrated phase noise plot was taken using a low phase noise signal generator, the noise floor of the signal generator is less than that of the device under test.

Using this configuration allows one to see the true spectral purity or phase noise performance of the PLL in the device under test. Due to the tracking ability of a PLL, it will track the input signal up to its loop bandwidth. Therefore, if the input phase noise is greater than that of the PLL, it will increase the output phase noise performance of the device. It is recommended that the phase noise performance of the input is verified in order to achieve the above phase noise performance.

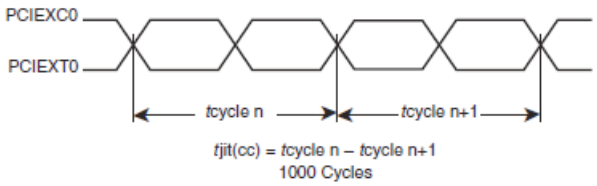
Parameter Measurement Information



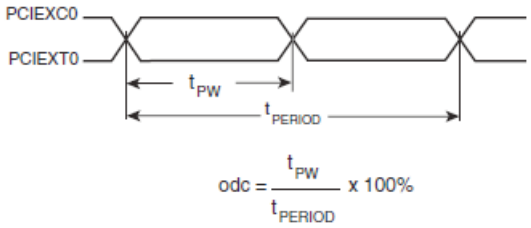
3.3V HCSL Output Load AC Test Circuit



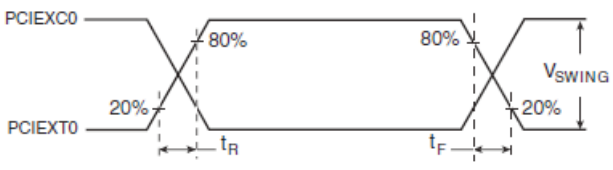
Differential Input Level



Cycle-to-Cycle Jitter



Output Duty Cycle/Pulse Width/Period



HCSL Output Rise/Fall Time

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 9DB202-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 24Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

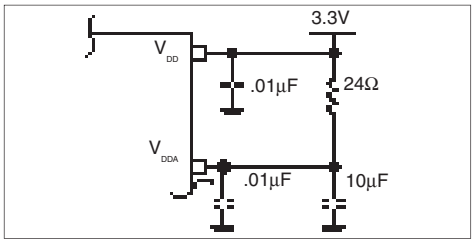


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

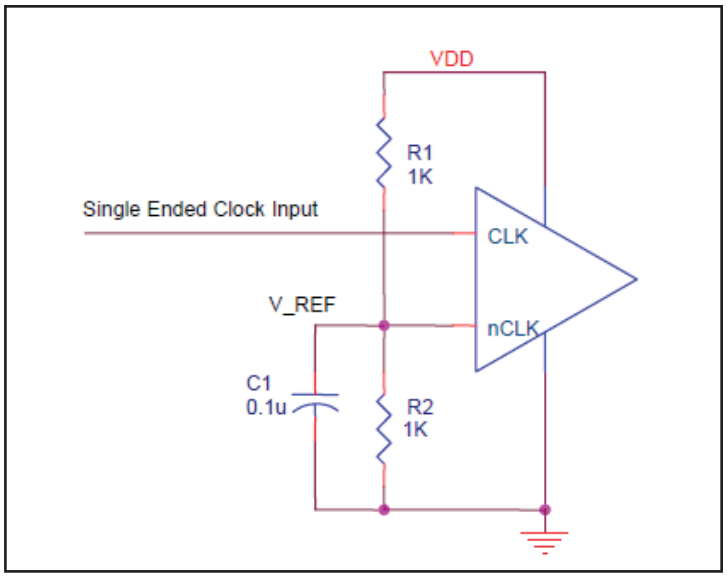


Figure 2. Single Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. Figures *4A to 4F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 4A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

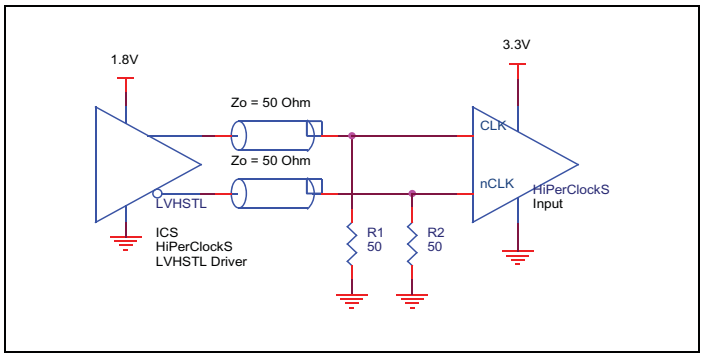


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

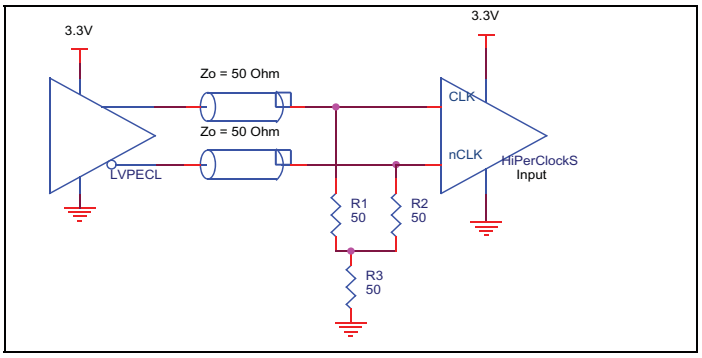


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

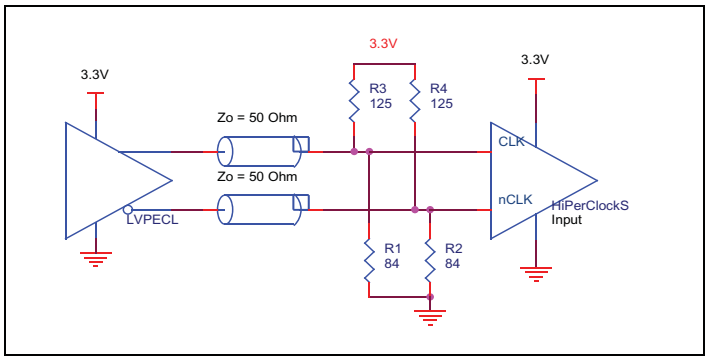


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

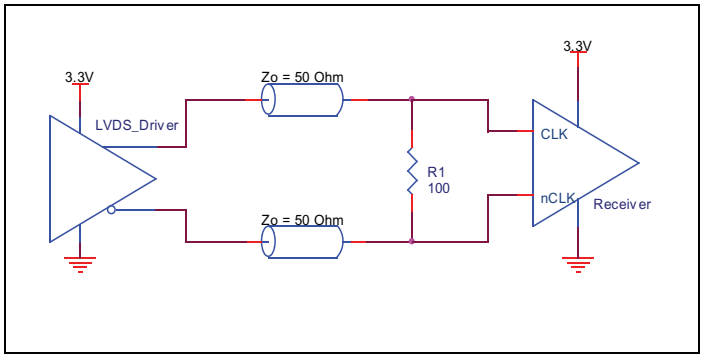


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

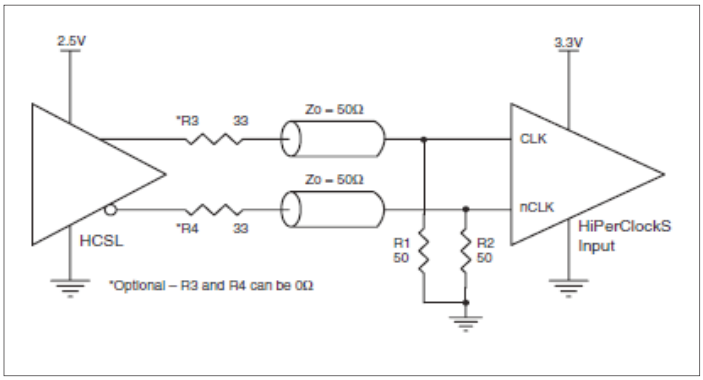


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

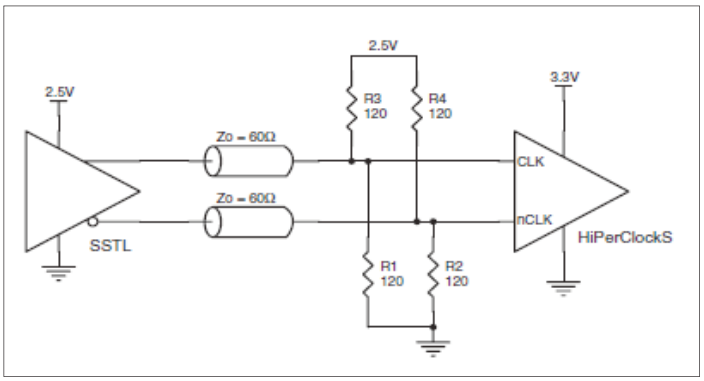


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

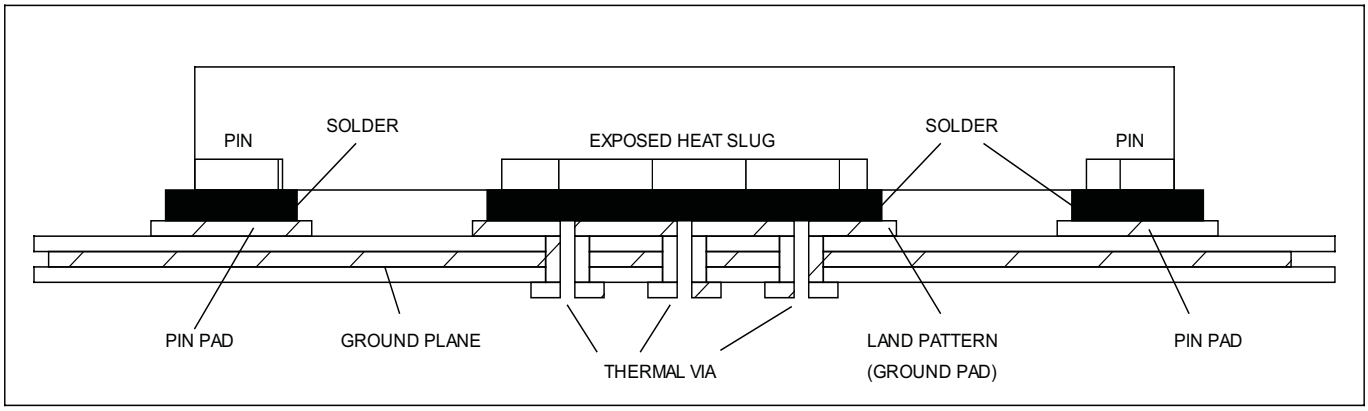


Figure 4. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

Schematic Example

The schematic below illustrates two different terminations. Both are reliable and adequate. The PCI Express termination is recommended for all PCI Express application. The optional termination, which has a slightly better signal integrity, is recommended for all other applications.

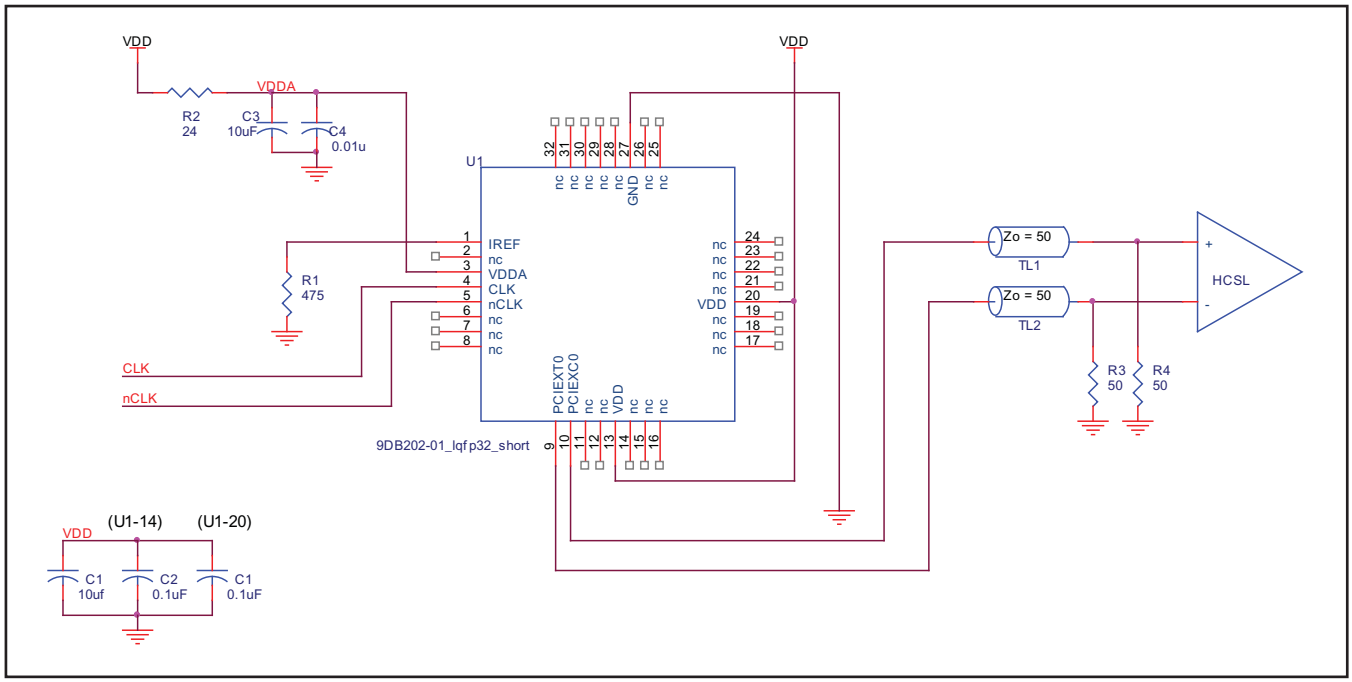


Figure 5. Example of 9DB202-01

Recommended Termination

Figure 6A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ω impedance.

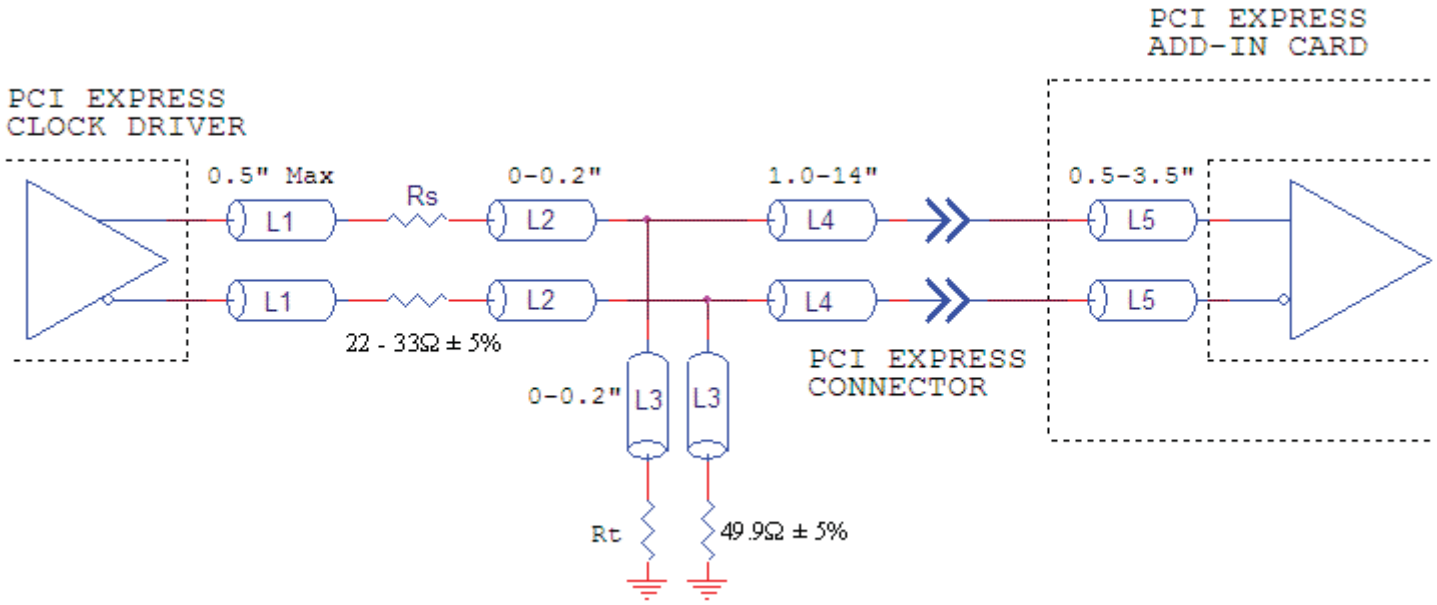


Figure 6A. Recommended Termination

Figure 6B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ω impedance.

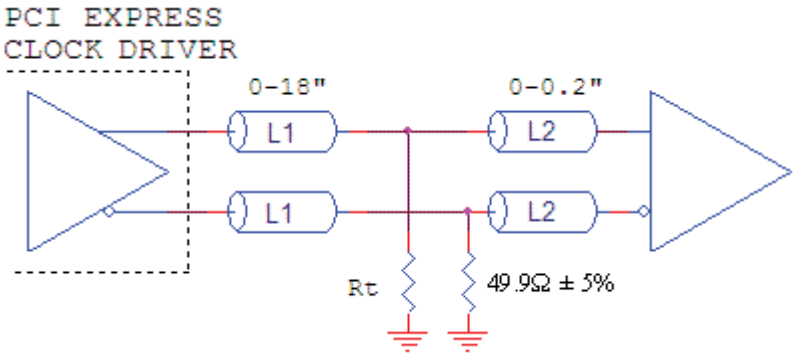


Figure 6B. Recommended Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the 9DB202-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 9DB202-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX})= 3.465V * (112mA + 22mA) = **464.3mW**
- Power (outputs)$_{MAX}$ = **44.5mW/Loaded Output pair**
  Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 464.3mW + 44.5mW = **508.81mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in Section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 34.8°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.509W * 34.8°C/W = 87.7°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 5. Thermal Resistance θ_{JA} for 32-Pin VFQFN, Forced Convection

θ_{JA} 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	34.8C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 7.*

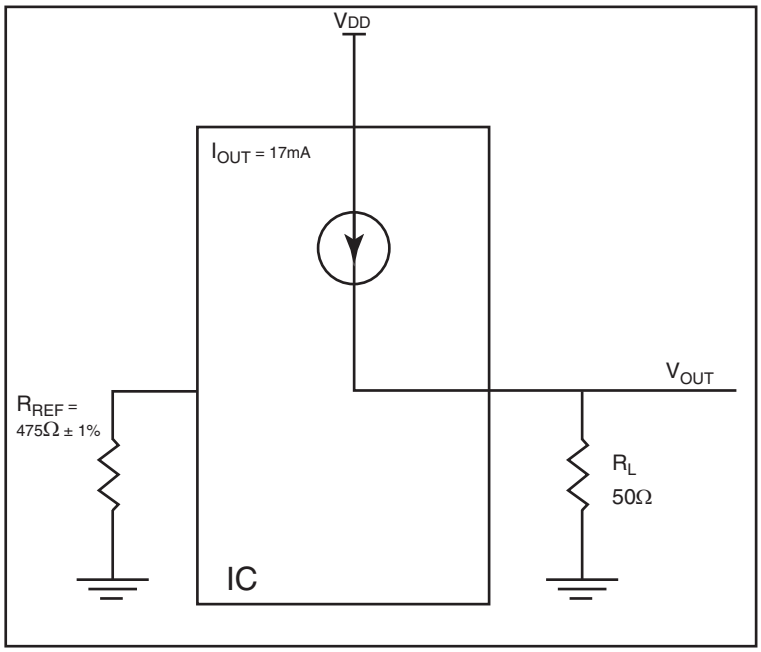


FIGURE 7. HCSL DRIVER CIRCUIT AND TERMINATION

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD_MAX}.

Power $= (V_{DD\_MAX} - V_{OUT}) * I_{OUT}$

since $V_{OUT} = I_{OUT} * R_L$

Power $= (V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$

$= (3.465V - 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

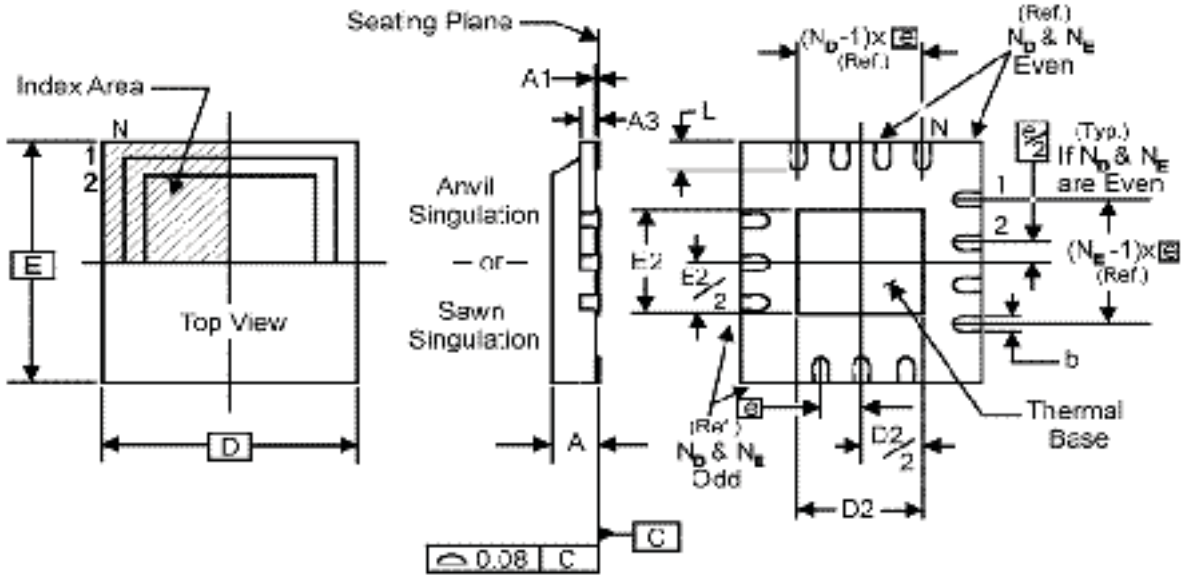
Table 7. θ_{JA} vs. Air Flow Table For 32 Lead VFQFN Package

θ_{JA} 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	34.8C/W

Transistor Count

The transistor count for 9DB202-01 is: 2471

Package Outline - K Suffix for 32 Lead VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	32	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	8	
N_E	8	
D	5.0	
D2	3.0	3.3
E	5.0	
E2	3.0	3.3
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
9DB202CK-01LF	ICS9DB202CK-01L	32 Lead “Lead-Free” VFQFN	Tray	0°C to 70°C
9DB202CK-01LFT	ICS9DB202CK-01L	32 Lead “Lead-Free” VFQFN	Tape & Reel	0°C to 70°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T3C	3	HCSL Table -adjusted V_{OH} min from 680mV to 610mV and added V_{OH} max.	12/21/04
B		1	Features Section - added Input Frequency Range and VCO Range bullets.	7/14/06
B	T3B T4 T9	3 3 5 6 8 10 11 - 12 15	Differential DC Characteristics Table - updated NOTES 1 and 2. AC Characteristics Table - added thermal note. Updated HCSL Output Load Test Circuit Diagram. Updated Power Supply Filtering Techniques from 10ohms to 24ohms. Added VFQFN EPAD Thermal Release Path section. Added HCSL Termination section. Added Power Considerations. Ordering Information Table - Deleted “ICS” prefix from Order/Part number.	2/18/09
B	T9	15	Ordering Information - removed leaded devices. Updated data sheet format.	7/22/15
B	T9	15	Ordering Information - Deleted LF note below table. Updated header and footer..	2/10/16
B		1	Product Discontinuation Notice - Last time buy expires September 7, 2016. PDN N-16-02.	3/11/16

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.