

**PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES SEPTEMBER 7, 2016**

## GENERAL DESCRIPTION

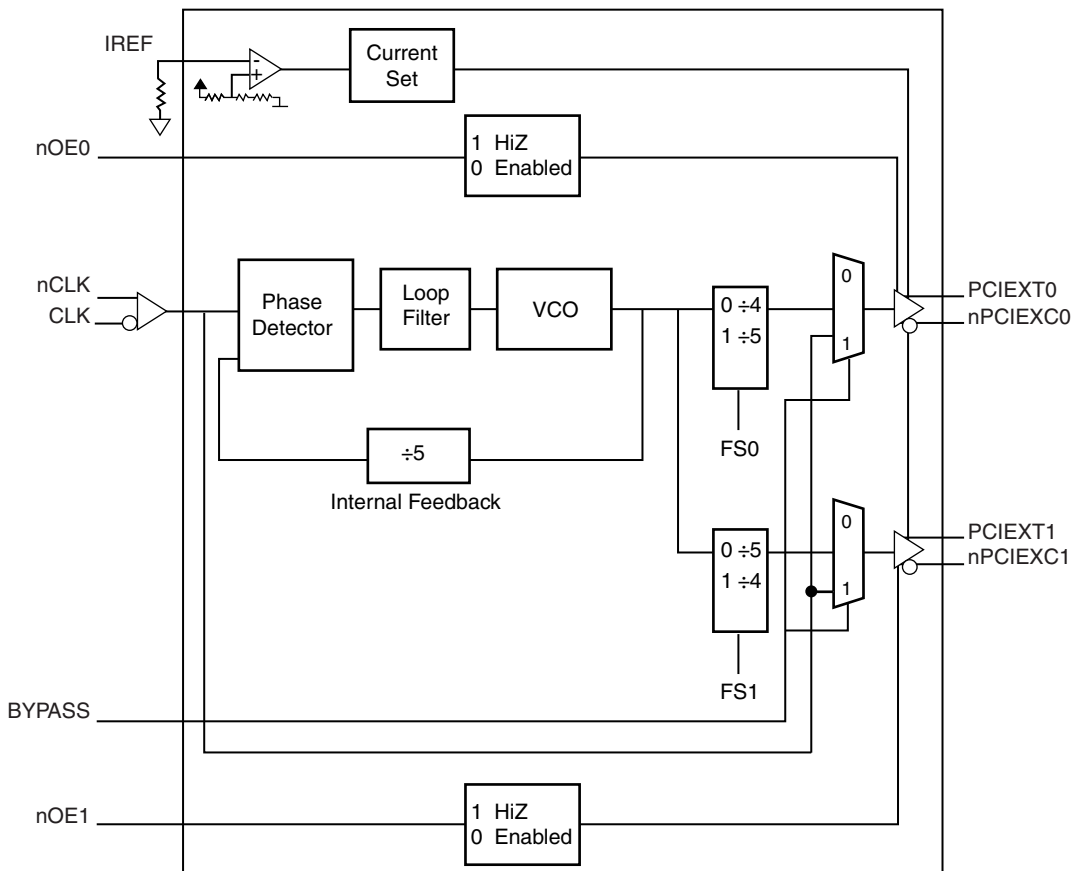
The 9DB202 is a high performance 1-to-2 Differential-to-HCSL Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express™ systems, such as those found in desktop PCs, the PCI Express™ clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter-attenuating device may be necessary in order to reduce high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The 9DB202 has two PLL bandwidth modes. In low bandwidth mode, the PLL loop bandwidth is 500kHz. This setting offers the best jitter attenuation and is still high enough to pass a triangular input spread spectrum profile. In high bandwidth mode, the PLL bandwidth is at 1MHz and allows the PLL to pass more spread spectrum modulation.

For serdes which have x10 reference multipliers instead of x12.5 multipliers, each of the two PCI Express™ outputs (PCIEX0:1) can be set for 125MHz instead of 100MHz by configuring the appropriate frequency select pins (FS0:1).

## FEATURES

- Two 0.7V current mode differential HCSL output pairs
- One differential clock input
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 140MHz
- Input frequency range: 90MHz - 140MHz
- VCO range: 450MHz - 700MHz
- Output skew: 110ps (maximum)
- Cycle-to-cycle jitter: 110ps (maximum)
- RMS phase jitter @ 100MHz, (1.5MHz - 22MHz): 2.42ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free RoHS compliant package
- Industrial temperature information available upon request
- For functional replacement use 8714004

## BLOCK DIAGRAM



## PIN ASSIGNMENT

PLL_BW	1	20	VDDA
CLK	2	19	BYPASS
nCLK	3	18	IREF
FS0	4	17	FS1
VDD	5	16	VDD
GND	6	15	GND
PCIEXT0	7	14	PCIEXT1
PCIEXC0	8	13	PCIEXC1
VDD	9	12	VDD
nOE0	10	11	nOE1

### 9DB202

#### 20-Lead TSSOP

6.50mm x 4.40mm x 0.92  
package body  
**G Package**  
Top View

### 9DB202

#### 20-Lead, 209-MIL SSOP

5.30mm x 7.20mm x 1.75mm  
body package  
**F Package**  
Top View

**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type	Description
1	PLL_BW	Input Pullup	Selects PLL Bandwidth input. LVCMOS/LVTTL interface levels.
2	CLK	Input Pulldown	Non-inverting differential clock input.
3	nCLK	Input Pullup/Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
4	FS0	Input Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
5, 9, 12, 16	$V_{DD}$	Power	Core supply pins.
6, 15	GND	Power	Power supply ground.
7, 8	PCIEXT0, PCIEXC0	Output	Differential output pairs. HCSL interface levels.
10, 11	nOE0, nOE1	Input Pulldown	Output enable. When HIGH, forces outputs to HiZ state. When LOW, enables outputs. LVCMOS/LVTTL interface levels.
13, 14	PCIEXC1, PCIEXT1	Output	Differential output pairs. HCSL interface levels.
17	FS1	Input Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
18	IREF	Input	A fixed precision resistor (475 $\Omega$ ) from this pin to ground provides a reference current used for differential current-mode PCIEX clock outputs.
19	BYPASS	Power Pulldown	BYPASS pin. When HIGH, bypass mode, when LOW, PLL mode. LVCMOS/LVTTL interface levels.
20	$V_{DDA}$	Power	Analog supply pin. Requires 24 $\Omega$ series resistor.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance			4		pF
$R_{PULLUP}$	Input Pullup Resistor			51		k $\Omega$
$R_{PULLDOWN}$	Input Pulldown Resistor			51		k $\Omega$

**TABLE 3A. RATIO OF OUTPUT FREQUENCY TO INPUT FREQUENCY FUNCTION TABLE, FS0**

Inputs	Outputs
FS0	PCIEX0
0	5/4
1	1

**TABLE 3B. RATIO OF OUTPUT FREQUENCY TO INPUT FREQUENCY FUNCTION TABLE, FS1**

Inputs	Outputs
FS1	PCIEX1
0	1
1	5/4

**TABLE 3C. BYPASS TABLE**

Inputs	Mode
BYPASS	
0	PLL Mode
1	Bypass Mode (output = inputs)

**TABLE 3D. OUTPUT ENABLE FUNCTION TABLE, nOE0**

Inputs	Outputs
nOE0	PCIEX0
0	Enabled
1	HiZ

**TABLE 3E. OUTPUT ENABLE FUNCTION TABLE, nOE1**

Inputs	Outputs
nOE1	PCIEX1
0	Enabled
1	HiZ

**TABLE 3F. PLL BANDWIDTH TABLE**

Inputs	Bandwidth
PLL_BW	
0	500kHz
1	1MHz

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	
20 Lead TSSOP	73.2°C/W (0 lfpm)
20 Lead SSOP	80.8°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$ ,  $R_{REF} = 475\Omega$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				112	mA
$I_{DDA}$	Analog Supply Current				22	mA

**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	mV
$V_{IL}$	Input Low Voltage		-0.3		0.8	mV
$I_{IH}$	Input High Current	BYPASS, nOE0, nOE1, FS1	$V_{DD} = V_{IN} = 3.465V$		150	$\mu\text{A}$
		FS0, PLL_BW			5	
$I_{IL}$	Input Low Current	BYPASS, nOE0, nOE1, FS1	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu\text{A}$
		FS0, PLL_BW		-150		

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$ ,  $R_{REF} = 475\Omega$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK, nCLK	$V_{DD} = V_{IN} = 3.465V$		150	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK, nCLK	$V_{DD} = 3.465V, V_{IN} = 0V$		150	$\mu\text{A}$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is  $V_{DD} + 0.3V$ .

**TABLE 4D. HCSL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$ ,  $R_{REF} = 475\Omega$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{OH}$	Output Current		12	14	16	mA
$V_{OH}$	Output High Voltage		610		780	mV
$V_{OL}$	Output Low Voltage				65	mV
$I_{OZ}$	High Impedance Leakage Current		-10		10	$\mu A$
$V_{OX}$	Output Crossover Voltage		250		550	mV

**TABLE 5. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$ ,  $R_{REF} = 475\Omega$** 

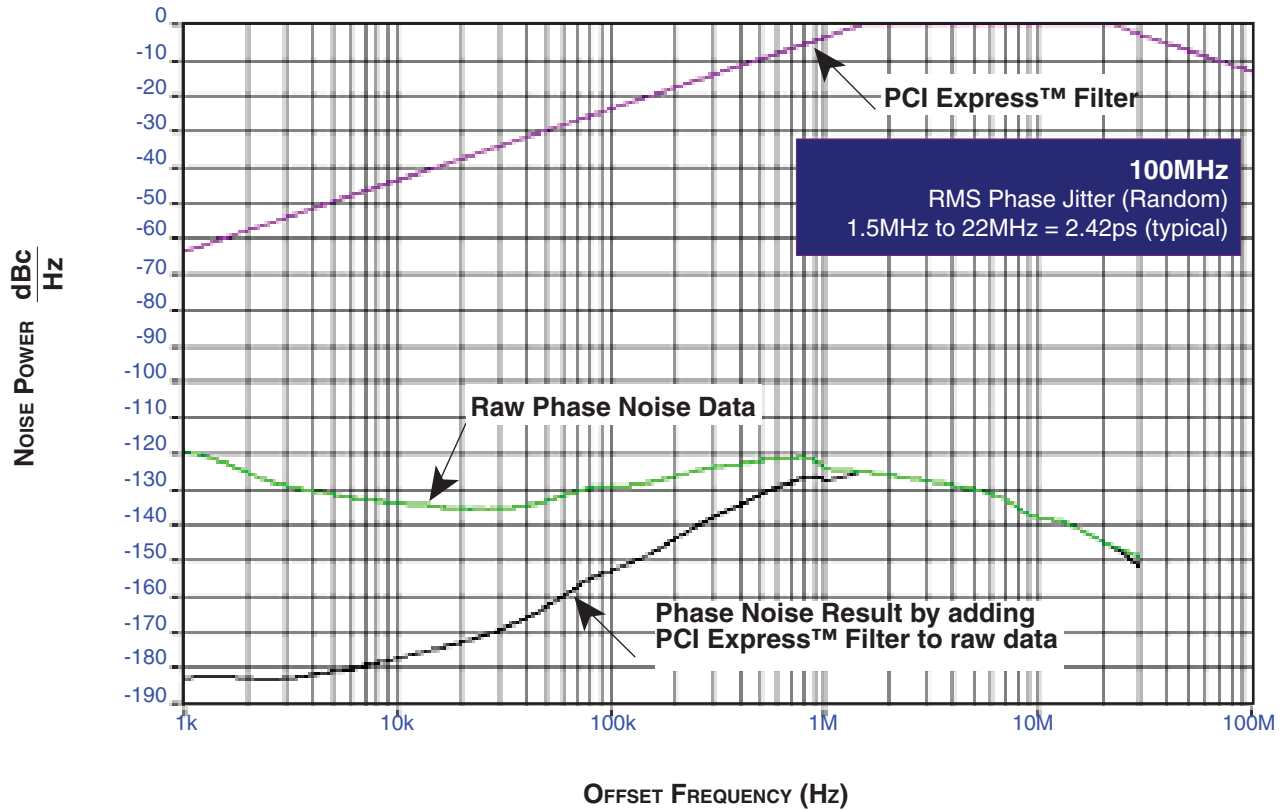
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				140	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 2			50	110	ps
$t_{jit(cc)}$	Cycle-to-Cycle Jitter	Outputs @ Different Frequencies			110	ps
		Outputs @ Same Frequencies			50	ps
$t_{jit(\phi)}$	RMS Phase Jitter (Random); NOTE 3	Integration Range: 1.5MHz - 22MHz		2.42		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	300		1100	ps
$t_{odc}$	Output Duty Cycle		48		52	%

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plot following this section.

## TYPICAL PHASE NOISE AT 100MHz

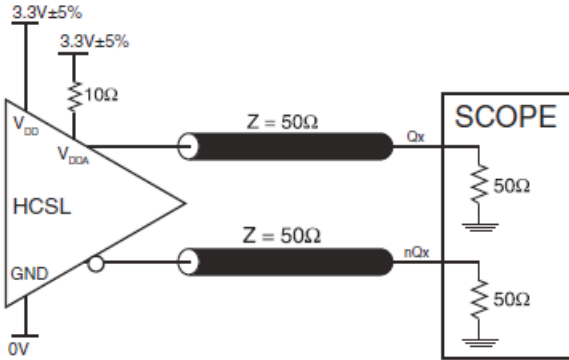


The illustrated phase noise plot was taken using a low phase noise signal generator, the noise floor of the signal generator is less than that of the device under test.

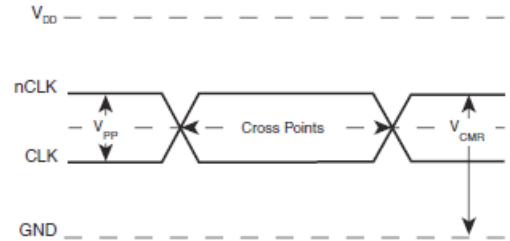
Using this configuration allows one to see the true spectral purity or phase noise performance of the PLL in the device under test. Due

to the tracking ability of a PLL, it will track the input signal up to its loop bandwidth. Therefore, if the input phase noise is greater than that of the PLL, it will increase the output phase noise performance of the device. It is recommended that the phase noise performance of the input is verified in order to achieve the above phase noise performance.

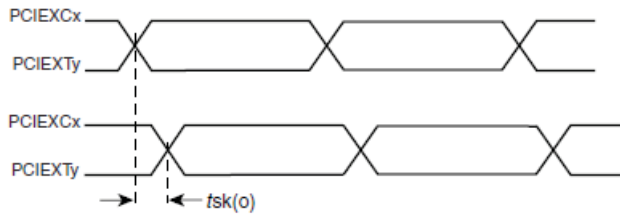
## PARAMETER MEASUREMENT INFORMATION



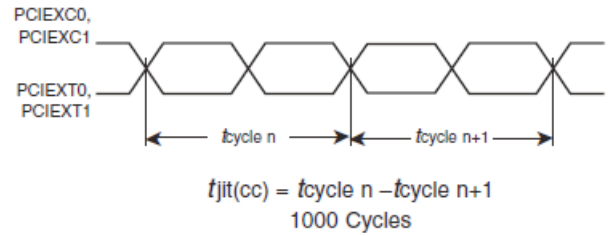
3.3V HCSL OUTPUT LOAD AC TEST CIRCUIT



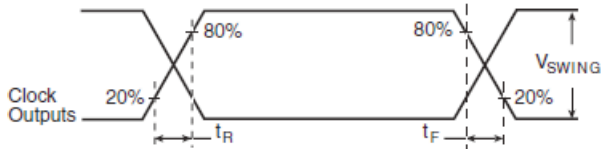
DIFFERENTIAL INPUT LEVEL



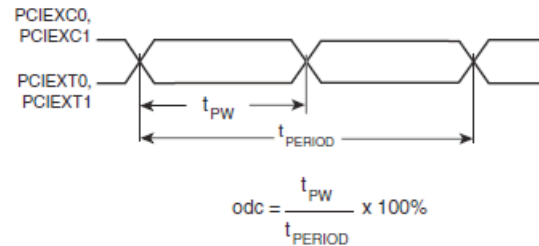
OUTPUT SKEW



CYCLE-TO-CYCLE JITTER



HCSL OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 9DB202 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$  and  $V_{DDA}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $24\Omega$  resistor along with a  $10\mu F$  and a  $.01\mu F$  bypass capacitor should be connected to each  $V_{DDA}$  pin. The  $10\Omega$  resistor can also be replaced by a ferrite bead.

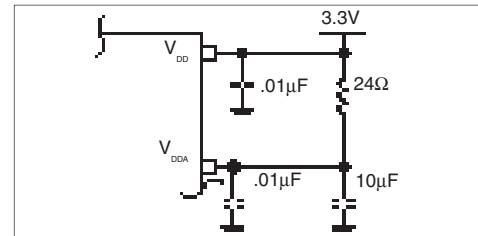


FIGURE 1. POWER SUPPLY FILTERING

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

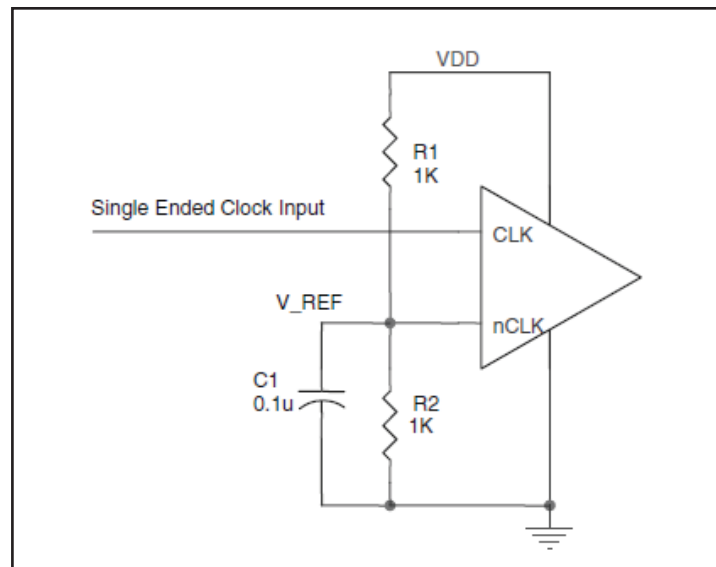
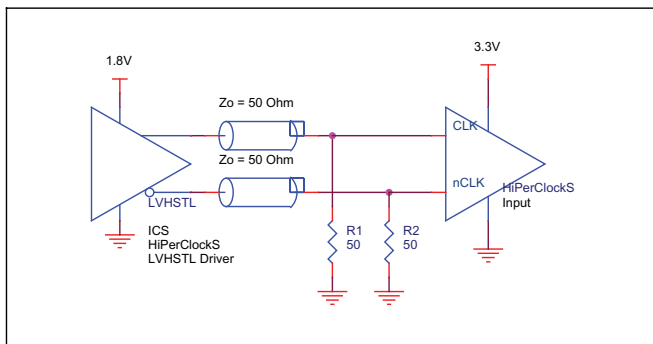


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

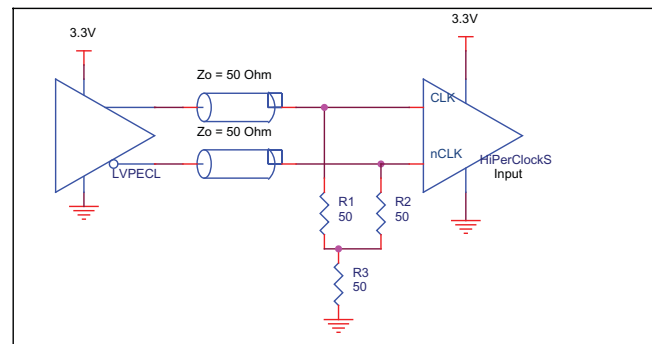
## DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

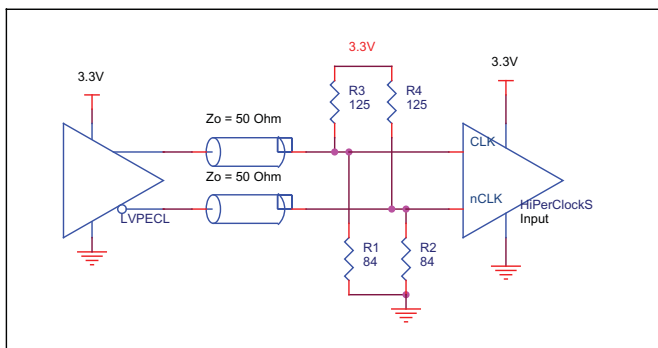
Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



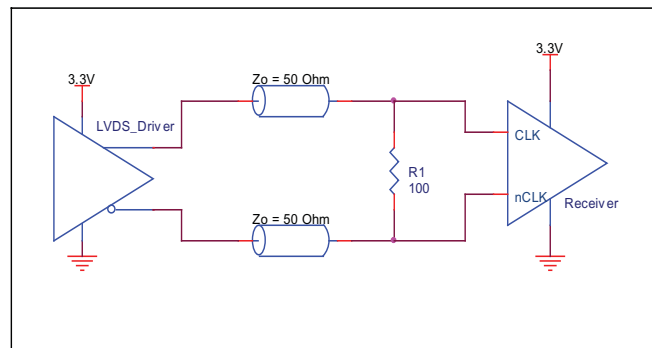
**FIGURE 3A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER**



**FIGURE 3B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**

## RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

### INPUTS:

#### LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

### OUTPUTS:

#### HCSL OUTPUT

All unused HCSL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.



# RELIABILITY INFORMATION

**TABLE 6A.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 20 LEAD TSSOP PACKAGE**

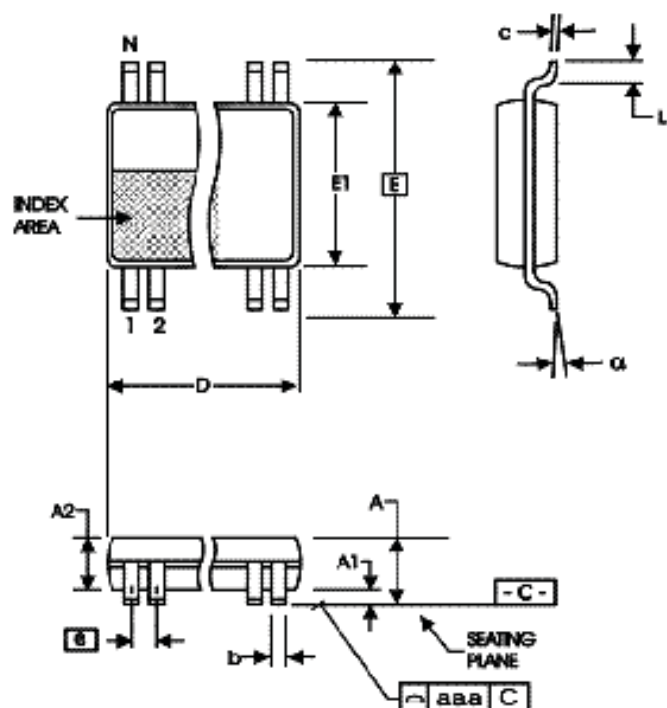
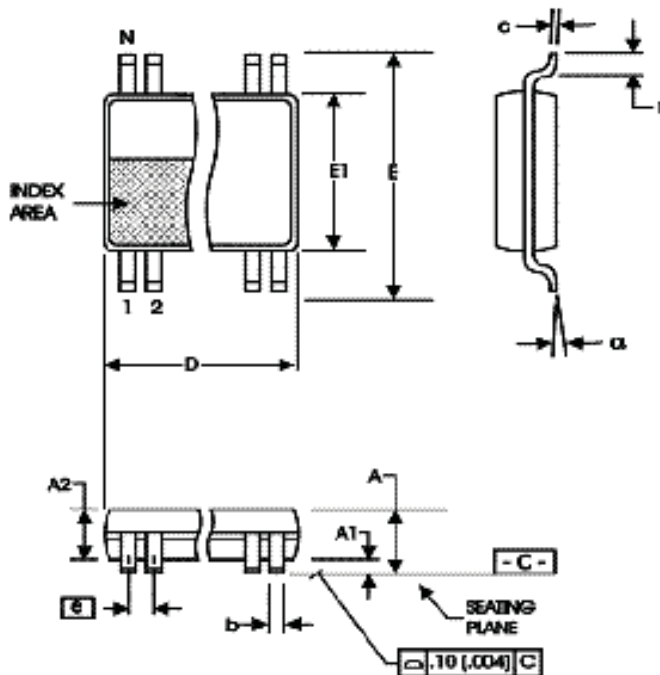
$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98°C/W	88°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W
<b>NOTE:</b> Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

**TABLE 6B.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 20 LEAD SSOP PACKAGE**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	80.8°C/W	73.2°C/W	69.2°C/W

## TRANSISTOR COUNT

The transistor count for 9DB202 is: 2471

**PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP**

**PACKAGE OUTLINE - F SUFFIX FOR 20 LEAD SSOP**

**TABLE 6A. PACKAGE DIMENSIONS**

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

**TABLE 6B. PACKAGE DIMENSIONS**

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	2.0
A1	0.05	--
A2	1.65	1.85
b	0.22	0.38
c	0.09	0.25
D	6.90	7.50
E	7.40	8.20
E1	5.0	5.60
e	0.65 BASIC	
L	0.55	0.95
α	0°	8°

Reference Document: JEDEC Publication 95, MO-150

**TABLE 7. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
9DB202CGLF	ICS9DB202CGL	20 Lead "Lead-Free" TSSOP	Tube	0°C to 70°C
9DB202CGLFT	ICS9DB202CGL	20 Lead "Lead-Free" TSSOP	Tape & Reel	0°C to 70°C
9DB202CFLF	ICS9DB202CFLF	20 Lead "Lead-Free" SSOP	Tube	0°C to 70°C
9DB202CFLFT	ICS9DB202CFLF	20 Lead "Lead-Free" SSOP	Tape & Reel	0°C to 70°C

# REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
B	T4D	4	HCSL Table -adjusted $V_{OH}$ min from 680mV to 610mV and added $V_{OH}$ max.	12/21/04
B	T7	6 8 11	Updated HCSL Output Load AC Test Circuit Diagram. Application Information - added <i>Recommendations for Unused Input and Output Pins</i> . Ordering Information Table - added lead-free note.	3/8/06
B	T4D	4	HCSL DC Characteristics - corrected units for $V_{OH}$ & $V_{OL}$ from V to mV.	5/26/06
B		1	Feature Section - added Input Frequency Range and VCO Range.	7/14/06
B	T7	11	Ordering Information - removed leaded devices. Updated data sheet format.	7/22/15
B	T7	11	Ordering Information - removed LF note below table. Updated header and footer	2/9/16
B		1	Product Discontinuation Notice - Last time buy expires September 7, 2016. PDN N-16-02.	3/11/16



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