

## Description

The 9DBU0841 is a member of Renesas' 1.5V Ultra-Low-Power (ULP) PCIe family. It has integrated output terminations providing  $Z_o = 100\Omega$  for direct connection to  $100\Omega$  transmission lines. The device has 8 output enables for clock management and 3 selectable SMBus addresses.

## Recommended Application

1.5V PCIe Gen1-2-3 Zero-Delay/Fan-out Buffer (ZDB/FOB)

## Output Features

- 8 – 1-167MHz Low-Power (LP) HCSL DIF pairs with  $Z_o = 100\Omega$

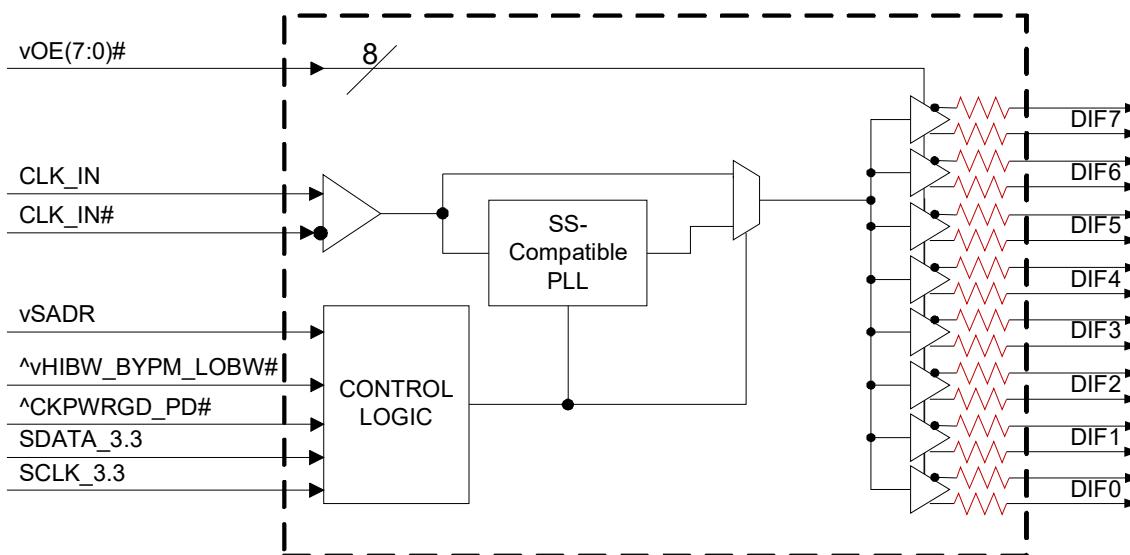
## Key Specifications

- DIF cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 80ps
- DIF phase jitter is PCIe Gen1–3 compliant
- Very low additive phase jitter in bypass mode

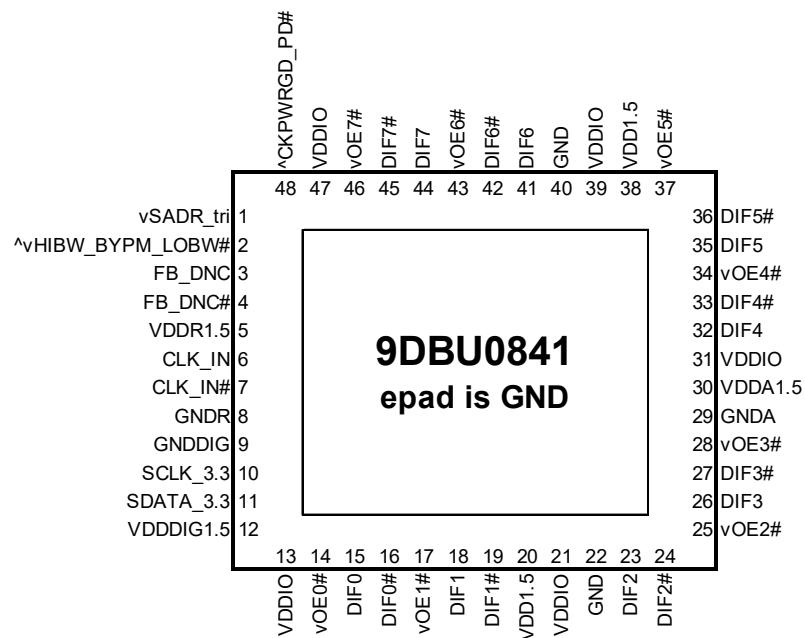
## Features/Benefits

- Direct connection to  $100\Omega$  transmission lines; saves 32 resistors compared to standard HCSL outputs
- 53mW typical power consumption in PLL mode; eliminates thermal concerns
- Outputs can optionally be supplied from any voltage between 1.05 and 1.5V; maximum power savings
- Spread Spectrum (SS) compatible; allows SS for EMI reduction
- OE# pins; support DIF power management
- HCSL-compatible differential input; can be driven by common clock sources
- Spread Spectrum tolerant; allows reduction of EMI
- SMBus-selectable features; optimize signal integrity to application:
  - Slew rate for each output
  - Differential output amplitude
- Pin/SMBus selectable PLL bandwidth and PLL Bypass; optimize PLL to application
- Outputs blocked until PLL is locked; clean system start-up
- Device contains default configuration; SMBus interface not required for device control
- Three selectable SMBus addresses; multiple devices can easily share an SMBus segment
- 3.3V tolerant SMBus interface works with legacy controllers
- Space saving 48-pin 6 x 6 mm VFQFPN; minimal board space

## Block Diagram



## Pin Configuration



### 48-pin VFQFPN, 6x6 mm, 0.4mm pitch

- ^v prefix indicates internal 120KOhm pull up *AND* pull down resistor (biased to VDD/2)
- v prefix indicates internal 120KOhm pull down resistor
- ^ prefix indicates internal 120KOhm pull up resistor

**SMBus Address Selection Table**

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	x
	M	1101100	x
	1	1101101	x

**Power Management Table**

CKPWRGD_PD#	CLK_IN	SMBus OEx bit	OEx# Pin	DIFx		PLL
				True O/P	Comp. O/P	
0	X	X	X	Low	Low	Off
1	Running	0	X	Low	Low	On <sup>1</sup>
1	Running	1	0	Running	Running	On <sup>1</sup>
1	Running	1	1	Low	Low	On <sup>1</sup>

1. If Bypass mode is selected, the PLL will be off, and outputs will be running.

**Power Connections**

Pin Number		Description	
VDD	VDDIO	GND	
5		8	Input receiver analog
12		9	Digital Power
20, 31, 38	13, 21, 31, 39, 47	22, 29, 40	DIF outputs
30		29	PLL Analog

Note: epad on this device is not electrically connected to the die. It should be connected to ground for best thermal performance.

**PLL Operating Mode**

HiBW_BypM_LoBW#	MODE	Byte1 [7:6] Readback	Byte1 [4:3] Control
0	PLL Lo BW	00	00
M	Bypass	01	01
1	PLL Hi BW	11	11

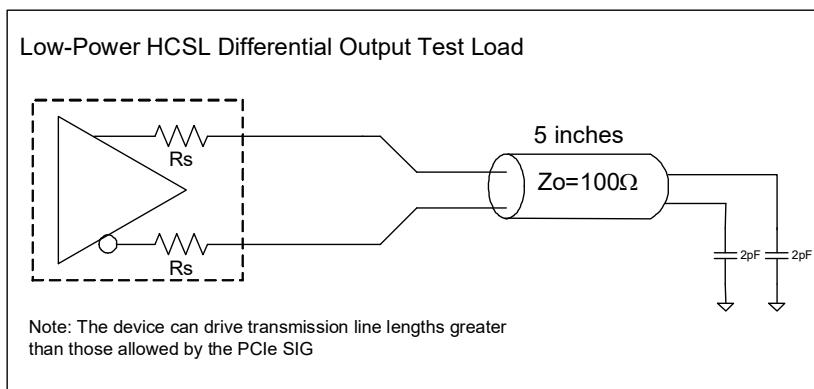
## Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	vSADR_tri	LATCHED IN	Tri-level latch to select SMBus Address. See SMBus Address Selection Table.
2	^vHIBW_BYPM_LOBW#	LATCHED IN	Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details.
3	FB_DNC	DNC	True clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
4	FB_DNC#	DNC	Complement clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
5	VDDR1.5	PWR	1.5V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
6	CLK_IN	IN	True Input for differential reference clock.
7	CLK_IN#	IN	Complementary Input for differential reference clock.
8	GNDR	GND	Analog Ground pin for the differential input (receiver)
9	GNDDIG	GND	Ground pin for digital circuitry
10	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
11	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
12	VDDDIG1.5	PWR	1.5V digital power (dirty power)
13	VDDIO	PWR	Power supply for differential outputs
14	vOE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
15	DIFO	OUT	Differential true clock output
16	DIF0#	OUT	Differential Complementary clock output
17	vOE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
18	DIF1	OUT	Differential true clock output
19	DIF1#	OUT	Differential Complementary clock output
20	VDD1.5	PWR	Power supply, nominally 1.5V
21	VDDIO	PWR	Power supply for differential outputs
22	GND	GND	Ground pin.
23	DIF2	OUT	Differential true clock output
24	DIF2#	OUT	Differential Complementary clock output
25	vOE2#	IN	Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
26	DIF3	OUT	Differential true clock output
27	DIF3#	OUT	Differential Complementary clock output
28	vOE3#	IN	Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
29	GNDA	GND	Ground pin for the PLL core.
30	VDDA1.5	PWR	1.5V power for the PLL core.
31	VDDIO	PWR	Power supply for differential outputs
32	DIF4	OUT	Differential true clock output
33	DIF4#	OUT	Differential Complementary clock output
34	vOE4#	IN	Active low input for enabling DIF pair 4. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
35	DIF5	OUT	Differential true clock output
36	DIF5#	OUT	Differential Complementary clock output
37	vOE5#	IN	Active low input for enabling DIF pair 5. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
38	VDD1.5	PWR	Power supply, nominally 1.5V
39	VDDIO	PWR	Power supply for differential outputs
40	GND	GND	Ground pin.

## Pin Descriptions (cont.)

PIN #	PIN NAME	TYPE	DESCRIPTION
41	DIF6	OUT	Differential true clock output
42	DIF6#	OUT	Differential Complementary clock output
43	vOE6#	IN	Active low input for enabling DIF pair 6. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
44	DIF7	OUT	Differential true clock output
45	DIF7#	OUT	Differential Complementary clock output
46	vOE7#	IN	Active low input for enabling DIF pair 7. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
47	VDDIO	PWR	Power supply for differential outputs
48	^CKPWRGD_PD#	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
49	EPAD	GND	Connect ePAD to ground.

## Test Loads



## Alternate Terminations

The output can easily drive other logic families. See “[AN-891 Driving LVPECL, LVDS, CML, and SSTL Logic with Universal Low-Power HCSL Outputs](#)” for LVPECL, LVDS, CML, and SSTL.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBU0841. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>DDx</sub>		-0.5		2	V	1,2
Input Voltage	V <sub>IN</sub>		-0.5		V <sub>DD</sub> +0.5	V	1,3
Input High Voltage, SMBus	V <sub>IHSMB</sub>	SMBus clock and data pins			3.3	V	1
Storage Temperature	T <sub>S</sub>		-65		150	°C	1
Junction Temperature	T <sub>J</sub>				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Operation under these conditions is neither implied nor guaranteed.

<sup>3</sup> Not to exceed 2.0V.

## Electrical Characteristics–Clock Input Parameters

TA = T<sub>AMB</sub>, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Common Mode Voltage - DIF_IN	V <sub>COM</sub>	Common Mode Input Voltage	200		725	mV	1
Input Swing - DIF_IN	V <sub>SWING</sub>	Differential value	300		1450	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND	-5		5	uA	
Input Duty Cycle	d <sub>tin</sub>	Measurement from differential waveform	45	50	55	%	1
Input Jitter - Cycle to Cycle	J <sub>DIFIn</sub>	Differential Measurement	0		150	ps	1

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Slew rate measured through +/-75mV window centered around differential zero

## Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx	Supply voltage for core and analog	1.425	1.5	1.575	V	
Output Supply Voltage	VDDIO	Supply voltage for Low Power HCSL Outputs	0.95	1.05-1.5	1.575	V	
Ambient Operating Temperature	$T_{AMB}$	Commercial range	0	25	70	°C	1
		Industrial range	-40	25	85	°C	1
Input High Voltage	$V_{IH}$	Single-ended inputs, except SMBus	0.75 $V_{DD}$		$V_{DD} + 0.3$	V	
Input Mid Voltage	$V_{IM}$	Single-ended tri-level inputs ('_tri' suffix)	0.4 $V_{DD}$		0.6 $V_{DD}$	V	
Input Low Voltage	$V_{IL}$	Single-ended inputs, except SMBus	-0.3		0.25 $V_{DD}$	V	
Input Current	$I_{IN}$	$V_{IN} = GND, V_{IN} = VDD$	-5		5	uA	
	$I_{INP}$	$V_{IN} = 0 V$ ; Inputs with internal pull-up resistors $V_{IN} = VDD$ ; Inputs with internal pull-down resistors	-200		200	uA	
Input Frequency	$F_{ibyp}$	Bypass mode	1		167	MHz	2
	$F_{ipll}$	100MHz PLL mode	20	100.00	110	MHz	2
Pin Inductance	$L_{pin}$				7	nH	1
Capacitance	$C_{IN}$	Logic Inputs, except DIF_IN	1.5		5	pF	1
	$C_{INDIF\_IN}$	DIF_IN differential clock inputs	1.5		2.7	pF	1,5
	$C_{OUT}$	Output pin capacitance			6	pF	1
Clk Stabilization	$T_{STAB}$	From $V_{DD}$ Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1,2
Input SS Modulation Frequency PCIe	$f_{MODINPCle}$	Allowable Frequency for PCIe Applications (Triangular Modulation)	30		33	kHz	
Input SS Modulation Frequency non-PCIe	$f_{MODIN}$	Allowable Frequency for non-PCIe Applications (Triangular Modulation)	0		66	kHz	
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	clocks	1,3
Tdrive_PD#	$t_{DRVPD}$	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	$t_F$	Fall time of single-ended control inputs			5	ns	2
Trise	$t_R$	Rise time of single-ended control inputs			5	ns	2
SMBus Input Low Voltage	$V_{ILSMB}$				0.6	V	
SMBus Input High Voltage	$V_{IHSM}$	$V_{DDSMB} = 3.3V$ , see note 4 for $V_{DDSMB} < 3.3V$	2.1		3.3	V	4
SMBus Output Low Voltage	$V_{OLSMB}$	@ $I_{PULLUP}$			0.4	V	
SMBus Sink Current	$I_{PULLUP}$	@ $V_{OL}$	4			mA	
Nominal Bus Voltage	$V_{DDSMB}$	Bus Voltage	1.425		3.3	V	
SCLK/SDATA Rise Time	$t_{RSMB}$	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	$t_{FSMB}$	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	$f_{MAXSMB}$	Maximum SMBus operating frequency			400	kHz	6

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup>Time from deassertion until outputs are >200 mV

<sup>4</sup> For  $V_{DDSMB} < 3.3V$ ,  $V_{IHSM} \geq 0.8 \times V_{DDSMB}$

<sup>5</sup>DIF\_IN input

<sup>6</sup>The differential input clock must be running for the SMBus to be active

## Electrical Characteristics—DIF Low-Power HCSL Outputs

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	dV/dt	Scope averaging on, fast setting	1	2.4	3.5	V/ns	1,2,3
	dV/dt	Scope averaging on, slow setting	0.7	1.7	2.5	V/ns	1,2,3
Slew rate matching	$\Delta$ dV/dt	Slew rate matching, Scope averaging on		9	20	%	1,2,4
Voltage High	$V_{HIGH}$	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	630	750	850	mV	7
Voltage Low	$V_{LOW}$		-150	26	150		7
Max Voltage	$V_{max}$	Measurement on single ended signal using absolute value. (Scope averaging off)		763	1150	mV	7
Min Voltage	$V_{min}$		-300	22			7
Vswing	$V_{swing}$	Scope averaging off	300	1448		mV	1,2
Crossing Voltage (abs)	$V_{cross\_abs}$	Scope averaging off	250	390	550	mV	1,5
Crossing Voltage (var)	$\Delta V_{cross}$	Scope averaging off		11	140	mV	1,6

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

<sup>4</sup> Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

<sup>5</sup>  $V_{cross}$  is defined as voltage where  $Clock = Clock\#$  measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>6</sup> The total variation of all  $V_{cross}$  measurements in any particular system. Note that this is a subset of  $V_{cross\_min/max}$  ( $V_{cross}$  absolute) allowed. The intent is to limit  $V_{cross}$  induced modulation by setting  $\Delta V_{cross}$  to be smaller than  $V_{cross}$  absolute.

<sup>7</sup> At default SMBus settings.

## Electrical Characteristics—Current Consumption

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	$I_{DDA}$	$V_{DDA}+V_{DDR}$ , PLL Mode, @100MHz		11	15	mA	
	$I_{DD}$	$V_{DD}$ , All outputs active @100MHz		6	9	mA	
	$I_{DDIO}$	$V_{DDIO}$ , All outputs active @100MHz		28	35	mA	
Powerdown Current	$I_{DDAPD}$	$V_{DDA}+V_{DDR}$ , CKPWRGD_PD#=0		0.5	1	mA	2
	$I_{DDPD}$	$V_{DDx}$ , CKPWRGD_PD#=0		0.6	1	mA	2
	$I_{DDIOPD}$	$V_{DDIO}$ , CKPWRGD_PD#=0		0.003	0.01	mA	2

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Input clock stopped.

## Electrical Characteristics—Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PLL Bandwidth	BW	-3dB point in High BW Mode (100MHz)	2.3	3.6	4.7	MHz	1,5
		-3dB point in Low BW Mode (100MHz)	1	1.6	2.5	MHz	1,5
PLL Jitter Peaking	$t_{JPEAK}$	Peak Pass band Gain (100MHz)		1.3	2.5	dB	1
Duty Cycle	$t_{DC}$	Measured differentially, PLL Mode	45	50	55	%	1
Duty Cycle Distortion	$t_{DCD}$	Measured differentially, Bypass Mode	-1	-0.6	0	%	1,3
Skew, Input to Output	$t_{pdBYP}$	Bypass Mode, $V_T = 50\%$	3400	4301	5200	ps	1
	$t_{pdPLL}$	PLL Mode $V_T = 50\%$	0	50	150	ps	1,4
Skew, Output to Output	$t_{sk3}$	$V_T = 50\%$		37	75	ps	1,4
		PLL mode		24	50	ps	1,2
Jitter, Cycle to cycle	$t_{j_{cyc-cyc}}$	Additive Jitter in Bypass Mode		0.1	10	ps	1,2

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

<sup>4</sup> All outputs at default slew rate

<sup>5</sup> The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

## Electrical Characteristics—Phase Jitter Parameters

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPClēG1}$	PCIe Gen 1		30	58	86	ps (p-p)	1,2,3,5
	$t_{jphPClēG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.9	1.4	3	ps (rms)	1,2,3,5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		2.1	2.6	3.1	ps (rms)	1,2,3,5
	$t_{jphPClēG3}$	PCIe Gen 3 Common Clock Architecture (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz)		0.5	0.6	1	ps (rms)	1,2,3,5
	$t_{jphPClēG3SRnS}$	PCIe Gen 3 Separate Reference No Spread (SRnS) (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz)		0.5	0.6	0.7	ps (rms)	1,2,3,5
Additive Phase Jitter, Bypass Mode	$t_{jphPClēG1}$	PCIe Gen 1		0.1	5	N/A	ps (p-p)	1,2,3,5
	$t_{jphPClēG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.1	0.5	N/A	ps (rms)	1,2,3,4,5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.1	0.7	N/A	ps (rms)	1,2,3,4
	$t_{jphPClēG3}$	PCIe Gen 3 (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz)		0.2	0.3	N/A	ps (rms)	1,2,3,4
	$t_{jph125M0}$	125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		200	250	N/A	fs (rms)	1,6
	$t_{jph125M1}$	125MHz, 12KHz to 20MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		313	350	N/A	fs (rms)	1,6

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> See <http://www.pcisig.com> for complete specs

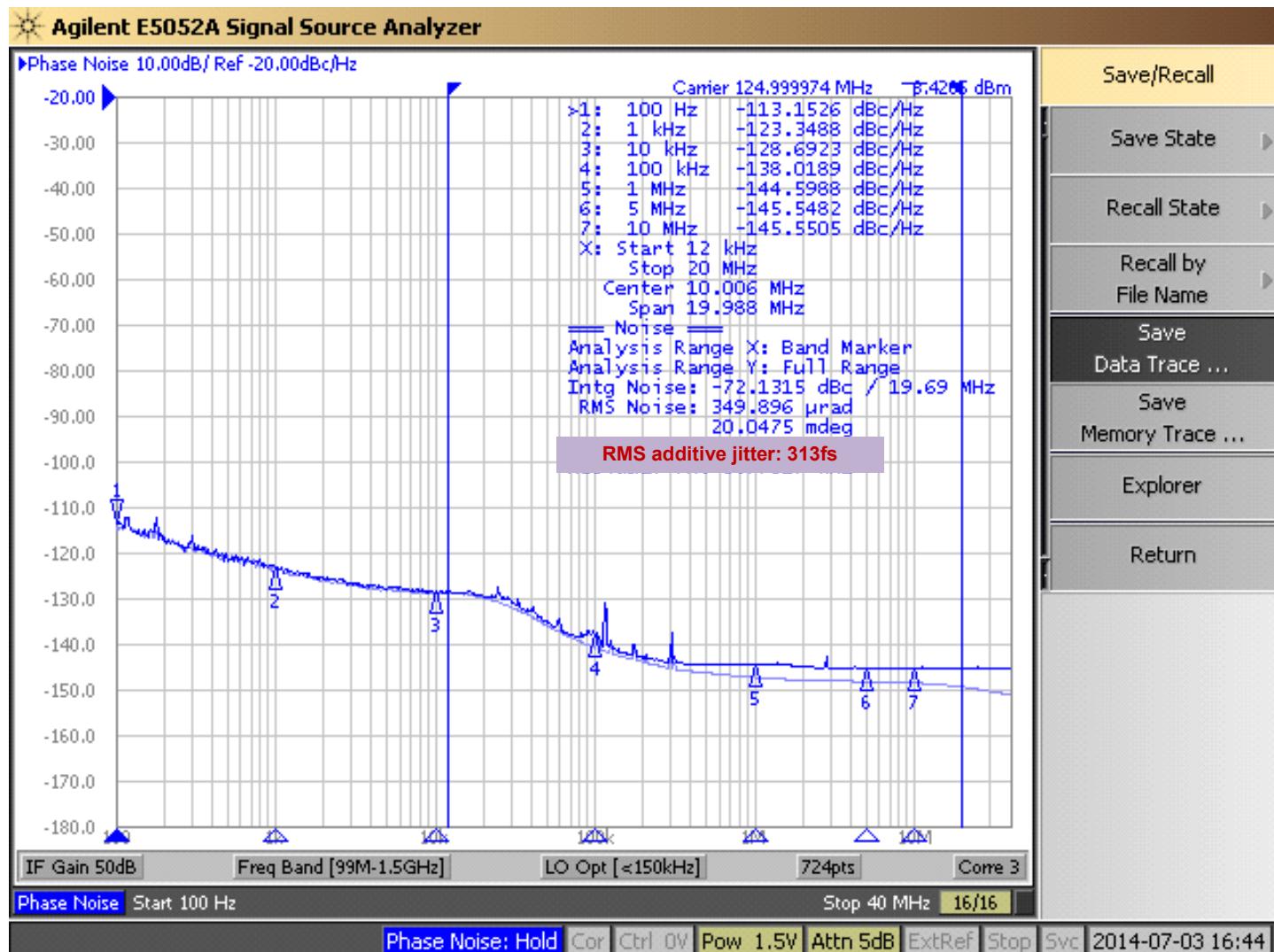
<sup>3</sup> Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

<sup>4</sup> For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter =  $\sqrt{(\text{total jitter})^2 - (\text{input jitter})^2}$

<sup>5</sup> Driven by 9FGU0831 or equivalent

<sup>6</sup> Rohde&Schartz SMA100

## Additive Phase Jitter Plot: 125M (12kHz to 20MHz)



## General SMBus Serial Interface Information

### How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N** through Byte **N+X-1**
- Renesas clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

### How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if X<sub>(H)</sub> was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation			
Controller (Host)		Renesas (Slave/Receiver)	
T	starT bit		
Slave Address			
WR	WRite		
		ACK	
Beginning Byte = N		ACK	
		ACK	
Data Byte Count = X		ACK	
		ACK	
Beginning Byte N		ACK	
O		O	
O		O	
O		O	
Byte N + X - 1			ACK
P	stoP bit		

Index Block Read Operation			
Controller (Host)		Renesas	
T	starT bit		
Slave Address			
WR	WRite		
		ACK	
Beginning Byte = N		ACK	
		ACK	
RT	Repeat starT		
Slave Address			
RD	ReaD		
		ACK	
			Data Byte Count=X
		ACK	
			Beginning Byte N
		ACK	
			O
		O	
		O	
		O	
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Note: SMBus Address is Latched on SADR pin.

**SMBus Table: Output Enable Register<sup>1</sup>**

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	DIF OE7	Output Enable	RW	Low/Low	Enabled	1
Bit 6	DIF OE6	Output Enable	RW	Low/Low	Enabled	1
Bit 5	DIF OE5	Output Enable	RW	Low/Low	Enabled	1
Bit 4	DIF OE4	Output Enable	RW	Low/Low	Enabled	1
Bit 3	DIF OE3	Output Enable	RW	Low/Low	Enabled	1
Bit 2	DIF OE2	Output Enable	RW	Low/Low	Enabled	1
Bit 1	DIF OE1	Output Enable	RW	Low/Low	Enabled	1
Bit 0	DIF OE0	Output Enable	RW	Low/Low	Enabled	1

1. A low on these bits will override the OE# pin and force the differential output Low/Low

**SMBus Table: PLL Operating Mode and Output Amplitude Control Register**

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	PLLMODERB1	PLL Mode Readback Bit 1	R	See PLL Operating Mode Table		Latch
Bit 6	PLLMODERB0	PLL Mode Readback Bit 0				
Bit 5	PLLMODE_SWCNTRL	Enable SW control of PLL Mode	RW	Values in B1[7:6] set PLL Mode	Values in B1[4:3] set PLL Mode	0
Bit 4	PLLMODE1	PLL Mode Control Bit 1	RW <sup>1</sup>	See PLL Operating Mode Table		0
Bit 3	PLLMODE0	PLL Mode Control Bit 0	RW <sup>1</sup>			0
Bit 2	Reserved					
Bit 1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.55V	01 = 0.65V	1
Bit 0	AMPLITUDE 0		RW	10 = 0.7V	11 = 0.8V	0

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

**SMBus Table: DIF Slew Rate Control Register**

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	SLEWRATESEL DIF7	Adjust Slew Rate of DIF7	RW	Slow Setting	Fast Setting	1
Bit 6	SLEWRATESEL DIF6	Adjust Slew Rate of DIF6	RW	Slow Setting	Fast Setting	1
Bit 5	SLEWRATESEL DIF5	Adjust Slew Rate of DIF5	RW	Slow Setting	Fast Setting	1
Bit 4	SLEWRATESEL DIF4	Adjust Slew Rate of DIF4	RW	Slow Setting	Fast Setting	1
Bit 3	SLEWRATESEL DIF3	Adjust Slew Rate of DIF3	RW	Slow Setting	Fast Setting	1
Bit 2	SLEWRATESEL DIF2	Adjust Slew Rate of DIF2	RW	Slow Setting	Fast Setting	1
Bit 1	SLEWRATESEL DIF1	Adjust Slew Rate of DIF1	RW	Slow Setting	Fast Setting	1
Bit 0	SLEWRATESEL DIF0	Adjust Slew Rate of DIF0	RW	Slow Setting	Fast Setting	1

Note: See "Low-Power HCSL Outputs" table for slew rates.

**SMBus Table: Frequency Select Control Register**

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					
Bit 6	Reserved					
Bit 5	Reserved					
Bit 4	Reserved					
Bit 3	Reserved					
Bit 2	Reserved					
Bit 1	Reserved					
Bit 0	SLEWRATESEL FB	Adjust Slew Rate of FB	RW	Slow Setting	Fast Setting	1

**Byte 4 is Reserved and reads back 'hFF'**

**SMBus Table: Revision and Vendor ID Register**

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	A rev = 0000		0
Bit 6	RID2		R			0
Bit 5	RID1		R			0
Bit 4	RID0		R			0
Bit 3	VID3	VENDOR ID	R	0001 = IDT		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

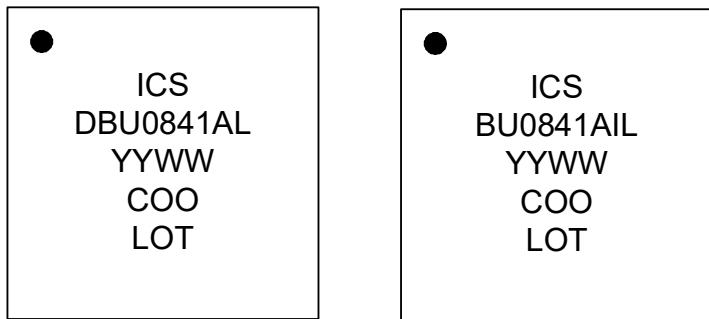
**SMBus Table: Device Type/Device ID**

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device Type1	Device Type	R	00 = FGx, 01 = DBx ZDB/FOB, 10 = DMx, 11= DBx FOB		0
Bit 6	Device Type0		R			1
Bit 5	Device ID5	Device ID	R	001000 binary or 08 hex		0
Bit 4	Device ID4		R			0
Bit 3	Device ID3	Device ID	R	001000 binary or 08 hex		1
Bit 2	Device ID2		R			0
Bit 1	Device ID1	Device ID	R	001000 binary or 08 hex		0
Bit 0	Device ID0		R			0

**SMBus Table: Byte Count Register**

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7		Reserved				0
Bit 6		Reserved				0
Bit 5		Reserved				0
Bit 4	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is = 8 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

## Marking Diagrams



### Notes:

1. "LOT" is the lot sequence number.
2. "COO" denotes country of origin.
3. YYWW is the last two digits of the year and week that the part was assembled.
4. Line 2: truncated part number
5. "L" denotes RoHS compliant package.
6. "I" denotes industrial temperature range device.

## Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP VALUE	UNITS	NOTES
Thermal Resistance	$\theta_{JC}$	Junction to Case	NDG48	33	°C/W	1
	$\theta_{Jb}$	Junction to Base		2.1	°C/W	1
	$\theta_{JA0}$	Junction to Air, still air		37	°C/W	1
	$\theta_{JA1}$	Junction to Air, 1 m/s air flow		30	°C/W	1
	$\theta_{JA3}$	Junction to Air, 3 m/s air flow		27	°C/W	1
	$\theta_{JA5}$	Junction to Air, 5 m/s air flow		26	°C/W	1

<sup>1</sup>ePad soldered to board

## Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

[48-VFQFPN 6.0 x 6.0 x 0.9 mm Body, 0.4 mm Pitch](#)

## Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9DBU0841AKLF	Trays	48-pin VFQFPN	0 to +70° C
9DBU0841AKLFT	Tape and Reel	48-pin VFQFPN	0 to +70° C
9DBU0841AKILF	Trays	48-pin VFQFPN	-40 to +85° C
9DBU0841AKILFT	Tape and Reel	48-pin VFQFPN	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

## Revision History

Revision Date	Description
7/16/2014	<ol style="list-style-type: none"><li>1. Updated electrical tables with char data.</li><li>2. Added an additive phase jitter plot.</li><li>3. Added 12kHz to 20MHz <i>additive</i> phase jitter spec.</li><li>4. Updated Amplitude control bit <i>descriptions</i> in Byte 1.</li></ol>
9/19/2014	Updated SMBus Input High/Low parameters conditions, MAX values, and footnotes.
4/17/2015	<ol style="list-style-type: none"><li>1. Updated pin out and pin descriptions to show ePad on package connected to ground.</li><li>2. Minor updates to front page text for family consistency.</li><li>3. Updated Clock Input Parameters table to be consistent with PCIe Vswing parameter.</li></ol>
12/3/2025	<ol style="list-style-type: none"><li>1. Rebranded datasheet to Renesas.</li><li>2. Updated "Alternate Terminations" section.</li><li>3. Updated "Package Outline Drawings" section.</li></ol>



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## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

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TOYOSU FORESIA, 3-2-24 Toyosu,  
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