

## General Description

The 9DMU0441 is a member of IDT's SOC-Friendly 1.5V Ultra-Low-Power (ULP) PCIe Gen1-2-3 family. It has integrated output terminations providing  $Z_o=100\text{ohms}$  for direct connection to 100ohm transmission lines. Each of the 4 outputs has its own dedicated OE# pin for optimal system control and power management. The part provides asynchronous and glitch-free switching modes.

## Recommended Application

2:4 PCIe Gen1-2-3 clock multiplexer

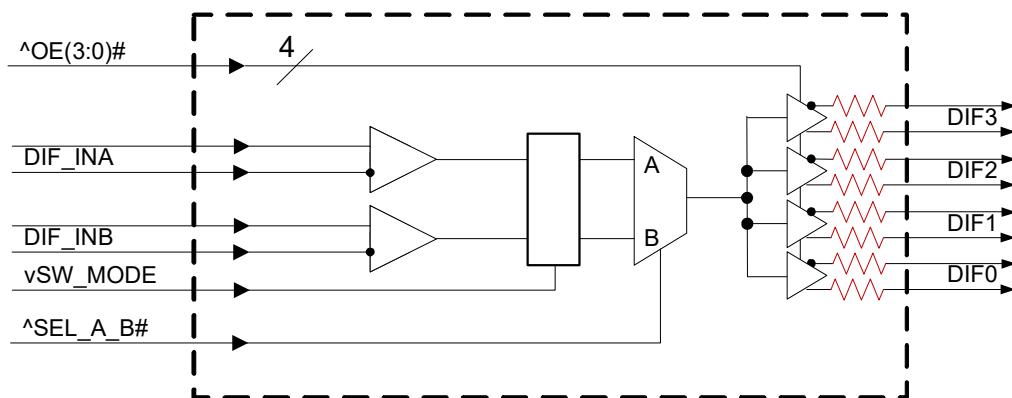
## Output Features

- 4 – Low-Power (LP) HCSL DIF pairs w/ $Z_o=100\Omega$

## Key Specifications

- DIF *additive* cycle-to-cycle jitter <5ps
- DIF phase jitter is PCIe Gen1-2-3 compliant
- Additive phase jitter @ 125MHz: 535fs rms typical (12kHz to 20MHz)
- DIF output-to-output skew <50ps

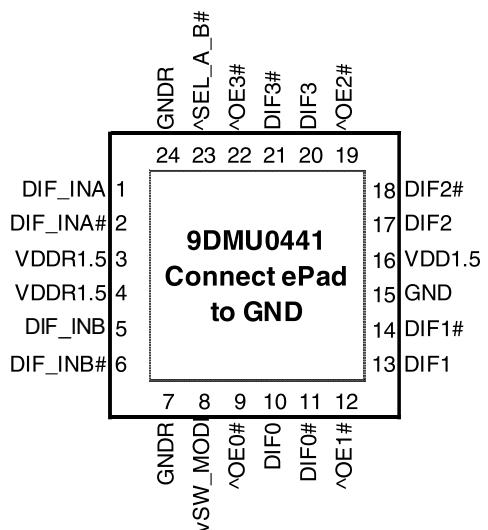
## Block Diagram



## Features/Benefits

- LP-HCSL outputs w/integrated terminations; saves 16 resistors compared to standard HCSL outputs
- 1.5V operation; 26mW typical power consumption
- Selectable asynchronous or glitch-free switching; allows the mux to be selected at power up even if both inputs are not running, then transition to glitch-free switching mode
- Spread Spectrum Compatible; supports EMI reduction
- OE# pins; support DIF power management
- HCSL differential inputs; can be driven by common clock sources
- 1MHz to 167MHz operating frequency
- Space saving 24-pin 4x4mm VFQFPN; minimal board space

## Pin Configuration



**24 VFQFPN, 4x4 mm, 0.5mm pitch**

^ prefix indicates internal 120KOhm pull up resistor  
v prefix indicates internal 120KOhm pull down resistor

### Power Management Table

OEx# Pin	DIF_IN	DIFx	
		True O/P	Comp. O/P
0	Running	Running	Running
1	Running	Low	Low

### Power Connections

Pin Number		Description
VDD	GND	
3	24	Input A receiver analog
4	7	Input B receiver analog
16	15	DIF outputs

### Pin Descriptions

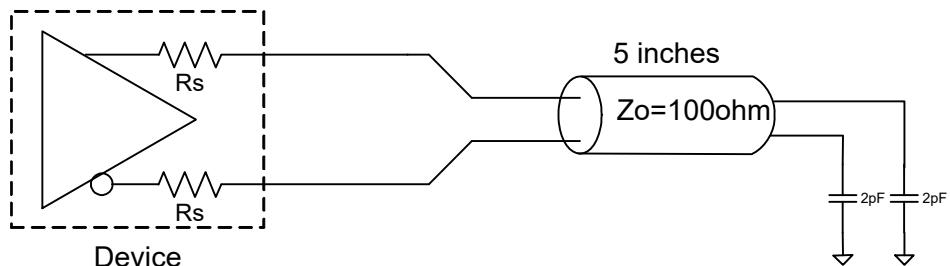
Pin#	Pin Name	Type	Pin Description
1	DIF_INA	IN	HCSL Differential True input
2	DIF_INA#	IN	HCSL Differential Complement Input
3	VDDR1.5	PWR	1.5V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
4	VDDR1.5	PWR	1.5V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
5	DIF_INB	IN	HCSL Differential True input
6	DIF_INB#	IN	HCSL Differential Complement Input
7	GNDR	GND	Analog Ground pin for the differential input (receiver)
8	vSW_MODE	IN	Switch Mode. This pin selects either asynchronous or glitch-free switching of the mux. Use asynchronous mode if 0 or 1 of the input clocks is running. Use glitch-free mode if both input clocks are running. This pin has an internal pull down resistor of ~120kohms. 0 = asynchronous mode 1 = glitch-free mode
9	^OE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs
10	DIF0	OUT	Differential true clock output
11	DIF0#	OUT	Differential Complementary clock output
12	^OE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs
13	DIF1	OUT	Differential true clock output
14	DIF1#	OUT	Differential Complementary clock output
15	GND	GND	Ground pin.

## Pin Descriptions (cont.)

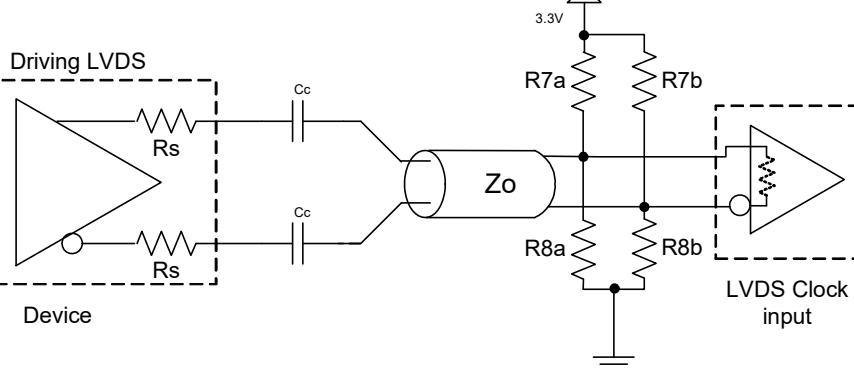
Pin#	Pin Name	Type	Pin Description
16	VDD1.5	PWR	Power supply, nominally 1.5V
17	DIF2	OUT	Differential true clock output
18	DIF2#	OUT	Differential Complementary clock output
19	^OE2#	IN	Active low input for enabling DIF pair 2. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs
20	DIF3	OUT	Differential true clock output
21	DIF3#	OUT	Differential Complementary clock output
22	^OE3#	IN	Active low input for enabling DIF pair 3. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs
23	^SEL_A_B#	IN	Input to select differential input clock A or differential input clock B. This input has an internal pull-up resistor. 0 = Input B selected, 1 = Input A selected.
24	GNDR	GND	Analog Ground pin for the differential input (receiver)
25	EPAD	GND	Connect to Ground.

## Test Loads

Low-Power HCSL Differential Output Test Load



## Driving LVDS



### Driving LVDS inputs

Component	Value		Note
	Receiver has termination	Receiver does not have termination	
$R_{7a}, R_{7b}$	10K ohm	140 ohm	
$R_{8a}, R_{8b}$	5.6K ohm	75 ohm	
$C_c$	0.1 $\mu\text{F}$	0.1 $\mu\text{F}$	
$V_{cm}$	1.2 volts	1.2 volts	

## Electrical Characteristics—Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>DDx</sub>		-0.5		2	V	1,2
Input Voltage	V <sub>IN</sub>		-0.5		V <sub>DD</sub> +0.5	V	1,3
Input High Voltage, SMBus	V <sub>IHSMB</sub>	SMBus clock and data pins			3.3	V	1
Storage Temperature	T <sub>S</sub>		-65		150	°C	1
Junction Temperature	T <sub>J</sub>				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Operation under these conditions is neither implied nor guaranteed.

<sup>3</sup> Not to exceed 2.0V.

## Electrical Characteristics—Input/Supply/Common Parameters—Normal Operating Conditions

TA = T<sub>AMB</sub>, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>DDx</sub>	Supply voltage for core and analog	1.425	1.5	1.575	V	
Ambient Operating Temperature	T <sub>AMB</sub>	Industrial range	-40	25	85	°C	1
Input High Voltage	V <sub>IH</sub>	Single-ended inputs, except SMBus	0.75 V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V	
Input Low Voltage	V <sub>IL</sub>	Single-ended inputs, except SMBus	-0.3		0.25 V <sub>DD</sub>	V	
Input Current	I <sub>IN</sub>	Single-ended inputs, V <sub>IN</sub> = GND, V <sub>IN</sub> = VDD	-5		5	uA	
	I <sub>INP</sub>	Single-ended inputs V <sub>IN</sub> = 0 V; Inputs with internal pull-up resistors V <sub>IN</sub> = VDD; Inputs with internal pull-down resistors	-200		200	uA	
Input Frequency	F <sub>in</sub>		1		167	MHz	2
Pin Inductance	L <sub>pin</sub>				7	nH	1
Capacitance	C <sub>IN</sub>	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C <sub>INDIF_IN</sub>	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C <sub>OUT</sub>	Output pin capacitance			6	pF	1
Clk Stabilization	T <sub>STAB</sub>	From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1,2
Input SS Modulation Frequency PCIe	f <sub>MODINPCIE</sub>	Allowable Frequency for PCIe Applications (Triangular Modulation)	30		33	kHz	
Input SS Modulation Frequency non-PCIe	f <sub>MODIN</sub>	Allowable Frequency for non-PCIe Applications (Triangular Modulation)	0		66	kHz	
OE# Latency	t <sub>LATOE#</sub>	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	clocks	1,3
Tfall	t <sub>F</sub>	Fall time of single-ended control inputs			5	ns	2
Trise	t <sub>R</sub>	Rise time of single-ended control inputs			5	ns	2

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup>Time from deassertion until outputs are >200 mV

<sup>4</sup> DIF\_IN input

## Electrical Characteristics—Clock Input Parameters

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	$V_{IHDF}$	Differential inputs (single-ended measurement)	300	750	1150	mV	1
Input Low Voltage - DIF_IN	$V_{ILDIF}$	Differential inputs (single-ended measurement)	$V_{SS} - 300$	0	300	mV	1
Input Common Mode Voltage - DIF_IN	$V_{COM}$	Common Mode Input Voltage	200		725	mV	1
Input Amplitude - DIF_IN	$V_{SWING}$	Peak to Peak value ( $V_{IHDF} - V_{ILDIF}$ )	300		1450	mV	1
Input Slew Rate - DIF_IN	$dV/dt$	Measured differentially	0.35		8	V/ns	1,2
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{DD}$ , $V_{IN} = GND$	-5		5	uA	
Input Duty Cycle	$d_{tin}$	Measurement from differential waveform	45	50	55	%	1
Input Jitter - Cycle to Cycle	$J_{DIFin}$	Differential Measurement	0		150	ps	1

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Slew rate measured through +/-75mV window centered around differential zero

## Electrical Characteristics—DIF Low-Power HCSL Outputs

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	$dV/dt$	Scope averaging on, fast setting	1.1	2.3	3.4	V/ns	1,2,3
Slew rate matching	$\Delta dV/dt$	Slew rate matching, Scope averaging on		12	20	%	1,2,4
Voltage High	$V_{HIGH}$	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	550	755	850	mV	
Voltage Low	$V_{LOW}$		-150	28	150		
Max Voltage	$V_{max}$	Measurement on single ended signal using absolute value. (Scope averaging off)		761	1150	mV	
Min Voltage	$V_{min}$		-300	10			
$V_{swing}$	$V_{swing}$	Scope averaging off	300	1455		mV	1,2
Crossing Voltage (abs)	$V_{cross\_abs}$	Scope averaging off	250	377	550	mV	1,5
Crossing Voltage (var)	$\Delta V_{cross}$	Scope averaging off		10	140	mV	1,6

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Slew rate is measured through the  $V_{swing}$  voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

<sup>4</sup> Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

<sup>5</sup>  $V_{cross}$  is defined as voltage where  $Clock = Clock\#$  measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>6</sup> The total variation of all  $V_{cross}$  measurements in any particular system. Note that this is a subset of  $V_{cross\_min/max}$  ( $V_{cross}$  absolute) allowed. The intent is to limit  $V_{cross}$  induced modulation by setting  $\Delta V_{cross}$  to be smaller than  $V_{cross}$  absolute.

## Electrical Characteristics—Current Consumption

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	$I_{DD}$	VDD, All outputs active @ 100MHz		17	26	mA	1
Powerdown Current	$I_{DDPD}$	VDD, all outputs disabled		1.4	2.5	mA	1, 2

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Input clock stopped.

## Electrical Characteristics—Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle Distortion	$t_{DCD}$	Measured differentially, Bypass Mode @100MHz	-1	-0.1	1	%	1,3
Skew, Input to Output	$t_{pdBYP}$	Bypass Mode, $V_T = 50\%$	2082	2915	4081	ps	1
Skew, Output to Output	$t_{sk3}$	$V_T = 50\%$		16	50	ps	1,4
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Additive Jitter in Bypass Mode		0.1	5	ps	1,2

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode

<sup>4</sup> All outputs at default slew rate

<sup>5</sup> The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

## Electrical Characteristics—Phase Jitter Parameters

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Additive Phase Jitter, Bypass Mode	$t_{jphPCleG1}$	PCIe Gen 1		1.3	5	N/A	ps (p-p)	1,2,3,5
	$t_{jphPCleG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.1	0.5	N/A	ps (rms)	1,2,3,4, 5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.1	0.6	N/A	ps (rms)	1,2,3,4
	$t_{jphPCleG3}$	PCIe Gen 3 (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz)		0.170	0.3	N/A	ps (rms)	1,2,3,4
	$t_{jph125M0}$	125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		365	380	N/A	fs (rms)	1,6
	$t_{jph125M1}$	125MHz, 12KHz to 20MHz, -20dB/decade rollover < 12kHz, -40db/decade rolloff > 20MHz		535	550	N/A	fs (rms)	1,6

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> See <http://www.pcisig.com> for complete specs

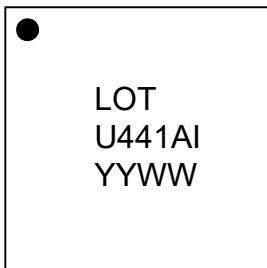
<sup>3</sup> Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

<sup>4</sup> For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter =  $\sqrt{(\text{total jitter})^2 - (\text{input jitter})^2}$

<sup>5</sup> Driven by 9FGU0831 or equivalent

<sup>6</sup> Rohde&Schartz SMA100

## Marking Diagrams



Notes:

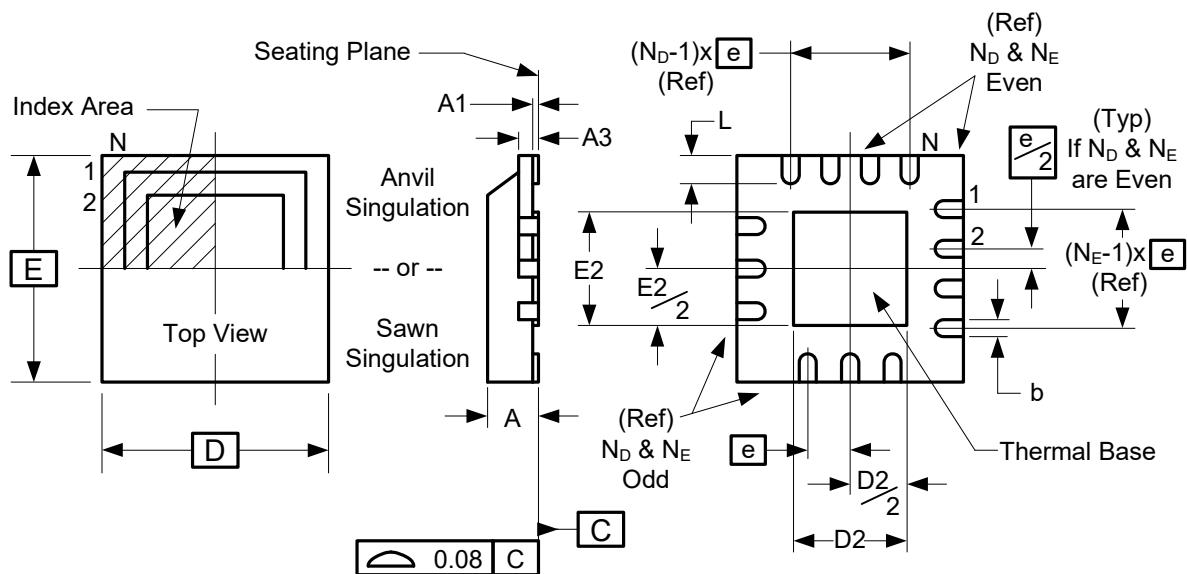
1. "LOT" denotes the lot number.
2. "YYWW" is the last two digits of the year and week that the part was assembled.
3. Line 2: truncated part number
4. "I" denotes industrial temperature grade.

## Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP VALUE	UNITS	NOTES
Thermal Resistance	$\theta_{JC}$	Junction to Case	NLG24	42	°C/W	1
	$\theta_{Jb}$	Junction to Base		2.4	°C/W	1
	$\theta_{JA0}$	Junction to Air, still air		39	°C/W	1
	$\theta_{JA1}$	Junction to Air, 1 m/s air flow		33	°C/W	1
	$\theta_{JA3}$	Junction to Air, 3 m/s air flow		28	°C/W	1
	$\theta_{JA5}$	Junction to Air, 5 m/s air flow		27	°C/W	1

<sup>1</sup>ePad soldered to board

## Package Outline and Package Dimensions (NLG24)



Millimeters		
Symbol	Min	Max
A	0.80	1.00
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
D x E BASIC	4.00 x 4.00	
D2 MIN./MAX.	2.3	2.55
E2 MIN./MAX.	2.3	2.55
L MIN./MAX.	0.30	0.50
N	24	
ND	6	
NE	6	

## Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9DMU0441AKILF	Tubes	24-pin VFQFPN	-40 to +85° C
9DMU0441AKILFT	Tape and Reel	24-pin VFQFPN	-40 to +85° C

"LF" to the suffix denotes Pb-Free configuration, RoHS compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

## Revision History

Rev.	Initiator	Issue Date	Description	Page #
A	RDW	9/24/2014	1. Updated additive phase jitter and General Description 2. Move to final	1,7

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