

General Description

The 9DMV0431 is a member of IDT's SOC-Friendly 1.8V Very-Low-Power (VLP) PCIe Gen1-2-3 family. Each of the 4 outputs has its own dedicated OE# pin for optimal system control and power management. The part provides asynchronous and glitch-free switching modes.

Recommended Application

2:4 PCIe Gen1-2-3 clock multiplexer

Output Features

- 4 -Low-Power (LP) HCSL DIF pairs

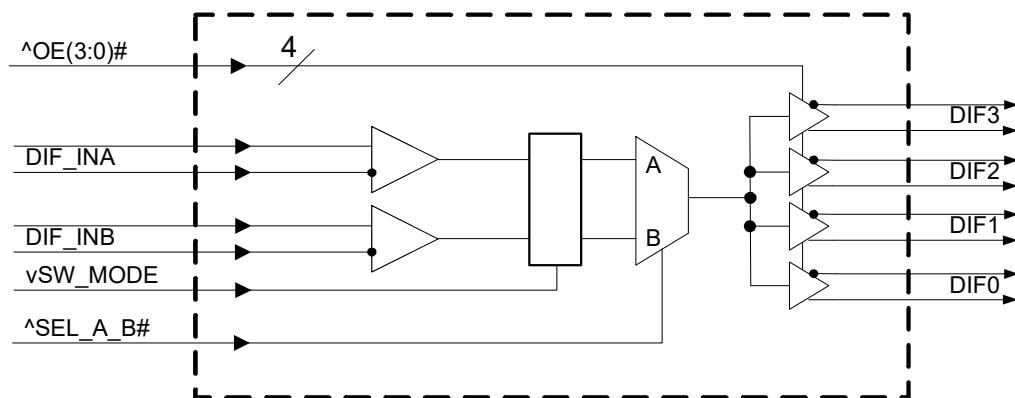
Key Specifications

- DIF additive cycle-to-cycle jitter <5ps
- DIF phase jitter is PCIe Gen1-2-3 compliant
- Additive phase jitter @ 125MHz: 420fs rms typical (12kHz to 20MHz)
- DIF output-to-output skew <50ps

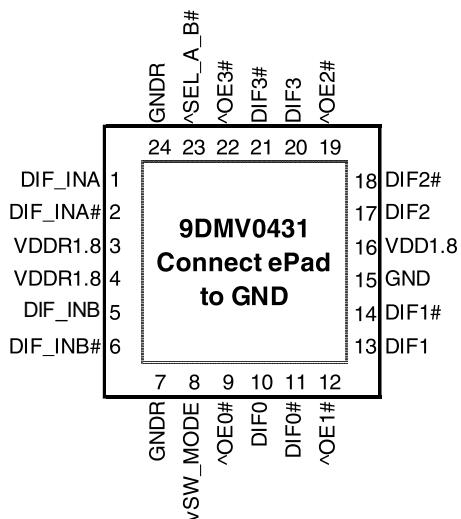
Features/Benefits

- LP-HCSL outputs; save 8 resistors compared to standard HCSL outputs
- 1.8V operation; 36mW typical power consumption
- Selectable asynchronous or glitch-free switching; allows the mux to be selected at power up even if both inputs are not running, then transition to glitch-free switching mode
- Spread Spectrum Compatible; supports EMI reduction
- OE# pins; support DIF power management
- HCSL differential inputs; can be driven by common clock sources
- 1MHz to 200MHz operating frequency
- Space saving 24-pin 4x4mm VFQFPN; minimal board space

Block Diagram



Pin Configuration



24 VFQFPN, 4x4 mm, 0.5mm pitch

^ prefix indicates internal 120KOhm pull up resistor

v prefix indicates internal 120KOhm pull down resistor

Power Management Table

OEx# Pin	DIF_IN	DIFx	
		True O/P	Comp. O/P
0	Running	Running	Running
1	Running	Low	Low

Power Connections

Pin Number		Description
VDD	GND	
3	24	Input A receiver analog
4	7	Input B receiver analog
16	15	DIF outputs

Pin Descriptions

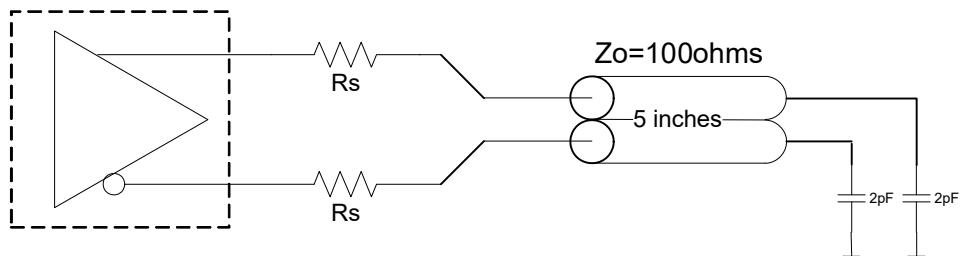
Pin#	Pin Name	Type	Pin Description
1	DIF_INA	IN	HCSL Differential True input
2	DIF_INA#	IN	HCSL Differential Complement Input
3	VDDR1.8	PWR	1.8V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
4	VDDR1.8	PWR	1.8V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
5	DIF_INB	IN	HCSL Differential True input
6	DIF_INB#	IN	HCSL Differential Complement Input
7	GNDR	GND	Analog Ground pin for the differential input (receiver)
8	vSW_MODE	IN	Switch Mode. This pin selects either asynchronous or glitch-free switching of the mux. Use asynchronous mode if 0 or 1 of the input clocks is running. Use glitch-free mode if both input clocks are running. This pin has an internal pull down resistor of ~120kohms. 0 = asynchronous mode 1 = glitch-free mode
9	^OE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs
10	DIFO	OUT	Differential true clock output
11	DIFO#	OUT	Differential Complementary clock output
12	^OE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs
13	DIF1	OUT	Differential true clock output
14	DIF1#	OUT	Differential Complementary clock output
15	GND	GND	Ground pin.

Pin Descriptions (cont.)

Pin#	Pin Name	Type	Pin Description
16	VDD1.8	PWR	Power supply, nominal 1.8V
17	DIF2	OUT	Differential true clock output
18	DIF2#	OUT	Differential Complementary clock output
19	^OE2#	IN	Active low input for enabling DIF pair 2. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs
20	DIF3	OUT	Differential true clock output
21	DIF3#	OUT	Differential Complementary clock output
22	^OE3#	IN	Active low input for enabling DIF pair 3. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs
23	^SEL_A_B#	IN	Input to select differential input clock A or differential input clock B. This input has an internal pull-up resistor. 0 = Input B selected, 1 = Input A selected.
24	GNDR	GND	Analog Ground pin for the differential input (receiver)
25	EPAD	GND	Connect to Ground.

Test Loads

Low-Power HCSL Output Test Load

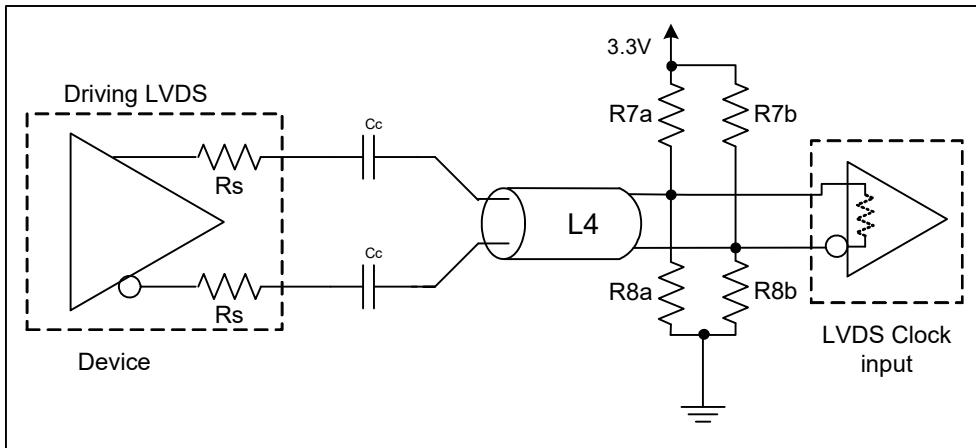


Low-Power HCSL Output

Alternate Differential Output Terminations

R_s	Z_o	Units
33	100	Ohms
27	85	

Driving LVDS



Driving LVDS inputs

Component	Value		Note
	Receiver has termination	Receiver does not have termination	
R_{7a}, R_{7b}	10K ohm	140 ohm	
R_{8a}, R_{8b}	5.6K ohm	75 ohm	
C_c	0.1 μF	0.1 μF	
V_{cm}	1.2 volts	1.2 volts	

Electrical Characteristics—Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V _{DDX}		-0.5		2.5	V	1,2
Input Voltage	V _{IN}		-0.5		V _{DD} +0.5	V	1,3
Input High Voltage, SMBus	V _{IHSMB}	SMBus clock and data pins			3.3	V	1
Storage Temperature	T _S		-65		150	°C	1
Junction Temperature	T _J				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

¹Guaranteed by design and characterization, not 100% tested in production.

² Operation under these conditions is neither implied nor guaranteed.

³ Not to exceed 2.5V.

Electrical Characteristics—Input/Supply/Common Parameters—Normal Operating Conditions

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V _{DDX}	Supply voltage for core and analog	1.7	1.8	1.9	V	
Ambient Operating Temperature	T _{AMB}	Industrial range	-40	25	85	°C	1
Input High Voltage	V _{IH}	Single-ended inputs, except SMBus	0.75 V _{DD}		V _{DD} + 0.3	V	
Input Low Voltage	V _{IL}	Single-ended inputs, except SMBus	-0.3		0.25 V _{DD}	V	
Input Current	I _{IN}	Single-ended inputs, V _{IN} = GND, V _{IN} = VDD	-5		5	uA	
	I _{INP}	Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	
Input Frequency	f _{in}		1		200	MHz	2
Pin Inductance	L _{pin}				7	nH	1
Capacitance	C _{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C _{INDIF IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C _{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T _{STAB}	From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1,2
Input SS Modulation Frequency PCIe	f _{MODINPCIE}	Allowable Frequency for PCIe Applications (Triangular Modulation)	30		33	kHz	
Input SS Modulation Frequency non-PCIe	f _{MODIN}	Allowable Frequency for non-PCIe Applications (Triangular Modulation)	0		66	kHz	
OE# Latency	t _{LATOE#}	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	clocks	1,3
Tfall	t _F	Fall time of single-ended control inputs			5	ns	2
Trise	t _R	Rise time of single-ended control inputs			5	ns	2

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

⁴ DIF_IN input

Electrical Characteristics—Clock Input Parameters

TA = T_{AMB} , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	V_{IHDF}	Differential inputs (single-ended measurement)	300	750	1150	mV	1
Input Low Voltage - DIF_IN	V_{LDIF}	Differential inputs (single-ended measurement)	$V_{SS} - 300$	0	300	mV	1
Input Common Mode Voltage - DIF_IN	V_{COM}	Common Mode Input Voltage	200		725	mV	1
Input Amplitude - DIF_IN	V_{SWING}	Peak to Peak value ($V_{IHDF} - V_{LDIF}$)	300		1450	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.35		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, $V_{IN} = GND$	-5		5	uA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform	45	50	55	%	1
Input Jitter - Cycle to Cycle	J_{DIFin}	Differential Measurement	0		150	ps	1

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics—DIF Low-Power HCSL Outputs

TA = T_{AMB} , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	dV/dt	Scope averaging on, fast setting	2.2	3.4	4.9	V/ns	1,2,3
Slew rate matching	$\Delta dV/dt$	Slew rate matching, Scope averaging on		3	20	%	1,2,4
Voltage High	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	789	850	mV	
Voltage Low	V_{LOW}		-150	38	150		
Max Voltage	V_{max}	Measurement on single ended signal using absolute value. (Scope averaging off)		829	1150	mV	
Min Voltage	V_{min}		-300	-20			
V_{swing}	V_{swing}	Scope averaging off	300	1501		mV	1,2
Crossing Voltage (abs)	V_{cross_abs}	Scope averaging off	250	419	550	mV	1,5
Crossing Voltage (var)	ΔV_{cross}	Scope averaging off		10	140	mV	1,6

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform

³ Slew rate is measured through the V_{swing} voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ V_{cross} is defined as voltage where $Clock = Clock\#$ measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all V_{cross} measurements in any particular system. Note that this is a subset of $V_{cross_min/max}$ (V_{cross} absolute) allowed. The intent is to limit V_{cross} induced modulation by setting ΔV_{cross} to be smaller than V_{cross} absolute.

Electrical Characteristics—Current Consumption

TA = T_{AMB} , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I_{DD}	VDD, All outputs active @100MHz		20	28	mA	1
Powerdown Current	I_{DDPD}	VDD, all outputs disabled		1.5	2.5	mA	1, 2

¹ Guaranteed by design and characterization, not 100% tested in production.

² Input clock stopped.

Electrical Characteristics—Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = T_{AMB} , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode @100MHz	-1	-0.15	1	%	1,3
Skew, Input to Output	t_{pdBYP}	Bypass Mode, $V_T = 50\%$	1819	2365	3075	ps	1
Skew, Output to Output	t_{sk3}	$V_T = 50\%$		16	50	ps	1,4
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Additive Jitter in Bypass Mode		0.1	5	ps	1,2

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform

³ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode

⁴ All outputs at default slew rate

⁵ The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

Electrical Characteristics—Phase Jitter Parameters

TA = T_{AMB} , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Additive Phase Jitter, Bypass Mode	$t_{jphPCleG1}$	PCIe Gen 1		1.3	5	N/A	ps (p-p)	1,2,3,5
	$t_{jphPCleG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.1	0.3	N/A	ps (rms)	1,2,3,4,5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.1	0.2	N/A	ps (rms)	1,2,3,4
	$t_{jphPCleG3}$	PCIe Gen 3 (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz)		0.065	0.1	N/A	ps (rms)	1,2,3,4
	$t_{jph125M0}$	125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		285	300	N/A	fs (rms)	1,6
	$t_{jph125M1}$	125MHz, 12KHz to 20MHz, -20dB/decade rollover < 12kHz, -40db/decade rolloff > 20MHz		420	450	N/A	fs (rms)	1,6

¹ Guaranteed by design and characterization, not 100% tested in production.

² See <http://www.pcisig.com> for complete specs

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = $\sqrt{(\text{total jitter})^2 - (\text{input jitter})^2}$

⁵ Driven by 9FGU0831 or equivalent

⁶ Rohde&Schartz SMA100

Marking Diagram



Notes:

1. "LOT" denotes the lot number.
2. "YYWW" is the last two digits of the year and week that the part was assembled.
3. Line 2: truncated part number
4. "L" denotes RoHS compliant package.
5. "I" denotes industrial temperature grade.

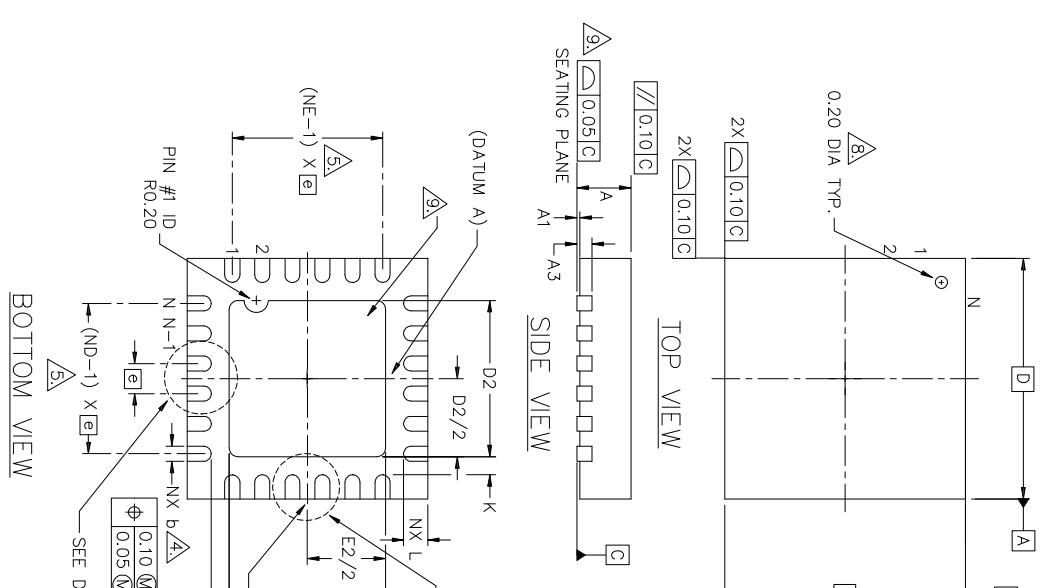
Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP VALUE	UNITS	NOTES
Thermal Resistance	θ_{JC}	Junction to Case	NLG24	42	°C/W	1
	θ_{Jb}	Junction to Base		2.4	°C/W	1
	θ_{JA0}	Junction to Air, still air		39	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		33	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		28	°C/W	1
	θ_{JA5}	Junction to Air, 5 m/s air flow		27	°C/W	1

¹ePad soldered to board

Package Outline and Package Dimensions (NLG24)

MIN.	NOM.	MAX.	
② 0.50 BSC.	24		
N 6			
NE 6			
L 0.30	0.40	0.50	
b 0.18	0.25	0.30	
D2 2.30	2.45	2.60	
E2 2.30	2.45	2.60	



MIN.	NOM.	MAX.		
② 0.50 BSC.	24			
A 0.00	0.02	0.05		
A3 0.20 REF.				
② 0	12	2		
K 0.20 MIN.				
D 4.0 BSC				
E 4.0 BSC				
L1 0.15 mm MAX				

BOTTOM VIEW

NOTES :

1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M - 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.

4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

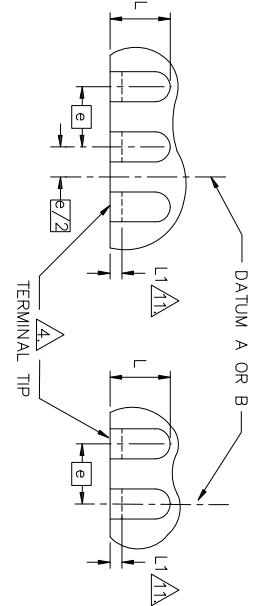
6. MAX. PACKAGE WARPAGE IS 0.05 mm.

7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.

8. PIN #1 ID ON TOP WILL BE LASER MARKED.

9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

10. THIS DRAWING CONFORMS TO JEDEC REGISTERED OUTLINE MO-220
- A1 DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULLBACK (L¹) MAYBE PRESENT
- A2 PULLBACK DESIGN OPTION IS FOR 0.50mm NOMINAL LANDLENGTH ONLY.



REVIEWS			
REV	DESCRIPTION	DATE	APPF
00	INITIAL RELEASE	10/15/08	R
01	ADD LAND PATTERN	11/19/10	J



6024 Silver Creek, Vall
San Jose, CA 95138

PHONE: (408) 284-8591
FAX: (408) 284-8591

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APPROVALS DATE TITLE NL/NLG24 PACKAGE OUTLINE

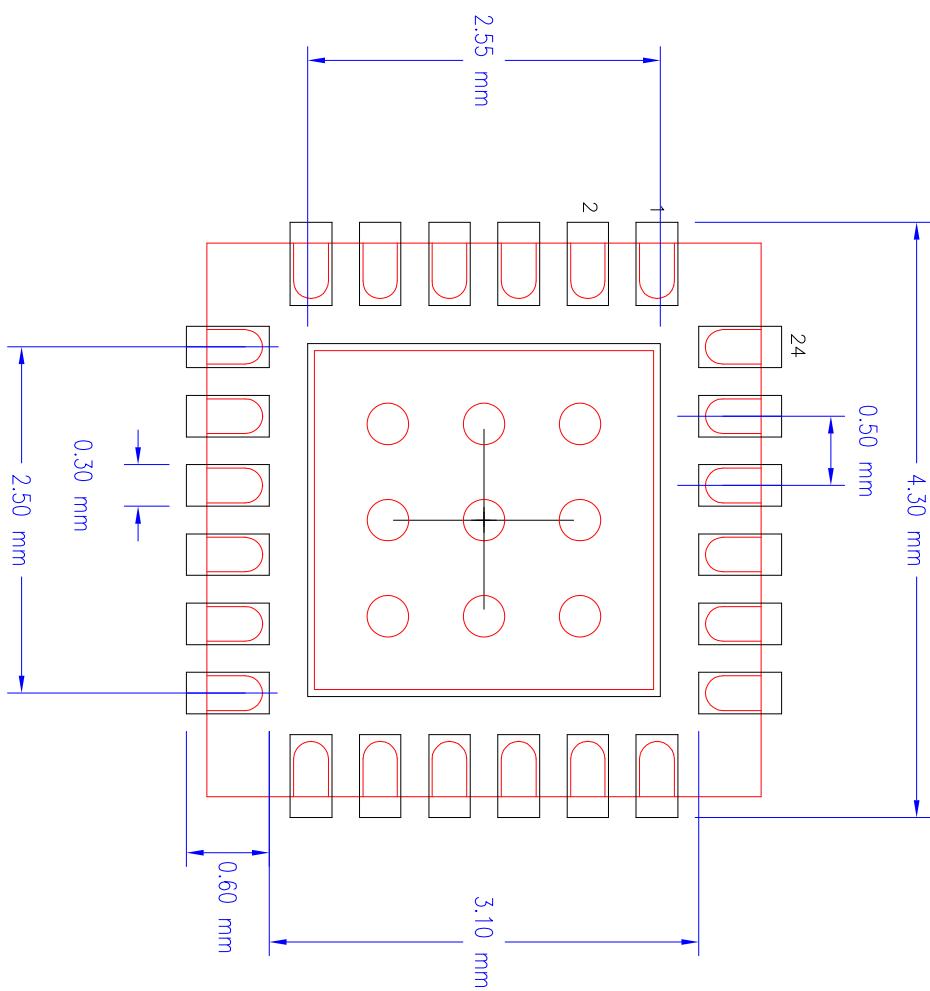
DRAWN BY C 10/15/08 4.0 x 4.0 mm BODY

CHECKED 0.5 mm PITCH QFN

SIZE C DRAWING NO. PSC-4192

Package Outline and Package Dimensions, cont. (NLG24)

NL24 RECOMMENDED FOOTPRINT 2.45 mm SQ EPAD



TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX±		REV. 6024 Silver Creek Valley R www.IDT.com PHONE: (408) 284-8200 FAX: (408) 284-8591	
APPROVALS	DATE	TITLE	NL/NLG24 PACKAGE OUTLINE
DRAWN <i>jj</i>	11/19/10	4.0 x 4.0 mm BODY 0.5 mm PITCH VQFPN	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVE
00	INITIAL RELEASE	11/19/10	JG
01	ADD LAND PATTERN	11/19/10	JG

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9DMV0431AKILF	Tubes	24-pin VFQFPN	-40 to +85° C
9DMV0431AKILFT	Tape and Reel	24-pin VFQFPN	-40 to +85° C

"LF" to the suffix denotes Pb-Free configuration, RoHS compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Initiator	Issue Date	Description	Page #
A	RDW	9/24/2014	1. Updated Electrical Tables with Char data 2. Updated General Description 3. Move to final	Various
B	RDW	1/26/2015	Updated package drawing and dimensions	9

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