

15 Output PCIe G2/QPI Differential Buffer with 2:1 Input Mux

9EX21501A

Description

The **ICS9EX21501** provides 15 output clocks for PCIe Gen2 (100MHz) or QPI (133MHz) applications. A differential CPU clock from a CK410B+ main clock generator, such as the ICS932S421, drives the **ICS9EX21501**. In fanout mode, the **ICS9EX21501** provides outputs up to 400MHz. A 2:1 input mux allows selection between local and remote clock sources.

Recommended Application:

15 Output PCIe G2/QPI Differential Buffer with 2:1 input mux

Key Specifications:

- DIF output cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 150 ps
- PCIe Gen2 compliant phase jitter
- QPI 6.4Gb/s 12UI compliant phase jitter

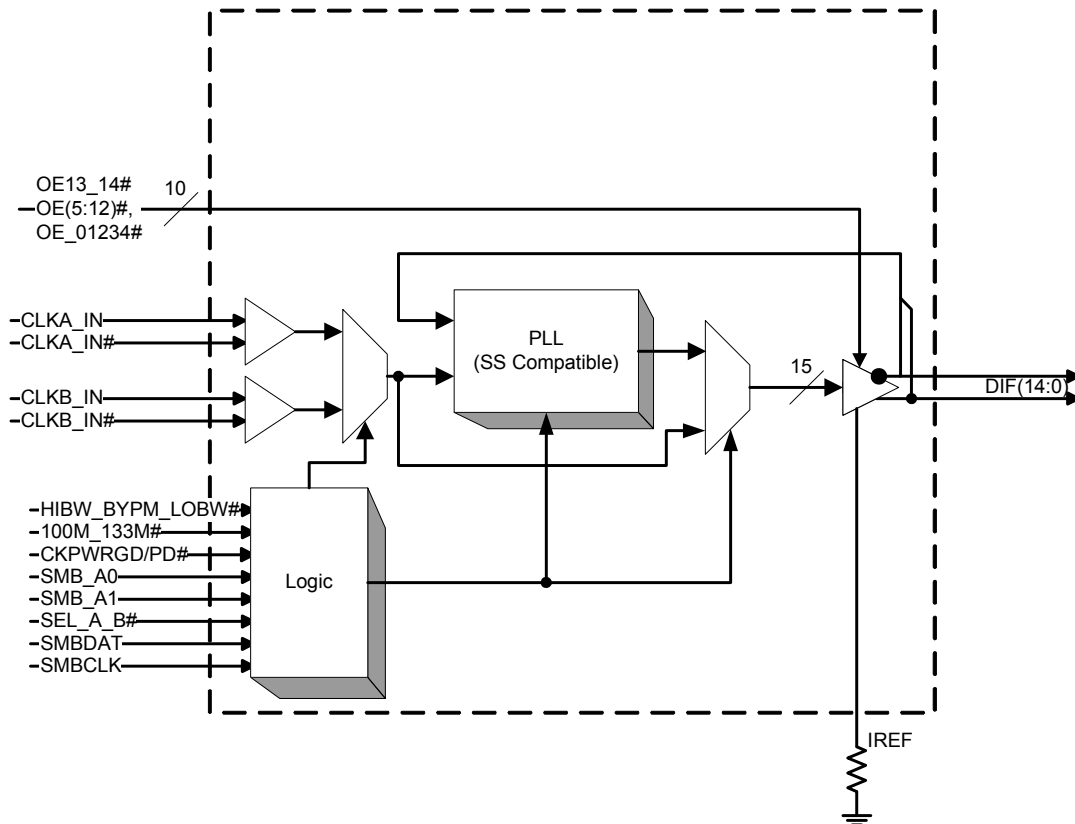
Features/Benefits:

- Output clock frequencies up to 400 MHz/supports wide range of applications
- 4 Selectable SMBus addresses/multiple devices can share SMBus segment
- SMBus address independent of PLL operating mode/maximum flexibility
- Dedicated CKPWRGD/PD# and VDDA pins/Easy board design
- 8 Dedicated OE# and 2 Group OE# pins/Support for hardware clock management

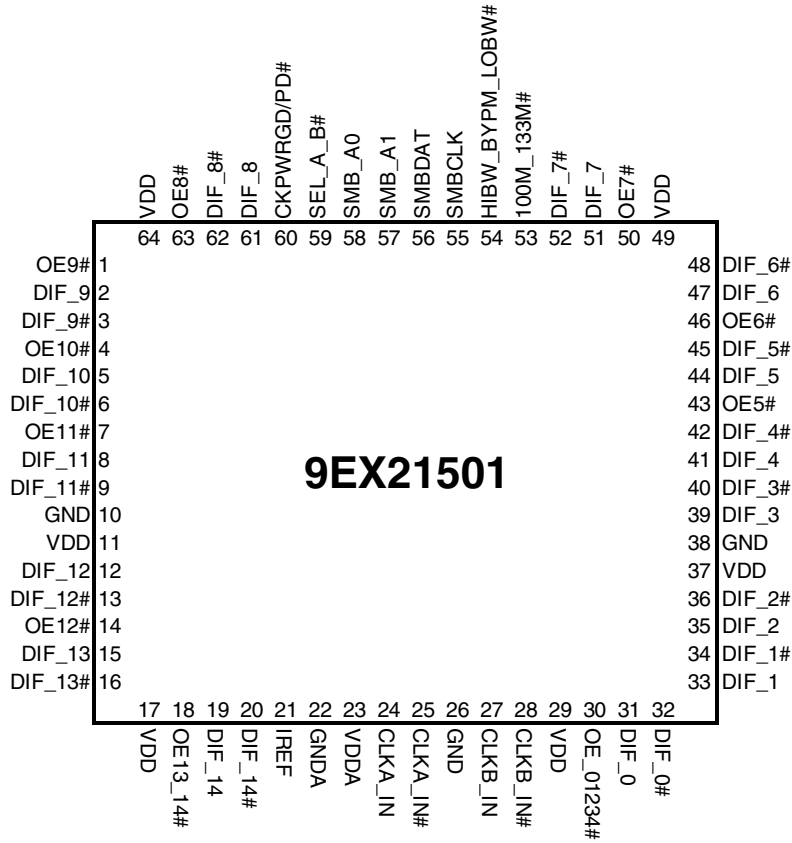
Output Features:

- 15 - 0.7V current-mode differential HCSL output pairs
- Supports zero delay buffer mode and fanout mode
- Selectable PLL bandwidth
- 80-150 MHz in PLL Mode
- 33-400 MHz operation in Bypass mode

Functional Block Diagram



Pin Configuration



9EX21501

64-pin MLF

Frequency/Functionality Table

| Byte 0, bit 2 (100_133M# Latch) | Byte 0, bit 1 FSB | Byte 0, bit 0 FSA | Input MHz | DIF_x MHz | Notes |
|---------------------------------|-------------------|-------------------|-----------|-----------|-------|
| 1 | 0 | 1 | 100.00 | 100.00 | 1 |
| 0 | 0 | 1 | 133.33 | 133.33 | 1 |
| 0 | 1 | 1 | 166.67 | 166.67 | 2 |
| 0 | 1 | 0 | 200.00 | 200.00 | 2 |
| 0 | 0 | 0 | 266.67 | 266.67 | 2 |
| 1 | 0 | 0 | 333.33 | 333.33 | 2 |
| 1 | 1 | 0 | 400.00 | 400.00 | 2 |
| 1 | 1 | 1 | Reserved | | |

Notes:100M_133M#

- Latch selects between 100 and 133 MHz. This is equivalent to FSC in CK410B+/CK509B FS table.
- Writing Byte 2 bits (2:0) can select other frequencies. These frequencies are not characterized in PLL Mode

HIBW_BYPM_LOBW# Selection (Pin 54)

| State | Voltage | Mode |
|-------|--------------|---------|
| Low | <0.8V | Low BW |
| Mid | 1.2<Vin<1.8V | Bypass |
| High | Vin > 2.0V | High BW |

Power Groups

| Pin Number | | Description |
|-----------------|--------|------------------|
| VDD | GND | |
| 23 | 22 | Main PLL, Analog |
| 29 | 26 | Input buffers |
| 11,17,37,49, 64 | 10, 38 | DIF clocks |

Power Down Functionality

| INPUTS | | OUTPUTS | PLL State |
|-------------|---------|---------|-----------|
| CKPWRGD/PD# | Input | DIF_x | |
| 1 | Running | Running | ON |
| 0 | X | Hi-Z | OFF |

SMBus Address Selection (pins 57, 58)

| SMB_A1 | SMB_A0 | Address |
|--------|--------|---------|
| 0 | 0 | D4 |
| 0 | 1 | D6 |
| 1 | 0 | D8 |
| 1 | 1 | DA |

Pin Description

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|-----------|------|---|
| 1 | OE9# | IN | Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs |
| 2 | DIF_9 | OUT | 0.7V differential true clock output |
| | DIF_9# | OUT | 0.7V differential complement clock output |
| 4 | OE10# | IN | Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs |
| 5 | DIF_10 | OUT | 0.7V differential true clock output |
| 6 | DIF_10# | OUT | 0.7V differential complement clock output |
| 7 | OE11# | IN | Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs |
| 8 | DIF_11 | OUT | 0.7V differential true clock output |
| 9 | DIF_11# | OUT | 0.7V differential complement clock output |
| 10 | GND | PWR | Ground pin. |
| 11 | VDD | PWR | Power supply, nominal 3.3V |
| 12 | DIF_12 | OUT | 0.7V differential true clock output |
| 13 | DIF_12# | OUT | 0.7V differential complement clock output |
| 14 | OE12# | IN | Active low input for enabling DIF pair 12. 1 = tri-state outputs, 0 = enable outputs |
| 15 | DIF_13 | OUT | 0.7V differential true clock output |
| 16 | DIF_13# | OUT | 0.7V differential complement clock output |
| 17 | VDD | PWR | Power supply, nominal 3.3V |
| 18 | OE13_14# | IN | Active low input for enabling DIF pairs 13 and 14. 1 = tri-state outputs, 0 = enable outputs |
| 19 | DIF_14 | OUT | 0.7V differential true clock output |
| 20 | DIF_14# | OUT | 0.7V differential complement clock output |
| 21 | IREF | OUT | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 22 | GND | PWR | Ground pin for the PLL core. |
| 23 | VDDA | PWR | 3.3V power for the PLL core. |
| 24 | CLKA_IN | IN | True Input for differential reference clock. |
| 25 | CLKA_IN# | IN | Complement Input for differential reference clock. |
| 26 | GND | PWR | Ground pin. |
| 27 | CLKB_IN | IN | True Input for differential reference clock. |
| 28 | CLKB_IN# | IN | Complement Input for differential reference clock. |
| 29 | VDD | PWR | Power supply, nominal 3.3V |
| 30 | OE_01234# | IN | Active low input for enabling DIF pairs 0, 1, 2, 3 and 4. 1 = tri-state outputs, 0 = enable outputs |
| 31 | DIF_0 | OUT | 0.7V differential true clock output |
| 32 | DIF_0# | OUT | 0.7V differential complement clock output |
| 33 | DIF_1 | OUT | 0.7V differential true clock output |
| 34 | DIF_1# | OUT | 0.7V differential complement clock output |
| 35 | DIF_2 | OUT | 0.7V differential true clock output |
| 36 | DIF_2# | OUT | 0.7V differential complement clock output |
| 37 | VDD | PWR | Power supply, nominal 3.3V |
| 38 | GND | PWR | Ground pin. |
| 39 | DIF_3 | OUT | 0.7V differential true clock output |
| 40 | DIF_3# | OUT | 0.7V differential complement clock output |

Pin Description (continued)

| | | | |
|----|-----------------|-----|--|
| 41 | DIF_4 | OUT | 0.7V differential true clock output |
| 42 | DIF_4# | OUT | 0.7V differential complement clock output |
| 43 | OE5# | IN | Active low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs |
| 44 | DIF_5 | OUT | 0.7V differential true clock output |
| 45 | DIF_5# | OUT | 0.7V differential complement clock output |
| 46 | OE6# | IN | Active low input for enabling DIF pair 6. 1 = tri-state outputs, 0 = enable outputs |
| 47 | DIF_6 | OUT | 0.7V differential true clock output |
| 48 | DIF_6# | OUT | 0.7V differential complement clock output |
| 49 | VDD | PWR | Power supply, nominal 3.3V |
| 50 | OE7# | IN | Active low input for enabling DIF pair 7. 1 = tri-state outputs, 0 = enable outputs |
| 51 | DIF_7 | OUT | 0.7V differential true clock output |
| 52 | DIF_7# | OUT | 0.7V differential complement clock output |
| 53 | 100M_133M# | IN | Input to select operating frequency. See Frequency/Functionality Table for functionality of this pin. |
| 54 | HIBW_BYPM_LOBW# | IN | Trilevel input to select High BW, Bypass Mode or Low BW. 0 = Low BW Mode, Mid= Bypass Mode, 1 = High Bandwidth |
| 55 | SMBCLK | IN | Clock pin of SMBUS circuitry, 5V tolerant |
| 56 | SMBDAT | I/O | Data pin of SMBUS circuitry, 5V tolerant |
| 57 | SMB_A1 | IN | SMBus address bit 1 |
| 58 | SMB_A0 | IN | SMBus address bit 0 (LSB) |
| 59 | SEL_A_B# | IN | Input to select differential input clock A or differential input clock B. 0 = Input B selected, 1 = Input A selected. |
| 60 | CKPWRGD/PD# | IN | Notifies the clock to sample latched inputs on the rising edge, and to power down on the falling edge. |
| 61 | DIF_8 | OUT | 0.7V differential true clock output |
| 62 | DIF_8# | OUT | 0.7V differential complement clock output |
| 63 | OE8# | IN | Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs |
| 64 | VDD | PWR | Power supply, nominal 3.3V |

Electrical Characteristics - Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage | VDDA | | | | 4.6 | V | 1,2 |
| 3.3V Logic Supply Voltage | VDD | | | | 4.6 | V | 1,2 |
| Input Low Voltage | V _{IL} | | GND-0.5 | | | V | 1 |
| Input High Voltage | V _{IH} | Except for SMBus interface | | | V _{DD} +0.5V | V | 1 |
| Input High Voltage | V _{IHSMB} | SMBus clock and data pins | | | 5.5V | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics - Clock Input Parameters

TA = T_{COM} or T_{IND}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------------------|--------------------|---|-----------------------|-----|------|-------|-------|
| Input High Voltage - DIF_IN | V _{IHDIF} | Differential inputs (single-ended measurement) | 600 | 800 | 1150 | mV | 1 |
| Input Low Voltage - DIF_IN | V _{ILDIF} | Differential inputs (single-ended measurement) | V _{SS} - 300 | 0 | 300 | mV | 1 |
| Input Common Mode Voltage - DIF_IN | V _{COM} | Common Mode Input Voltage | 300 | 400 | 1000 | mV | 1 |
| Input Amplitude - DIF_IN | V _{SWING} | Peak to Peak value | 300 | 750 | 1450 | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | 2 | 8 | V/ns | 1,2 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | uA | 1 |
| Input Duty Cycle | d _{tin} | Measurement from differential waveform | 45 | 50 | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | J _{DIFIn} | Differential Measurement | 0 | 50 | 125 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics - Phase Jitter Parameters

TA = T_{COM} or T_{IND}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---------------------------------------|------------------------|--|-----|-----------|-----|-------------|---------|
| Phase Jitter, PLL Mode | t _{jphPCleG1} | PCIe Gen 1 | | 32/42 | 86 | ps (p-p) | 1,2,3,4 |
| | t _{jphPCleG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 1.2/1.5 | 3 | ps (rms) | 1,2,4 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 2.1/2.7 | 3.1 | ps (rms) | 1,2,4 |
| | t _{jphQPI} | QPI (133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.25/0.28 | 0.5 | ps (rms) | 1,4,5 |
| Additive Phase Jitter, Bypass mode | t _{jphPCleG1} | PCIe Gen 1 | | 2 | 10 | ps (p-p) | 1,2,3 |
| | t _{jphPCleG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.0 | 0.3 | ps (rms) | 1,2,6 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 0.30 | 0.5 | ps (rms) | 1,2,6 |
| | t _{jphQPI} | QPI (133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.25 | 0.4 | ps (rms) | 1,5,6 |

¹Applies to all outputs. Device driven by IDT CK410B+ (932S421CGLF) or equivalent

²See <http://www.pcisiq.com> for complete specs

³Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴First number is Low BW, second number is Hi BW.

⁵Calculated from Intel-supplied Clock Jitter Tool v 1.6.4, with 7.8M rolloff

⁶For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)² = (total jitter)² - (input jitter)²

Electrical Characteristics - Input/Supply/Common Parameters

TA = T_{COM} or T_{IND}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-------------------------------|-----------------------|---|-----------|--------|-----------------------|--------|-------|
| Ambient Operating Temperature | T _{COM} | Commercial range | 0 | 25 | 70 | °C | 1 |
| | T _{IND} | Industrial range | -40 | 25 | 85 | °C | 1 |
| Input High Voltage | V _{IH} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | 2 | 2.400 | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{IL} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | GND - 0.3 | 0.400 | 0.8 | V | 1 |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = VDD | -5 | | 5 | uA | 1 |
| | I _{INP} | Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors | -200 | | 200 | uA | 1 |
| Input Frequency | F _{ibyp} | V _{DD} = 3.3 V, Bypass mode | 33 | | 400 | MHz | 2 |
| | F _{ipll} | V _{DD} = 3.3 V, 100MHz PLL mode | 80 | 100.00 | 110 | MHz | 2 |
| | F _{ipll} | V _{DD} = 3.3 V, 133.33MHz PLL mode | 120 | 133.33 | 150 | MHz | 2 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | C _{INDIF_IN} | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,4 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | 0.5 | 1 | ms | 1,2 |
| Input SS Modulation Frequency | f _{MODIN} | Allowable Frequency (Triangular Modulation) | 30 | | 33 | kHz | 1 |
| OE# Latency | t _{LATOE#} | DIF start after OE# assertion DIF stop after OE# deassertion | 4 | 10 | 12 | clocks | 1,3 |
| Tdrive_PD# | t _{DRVPD} | DIF output enable after PD# de-assertion | | 0.2 | 300 | us | 1,3 |
| Tfall | t _F | Fall time of control inputs | | | 5 | ns | 1,2 |
| Trise | t _R | Rise time of control inputs | | | 5 | ns | 1,2 |
| SMBus Input Low Voltage | V _{ILSMB} | | | 0.4 | 0.8 | V | 1 |
| SMBus Input High Voltage | V _{IHSMB} | | 2.1 | 2.4 | V _{DD} SMB | V | 1 |
| SMBus Output Low Voltage | V _{OLSMB} | @ I _{PULLUP} | | 0.3 | 0.4 | V | 1 |
| SMBus Sink Current | I _{PULLUP} | @ V _{OL} | 4 | 5 | | mA | 1 |
| Nominal Bus Voltage | V _{DD} SMB | 3V to 5V +/- 10% | 2.7 | 3.3 | 5.5 | V | 1 |
| SCLK/SDATA Rise Time | t _{RSMB} | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t _{FSMB} | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{MAXSMB} | Maximum SMBus operating frequency | | 400 | 100 | kHz | 1,5 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

⁴DIF_IN input

⁵The differential input clock must be running for the SMBus to be active. Tested at Fin=100MHz.

Electrical Characteristics - DIF 0.7V Current Mode Differential OutputsTA = T_{COM} or T_{IND}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------|---|------|------|------|-------|---------|
| Slew rate | Trf | Scope averaging on | 1 | 2.2 | 4 | V/ns | 1, 2, 3 |
| Slew rate matching | ΔTrf | Slew rate matching, Scope averaging on | | 11 | 20 | % | 1, 2, 4 |
| Voltage High | VHigh | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 772 | 850 | mV | 1 |
| Voltage Low | VLow | | -150 | 10 | 150 | | 1 |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. (Scope averaging) | | 870 | 1150 | mV | 1 |
| Min Voltage | Vmin | | -300 | -47 | | | 1 |
| Vswing | Vswing | Scope averaging off | 300 | 1390 | | mV | 1, 2 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 250 | 360 | 550 | mV | 1, 5 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off | | 14 | 140 | mV | 1, 6 |

¹Guaranteed by design and characterization, not 100% tested in production. IREF = VDD/(3xR_R). For R_R = 475Ω (1%), IREF = 2.32mA.I_{OH} = 6 x IREF and V_{OH} = 0.7V @ Z_O=50Ω (100Ω differential impedance).²Measured from differential waveform³Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.⁴Matching applies to rising edge rate of Clock / falling edge rate of Clock#. It is measured in a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations.⁵Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).⁶The total variation of all Vcross measurements in any system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross absolute.**Electrical Characteristics - Current Consumption**TA = T_{COM} or T_{IND}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---------------------------|---|-----|-----|-----|-------|-------|
| VDD Operating Current, Commercial Temp | I _{DD3.3VDDOP} | TA - T _{COM} , All outputs active <200MHz | | 306 | 330 | mA | 1 |
| | I _{DD3.3VDDOP} | TA - T _{COM} , All outputs active >=200MHz | | 360 | 390 | mA | 1 |
| VDDA Operating Current, Commercial Temp | I _{DD3.3VDDAOP} | TA - T _{COM} , All outputs active <200MHz | | 29 | 36 | mA | 1 |
| | I _{DD3.3VDDAOP} | TA - T _{COM} , All outputs active >=200MHz | | 29 | 36 | mA | 1 |
| VDD Powerdown Current, Commercial Temp | I _{DD3.3VDDPDZ} | TA = T _{COM} , All differential pairs Hi-Z | | 12 | 15 | mA | 1 |
| VDDA Powerdown Current, Commercial Temp | I _{DD3.3VDDAPDZ} | TA = T _{COM} , All differential pairs Hi-Z | | 15 | 20 | mA | 1 |
| VDD Operating Current, Industrial Temp | I _{DD3.3VDDOP} | TA - T _{IND} , All outputs active <200MHz | | 325 | 350 | mA | 1 |
| | I _{DD3.3VDDAOP} | TA - T _{IND} , All outputs active >=200MHz | | 390 | 420 | mA | 1 |
| VDDA Operating Current, Industrial Temp | I _{DD3.3VDDOP} | TA - T _{IND} , All outputs active >=200MHz | | 33 | 40 | mA | 1 |
| | I _{DD3.3VDDAOP} | TA - T _{IND} , All outputs active >=200MHz | | 33 | 40 | mA | 1 |
| VDD Powerdown Current, Industrial Temp | I _{DD3.3VDDPDZ} | TA = T _{IND} , All differential pairs Hi-Z | | 15 | 20 | mA | 1 |
| VDDA Powerdown Current, Industrial Temp | I _{DD3.3VDDAPDZ} | TA = T _{IND} , All differential pairs Hi-Z | | 16 | 20 | mA | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Skew and Differential Jitter Parameters

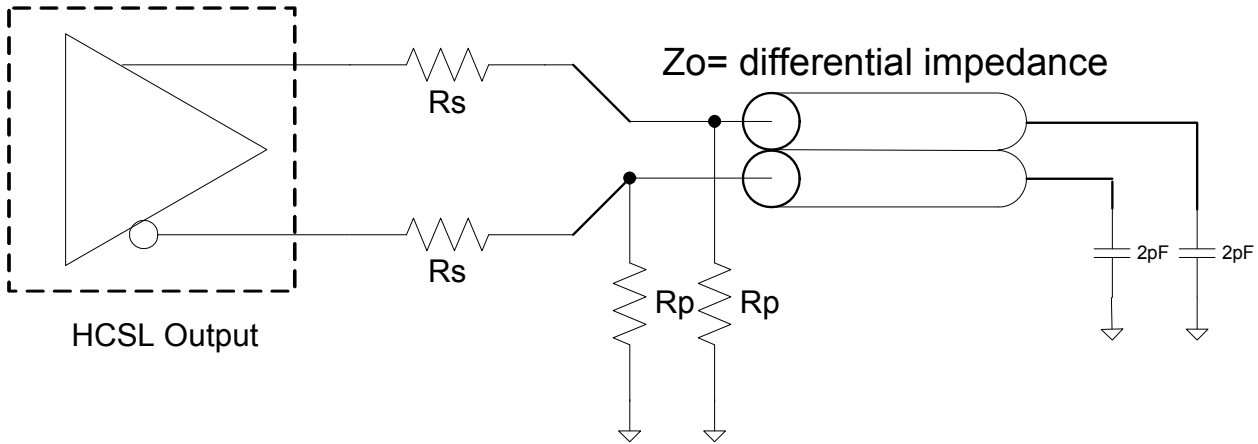
TA = T_{COM} or T_{IND}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|----------------------------------|---|------|-------|-------|----------|--------------|
| CLK_IN, DIF[x:0], 100M | t _{SPO_PLL100M} | Input-to-Output Skew in PLL mode nominal value @ 25°C, 3.3V | 925 | 1019 | 1125 | ps | 1,2,4,5,8 |
| CLK_IN, DIF[x:0], 133M | t _{SPO_PLL133M} | Input-to-Output Skew in PLL mode nominal value @ 25°C, 3.3V | 1100 | 1120 | 1200 | ps | 1,2,4,5,8 |
| CLK_IN, DIF[x:0] | t _{PD_BYP} | Input-to-Output Skew in Bypass mode nominal value @ 25°C, 3.3V | 4 | 4.6 | 5.2 | ns | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DSPO_PLL} | Input-to-Output Skew Variation in PLL mode across voltage and temperature | | 12581 | 13501 | ps | 1,2,3,5,6,8 |
| CLK_IN, DIF[x:0] | t _{DSPO_BYP} | Input-to-Output Skew Variation in Bypass mode across voltage and temperature | | 17711 | 19001 | ps | 1,2,3,5,6,8 |
| CLK_IN, DIF[x:0] | t _{DTE} | Random Differential Tracking error between two 9EX2 devices in Hi BW Mode | | 2 | 10 | ps (rms) | 1,2,3,5,8,12 |
| CLK_IN, DIF[x:0] | t _{DSSTE} | Random Differential Spread Spectrum Tracking error between two 9EX2 devices in Hi BW Mode | | 20 | 75 | ps | 1,2,3,5,8,13 |
| DIF[x:0] | t _{SKREW_ALL} | Output-to-Output Skew across all outputs (Common to Bypass and PLL mode) | | 75 | 150 | ps | 1,2,8 |
| PLL Jitter Peaking | j _{peak-hibw} | High Bandwidth | 0 | 2.3 | 3 | dB | 7,8 |
| PLL Jitter Peaking | j _{peak-lobw} | Low Bandwidth | 0 | 2.5 | 3 | dB | 7,8 |
| PLL Bandwidth | pll _{HIBW} | High Bandwidth | 2 | 2.5 | 4 | MHz | 8,9 |
| PLL Bandwidth | pll _{LOBW} | Low Bandwidth | 0.7 | 0.87 | 1.4 | MHz | 8,9 |
| Duty Cycle | t _{DC} | Measured differentially, PLL Mode | 45 | 49.6 | 55 | % | 1 |
| Duty Cycle Distortion | t _{DCD} | Measured differentially, Bypass Mode @100MHz | -2 | 0.2 | 2 | % | 1,10 |
| Jitter, Cycle to cycle | t _{j_{cyc-cyc}} | PLL mode | | 27 | 50 | ps | 1 |
| | | Additive Jitter in Bypass Mode | | 20 | 50 | ps | 1 |

Notes for preceding table:

- Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
- Measured from differential cross-point to differential cross-point.
- All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
- This parameter is deterministic for a given device
- Measured with scope averaging on to find mean value.
- Long-term variation from nominal of input-to-output skew over temperature and voltage for a single device.
- Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
- Guaranteed by design and characterization, not 100% tested in production.
- Measured at 3 db down or half power point.
- Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode
- Measured from differential waveform
- This parameter is measured at the outputs of two separate ICS9EX21501 devices driven by a single CK410B+. The ICS9EX21501's must be set to high bandwidth. Differential phase jitter is the accumulation of the phase jitter not shared by the outputs (eg. not including the affects of spread spectrum). Target ranges of consideration are agents with BW of 1-22Mhz and 11-33Mhz.
- Differential spread spectrum tracking error is the difference in spread spectrum tracking between two ICS9EX21501 devices. This parameter is measured at the outputs of two separate ICS9EX21501 devices driven by a single CK410B+ in Spread Spectrum mode. The ICS9EX21501's must be set to high bandwidth. The spread spectrum characteristics are: maximum of 0.5%, 30-33KHz modulation frequency, triangle profile.

HCSL Differential Output Test Load



Differential Output Termination Table

| DIF Zo (Ω) | Iref (Ω) | Rs (Ω) | Rp (Ω) | C _L (pF) |
|---------------------|-------------------|-----------------|-----------------|---------------------|
| 100 | 475 | 33 | 50 | 2 |
| 85 | 412 | 27 | 43.2 | 2 |

← Test Load

General SMBus serial interface information for the 9EX21501

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D4_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

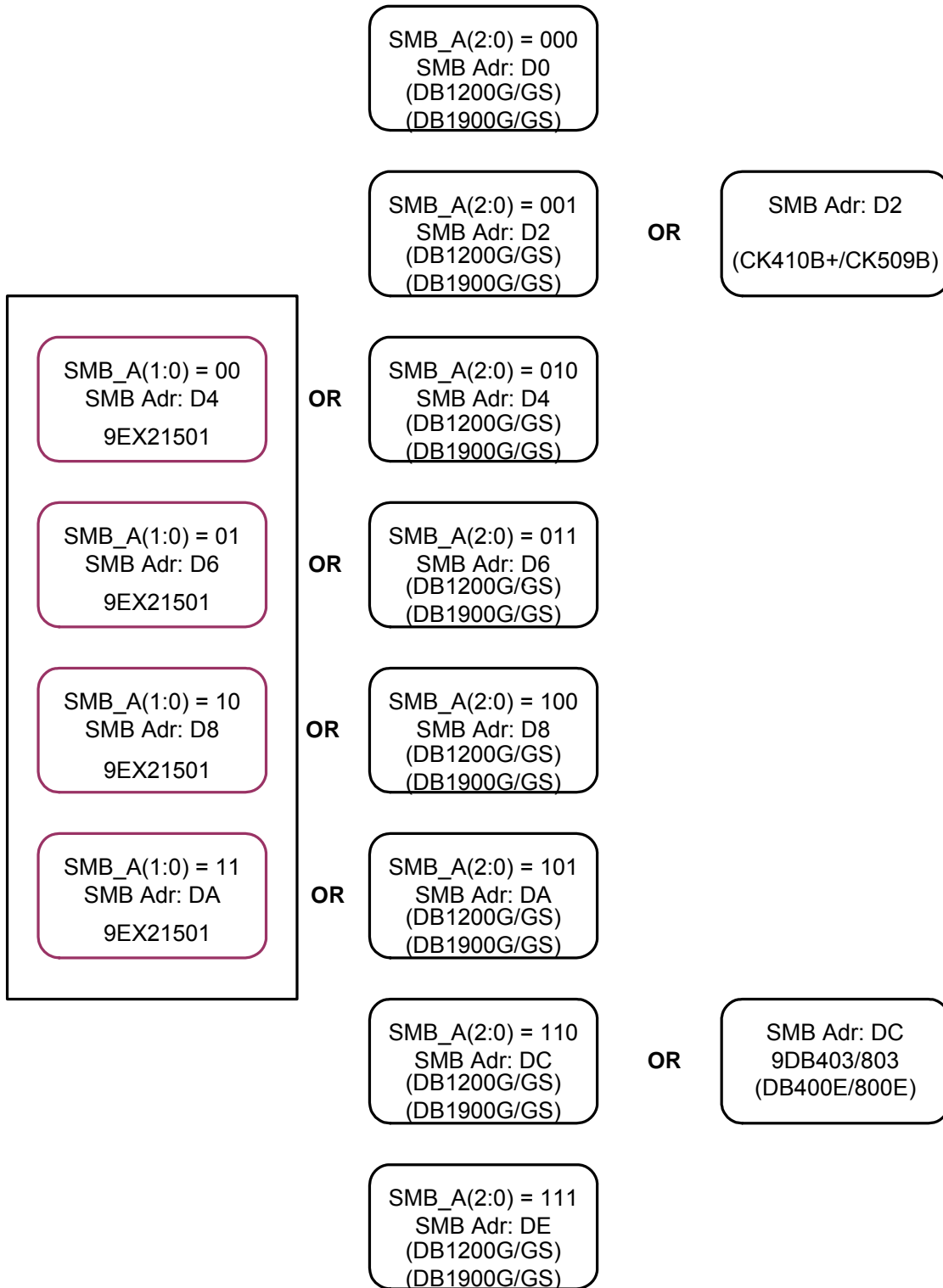
- Controller (host) will send start bit.
- Controller (host) sends the write address D4_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D5_(H)
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if X_(H) was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation | | |
|---------------------------------|-----------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address D4 _(H) | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | X Byte | ACK |
| ◊ | | ◊ |
| ◊ | | ◊ |
| ◊ | | ◊ |
| Byte N + X - 1 | | ◊ |
| | | ACK |
| P | stoP bit | |

| Index Block Read Operation | | | |
|---------------------------------|-----------------|----------------------|------------------|
| Controller (Host) | | ICS (Slave/Receiver) | |
| T | starT bit | | |
| Slave Address D4 _(H) | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| RT | Repeat starT | | |
| Slave Address D5 _(H) | | | |
| RD | ReaD | | |
| | | ACK | |
| | | Data Byte Count = X | |
| ACK | | | |
| | | X Byte | |
| ACK | | | Beginning Byte N |
| ◊ | | | ◊ |
| ◊ | | | ◊ |
| ◊ | | | ◊ |
| | | Byte N + X - 1 | |
| N | Not acknowledge | | |
| P | stoP bit | | |

Note: SMBus address is selectable among 4 addresses. See tabel on page 2.

9EX21501 SMBus Addressing



SMBusTable: Output, and PLL BW Control Register

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-------------------------|------------------------|------|-----------------------------------|--------|---------|
| Bit 7 | 54 | PLL_BW# adjust | | RW | 00 = Low BW (1MHz) 10 = Bypass | | Latch |
| Bit 6 | | BYPASS# test mode / PLL | | RW | 11 = High BW (3MHz) | | Latch |
| Bit 5 | | RESERVED | | | | | 1 |
| Bit 4 | | DIF_14 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 3 | | RESERVED | | | | | 0 |
| Bit 2 | - | 100M_133M# | Frequency Select Bit C | RW | 133MHz | 100MHz | Latch |
| Bit 1 | - | FSB | Frequency Select Bit B | RW | See Frequency Select | | 0 |
| Bit 0 | - | FSA | Frequency Select bit A | RW | Table | | 1 |

SMBusTable: Output Control Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------|------|------|--------|---------|
| Bit 7 | | RESERVED | | | | | 1 |
| Bit 6 | | DIF_6 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 5 | | DIF_5 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 4 | | DIF_4 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 3 | | DIF_3 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 2 | | DIF_2 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 1 | | DIF_1 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 0 | | DIF_0 | Output Control | RW | Hi-Z | Enable | 1 |

SMBusTable: Output Control Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------|------|------|--------|---------|
| Bit 7 | | DIF_13 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 6 | | RESERVED | | | | | 1 |
| Bit 5 | | DIF_12 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 4 | | DIF_11 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 3 | | DIF_10 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 2 | | DIF_9 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 1 | | DIF_8 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 0 | | DIF_7 | Output Control | RW | Hi-Z | Enable | 1 |

SMBusTable: Output Enable Readback Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-----------------|------------------|------|---------|--------|---------|
| Bit 7 | 4 | OE10# Input | Pin Readback | R | Pin Low | Pin Hi | X |
| Bit 6 | 1 | OE9# Input | Pin Readback | R | Pin Low | Pin Hi | X |
| Bit 5 | 63 | OE8# Input | Pin Readback | R | Pin Low | Pin Hi | X |
| Bit 4 | 50 | OE7# Input | Pin Readback | R | Pin Low | Pin Hi | X |
| Bit 3 | | RESERVED | | | | | 1 |
| Bit 2 | 46 | OE6# Input | Pin Readback | R | Pin Low | Pin Hi | X |
| Bit 1 | 43 | OE5# Input | Pin Readback | R | Pin Low | Pin Hi | X |
| Bit 0 | 30 | OE_01234# Input | Pin Readback | R | Pin Low | Pin Hi | X |

SMBusTable: Output Enable Readback Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------------------|------------------|------|---------|---------|---------|
| Bit 7 | | | RESERVED | | | | 0 |
| Bit 6 | | | RESERVED | | | | 0 |
| Bit 5 | | 100M_133M# Input | Pin Readback | R | 133M | 100M | X |
| Bit 4 | | SEL_A_B# Input | Pin Readback | R | Input B | Input A | X |
| Bit 3 | 18 | OE13_14# Input | Pin Readback | R | Pin Low | Pin Hi | X |
| Bit 2 | | | RESERVED | | | | 1 |
| Bit 1 | 14 | OE12# Input | Pin Readback | R | Pin Low | Pin Hi | X |
| Bit 0 | 7 | OE11# Input | Pin Readback | R | Pin Low | Pin Hi | X |

Note: For an output to be enabled, BOTH the Output Enable Bit and the OE# pin must be enabled. This means that the Output Enable Bit must be '1' and the corresponding OE# pin must be '0'.

SMBusTable: Vendor & Revision ID Register

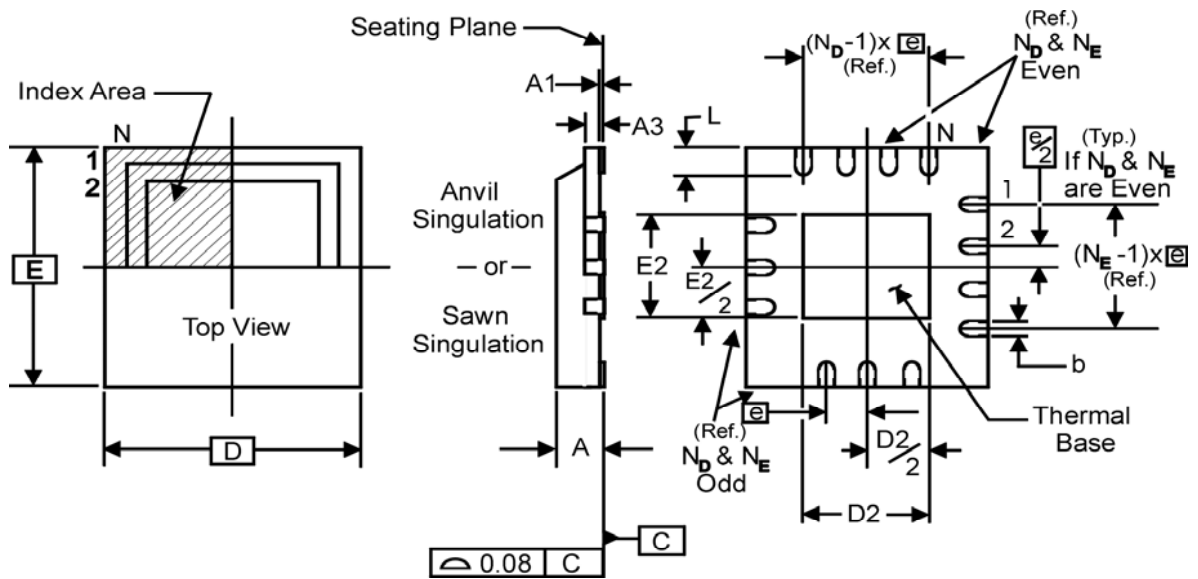
| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | - | RID3 | REVISION ID | R | - | - | 0 |
| Bit 6 | - | RID2 | | R | - | - | 0 |
| Bit 5 | - | RID1 | | R | - | - | 0 |
| Bit 4 | - | RID0 | | R | - | - | 1 |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

SMBusTable: DEVICE ID

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-------------------|------------------|------|---------------------|---|---------|
| Bit 7 | - | Device ID 7 (MSB) | | R | Device ID is 18 hex | | 0 |
| Bit 6 | - | Device ID 6 | | R | | 0 | |
| Bit 5 | - | Device ID 5 | | R | | 0 | |
| Bit 4 | - | Device ID 4 | | R | | 1 | |
| Bit 3 | - | Device ID 3 | | R | | 1 | |
| Bit 2 | - | Device ID 2 | | R | | 0 | |
| Bit 1 | - | Device ID 1 | | R | | 0 | |
| Bit 0 | - | Device ID 0 | | R | | 0 | |

SMBusTable: Byte Count Register

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|---|------|---|---|---------|
| Bit 7 | - | BC7 | Writing to this register configures how many bytes will be read back. | RW | - | - | 0 |
| Bit 6 | - | BC6 | | RW | - | - | 0 |
| Bit 5 | - | BC5 | | RW | - | - | 0 |
| Bit 4 | - | BC4 | | RW | - | - | 0 |
| Bit 3 | - | BC3 | | RW | - | - | 0 |
| Bit 2 | - | BC2 | | RW | - | - | 1 |
| Bit 1 | - | BC1 | | RW | - | - | 1 |
| Bit 0 | - | BC0 | | RW | - | - | 1 |



**THERMALLY ENHANCED, VERY THIN, FINE PITCH
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DIMENSIONS

| | |
|-------|----|
| | |
| N | 64 |
| N_D | 16 |
| N_E | 16 |

DIMENSIONS (mm)

| SYMBOL | MIN. | MAX. |
|----------------|----------------|------|
| A | 0.8 | 1.0 |
| A1 | 0 | 0.05 |
| A3 | 0.25 Reference | |
| b | 0.18 | 0.3 |
| e | 0.50 BASIC | |
| D x E BASIC | 9.00 x 9.00 | |
| D2 MIN. / MAX. | 7.00 | 7.25 |
| E2 MIN. / MAX. | 7.00 | 7.25 |
| L MIN. / MAX. | 0.30 | 0.50 |

Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---------------------|--------------------|------------|---------------|
| 9EX21501AKLF | Trays | 64-pin MLF | 0 to +70° C |
| 9EX21501AKLFT | Tape and Reel | 64-pin MLF | 0 to +70° C |
| 9EX21501AKILF | Trays | 64-pin MLF | -40 to +85° C |
| 9EX21501AKILFT | Tape and Reel | 64-pin MLF | -40 to +85° C |

"LF" suffix to the part number are the Pb-free configuration and are RoHS compliant.

"A" is the revision designator (will not correlate with datasheet revision).

Due to package size constraints actual top side marking may differ from the full orderable part number.

Revision History

| Rev. | Who | Issue Date | Description | Page # |
|------|-----|------------|---|---------|
| 0.1 | RDW | 4/6/2009 | Initial Release | - |
| 0.2 | RDW | 4/7/2008 | 1. Lowered IDD 2. Updated block diagram to correct typo's 3. Corrected Pin descriptions 4. Corrected Frequency/functionality table references to Byte 2, should be Byte 0 5. Updated Power Groups Table 6. Corrected typo in SMBus Address Selection Table. 7. Corrected references to 9EX1501 to be 9EX21501 | Various |
| 0.3 | RDW | 11/24/2009 | 1. Added more detailed Idd numbers to DS 2. Added industrial temp Idd numbers and ordering information | |
| 0.4 | RDW | 2/4/2010 | 1. Corrected Pin Description for Pin 52. There was discrepancy between the Frequency/Functionality Table and the Pin Description. The Pin Description was not correct. Instead of the pin description defining functionality, it now refers to the Frequency Functionality Table for the definition. | 4 |
| 0.5 | RDW | 1/18/2011 | 1. Reformatted Electrical Tables to latest template 2. Updated electrical tables with characterized data 3. Added Test loads diagram and table 4. Move to Final | Various |
| | | | | |
| | | | | |

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