

Description

The 9INT31H200 is a 2-output very high-performance HCSL fanout buffer for high performance interconnect applications. It can be used at speeds up to 350MHz and is compliant to the DB200H specification.

Typical Applications

- DB200H
- Ethernet
- PCIe

Output Features

- 2 HCSL differential pairs

Key Specifications

- Qx output-to-output skew across all outputs: 5ps (typical)
- RMS additive phase jitter: 64fs typical (12kHz–20MHz at 156.25MHz)

Block Diagram

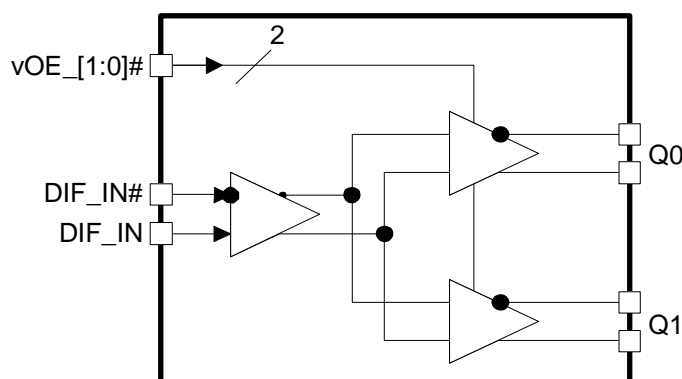


Table 1. Power Management

| DIF_IN | OEx# Pin | Qx | nQx |
|------------|----------|------------------|------------------|
| Running | 1 | Low ¹ | Low ¹ |
| Running | 0 | Running | Running |
| NotRunning | X | X | X |

Notes:

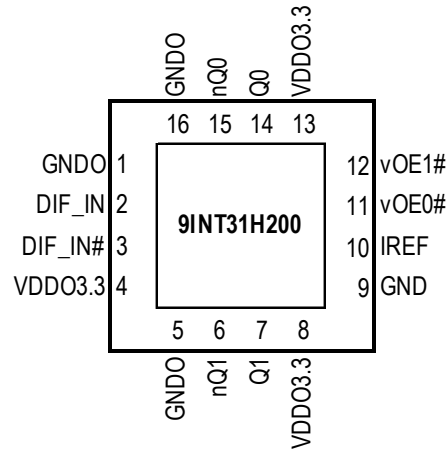
1. The outputs are tristated, and the termination networks pulls them low.

Table 2. Power Connections

| Pin Number | | Description |
|------------|----------|-----------------------|
| VDD | GND | |
| 4 | 1 | Input receiver analog |
| 8, 13 | 5, 9, 16 | DIF outputs |

Pin Assignments

Figure 1. Pin Assignments for 3 × 3 mm 16-QFN Package – Top View



16-QFN, 3 x 3 mm, 0.5mm pitch

^ prefix indicates internal 120kOhm pull-up resistor
v prefix indicates internal 120kOhm pull-down resistor

Pin Descriptions

| Pin# | Pin Name | Type | Pin Description |
|------|----------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | GND0 | GND | Ground pin for outputs. |
| 2 | DIF_IN | IN | HCSL true input |
| 3 | DIF_IN# | IN | HCSL complementary input |
| 4 | VDDO3.3 | PWR | Power supply for outputs, nominally 3.3V. |
| 5 | GND0 | GND | Ground pin for outputs. |
| 6 | nQ1 | OUT | Inverting output of differential pair 1. |
| 7 | Q1 | OUT | Non-inverting output of differential pair 1. |
| 8 | VDDO3.3 | PWR | Power supply for outputs, nominally 3.3V. |
| 9 | GND | GND | Ground pin. |
| 10 | IREF | OUT | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 11 | vOE0# | IN | Active low input for enabling output 0. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs. |
| 12 | vOE1# | IN | Active low input for enabling output 1. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs. |
| 13 | VDDO3.3 | PWR | Power supply for outputs, nominally 3.3V. |
| 14 | Q0 | OUT | Non-inverting output of differential pair 0. |
| 15 | nQ0 | OUT | Inverting output of differential pair 0. |
| 16 | GND0 | GND | Ground pin for outputs. |
| 17 | EPAD | GND | Connect epad to ground. |

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9INT31H200 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|----------------------|--------------------|----------------------------|---------|---------|----------------------|-------|-------|
| Supply Voltage | VDDx | | | | 4.6 | V | 1,2 |
| Input Low Voltage | V _{IL} | | GND-0.5 | | | V | 1 |
| Input High Voltage | V _{IH} | Except for SMBus interface | | | V _{DD} +0.5 | V | 1,3 |
| Input High Voltage | V _{IHSMB} | SMBus clock and data pins | | | 5.5 | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Operation under these conditions is neither implied nor guaranteed.

³ Not to exceed 4.6V.

Electrical Characteristics–DIF_IN Clock Input Parameters

T_{AMB} = T_{COM} or T_{IND} unless otherwise indicated, supply voltages per normal operation conditions; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|----------------------------------|--------------------|-----------------------------------------------------------|---------|---------|---------|-------|-------|
| Input Crossover Voltage - DIF_IN | V _{CROSS} | Crossover voltage | 150 | | 900 | mV | 1 |
| Input Swing - DIF_IN | V _{SWING} | Differential value | 300 | | | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | uA | |
| Input Duty Cycle | d _{in} | Measurement from differential waveform | 45 | | 55 | % | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through +/-75mV window centered around differential zero.

Electrical Characteristics–Current Consumption

T_A = T_{IND}; supply voltage VDDx = 3.3V +/-5%; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|--------------------------|------------------------|------------------------------------------------------------------------------|---------|---------|---------|-------|-------|
| Operating Supply Current | I _{DD3.3OP} | All outputs running at 350MHz C _L = 2pF; Z _o = 85Ω. | | 65 | 80 | mA | - |
| | I _{DD3.3STBY} | 1 output running at 350MHz, other output disabled. | | 50 | 62 | mA | - |
| | I _{DD3.3IDLE} | All outputs stopped, input clock running at 350MHz or stopped. | | 35 | 43 | mA | - |

Electrical Characteristics–Input/Supply/Common Parameters

$T_{AMB} = T_{COM}$ or T_{IND} unless otherwise indicated, supply voltages per normal operation conditions; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|-------------------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----------|---------|----------------|--------|-------|
| Supply Voltage | VDDx | Supply voltage | 3.135 | 3.3 | 3.465 | V | |
| Ambient Operating Temperature | T_{AMB} | Industrial range (T_{IND}) | -40 | 25 | 85 | °C | |
| Input High Voltage | V_{IH} | Single-ended inputs | 2 | | $V_{DD} + 0.3$ | V | |
| Input Low Voltage | V_{IL} | Single-ended inputs | GND - 0.3 | | 0.8 | V | |
| Input Current | I_{IN} | Single-ended inputs, $V_{IN} = GND$, $V_{IN} = V_{DD}$ | -5 | | 5 | μA | |
| | I_{INP} | Single-ended inputs $V_{IN} = 0$ V; Inputs with internal pull-up resistors $V_{IN} = V_{DD}$; Inputs with internal pull-down resistors | -50 | | 50 | μA | |
| Input Frequency | F_{in} | $V_{DD} = 3.3$ V | 1 | | 350 | MHz | |
| Pin Inductance | L_{pin} | | | | 7 | nH | 1 |
| Capacitance | C_{IN} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | C_{INDIF_IN} | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,4 |
| | C_{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | T_{STAB} | From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | 0.1 | 1.8 | ms | 1,2 |
| OE# Latency | $t_{LTOE\#}$ | DIF start after OE# assertion DIF stop after OE# deassertion | 4 | 6 | 10 | clocks | 1,2,3 |
| Tdrive_PD# | t_{DRVPD} | DIF output enable after PD# de-assertion | | 40 | 300 | us | 1,3 |
| Tfall | t_f | Fall time of control inputs | | | 5 | ns | 2 |
| Trise | t_r | Rise time of control inputs | | | 5 | ns | 2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200 mV.

⁴ DIF_IN input

Electrical Characteristics–Qx HCSL/LP-HCSL Outputs

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limit | Units | Notes |
|------------------------|------------------------------|-------------------------------------------------------------------------------------------------------|---------|---------|---------|----------------|-------|-------|
| Slew Rate | dV/dt | Scope averaging on. | 1 | 1.5 | 2 | 0.6 - 4 | V/ns | 1,2,3 |
| Slew Rate Matching | Δ dV/dt | Single-ended measurement | | 7 | 15 | 20 | % | 1,4 |
| Voltage High | V _{high} | Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on). | 625 | 681 | 725 | 850 | mV | |
| Voltage Low | V _{low} | | -25 | 14 | 50 | 150 | | |
| Max Voltage | V _{max} | Measurement on single-ended signal using absolute value (scope averaging off). | | 705 | 750 | 1150 | mV | |
| Min Voltage | V _{min} | | -50 | -3 | | -300 | | |
| Crossing Voltage (abs) | V _{cross_abs} | Scope averaging off. | 325 | 349 | 375 | 250 - 550 | mV | 1,5 |
| Crossing Voltage (var) | Δ -V _{cross} | Scope averaging off. | | 3.4 | 20 | 140 | mV | 1,6 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Measured from differential waveform.

³Slew rate is measured through the V_{swing} voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵V_{cross} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶The total variation of all V_{cross} measurements in any particular system. Note that this is a subset of V_{cross_min/max} (V_{cross} absolute) allowed. The intent is to limit V_{cross} induced modulation by setting Δ -V_{cross} to be smaller than V_{cross} absolute.

Electrical Characteristics–Qx Output Duty Cycle, Jitter, and Skew Characteristics

$T_A = T_{IND}$; supply voltage VDDx = 3.3V +/-5%; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---------------------------------|-------------------------|------------------------------------------|---------|---------|---------|-------|-------|
| Duty Cycle Distortion | t _{CD} | Measured differentially | -0.5 | 0 | 0.5 | % | 1,2 |
| Skew, Input to Output | t _{PD} | V _T = 50% | 2.3 | 2.6 | 3.1 | ps | 1 |
| Skew, Output to Output | t _{sk3} | Across all outputs, V _T = 50% | | 5 | 40 | ps | 1 |
| Jitter, Cycle to cycle additive | t _{cyc-cycadd} | Additive | | 1.1 | 2 | ps | 1,3 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Duty cycle distortion is the difference in duty cycle between the output and the input clock.

³Measured from differential waveform.

Electrical Characteristics–Additive Phase Jitter

$T_A = T_{IND}$; supply voltage VDDx = 3.3V +/-5%; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|-----------------------|-----------------|--------------------------------------------------|---------|---------|---------|----------|-------|
| Additive Phase Jitter | t _{ph} | All outputs running at 156.25MHz, 12kHz to 20MHz | | 64 | 75 | fs (rms) | 1,2,3 |

¹Applies to all outputs.

²Signal source is Wenzel.

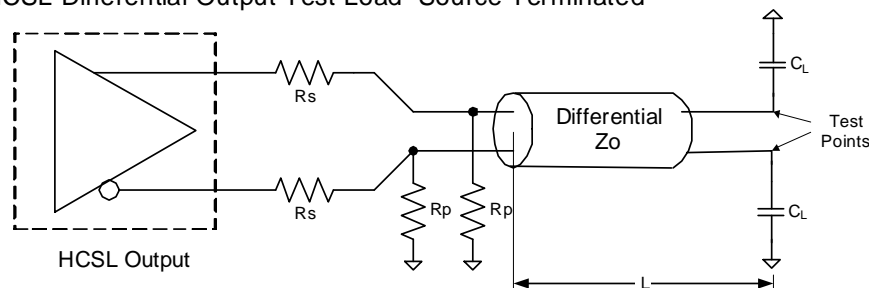
³For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)² - (input jitter)²].

Test Loads

Differential Output Termination Table

| DIF Zo (Ω) | L (in) | C _L (pF) | Iref (Ω) | Rs (Ω) | Rp (Ω) |
|---------------------|--------|---------------------|-------------------|-----------------|-----------------|
| 100 | 5 | 2 | 475 | 33 | 50 |
| 85 | 5 | 2 | 412 | 27 | 42.2 or 43.2 |

HCSL Differential Output Test Load -Source Terminated



Thermal Characteristics

Table 3. Thermal Characteristics ^[1]

| Symbol | Parameter | Typical Value | Units |
|----------------|---------------------------------|---------------|-------|
| θ_{JC} | Junction to case | 65.8 | °C/W |
| θ_{Jb} | Junction to base | 5.1 | °C/W |
| θ_{JA0} | Junction to Air, still air | 63.2 | °C/W |
| θ_{JA1} | Junction to Air, 1 m/s air flow | 55.9 | °C/W |
| θ_{JA3} | Junction to Air, 3 m/s air flow | 51.4 | °C/W |
| θ_{JA5} | Junction to Air, 5 m/s air flow | 49.2 | °C/W |

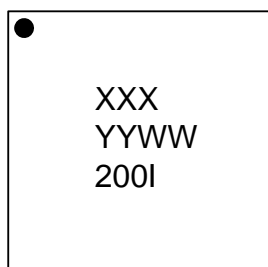
[1] ePad soldered to board.

Package Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/16-vfqfpn-package-outline-drawing-30-x-30-x-09-mm-05-mm-170-x-170-mm-epad-nl16p2

Marking Diagram



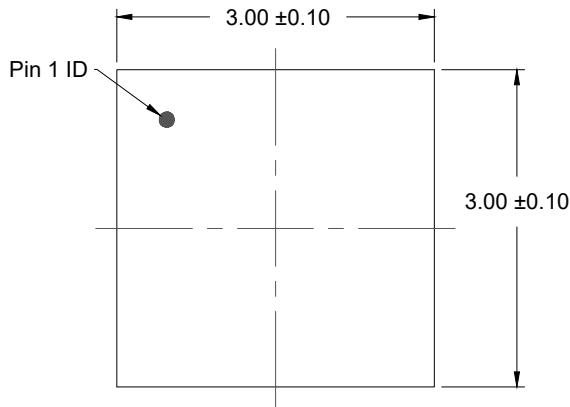
1. "XXX" is the last three characters of the Asm lot.
2. "YYWW" is the last digits of the year and week that the part was assembled.
3. Line 3 is the truncated part number.
4. "I" denotes industrial temperature.

Ordering Information

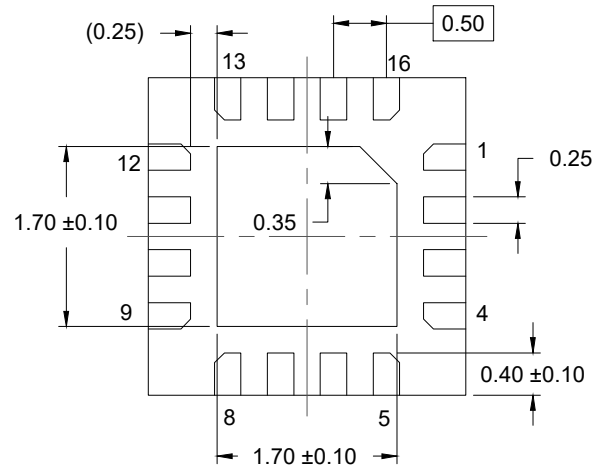
| Orderable Part Number | Package | Carrier Type | Temperature |
|-----------------------|------------------------------|---------------|---------------|
| 9INT31H200NLGI | 3 × 3 mm, 0.5mm pitch 16-QFN | Tray | -40° to +85°C |
| 9INT31H200NLGI8 | 3 × 3 mm, 0.5mm pitch 16-QFN | Tape and Reel | -40° to +85°C |

Revision History

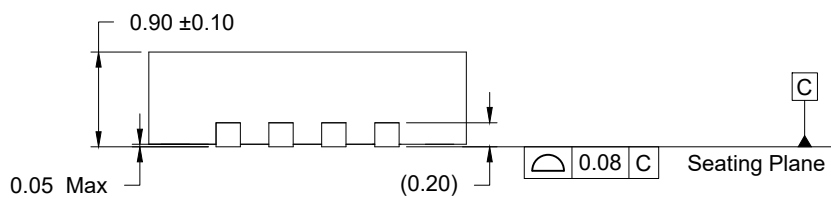
| Revision Date | Description of Change |
|----------------|-----------------------|
| August 9, 2018 | Initial release. |



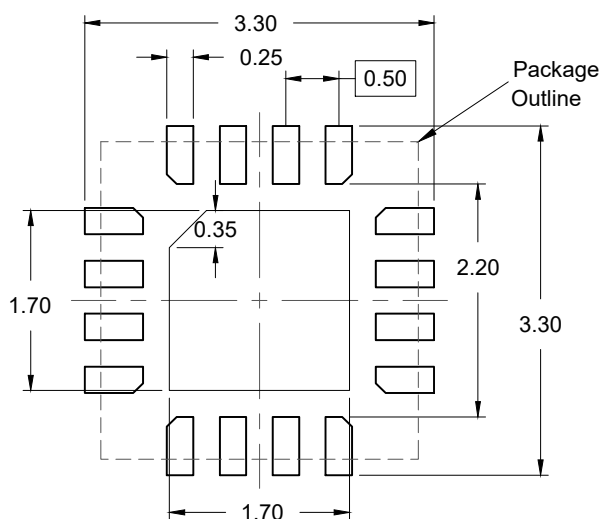
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.