

## Description

The 9INT31H400 is a 4-output very high-performance HCSL fanout buffer for high-performance interconnect applications. It can be used at speeds up to 350MHz and is compliant to the DB400H specification. There are four OE pins on the device, each controlling one output.

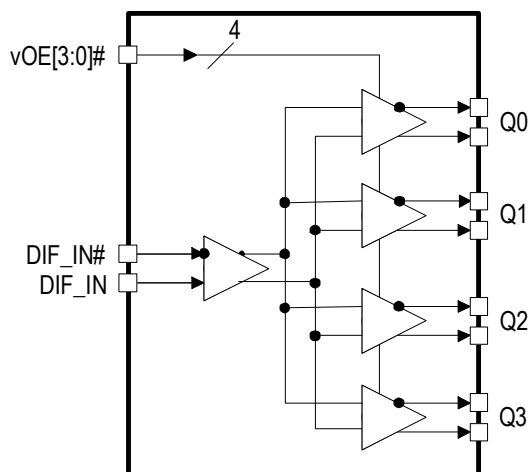
## Typical Applications

- DB400H

## Key Specifications

- Qx output-to-output skew within a pair: 19ps (typical)
- Qx output-to-output skew across all outputs: 26ps (typical)
- RMS additive phase jitter: 61fs typical (12kHz to 20MHz at 156.25MHz)

## Block Diagram



## Features

- Extremely low additive phase jitter; supports DB400H requirements
- 3.3V operation; standard industry power supply
- 4 OE pins (1 for each output); easy control of clocks to CPU sockets
- HCSL-compatible input; supports popular devices
- 1MHz to 350MHz operating frequency; covers all popular Ethernet frequencies
- Space saving 4 × 4 mm 24-VFQFPN; minimal board space

## Output Features

- 4 HCSL differential pairs

## Power Management

DIF_IN	OEx# Pin	Qx	nQx
Running	1	Low <sup>1</sup>	Low <sup>1</sup>
Running	0	Running	Running
Not Running	X	X	X

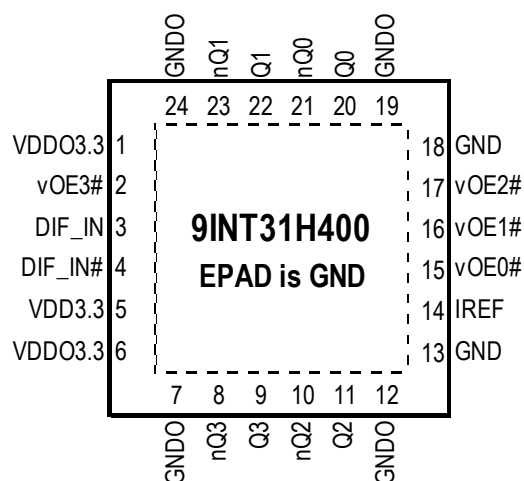
<sup>1</sup> The outputs are tri-stated, and the termination networks pulls them low.

## Power Connections

Pin Number		Description
V <sub>DD</sub>	GND	
5	25	Input receiver analog
5	13,18	Internal circuitry
1,6	7,12,19,24	DIF outputs

## Pin Assignments

**Figure 1. Pin Assignments for 4 × 4 mm 24-VFQFPN Package – Top View**



### 4 x 4 mm 24-VFQFPN, 0.5mm pitch

^ prefix indicates internal 120kOhm pull-up resistor

v prefix indicates internal 120kOhm pull down-resistor

# Pin Descriptions

**Table 1. Pin Descriptions**

Number	Name	Type	Description
1	VDDO3.3	Power	Power supply for outputs, nominal 3.3V.
2	vOE3#	Input	Active low input for enabling output 3. This pin has an internal 120kΩ pull-down resistor. 1 = disable outputs, 0 = enable outputs.
3	DIF_IN	Input	HCSL True input.
4	DIF_IN#	Input	HCSL Complementary input.
5	VDD3.3	Power	Power supply, nominal 3.3V.
6	VDDO3.3	Power	Power supply for outputs, nominal 3.3V.
7	GNDO	GND	Ground pin for outputs.
8	nQ3	Output	Inverting output of differential pair 3.
9	Q3	Output	Non-inverting output of differential pair 3.
10	nQ2	Output	Inverting output of differential pair 2.
11	Q2	Output	Non-inverting output of differential pair 2.
12	GNDO	GND	Ground pin for outputs.
13	GND	GND	Ground pin.
14	IREF	Output	This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475Ω is the standard value for 100Ω differential impedance. Other impedances require different values.
15	vOE0#	Input	Active low input for enabling output 0. This pin has an internal 120kΩ pull-down resistor. 1 = disable outputs, 0 = enable outputs.
16	vOE1#	Input	Active low input for enabling output 1. This pin has an internal 120kΩ pull-down resistor. 1 = disable outputs, 0 = enable outputs.
17	vOE2#	Input	Active low input for enabling output 2. This pin has an internal 120kΩ pull-down resistor. 1 = disable outputs, 0 = enable outputs.
18	GND	GND	Ground pin.
19	GNDO	GND	Ground pin for outputs.
20	Q0	Output	Non-inverting output of differential pair 0.
21	nQ0	Output	Inverting output of differential pair 0.
22	Q1	Output	Non-inverting output of differential pair 1.
23	nQ1	Output	Inverting output of differential pair 1.
24	GNDO	GND	Ground pin for outputs.
25	EPAD	GND	Connect to Ground.

## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9INT31H400 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 2. Absolute Maximum Ratings**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Supply Voltage	$V_{DDx}$				4.6	V	1,2
Input Low Voltage	$V_{IL}$		GND-0.5			V	1
Input High Voltage	$V_{IH}$	Except for SMBus interface.			$V_{DD} + 0.5$	V	1,3
Input High Voltage	$V_{IHSMB}$	SMBus clock and data pins.			5.5	V	1
Storage Temperature	$T_s$		-65		150	°C	1
Junction Temperature	$T_j$				125	°C	1
Input ESD Protection	ESD prot	Human Body Model.	2500			V	1

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Operation under these conditions is neither implied nor guaranteed.

<sup>3</sup> Not to exceed 4.6V.

## Electrical Characteristics

$T_{AMB} = T_{COM}$  or  $T_{IND}$  unless otherwise indicated. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

**Table 3. DIF\_IN Clock Input Parameters**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Input Crossover Voltage–DIF_IN	$V_{CROSS}$	Crossover voltage.	200		900	mV	1
Input Swing–DIF_IN	$V_{SWING}$	Differential value.	300			mV	1
Input Slew Rate–DIF_IN	$dv/dt$	Measured differentially.	0.4		8	V/ns	1,2
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{DD}$ , $V_{IN} = GND$ .	-5		5	μA	
Input Duty Cycle	$d_{tin}$	Measurement from differential waveform.	45		55	%	1

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Slew rate measured through  $\pm 75$ mV window centered around differential zero.

**Table 4. Input/Supply/Common Parameters**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Supply Voltage	$V_{DDx}$	Supply voltage.	3.135	3.3	3.465	V	
Ambient Operating Temperature	$T_{AMB}$	Industrial range ( $T_{IND}$ ).	-40		85	°C	
Input High Voltage	$V_{IH}$	Single-ended inputs.	2		$V_{DD} + 0.3$	V	
Input Low Voltage	$V_{IL}$	Single-ended inputs.	GND - 0.3		0.8	V	
Input Current	$I_{IN}$	Single-ended inputs, $V_{IN} = \text{GND}$ , $V_{IN} = V_{DD}$ .	-5		5	μA	
	$I_{INP}$	Single-ended inputs. $V_{IN} = 0\text{V}$ ; inputs with internal pull-up resistors. $V_{IN} = V_{DD}$ ; inputs with internal pull-down resistors.	-50		50	μA	
Input Frequency	$F_{IN}$	$V_{DD} = 3.3\text{V}$ .	1		350	MHz	
Pin Inductance	$L_{pin}$				7	nH	1
Capacitance	$C_{IN}$	Logic inputs, except DIF_IN.	1.5		5	pF	1
	$C_{INDIF\_IN}$	DIF_IN differential clock inputs.	1.5		2.7	pF	1,4
	$C_{OUT}$	Output pin capacitance.			6	pF	1
Clk Stabilization	$t_{STAB}$	From $V_{DD}$ power-up and after input clock stabilization or deassertion of PD# to 1st clock.			0.08	ms	1,2
OE# Latency	$t_{LATO\#}$	DIF start after OE# deassertion. DIF stop after OE# deassertion.	6		8	clocks	1,2,3
Tdrive_PD#	$t_{DRV\#}$	DIF output enable after PD# deassertion.			75	μs	1,3
Tfall	$t_F$	Fall time of control inputs.			5	ns	2
Trise	$t_R$	Rise time of control inputs.			5	ns	2

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup> Time from deassertion until outputs are > 400mV.

<sup>4</sup> DIF\_IN input.

**Table 5. Qx HCSL/LP-HCSL Outputs**

$T_{AMB}$  = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Unit	Notes
Slew Rate	dV/dt	Scope averaging on.	1.4	1.9	2.5	0.6–4	V/ns	1,2,3
Slew Rate Matching	$\Delta$ dV/dt	Single-ended measurement.		7	19	20	%	1,4
Maximum Voltage	$V_{MAX}$	Measurement on single-ended signal using absolute value (scope averaging off).		742	850	1150	mV	
Minimum Voltage	$V_{MIN}$		-100	-29		-300	mV	
Crossing Voltage (abs)	$V_{CROSS\_ABS}$	Scope averaging off.	300	348	400	250–550	mV	1,5
Crossing Voltage (var)	$\Delta$ - $V_{CROSS}$	Scope averaging off.		9	60	140	mV	1,6

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Measured from differential waveform.

<sup>3</sup> Slew rate is measured through the  $V_{SWING}$  voltage range centered around differential 0 V. This results in a  $\pm 150$ mV window around differential 0V.

<sup>4</sup> Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a  $\pm 75$ mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

<sup>5</sup>  $V_{CROSS}$  is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>6</sup> The total variation of all  $V_{CROSS}$  measurements in any particular system. Note that this is a subset of  $V_{CROSS\_MIN/MAX}$  ( $V_{CROSS}$  absolute) allowed. The intent is to limit  $V_{CROSS}$  induced modulation by setting  $\Delta$ - $V_{CROSS}$  to be smaller than  $V_{CROSS}$  absolute.

**Table 6. Current Consumption**

$T_A = T_{IND}$ ; supply voltage  $V_{DDX} = 3.3V \pm 5\%$ ; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Operating Supply Current	$I_{DD3.3OP}$	All outputs running at 350MHz, $C_L = 2pF$ ; $Z_o = 85\Omega$ .		95	117	mA
	$I_{DD3.3IDLE}$	All outputs stopped, input clock running at 350MHz or stopped.		35	43	mA

**Table 7. Qx Output Duty Cycle, Jitter, and Skew Characteristics**

$T_A = T_{IND}$ ; supply voltage  $V_{DDX} = 3.3V \pm 5\%$ ; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Duty Cycle Distortion	$t_{DCD}$	Measured differentially.	-1	0	1	%	1,2
Skew, Input to Output	$t_{PD}$	$V_T = 50\%$ .	2.3	2.6	3.1	ns	1
Skew, Output to Output	$t_{SK3}$	Across all outputs, $V_T = 50\%$ .		13	40	ps	1
Jitter, Cycle to Cycle, Additive	$t_{jcc-cycadd}$	Additive.		1.4	5	ps	1,3

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Duty cycle distortion is the difference in duty cycle between the output and the input clock.

<sup>3</sup> Measured from differential waveform.

**Table 8. Additive Phase Jitter**

$T_A = T_{IND}$ ; supply voltage  $V_{DDX} = 3.3V \pm 5\%$ ; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Additive Phase Jitter	$t_{jph}$	All outputs running at 156.25MHz, 12kHz to 20MHz.		62	75	fs (rms)	1,2,3

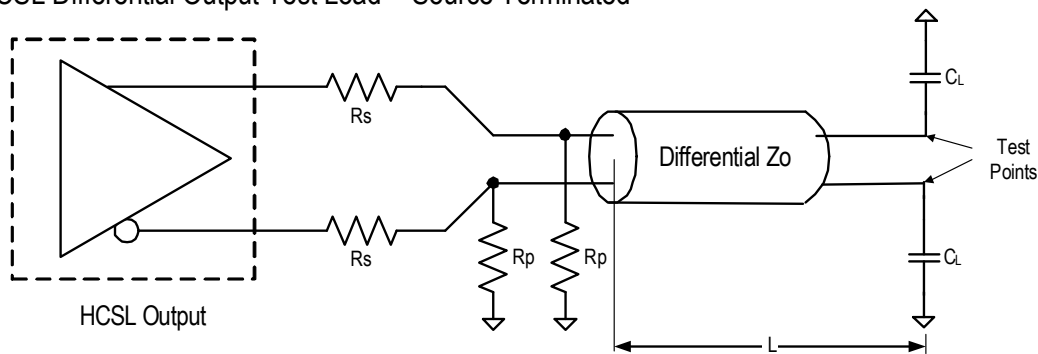
<sup>1</sup> Applies to all outputs.

<sup>2</sup> Signal source is Wenzel.

<sup>3</sup> For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter =  $\sqrt{(\text{total jitter})^2 - (\text{input jitter})^2}$ .

## Test Loads

HCSL Differential Output Test Load - Source Terminated



**Table 9. Differential Output Termination**

DIF Zo (Ω)	L (in)	CL (pF)	Iref (Ω)	Rs (Ω)	Rp (Ω)
100	5	2	475	33	50
85	5	2	412	27	42.2 or 43.2

## Thermal Characteristics

**Table 10. Thermal Characteristics <sup>1</sup>**

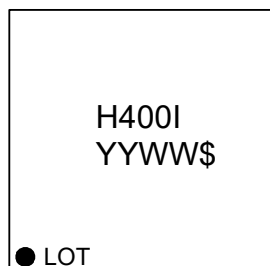
Parameter	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	$\theta_{JC}$	Junction to case.	61.7	°C/W
	$\theta_{Jb}$	Junction to base.	5.4	°C/W
	$\theta_{JA0}$	Junction to Air, still air.	50.1	°C/W
	$\theta_{JA1}$	Junction to Air, 1 m/s air flow.	43.1	°C/W
	$\theta_{JA3}$	Junction to Air, 3 m/s air flow.	40.7	°C/W
	$\theta_{JA5}$	Junction to Air, 5 m/s air flow.	39.4	°C/W

<sup>1</sup> EPAD soldered to board.

## Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

## Marking Diagram



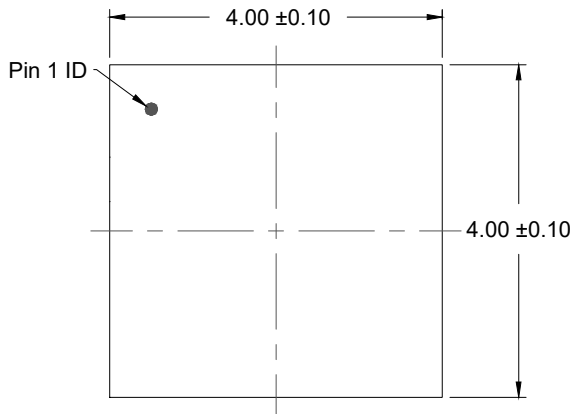
- Line 1 is the truncated part number.
- "I" denotes industrial temperature.
- "YYWW" is the last digits of the year and week that the part was assembled.
- "\$" denotes the mark code.
- "LOT" denotes the sequential lot number.

## Ordering Information

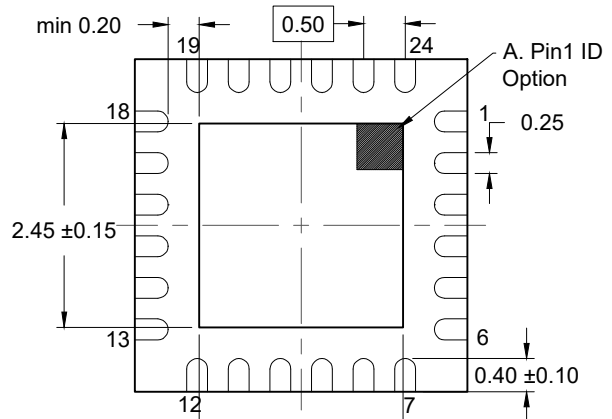
Part Number	Package	Carrier Type	Temperature Range
9INT31H400NLGI	4 × 4 mm, 0.5mm pitch <a href="#">24-VFQFPN</a>	Tray	-40° to +85°C
9INT31H400NLGI8	4 × 4 mm, 0.5mm pitch <a href="#">24-VFQFPN</a>	Tape and Reel	-40° to +85°C

## Revision History

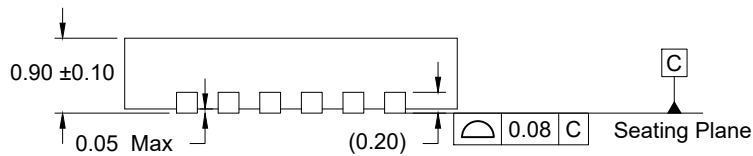
Revision Date	Description of Change
December 1, 2022	Updated <a href="#">Package Outline Drawings</a> text and added POD links to <a href="#">Ordering Information</a> .
March 26, 2020	Corrected units typo for t <sub>PD</sub> from ps to ns.
August 9, 2018	Initial release.



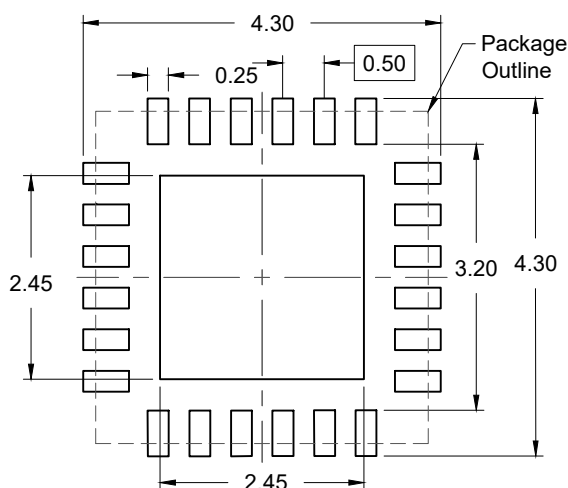
TOP VIEW



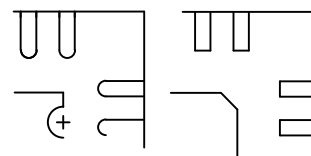
BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)



A. PIN1 ID OPTION DETAILS

### NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Pin#1 ID is identified by either chamfer or notch.

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