

ACS373MS

Radiation Hardened Octal Transparent Latch, Three-State

FN3999
Rev 0.00
April 1995

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose 300K RAD (Si)
- Single Event Upset (SEU) Immunity
 $<1 \times 10^{-10}$ Errors/Bit-Day (Typ)
- SEU LET Threshold >80 MEV-cm²/mg
- Dose Rate Upset $>10^{11}$ RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
 - VIL = 30% of VCC Max
 - VIH = 70% of VCC Min
- Input Current $\leq 1\mu\text{A}$ at VOL, VOH

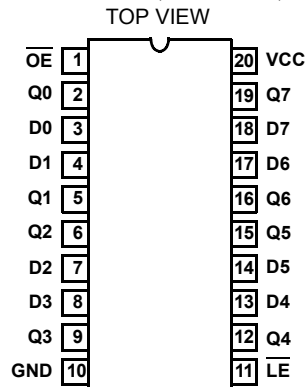
Description

The Intersil ACS373MS is a radiation hardened octal transparent latch with three-state outputs. The outputs are transparent to the inputs when the latch enable ($\overline{\text{LE}}$) is high. When the $\overline{\text{LE}}$ goes low, the data is latched. When the Output Enable ($\overline{\text{OE}}$) is high, the outputs are in the high impedance state. The latch operation is independent of the state of the output enable.

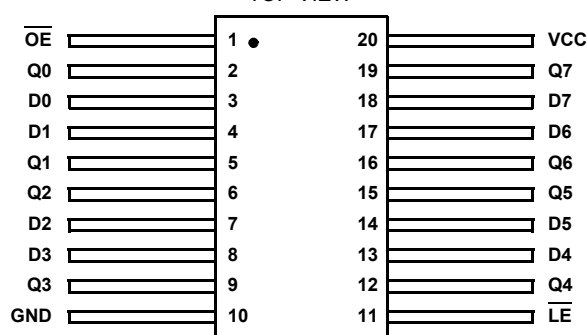
The ACS373MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of the radiation hardened, high-speed, CMOS/SOS Logic Family.

Pinouts

20 LEAD CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T20, LEAD FINISH C



20 LEAD CERAMIC FLATPACK
MIL-STD-1835 DESIGNATOR, CDFP4-F20, LEAD FINISH C



Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
ACS373DMSR	-55°C to +125°C	Intersil Class S Equivalent	20 Lead SBDIP
ACS373KMSR	-55°C to +125°C	Intersil Class S Equivalent	20 Lead Ceramic Flatpack
ACS373D/Sample	+25°C	Sample	20 Lead SBDIP
ACS373K/Sample	+25°C	Sample	20 Lead Ceramic Flatpack
ACS373HMSR	+25°C	Die	Die

Truth Table

$\overline{\text{OE}}$	$\overline{\text{LE}}$	D	Q
L	H	H	H
L	H	L	L
L	L	I	L
L	L	h	H
H	X	X	Z

NOTE:

L = Low Voltage Level

X = Don't Care

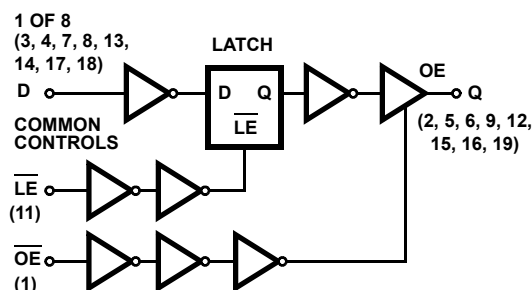
H = High Voltage Level

Z = High Impedance State

I = Low voltage level one set-up time prior to the high to low latch enable transition

h = High voltage level one set-up time prior to the high to low latch enable transition

Functional Diagram



Absolute Maximum Ratings

Supply Voltage	-0.5V to +6.0V
Input Voltage Range, All Inputs	-0.5V to VCC +0.5V
DC Input Current, Any One Input	±10mA
DC Drain Current, Any One Output	±50mA
Storage Temperature Range (TSTG)	-65°C to +150°C
Lead Temperature (Soldering 10s)	+265°C
Junction Temperature (TJ)	+175°C
ESD Classification	Class 1
(All Voltages Reference to VSS)	

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Reliability Information

Thermal Impedance	θ_{JA}	θ_{JC}
DIP	72°C/W	24°C/W
Flatpack	107°C/W	28°C/W
Maximum Package Power Dissipation at +125°C		
DIP	0.7W	
Flatpack	0.5W	
Maximum Device Power Dissipation	(TBD)W	
Gate Count	121 Gates	

Operating Conditions

Supply Voltage (VCC)	+4.5V to +5.5V	Input High Voltage (VIH)	VCC to 70% of VCC
Input Rise and Fall Times at VCC = 4.5V (TR, TF)	10ns/V Max	Input Low Voltage (VIL)	0.0V to 30% of VCC
Operating Temperature Range (TA)	-55°C to +125°C		

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	μA
			2, 3	+125°C, -55°C	-	400	μA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V, (Note 2)	1	+25°C	-12	-	mA
			2, 3	+125°C, -55°C	-8	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0V, (Note 2)	1	+25°C	12	-	mA
			2, 3	+125°C, -55°C	8	-	mA
Output Voltage High	VOH	VCC = 5.5V, VIH = 3.85V VIL = 1.65V, IOH = -50μA	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = -50μA	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 3.85V VIL = 1.65V, IOH = 50μA	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = 50μA	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	μA
			2, 3	+125°C, -55°C	-	±1.0	μA
Three-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	+25°C	-	±1	μA
			2, 3	+125°C, -55°C	-	±35	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	V

NOTE:

1. All voltages referenced to device GND.
2. Force/measure functions may be interchanged.
3. For functional tests, VO ≥4.0V is recognized as a logic "1", and VO ≤0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPHL1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	14	ns
			10, 11	+125°C, -55°C	2	15	ns
	TPLH1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	15	ns
			10, 11	+125°C, -55°C	2	18	ns
	TPHL2	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	13	ns
			10, 11	+125°C, -55°C	2	14	ns
	TPLH2	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	14	ns
			10, 11	+125°C, -55°C	2	16	ns
	TPZL1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	14	ns
			10, 11	+125°C, -55°C	2	15	ns
	TPLZ1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	14	ns
			10, 11	+125°C, -55°C	2	14	ns
	TPHZ1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	15	ns
			10, 11	+125°C, -55°C	2	16	ns
	TPZH1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	15	ns
			10, 11	+125°C, -55°C	2	16	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS			UNITS
					MIN	TYP	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	25	-	pF
				+125°C	-	30	-	pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	-	10	pF
				+125°C	-	-	10	pF
Output Capacitance	COUT	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	-	20	pF
				+125°C	-	-	20	pF
Pulse Width Time	TW	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	7	-	-	ns
				+125°C	7	-	-	ns
Setup Time	TSU	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	5	-	-	ns
				+125°C	5	-	-	ns
Hold Time	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	3	-	-	ns
				+125°C	3	-	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMP	RAD LIMITS		UNITS
				MIN	MAX	
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	400	μA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOU = VCC - 0.4V, VIL = 0	+25°C	-8	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	8	-	mA
Output Voltage High	VOH	VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOH = -50μA	+25°C	VCC - 0.1	-	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = -50μA	+25°C	VCC - 0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOH = 50μA	+25°C	-	0.1	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = 50μA	+25°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±1	μA
Three-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25°C	-	±35	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, (Note 2)	+25°C	-	-	V
Propagation Delay	TPHL1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	15	ns
	TPLH1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	18	ns
	TPHL2	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	14	ns
	TPLH2	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	16	ns
	TPZL1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	15	ns
	TPLZ1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	14	ns
	TPHZ1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	16	ns
	TPZH1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	16	ns

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	(NOTE 1) DELTA LIMIT	UNITS
Supply Current	ICC	±4.0	μA
Three-State Leakage Current	IOZ	±200	nA
Output Current	IOL/IOH	±15	%

NOTE:

1. All delta calculations are referenced to 0 hour readings or pre-life readings.

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test 1 (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test 2 (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test 3 (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 7, 9	

NOTE:

1. Alternate Group A testing may be exercised in accordance with MIL-STD-883, Method 5005.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUP	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. BURN-IN TEST CONNECTIONS (+125°C < TA < 139°C)

OPEN	GROUND	1/2 VCC = 3V ±0.5V	VCC = 6V ±0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN 1 (Note 1)					
-	1, 3, 4, 7, 8, 10, 11, 13, 14, 17, 18	2, 5, 6, 9, 12, 15, 16, 19	20	-	-
STATIC BURN-IN 2 (Note 1)					
-	10	2, 5, 6, 9, 12, 15, 16, 19	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20	-	-
DYNAMIC BURN-IN (Note 1)					
-	1, 10	2, 5, 6, 9, 12, 15, 16, 19	20	11	3, 4, 7, 8, 13, 14, 17, 18

NOTE:

1. Each pin except VCC and GND will have a series resistor of 500 Ω $\pm$ 5% for static burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS (TA = +25°C, $\pm$ 5°C)

FUNCTION	OPEN	GROUND	VCC = 5V $\pm$ 0.5V
Irradiation Circuit (Note 1)	2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20

NOTE:

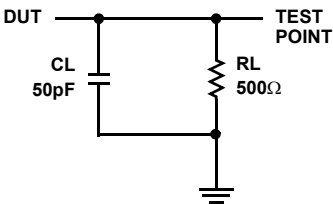
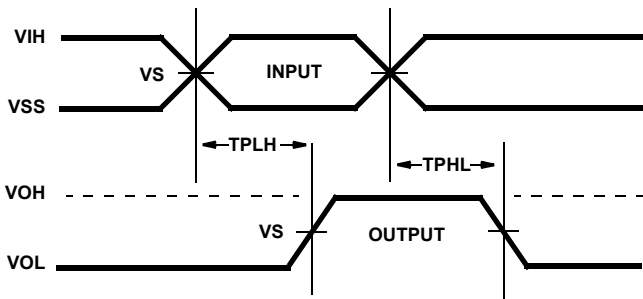
1. Each pin except VCC and GND will have a series resistor of 47k Ω $\pm$ 5%. Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures.

Intersil - Space Products MS Screening

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)	100% Static Burn-In 2 Method 1015, 24 Hours at +125°C Min
Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects	100% Interim Electrical Test 2 (Note 1)
100% Nondestructive Bond Pull Method 2023	100% Dynamic Burn-In Method 1015, 240 Hours at +125°C or 180 Hours at +135°C
100% Internal Visual Inspection Method 2010	100% Interim Electrical Test 3 (Note 1)
100% Temperature Cycling Method 1010 Condition C (-65° to +150°C)	100% Final Electrical Test
100% Constant Acceleration	100% Fine and Gross Seal Method 1014
100% PIND Testing	100% Radiographics Method 2012 (2 Views)
100% External Visual Inspection	100% External Visual Method 2009
100% Serialization	Group A (All Tests) Method 5005 (Class S)
100% Initial Electrical Test	Group B (Optional) Method 5005 (Class S) (Note 2)
100% Static Burn-In 1 Method 1015, 24 Hours at +125°C Min	Group D (Optional) Method 5005 (Class S) (Note 2)
100% Interim Electrical Test 1 (Note 1)	CSI and/or GSI (Optional) (Note 2)
	Data Package Generation (Note 3)

- NOTES:
- Failures from interim electrical tests 1 and 2 are combined for determining PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures). Interim electrical tests 3 PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures).
 - These steps are optional, and should be listed on the purchase order if required.
 - Data Package Contents:
Cover Sheet (P.O. Number, Customer Number, Lot Date Code, Intersil Number, Lot Number, Quantity).
Certificate of Conformance (as found on shipper).
Lot Serial Number Sheet (Good Unit(s) Serial Number and Lot Number).
Variables Data (All Read, Record, and delta operations).
Group A Attributes Data Summary.
Wafer Lot Acceptance Report (Method 5007) to include reproductions of SEM photos. NOTE: SEM photos to include percent of step coverage.
X-Ray Report and Film, including penetrometer measurements.
GAMMA Radiation Report with initial shipment of devices from the same wafer lot; containing a Cover Page, Disposition, RAD Dose, Lot Number, Test Package, Spec Number(s), Test Equipment, etc. Irradiation Read and Record data will be on file at Intersil.

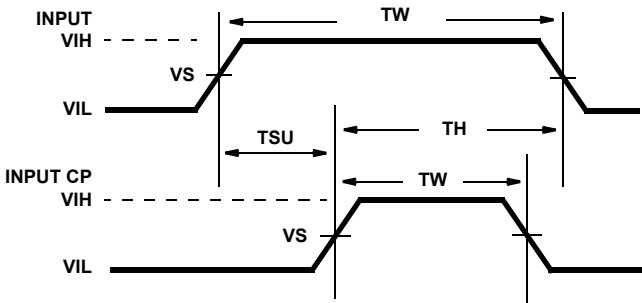
Propagation Delay Timing Diagram and Load Circuit



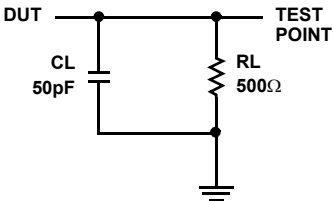
AC VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger and AC Load Circuit



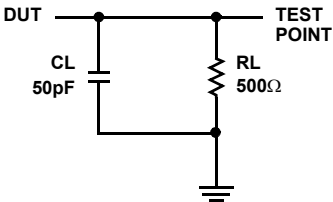
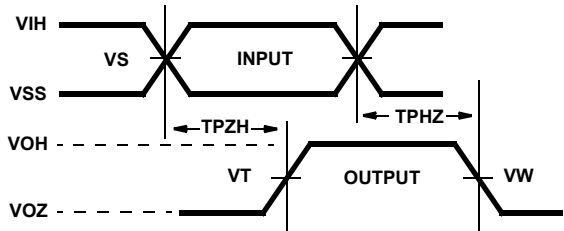
TH = HOLD TIME
TSU = SETUP TIME
TW = PULSE WIDTH



PULSE WIDTH, SETUP, HOLD VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

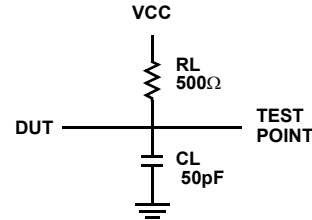
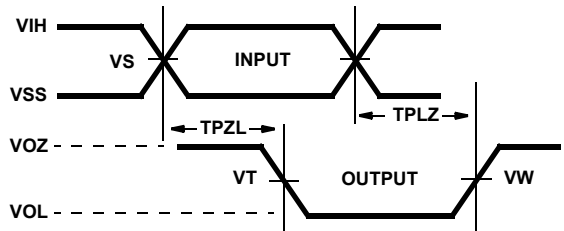
Three-State High Timing Diagram and Load Circuit



PULSE WIDTH, SETUP, HOLD VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	3.60	V
GND	0	V

Three-State Low Timing Diagram and Load Circuit



PULSE WIDTH, SETUP, HOLD VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.90	V
GND	0	V

Die Characteristics**DIE DIMENSIONS:**

102 mils x 102 mils
2,600mm x 2,600mm

METALLIZATION:

Type: AlSiCu
Metal 1 Thickness: 6.75kÅ (Min), 8.25kÅ (Max)
Metal 2 Thickness: 9kÅ (Min), 11kÅ (Max)

GLASSIVATION:

Type: SiO₂
Thickness: 8kÅ ±1kÅ

DIE ATTACH:

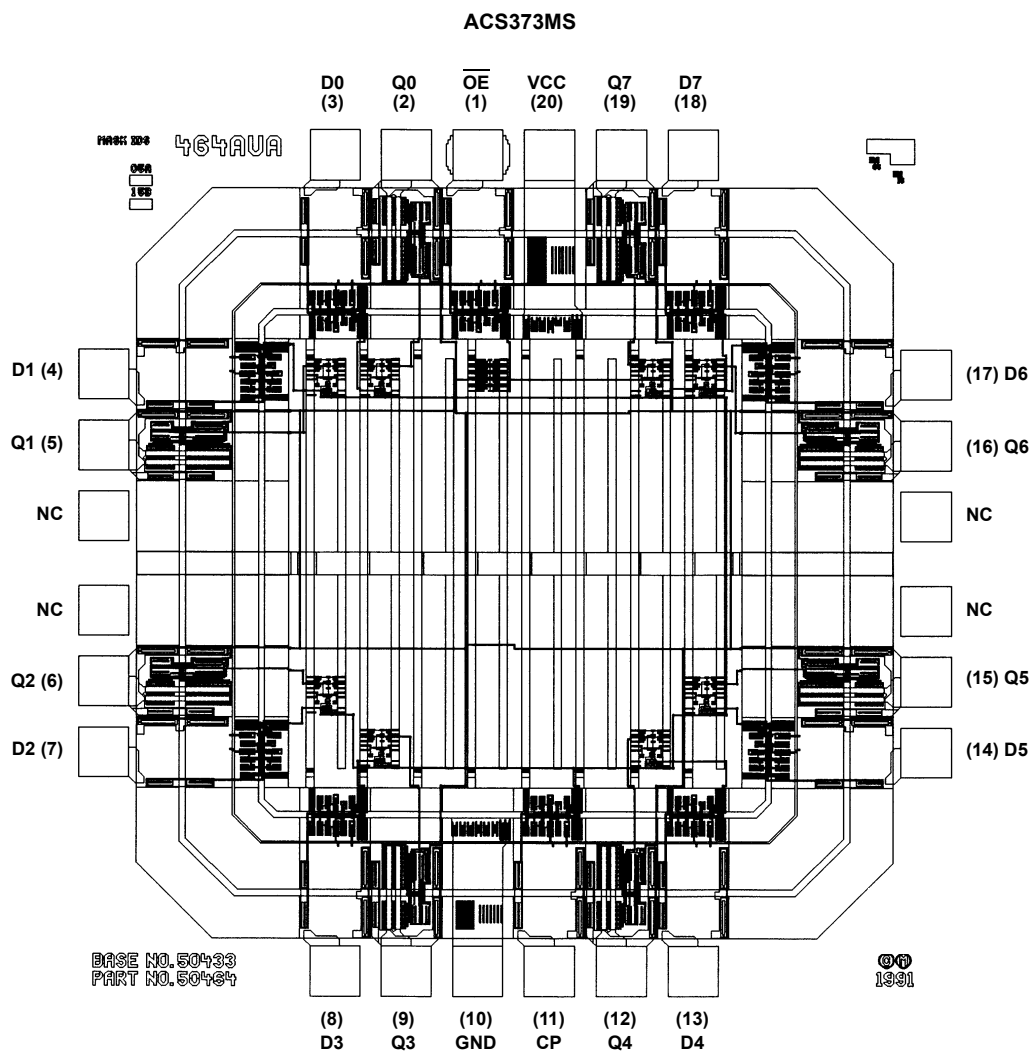
Material: Silver Glass or JM 7000 after 7/1/95

WORST CASE CURRENT DENSITY:

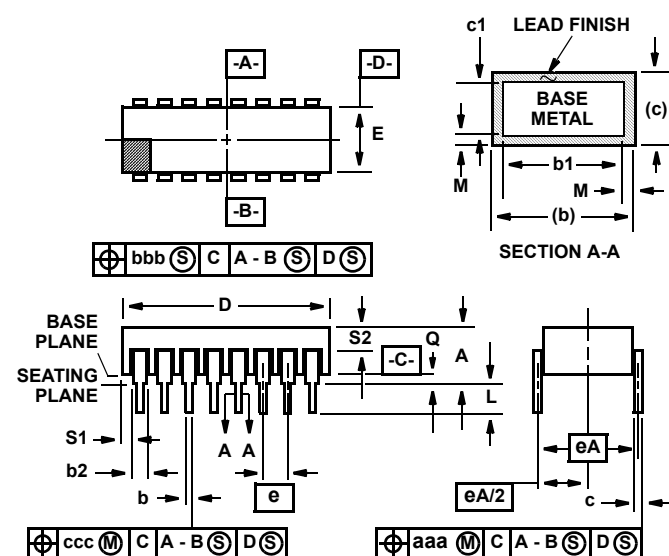
$< 2.0 \times 10^5 \text{ A/cm}^2$

BOND PAD SIZE:

$> 4.3 \text{ mils} \times 4.3 \text{ mils}$
 $> 110\mu\text{m} \times 110\mu\text{m}$

Metallization Mask Layout

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D20.3 MIL-STD-1835 CDIP2-T20 (D-8, CONFIGURATION C) 20 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.060	-	26.92	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	20		20		8

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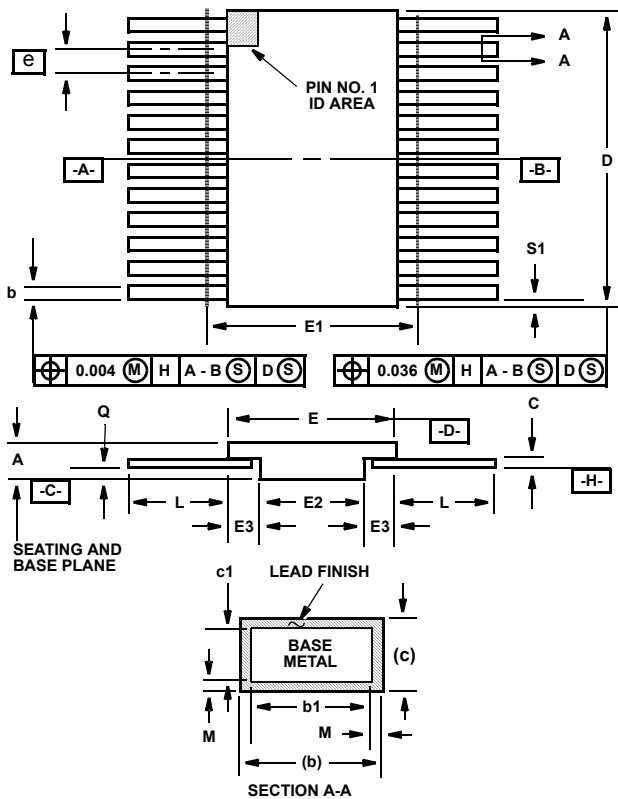
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Ceramic Metal Seal Flatpack Packages (Flatpack)



K20.A MIL-STD-1835 CDFP4-F20 (F-9A, CONFIGURATION B)
20 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.540	-	13.72	3
E	0.245	0.300	6.22	7.62	-
E1	-	0.330	-	8.38	3
E2	0.130	-	3.30	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	20		20		-

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.