AT25SF2561C / AT25QF2561C

256-Mbit SPI Serial Flash Memory with Dual I/O and Quad I/O Support

Features

- Single voltage operation with range of 2.7 V to 3.6 V
- Serial Peripheral Interface (SPI) compatible support
  - Supports SPI modes 0 and 3
  - Supports single input/output operations (1-1-1)
  - Supports SPI dual output operations (1-1-2)
  - Supports SPI dual I/O operations (1-2-2)
  - Supports Quad output operations (1-1-4)
  - Supports Quad I/O / XiP operations (1-4-4, 0-4-4)
  - Supports QPI operations
- Supports 3- and 4-byte addressing
- Read operations
  - Fast read up to 133 MHz
  - Quad SPI and QPI read up to 133 MHz
  - DTR frequency up to 84 MHz
  - Continuous read with 8/16/32/64-byte wrap
- Flexible erase architecture and time
  - Block erase 4 kB (45 ms typical)
  - Block erase 32 kB and 64 kB (90 ms and 150 ms typical)
  - Full chip erase (80 s typical)
- Flexible programming and time
  - Page/byte program (from 1 to 256 bytes)
  - Page program time (0.15 ms, typical)
- Erase program suspend resume
- JEDEC hardware reset
- Hardware Reset pin option in 16-pin SOIC package
- JEDEC Standard Manufacturer and Device ID
- Multiple memory protection schemes
  - Individual block protection
  - Top, bottom, or block selection
  - Enable/disable protection with $\overline{WP}$ pin
  - Write protect all portions of memory via software protect
- 3 x 1024-byte One-Time Programmable (OTP) security registers
- Serial Flash Discoverable Parameter (SFDP) register
- Low power dissipation
  - 12 µA Standby current (typical)
  - 0.5 µA Deep power-down current (typical)
  - 11 mA active read current (typical)
- User-configurable I/O pin drive strength levels
- Endurance 100,000 program/erase cycles
- Data Retention: 20 years
- Temperature Range: Industrial (-40 ºC to 85 ºC)
- Industry standard green (Pb/Halide-free/RoHS compliant) package options
  - 8-pin Wide Body SOIC (208 mil)
  - 8-pin DFN (6 x 8 x 0.8 mm)
  - 8-pin DFN (5 x 6 x 0.8 mm)
  - 16-pin SOIC (300 mil)

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1. Product Overview

The AT25SF2561C / AT25QF2561C is a 256-Mbit Serial Peripheral Interface (SPI) Flash memory device designed for use in a wide variety of high-volume industrial, consumer and connected applications.

It can be used for storing program memory that is booted from Flash memory into embedded or external RAM; it can also be used for directly executing the program code from the Flash memory (execute in place [XiP]).

XiP is specifically supported by features which enhance read speed:

- Quad-SPI, which allows reading four bits in one clock cycle, or eight bits when double transfer rate (DTR) is enabled.
- Continuous read mode (0-4-4 command format), which removes the need to send a command opcode.
- High SPI clock frequency.

These features allow fast response from the Flash memory whenever the host must fetch commands or data from it.

Both the AT25SF2561C and the AT25QF2561C support quad-SPI operations. The AT25QF2561C has quad-SPI enabled by default. The AT25SF2561C does not have quad-SPI enabled by default; thus, for quad-SPI operations, users must enable it explicitly (by setting the QE bit in Status Register 2 to 1).

2. Pin Descriptions

Table 1. AT25SF2561C / AT25QF2561C Pin Names

Pin Name	I/O	Description
$\overline{CS}$	I	**Chip Select.** The chip select signal indicates the beginning of a device operation. When the $\overline{CS}$ signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. Unless an internal *Program*, *Erase* or *Write Status Registers* embedded operation is in progress, the device remains in the Standby Power mode. Driving the $\overline{CS}$ input to logic low state enables the device, placing it in the *Active Power* mode. After power-up, a falling edge on $\overline{CS}$ is required prior to the start of any command.
SO (IO_1)	I/O	**Serial Output** for single bit data commands. **IO_1** for dual or quad commands. During single SPI transfers, the SO output signal is used to transfer data serially out of the AT25SF2561C / AT25QF2561C device. Data is shifted out on the falling edge of the serial SCK clock signal. During a dual or quad transfer, the SO pin becomes an I/O pin (I/O). This pin works in conjunction with the other I/O pins to transfer data. Data is shifted out on the falling edge of SCK, MSB first.
$\overline{WP}$ (IO_2)	I/O	**Write Protect** in single bit or dual data commands. **IO_2** in quad mode. The signal has an internal pull-up resistor and can be left unconnected in the host system if not used for quad commands. When $\overline{WP}$ is driven low, while the Status Register Protect bits (SRP1 and SRP0) are set to 0 and 1 respectively, it is not possible to write to the Status Registers. This prevents any alteration of the Status Registers. As a consequence, all the data bytes in the memory area that are protected by the Block Protect bits in the Status Registers are also hardware protected against data modification while $\overline{WP}$ remains low. The $\overline{WP}$ function is not available when the Quad mode is enabled (QE bit in Status Register 2 = 1). The $\overline{WP}$ function is replaced by I/O_2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK). $\overline{WP}$ has an internal pull-up resistor.
GND		**Ground.** The ground reference for the V_{CC} supply voltage.

Table 1. AT25SF2561C / AT25QF2561C Pin Names *(continued)*

Pin Name	I/O	Description
SI (IO_0)	I/O	**Serial Input** for single bit data commands. **IO_0** for dual or quad commands. During the write phase of an operation, this signal transfers command, address, and data from the host into the AT25SF2561C / AT25QF2561C device. The command is transmitted first, followed by the address, followed by write data (on a write operation). The MSB of each field is transmitted first. Values are latched on the rising edge of serial SCK clock signal. During the read phase of a single SPI operation, the SO pin is used to transfer data to the device; the SI pin is not used. During the read phase of a dual or quad operation, the SI pin becomes the I/O_0 an output pin and works in conjunction with the other I/O pins to allow data from the AT25SF2561C / AT25QF2561C device to be driven to the host during execution of a dual or quad mode command. The data is shifted out of the memory on the falling edge of SCK.
SCK	I	**Serial Clock.** This input signal provides the synchronization reference for the SPI interface. Commands, addresses, or data input are latched on the rising edge of the SCK signal. Data output changes after the falling edge of SCK.
$\overline{HOLD}$ / $\overline{RESET}$ (IO_3)	I/O	**Hold/Reset/IO_3** This pin is used either for pausing communication (in which case it is referred to as $\overline{HOLD}$), as a hardware reset pin (in which case it is referred to as $\overline{RESET}$), or as one of the quad-SPI I/O pins (in which case it is referred to as IO_3). When the Quad Enable (QE) bit of Status Register 2 is 0 and the HOLD/RST bit in Status Register 3 is 0, this pin is used as a $\overline{HOLD}$ pin. When the Quad Enable (QE) bit of Status Register 2 is 0 and the HOLD/RST bit in Status Register 3 is 1, this pin is used as a $\overline{RESET}$ pin. When the QE bit of Status Register 2 is 1, quad-SPI communication is enabled, and the pin is used as the IO_3 pin in any command that makes use of quad-SPI. In this setting, do not use the pin for pausing communication or for reset. The $\overline{HOLD}$ pin is used to pause a SPI sequence without resetting the clocking sequence. To enable the HOLD mode, the $\overline{CS}$ must be low. The HOLD mode effect is on with the falling edge of the $\overline{HOLD}$ signal with SCK being low. The HOLD mode ends on the rising edge of $\overline{HOLD}$ signal with SCK being low. If not used, the $\overline{HOLD}$ pin is internally pulled-high and can be left floating. Note: When using the device in a 16-pin SOIC package, use the dedicated $\overline{RESET}$ (pin3) for a hardware reset.
V_{CC}		**Power Supply** for core and I/O. It is the single voltage used for all device functions including read, program, and erase.

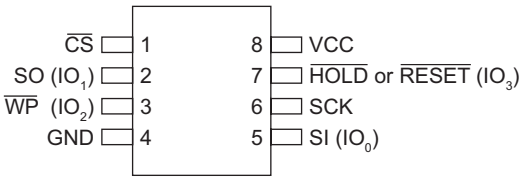


Figure 1. 8-SOIC (150 and 208 mil) — Top View

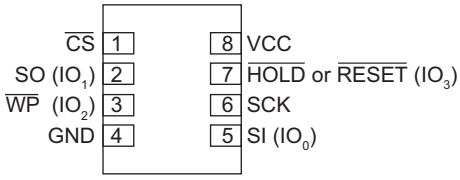
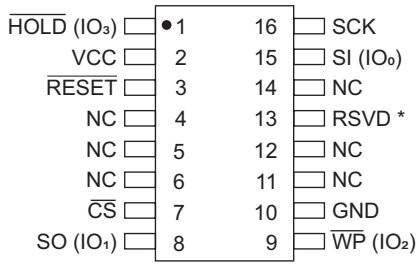


Figure 3. 8-DFN — Top View



* RSVD = Reserved. Do not connect this pin.

Figure 2. 16-SOIC (300 mil) — Top View

3. Memory Architecture

Table 2. Memory Architecture Diagram of AT25SF2561C / AT25QF2561C

Memory Density	512 kB Block	64 kB Block	32 kB Block	4 kB Block	Address Range
256 Mbit	Block 0	Block 0	Block 0	Block 0	0000000h - 0000FFFh
				·	·
				Block 7	0007000h - 0007FFFh
			Block 1	Block 8	0008000h - 0008FFFh
				·	·
				Block 15	000F000h - 000FFFFh
		Block 7	Block 14	Block 112	0070000h - 0070FFFh
				·	·
				Block 119	0077000h - 0077FFFh
			Block 15	Block 120	0078000h - 0078FFFh
				·	·
				Block 127	007F000h - 007FFFFh
	·	·	·	·	·
	Block 63	Block 504	Block 1008	Block 8064	1F80000h - 1F80FFFh
				·	·
				Block 8071	1F87000h - 1F87FFFh
			Block 1009	Block 8072	1F88000h - 1F88FFFh
				·	·
				Block 8079	1F8F000h - 1F8FFFFh
		·	·	·	·
		Block 511	Block 1022	Block 8176	1FF0000h - 1FF0FFFh
				·	·
				Block 8183	1FF7000h - 1FF7FFFh
			Block 1023	Block 8184	1FF8000h - 1FF8FFFh
				·	·
				Block 8191	1FFF000h - 1FFFFFFh

4. SPI Operation

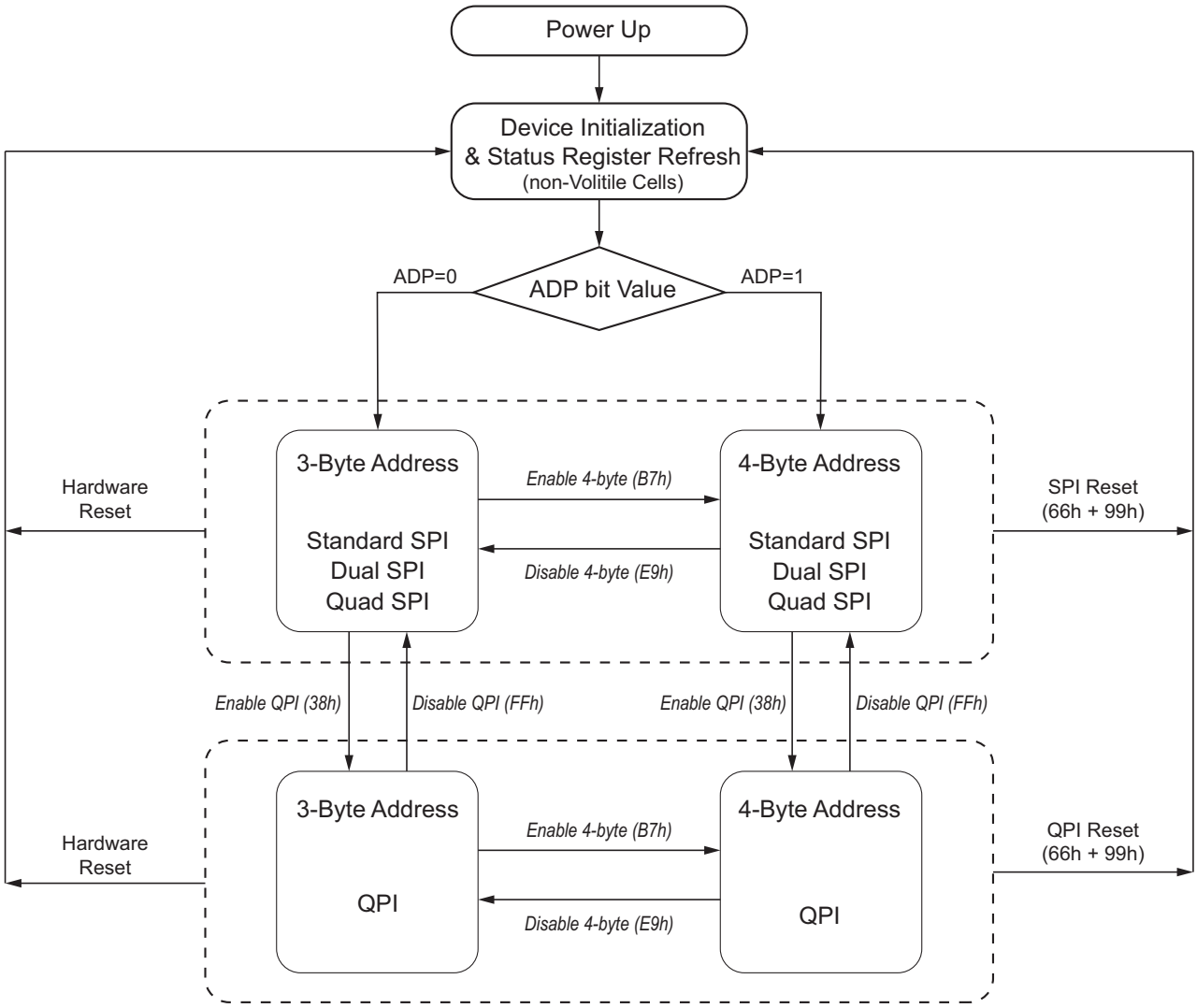


Figure 4. Device Operation Modes

4.1 Standard SPI Commands

The AT25SF2561C / AT25QF2561C features a four-pin serial peripheral interface on a four-signal bus: Serial Clock (SCK), Chip Select ($\overline{CS}$), Serial Data Input (SI) and Serial Data Output (SO). SPI bus modes 0 and 3 are supported. Input data is latched on the rising edge of SCK and data shifts out on the falling edge of SCK.

4.2 Dual SPI Commands

The AT25SF2561C / AT25QF2561C supports Dual SPI operation when using the 3Bh, 3Ch, BBh, BCh, and 92h commands. These commands allow data to be transferred to, or from, the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: I/O_0 and I/O_1, respectively.

4.3 Quad SPI Commands

The AT25SF2561C / AT25QF2561C supports Quad SPI operation when using the 6Bh, 6Ch, EBh, EDh, ECh, 94h, 32h, and 34h commands. These commands allow data to be transferred to, or from, the device at four times the rate of the standard SPI. Quad SPI is enabled by default on the AT25QF2561C. When using the Quad SPI command, the SI and SO pins become bidirectional I/O pins: I/O_0 and I/O_1, and the $\overline{WP}$ and $\overline{HOLD}$ pins become I/O_2 and I/O_3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

4.4 QPI Commands

The AT25SF2561C / AT25QF2561C supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the Enter QPI (38h) command. The typical SPI protocol requires that the byte long command code being shifted into the device only through the SI pin in eight serial clocks. QPI mode uses all four IO pins to input the command code; thus, only two serial clocks are required.

Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at a time. The Enter QPI (38h) and Exit QPI (FFh) commands are used to switch between these two modes. QPI mode requires Quad-SPI to be enabled (QE bit in Status Register 2 must be set to 1).

4.5 DTR Commands

The AT25SF2561C / AT25QF2561C supports DTR operation when using the DTR Quad I/O Fast Read (EDh/EEh) commands or the Burst Read with Wrap (0Ch) command. These commands allow data to be transferred to, or from, the device at eight times the rate of the standard SPI, and data output is latched on both rising and falling edges of the serial clock. When using the DTR instructions the SI and SO pins become bidirectional I/O pins: IO_0 and IO_1.

4.6 Three-Byte / Four-Byte Address Modes

The AT25SF2561C / AT25QF2561C provides two Address Modes to specify any byte of data in the memory array. The Three-Byte Address Mode is backward-compatible to older generations of serial Flash memory that only support up to 128 Mbit data. To address the 256 Mbit or more data in Three-Byte Address Mode, Extended Address Register must be used in addition to the three-byte addresses.

Four-Byte Address Mode supports Serial Flash Memory devices from 256 Mbit to 32 Gbit. The extended Address Register is not necessary when Four-Byte Address Mode is enabled.

On power-up, the AT25SF2561C / AT25QF2561C can operate in either Three-Byte Address Mode or Four-Byte Address Mode, depending on the Non-Volatile Status Register Bit ADP (SR3 bit 1) setting. If ADP=0, the device operates in Three-Byte Address Mode; if ADP=1, the device operates in Four-Byte Address Mode. The factory default value for ADP is 0.

To switch between the address modes, use either the Enter 4 Byte Address Mode (B7h) or Exit 4 Byte Address Mode (E9h) command. The current address mode is indicated by the Status Register Bit ADS (SR1 bit 0).

5. Status Registers

The AT25SF2561C / AT25QF2561C contains three Status registers. The registers are read and written as follows:

- Write Status Register 1 (01h)
- Read Status Register 1 (05h)
- Write Status Register 2 (31h)
- Read Status Register 2 (35h)
- Write Status Register 3 (11h)
- Read Status Register 3 (15h)

5.1 Status Register

The following shows the layout of Status Register 1. This register is written using the Status Register 1 Write command (05h) and read using the Status Register 1 Read command (01h).

Table 3. Status Register 1 Bit Encoding

	7	6	5	4	3	2	1	0
	SRP0	BP4	BP3	BP2	BP1	BP0	WEL	RDY/BSY
Default [1]	0	0	0	0	0	0	0	0
							Read Only	Read Only

The following shows the layout of Status Register 2. This register is written using the Status Register 2 Write command (35h) and read using the Status Register 2 Read command (31h).

Table 4. Status Register 2 Bit Encoding

	7	6	5	4	3	2	1	0
	SUS1	CMP	LB3	LB2	LB1	SUS2	QE	SRP1
Default [1]	0	0	0	0	0	0	0 for AT25SF2561C 1 for AT25QF2561C	0
	Read Only		OTP	OTP	OTP	Read Only		

The following shows the layout of Status Register 3. This register is written using the Status Register 3 Write command (15h) and read using the Status Register 3 Read command (11h).

Table 5. Status Register 3 Bit Encoding

	7	6	5	4	3	2	1	0
	HOLD/RST	DRV1	DRV0	DC1	DC0	WPS	ADP	ADS
Default [1]	0	0	0	X	X	0	0	0
						OTP		Read Only

1. Default value is set by manufacturer during wafer sort, marked Default in following text.

5.2 Status and Control Bits

5.2.1 RDY/BSY Bit

The RDY/BSY (Ready/Busy) bit indicates whether the memory is busy in program/erase/write status register progress. When RDY/BSY bit sets to 1, means the device is busy in program/erase/write status register progress, when RDY/BSY bit sets 0, means the device is not in program/erase/write status register progress.

5.2.2 WEL Bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program, or Erase commands are accepted.

5.2.3 BP4, BP3, BP2, BP1, BP0 Bits

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register 1 command.

- When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory becomes protected against Page Program and Block Erase commands.
- The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.
- The Chip Erase (CE) command is executed if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP = 0 or the Block Protect (BP2, BP1, BP0) bits are 1 and CMP = 1.

5.2.4 SRP1, SRP0 Bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in Status Registers 1 and 2. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection. For more information on how the SRP[1:0] bits are used for software and hardware protection, see Section 6.6.1, Block Protect Table (WPS = 0).

5.2.5 QE Bit

The Quad Enable (QE) bit is a non-volatile Read/Write bit in Status Register 2 that allows Quad operation. When the QE bit is set to 0 (default for the AT25SF2561C), the $\overline{WP}$ pin and $\overline{HOLD}$ pin are enable. When the QE bit is set to 1 (default for the AT25QF2561C), the Quad I/O_2 and I/O_3 pins are enabled. Never set the QE bit to 1 during standard SPI or Dual SPI operation if the $\overline{WP}$ or $\overline{HOLD}$ pins directly to the power supply or ground. For the AT25QF2561C, note that if these pins are connected to power or ground, software must first clear the QE bit.

For the AT25SF2561C, the QE bit must be set to 1 before issuing an Enter QPI (38h) command to switch the device from Standard/Dual/Quad SPI to QPI; otherwise, the command is ignored. When the device is in QPI mode, the QE bit remains set to 1. A Write Status Register command in QPI mode cannot change the QE bit from 1 to 0.

5.2.6 LB3/LB2/LB1 Bits

The LB bits are non-volatile One Time Program (OTP) bits in Status Register 2 (5 - 3) that provide the write protect control and status to the Security Registers. The default state of LBx is 0, the security registers are unlocked. The LBx bits can be set to 1 individually using the Write Register command. The LBx bits are One-Time Programmable. Once they are set to 1, the Security Registers become read-only permanently.

5.2.7 CMP Bit

The CMP bit is a non-volatile Read/Write bit in the Status Register (SR2 bit 6). It is used in conjunction the SEC and BP0 bits to provide more flexibility for the array protection. See Table 11 and Table 12 for details; the default setting is CMP = 0.

5.2.8 SUS1/SUS2 Bits

The Suspend Status (SUS1 and SUS2) bits are read only bits in the Status Register 2 (7 and 2) that are set to 1 after executing an Erase/Program Suspend (75h) command. The Erase Suspend sets SUS1 to 1, and the Program Suspend sets SUS2 to 1. The SUS1 and SUS2 bits are cleared to 0 by Erase/Program Resume (7Ah) command as well as a power-down, power-up cycle.

5.2.9 ADS Bit

The Current Address Mode (ADS) bit is a read-only bit in Status Register 3 that indicates the current address mode of the device. When ADS = 0, the device is in three-byte address mode. When ADS = 1, the device is in four-byte address mode.

5.2.10 ADP Bit

The Power-Up Address Mode (ADP) bit is non-volatile and indicates the initial address mode when the device is powered on or reset. This bit is only used during power-on or reset initialization period. It can only be written by the non-volatile Write Status Register sequence (06h + 11h). When ADP = 0 (factory default), the device powers up in three-byte address mode. In this case, the Extended Address register must be used to access memory regions beyond 128 Mbit. When ADP = 1, the device powers up in four-byte address mode directly.

5.2.11 HOLD/RST Bit

The $\overline{\text{HOLD}}$ or $\overline{\text{RESET}}$ pin Function (HOLD/RST) bit is used to determine whether the $\overline{\text{HOLD}}$ or the $\overline{\text{RESET}}$ function is implemented on the hardware pin. When HOLD/RST=0 (factory default), the pin acts as $\overline{\text{HOLD}}$; when HOLD/RST=1, the pin acts as $\overline{\text{RESET}}$. However, $\overline{\text{HOLD}}$ or $\overline{\text{RESET}}$ functions are only avail able when QE=0. If QE is set to 1, the $\overline{\text{HOLD}}$ and $\overline{\text{RESET}}$ functions are disabled; the pin then is a dedicated data I/O.

5.2.12 WPS Bit

There are two write memory array protection methods provided: Block Protection (BP) mode or Individual Block Memory Protection mode. The protection modes are mutually exclusive. The WPS bit selects which protection mode is enabled. Note that the WPS bit is an OTP bit. Once WPS is set to 1, it cannot be programmed back to 0.

If WPS=0 (factory default), the BP mode is enabled, and Individual Block Memory Protection mode is disabled. If WPS =0, all Individual Block Memory Protection commands are not available.

If WPS=1, the Individual Block Memory Protection mode is enabled, and BP mode is disabled. Blocks are individually protected by their own Individual Block Lock bit. On power-up, all blocks are write-protected by the Individual Block Lock bits by default, and the Individual Block Memory Protection commands are activated. The CMP, BP[4:0] bits of the Status Register are disabled and have no effect.

5.2.13 DC1/DC0

The Dummy Configuration (DC) bit, which is non volatile, selects the number of dummy cycles between the end of address and the start of read data output. Dummy cycles provide additional latency needed to complete the initial read access of the Flash array before data can be returned to the host system. Some read commands require additional dummy cycles as the SCK frequency increases.

Table 6, Table 7, and Table 8 provide different dummy cycle settings that are configured.

Table 6. STR Mode Dual I/O

DC Bit	Number of Dummy Cycles [1]	Dual I/O Fast Read (BBh)	Fast Read Dual I/O with 4-Byte Address (BCh)
00 (default)	4	108 MHz	108 MHz
01	8	166 MHz	166 MHz
10	12	166 MHz	166 MHz
11	16	166 MHz	166 MHz

1. The number of dummy cycles includes M7-0.

Table 7. STR Mode Quad I/O

DC Bit	Number of Dummy Cycles [1]	Dual I/O Fast Read (EBh)	Fast Read Dual I/O with 4-Byte Address (ECh)
00	6	80 MHz	80 MHz
01	10	133 MHz	133 MHz
10	14	166 MHz	166 MHz
11	18	166 MHz	166 MHz

1. The number of dummy cycles includes M7-0.

Table 8. DTR Mode

DC Bit	Number of Dummy Cycles [1]	DTR Fast Read Quad I/O (EDh)	DTR Quad I/O Fast Read with 4-Byte Address (EEh)
00	6	54 MHz	54 MHz
01	10	80 MHz	80 MHz
10	14	84 MHz	84 MHz
11	18	84 MHz	84 MHz

1. The number of dummy cycles includes M7-0.

5.2.13.1 DRV1/DRV0 Bits

The DRV1 and DRV0 bits determine the output driver strength for the Read command.

Table 9. DRV1 / DRV0 Bit Encoding

DRV1, DRV0	Driver Strength
00	100%
01	75%
10	50%
11	25%

6. Operating Features

6.1 Supply Voltage

6.1.1 Operating Supply Voltage

Prior to selecting the memory and issuing commands to it, a valid and stable V_{CC} voltage within the specified V_{CC} (min) / V_{CC} (max) range must be applied (see Section 8, Electrical Characteristics, on page 111). To secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a 0.1 µF to 1 µF low ESR/ESL capacitor placed close to the V_{CC}/GND package pins. This voltage must remain stable and valid until the end of the transmission of the command and, for a Write command, until the completion of the internal write cycle t_W).

6.1.2 Power-up Conditions

When the power supply is turned on, V_{CC} rises continuously from GND to V_{CC}. During this time, the Chip Select ($\overline{CS}$) line is not allowed to float but should follow the V_{CC} voltage; therefore, it is recommended to connect the $\overline{CS}$ line to V_{CC} through a pull-up resistor.

Also, the $\overline{CS}$ input is both edge sensitive and level sensitive. After power-up, the device does not become selected until a falling edge is first detected on $\overline{CS}$. This ensures that $\overline{CS}$ must have been High, prior to going Low to start the first operation.

6.1.3 Device Reset

To prevent inadvertent Write operations during power-up (continuous rise of V_{CC}), a power on reset (POR) circuit is included. At Power-up, the device does not respond to any command until V_{CC} has reached the power-on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined by the DC operating ranges).

When V_{CC} has passed the POR threshold, the device is reset.

6.1.4 Power-Down

At power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops from the normal operating voltage to below the power on reset threshold voltage, the device stops responding to any command sent to it. During Power-down, the device must be deselected (Chip Select ($\overline{CS}$) must be allowed to follow the voltage applied on V_{CC}) and in Standby Power mode (that is there must be no internal Write cycle in progress).

6.2 Active Power and Standby Power Modes

When Chip Select ($\overline{CS}$) is low, the device is selected and in the Active Power mode and consuming current (I_{CC}).

When Chip Select ($\overline{CS}$) is high, the device is deselected. If a Write cycle is not currently in progress, the device enters the Standby Power mode, and the current consumption drops to I_{CC1}.

6.3 Hold Condition

When QE = 0 and HOLD/RST = 0, the $\overline{HOLD}$ signal is used to pause any serial communications with the device without resetting the clocking sequence. During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCK) are don't care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{CS}$) low. Normally, the device remains selected for the duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the $\overline{HOLD}$ signal is driven low at the same time as Serial Clock (SCK) is low. The Hold condition ends when the $\overline{HOLD}$ signal is driven high at the same time as Serial Clock is low.

6.4 Software Reset and Hardware Reset

6.4.1 Software Reset

The AT25SF2561C / AT25QF2561C can be reset to the initial power-on state by a software reset sequence, either in SPI mode or QPI mode. This sequence must include two consecutive commands: Enable Reset (66h) and Reset (99h). If the command sequence is successfully accepted, the device takes approximately 300 µs (t_{RST}) to reset. No command is accepted during the reset period.

6.4.2 Hardware Reset ($\overline{\text{HOLD}}$ pin or $\overline{\text{RESET}}$ pin)

The AT25SF2561C / AT25QF2561C can also be configured to use the hardware $\overline{\text{RESET}}$ pin. The HOLD/RST bit in the Status Register 3 is the configuration bit for $\overline{\text{HOLD}}$ pin function or $\overline{\text{RESET}}$ pin function. When HOLD/RST=0 (factory default), the pin acts as a $\overline{\text{HOLD}}$ pin; when HOLD/RST=1, the pin acts as a $\overline{\text{RESET}}$ pin. Drive the $\overline{\text{RESET}}$ pin low for a minimum period of $t_{RESET(1)}$ to reset the device to its initial power-on state. Any on-going Program/Erase operation are interrupted, and data corruption can happen. While $\overline{\text{RESET}}$ is low, the device does not accept any command input.

If the QE bit is set to 1, the $\overline{\text{HOLD}}$ or $\overline{\text{RESET}}$ function is disabled, the pin becomes one of the four data I/O pins.

For the 16-pin SOP 300-mil package, the AT25SF2561C / AT25QF2561C provides a dedicated $\overline{\text{RESET}}$ pin in addition to the $\overline{\text{HOLD}}$/$\overline{\text{RESET}}$ (IO_3) pin. Drive the $\overline{\text{RESET}}$ pin low for the minimum $t_{RESET(1)}$ to reset the device to its initial power-on state. The HOLD/RST bit or QE bit in the Status Register does not affect the function of this dedicated $\overline{\text{RESET}}$ pin.

The hardware $\overline{\text{RESET}}$ pin has the highest priority among all the input signals. Drive $\overline{\text{RESET}}$ low for a minimum period of t_{RESET} [1] to interrupt any on-going external/internal operations, regardless of the status of other SPI signals ($\overline{\text{CS}}$, SCK, IOs, $\overline{\text{WP}}$ and $\overline{\text{HOLD}}$).

Notes:

1. While a faster $\overline{\text{RESET}}$ pulse (as short as a few hundred nanoseconds) often resets the device, a t_{RST} minimum pulse is recommended to ensure reliable operation.
2. There is an internal pull-up resistor for the dedicated $\overline{\text{RESET}}$ pin on the 16-pin SOP 300-mil package. If the reset function is not used, this pin can be left floating.

6.4.3 Hardware Reset (JEDEC Standard Hardware Reset)

The AT25SF2561C / AT25QF2561C supports JEDEC Standard Hardware Reset. The JEDEC Standard Hardware Reset sequence also can be used to reset the device to its power-on state without cycling power.

The reset sequence does not use the SCK pin. SCK must be low (mode 0) or high (mode 3) throughout the entire reset sequence. This prevents any confusion with it being an command, since no command bits are transferred (clocked).

A reset is commanded when the data on the SI pin is 0101 on four consecutive positive edges of the $\overline{CS}$ pin with no edge on the SCK pin throughout. There is a sequence where:

1. $\overline{CS}$ is driven active low to select the device.
2. The clock (SCK) remains stable in either a high or low state.
3. SI is driven low by the bus master, simultaneously with $\overline{CS}$ going active low. No SPI bus slave drives SI during $\overline{CS}$ low before a transition of SCK; that is: slave streaming output active is not allowed until after the first edge of SCK.
4. $\overline{CS}$ is driven inactive. The slave captures the state of SI on the rising edge of $\overline{CS}$.

The above steps are repeated four times, each time alternating the state of SI.

After the fourth $\overline{CS}$ pulse, the slave triggers its internal reset. SI is low on the first $\overline{CS}$, high on the second, low on the third, high on the fourth. This provides a value of 5h, unlike random noise. Any activity on SCK during this time halts the sequence, and a Reset is not generated. Figure 5 shows the timing for hardware Reset operation.

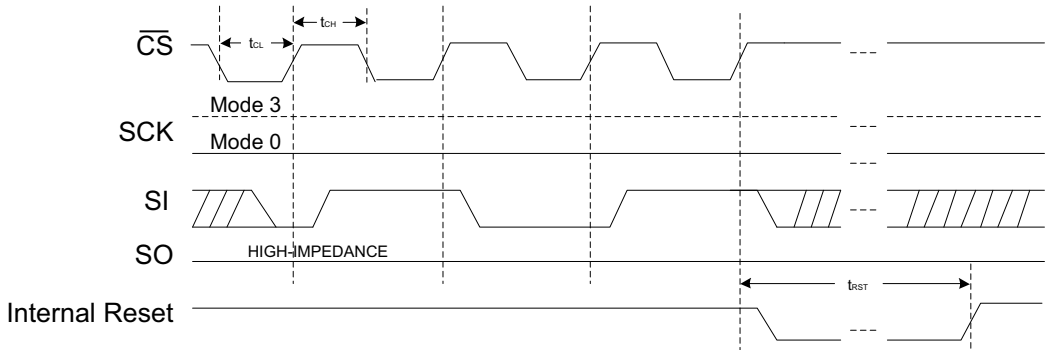


Figure 5. JEDEC Standard Hardware Reset

Table 10. JEDEC Standard Hardware Reset Timing Parameters

Parameters	Min	Typ.	Max.	Unit
t_{CL}	20			ns
t_{CH}	20			ns
Setup Time	5			ns
Hold Time	5			ns

6.5 Write Protect Features

1. Software Protection (Memory array):
   - The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but not changed.
   - Individual Block Memory Protection (Solid and Password Protect): The AT25SF2561C / AT25QF2561C also provides another Write Protect method using the Individual Block Memory Protection. Each 64-kB block (except the top and bottom blocks, total of 510 blocks) and each 4-kB block within the top/bottom blocks (total of 32 blocks) are equipped with the Individual Block Lock bit. When the Individual Block Lock bit is 0, the corresponding block can be erased or programmed; when the Individual Block Lock bit is set to 1, Erase or Program commands issued to the corresponding block are ignored.

     The WPS bit in Status Register 3 is used to decide which Write Protect scheme is used. When WPS=0 (factory default), the device uses only CMP, BP[4:0] bits to protect specific areas of the array; when WPS=1, the device uses the Individual Block Memory Protection for write protection.
2. Hardware Protection (Status register): $\overline{WP}$ going low to protected the writable bits of Status Register.
3. Deep Power-Down: In Deep Power-Down Mode, all commands are ignored except Release from Deep Power-Down Mode.
4. The device resets when V_{CC} is below threshold: On power-up or at power-down, the AT25SF2561C / AT25QF2561C stays in the reset condition while V_{CC} is below the threshold value of V_{WI}. While reset, all operations are disabled, and no commands are recognized.
5. Time delay write disable after power-up, during power-up, and after the V_{CC} voltage exceeds V_{CC} (min), all program and erase related commands are further disabled for a time delay of t_{VSL}. This includes the Write Enable, Page Program, Block Erase, Chip Erase, and Write Status Register commands.
6. Write Enable: The Write Enable command is set with the Write Enable Latch bit. The WEL bit returns to reset under the following conditions:
   - Power-up
   - Write Disable
   - Write Status Register (when the SR is protected, WEL returns to reset)
   - Write Extended Address Register (when in three-byte Address Mode)
   - After some Individual Block Memory Protection commands that require the Write Enable command (see Table 27) are executed correctly, the WEL bit returns to reset (when WPS=1)
   - Page Program if the program area is protected, WEL returns to reset)
   - Block Erase/Chip Erase (if the erase area is protected, WEL returns to reset)
   - Software Reset
   - Hardware Reset
7. One Time Program (OTP) write protection for array and Security Registers using the Status Register.

6.6 Array Memory Protection

6.6.1 Block Protect Table (WPS = 0)

Table 11. AT25SF2561C / AT25QF2561C Status Register Memory Protection (CMP = 0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Protected Blocks	Addresses	Density	Portion
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	511	01FF0000h - 01FFFFFFh	64 kB	Upper 1/512
0	0	0	1	0	510 to 511	01FE0000h - 01FFFFFFh	128 kB	Upper 1/256
0	0	0	1	1	508 to 511	01FC0000h - 01FFFFFFh	256 kB	Upper 1/128
0	0	1	0	0	504 to 511	01F80000h - 01FFFFFFh	512 kB	Upper 1/64
0	0	1	0	1	496 to 511	01F000000h - 01FFFFFFh	1 MB	Upper 1/32
0	0	1	1	0	480 to 511	01E00000h - 01FFFFFFh	2 MB	Upper 1/16
0	0	1	1	1	448 to 511	01C00000h - 01FFFFFFh	4 MB	Upper 1/8
0	1	0	0	0	384 to 511	01800000h - 01FFFFFFh	8 MB	Upper 1/4
0	1	0	0	1	256 to 511	01000000h - 01FFFFFFh	16 MB	Upper 1/2
1	0	0	0	1	0	00000000h - 0000FFFFh	64 kB	Lower 1/512
1	0	0	1	0	0 to 1	00000000h - 0001FFFFh	128 kB	Lower 1/256
1	0	0	1	1	0 to 3	00000000h - 0003FFFFh	256 kB	Lower 1/128
1	0	1	0	0	0 to 7	00000000h - 0007FFFFh	512 kB	Lower 1/64
1	0	1	0	1	0 to 15	00000000h - 000FFFFFh	1 MB	Lower 1/32
1	0	1	1	0	0 to 31	00000000h - 001FFFFFh	2 MB	Lower 1/16
1	0	1	1	1	0 to 63	00000000h - 003FFFFFh	4 MB	Lower 1/8
1	1	0	0	0	0 to 127	00000000h - 007FFFFFh	8 MB	Lower 1/4
1	1	0	0	1	0 to 255	00000000h - 00FFFFFFh	16 MB	Lower 1/2
X	1	1	0	X	0 to 511	00000000h - 01FFFFFFh	32 MB	All
X	1	X	1	X	0 to 511	00000000h - 01FFFFFFh	32 MB	All

Table 12. AT25SF2561C / AT25QF2561C Status Register Memory Protection (CMP = 1)

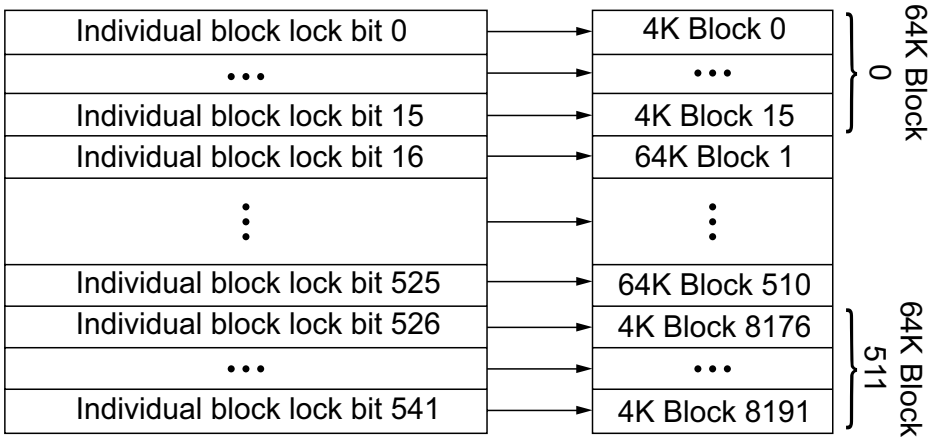
Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Protected Blocks	Addresses	Density	Portion
X	0	0	0	0	All	00000000h - 01FFFFFFh	All	All
0	0	0	0	1	0 to 510	00000000h - 10FEFFFFh	32,704 kB	Lower 511/512
0	0	0	1	0	0 to 509	00000000h - 01FDFFFFh	32,640 kB	Lower 255/256
0	0	0	1	1	0 to 507	00000000h - 01FBFFFFh	32,512 kB	Lower 127/128
0	0	1	0	0	0 to 503	00000000h - 01F7FFFFh	32,256 kB	Lower 63/64
0	0	1	0	1	0 to 495	00000000h - 01EFFFFFh	31 MB	Lower 31/32
0	0	1	1	0	0 to 479	00000000h - 01DFFFFFh	30 MB	Lower 15/16
0	0	1	1	1	0 to 447	00000000h - 01BFFFFFh	28 MB	Lower 7/8
0	1	0	0	0	0 to 383	00000000h - 017FFFFFh	24 MB	Lower 3/4
0	1	0	0	1	0 to 255	00000000h - 00FFFFFFh	16 MB	Lower 1/2
1	0	0	0	1	1 to 511	00010000h - 01FFFFFFh	32,704 kB	Upper 511/512
1	0	0	1	0	2 to 511	00020000h - 01FFFFFFh	32,640 kB	Upper 255/256
1	0	0	1	1	4 to 511	00040000h - 01FFFFFFh	32,512 kB	Upper 127/128
1	0	1	0	0	8 to 511	00080000h - 01FFFFFFh	32,256 kB	Upper 63/64
1	0	1	0	1	16 to 511	00100000h - 01FFFFFFh	31 MB	Upper 31/32
1	0	1	1	0	32 to 511	00200000h - 01FFFFFFh	30 MB	Upper 15/16
1	0	1	1	1	64 to 511	00400000h - 01FFFFFFh	28 MB	Upper 7/8
1	1	0	0	0	128 to 511	00800000h - 01FFFFFFh	24 MB	Upper 3/4
1	1	0	0	1	256 to 511	01000000h - 01FFFFFFh	16 MB	Upper 1/2
X	1	1	0	X	None	None	None	None
X	1	X	1	X	None	None	None	None

6.6.2 Individual Block Memory Protection (WPS = 1)

Individual Block Memory Protection can protect individual 4 kB blocks in the bottom and top 64 kB of memory and protect individual 64 kB blocks in the rest of memory.

There is one volatile individual block lock bit assigned to each 4 kB block at the bottom and top 64 kB of memory, as well as to each 64 kB block in the rest of memory. A block is write-protected from programming or erasing when its associated individual block lock bit is set to 1.

Note: If WPS=0, Individual Block Memory Protection commands (Section 7.7.1 through Section 7.7.5) are not available.



Notes: 1. Individual block protection is only valid when WPS = 1.
2. When Individual block protection is in effect (WPS=1) all individual block lock bits are set to 1 by default after power-up (the entire memory array is protected).

Figure 6. Individual Block Lock Bit for Block Array

6.6.2.1 Individual Block Lock Bit

The individual block lock bits are volatile bits for quickly and easily enabling or disabling write protection to blocks. An individual block lock bit is assigned to each 4 kB block in the bottom and top 64 kB of memory and to each 64 kB block in the rest of the memory.

When an individual block lock bit is 1, the associated block is write protected, preventing any program or erase operation on the block. All individual block lock bits default to 1 after power-on or reset.

Individual block lock bits can be set to 1 by the Individual Block Lock command. The individual block lock bits can also be globally cleared to 0 with the Global Block Unlock command. A Write Enable command must be executed to set the WEL bit before sending the Individual Block Lock, Individual Block Unlock, Global Block Lock, or Global Block Unlock command.

The Read Block Lock command reads the status of the individual block lock bit of a block. The Read Block Lock command returns 00h if the individual block lock bit is 0, indicating write protection is disabled. The Read Block Lock Status command returns FFh if the individual block lock bit is 1, indicating write protection is enabled.

Table 13. Individual Protection Bit

Description	Bit Status	Default	Type
Individual Block Lock bit	0 = Unprotect Block 1 = Protect Block	1	Volatile

6.7 Extended Address Register

In addition to the Status Registers, the AT25SF2561C / AT25QF2561C also provides a volatile Extended Address Register that allows the 256 Mb area of the device to be used normally in three-byte Address Mode. The value of the Extended Address Register and the 24-bit address input in the three-byte Address Mode together form the complete start address of the command operation. That is, when A24 = 0, the starting address of the command operation selects the lower 128 Mb memory array (00000000h 00FFFFFFh). When A24 = 1, the start address of the command operation selects the high 128 Mb memory array (01000000h 01FFFFFFh).

Notes

1. In three-byte Address Mode, when A24 = 0 /1, the starting address of the command operation selects the lower high-128-Mb memory array. However, as the command operation address continues to be carried, the address of the command operation can enter the high lower-128-Mb memory array. At this time, the value of the Extended Address Register does not change with the carry of the address; that is, the value of Extended Address Register can only be modified by the Write Extended Address Register command.
2. In four-byte Address Mode, Extended Address Register is not available. The value of Extended Address Register has no effect on the command operation. The device requires four-byte address input for all address related commands, and the Extended Address Register setting is ignored. The Read Extended Address Register and Write Extended Address Register commands are not available in the four-byte Address Mode. At the same time, during the command operation, the same as in the three-byte Address Mode, the carry of the address does not have any effect on the Extended Address Register.

Table 14. Extended Address Register

EA7	EA6	EA5	EA4	EA3	EA2	EA1	EA0
A31 [1]	A30 [1]	A29 [1]	A28[1]	A27 [1]	A26 [1]	A25 [1]	A24 [2]

1. Reserved for higher densities: 512 Mb ~ 32 Gb.
2. Address Bit #24: A24 = 0: Select lower 128 Mb; A24 = 1: Select upper 128 Mb.

7. Command Set

All commands, addresses, and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCK after $\overline{CS}$ is driven low. Then, the one byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on a rising edge of SCK.

In Table 15, every command sequence starts with a one byte command code. Depending on the command, this can be followed by address bytes, or by data bytes, by both, or none. $\overline{CS}$ must be driven high after the last bit of the command sequence has been shifted in. For the Read, Fast Read, Read Status Register, Release from Deep Power-Down, and Read Device ID commands, the shifted in command sequence is followed by a data out sequence. $\overline{CS}$ can be driven high after any bit of the data out sequence is shifted out.

For the Page Program, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable, or Deep Power-Down command, $\overline{CS}$ must be driven high exactly at a byte boundary; otherwise, the command is rejected (not executed). That is, $\overline{CS}$ must go high when the number of clock pulses after $\overline{CS}$ driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing happens, and WEL is not reset.

Table 15. Command Set Table: Standard/Dual/Quad SPI Commands, 3-Byte and 4-Byte Mode [1]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0-7)**	**(8-15)**	**(16-23)**	**(24-31)**	**(32-39)**	**(40-47)**	**(48-55)**
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Read Status Register 1	05h	(SR1 Bits 7-0)[2]					
Write Status Register[4]	01h	(SR1 Bits 7-0)[4]	(SR2 Bits 7-0)				
Read Status Register 2	35h	(SR2 Bits 7-0)[2]					
Write Status Register 2	31h	(SR2 Bits 7-0)					
Read Status Register 3	15h	(SR3 Bits 7-0)[2]					
Write Status Register 3	11h	(SR3 Bits 7-0)					
Chip Erase	C7h/60h						
Program/Erase Suspend	75h						
Program/Erase Resume	7Ah						
Deep Power-down	B9h						
Release Power-down / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)[2]		
Release Power-down	ABh						
Manufacturer/Device ID	90h	Dummy	Dummy	00/01h	(MF7-MF0)/ (ID7-ID0)	(ID7-ID0))/ (MF7-MF0)	
Read JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)[9]			
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Enter QPI Mode	38h						
Enable Reset	66h						
Reset Device	99h						
Read Data with 4-Byte Address	13h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read with 4-Byte Address	0Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Fast Read Dual Output with 4-Byte Address	3Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0, …)[7]
Fast Read Quad Output with 4-Byte Address	6Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0, …)[9]
Data Input Output	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**
Clock Number	**(0-7)**	**(8-11)**	**(12-15)**	**(16-19)**	**(20-23)**	**(24-27)**	**(28-31)**
Fast Read Dual I/O with 4-Byte Address	BCh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)

Table 15. Command Set Table: Standard/Dual/Quad SPI Commands, 3-Byte and 4-Byte Mode [1] *(continued)*

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Clock Number	(**0-7**)	(**8-9**)	(**10-11**)	(**12-13**)	(**14-15**)	(**16-17**)	(**18-19**)	(**20-21**)	(**22-23**)
Fast Read Quad I/O with 4-Byte Address	ECh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(D7-D0)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	(**0-7**)	(**8-9**)	(**10-11**)	(**12-13**)	(**14-15**)	(**16-17**)	(**18-19**)
Page Program with 4-Byte Address	12h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)[3]
Quad Page Program with 4-Byte Address	34h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Block Erase (4kB) with 4-Byte Address	21h	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32K) with 4-Byte Address	5Ch	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase(64K) with 4-Byte Address	DCh	A31-A24	A23-A16	A15-A8	A7-A0		
Global Block Lock	7Eh						
Global Block Unlock	98h						

Table 16. Command Set Table: Standard/Dual/Quad SPI Commands, 3-Byte Address Mode [1]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Clock Number	**0-7**	**8-15**	**16-23**	**24-31**	**32-39**	**40-55**
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummy	(ID127-ID0)
Clock Number	**0-7**	**8-15**	**16-23**	**24-31**	**32-39**	**40-47**
Page Program	02h	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)[3]
Quad Page Program	32h	A23-A16	A15-A8	A7-A0	(D7-D0, …)[9]	(D7-D0, …)[3]
Block Erase (4 kB)	20h	A23-A16	A15-A8	A7-A0		
Block Erase (32 kB)	52h	A23-A16	A15-A8	A7-A0		
Block Erase (64 kB)	D8h	A23-A16	A15-A8	A7-A0		
Normal Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next Byte)
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Dual Output Fast read	3Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)[7]
Quad Output Fast read	6Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)[9]
Erase Security Registers[5]	44h	A23-A16[8]	A15-A8[8]	A7-A0[8]		
Program Security Registers[5]	42h	A23-A16[8]	A15-A8[8]	A7-A0[8]	D7-D0	Next Byte
Read Security Registers[5]	48h	A23-A16[8]	A15-A8[8]	A7-A0[8]	Dummy	D7-D0

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**0-7**	**8-11**	**12-15**	**16-19**	**20-23**	**24-27**	**28-31**
Dual I/O Fast read	BBh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Mftr./Device ID Dual I/O	92h	A23-A16	A15-A8	A7-A0	Dummy	(MF7-MF0)	(ID7-ID0)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Clock Number	**0-7**		**10-11**	**12-13**	**14-15**	**16-17**	**18-19**	**20-21**	**22-23**
Set Burst With Wrap	77h	Dummy	Dummy	Dummy	W6-W4				
Quad I/O Fast read	EBh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(D7-D0)	(D7-D0)
Mftr./Device ID Quad I/O	94h	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)
Read Block Lock	3Dh	A23-A16	A15-A8	A7-A0	(D7-D0)				
Individual Block Lock	36h	A23-A16	A15-A8	A7-A0					
Individual Block Unlock	39h	A23-A16	A15-A8	A7-A0					
Enter 4-Byte Address Mode	B7h								
Read Extended Addr. Register	C8h	(EA7-EA0)[2]							
Write Extended Addr. Register	C5h	(EA7-EA0)							

Table 17. Command Set Table: Standard/Dual/Quad SPI Commands, 4-Byte Address Mode [1]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**0-7**	**8-15**	**16-23**	**24-31**	**32-39**	**40-47**	**48-63**
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummy	Dummy	ID127-ID0
Clock Number	**0-7**	**8-15**	**16-23**	**24-31**	**32-39**	**40-47**	**48-55**
Page Program	02h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0[3]
Quad Page Program	32h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0, …[9]	D7-D0, …[3]
Block Erase (4-kB)	20h	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32-kB)	52h	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64-kB)	D8h	A31-A24	A23-A16	A15-A8	A7-A0		
Normal Read Data	03h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte
Fast Read	0Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0
Dual Output Fast read	3Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0[7]
Quad Output Fast read	6Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0[9]
Erase Security Registers[5]	44h	A31-A24	A23-A16[8]	A15-A8[8]	A7-A0[8]		
Program Security Registers[5]	42h	A31-A24	A23-A16[8]	A15-A8[8]	A7-A0[8]	D7-D0	Next Byte
Read Security Registers[5]	48h	A31-A24	A23-A16[8]	A15-A8[8]	A7-A0[8]	Dummy	D7-D0

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number	**0-7**	**8-11**	**12-15**	**16-19**	**20-23**	**24-27**	**28-31**	**22-35**
Dual I/O Fast read	BBh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	D7-D0
Mftr./Device ID Dual I/O	92h	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	MF7-MF0	ID7-ID0

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10
Clock Number	**0-7**	**8-9**	**10-11**	**12-13**	**14-15**	**16-17**	**18-19**	**20-21**	**22-23**	**24-25**
Set Burst With Wrap	77h	Dummy	Dummy	Dummy	Dummy	W6-W4				
Quad I/O Fast read	EBh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	D7-D0	D7-D0
Mftr./Device ID Quad I/O	94h	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	MF7-MF0	D7-D0
Read Block Lock	3Dh	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0				
Individual Block Lock	36h	A31-A24	A23-A16	A15-A8	A7-A0					
Individual Block Unlock	39h	A31-A24	A23-A16	A15-A8	A7-A0					
Exit 4-Byte Address Mode	E9h									

Table 18. Command Set Table: QPI Commands, 3- and 4-Byte Address Mode [14]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number	**(0-1)**	**(2-3)**	**(4- 5)**	**(6- 7)**	**(8-9)**	**(10-11)**	**(12-13)**	**(14-15)**
Write Enable	06h							
Volatile SR Write Enable	50h							
Write Disable	04h							
Read Status Register 1	05h	(SR1 Bits 7-0)(2)						
Write Status Register 1 [4]	01h	(SR1 Bits 7-0)(4)	(SR2 Bits 7-0)					
Read Status Register 2	35h	(SR2 Bits 7-0)(2)						
Write Status Register 2	31h	(SR2 Bits 7-0)						
Read Status Register 3	15h	(SR3 Bits 7-0)(2)						
Write Status Register 3	11h	(SR3 Bits 7-0)						
Chip Erase	C7h/60h							
Erase / Program Suspend	75h							
Erase / Program Resume	7Ah							
Power-down	B9h							
Set Read Parameters	C0h	P7-P0						
Release Power-down / ID	ABh	Dummy	Dummy	Dummy	ID7-ID0(2)			
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)	ID7-ID0		
JEDEC ID	9Fh	MF7-MF0	ID15-ID8	ID7-ID0				
Exit QPI Mode	FFh							
Enable Reset	66h							
Reset Device	99h							
Fast Read Quad I/O with 4-Byte Address	ECh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0(15)	Dummy	D7-D0
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	Dummy	D7-D0		
Page Program with4-Byte Address	12h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	
Block Erase (4 kB) with 4-Byte Address	21h	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase(32 kB) with 4-Byte Address	5Ch	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase(64 kB) with 4-Byte Address	DCh	A31-A24	A23-A16	A15-A8	A7-A0			

Table 19. Command Set Table: QPI Commands, 3-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**0-1**	**2-3**	**4-5**	**6-7**	**8-9**	**10-11**	**12-13**
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0(9)	D7-D0(3)	
Block Erase (4-kB)	20h	A23-A16	A15-A8	A7-A0			
Block Erase (32-kB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase (64-kB)	D8h	A23-A16	A15-A8	A7-A0			
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy(15)	D7-D0	
Burst Read with W rap(16)	0Ch	A23-A16	A15-A8	A7-A0	Dummy(15)	D7-D0	
Fast Read Quad I/O	EBh	A23-A16	A15-A8	A7-A0	M7-M0(15)	Dummy	D7-D0
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummys*	ID127-ID0	
Read Security Registers(5)	48h	A23-A16(8)	A15-A8(8)	A7-A0(8)	Dummy	D7-D0	
Erase Security Registers(5)	44h	A23-A16(8)	A15-A8(8)	A7-A0(8)			
Program Security Registers(5)	42h	A23-A16(8)	A15-A8(8)	A7-A0(8)	D7-D0	Next Byte	
Read Block Lock	3Dh	A23-A16	A15-A8	A7-A0	D7-D0		
Individual Block Lock	36h	A23-A16	A15-A8	A7-A0			
Individual Block Unlock	39h	A23-A16	A15-A8	A7-A0			
Enter 4-Byte Address Mode	B7h						
Read Extended Addr. Register	C8h	EA7-EA0(2)					
Write Extended Addr. Register	C5h	EA7-EA0					

Table 20. Command Set Table: QPI Commands, 4-Byte Address Mode (14)

Data Input Output	Byte 1	2	3	4	5	6	7	8
Clock Number	**0-1**	**2-3**	**4-5**	**6-7**	**8-9**	**10-11**	**12-13**	**13-14**
Page Program	02h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0(9)	D7-D0(3)	
Block Erase (4-kB)	20h	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase (32-kB)	52h	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase (64-kB)	D8h	A31-A24	A23-A16	A15-A8	A7-A0			
Fast Read	0Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(15)	D7-D0	
Burst Read with Wrap(16)	0Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(15)	D7-D0	
Fast Read Quad I/O	EBh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0(15)	Dummy	D7-D0
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummy	Dummys*	ID127-ID0	
Read Security Registers(5)	48h	A31-A24	A23-A16(8)	A15-A8(8)	A7-A0(8)	Dummy	D7-D0	
Erase Security Registers(5)	44h	A31-A24	A23-A16(8)	A15-A8(8)	A7-A0(8)			
Program Security Registers(5)	42h	A31-A24	A23-A16(8)	A15-A8(8)	A7-A0(8)	D7-D0	Next Byte	
Read Block Lock	3Dh	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0		
Individual Block Lock	36h	A31-A24	A23-A16	A15-A8	A7-A0			
Individual Block Unlock	39h	A31-A24	A23-A16	A15-A8	A7-A0			
Exit 4-Byte Address Mode	E9h							

Table 21. Command Set Table-DTR with SPI Commands, 3-Byte & 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(1-1-1)	**8**	**4**	**4**	**4**	**6**	**4**	**4**
DTR Quad I/O Fast Read with 4- Byte Address	EEh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	D7-D0

Table 22. Command Set Table-DTR with QPI Commands, 3-Byte & 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(1-1-1)	**8**	**4**	**4**	**4**	**6**	**4**	**4**
DTR Quad I/O Fast Read with 4- Byte Address	EEh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	D7-D0

Table 23. Command Set Table-DTR with SPI Commands, 3-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(1-4-4)	**8**	**1**	**1**	**1**	**1**	**7**	**1**
DTR Fast Read Quad I/O	EDh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0

Table 24. Command Set Table-DTR with SPI Commands, 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(1-4-4)	**8**	**1**	**1**	**1**	**1**	**7**	**1**
DTR Fast Read Quad I/O	EDh	A31-A16	A15-A0	M7-M0	Dummy	D7-D0	

Table 25. Command Set Table-DTR with QPI Commands, 3-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(4-4-4)	**2**	**1**	**1**	**1**	**8**	**1**	**1**
DTR Read with Wrap(13)	0Eh	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
Clock Number(4-4-4)	**2**	**1**	**1**	**1**	**1**	**7**	**1**
DTR Fast Read Quad I/O	EDh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0

Table 26. Command Set Table-DTR with QPI Commands, 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number(4-4-4)	**2**	**1**	**1**	**1**	**61**	**8**	**1**	**1**
DTR Read with Wrap(13)	0Eh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
Clock Number(4-4-4)	**2**	**1**	**1**	**1**	**1**	**1**	**7**	**1**
DTR Fast Read Quad I/O	EDh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0

Notes:

1. Data bytes are shifted, with the most significant bit first.
2. The Status Register contents and Device ID repeat continuously until $\overline{CS}$ terminates the command.
3. At least one byte of data input is required for Page Program, Quad Page Program, and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing wraps to the beginning of the page and overwrites previously sent data.
4. When the Write Status Register command 01h is followed by one byte of data, the data are written to Status Register 1. When the Write Status Register command 01h is followed by two bytes of data, the first byte data is written to Status Register 1, and the second byte data is written to Status Register 2; see Write Status Register (01h or 31h or 11h).
5. Security Register Address:
   Security Register 1: A23-16=00h; A15-12=0001; A11-9=000; A8-0=byte address
   Security Register 2: A23-16=00h; A15-12=0010; A11-9=000; A8-0=byte address
   Security Register 3: A23-16=00h; A15-12=0011; A11-9=000; A8-0=byte address
6. Dual SPI address input format:
   IO_0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   IO_1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1

7. Dual SPI data output format:
   IO_0 = (D6, D4, D2, D0) IO_1 = (D7, D5, D3, D1)
8. Quad SPI address input format: Set Burst with Wrap input format:
   IO_0 = A20, A16, A12, A8, A4, A0, M4, M0, IO_0 = x, x, x, x, x, x, W4, x
   IO_1 = A21, A17, A13, A9, A5, A1, M5, M1, IO_1 = x, x, x, x, x, x, W5, x
   IO_2 = A22, A18, A14, A10, A6, A2, M6, M2, IO_2 = x, x, x, x, x, x, W6, x
   IO_3 = A23, A19, A15, A11, A7, A3, M7, M3, IO_3 = x, x, x, x, x, x, x, x
9. Quad SPI data input/output format:
   IO_0 = (D4, D0, ...)
   IO_1 = (D5, D1, ...)
   IO_2 = (D6, D2, ...)
   IO_3 = (D7, D3, ...)
10. Fast Read Quad I/O data output format:
    IO_0 = (x, x, x, x, D4, D0, D4, D0)
    IO_1 = (x, x, x, x, D5, D1, D5, D1)
    IO_2 = (x, x, x, x, D6, D2, D6, D2)
    IO_3 = (x, x, x, x, D7, D3, D7, D3)
11. Word Read Quad I/O data output format:
    IO_0 = (x, x, D4, D0, D4, D0, D4, D0)
    IO_1 = (x, x, D5, D1, D5, D1, D5, D1)
    IO_2 = (x, x, D6, D2, D6, D2, D6, D2)
    IO_3 = (x, x, D7, D3, D7, D3, D7, D3)
12. For Word Read Quad I/O, the lowest address bit must be 0 (A0 = 0).
13. The lowest four address bits must be 0 (A3, A2, A1, A0 = 0).
14. QPI Command, Address, Data input/output format:

SCK #	0, 1	2, 3	4, 5	6, 7	8, 9	10, 11
IO_0 =	C4, C0,	A20, A16	A12, A8	A4, A0	D4, D0	D4, D0
IO_1 =	C5, C1,	A21, A17	A13, A9	A5, A1	D5, D1	D5, D1
IO_2 =	C6, C2,	A22, A18	A14, A10	A6, A2	D6, D2	D6, D2
IO_3 =	C7, C3,	A23, A19	A15, A11	A7, A3	D7, D3	D7, D3

15. The number of dummy clocks for QPI Fast Read, QPI Fast Read Quad I/O & QPI Burst Read with Wrap is controlled by read parameter P7 – P4.
16. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 – P0.

Table 27. Commands that must send Write Enable / Write Enable for Volatile Status Register Command

Mode	Command	Opcode	Write
SPI/QPI	Write Status Register	01h, 31h, 11h	06h, 50h
	Write Extended Address Register	C5h	06h
	Erase Security Registers	44h	06h
	Program Security	42h	06h
	Page Program	02h	06h
	Page Program with 4-Byte Address	12h	06h
SPI	Quad Page Program	32h	06h
	Quad Input Page Program with 4-Byte Address	34h	06h
SPI/QPI	4-kB Block Erase	20h	06h
	4-kB Block Erase with 4-Byte Address	21h	06h
	32-kB Block Erase	52h	06h
	32-kB Block Erase with 4-Byte Address	5Ch	06h
	64-kB Block Address	D8h	06h
	64-kB Block Address with 4-Byte Address	DCh	06h
	Chip Erase	60h/C7h	06h
	Individual Block Lock	36h	06h
	Individual Block Unlock	39h	06h
	Global Block Lock	7Eh	06h
	Global Block Unlock	98h	06h

7.1 Configuration and Status Commands

7.1.1 Write Enable (06h)

The Write Enable command is for setting the Write Enable Latch (WEL) bit. The WEL bit must be set prior to every *Page Program*, *Block Erase*, *Chip Erase*, *Write Status Register*, and *Erase/Program Security Registers* command. The Write Enable command sequence is: $\overline{CS}$ goes low sending the Write Enable command $\overline{CS}$ goes high.

Note that this command is not accepted when the Write Enable for Volatile Status Register command is valid. If the Write Enable command is to be sent, but it is not known if the Write Enable for Volatile Status Register command is valid, send the Write Disable command first.

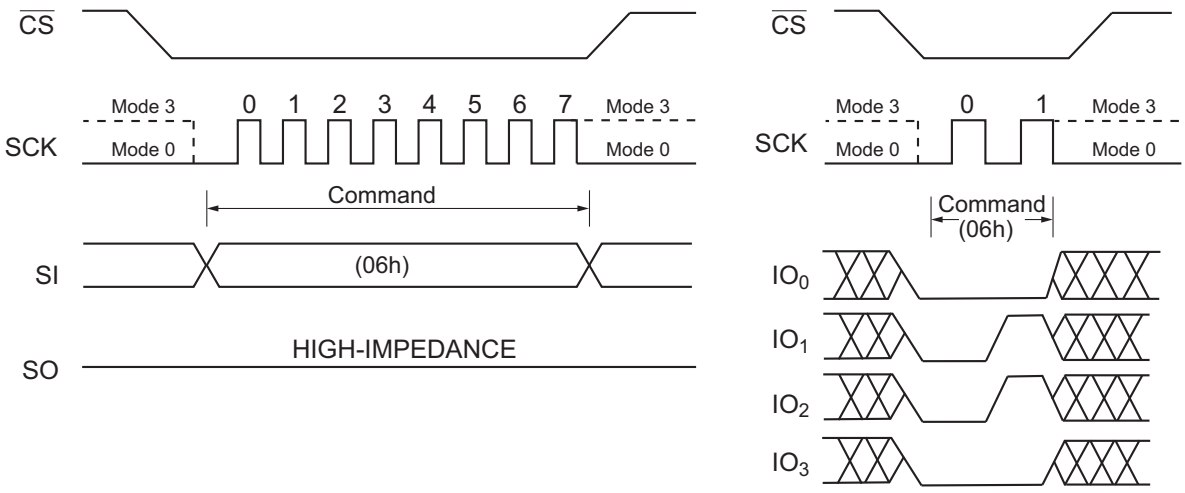


Figure 7. Write Enable Sequence Diagram (SPI left, QPI right)

7.1.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits can also be written to as volatile bits (HOLD/RES, DRV1, DRV0, CMP, QE, SRP1, SRP0, BP4, BP3, BP2, BP1, BP0). This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command does not set the Write Enable Latch bit, it is only valid for the Write Status Registers command to change the volatile Status Register bit values. (After the software/hardware reset or re-powered, the volatile Status Register bit values are restored to the default value or the value input by the Write Enable command).

Note that if the Write Enable command is valid when the Write Enable for Volatile Status Register command is sent, the latter is not accepted. Thus, when sending the Write Enable for Volatile Status Register command, first ensure that the Write Enable command is not valid.

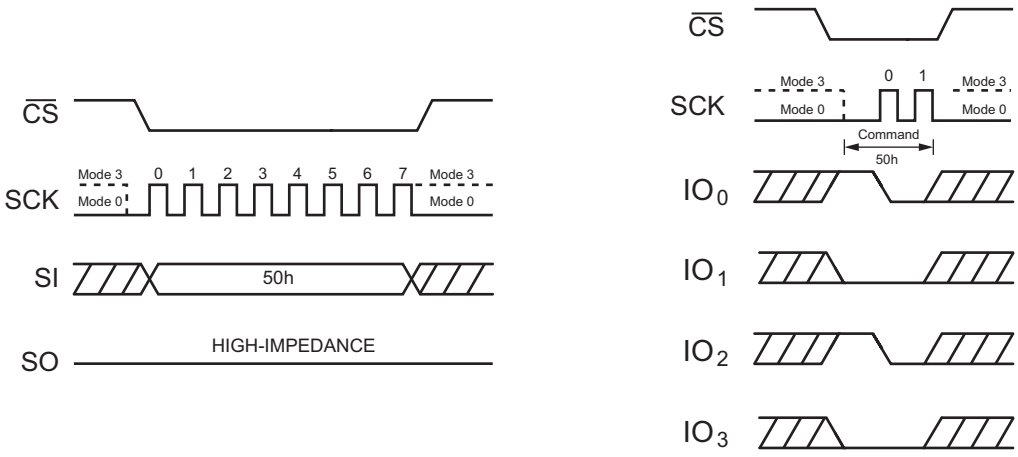


Figure 8. Write Enable for Volatile Status Register (SPI left, QPI right)

7.1.3 Write Disable (04h)

The Write Disable command is for resetting the Write Enable Latch bit. The Write Disable command sequence: $\overline{CS}$ goes low → sending the Write Disable command → $\overline{CS}$ goes high. The WEL bit is reset by following condition: Power-up and on completion of the *Write Status Register*, *Page Program*, *Block Erase*, *Chip Erase*, *Erase/Program Security Registers,* and *Reset* commands.

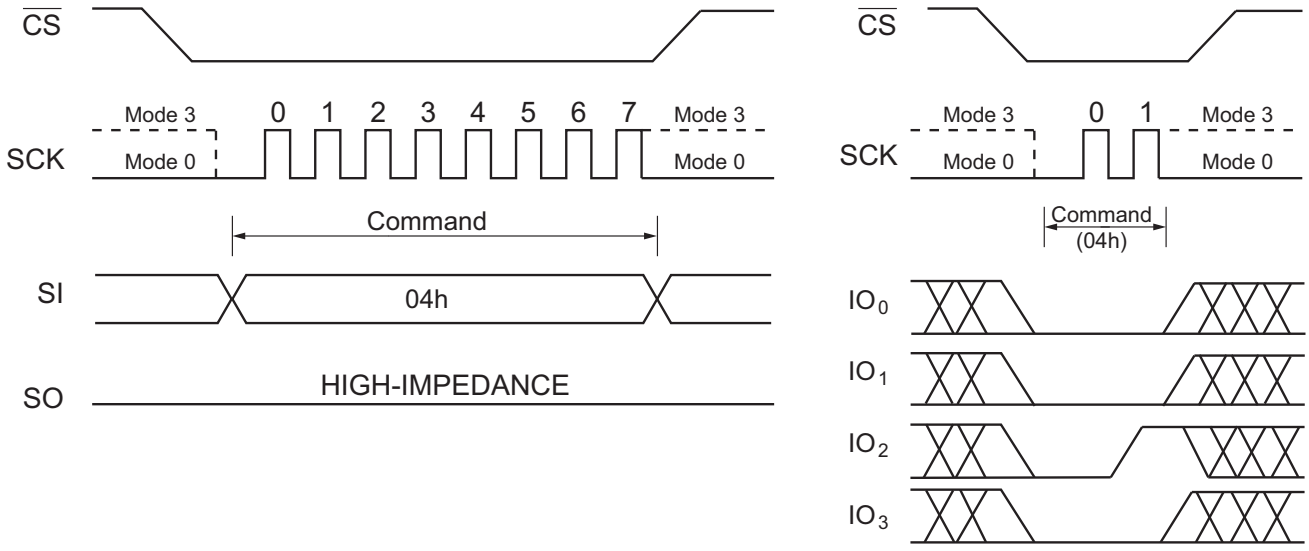


Figure 9. Write Disable Sequence Diagram

7.1.4 Read Status Register (05h or 35h or 15h)

The three Read Status Register commands are used for reading Status Register 1, 2 and 3. Each Status Register can be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the RDY/BSY bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code 05h, the SO pin outputs bits 7-0 from Status Register 1. For command code 35h, the SO pin outputs bits 7-0 from Status Register 2. For command code 15h, the SO pin outputs bits 7-0 from Status Register 3.

Figure 10 shows a Read Status Register operation for Status Register 1 (05h). The Read Status Register 2 and 3 operations are similar, but with a different opcode in the first eight clocks.

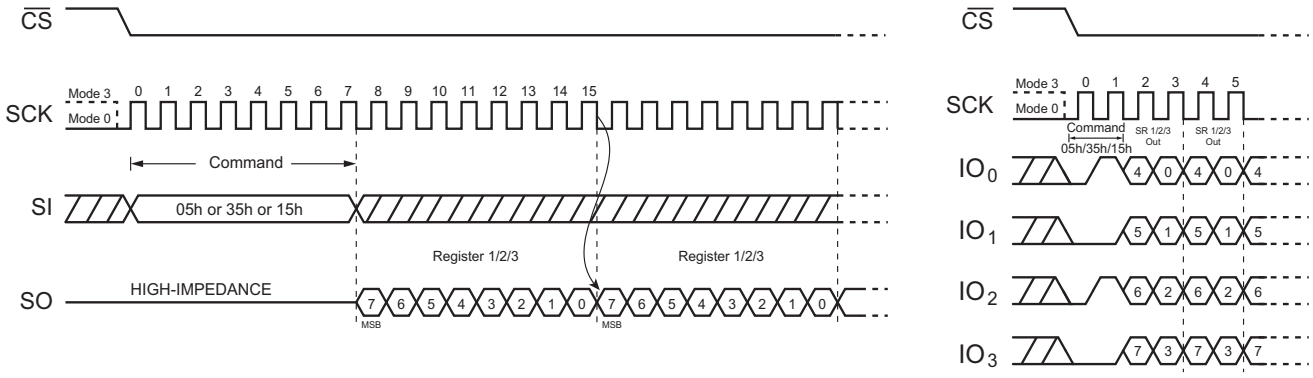


Figure 10. Read Status Register Sequence Diagram (SPI left, QPI right)

7.1.5 Write Status Register (01h or 31h or 11h)

The Write Status Register command allows the Status Registers to be written. Status Register 1 can be written by the Write Status Register 01h command. Status Register 2 can be written by the Write Status Register 01h or 31h command. Status Register 3 can be written by the Write Status Register 11h command. When the Write Status Register command 01h is followed by one byte data, it is written to Status Register 1. When the Write Status Register command 01h is followed by two bytes of data, the first byte data is written to Status Register 1; the second byte data is written to Status Register 2. The Write Status Register command 31h or 11h can only follow one byte data, which is written to Status Register 2 or Status Register 3, respectively. The writable Status Register bits include: SRP0, BP[4:0] in Status Register 1; CMP, LB[3:1], QE, SRP1 in Status Register 2; ADS, ADP, DRV1, DRV0, Hold/RES in Status Register 3. All other Status Register bit locations are read-only and are not affected by the Write Status Register command. LB[3:1] are non-volatile OTP bits; once one of them is set to 1, it cannot be cleared to 0.

The Write Status Register command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable or Write Enable For Volatile SR command must have been executed. After the Write Enable command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register command has no effect on SR2 bit 7 (SUS1), SR2 bit 2 (SUS2), SR1 bit 1 (WEL), and SR1 bit 0 (RDY/BSY) of the Status Register. $\overline{CS}$ must be driven high after the 8 or 16 bits data have been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register can be read to check the value of the RDY/BSY bit. The RDY/BSY bit is 1 during the self-timed Write Status Register cycle; it is 0 when completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 11 and Table 12. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect ($\overline{WP}$) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect ($\overline{WP}$) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register command is not executed once the Hardware Protected Mode is entered.

The sequence of issuing WRSR command is: $\overline{CS}$ goes low → sending WRSR command code → Status Register data on SI → $\overline{CS}$ goes high.

The $\overline{CS}$ must go high exactly at the 8-bit or 16-bit data boundary; otherwise, the command is rejected and not executed. The self-timed Write Status Register cycle time (t_W) is initiated as soon as $\overline{CS}$ goes high. The RDY/BSY bit can be checked during the Write Status Register cycle is in progress. RDY/BSY is set 1 during the t_W timing; it is set 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

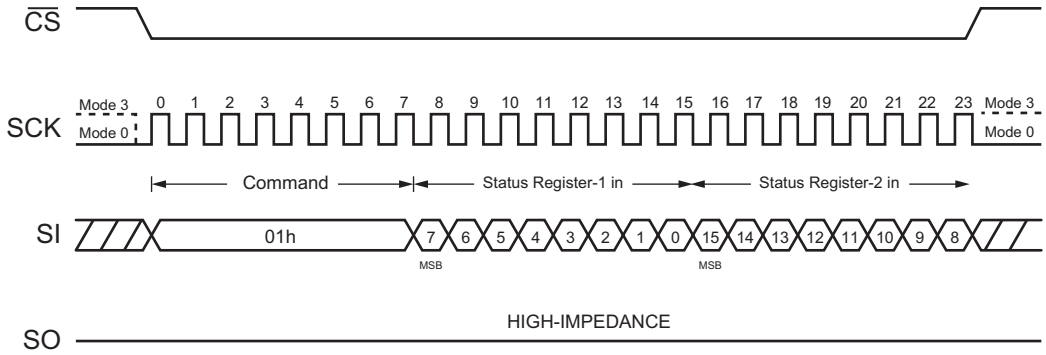


Figure 11. Write Status Register Sequence Diagram 01h Two-Byte (SPI Mode)

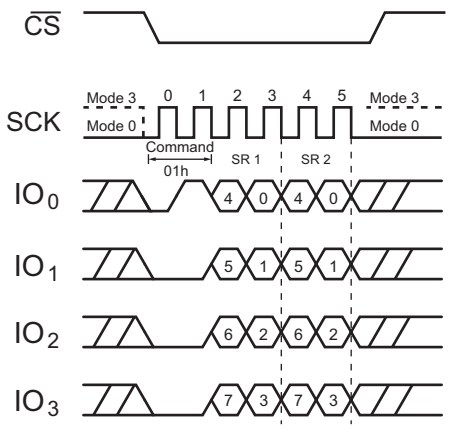


Figure 12. Write Status Register Sequence Diagram 01h Two-Byte (QPI Mode)

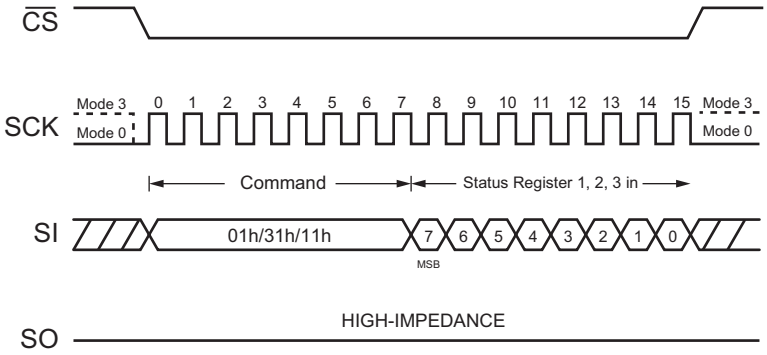


Figure 13. Write Status Register Sequence Diagram 01h, 31h, 11h One-Byte (SPI Mode)

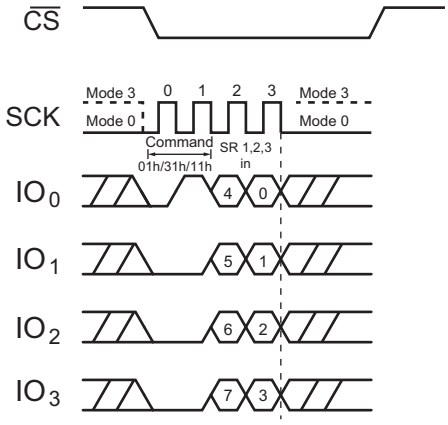


Figure 14. Write Status Register Sequence Diagram 01h, 31h, 11h One-Byte (QPI Mode)

7.1.6 Read Extended Address Register (C8h)

When the device is in the three-byte Address Mode, the Extended Address Register is used as the fourth address byte A[31:24] to access memory regions beyond 128 Mb. The Read Extended Address Register command is entered by driving $\overline{CS}$ low and shifting the opcode C8h into the SI pin on the rising edge of SCK. The Extended Address Register bits are then shifted out on the DO pin at the falling edge of SCK, with the most significant bit (MSB) first.

When the device is in four-byte Address Mode, the Extended Address Register is not used.

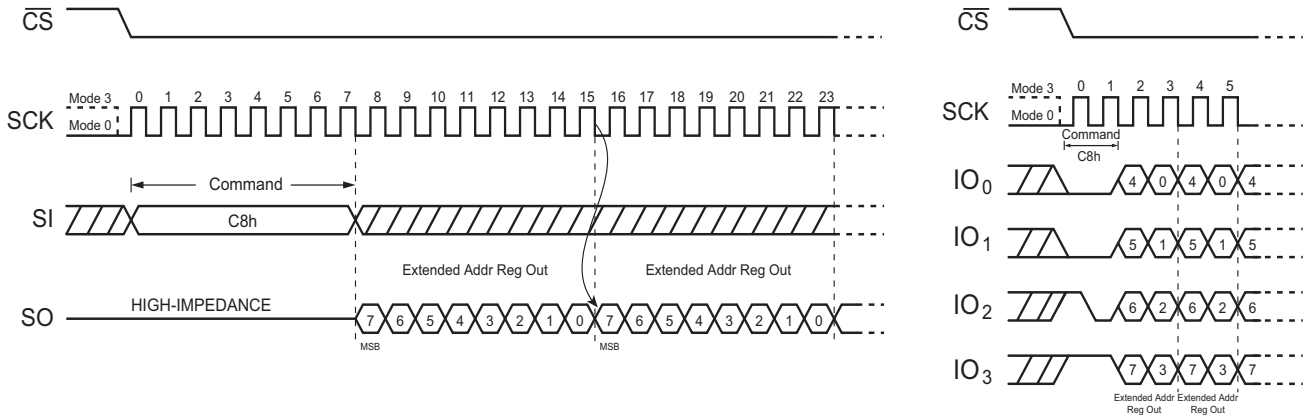


Figure 15. Read Extended Address Register (SPI left, QPI right)

7.1.7 Write Extended Address Register (C5h)

The Extended Address Register is a volatile register that stores the fourth byte address (A31-A24) when the device is operating in the three-byte Address Mode (ADS=0). To write the Extended Address Register bits, a Write Enable (06h) command must previously have been executed for the device to accept the Write Extended Address Register command (Status Register bit WEL must equal 1). Once write enabled, the command is entered by driving $\overline{CS}$ low, sending the opcode C5h, then writing the Extended Address Register data byte as shown in Figure 16.

On power-up or the execution of a software reset, the Extended Address Register bit values are cleared to 0.

The Extended Address Register is only effective when the device is in the three-byte Address Mode. When the device operates in the four-byte Address Mode (ADS=1), any command with address input of A31-A24 replaces the Extended Address Register values. If necessary, check and update the Extended Address Register when the device is switched from four-byte to three-byte Address Mode.

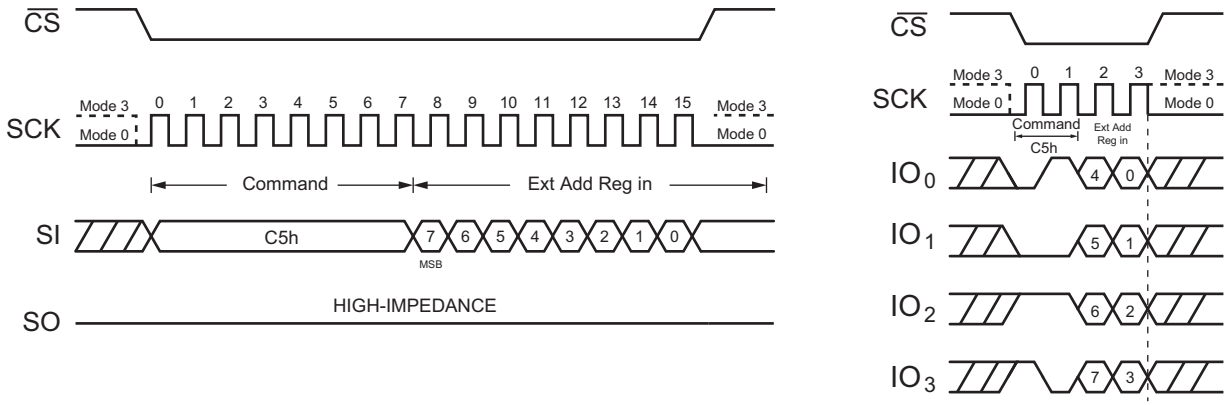


Figure 16. Write Extended Address Register (SPI left, QPI right)

7.1.8 Enter Four-Byte Address Mode (B7h)

This command allows a 32-bit address (A31-A0) to be used to access the memory array beyond 128 Mb. The command is entered by driving $\overline{CS}$ low, shifting the command code B7h into the SI pin, then driving $\overline{CS}$ high.

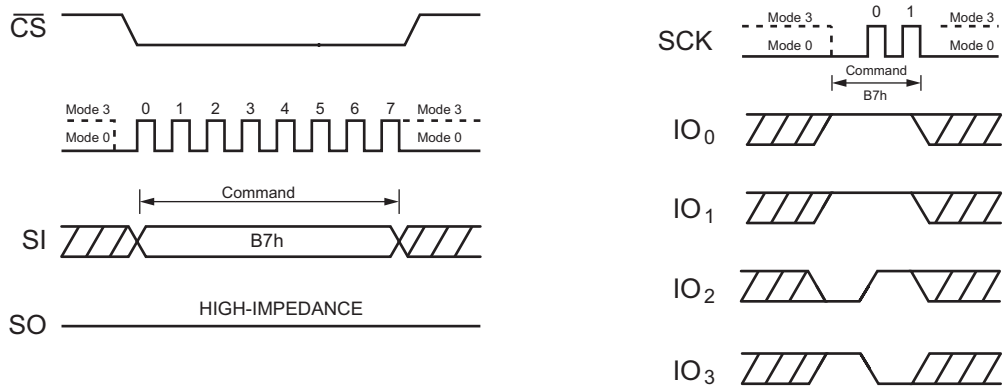


Figure 17. Enter Four-Byte Address Mode Command (SPI left, QPI right)

7.1.9 Exit Four-Byte Address Mode (E9h)

To be backward compatible, the Exit Four-Byte Address Mode command only allows a 24-bit address (A23-A0) to be used to access the memory array up to 128 Mb. The Extended Address Register must be used to access the memory array beyond 128 Mb. The Exit Four-Byte Address Mode command is entered by driving $\overline{CS}$ low, shifting the command code E9h into the SI pin, then driving $\overline{CS}$ high.

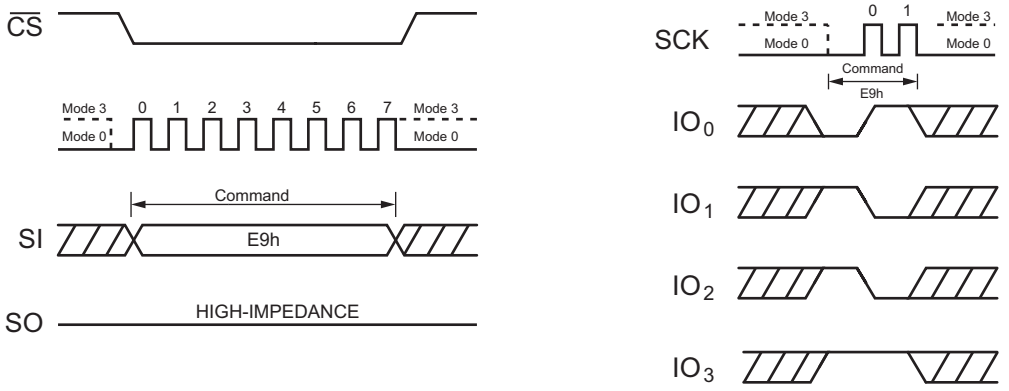


Figure 18. Exit Four-Byte Address Mode (SPI left, QPI right)

7.1.10 Enter QPI Mode (38h)

The AT25SF2561C / AT25QF2561C supports both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). SPI mode and QPI mode cannot be used at the same time. The Enter QPI (38h) command is the only way to switch the device from SPI mode to QPI mode.

On power-up, the default state of the device is Standard/Dual/Quad SPI mode for the AT25SF2561C; it is Quad I/O for the AT25QF2561C. To switch the AT25SF2561C device to QPI mode, first set the Quad Enable (QE) bit in Status Register 2 to 1; then, issue an Enter QPI (38h) command. If the Quad Enable (QE) bit is 0, the Enter QPI (38h) command is ignored, and the device stays in SPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting remain unchanged.

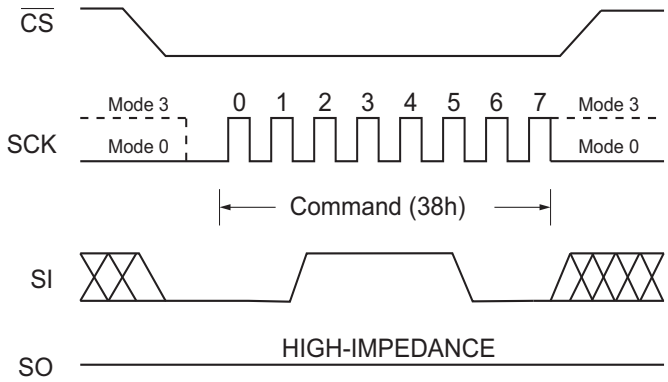


Figure 19. Enter QPI Mode (from SPI Mode)

7.1.11 Exit QPI Mode (FFh)

To exit the QPI mode and return to the Standard/Dual/Quad SPI mode, issue the Exit QPI (FFh) command.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL), the Program/Erase Suspend status, and the Wrap Length setting remain unchanged.

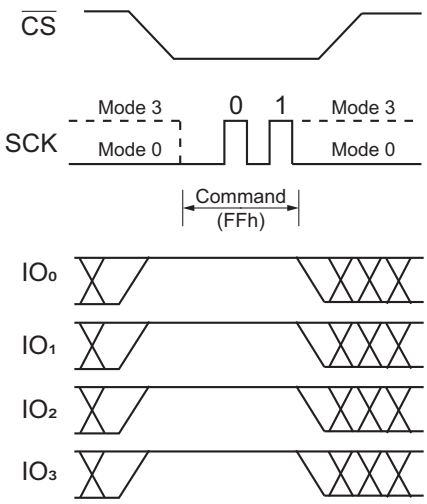


Figure 20. Exit QPI Mode

7.1.12 Enable Reset (66h) and Reset Device (99h)

The AT25SF2561C / AT25QF2561C provides a software Reset command instead of a dedicated $\overline{\text{RESET}}$ pin. Once the software Reset command is accepted, any on-going internal operations are terminated and the device returns to its default power-on state and loses all of the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting (M7-M0) and Wrap Bit setting (W6-W4).

To avoid accidental reset, issue both Enable Reset (66h) and Reset (99h) commands in sequence. Any other commands other than Reset (99h) after the Enable Reset (66h) command disables the Reset Enable state. A new sequence of Enable Reset (66h) and Reset (99h) is needed to reset the device. Once the Reset command is accepted by the device, the device takes a period of approximately t_{RST} to reset. During this period, no commands are accepted.

The Enable Reset (66h) and Reset (99h) command sequence is shown in Figure 21.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when the Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

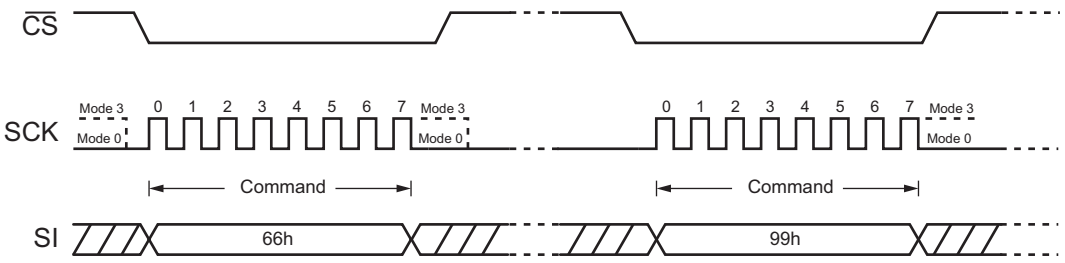


Figure 21. Enable Reset (66h) and Reset (99h) Command Sequence (SPI)

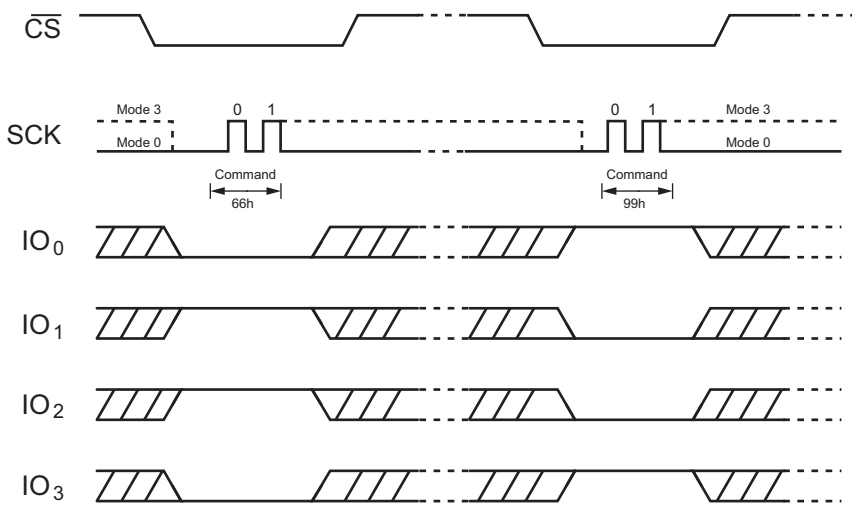


Figure 22. Enable Reset (66h) and Reset (99h) Command Sequence (QPI)

7.2 Read Commands

7.2.1 Read Data (03h)

The Read Data command is followed by a three-byte/four-byte address (A23/A31 - A0), each bit being latched-in during the rising edge of SCK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_R, during the falling edge of SCK. The address automatically increments to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues. The command is completed by driving $\overline{CS}$ high. The whole memory can be read with a single Read Data Bytes command. Any *Read Data* command attempting to execute while an *Erase*, *Program* or *Write* cycle is in progress, is rejected without having any effects on the cycle that is in progress.

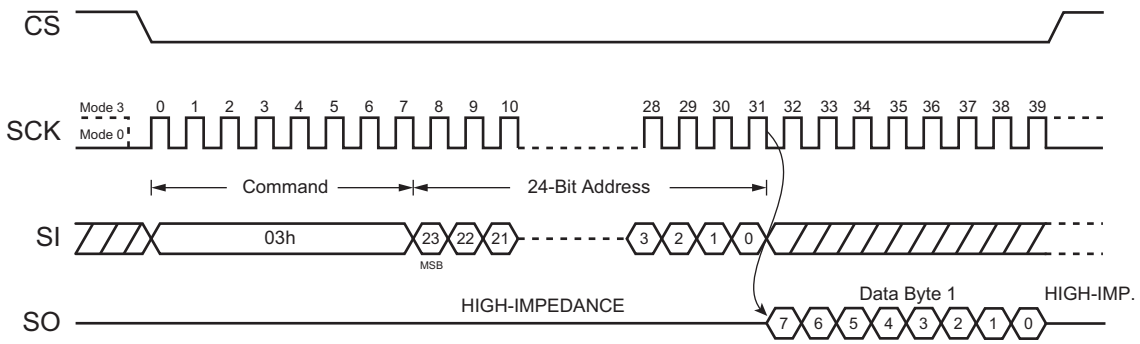


Figure 23. Read Data Bytes Sequence Diagram (SPI Mode, Three-Byte Address Mode)

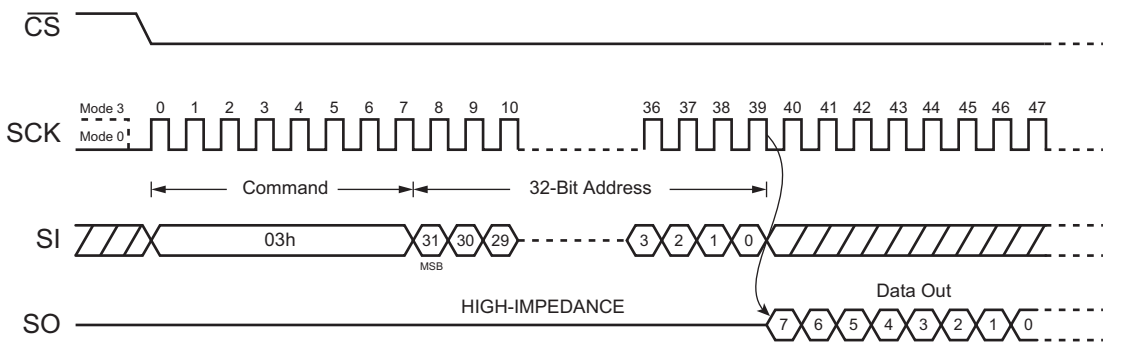


Figure 24. Read Data Bytes Sequence Diagram (SPI Mode, Four-Byte Address Mode)

7.2.2 Read Data with Four-Byte Address (13h)

The Read Data with Four-Byte Address command is similar to the Read Data (03h) command. Instead of a 24- bit address, a 32-bit address is needed following the command code 13h. It does not matter if the device is operating in three-byte Address Mode or four-byte Address Mode, the Read Data with 4-Byte Address command always requires a 32-bit address to access the entire 256 Mb memory.

The Read Data with 4-Byte Address command sequence is shown in Figure 25. If this command is issued while an Erase, Program, or Write cycle is in process (RDY/BSY=1), the command is ignored and does not have any effects on the current cycle. The Read Data with 4-Byte Address command allows clock rates from D.C. to a maximum of f_R (see Section 8.7).

This command is supported only in Standard SPI mode.

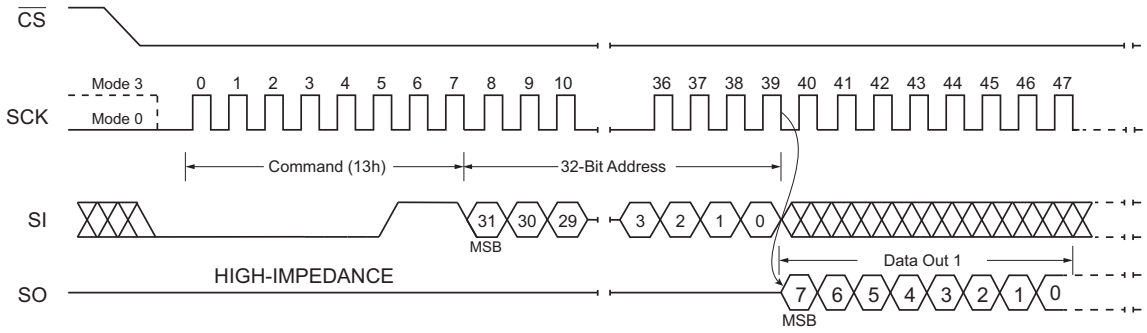


Figure 25. Read Data with Four-Byte Address Sequence Diagram (SPI Mode)

7.2.3 Fast Read (0Bh)

7.2.3.1 Fast Read (0Bh) in SPI Mode

The Read Data at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a three-byte/four-byte address (A23/A31 - A0) and a dummy byte, each bit being latched-in during the rising edge of SCK. Then, the memory content at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_C during the falling edge of SCK. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out.

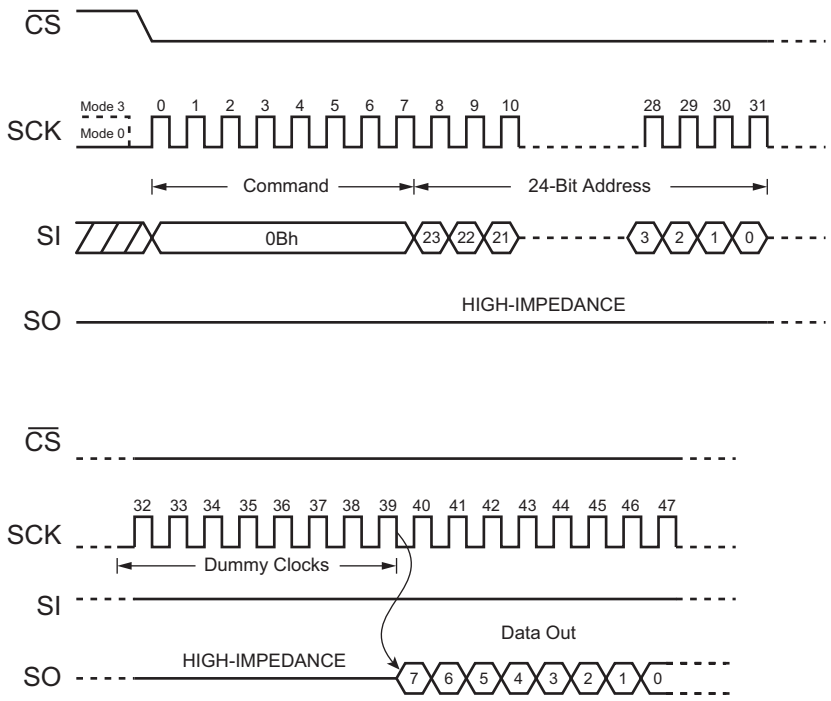


Figure 26. Fast Read Sequence Diagram (SPI Mode, Three-Byte Address Mode)

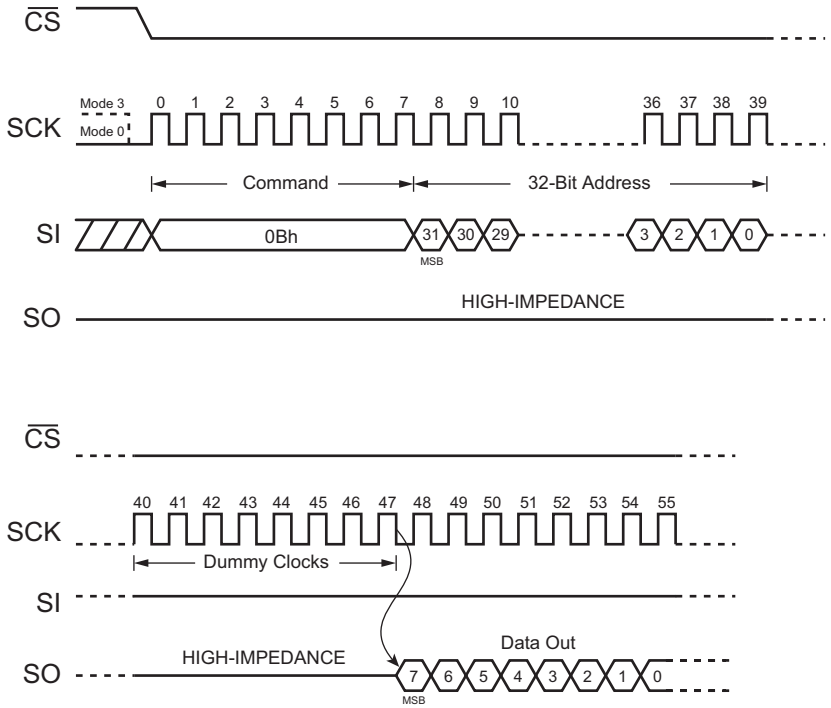


Figure 27. Fast Read Sequence Diagram (SPI Mode, Four-Byte Address Mode)

7.2.3.2 Fast Read (0Bh) in QPI Mode

The Fast Read command is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the Set Read Parameters (C0h) command to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[6:4] setting, the number of dummy clocks can be configured from 4 to 18. The default number of dummy clocks on power-up or after a Reset command is 4.

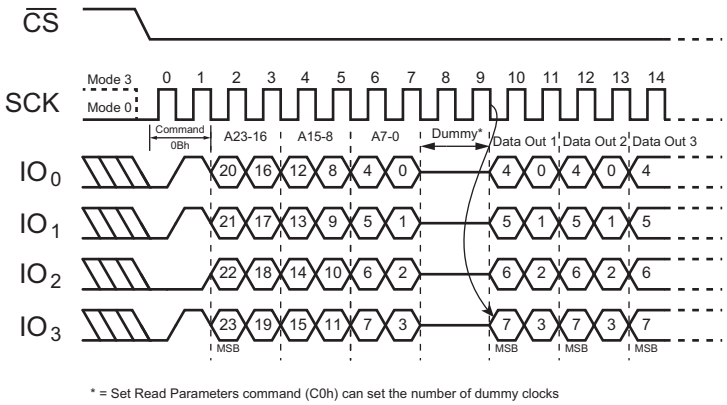


Figure 28. Fast Read Sequence Diagram (QPI Mode, Three-Byte Address Mode)

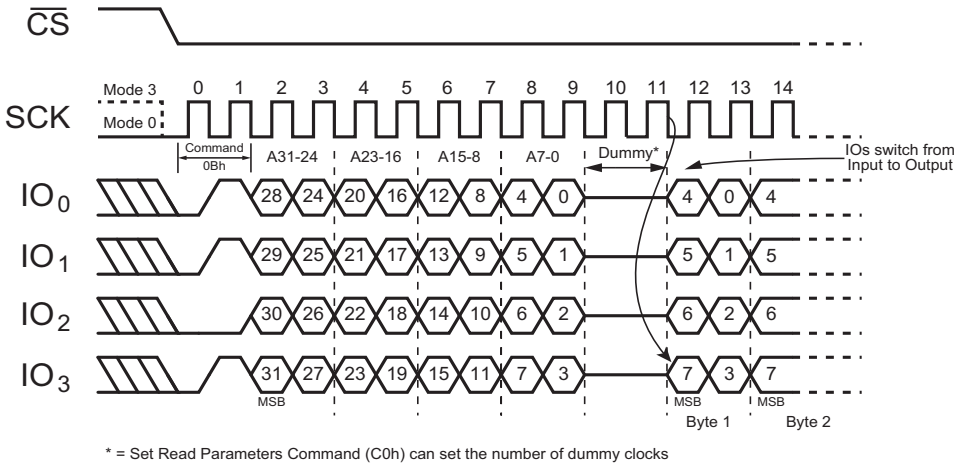


Figure 29. Fast Read Sequence Diagram (QPI Mode, Four-Byte Address Mode)

7.2.4 Fast Read with Four-Byte Address (0Ch)

The Fast Read with 4-Byte Address (0Ch) command is similar to the Fast Read command, except that it requires a 32-bit address instead of a 24-bit address. No matter what address mode the device is operating in, the Read Data with 4-Byte Address command always requires a 32-bit address to access the entire 256 Mb memory.

This command is supported only in Standard SPI mode. In QPI mode, the command code 0Ch is used for the Burst Read with Wrap command.

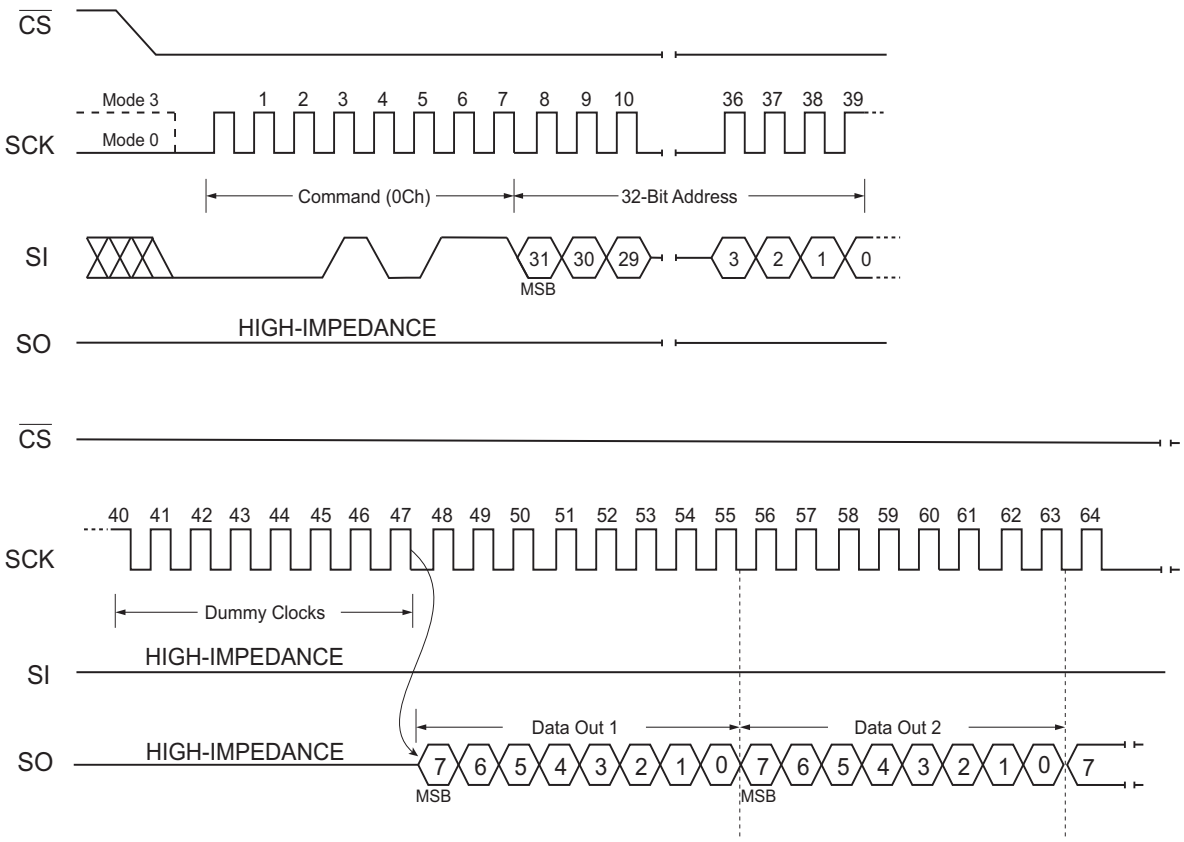


Figure 30. Fast Read with Four-Byte Address

7.2.5 Dual Output Fast Read (3Bh)

The Dual Output Fast Read command is followed by three-byte or four-byte address (A23/A31 - A0) and a dummy byte, each bit being latched on the rising edge of SCK; then, the memory contents are shifted out two bits per clock cycle from SI and SO. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out.

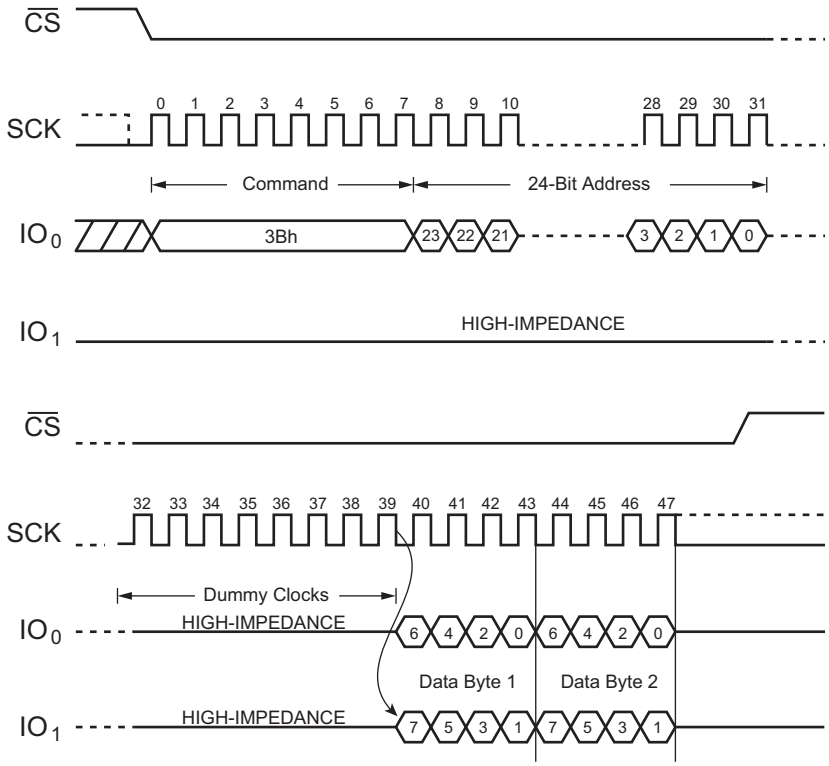


Figure 31. Dual Output Fast Read Sequence Diagram (SPI Mode, Three-Byte Address Mode)

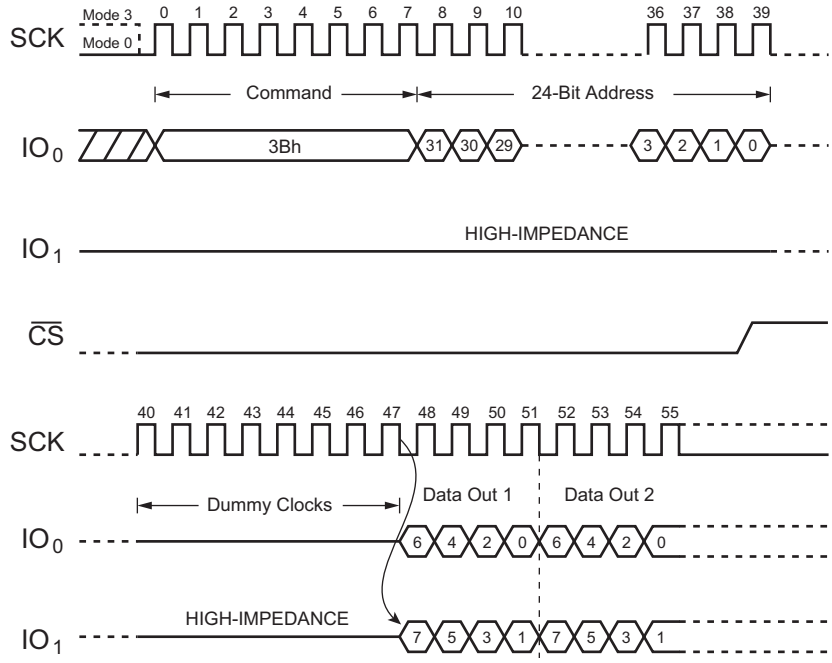


Figure 32. Dual Output Fast Read Sequence Diagram (SPI Mode, Four-Byte Address Mode)

7.2.6 Fast Read Dual Output with Four-Byte Address (3Ch)

The Fast Read Dual Output with Four-Byte Address command is similar to the Fast Read Dual Output command, except that it requires a 32-bit address instead of a 24-bit address. No matter what the address mode the device is operating in, this command always requires a 32-bit address to access the entire 256 Mb memory.

This command is only supported in Standard SPI mode.

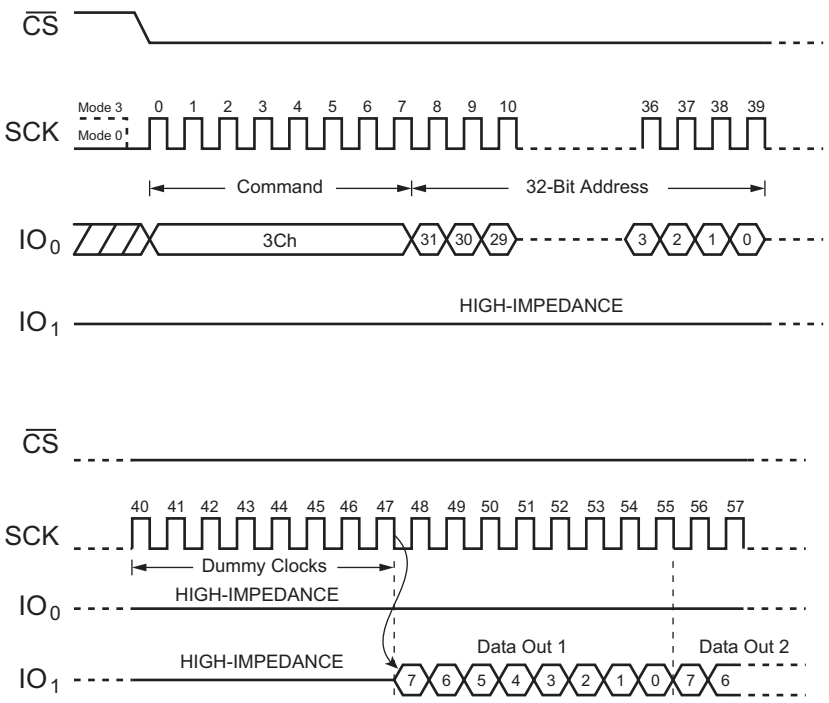


Figure 33. Fast Read Dual Output with Four-Byte Address

7.2.7 Quad Output Fast Read (6Bh)

The Quad Output Fast Read command is followed by a three-byte or four-byte address (A23/A31 - A0) and a dummy byte, each bit being latched on the rising edge of SCK; then, the memory contents are shifted out four-bit per clock cycle from IO_3, IO_2, IO_1, and IO_0. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) must be set to enable.

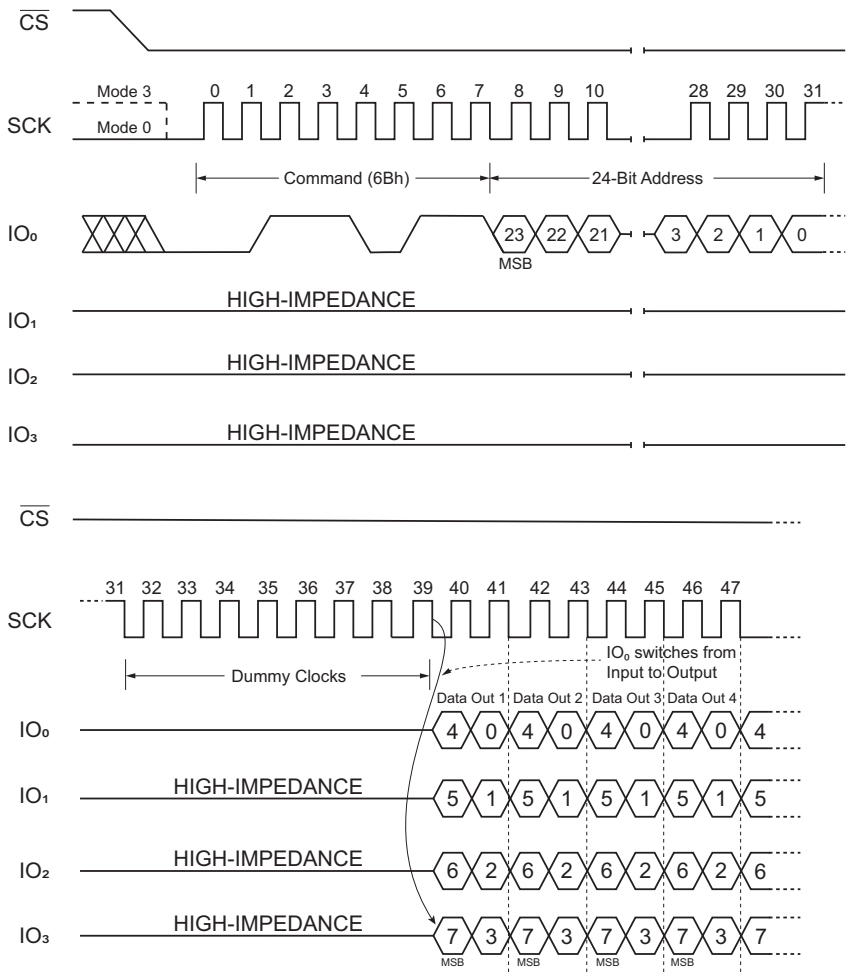


Figure 34. Quad Output Fast Read Sequence Diagram (SPI Mode, Three-Byte Address)

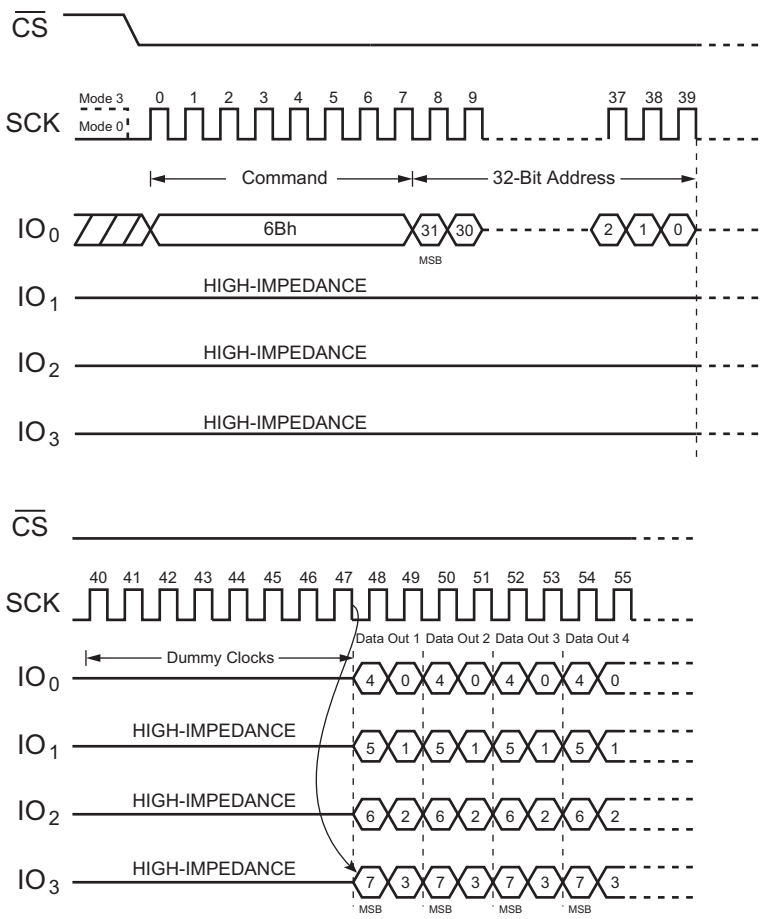


Figure 35. Quad Output Fast Read Sequence Diagram (SPI Mode, Four-Byte Address)

7.2.8 Fast Read Quad Output with Four-Byte Address (6Ch)

The Fast Read Quad Output with Four-Byte Address command is similar to the Fast Read Quad Output command, except that it requires a 32-bit address instead of a 24-bit address. No matter what address mode the device is operating in, this command always requires a 32-bit address to access the entire 256 Mb memory.

This command is supported only in Standard SPI mode.

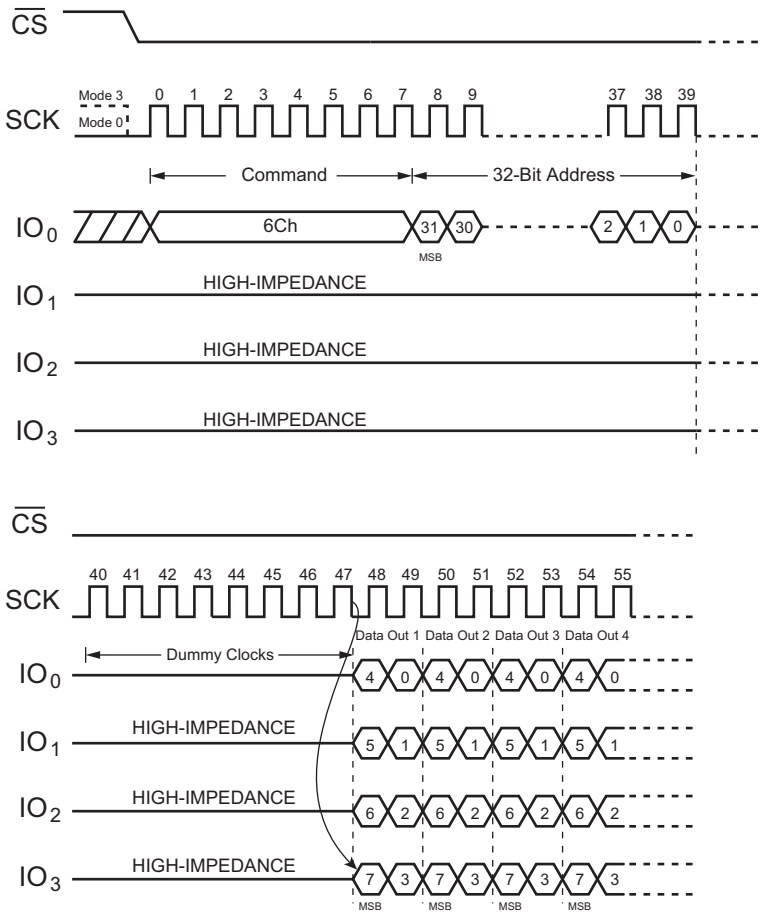


Figure 36. Fast Read Quad Output with Four-Byte Address

7.2.9 Dual I/O Fast Read (BBh)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input a three-byte or four-byte address (A23/A31 - 0) and a Continuous Read Mode byte two bits per clock by SI and SO, each bit being latched on the rising edge of SCK; then, the memory contents are shifted out two bits per clock cycle on the SI and SO pins. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out.

7.2.9.1 Dual I/O Fast Read with Continuous Read Mode

The Dual I/O Fast Read command can further reduce command overhead through setting the Continuous Read Mode bits (M7 - 4) after the inputs three-byte address A23 - A0).

If the Continuous Read Mode bits (M5:M4) do not equal (1,0), the next command requires the first BBh command code, thus returning to normal operation. A Continuous Read Mode Reset command can be used to reset (M5:M4) before issuing normal command. The command sequence is shown in the following Figure 38.

If the Continuous Read Mode bits (M5:M4) = (1, 0), then the next Dual I/O fast Read command (after $\overline{CS}$ is raised and then lowered) does not require the BBh command code. The command sequence is shown in the following Figure 40.

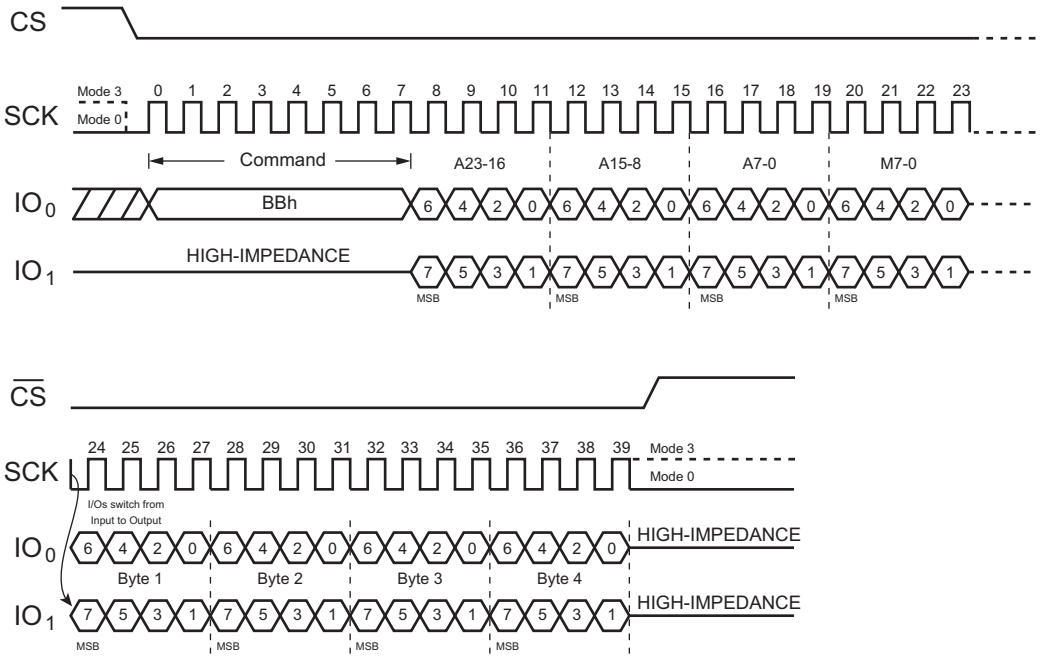


Figure 37. Dual I/O Fast Read Sequence Diagram (SPI Mode, Three-Byte Address Mode; Initial command or previous (M5:4) ≠ (1,0))

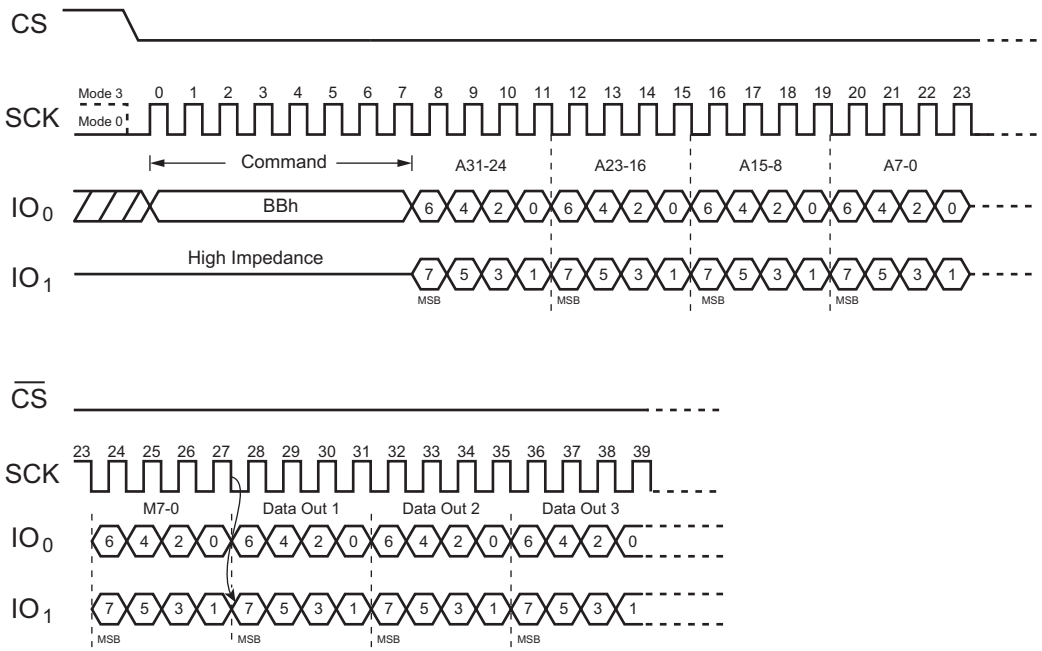


Figure 38. Dual I/O Fast Read Sequence Diagram (SPI Mode, Four-Byte Address Mode; Initial command or previous (M5:4) ≠ (1,0))

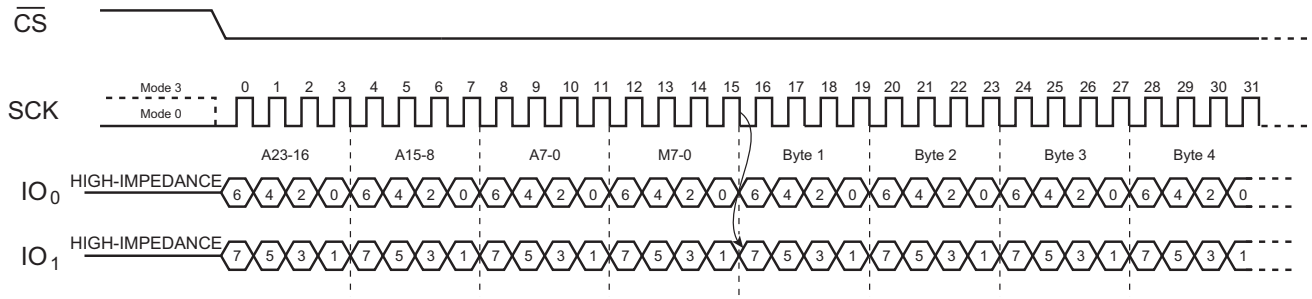


Figure 39. Dual I/O Fast Read Sequence Diagram (SPI Mode, Three-Byte Address Mode; Initial command or previous (M5:4) = (1,0))

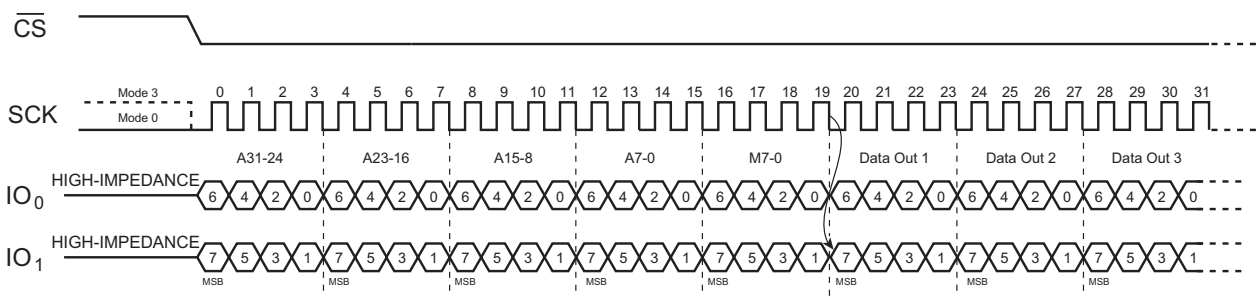


Figure 40. Dual I/O Fast Read Sequence Diagram (SPI Mode, Four-Byte Address Mode; Previous command set (M5:4) = (1,0))

7.2.10 Fast Read Dual I/O with 4-Byte Address (BCh)

The Fast Read Dual I/O with a Four-Byte Address command is similar to the Fast Read Dual I/O command, except that it requires a 32-bit address instead of a 24-bit address. No matter what address mode the device is operating in, this command always requires a 32-bit address to access the entire 256 Mb memory.

This command is supported only in Standard SPI mode.

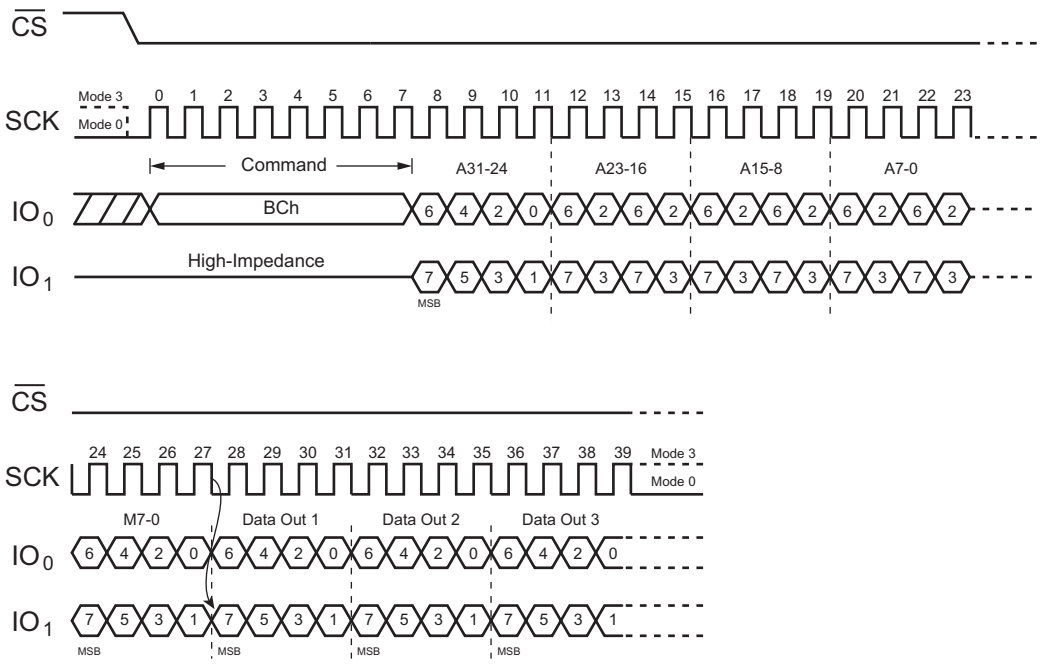


Figure 41. Fast Read Dual I/O with 4-Byte Address (SPI Mode only; Initial command or previous M5-4 ≠ 1,0)

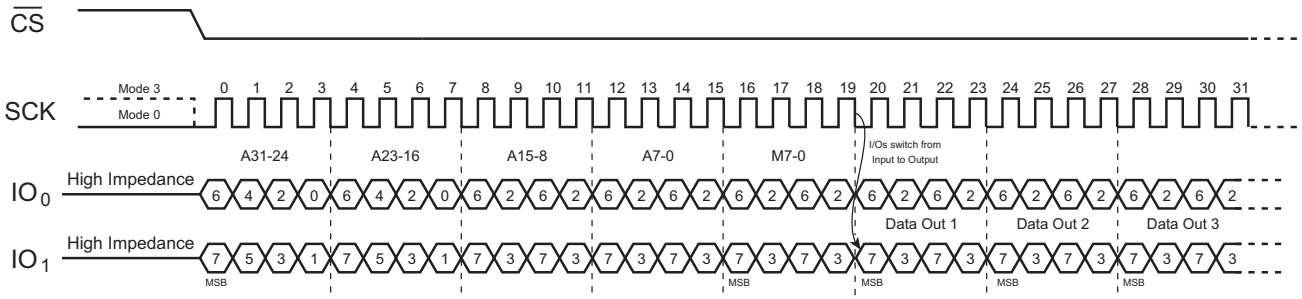


Figure 42. Fast Read Dual I/O with Four-Byte Address (SPI Mode only; Initial command or previous M5-4 = 1,0)

7.2.11 Quad I/O Fast Read (EBh)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the three-byte or four-byte address (A23/A31-0) and a Continuous Read Mode byte and four dummy clocks, each bit being latched on the rising edge of SCK; then, the memory contents are shifted out four bits per clock cycle from IO_0, IO_1, IO_2, IO_3. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register must be set to enable for the Quad I/O Fast read command.

7.2.11.1 Quad I/O Fast Read with Continuous Read Mode

The Quad I/O Fast Read command can further reduce command overhead through setting the Continuous Read Mode bits (M7-0) after the input Address bits (A23-0).

If the Continuous Read Mode bits M5-4 do not equal to (1,0), the next command requires the first EBh command code, thus returning to normal operation. A Continuous Read Mode Reset command can also be used to reset (M5-4) before issuing normal command. The command sequence is shown in the followed Figure 43.

If the Continuous Read Mode bits (M5-4) = (1,0), then the next Fast Read Quad I/O command (after $\overline{CS}$ is raised and then lowered) does not require the EBh command code. The command sequence is shown in the following Figure 45.

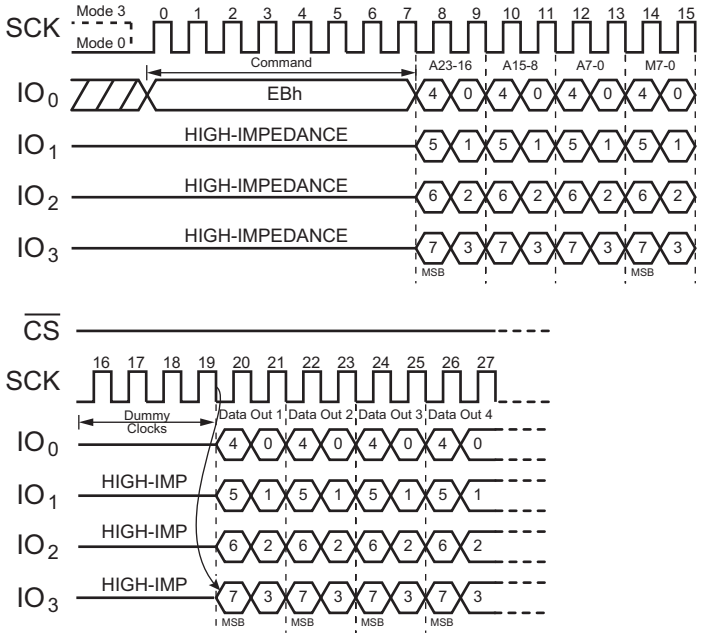


Figure 43. Quad I/O Fast Read Sequence Diagram (SPI Mode, Three-Byte Address Mode; Initial command or previous (M5-4) ≠ (1,0))

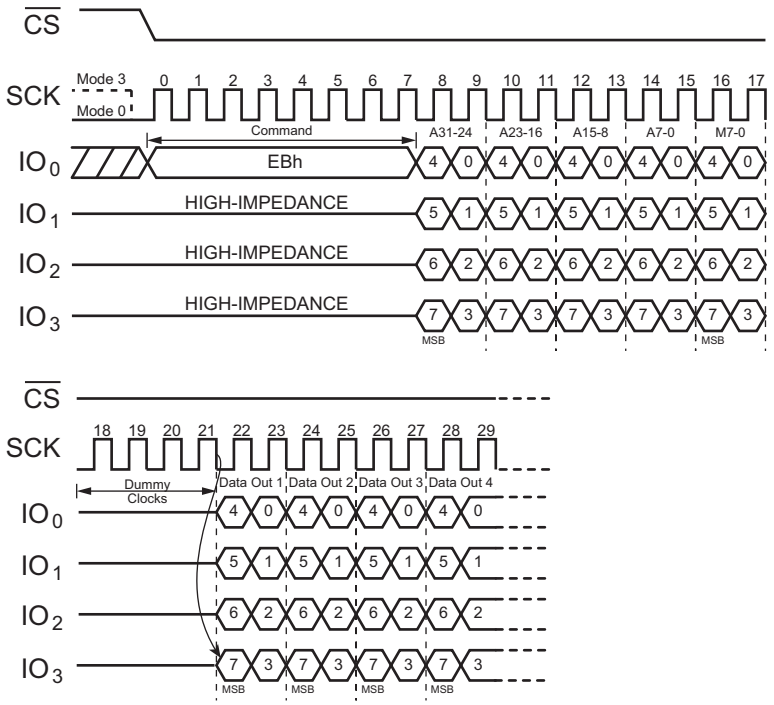


Figure 44. Quad I/O Fast Read Sequence Diagram (SPI Mode, Four-Byte Address Mode; Initial command or previous (M5-4) ≠ (1,0))

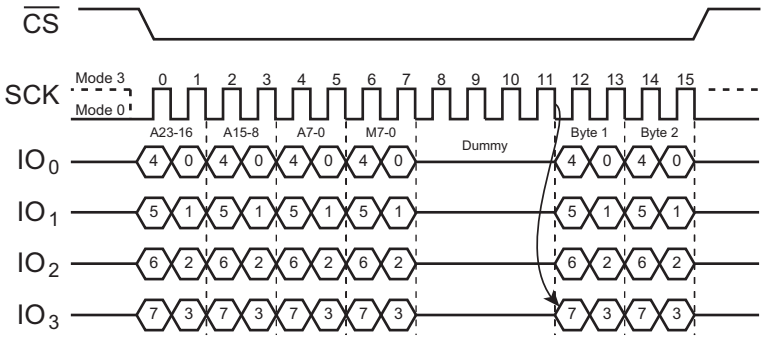


Figure 45. Quad I/O Fast Read Sequence Diagram (SPI Mode, Three-Byte Address Mode; Previous command set (M5-4) = (1,0))

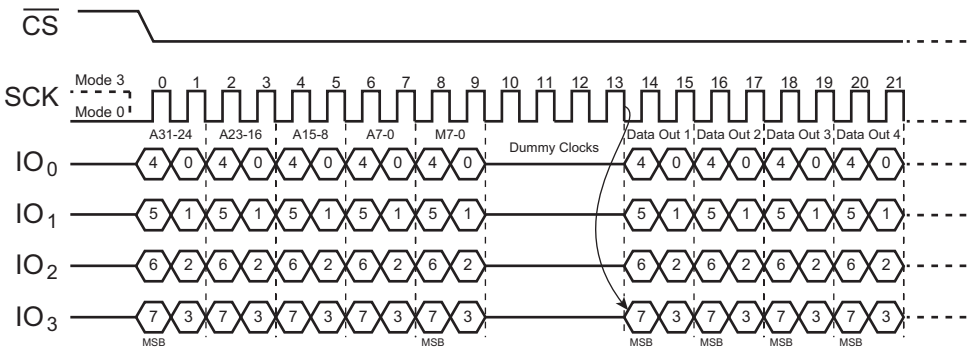


Figure 46. Quad I/O Fast Read Sequence Diagram (SPI Mode, Four-Byte Address Mode; Initial command or previous (M5-4) = (1,0))

7.2.11.2 Quad I/O Fast Read with 8/16/32/64-Byte Wrap Around

The Quad I/O Fast Read command can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) command prior to EBh. This command can either enable or disable the Wrap Around feature for the following EBh commands.

When Wrap Around is enabled, the data being accessed can be limited to either an 8, 16, 32, or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The Set Burst with Wrap command allows three Wrap Bits, W6-4, to be set. The W4 bit is used to enable or disable the Wrap Around operation while W6-5 are used to specify the length of the wrap around section within a page.

7.2.11.3 Fast Read Quad I/O (EBh) in QPI Mode

The Fast Read Quad I/O command is also supported in QPI mode, as shown in Figure 47 to Figure 50. When QPI mode is enabled, the number of dummy clocks is configured by the Set Read Parameters (C0h) command to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[6:4] setting, the number of dummy clocks can be configured from 4 to 18. The default number of dummy clocks on power-up or after a Reset command is 4. In QPI mode, the Continuous Read Mode bits M7-0 are also considered as dummy clocks. In the default setting, the data output follow the Continuous Read Mode bits immediately.

The Continuous Read Mode feature is also available in QPI mode for Fast Read Quad I/O command. See the description on previous pages.

The Wrap Around feature is not available in QPI mode for Fast Read Quad I/O command. To perform a read operation with fixed data length wrap around in QPI mode, use a dedicated Burst Read with Wrap (0Ch) command.

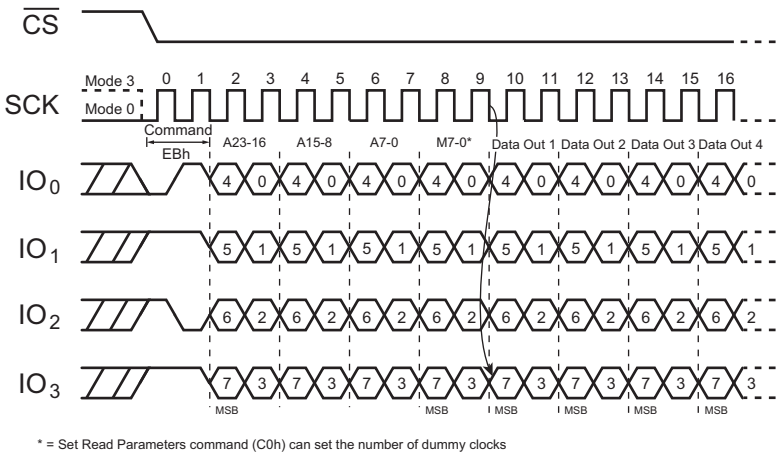


Figure 47. Quad I/O Fast Read Sequence Diagram (QPI Mode, Three-Byte Address Mode; Initial command or previous (M5-4≠(1,0))

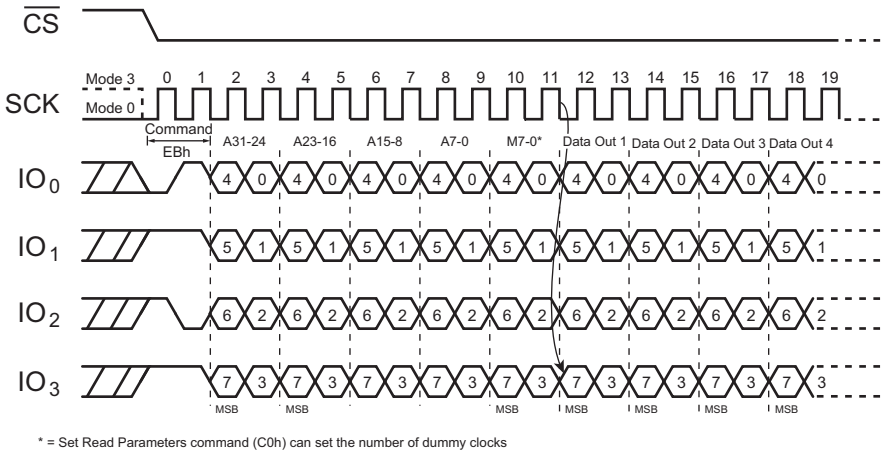


Figure 48. Quad I/O Fast Read Sequence Diagram (QPI Mode, Four-Byte Address Mode; Initial command or previous (M5-4≠(1,0))

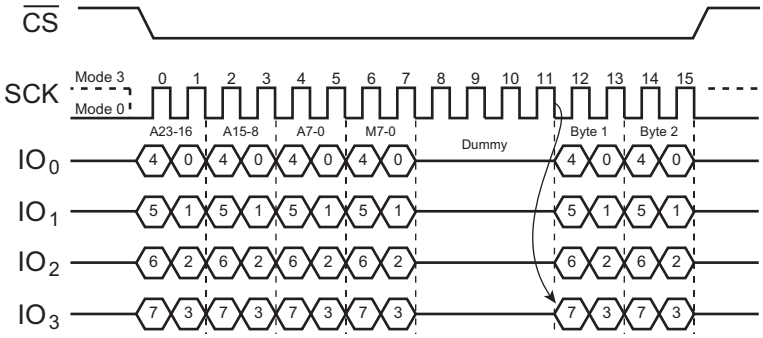


Figure 49. Quad I/O Fast Read Sequence Diagram (QPI Mode, Three-Byte Address Mode; Initial command or previous (M5-4=(1,0))

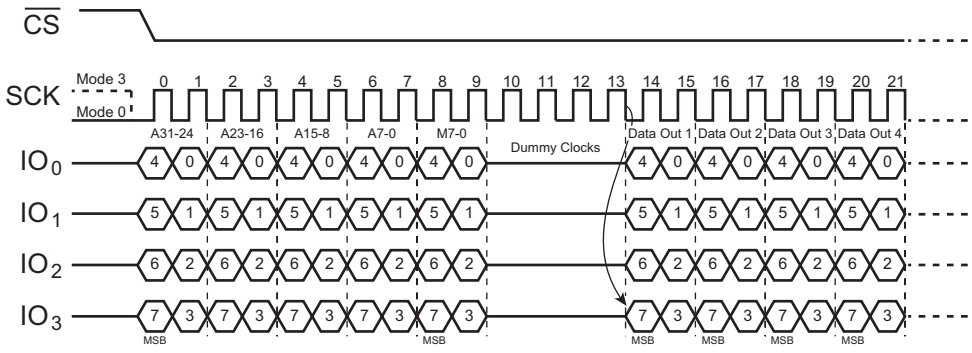


Figure 50. Quad I/O Fast Read Sequence Diagram (QPI Mode, Four-Byte Address Mode; Initial command or previous (M5-4=(1,0))

7.2.12 DTR Fast Read Quad I/O (EDh)

The DTR Fast Read Quad I/O (EDh) command is similar to the Fast Read Dual I/O (BBh) command, except that address and data bits are input and output through four pins: IO_0, IO_1, IO_2, and IO_3; also, four Dummy clocks are required in SPI mode before the data output, as shown in Figure 51 to Figure 58. The Quad Enable bit (QE) of Status Register must be set to enable.

7.2.12.1 DTR Fast Read Quad I/O with Continuous Read Mode

The Fast Read Quad I/O command can further reduce command overhead through setting the Continuous Read Mode bits (M7-0) after the input Address bits (A23/A31-0). The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O command through the inclusion or exclusion of the first byte command code. The lower nibble bits of the (M3-0) are don't care (x); however, the IO pins must be high-impedance before the falling edge of the first data out clock.

If the Continuous Read Mode bits M5-4 = (1,0), the next Fast Read Quad I/O command (after $\overline{CS}$ is raised and then lowered) does not require the EDh opcode. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after $\overline{CS}$ is asserted low. If the Continuous Read Mode bits M5-4 do not equal to (1,0), the next command (after $\overline{CS}$ is raised and then lowered) requires the first byte command code, thus returning to normal operation.

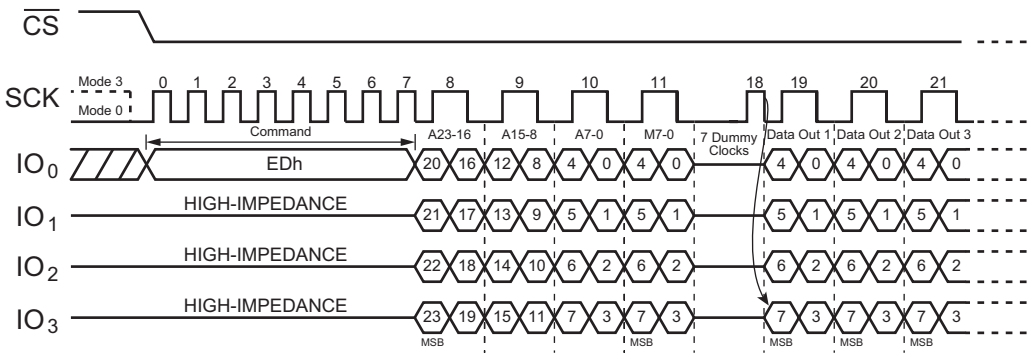


Figure 51. DTR Fast Read Quad I/O (SPI Mode, Three-Byte Address Mode; Initial command or previous (M5-4≠(1,0))

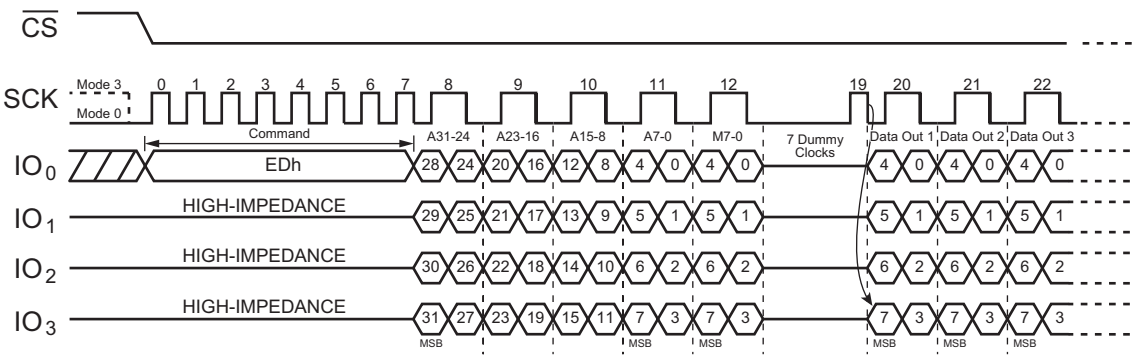


Figure 52. DTR Fast Read Quad I/O (SPI Mode, Four-Byte Address Mode; Initial command or previous (M5-4≠(1,0))

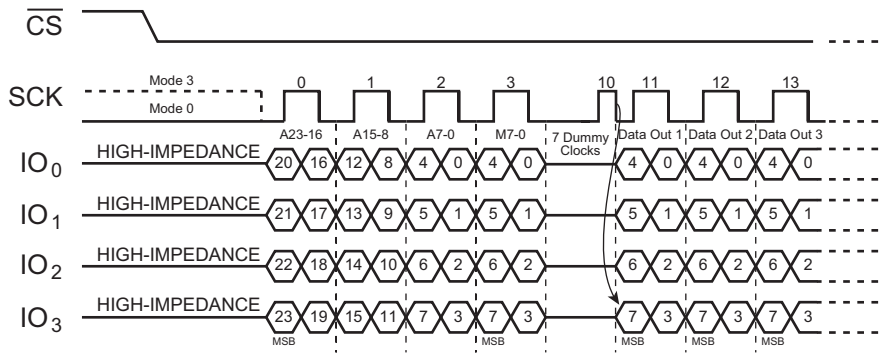


Figure 53. DTR Fast Read Quad I/O (SPI Mode, 3-Byte Address Mode; Initial command or previous (M5-4=(1,0)))

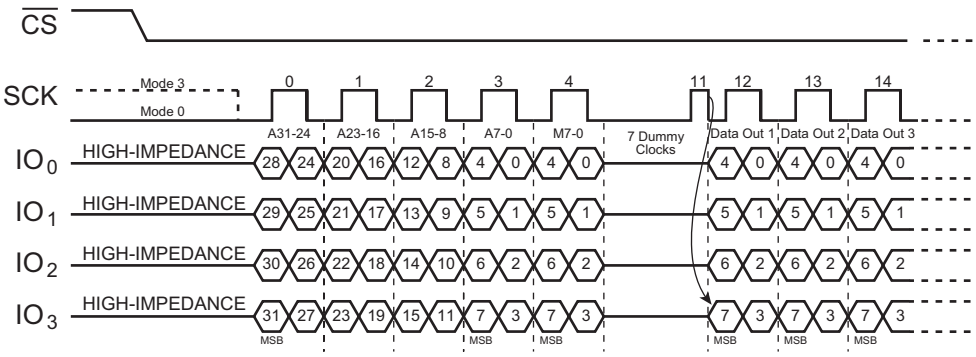


Figure 54. DTR Fast Read Quad I/O (SPI Mode, Four-Byte Address Mode; Initial command or previous (M5-4=(1,0)))

7.2.12.2 DTR Fast Read Quad I/O with 8/16/32/64-Byte Wrap Around in Standard SPI mode

The Fast Read Quad I/O command can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) command before EDh. This command can either enable or disable the Wrap Around feature for the following EDh commands. When Wrap Around is enabled, the data being accessed can be limited to either an 8, 16, 32, or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the command. Once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The Set Burst with Wrap command allows three Wrap Bits, W6-4, to be set. The W4 bit is used to enable or disable the Wrap Around operation, while W6-5 are used to specify the length of the wrap around section within a page.

7.2.12.3 DTR Fast Read Quad I/O (EDh) in QPI Mode

The DTR Fast Read Quad I/O command is also supported in QPI mode, as shown in Figure 55 to Figure 58. In QPI mode, the Continuous Read Mode can further reduce command overhead by setting the Continuous Read Mode bits (M7-0) after the input Address bits (A23/31-0).See the description on previous pages.If the Continuous Read Mode bits (M5-4)= (1,0), the next Fast Read Quad I/O command (after $\overline{CS}$ is raised and then lowered) does not require the EDh opcode. If the Continuous Read Mode bits M5-4 do not equal (1,0), the next command requires the first EDh opcode, thus returning to normal operation. A Continuous Read Mode Reset command can also be used to reset (M5-4) before issuing normal command.

When QPI mode is enabled, the number of dummy clocks is configured by the Set Read Parameters (C0h) command to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[6:4] setting, the number of

dummy clocks can be configured from 6 to 20. The default number of dummy clocks on power-up or after a Reset command is 6. Note that the number of dummy includes M7-0.

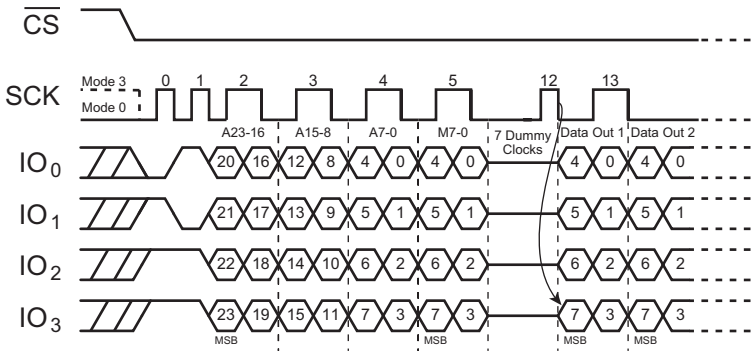


Figure 55. DTR Fast Read Quad I/O (QPI Mode, Three-Byte Address Mode; Initial command or previous (M5-4≠(1,0))

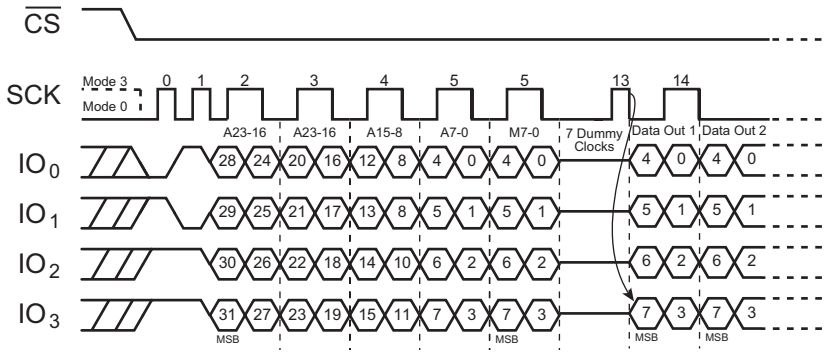


Figure 56. DTR Fast Read Quad I/O (QPI Mode, Four-Byte Address Mode; Initial command or previous (M5-4≠(1,0))

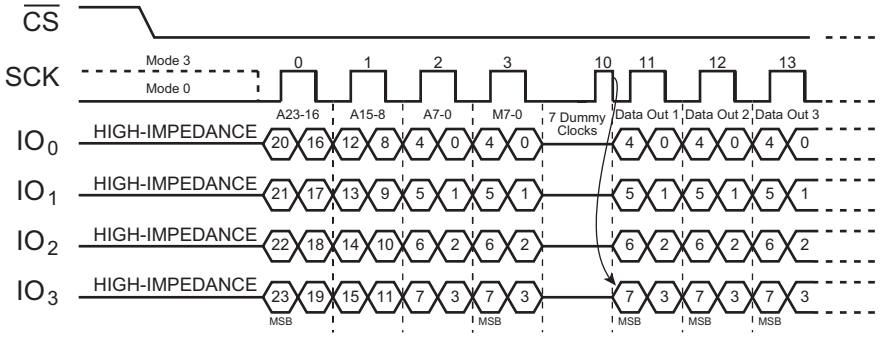


Figure 57. DTR Fast Read Quad I/O (QPI Mode, Three-Byte Address Mode; Initial command or previous (M5-4=(1,0))

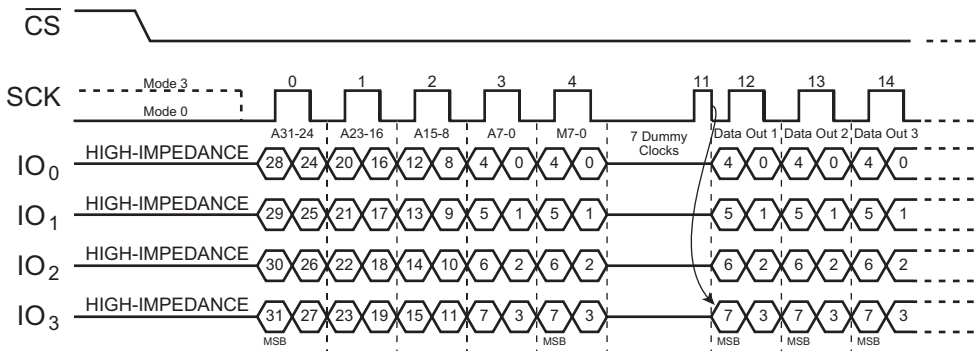


Figure 58. DTR Fast Read Quad I/O (QPI Mode, Four-Byte Address Mode; Initial command or previous (M5-4=(1,0))

7.2.13 Fast Read Quad I/O with Four-Byte Address (ECh)

The Fast Read Quad I/O with Four-Byte Address command is similar to the Quad I/O Fast Read command, except that it requires a 32-bit address instead of a 24-bit address. No matter what address mode the device is operating in, the Fast Read Quad I/O with 4-Byte Address command require a 32-bit address to access the entire 256 Mb memory. The Quad Enable bit (QE) of Status Register must be set to enable.

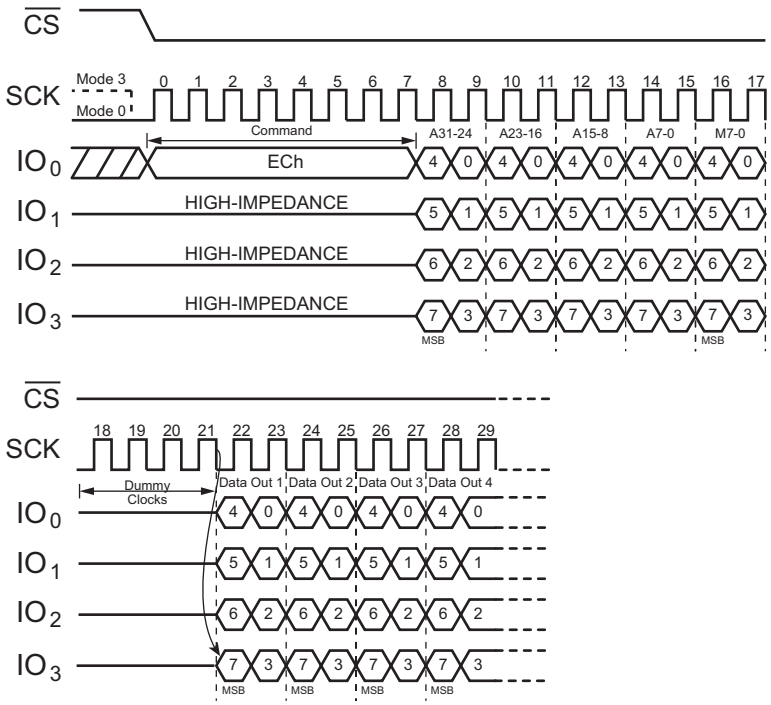


Figure 59. Fast Read Quad I/O with Four-Byte Address (SPI Mode; Initial command or previous (M5-4≠(1,0))

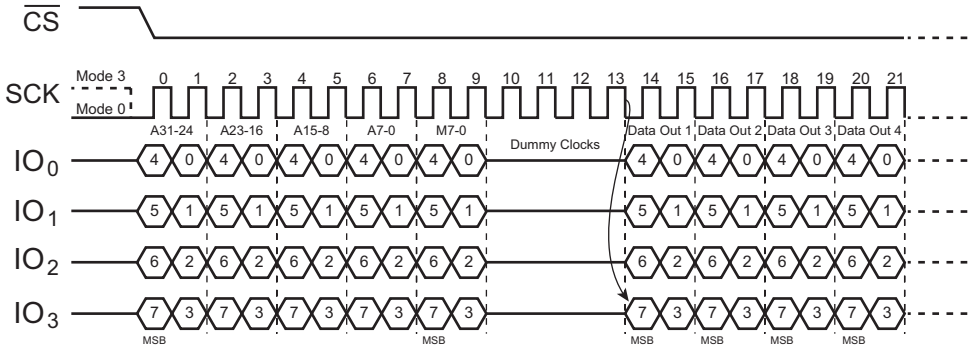


Figure 60. Fast Read Quad I/O with Four-Byte Address (SPI Mode, Initial command or previous M5-4=10)

7.2.13.1 Fast Read Quad I/O with Four-Byte Address with 8/16/32/64-Byte Wrap Around (SPI Mode)

The Fast Read Quad I/O with 4-Byte Address command can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) command before ECh. This command can either enable or disable the Wrap Around feature for the following ECh commands. When Wrap Around is enabled, the data being accessed can be limited to either an 8,16, 32, or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the command. Once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The Set Burst with Wrap command allows three Wrap Bits, W6-4 to be set. The W4 bit is used to enable or disable the Wrap Around operation, while W6-5 are used to specify the length of the wrap around section within a page.

7.2.13.2 Fast Read Quad I/O with 4-Byte Address (ECh) in QPI Mode

The Fast Read Quad I/O with Four-Byte Address command is also supported in QPI mode, as shown in Figure 61 and Figure 62. When QPI mode is enabled, the number of dummy clocks is configured by the Set Read Parameters (C0h) command to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter bits P[6:4] setting, the number of dummy clocks can be configured from 4 to 18. The default number of dummy clocks on power-up or after a Reset command is 4. In QPI mode, the Continuous Read Mode bits M7-0 are also considered as dummy clocks. In the default setting, the data output immediately follows the Continuous Read Mode bits.

The Continuous Read Mode feature is also available in QPI mode for Fast Read Quad I/O with Four-Byte Address command. See the description on previous pages.

The Wrap Around feature is not available in QPI mode for Fast Read Quad I/O with Four-Byte Address command. To perform a read operation with fixed data length wrap around in QPI mode, use a dedicated Burst Read with Wrap (0Ch) command.

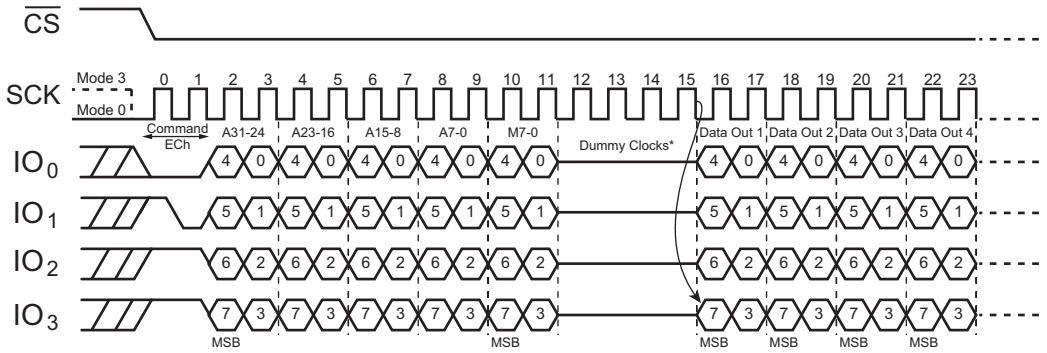


Figure 61. Fast Read Quad I/O with Four-Byte Address (QPI Mode; Initial command or previous M5-4≠10)

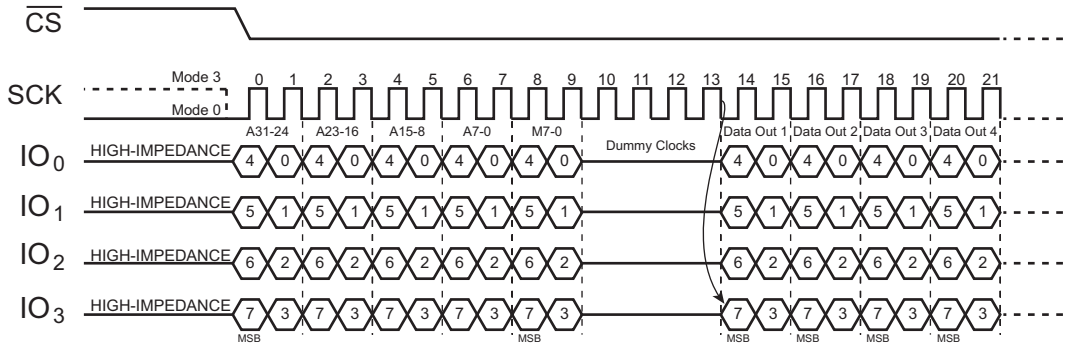


Figure 62. Fast Read Quad I/O with Four-Byte Address (QPI Mode; Initial command or previous M5-4=10)

7.2.14 DTR Quad I-O Fast Read with Four-Byte Address (EEh)

The DTR Quad I/O Fast Read with Four-Byte Address (EEh) command is similar to the Fast Read Dual I/O (BBh) command except that address and data bits are input and output through four pins IO_0, IO_1, IO_2, and IO_3, as well as four Dummy clocks, are required in SPI mode before the data output, as shown in Figure 63 to Figure 66.The Quad Enable bit (QE) of Status Register must be set to enable.

7.2.14.1 DTR Fast Read Quad I/O with Continuous Read Mode

The DTR Quad I/O Fast Read with Four-Byte Address command can further reduce command overhead through setting the Continuous Read Mode bits (M7-0) after the input Address bits (A31-0). The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O command through the inclusion or exclusion of the first byte opcode. The lower nibble bits of the (M3-0) are don't care (x); however, the IO pins must be high-impedance before the falling edge of the first data out clock.

If the Continuous Read Mode bits M5-4 = (1,0), the next DTR Quad I/O Fast Read with the Four-Byte Address command (after $\overline{CS}$ is raised and then lowered) does not require the EEh command code, as shown in Figure 64. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after $\overline{CS}$ is asserted low. If the Continuous Read Mode bits M5-4 do not equal to (1,0), the next command (after $\overline{CS}$ is raised and then lowered) requires the first byte command code, thus returning to normal operation.

When QPI mode is enabled, the number of dummy clocks is configured by the Set Read Parameters (C0h) command to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[6:4] setting, the number of dummy clocks can be configured from 6 to 20. The default number of dummy clocks on power-up or after a Reset command is 6. Note that the number of dummy includes M7-0.

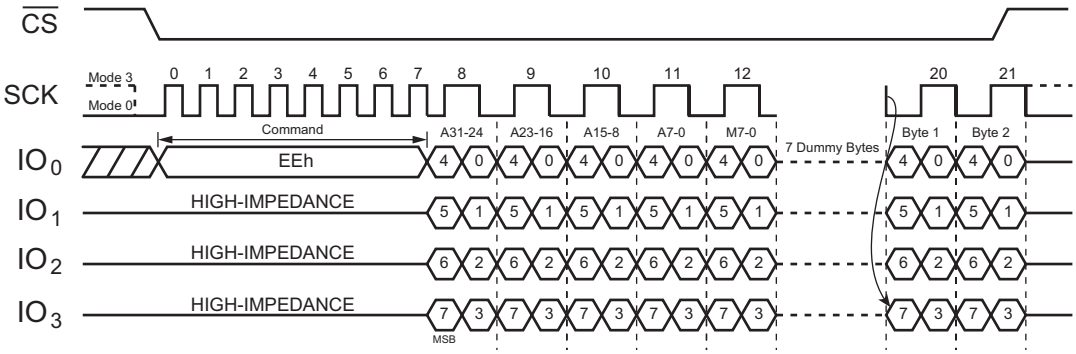


Figure 63. DTR Quad I/O Fast Read with Four-Byte Address (SPI Mode, Initial command or previous M5-4≠10)

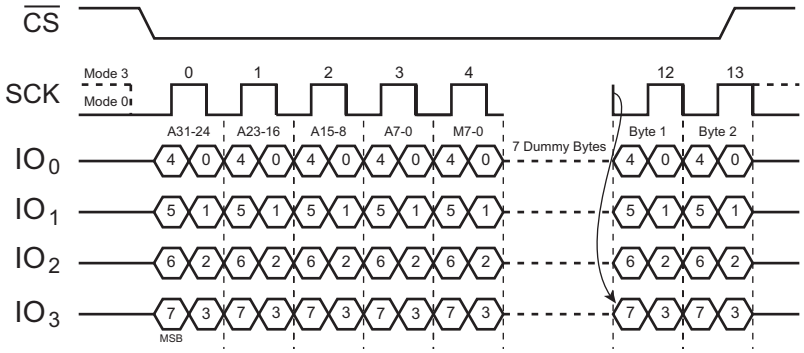


Figure 64. DTR Quad I/O Fast Read with Four-Byte Address (SPI Mode, Initial command or previous M5-4=10)

7.2.14.2 DTR Quad I/O Fast Read with Four-Byte Address with 8/16/32/64-Byte Wrap Around in Standard SPI Mode

The DTR Quad I/O Fast Read with Four-Byte Address command can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) command before EEh. This command can either enable or disable the Wrap Around feature for the following EEh commands. When Wrap Around is enabled, the data being accessed can be limited to either an 8, 16, 32, or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the command. Once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The Set Burst with Wrap command allows three Wrap Bits, W6-4, to be set. The W4 bit is used to enable or disable the Wrap Around operation, while W6-5 are used to specify the length of the wrap around section within a page.

7.2.14.3 DTR Quad I/O Fast Read with 4- Byte Address (EEh) in QPI Mode

The Continuous Read Mode feature is also available in QPI mode for DTR Quad I/O Fast Read with Four-Byte Address command.

The Wrap Around feature is not available in QPI mode for Fast Read Quad I/O command. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated Burst Read with Wrap (0Ch) command must be used.

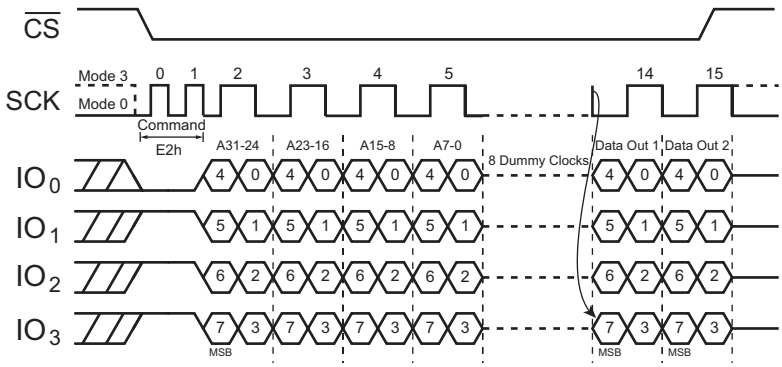


Figure 65. DTR Quad I/O Fast Read with Four-Byte Address (QPI Mode; Initial command or previous M5-4≠10)

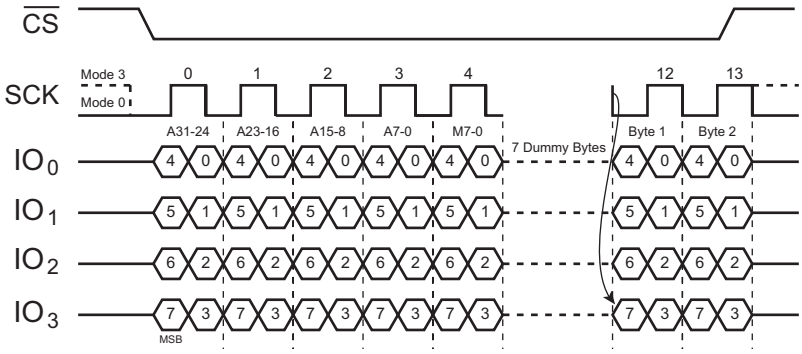


Figure 66. DTR Quad I/O Fast Read with Four-Byte Address (QPI Mode; Initial command or previous M5-4=10)

7.2.15 Set Burst with Wrap (77h)

The Set Burst with Wrap command is used in conjunction with the EBh, EDh, ECh, EEh, and E7 commands to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode. The Set Burst with Wrap command sequence is as follows: $\overline{CS}$ goes low → Send Set Burst with Wrap command → Send 24 Dummy bits → Send 8 Wrap bits → $\overline{CS}$ goes high.

If W6-4 is set by a Set Burst with Wrap command, all the following EBh, EDh, ECh, and EEh commands use the W6-4 setting to access the 8/16/32/64-byte section within any page (see Table 28). To exit the Wrap Around function and return to normal read operation, issue another Set Burst with Wrap command to set W4 = 1. The default value of W4 on power on is 1.

Table 28. W6 - W4 Settings

W6. W5	W4 = 0		W4 = 1	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	n/a
0 1	Yes	16-byte	No	n/a
1 0	Yes	32-byte	No	n/a
1 1	Yes	64-byte	No	n/a

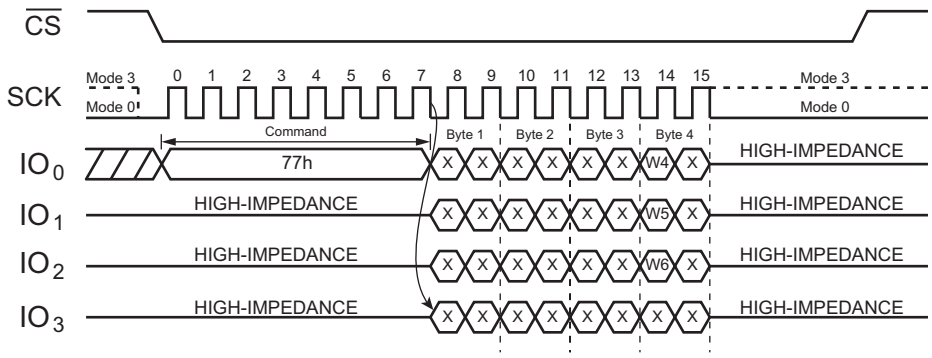


Figure 67. Set Burst with Wrap Sequence Diagram (SPI Mode only, Three-Byte Address Mode)

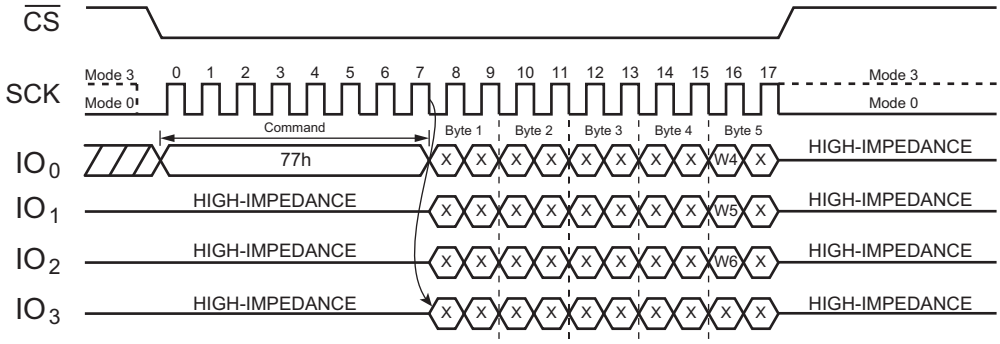


Figure 68. Set Burst with Wrap Sequence Diagram (SPI Mode only, Four-Byte Address Mode)

7.2.16 Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, the Set Read Parameters (C0h) command can be used to configure the number of dummy clocks for 0Bh, EBh, ECh, 0Ch, EDh, EEh, 0Eh, 4Bh, 48h, and 5Ah commands, as shown in Table 29, and to configure the number of bytes of Wrap Length for the 0Ch and 0Eh commands.

Table 29. Commands that Configure Number of Dummy Cycles in QPI Mode

Command	Opcode
Fast Read	0Bh
Fast Read Quad I/O	EBh
Fast Read Quad I/O with Four-Byte Address	ECh
Burst Read with Wrap	0Ch
DTR Fast Read Quad I/O	EDh
DTR Quad I/O Fast Read with 4-Byte Address	EEh
DTR Burst Read with Wrap	0Eh
Read Unique ID Number	4Bh
Read Security Registers	48h
Read Serial Flash Discoverable Parameter	5Ah

In Standard SPI mode, this command is not accepted. The dummy clocks for various Fast Read commands in Standard/Dual/Quad SPI mode are fixed (see Table 15 to Table 26 for details). The Wrap Length is set by the W5-4 bits in the Set Burst with Wrap (77h) command. This setting remains unchanged when the device is switched from Standard SPI to QPI. The default Wrap Length after a power-up or a Reset command is eight bytes; the default number of dummy clocks is four. The number of dummy clocks is only programmable for 0Bh, EBh, ECh, 0Ch, 4Bh, 48h, and 5Ah commands in QPI mode. Whenever the device is switched from SPI mode to QPI mode, the number of dummy clocks must be set again before any 0Bh, EBh, ECh, 0Ch, 4Bh, 48h, and 5Ah commands.

Table 30 shows the configuration of dummy numbers for non-DTR commands (0Bh, EBh, ECh, 0Ch, 48h, and 5Ah).

Table 30. Configuration of the Number of Dummies for Non-DTR Commands

P6 - P4	Dummy Clocks	Max Read Freq. A[1:0]=0,0		P1 - P0	Wrap Length
0 0 0	4	70 MHz		0 0	8-byte
0 0 1	6	108 MHz			
0 1 0	8	133 MHz		0 1	16-byte
0 1 1	10	166 MHz			
1 0 0	12	166 MHz		1 0	32-byte
1 0 1	14	166 MHz			
1 1 0	16	166 MHz		1 1	64-byte
1 1 1	18	166 MHz			

Table 31 shows the configuration of dummy numbers for DTR commands (EDh, EEh, and 0Eh).

Table 31. Configuration of the Number of Dummies for DTR Commands

P6 - P4	Dummy Clocks	Max Read Freq. A[1:0]=0,0		P1 - P0	Wrap Length
0 0 0	6	54 MHz		0 0	8-byte
0 0 1	8	54 MHz			
0 1 0	10	66 MHz		0 1	16-byte
0 1 1	12	66 MHz			
1 0 0	14	66 MHz		1 0	32-byte
1 0 1	16	66 MHz			
1 1 0	18	66 MHz		1 1	64-byte
1 1 1	20	66 MHz			

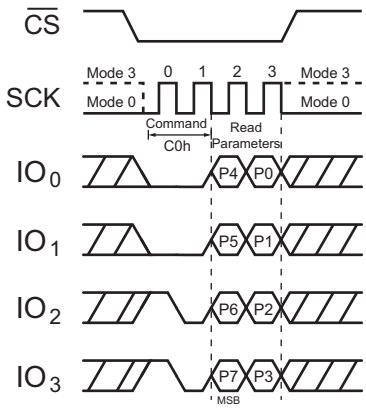


Figure 69. Burst Read with Wrap (QPI Mode Only)

7.2.17 Burst Read with Wrap (0Ch)

This command provides an alternative way to perform the read operation with Wrap Around in QPI mode. The command is similar to the Fast Read (0Bh) command in QPI mode, except the addressing of the read operation wraps around to the beginning boundary of the Wrap Length once the ending boundary is reached. The Wrap Length and the number of dummy clocks can be configured by the Set Read Parameters (C0h) command.

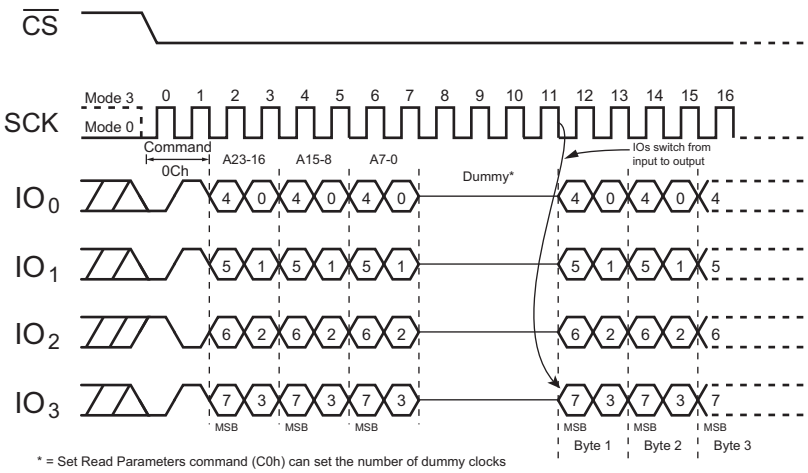


Figure 70. Burst Read with Wrap (QPI Mode Only, Three-Byte Address Mode)

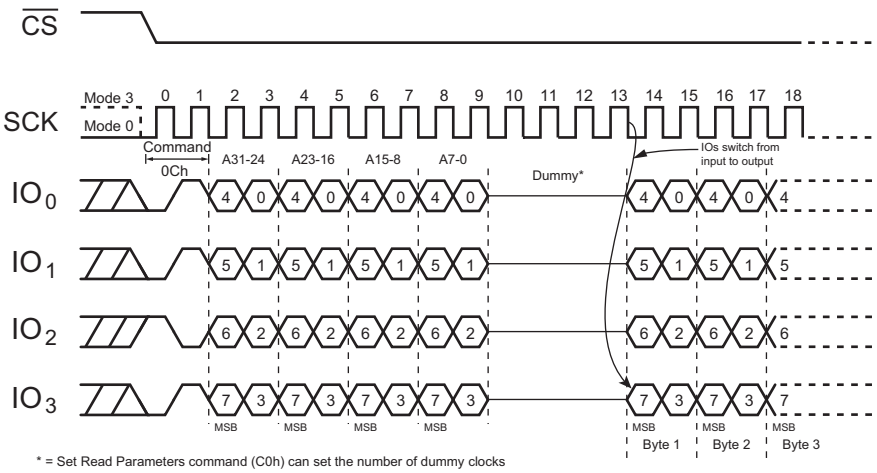


Figure 71. Burst Read with Wrap (QPI Mode Only, Four-Byte Address Mode)

7.2.18 DTR Burst Read with Wrap (0Eh)

This command provides an alternative way to perform the read operation with Wrap Around in QPI mode. The command is similar to the Fast Read (0Bh) command in QPI mode, except the addressing of the read operation wraps around to the beginning boundary of the Wrap Length once the ending boundary is reached.

The Wrap Length can be configured by the Set Read Parameters (C0h) command.

The number of dummy clocks is configured by the Set Read Parameters (C0h) command to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[6:4] setting, the number of dummy clocks can be configured from 6 to 20.

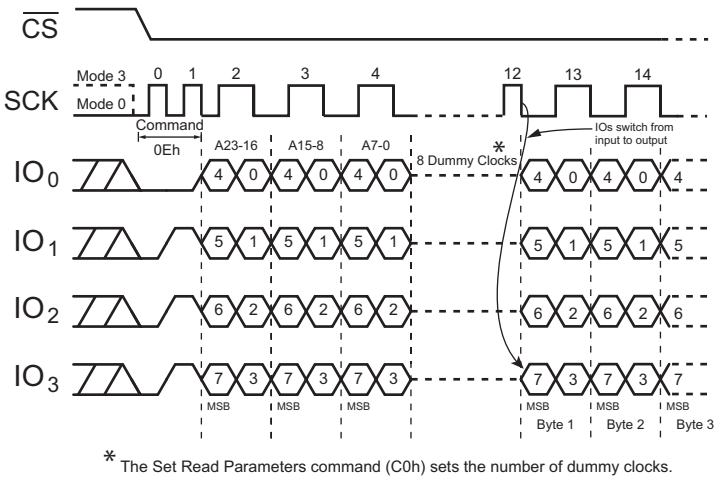


Figure 72. DTR Burst Read with Wrap (QPI Mode Only, Three-Byte Address Mode)

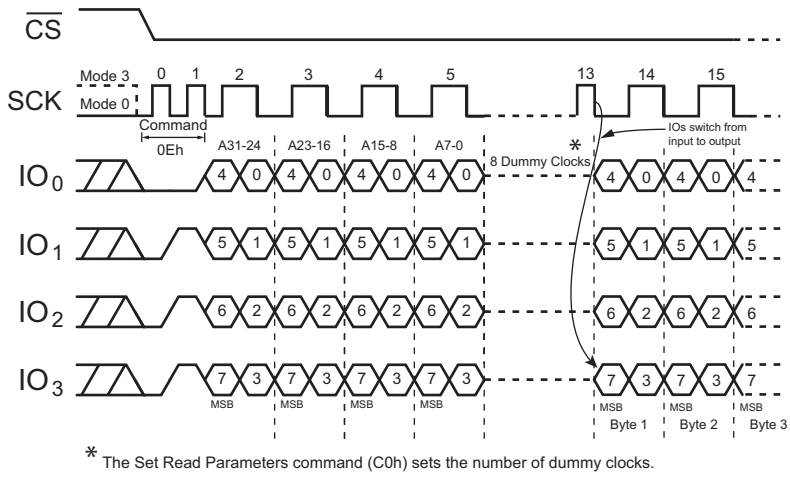


Figure 73. DTR Burst Read with Wrap (QPI Mode Only, Four-Byte Address Mode)

7.3 Security Commands

7.3.1 Read Security Registers (48h)

The Read Security Registers command is similar to Fast Read command. The command is followed by a three- or four-byte address (A23/A31 - A0) and a dummy byte. The number of dummy bytes can be configured by the C0h command. Each bit is latched in during the rising edge of SCK. The memory content at that address then is shifted out on SO, each bit being shifted out at a Max frequency f_C, during the falling edge of SCK. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out. Once the A8 - A0 address reaches the last byte of the register (byte FFh), it resets to 000h. The command is completed by driving $\overline{CS}$ high.

Table 32. Read Security Registers

Address	A23/A31-A16	A15-A12	A11-A9	A8-A0
Security Registers 1	00h/0000h	0001	000	Byte Address
Security Registers 2	00h/0000h	0010	000	Byte Address
Security Registers 3	00h/0000h	0011	000	Byte Address

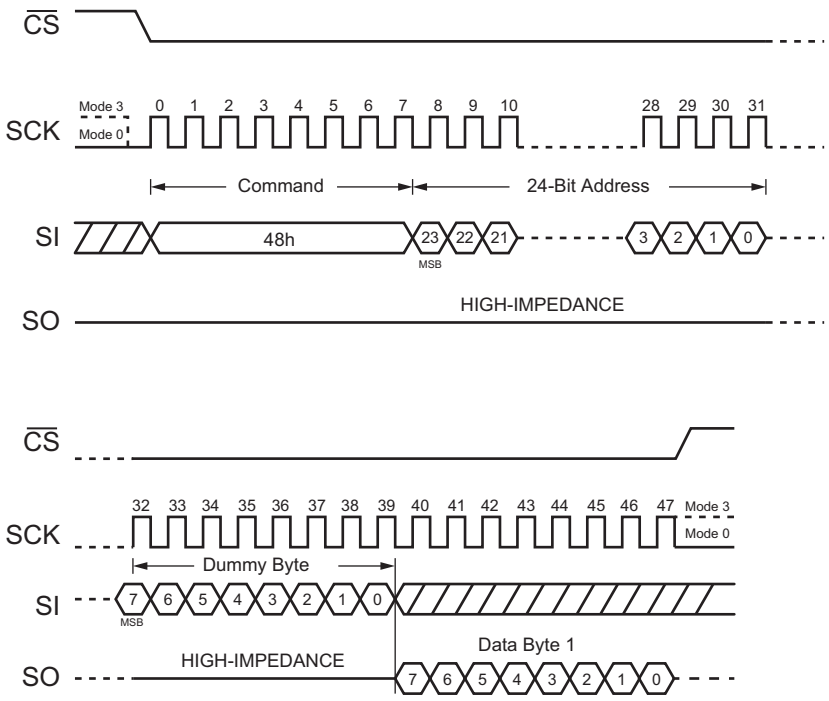


Figure 74. Read Security Registers Command Sequence Diagram (SPI Mode, Three-Byte Address Mode)

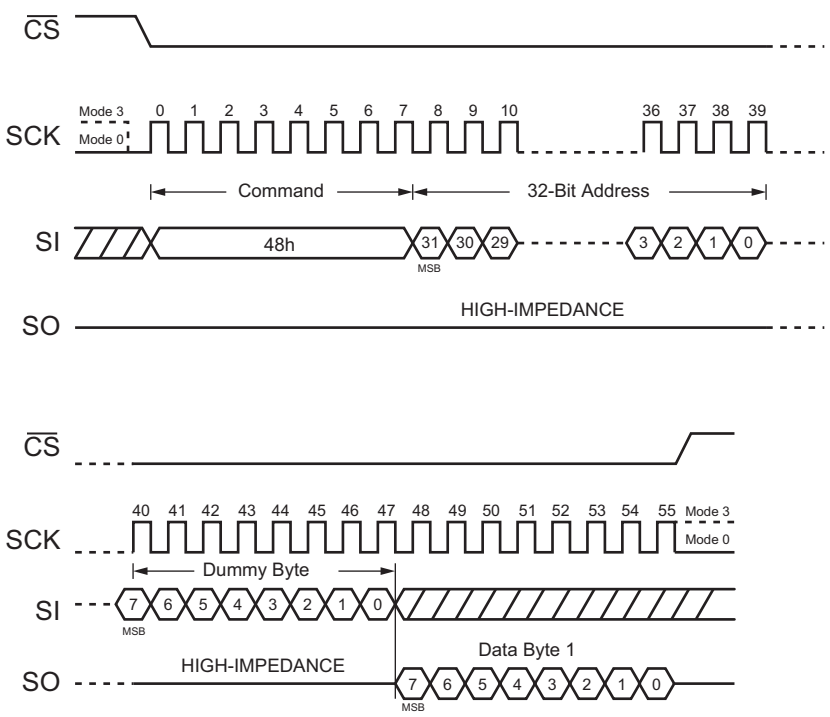
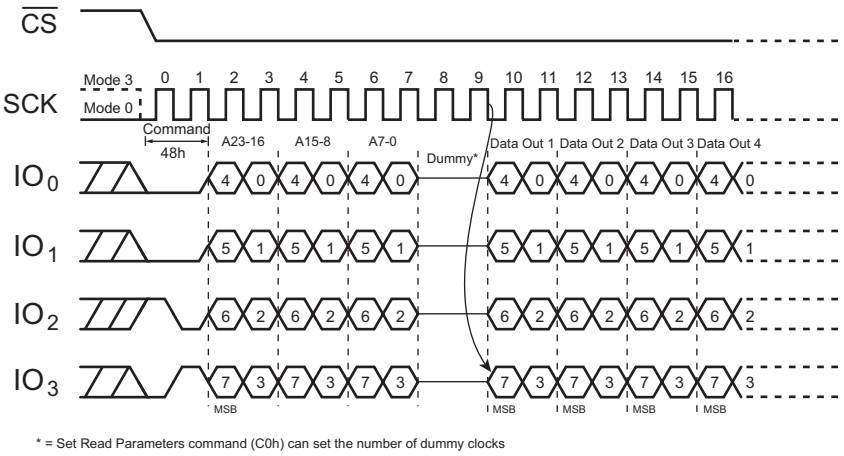


Figure 75. Read Security Registers Command Sequence Diagram (SPI Mode, Four-Byte Address Mode)



* = Set Read Parameters command (C0h) can set the number of dummy clocks

Figure 76. Read Security Registers Command Sequence Diagram (QPI Mode, Three-Byte Address Mode)

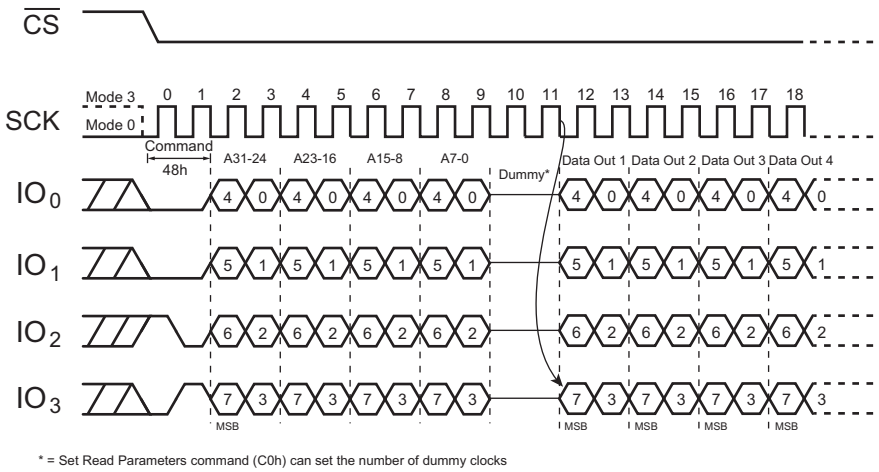


Figure 77. Read Security Registers Command Sequence Diagram (QPI Mode, Four-Byte Address Mode)

7.3.2 Erase Security Registers (44h)

The AT25SF2561C / AT25QF2561C provides three 1024-byte Security Registers which can be erased and programmed individually. These registers can be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Block Erase command. A Write Enable command must have been executed before to set the Write Enable Latch bit.

The Erase Security Registers command sequence is: $\overline{CS}$ goes low, the host sends the Erase Security Registers command, then $\overline{CS}$ goes high. No address is required for this command. $\overline{CS}$ must be driven high after the eighth bit of the command code has been latched in; otherwise, the Erase Security Registers command is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Erase Security Registers cycle (whose duration is t_{SE}) is initiated. While the Erase Security Registers cycle is in progress, the Status Register can be read to check the value of the RDY/BSY bit. This bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it the operation completes. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers are permanently locked; the Erase Security Registers command is ignored.

Table 33. Erase Security Registers

Address	A23/A31-A16	A15-A12	A11-A9	A0-A0
Security Registers 1	00h/0000h	0001	000	Byte Address
Security Registers 2	00h/0000h	0010	000	Byte Address
Security Registers 3	00h/0000h	0011	000	Byte Address

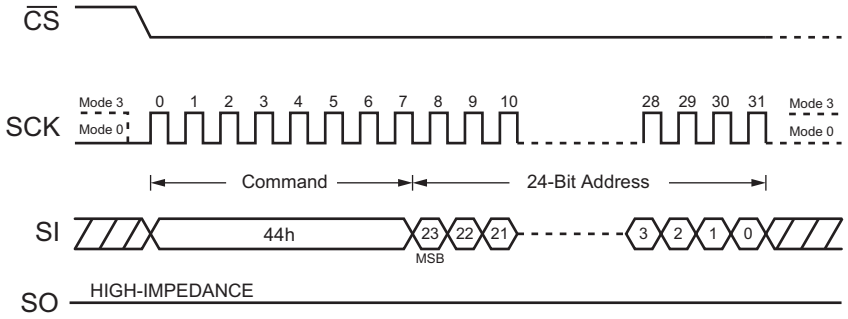


Figure 78. Erase Security Registers Command Sequence Diagram (SPI Mode, Three-Byte Address Mode)

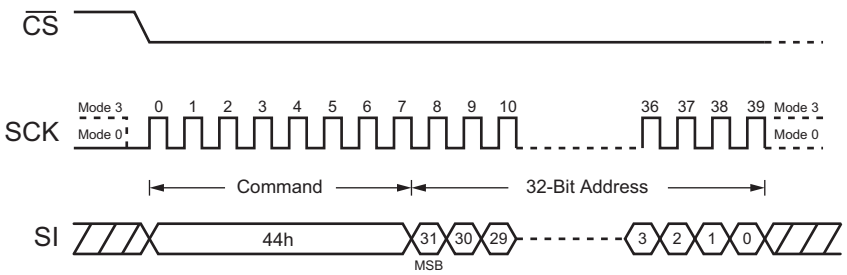


Figure 79. Erase Security Registers Command Sequence Diagram (SPI Mode, Four-Byte Address Mode)

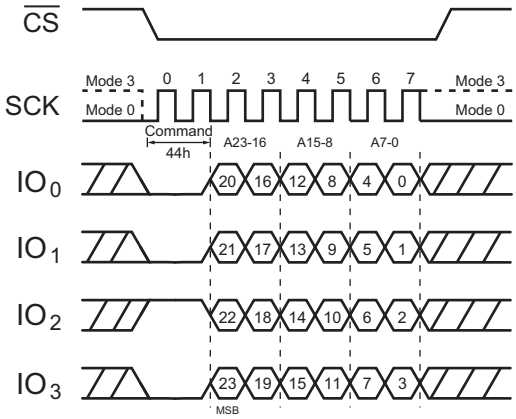


Figure 80. Erase Security Registers Command Sequence Diagram (QPI Mode, Three-Byte Address Mode)

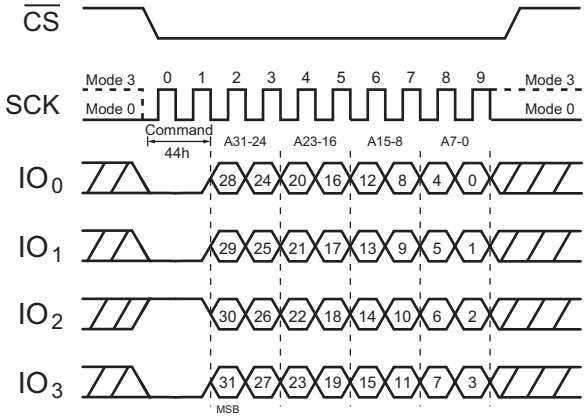


Figure 81. Erase Security Registers Command Sequence Diagram (QPI Mode, Four-Byte Address Mode)

7.3.3 Program Security Registers (42h)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 1024 bytes of Security Registers data to be programmed by two times (one-time program 256 bytes). A Write Enable command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command.

The Program Security Registers command is entered by driving $\overline{CS}$ low, followed by the command code (42h), a three- or four-byte address and at least one data byte on the SI pin. As soon as $\overline{CS}$ is driven high, the self-timed Program Security Registers cycle (whose duration is t_{PP}) is initiated. While the Program Security Registers cycle is in progress, the Status Register can be read to check the value of the RDY/BSY bit. The RDY/BSY bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

If the Security Registers Lock bit (LB3/LB2/LB1) bits are set to 1, the Security Registers are permanently locked. The Program Security Registers command is ignored.

Table 34. Program Security Registers

Address	A23/A31-A16	A15-A12	A11-A9	A0-A0
Security Registers 1	00h/0000h	0001	000	Byte Address
Security Registers 2	00h/0000h	0010	000	Byte Address
Security Registers 3	00h/0000h	0011	000	Byte Address

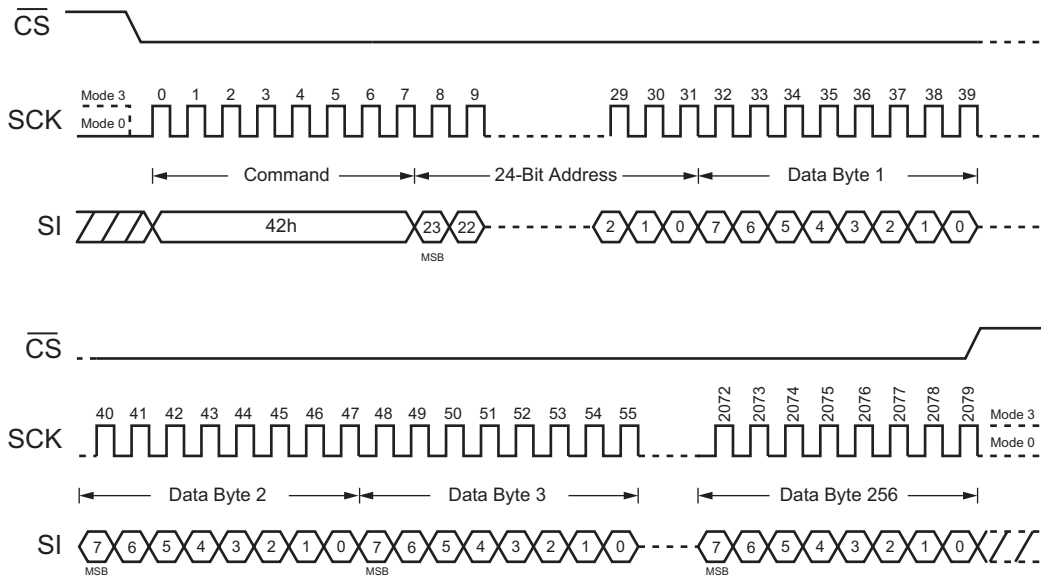


Figure 82. Program Security Registers Command Sequence Diagram (SPI Mode, Three-Byte Address Mode)

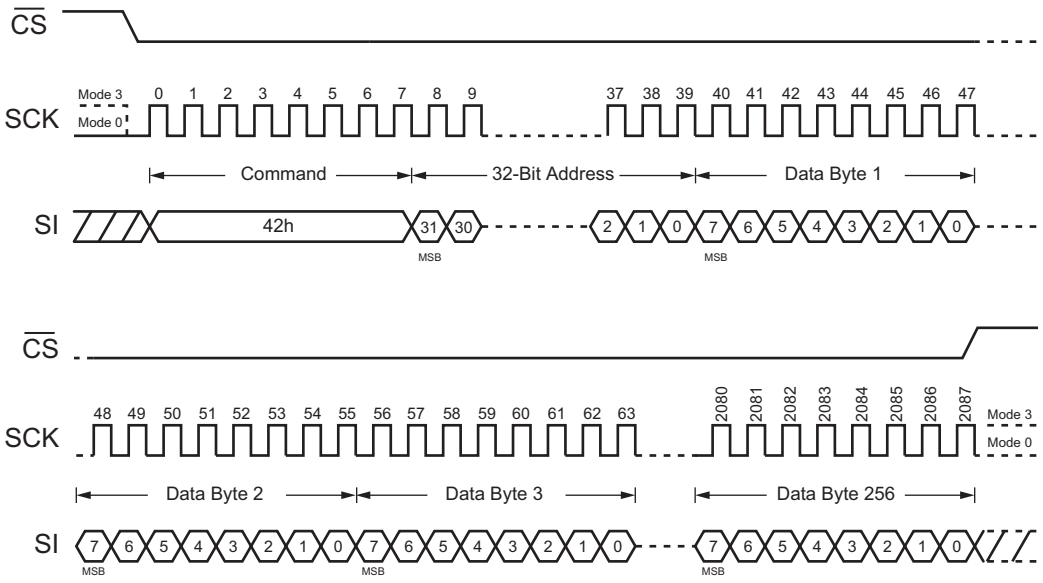


Figure 83. Program Security Registers Command Sequence Diagram (SPI Mode, Four-Byte Address Mode)

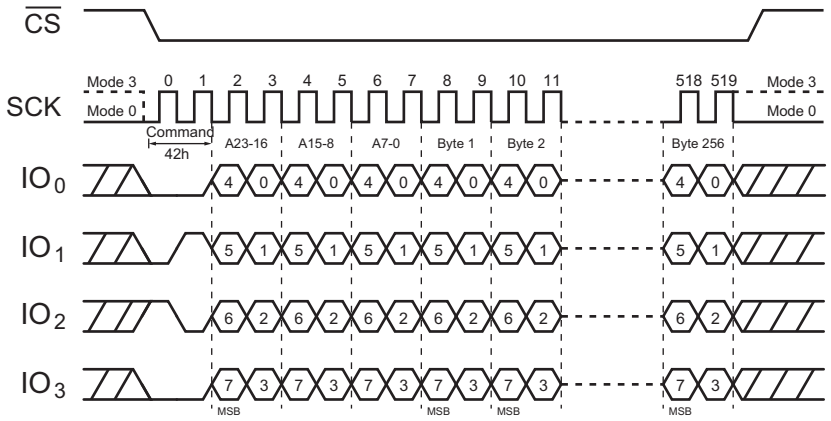


Figure 84. Program Security Registers Command Sequence Diagram (QPI Mode, Three-Byte Address Mode)

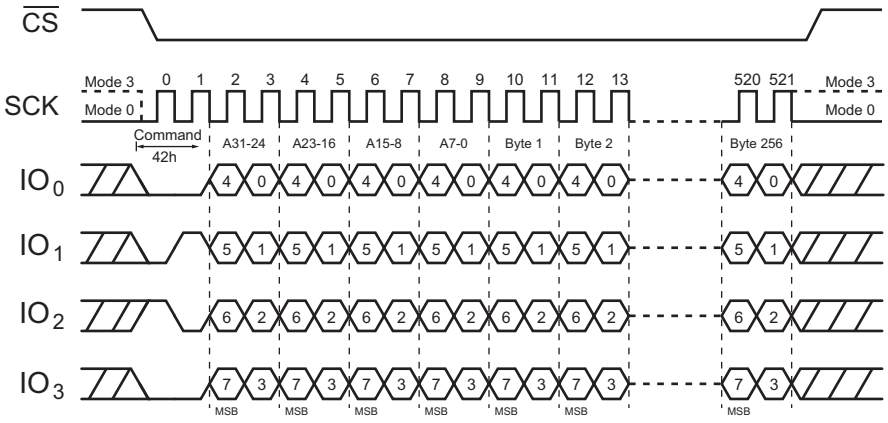


Figure 85. Program Security Registers Command Sequence Diagram (QPI Mode, Four-Byte Address Mode)

7.3.4 Read Serial Flash Discoverable Parameter (5Ah)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial Flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the *Introduction of JEDEC Standard, JESD68on CFI*. SFDP is a standard of JEDEC Standard No.216.

The Read SFDP command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 5Ah, followed by a 24-bit address (A23-A0) into the SI pin, regardless of the three- or 4-byte Address Mode. Eight dummy clocks are also required in SPI mode. In QPI mode, the number of dummy clocks can be configured by the Set Read Parameters (C0h) command.

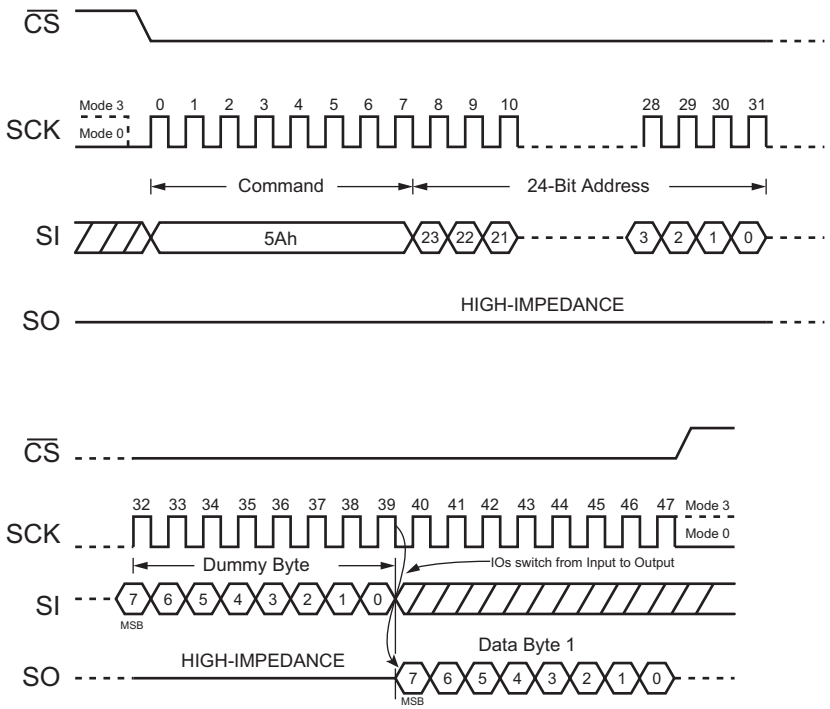


Figure 86. Read Serial Flash Discoverable Parameter Command Sequence Diagram (SPI Mode)

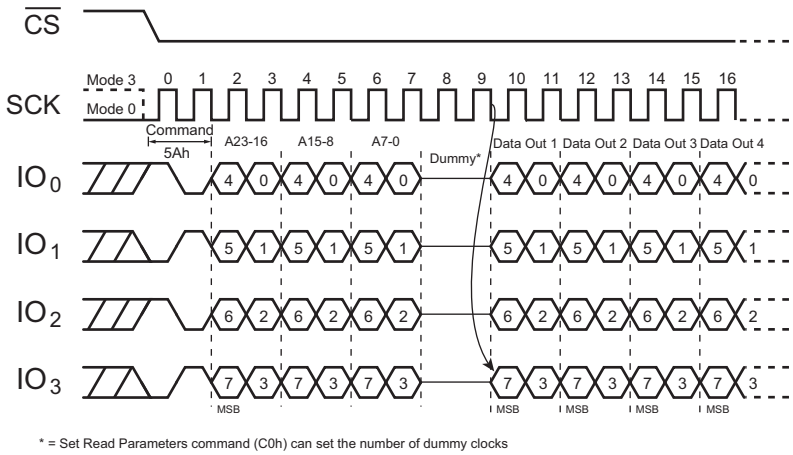


Figure 87. Read Serial Flash Discoverable Parameter Command Sequence Diagram (QPI Mode)

7.4 ID Commands

The AT25SF2561C / AT25QF2561C supports commands to access device identification that indicates the manufacturer, device type, and memory density. For the AT25SF2561C, the returned data bytes provide the information shown in Table 35. For the AT25QF2561C, the returned data bytes provide the information shown in Table 36.

Table 35. Manufacturer and Device ID Information for the AT25SF2561C

Command	Opcode	Manufacturing ID (Byte #1)	Device ID (Byte #2)	Device ID (Byte #3)
Read Manufacturer and Device ID	9Fh	1Fh	8Ah	01h
Read ID (Legacy Command)	90h	1Fh		18h
Read ID (Dual I/O)	92h	1Fh		18h
Read ID (Quad I/O)	94h	1Fh		18h
Resume from Deep Power-Down and Read Device ID	ABh			18h

Table 36. Manufacturer and Device ID Information for the AT25QF2561C

Command	Opcode	Manufacturing ID (Byte #1)	Device ID (Byte #2)	Device ID (Byte #3)
Read Manufacturer and Device ID	9Fh	1Fh	8Ah	81h
Read ID (Legacy Command)	90h	1Fh		18h
Read ID (Dual I/O)	92h	1Fh		18h
Read ID (Quad I/O)	94h	1Fh		18h
Resume from Deep Power-Down and Read Device ID	ABh			18h

7.4.1 Read Manufacturer ID/ Device ID (90h)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down/Device ID command that provides both the JEDEC-assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 90h, followed by a 24-bit address (A23-A0) of 000000h, regardless of the 3-byte/4-byte address mode. If the 24-bit address is initially set to 000001h, the Device ID is read first.

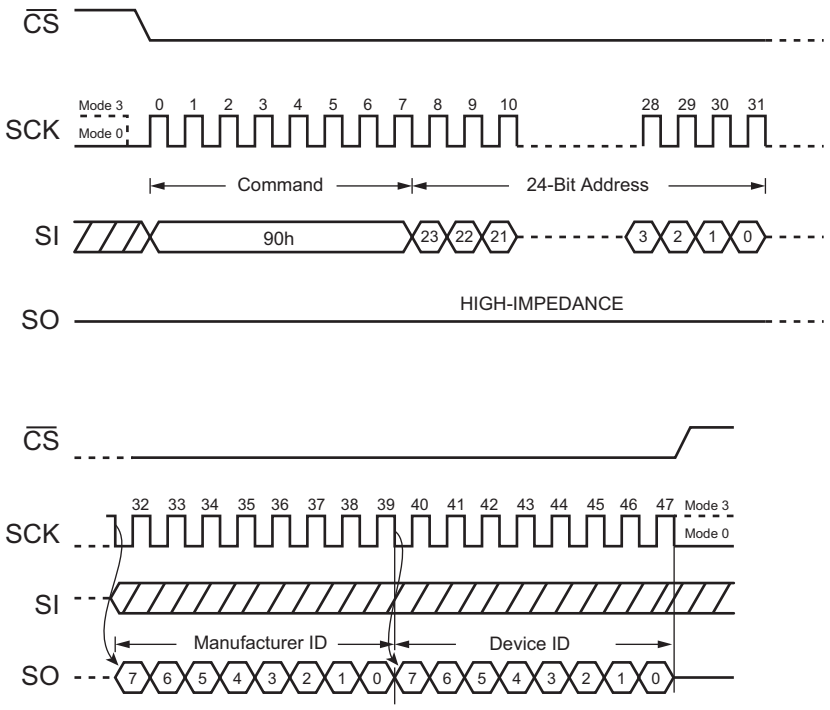


Figure 88. Read Manufacturer ID/ Device ID Sequence Diagram (SPI Mode)

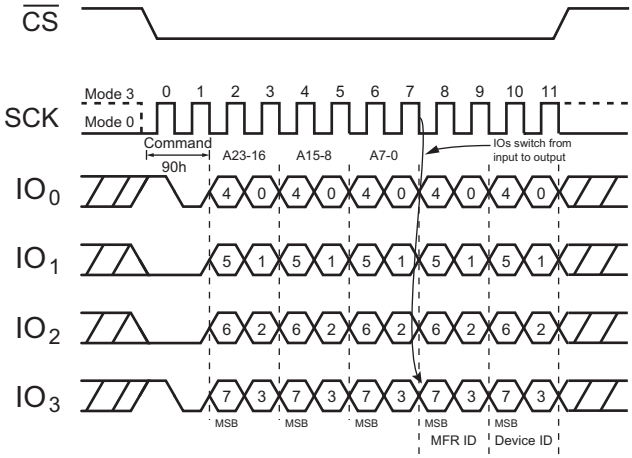


Figure 89. Read Manufacturer ID/ Device ID Sequence Diagram (QPI Mode)

7.4.2 Dual I/O Read Manufacturer ID/ Device ID (92h)

The Dual I/O Read Manufacturer/Device ID command is an alternative to the Release from Power-Down/Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by Dual I/O.

The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 92h followed by a 24- or 32-bit address (A23/A31 - A0) of 000000h/00000000h. If the 24/32-bit address is initially set to 000001h/00000001h, the Device ID is read first.

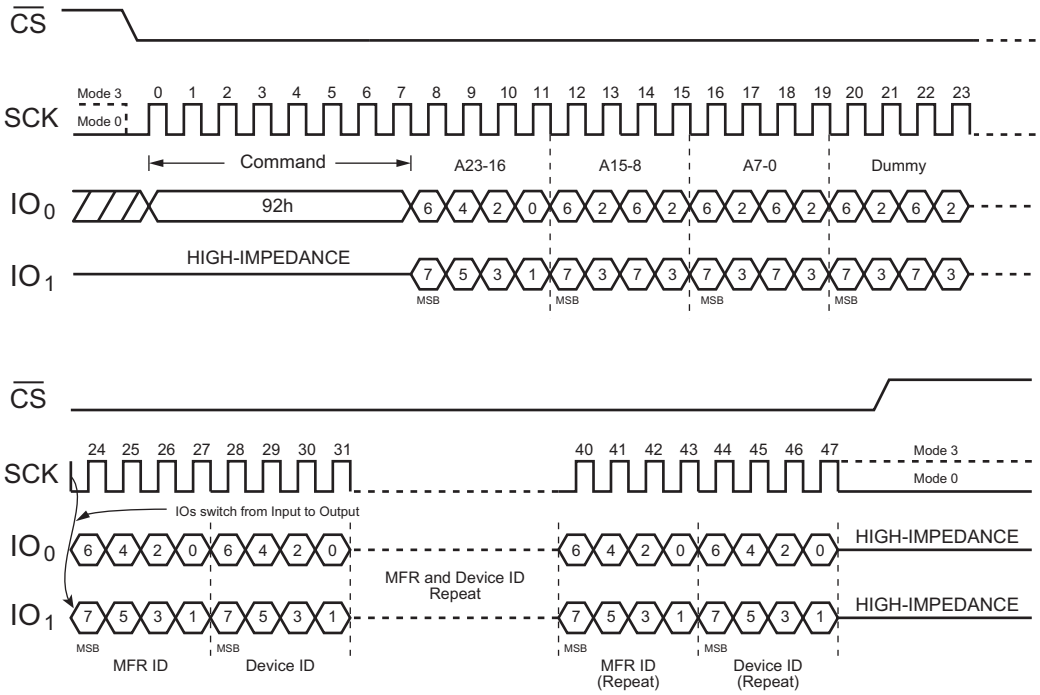


Figure 90. Dual I/O Read Manufacturer ID/Device ID Sequence Diagram (SPI Mode, Three-Byte Address Mode)

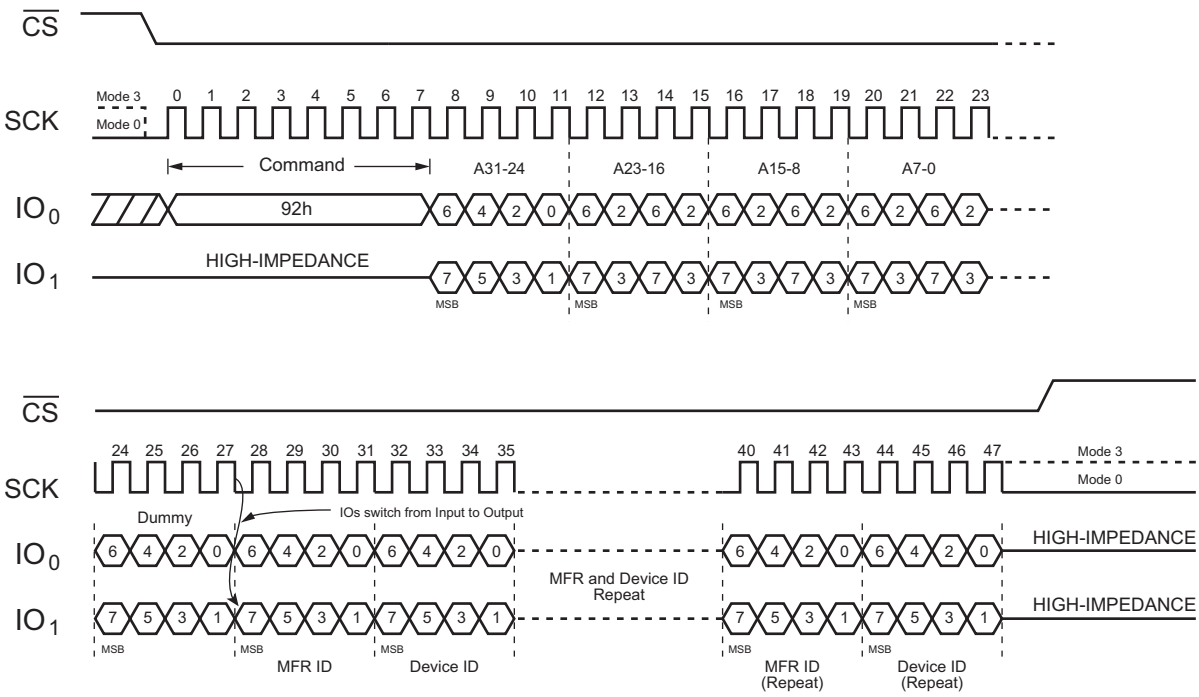


Figure 91. Dual I/O Read Manufacturer ID/Device ID Sequence Diagram (SPI Mode, Four-Byte Address Mode)

7.4.3 Quad I/O Read Manufacturer ID/ Device ID (94h)

The Quad I/O Read Manufacturer/Device ID command is an alternative to the Release from Power-Down/Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O. The Quad Enable bit (QE) of the Status Register must be set to enable. The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 94h, followed by a 24/32-bit address (A23/A31 - A0) of 000000h/00000000h and six dummy clocks. If the 24/32-bit address is initially set to 000001h/00000001h, the Device ID is read out first.

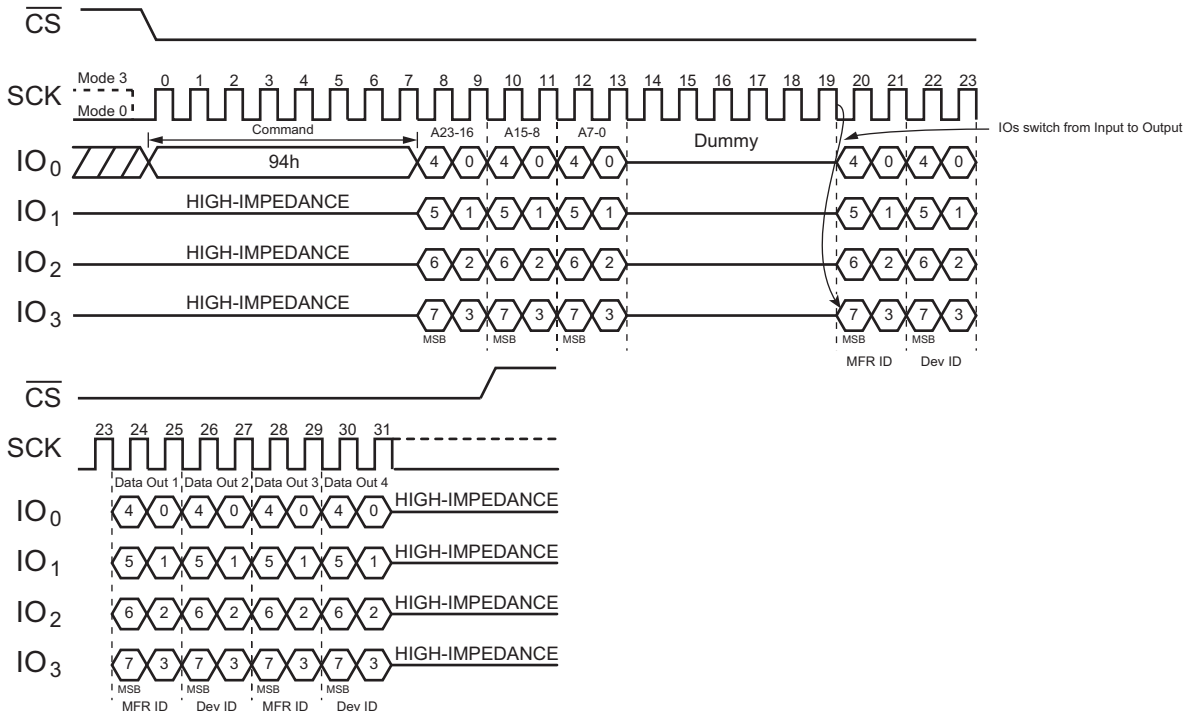


Figure 92. Quad I/O Read Manufacturer ID/Device ID Sequence Diagram (SPI Mode, Three-Byte Address Mode)

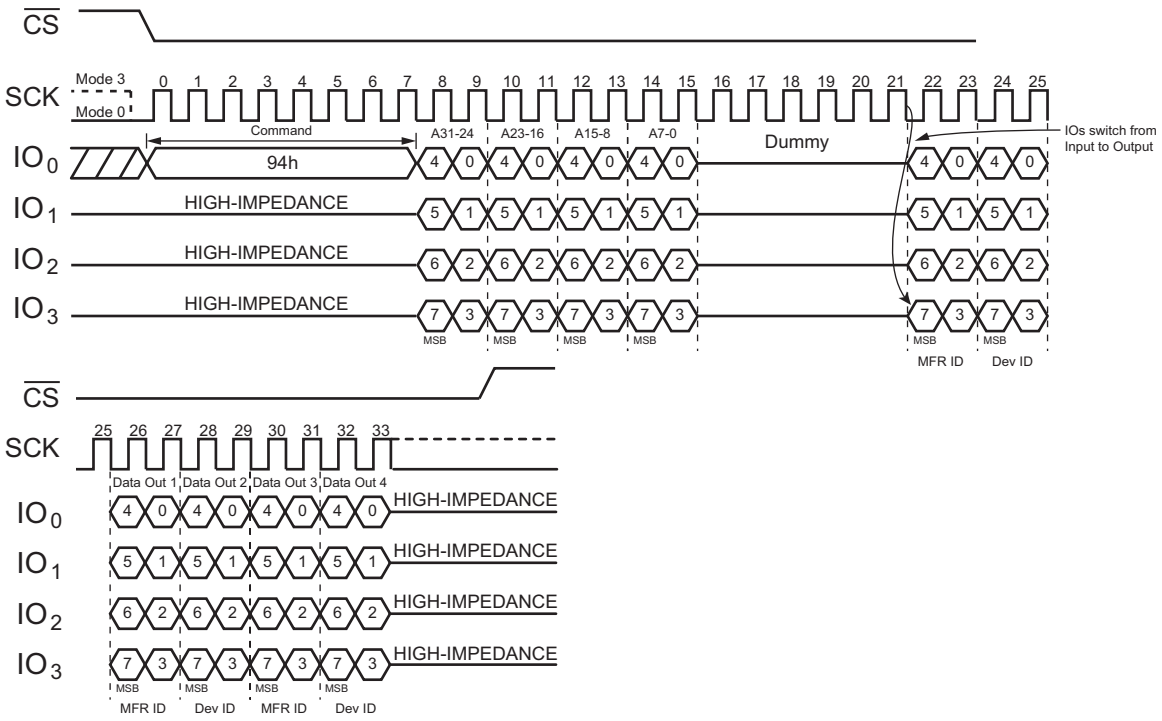


Figure 93. Quad I/O Read Manufacturer ID/Device ID Sequence Diagram (SPI Mode, Four-Byte Address Mode)

7.4.4 Read JEDEC ID (9Fh)

The JEDEC ID command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. During an Erase or Program cycle is in progress, the JEDEC ID command is not decoded and has no effect on the cycle that is in progress. Do not issue the JEDEC ID command while the device is in Deep Power-Down Mode.

The device is first selected by driving $\overline{CS}$ to low. Then, the eight-bit command code for the command is shifted in. This is followed by the 24-bit device identification (eight-bit manufacturer ID ID[23:16] — eight-bit memory type ID[15:8] — eight-bit memory capacity ID[7:0]). This value is shifted out on serial data output, each bit being shifted out during the falling edge of SCK. The JEDEC ID command is terminated by driving $\overline{CS}$ to high at any time during data output. When $\overline{CS}$ is driven high, the device is put in the standby mode. Once in the standby mode, the device waits to be selected, so that it can receive, decode, and execute commands.

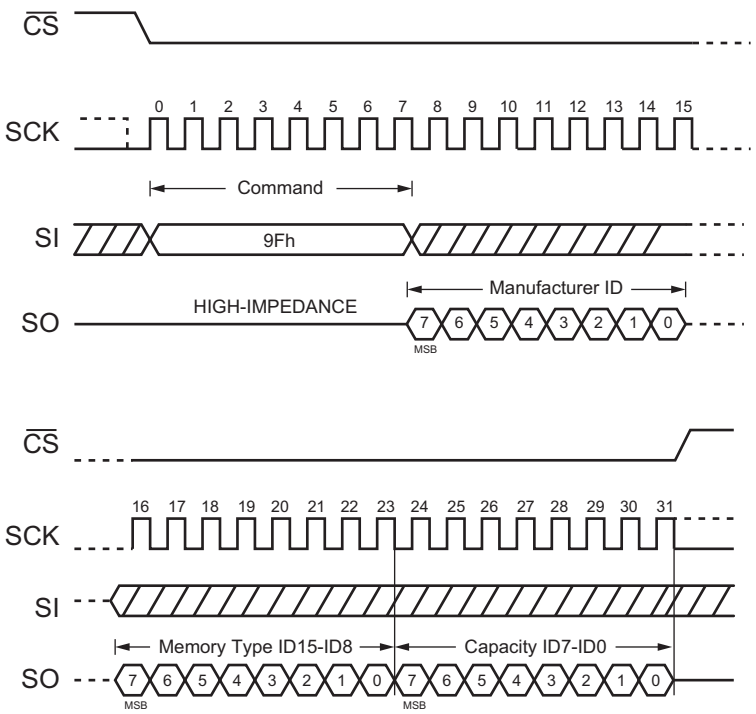


Figure 94. JEDEC ID Sequence Diagram (SPI Mode)

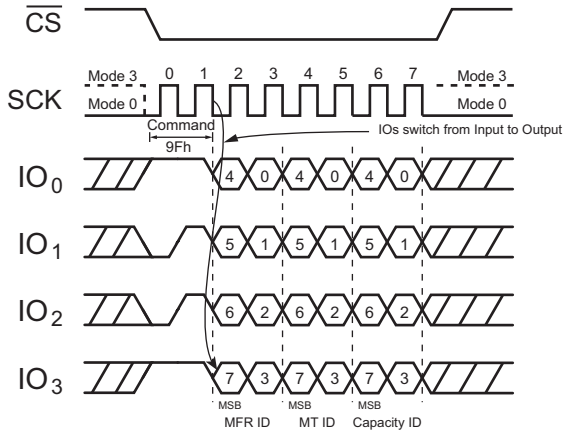


Figure 95. JEDEC ID Sequence Diagram (QPI Mode)

7.4.5 Read Unique ID Number (4Bh)

The Read Unique ID Number command accesses a factory-set read-only 128-bit number that is unique to each AT25SF2561C / AT25QF2561C device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 4Bh, followed by a four or five bytes of dummy clocks in SPI Mode. In QPI Mode, it contains three or four bytes dummy clocks and some dummy clocks that can be configured by the Set Read Parameters (C0h) command. After this, the 128-bit ID is shifted out on the falling edge of SCK.

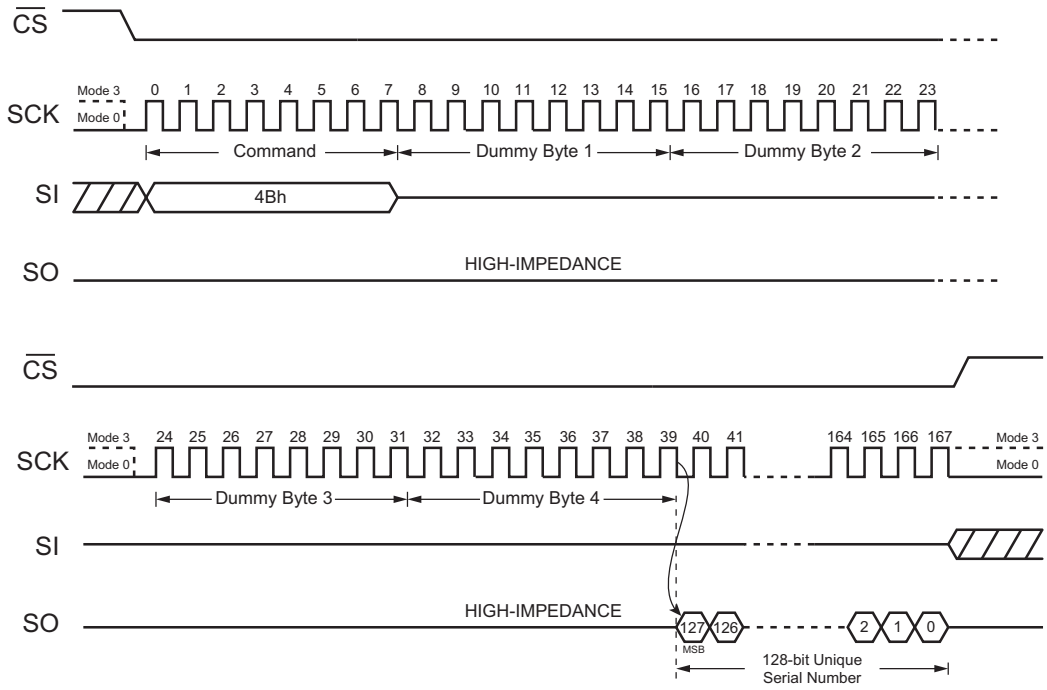


Figure 96. Read Unique ID Sequence Diagram (SPI Mode, Three-Byte Address Mode)

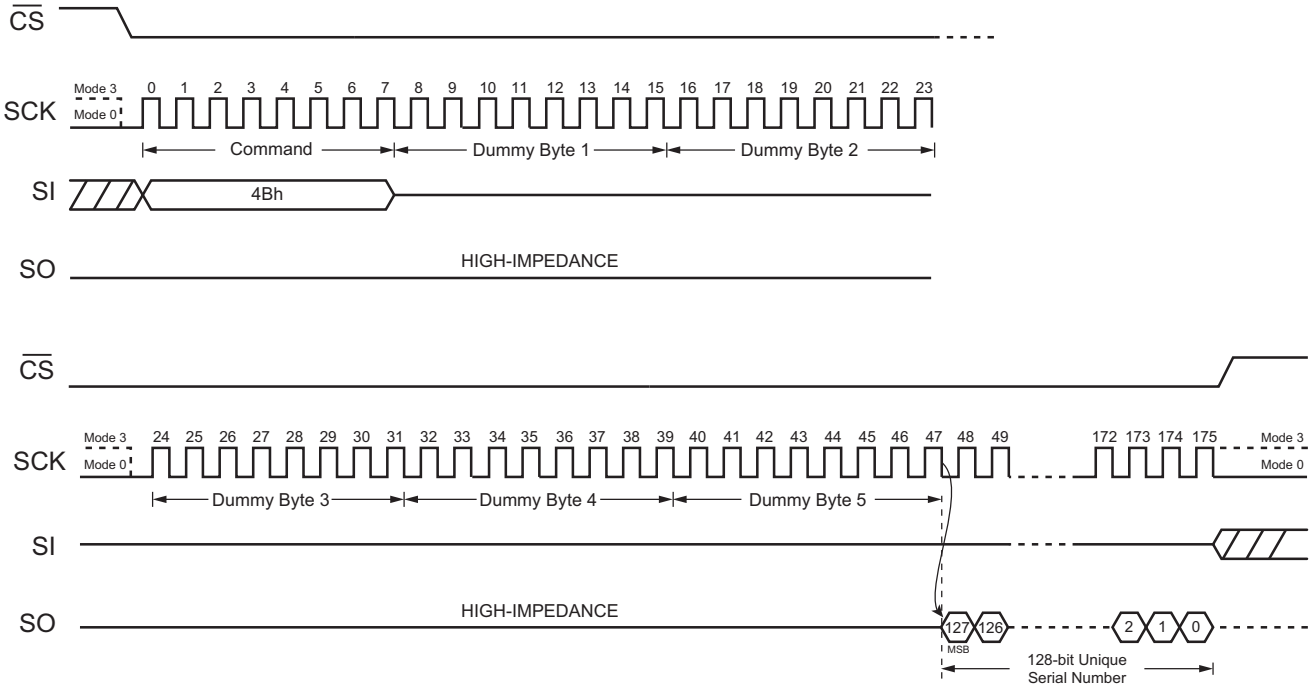


Figure 97. Read Unique ID Sequence Diagram (SPI Mode, Four-Byte Address Mode)

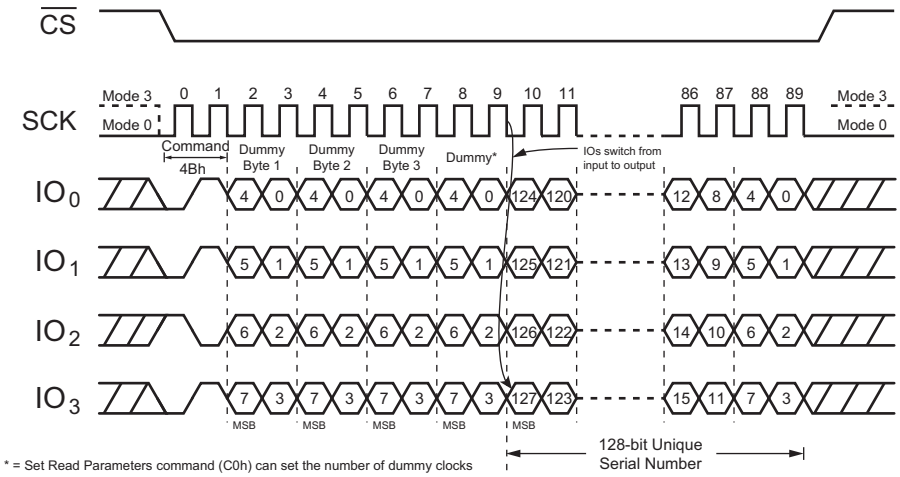


Figure 98. Read Unique ID Sequence Diagram (QPI Mode, Three-Byte Address Mode)

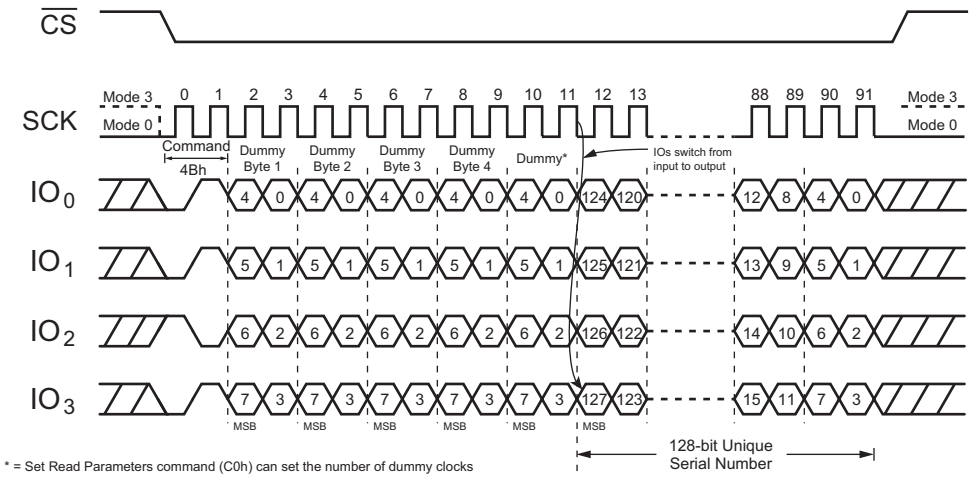


Figure 99. Read Unique ID Sequence Diagram (QPI Mode, Four-Byte Address Mode)

7.5 Power-Down Commands

7.5.1 Deep Power-Down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down command. The lower power consumption makes the Deep Power-down (DPD) command especially useful for battery powered applications (see I_{CC1} and I_{CC2}). The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code B9h, as shown in Figure 100 and Figure 101.

The $\overline{CS}$ pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power-Down command is not executed. After $\overline{CS}$ is driven high, the power-down state is entered within the time duration of t_{DP}. While in the power-down state only the Release from Deep Power-down / Device ID command, software reset sequence, or hardware reset sequence, which restores the device to normal operation, is recognized. All other commands are ignored. This includes the Read Status Register command, which is always available during normal operation. Ignoring all but one command also makes the Power-Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of I_{CC1}.

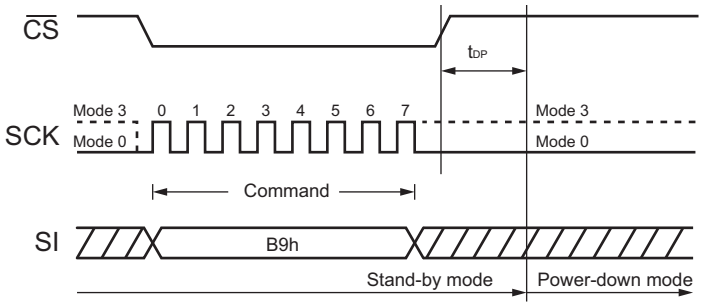


Figure 100. Deep Power-Down Sequence Diagram (SPI Mode)

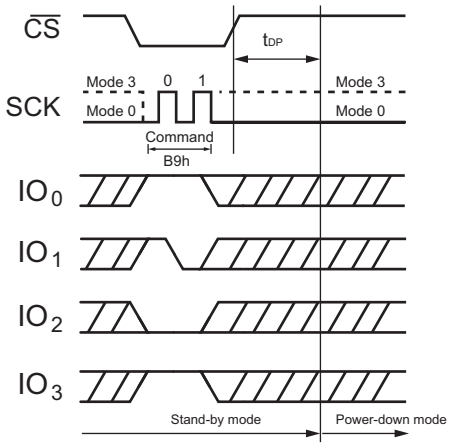


Figure 101. Deep Power-Down Sequence Diagram (QPI Mode)

7.5.2 Release from Deep Power-Down/Read Device ID (ABh)

The Release from Power-Down or Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the $\overline{CS}$ pin low, shifting the command code ABh and driving $\overline{CS}$ high. Release from Power-Down takes of t_{RES1} time (see Section 8.7, AC Electrical Characteristics) before the device resumes normal operation and other command are accepted. The $\overline{CS}$ pin must remain high during the t_{RES1} time.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the $\overline{CS}$ pin low and shifting the command code ABh, followed by three dummy bytes. The Device ID bits are then shifted out on the falling edge of SCK, with the most significant bit (MSB) first, as shown in Figure 104 and Figure 105. The Device ID value for is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving $\overline{CS}$ high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure 104 and Figure 105, except that after $\overline{CS}$ is driven high it must remain high for a time duration of t_{RES2} (see Section 8.7, AC Electrical Characteristics). After this time, the device resumes normal operation, and other commands are accepted. If the Release from Power-Down/Device ID command is issued while an Erase, Program or Write cycle is in process (when RDY/BSY equal 1), the command is ignored and does not effect the current cycle.

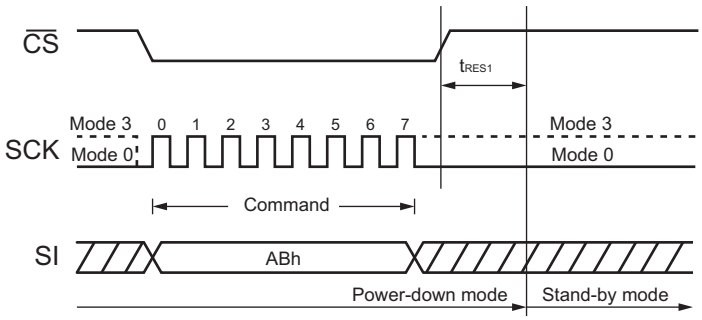


Figure 102. Release Power-Down Sequence Diagram (SPI Mode)

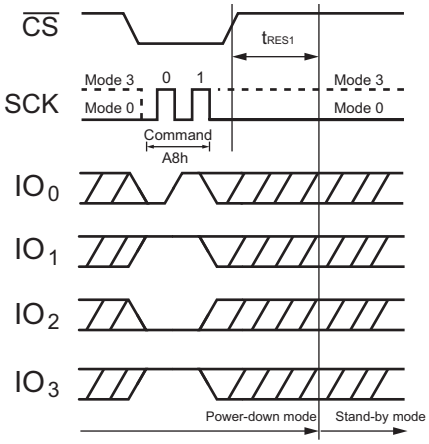


Figure 103. Release Power-Down Sequence Diagram (QPI Mode)

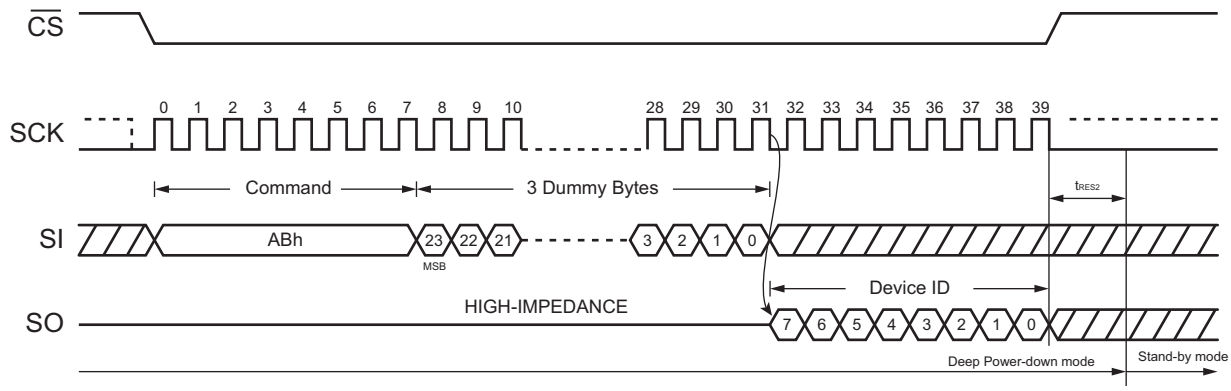


Figure 104. Release Power-Down/Read Device ID Sequence Diagram (SPI Mode)

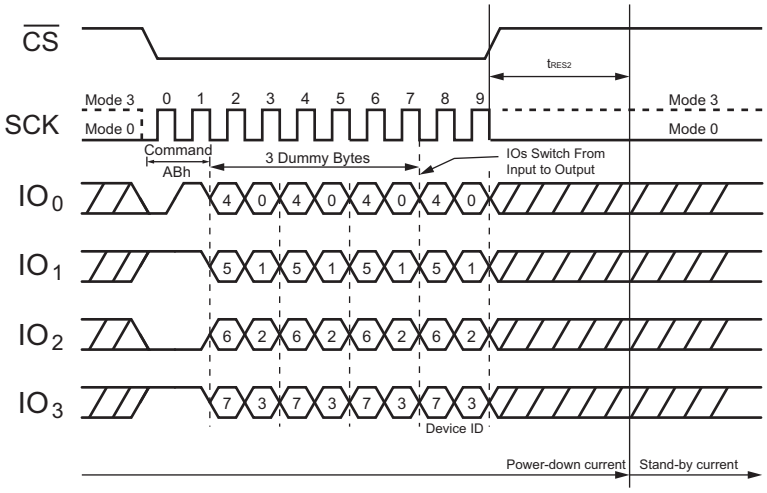


Figure 105. Release Power-Down/Read Device ID Sequence Diagram (QPI Mode)

7.6 Program and Erase Commands

7.6.1 Page Program (02h)

The Page Program command is for programming the memory. A Write Enable command must previously have been executed to set the Write Enable Latch bit before sending the Page Program command.

The Page Program command is entered by driving $\overline{CS}$ Low, followed by the command code, three-byte address and at least one data byte on SI. If the eight least significant address bits (A7 - A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose eight least significant bits (A7 - A0) are all zero). $\overline{CS}$ must be driven low for the entire duration of the sequence. The Page Program command sequence: $\overline{CS}$ goes low → sending Page Program command → three-byte address on SI → at least 1 byte of data on SI → $\overline{CS}$ goes high.

If more than 256 bytes are sent to the device, previously latched data are discarded, and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to the device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. $\overline{CS}$ must be driven high after the eighth bit of the last data byte has been latched in; otherwise, the Page Program command is not executed.

As soon as $\overline{CS}$ is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register can be read to check the value of the RDY/BSY bit. The RDY/BSY bit is 1 during the self-timed Page Program cycle; it is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

When a Page Program command is applied to a page protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits, the Individual Block Lock bits are not executed.

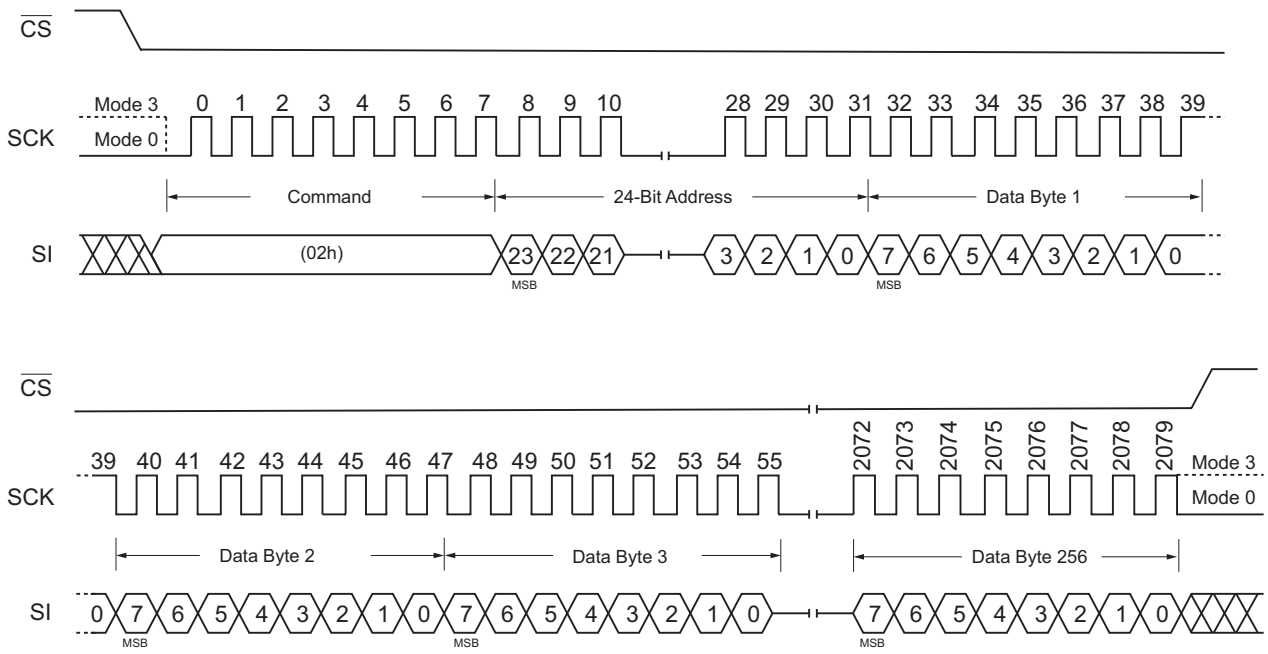


Figure 106. Page Program Sequence Diagram (SPI Mode, Three-Byte Address Mode)

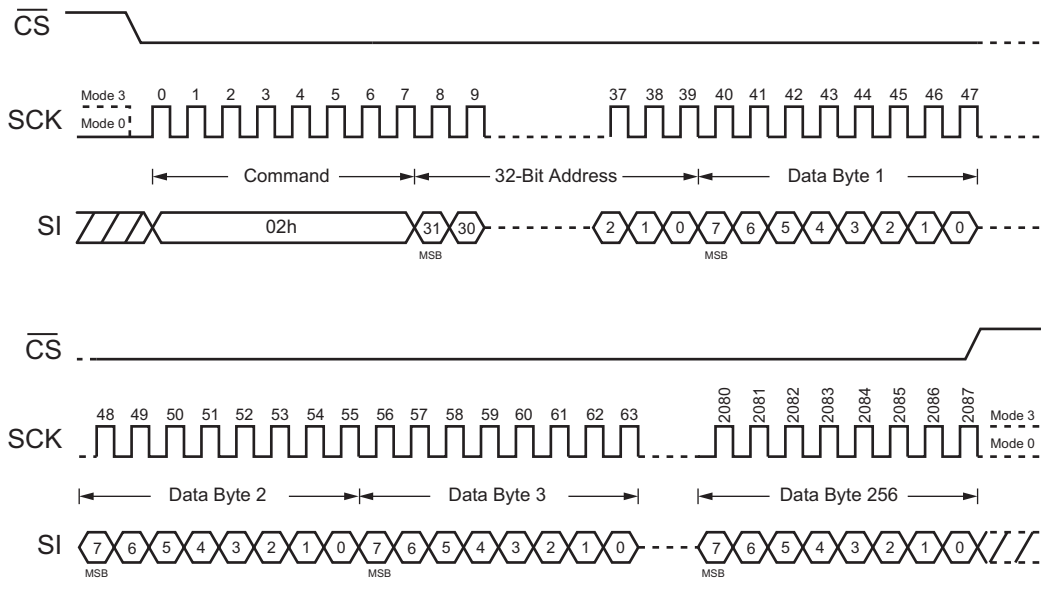


Figure 107. Page Program Sequence Diagram (SPI Mode, Four-Byte Address Mode)

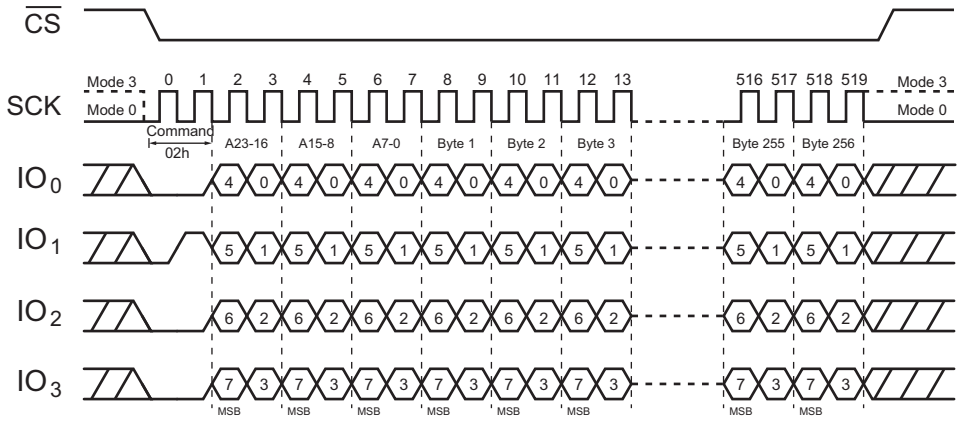


Figure 108. Page Program Sequence Diagram (QPI Mode, Three-Byte Address Mode)

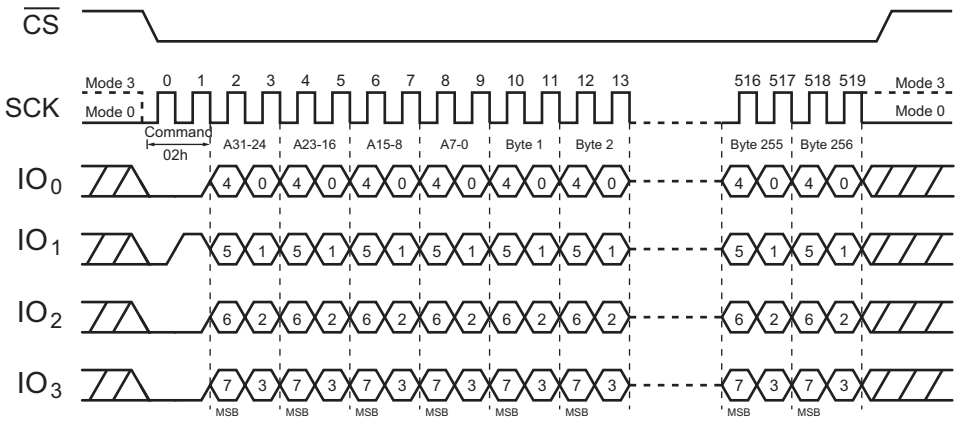


Figure 109. Page Program Sequence Diagram (QPI Mode, Four-Byte Address Mode)

7.6.2 Page Program with Four-Byte Address (12h)

The Page Program with Four-Byte Address command is similar to the Page Program command except that it requires a 32-bit address instead of a 24-bit address. No matter what address mode the device is operating in, the Page Program with Four-Byte Address command always requires a 32- bit address to access the entire 256 Mb memory.

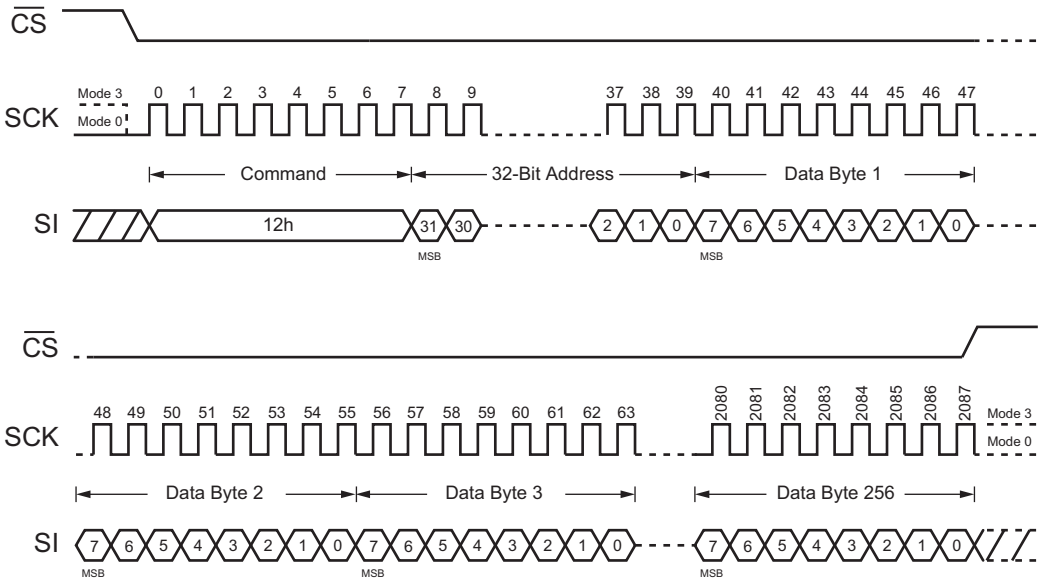


Figure 110. Page Program with Four-Byte Address (SPI Mode)

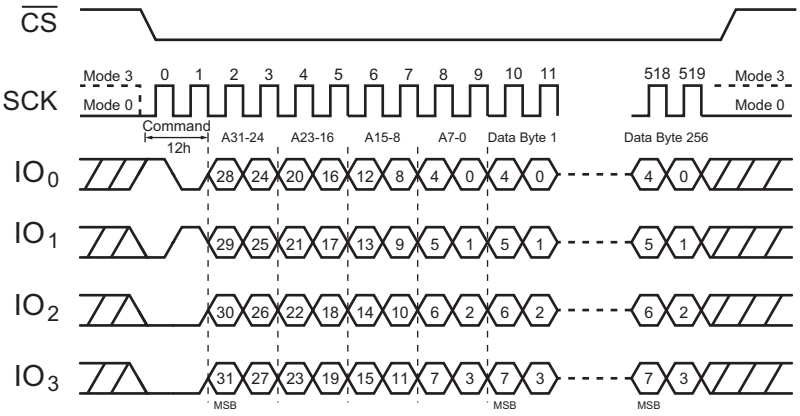


Figure 111. Page Program with Four-Byte Address (QPI Mode)

7.6.3 Quad Page Program (32h)

The Quad Page Program command is for programming the memory using for pins: IO_0, IO_1, IO_2, and IO_3. To use this command, the Quad enable in status register bit 9 must be set (QE=1). A Write Enable command must have been executed to set the Write Enable Latch bit before sending the Page Program command.This command is entered by driving $\overline{CS}$ low, followed by the command code 32h, three address bytes, and at least one data byte on the I/O pins.The Quad Enable bit (QE) of Status Register must be set to enable.

The command sequence is shown in Figure 112 and Figure 113. If more than 256 bytes are sent to the device, previously latched data are discarded, and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If fewer than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. $\overline{CS}$ must be driven high after the eighth bit of the last data byte has been latched in; otherwise, the Quad Page Program command is not executed.

As soon as $\overline{CS}$ is driven high, the self-timed Quad Page Program cycle (whose duration is t_{PP}) is initiated. While the Quad Page Program cycle is in progress, the Status Register can be read to check the value of the RDY/BSY bit. The RDY/BSY bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.A Quad Page Program command applied to a page that is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

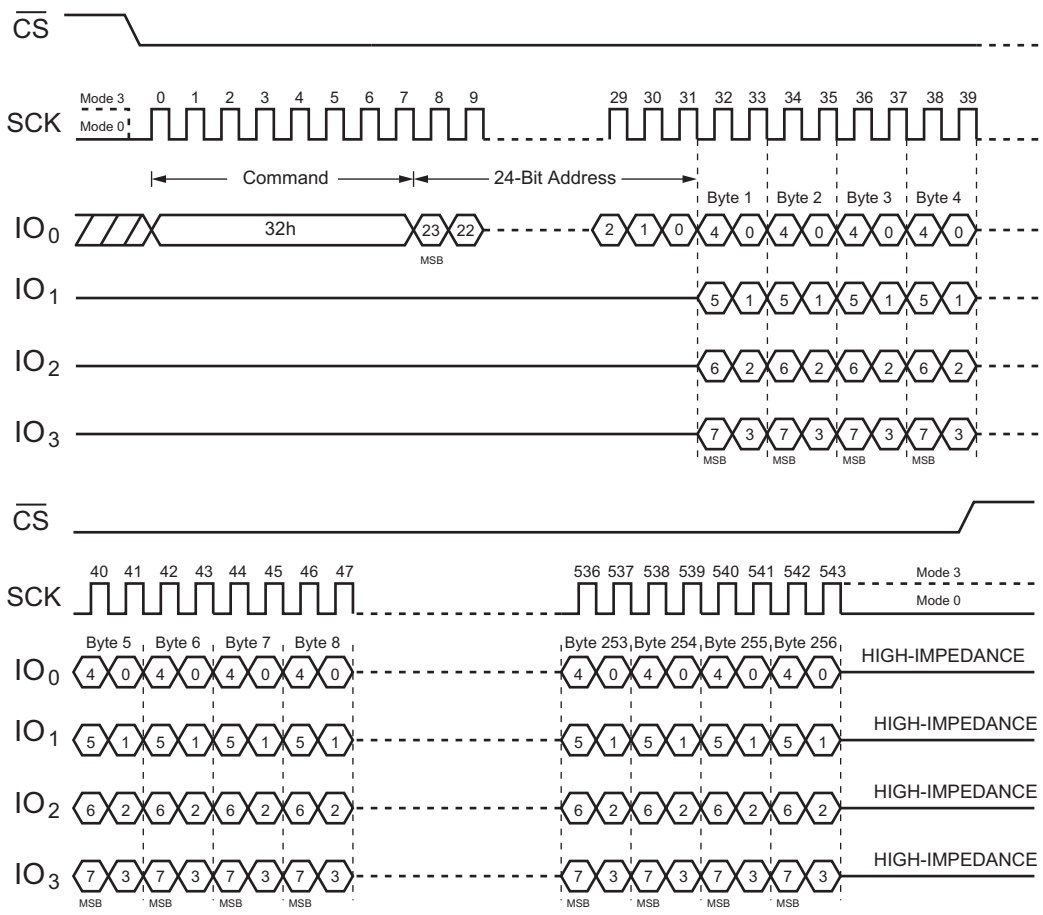


Figure 112. Quad Page Program Sequence Diagram (SPI Mode only, Three-Byte Address Mode)

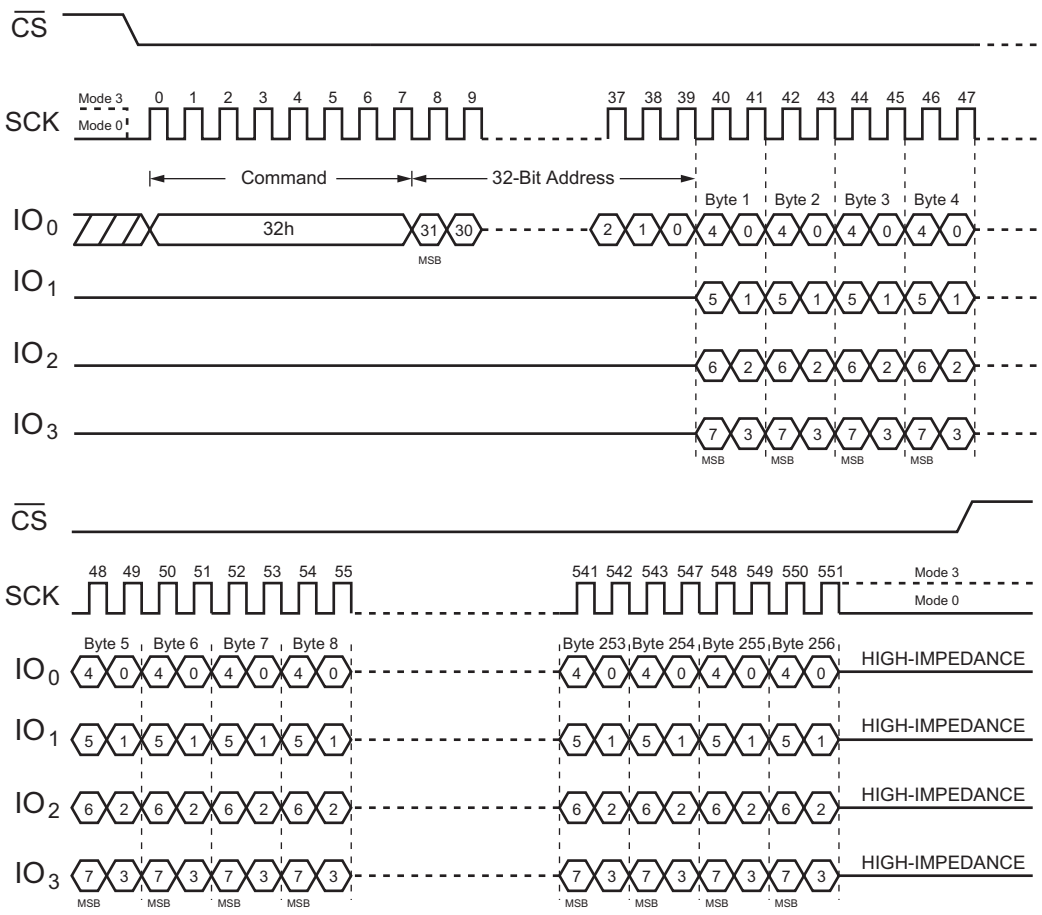


Figure 113. Quad Page Program Sequence Diagram (SPI Mode only, Four-Byte Address Mode)

7.6.4 Quad Input Page Program with Four-Byte Address (34h)

The Quad Input Page Program with Four-Byte Address command is similar to the Quad Input Page Program command, except that it requires a 32-bit address instead of a 24-bit address. No matter what address mode the device is operating in, the Quad Input Page Program with Four-Byte Address command always requires a 32-bit address to access the entire 256 Mb memory.The Quad Enable bit (QE) of Status Register must be set to enable.

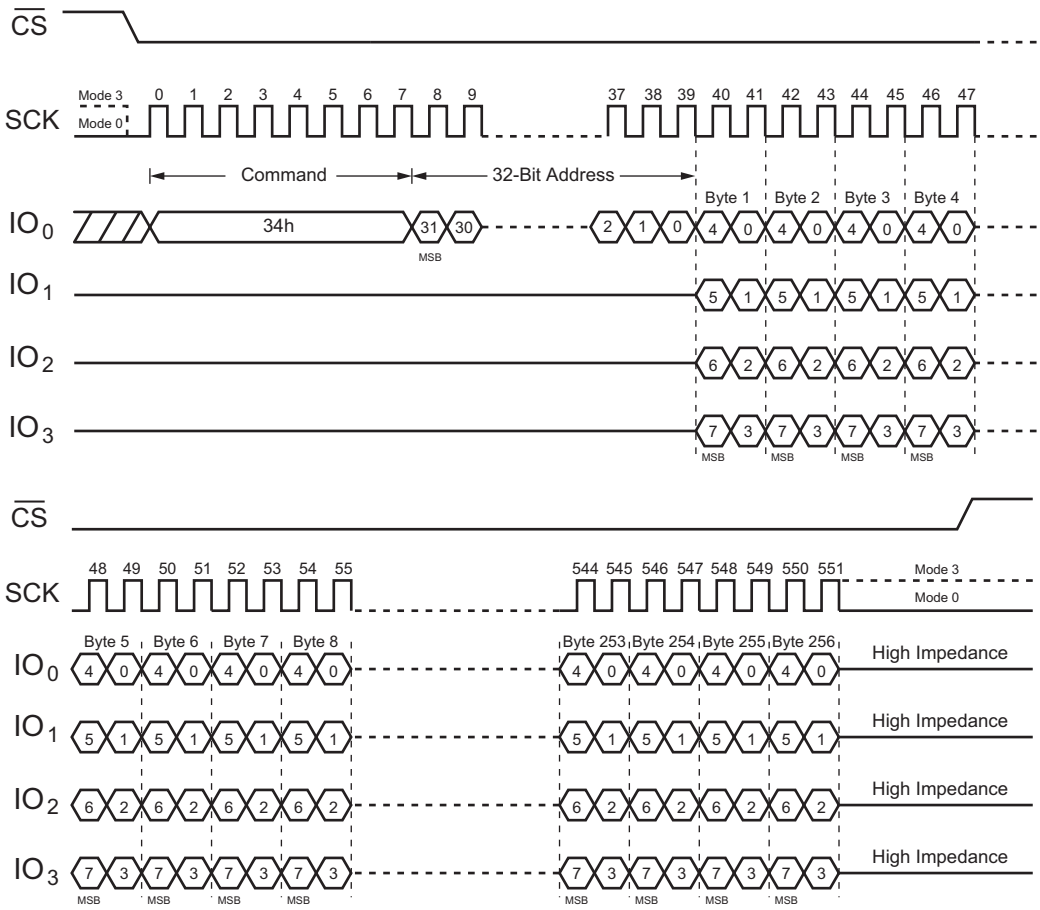


Figure 114. Quad Page Program with Four-Byte Address Sequence Diagram (SPI Mode only)

7.6.5 4 kB Block Erase (20h)

The 4 kB Block Erase command is for erasing the all data of the chosen block. A Write Enable command must previously have been executed to set the Write Enable Latch bit. The 4 kB Block Erase command is entered by driving $\overline{CS}$ low, followed by the command code, and three-byte address on the SI pin. Any address inside the block is a valid address for the 4 kB Block Erase command. $\overline{CS}$ must be driven low for the entire duration of the sequence.

The 4 kB Block Erase command sequence: $\overline{CS}$ goes low → sending 4 kB Block Erase command → three-/four-byte address on SI → $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the last address byte has been latched in; otherwise, the 4 kB Block Erase command is not executed. As soon as $\overline{CS}$ is driven high, the self-timed 4 kB Block Erase cycle (whose duration is t_{SE}) is initiated. While the 4 kB Block Erase cycle is in progress, the Status Register can be read to check the value of the RDY/BSY bit. The RDY/BSY bit is 1 during the self-timed 4 kB Block Erase cycle; it is 0 when completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 4 kB Block Erase command applied to a block that is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

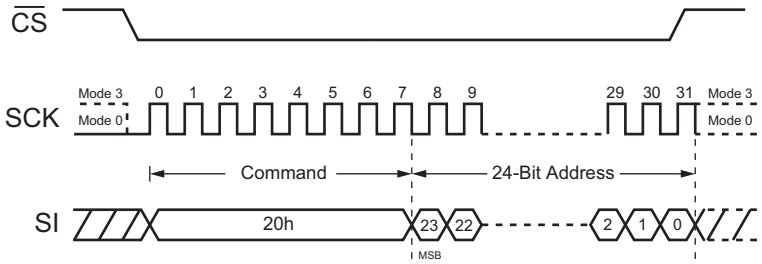


Figure 115. 4 kB Block Erase Sequence Diagram (SPI Mode, Three-Byte Address Mode)

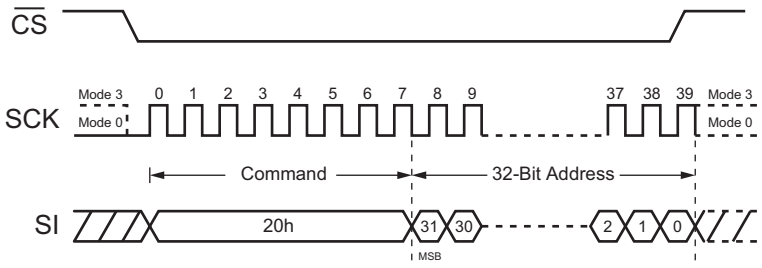


Figure 116. 4 kB Block Erase Sequence Diagram (SPI Mode, Four-Byte Address Mode)

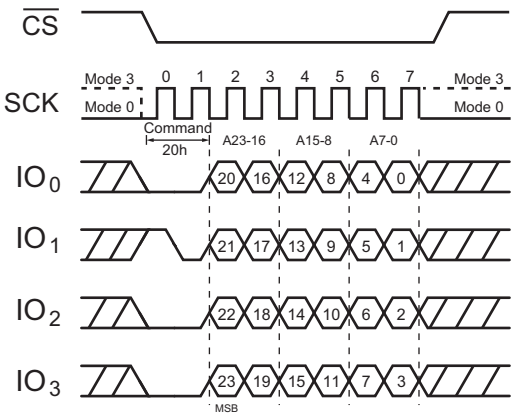


Figure 117. 4 kB Block Erase Sequence Diagram (QPI Mode, Three-Byte Address Mode)

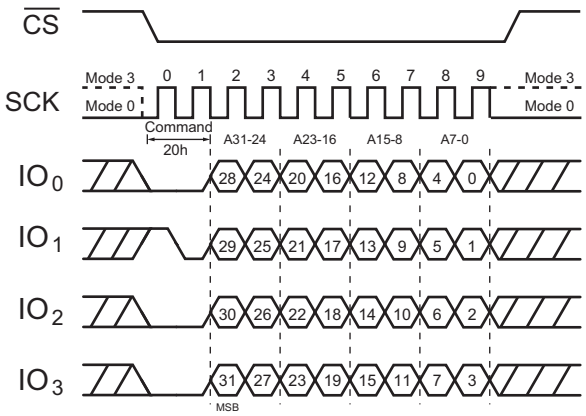


Figure 118. 4 kB Block Erase Sequence Diagram (QPI Mode, Four-Byte Address Mode)

7.6.6 4 kB Block Erase with Four-Byte Address (21h)

The 4 kB Block Erase with Four-Byte Address command is similar to the 4 kB Block Erase command, except that it requires a 32-bit address instead of a 24-bit address. No matter what address mode the device is operating in, the 4 kB Block Erase with Four-Byte Address command always requires a 32-bit address to access the entire 256-Mb memory.

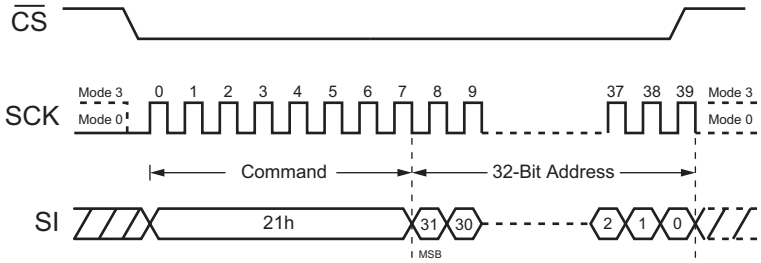


Figure 119. 4 kB Block Erase with Four-Byte Address (SPI Mode)

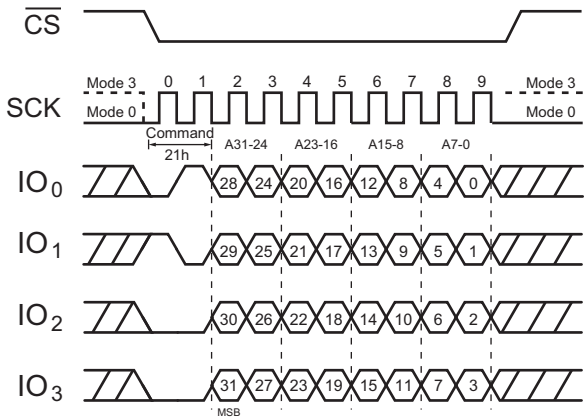


Figure 120. 4 kB Block Erase with Four-Byte Address (QPI Mode)

7.6.7 32-kB Block Erase (52h)

The 32-kB Block Erase command is for erasing all data of a chosen block. A Write Enable command must have been previously executed to set the WEL bit. The 32-kB Block Erase command is entered by driving $\overline{CS}$ low, followed by the command code, and three- or four-byte address on SI. Any address inside the block is a valid address for the 32-kB Block Erase command. $\overline{CS}$ must be driven low for the entire duration of the sequence.

The 32-kB Block Erase command sequence is: $\overline{CS}$ goes low → sending 32-kB Block Erase command → three-/four-byte address on SI → $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the last address byte has been latched in; otherwise, the 32-kB Block Erase command is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Block Erase cycle (duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the RDY/BSY bit. The RDY/BSY bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32-kB Block Erase command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

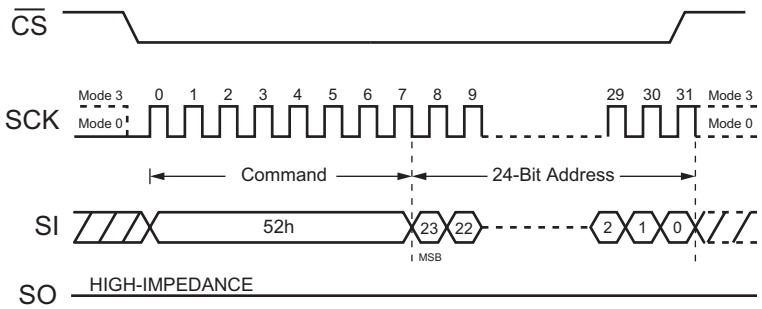


Figure 121. 32-kB Block Erase Sequence Diagram (SPI Mode, Three-Byte Address Mode)

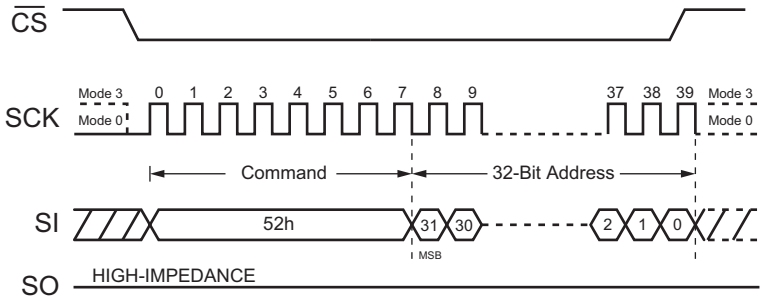


Figure 122. 32-kB Block Erase Sequence Diagram (SPI Mode, Four-Byte Address Mode)

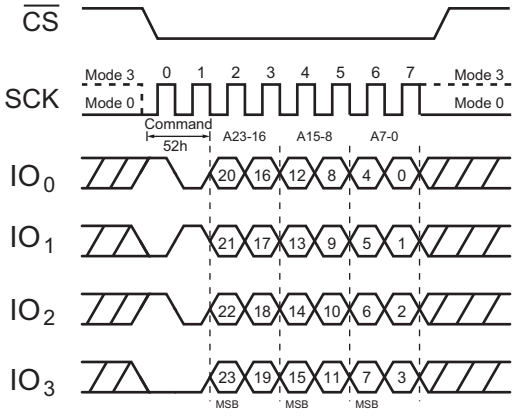


Figure 123. 32-kB Block Erase Sequence Diagram (QPI Mode, Three-Byte Address Mode)

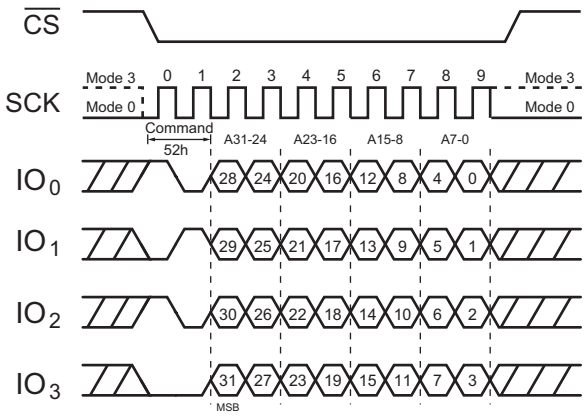


Figure 124. 32-kB Block Erase Sequence Diagram (QPI Mode, Four-Byte Address Mode)

7.6.8 32-kB Block Erase with Four-Byte Address (5Ch)

The 32-kB Block Erase with Four-Byte Address command is similar to the 32-kB Block Erase command, except that it requires a 32-bit address instead of a 24-bit address. No matter what address mode the device is operating in, the 32-kB Block Erase with Four-Byte Address command always requires a 32-bit address to access the entire 256-Mb memory.

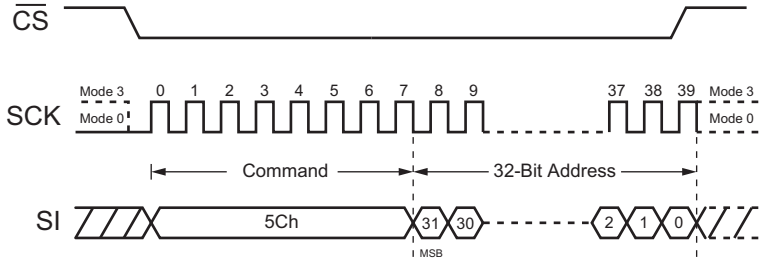


Figure 125. 32-kB Block Erase with Four-Byte Address (SPI Mode)

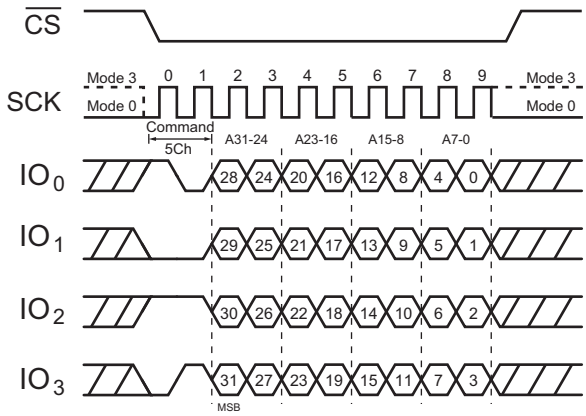


Figure 126. 32-kB Block Erase with Four-Byte Address (QPI Mode)

7.6.9 64-kB Block Erase (D8h)

The 64-kB Block Erase command is for erasing the all data of the chosen block. A Write Enable command must previously have been executed to set the WEL bit. The 64-kB Block Erase command is entered by driving $\overline{CS}$ low, followed by the command code, and three-/four-byte address on SI. Any address inside the block is a valid address for the 64-kB Block Erase command. $\overline{CS}$ must be driven low for the entire duration of the sequence.

The 64-kB Block Erase command sequence is: $\overline{CS}$ goes low, sending 64-kB Block Erase command 3-byte/4-byte address on SI, $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the last address byte has been latched in; otherwise, the 64-kB Block Erase command is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Block Erase cycle (duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the RDY/BSY bit. The RDY/BSY bit is 1 during the self-timed Block Erase cycle; it is 0 when completed. At some unspecified time before the cycle is completed, the WEL bit is reset. A 64-kB Block Erase command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

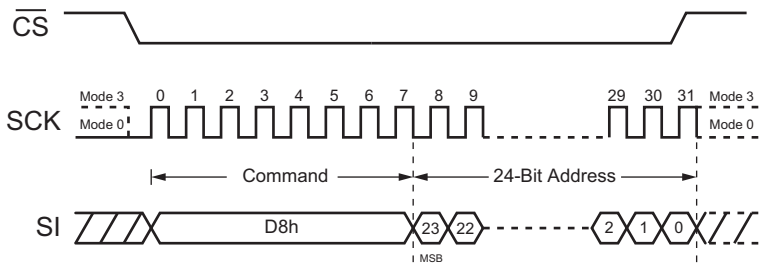


Figure 127. 64-kB Block Erase Sequence Diagram (SPI Mode, Three-Byte Address Mode)

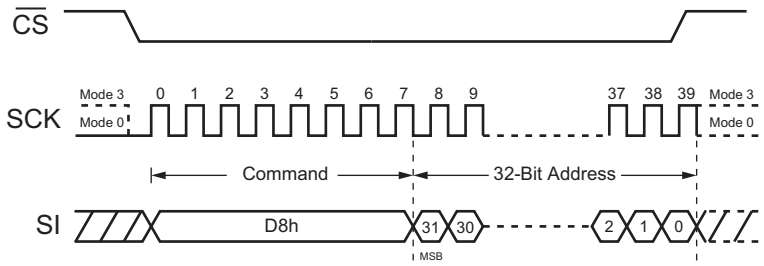


Figure 128. 64-kB Block Erase Sequence Diagram (SPI Mode, Four-Byte Address Mode)

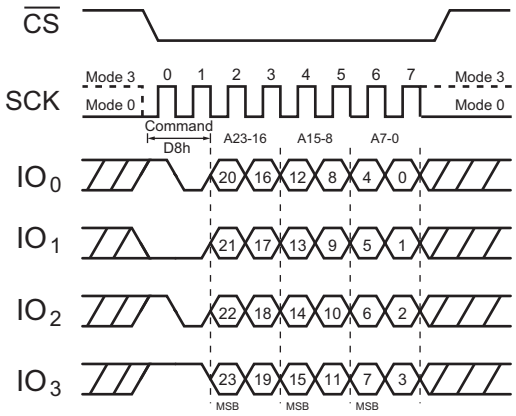


Figure 129. 64-kB Block Erase Sequence Diagram (QPI Mode, Three-Byte Address Mode)

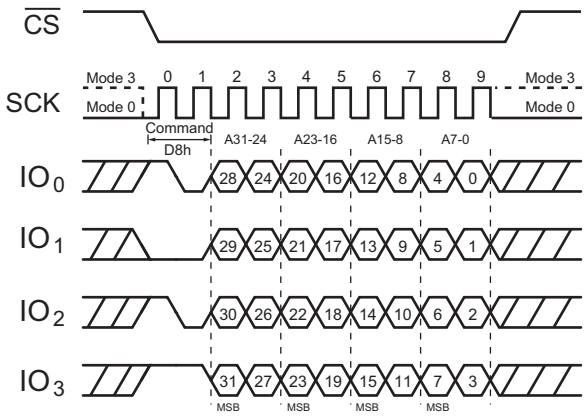


Figure 130. 64-kB Block Erase Sequence Diagram (QPI Mode, Four-Byte Address Mode)

7.6.10 64-kB Block Erase with Four-Byte Address (DCh)

The 64-kB Block Erase with Four-Byte Address command is similar to the 64-kB Block Erase command, except that it requires a 32-bit address instead of a 24-bit address. No matter what address mode the device is operating in, the 64-kB Block Erase with Four-Byte Address command always requires a 32-bit address to access the entire 256 Mb memory.

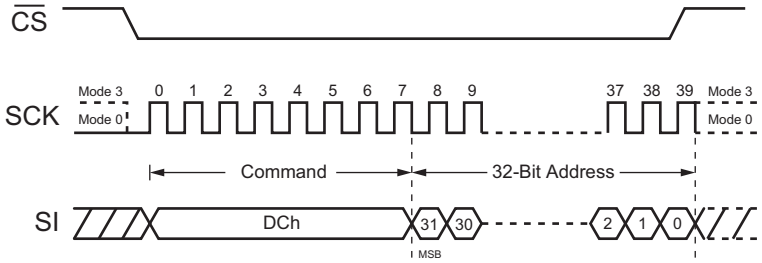


Figure 131. 64-kB Block Erase with Four-Byte Address (SPI Mode)

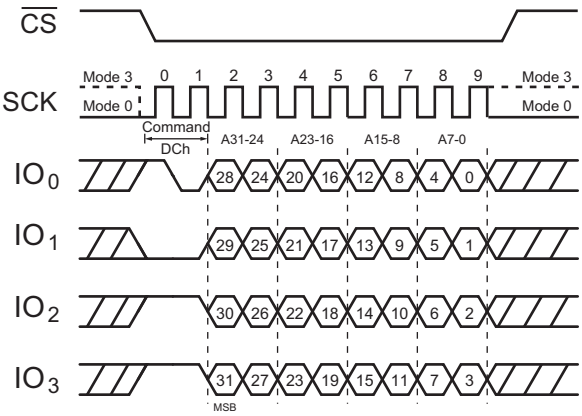


Figure 132. 64-kB Block Erase with Four-Byte Address (QPI Mode)

7.6.11 Chip Erase (60/C7h)

The Chip Erase command sets all memory within the device to the erased state of all 1s (FFh). A Write Enable command must be executed before the device accepts the Chip Erase command (Status Register bit WEL must equal 1). The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code C7h or 60h. The Chip Erase command sequence is shown in Figure 133.

The $\overline{CS}$ pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase command is not executed. After $\overline{CS}$ is driven high, the self-timed Chip Erase command commences for a time duration of t_{CE}. While the Chip Erase cycle is in progress, the Read Status Register command can still be accessed to check the status of the RDY/BSY bit.

The RDY/BSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other commands again. After the Chip Erase cycle has finished the WEL bit in the Status Register is cleared to 0. The Chip Erase command is executed only if all Block Protect (BP2, BP1, and BP0) bits are 0. The Chip Erase command is ignored if one or more blocks are protected.

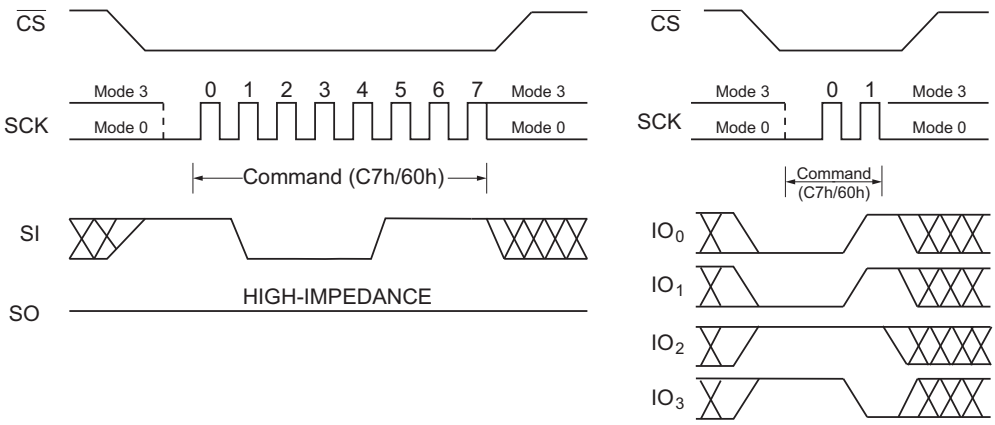


Figure 133. Chip Erase Sequence Diagram (SPI Mode left, QPI Mode right)

7.6.12 Erase / Program Suspend (75h)

The Erase/Program Suspend command allows the system to interrupt a block erase operation or a program operation.

After a program operation has entered the suspended state, the memory array can be read except for the page being programmed. After an erase operation has entered the suspended state, the memory array can be read or programmed except for the block being erased. During a suspend state of any type, erase operations are not allowed. Write status register operation cannot be suspended.

The Erase/Program Suspend command sequence is shown in Figure 134 and Figure 135.

Table 37. Readable or Erasable Area of Memory While a Program Operation is Suspended

Suspended Operation	Readable Region of Memory Array
Page Program	All but the Page being programmed
Page Program with Four-Byte Address	All but the Page being programmed
Quad Page Program	All but the Page being programmed
Quad Page Program with Four-Byte Address	All but the Page being programmed

Table 38. Readable or Programmable Area of Memory While an Erase Operation is Suspended

Suspended Operation	Readable or Programmable Region of Memory Array
Block Erase (4-kB)	All but the Block being erased
Block Erase with Four-Byte Address (4-kB)	All but the Block being erased
Block Erase (32-kB)	All but the 32-kB Block being erased
Block Erase with Four-Byte Address (32-kB)	All but the 32-kB Block being erased
Block Erase (64-kB)	All but the 64-kB Block being erased
Block Erase with Four-Byte Address (64-kB)	All but the 64-kB Block being erased

When the Serial NOR Flash receives the Suspend command, there is a latency of t_{PSL} or t_{ESL} before the Write Enable Latch (WEL) bit clears to 0 and the SUS2 or SUS1 bits are set to 1. After this, the device is ready to accept one of the commands listed in Table 39. See Section 8.7, AC Electrical Characteristics, for t_{PSL}/t_{ESL} timings. Table 40 lists the commands for which the t_{PSL} and t_{ESL} latencies do no apply. For example: 05h, 66h, and 99h can be issued at any time after the Suspend command.

Status Register 2 bit 7 (SUS2) and bit 2 (SUS1) can be read to check the suspend status. The SUS2 (Program Suspend Bit) sets to 1 when a program operation is suspended. The SUS1 (Erase Suspend Bit) sets to 1 when a program or an erase operation is suspended. The SUS2 or SUS1 clears to 0 when the program or erase command is resumed.

Table 39. Acceptable Commands During Program/Erase Suspend after t_{PSL}/t_{ESL}

Command Name	Opcode	Program Suspend	Erase Suspend
Write Enable	06h	*	*
Write Disable	04h	*	*
Enter 4-Byte Address Mode	B7h	*	*
Exit 4-Byte Address Mode	E9h	*	*
Enter QPI Mode	38h	*	*
Exit QPI Mode	FFh	*	*
Read Extended Address Register	C8h	*	*
Read Data	03h	*	*
Read Data with 4-Byte Address	13h	*	*
Fast Read	0Bh	*	*
Fast Read with 4-Byte Address	0Ch	*	*
Dual Output Fast Read	3Bh	*	*
Fast Read Dual Output with 4-Byte Address	3Ch	*	*
Quad Output Fast Read	6Bh	*	*
Fast Read Quad Output with 4-Byte Address	6Ch	*	*
Dual I/O Fast Read	BBh	*	*
Fast Read Dual I/O with 4-Byte Address	BCh	*	*
Quad I/O Fast Read	EBh	*	*
DTR Fast Read Quad I/O	EDh	*	*
Fast Read Quad I/O with 4-Byte Address	ECh	*	*
DTR Quad I/O Fast Read with 4-Byte Address	EEh	*	*
Set Burst with Wrap	77h	*	*
Set Read Parameters	C0h	*	*
Read Mftr./Device ID	90h	*	*
Dual IO Read Mftr./Device ID	92h	*	*
Quad IO Read Mftr./Device ID	94h	*	*
Read JEDEC ID	9Fh	*	*
Read Unique ID Number	4Bh	*	*
Release Power-down/Device ID	ABh	*	*
Read Security Registers	48h	*	*
Read SFDP	5Ah	*	*
Page Program	02h		*
Page Program with 4-Byte Address	12h		*
Quad Page Program	32h		*
Quad Input Page Program with 4-Byte Address	34h		*
Program/Erase Resume	7Ah	*	*
Read Block Lock	3Dh	*	*

Table 40. Acceptable Commands During Suspend (t_{PSL}/t_{ESL} not required)

Command Name	Opcode	Program Suspend	Erase Suspend
Read Status Register 1	05h	*	*
Read Status Register 2	35h	*	*
Read Status Register 3	15h	*	*
Enable Reset	66h	*	*
Reset Device	99h	*	*

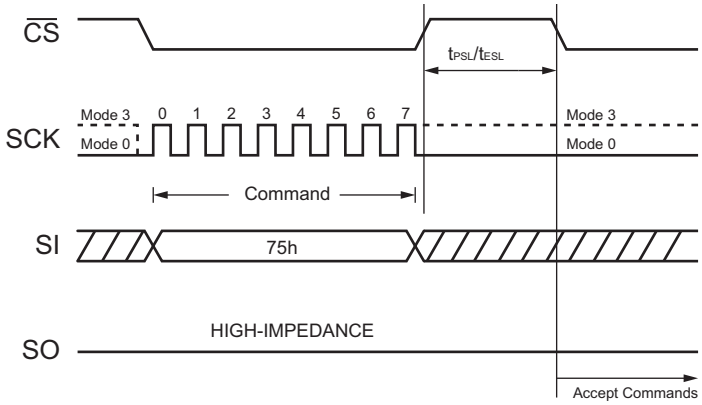


Figure 134. Erase/Program Suspend Command Sequence (SPI Mode)

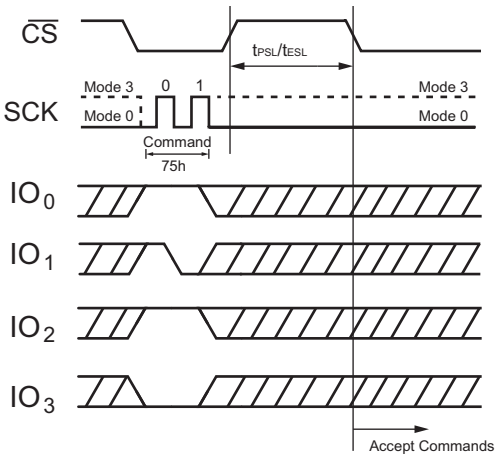


Figure 135. Erase/Program Suspend Command Sequence (QPI Mode)

7.6.13 Erase / Program Resume (7Ah)

The Erase/Program Resume command 7Ah must be written to resume the Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume command 7Ah is accepted by the device only if the SUS bit in the Status Register equals to 1 and the RDY/BSY bit equals to 0.

After the Resume command is issued the SUS bit is cleared from 1 to 0 immediately, the RDY/BSY bit is set from 0 to 1 within 200 ns and the Block completes the erase operation or the page completes the program operation. If the SUS bit equals to 0 or the RDY/BSY bit equals to 1, the Resume command 7Ah is ignored by the device.

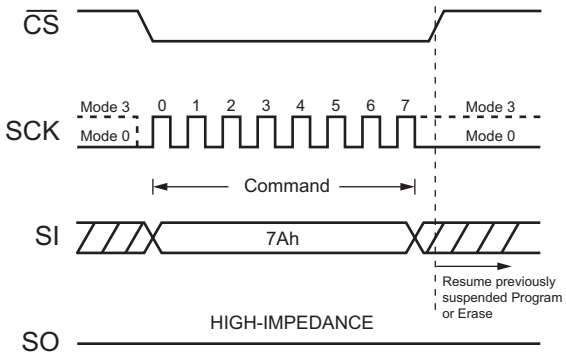


Figure 136. Erase/Program Resume Command Sequence (SPI Mode)

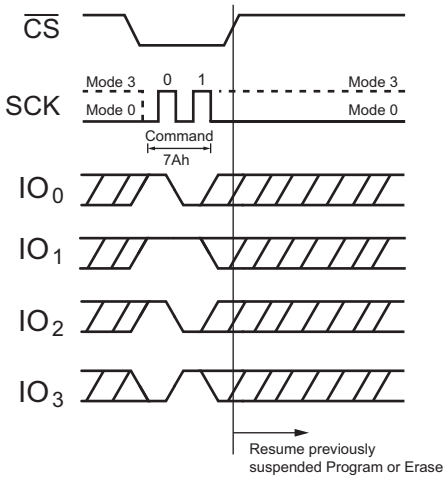


Figure 137. Erase/Program Resume Command Sequence (QPI Mode)

7.7 Individual Block Memory Protection Commands

7.7.1 Read Block Lock (3Dh)

The Read Block Lock (3Dh) command reads the status of the Individual Block Lock bit of a block. The Read Block Lock Status command returns 00h if the Individual Block Lock bit is 0, indicating write-protection is disabled. The Read Block Lock command returns FFh if the Individual Block Lock bit is 1, indicating write-protection is enabled.

The Individual Block Lock bits are volatile bits for quickly and easily enabling, or disabling, write-protection to blocks. A Individual Block Lock bit is assigned to each 4-kB Block in the bottom and top 64 kB of memory and to each 64-kB block in the rest of the memory. When an Individual Block Lock bit is 1, the associated block is write-protected, preventing any program or erase operation on the block. All Individual Block Lock bits default to 1 after power-on or reset.

To read out the Individual Block Lock bit value of a specific block, issue the Read Block Lock (3Dh) command by driving $\overline{CS}$ low, shifting the command code 3Dh into the Data Input (SI or IO_0-IO_3) pin on the rising edge of SCK, followed by a 24/32-bit address. The Individual Block Lock bit value is shifted out on the SO or IO_0-IO_3 pin at the falling edge of SCK, with the most significant bit (MSB) first, then driving $\overline{CS}$ high. Note that if $\overline{CS}$ is not driven high, the Individual Block Lock bit value is repeatedly output.

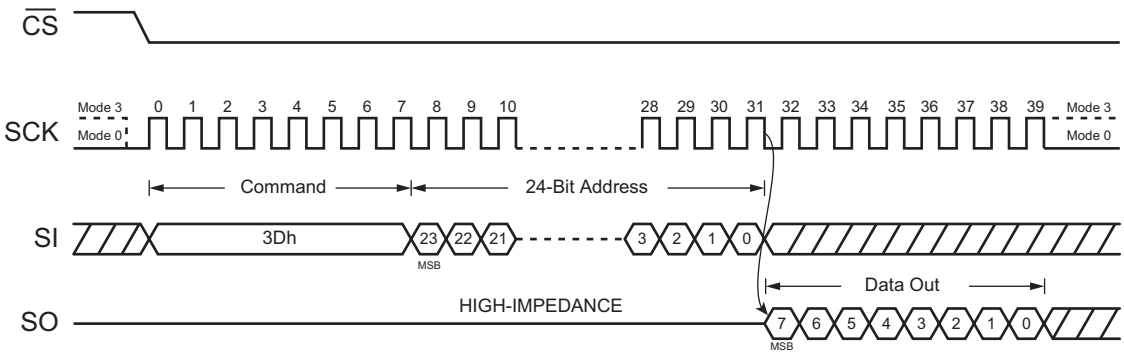


Figure 138. Read Block Lock (SPI Mode, Three-Byte Address Mode)

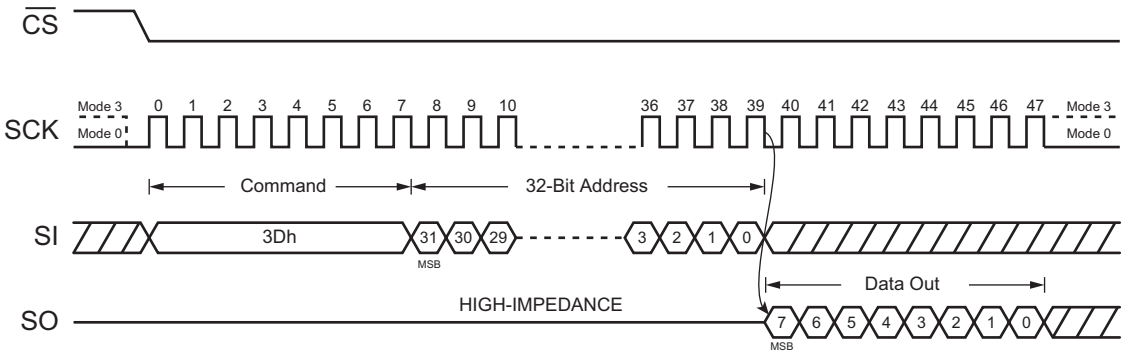


Figure 139. Read Block Lock (SPI Mode, Four-Byte Address Mode)

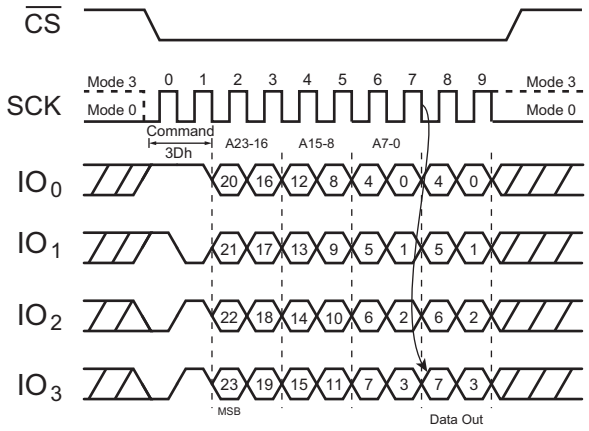


Figure 140. Read Block Lock (QPI Mode, Three-Byte Address Mode)

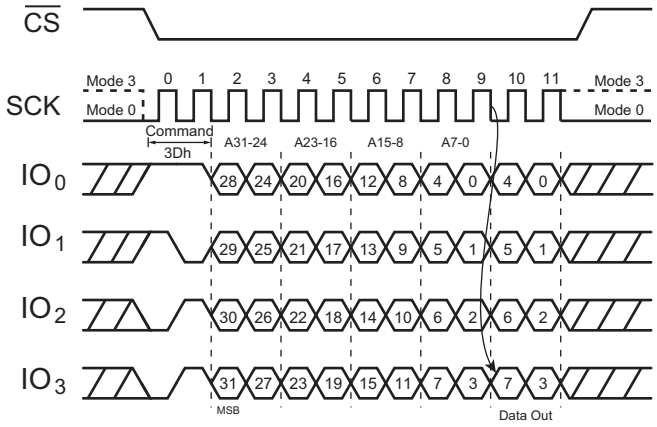


Figure 141. Read Block Lock (QPI Mode, Four-Byte Address Mode)

7.7.2 Individual Block Lock (36h)

The Individual Block Lock (36h) command can individually set Individual Block Lock bits to 1. When an Individual Block Lock bit is 1, the associated block is write-protected, preventing any program or erase operation on the block. All Individual Block Lock bits default to 1 after power-on or reset.

A Write Enable (06h) command must be executed to set the WEL bit before sending the Individual Block Lock command.

To set an Individual Block Lock bit to 1, issue the Individual Block Lock (36h) command by driving $\overline{CS}$ low, shifting the command code 36h into the Data Input (SI or IO_0-IO_3) pin on the rising edge of SCK, followed by a 24/32-bit address, then driving $\overline{CS}$ high.

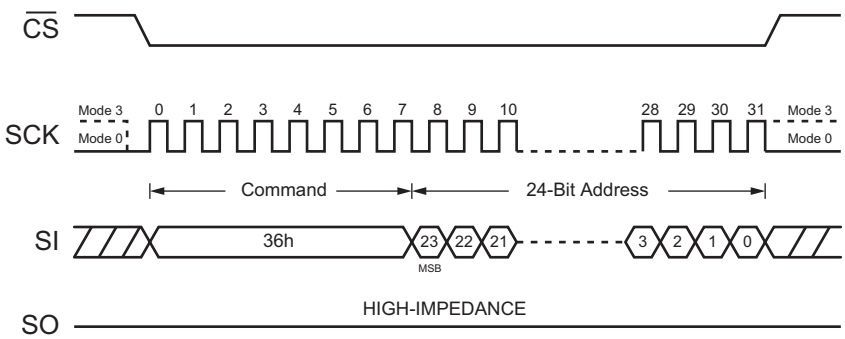


Figure 142. Individual Block Lock (SPI Mode, Three-Byte Address Mode)

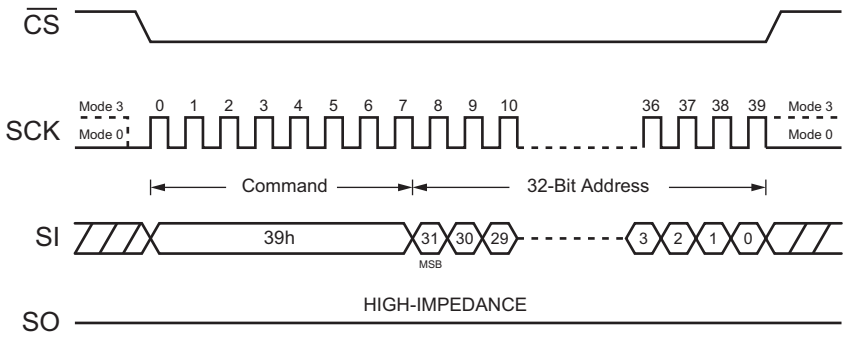


Figure 143. Individual Block Lock (SPI Mode, Four-Byte Address Mode)

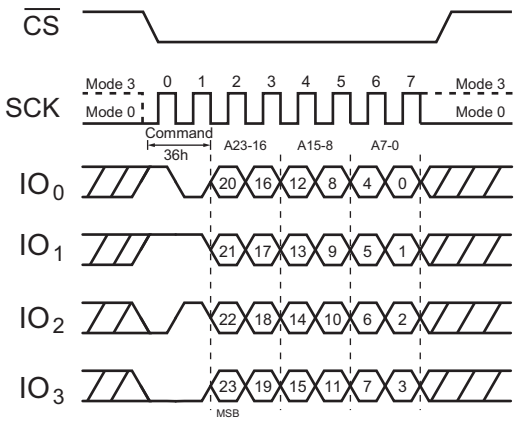


Figure 144. Individual Block Lock (QPI Mode, Three-Byte Address Mode)

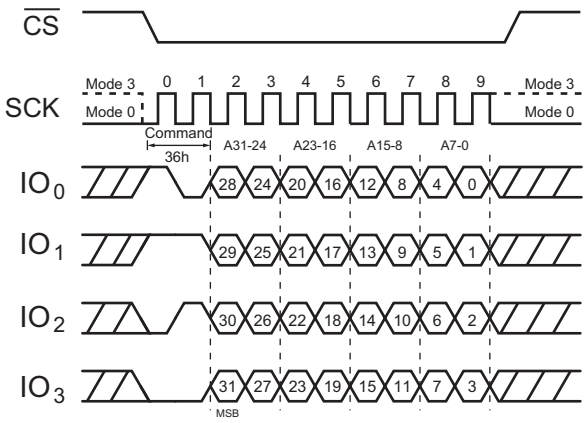


Figure 145. Individual Block Lock (QPI Mode, Four-Byte Address Mode)

7.7.3 Individual Block Unlock (39h)

The Individual Block Unlock (39h) command can individually set Individual Block Lock bits to 0.

A Write Enable (06h) command must be executed to set the WEL bit before sending the Individual Protection Block Unlock command.

To set the Individual Block Lock bit to 0, issue the Individual Block Unlock (39h) command by driving $\overline{CS}$ low, shifting the command code 39h into the Data Input (SI or IO_0-IO_3) pin on the rising edge of SCK, followed by a 24/32-bit address, then driving $\overline{CS}$ high.

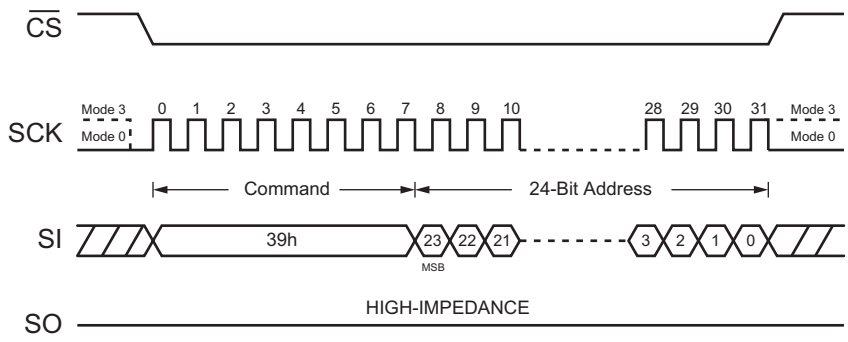


Figure 146. Individual Block Unlock (SPI Mode, Three-Byte Address Mode)

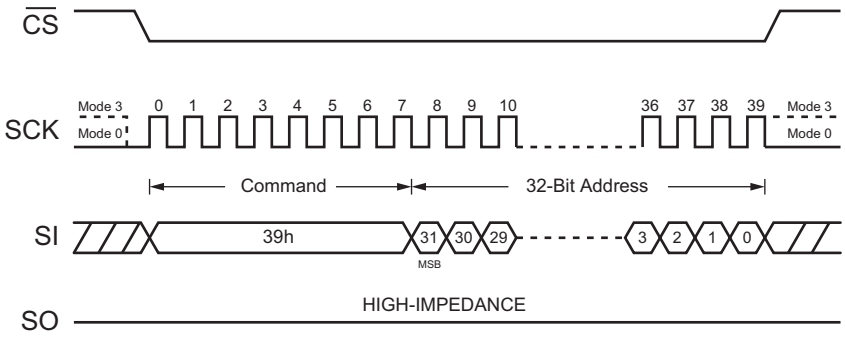


Figure 147. Individual Block Unlock (SPI Mode, Four-Byte Address Mode)

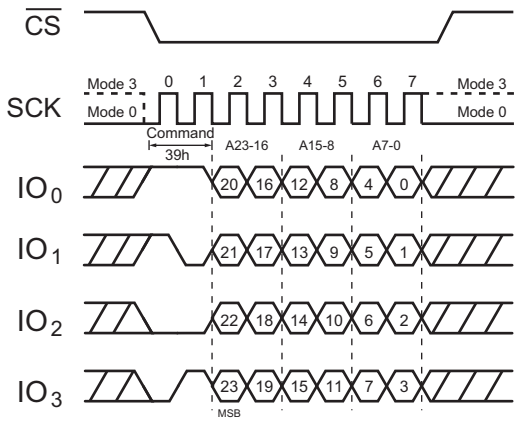


Figure 148. Individual Block Unlock (QPI Mode, Three-Byte Address Mode)

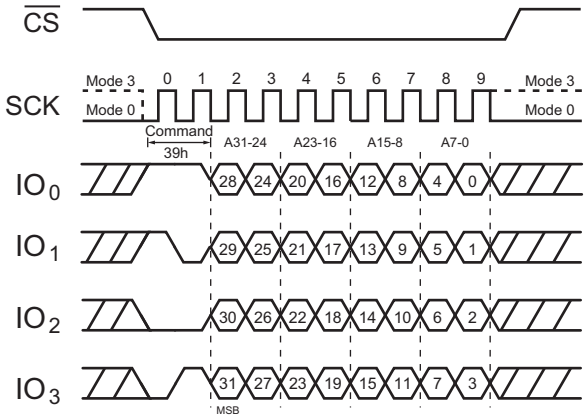


Figure 149. Individual Block Unlock (QPI Mode, Four-Byte Address Mode)

7.7.4 Global Block Lock (7Eh)

The Global Block Lock(7Eh) command can set all Individual Block Lock bits to 1.

A Write Enable (06h) command must be executed to set the WEL bit before sending the Global Block Lock command.

To set all Individual Block Lock bits to 1, issue the Global Block Lock (7Eh) command by driving $\overline{CS}$ low, shifting the command code 7Eh into the Data Input (SI or IO_0-IO_3) pin on the rising edge of SCK, then driving $\overline{CS}$ high.

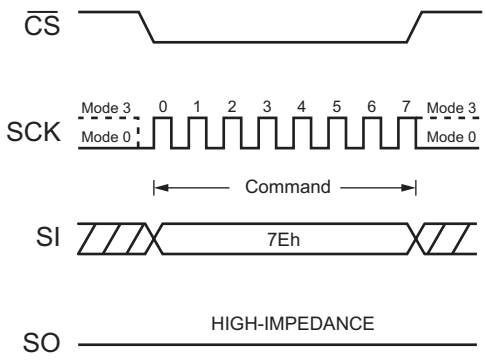


Figure 150. Global Block Lock (SPI Mode)

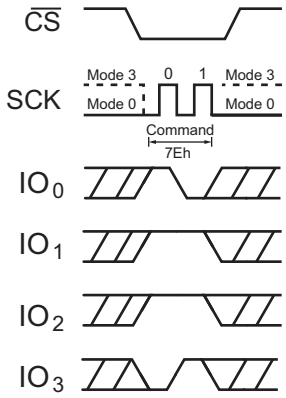


Figure 151. Global Block Lock (QPI Mode)

7.7.5 Global Block Unlock (98h)

The Global Block Unlock (98h)) command can set all Individual Block Lock bits to 0.

A Write Enable (06h) command must be executed to set the WEL bit before sending the Global Block Unlock command.

To set all Individual Block Lock bits 0, issue the Global Block Unlock (98h) command by driving $\overline{CS}$ low, shifting the command code 98h into the Data Input (SI or IO_0-IO_3) pin on the rising edge of SCK, then driving $\overline{CS}$ high.

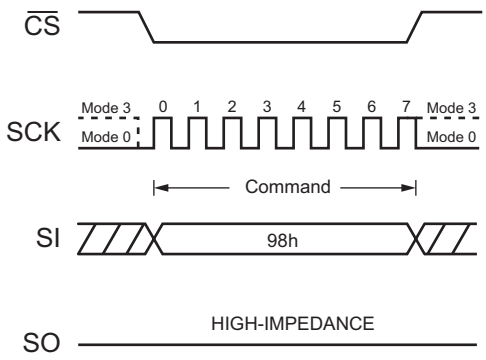


Figure 152. Global Block Unlock (SPI Mode)

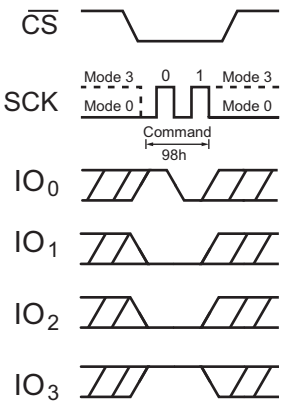


Figure 153. Global Block Unlock (QPI Mode)

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Table 41. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Range	Units
Supply Voltage	V_{CC}		-0.5 to 4	V
Voltage Applied to Any Pin	V_{IO}	Relative to Ground	-0.5 to 4	V
Transient Voltage on any Pin	V_{IOT}	<20 ns Transient Relative to Ground	-2.0 to V_{CC} + 2.0 V	V
Storage Temperature	T_{STG}		-65 to +150	°C
Electrostatic Discharge Voltage	V_{ESD}	Human Body Model [1]	-2000 to +2000	V

1. JEDEC Std JESD22-A114 (C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).

8.2 Operating Ranges

Table 42. Operating Range

PARAMETERS	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Supply Voltage	V_{CC}		2.7	3.6	V
Operating Temperature	T_A	Industrial	-40	+85	°C

8.3 Latch Up Characteristics

Table 43. Latch Up Characteristics

Parameter	Min	Max	Units
Input Voltage with Respect to V_{SS} on I/O Pins	-1.0	V_{CC} + 1.0 V	V
V_{CC} Current	-100	100	mA

8.4 Power-up and Brown-out Timing

Table 44. Power-up and Brown-out Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{VSL}	V_{CC} (min) to full operation permitted.	0.6			ms
V_{WI}	Write inhibit threshold voltage.	1.8		2.2	V
t_{VR}	V_{CC} Rise time (from 0 V to V_{CC} min)		1	6000	µs/V
t_{PWD}	V_{CC} minimum time duration below V_{PWDMAX} to guarantee reset.	300			µs
V_{PWDMAX}	V_{CC} level below which a reset is guaranteed.			0.2	V

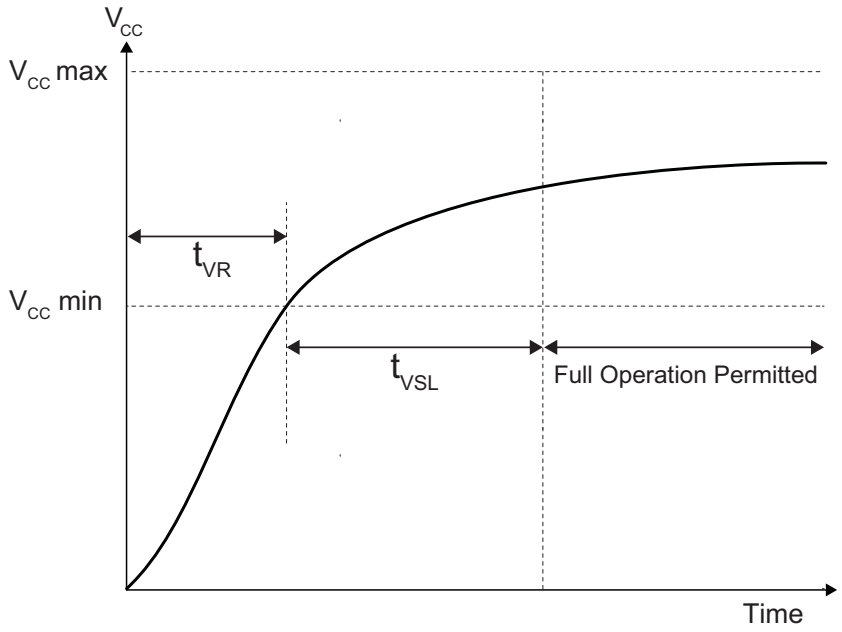


Figure 154. Power-up Timing and Voltage Levels

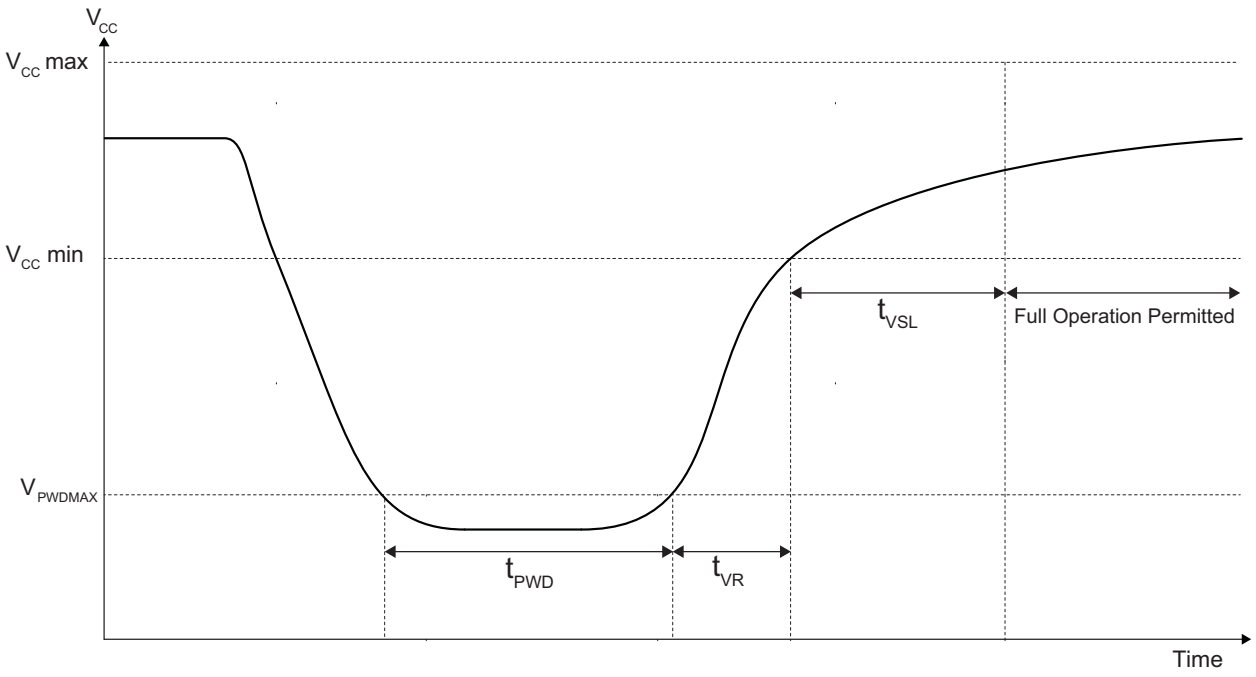


Figure 155. Power-up Timing After Brown-out

8.5 DC Electrical Characteristics

Table 45. DC Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ[1]	Max	Units
I_{LI}	Input Leakage Current				±2	µA
I_{LO}	Output Leakage Current				±2	µA
I_{CC1}	Standby Current	$\overline{CS}$ = V_{CC}, V_{IN} = V_{CC} or V_{SS}		12	50	µA
I_{CC2}	Deep Power-Down Current	$\overline{CS}$ = V_{CC}, V_{IN} = V_{CC} or V_{SS}		0.5	10	µA
I_{CC3}	Operating Current: (Read)	SCK = 0.1 V_{CC}/0.9 V_{CC} at 120 MHz, Q = Open (*1,*2,*4 I/O) SCK = 0.1 V_{CC}/0.9 V_{CC} at 80 MHz, Q = Open (*1,*2,*4 I/O)		13 11	15 13	mA
I_{CC4}	Operating Current (Page Program)	$\overline{CS}$ = V_{CC}			12	mA
I_{CC5}	Operating Current (WRSR)	$\overline{CS}$ = V_{CC}			12	mA
I_{CC6}	Operating Current (4 kB Block Erase)	$\overline{CS}$ = V_{CC}			15	mA
I_{CC7}	Operating Current (32/64 kB Block Erase)	$\overline{CS}$ = V_{CC}			15	mA
I_{CC8}	Operating Current (Chip Erase)	$\overline{CS}$ = V_{CC}			15	mA
V_{IL}	Input Low Voltage		-0.5		0.2 V_{CC}	V
V_{IH}	Input High Voltage		0.8 V_{CC}		V_{CC} +0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2			V

1. Typical values measured at 3.0 V @ +25 ºC.

8.6 AC Measurement Conditions

Table 46. AC Measurement Conditions

Symbol	Parameter	Min	Typ	Max	Unit
C_L	Load Capacitance			30	pF
t_R, t_F	Input Rise and Fall time			5	ns
V_{IN}	Input Pause Voltage	0.2 V_{CC} to 0.8 V_{CC}			V
IN	Input Timing Reference Voltage	0.5 V_{CC}			V
OUT	Output Timing Reference Voltage	0.5 V_{CC}			V

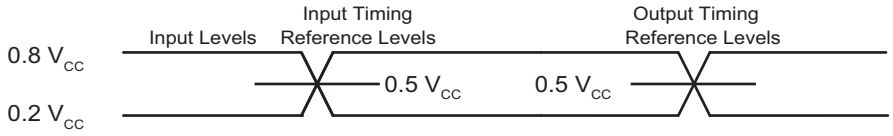


Figure 156. AC Measurement I/O Waveform

8.7 AC Electrical Characteristics

Table 47. AC Electrical Characteristics

Symbol	Parameter	Min	Typ [1]	Max	Units
Fc	Clock frequency for Read Array commands except 03h, 13h, BBh, BCh, EBh, ECh, EDh, EEh, 0Eh on 2.7 - 3.6 V power supply			133	MHz
Fc	Clock frequency for Read Array commands BBh, BCh, EBh, and ECh	See DC1/DC0 bit for SPI (Section 5.2.13) and Set Read Parameters (C0h) command for QPI (Section 7.2.16)			MHz
F_R	Clock frequency for DTR commands EDh, EEH, and 0Eh	See DC1/DC0 bit for SPI (Section 5.2.13) and Set Read Parameters (C0h) command for QPI (Section 7.2.16)			MHz
f_R	Clock frequency for Read Array commands 03h and 13h	DC		60	MHz
t_{CLH}	Serial Clock High Time	45% (1/F_C)			ns
t_{CLL}	Serial Clock Low Time	45% (1/F_C)			ns
t_{CLCH}[3]	Serial Clock Rise Time (Slew Rate)	0.1 [1]			V/ns
t_{CHCL}[3]	Serial Clock Fall Time (Slew Rate)	0.1 [1]			V/ns
t_{SLCH}	$\overline{CS}$ Active Setup Time	5			ns
t_{CHSH}	$\overline{CS}$ Active Hold Time	5			ns
t_{SHCH}	$\overline{CS}$ Not Active Setup Time	5			ns
t_{CHSL}	$\overline{CS}$ Not Active Hold Time	5			ns
t_{SHSL}	$\overline{CS}$ High Time (read/write)	22			
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	2			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{HLCH}[3]	$\overline{HOLD}$ Low Setup Time (relative to Clock)	5			ns
t_{HHCH}[3]	$\overline{HOLD}$ High Setup Time (relative to Clock)	5			ns
t_{CHHH}[3]	$\overline{HOLD}$ Low Hold Time (relative to Clock)	5			ns
t_{CHHL}[3]	$\overline{HOLD}$ High Hold Time (relative to Clock)	5			ns
t_{HHQX}[3]	$\overline{HOLD}$ Low To Low-Z Output			6	ns
t_{HLQZ}[3]	$\overline{HOLD}$ Low To High-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid			7	ns
t_{WHSL}	Write Protect Setup Time Before $\overline{CS}$ Low	20			ns
t_{SHWL}	Write Protect Hold Time After $\overline{CS}$ High	100			ns
t_{DP}	$\overline{CS}$ High To Deep Power-Down Mode			3	µs

Table 47. AC Electrical Characteristics *(continued)*

Symbol	Parameter	Min	Typ [1]	Max	Units
t_{RES1}	$\overline{CS}$ High To Standby Mode Without Electronic Signature Read			30	µs
t_{RES2}	$\overline{CS}$ High To Standby Mode With Electronic Signature Read			30	µs
t_{ESL}	Erase Suspend Latency			30	µs
t_{PSL}	Program Suspend Latency			20	µs
t_{PRS}	Latency Between Program Resume to next Suspend	20			µs
t_{ERS}	Latency Between Erase Resume to next Suspend	20			µs
t_{RST}	$\overline{CS}$ High to Next command After Reset in standby/read			1	µs
	$\overline{CS}$ High to Next command After Reset in program/Deep Power-Down			60	µs
	$\overline{CS}$ High to Next command After Reset in erase			10	ms
	$\overline{CS}$ High to Next command After Reset in write SR		Align to t_W		ms
t_W	Write Status Register Cycle Time		5	30	ms
t_{BP1}	Byte Program Time (First Byte)		50	150	µs
t_{BP2} [4]	Additional Byte Program Time (After First Byte)		1.4	8	µs
t_{PP} [2]	Page Programming Time		0.4	2.4	ms
t_{SE} [2]	Block Erase Time (4 kBytes)		45	160	ms
t_{BE} [2]	Block Erase Time (32 kBytes/64 kBytes)		90/150	300/450	ms
t_{CE}	Chip Erase Time		80	120	sec

1. Tested with clock frequency lower than 50 MHz.
2. Maximum is worst case measurement at cycling conditions after 100k cycles.
3. Not 100% tested (value guaranteed by design and characterization).
4. The time to program N bytes can be calculated as follows: $t_{BP1} + (N - 1) * t_{BP2}$.

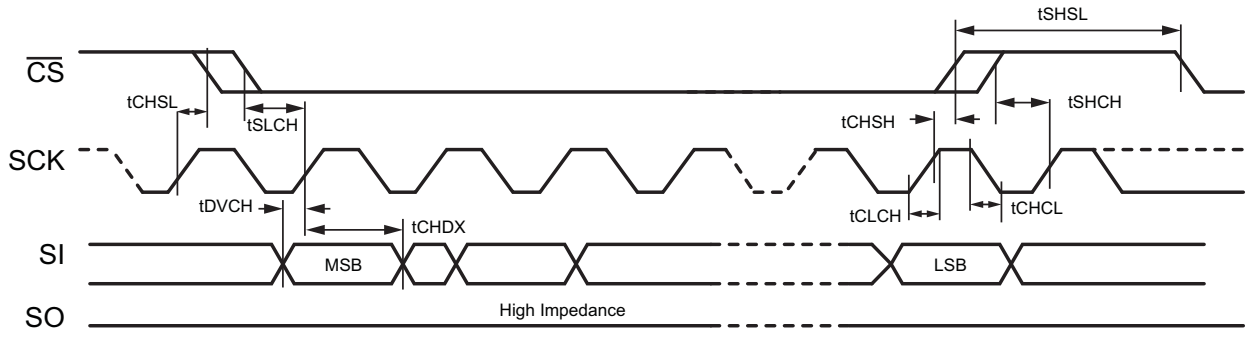


Figure 157. Serial Input Timing

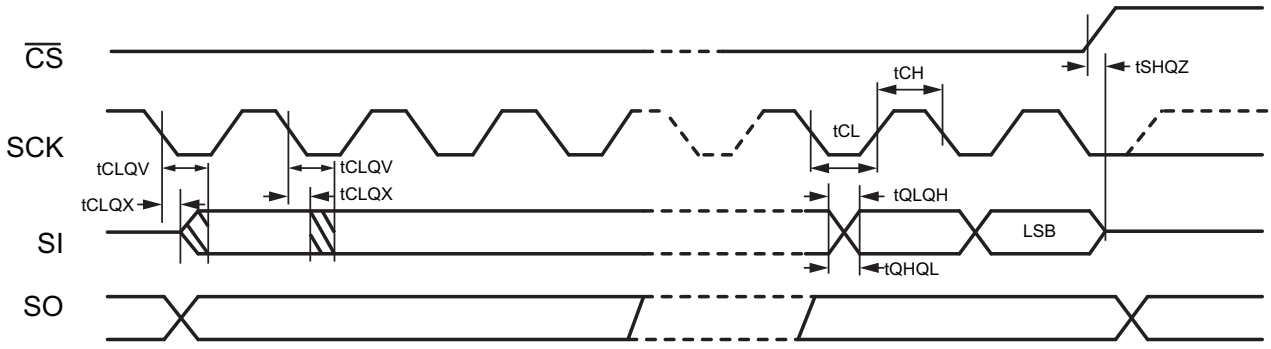


Figure 158. Output Timing

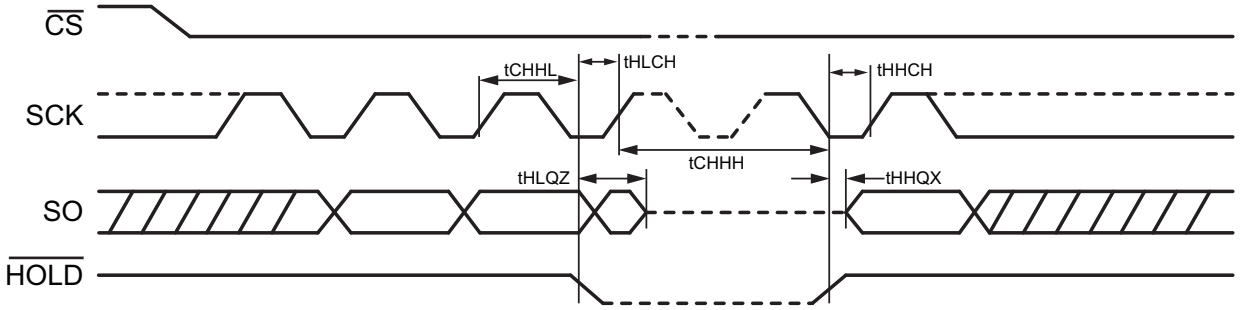


Figure 159. $\overline{\text{HOLD}}$ Timing

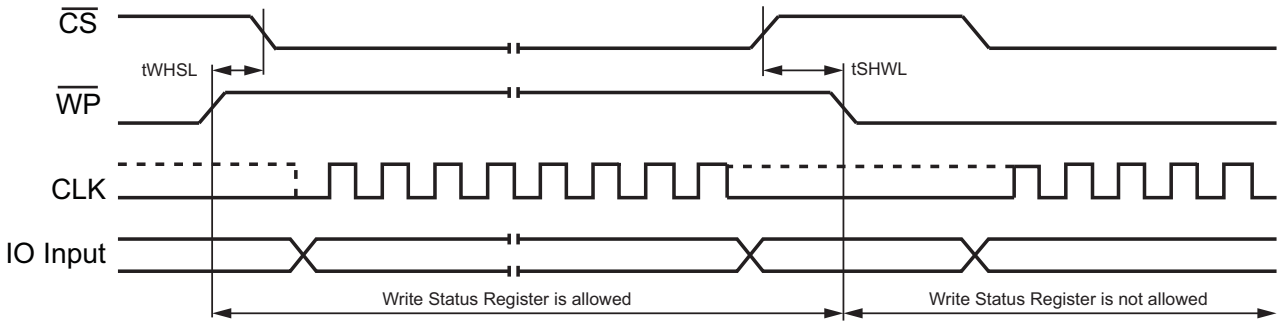
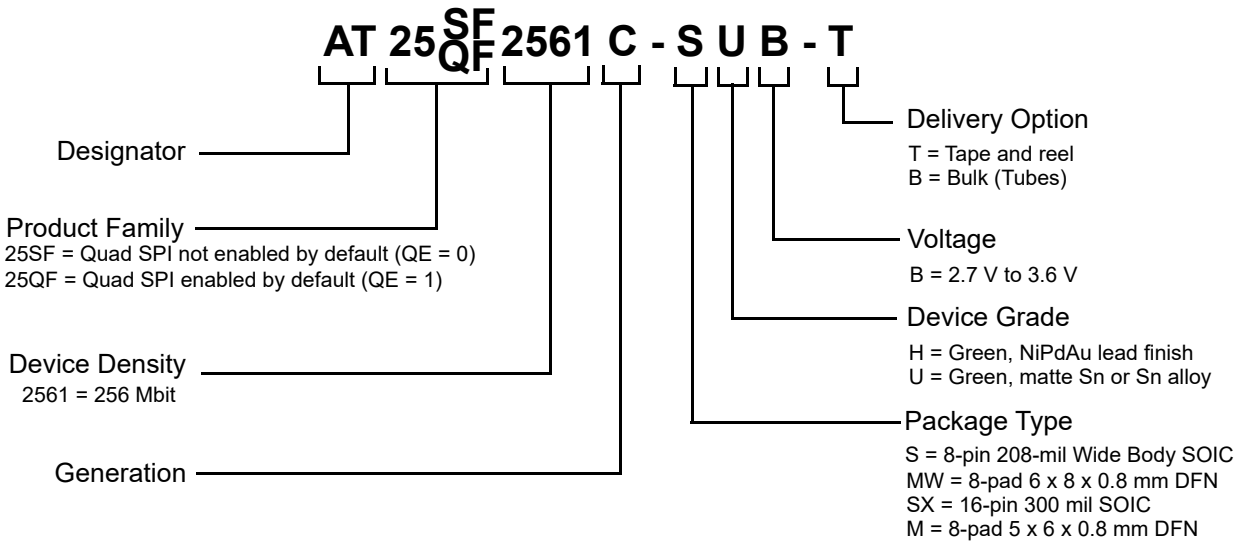


Figure 160. $\overline{\text{WP}}$ Timing

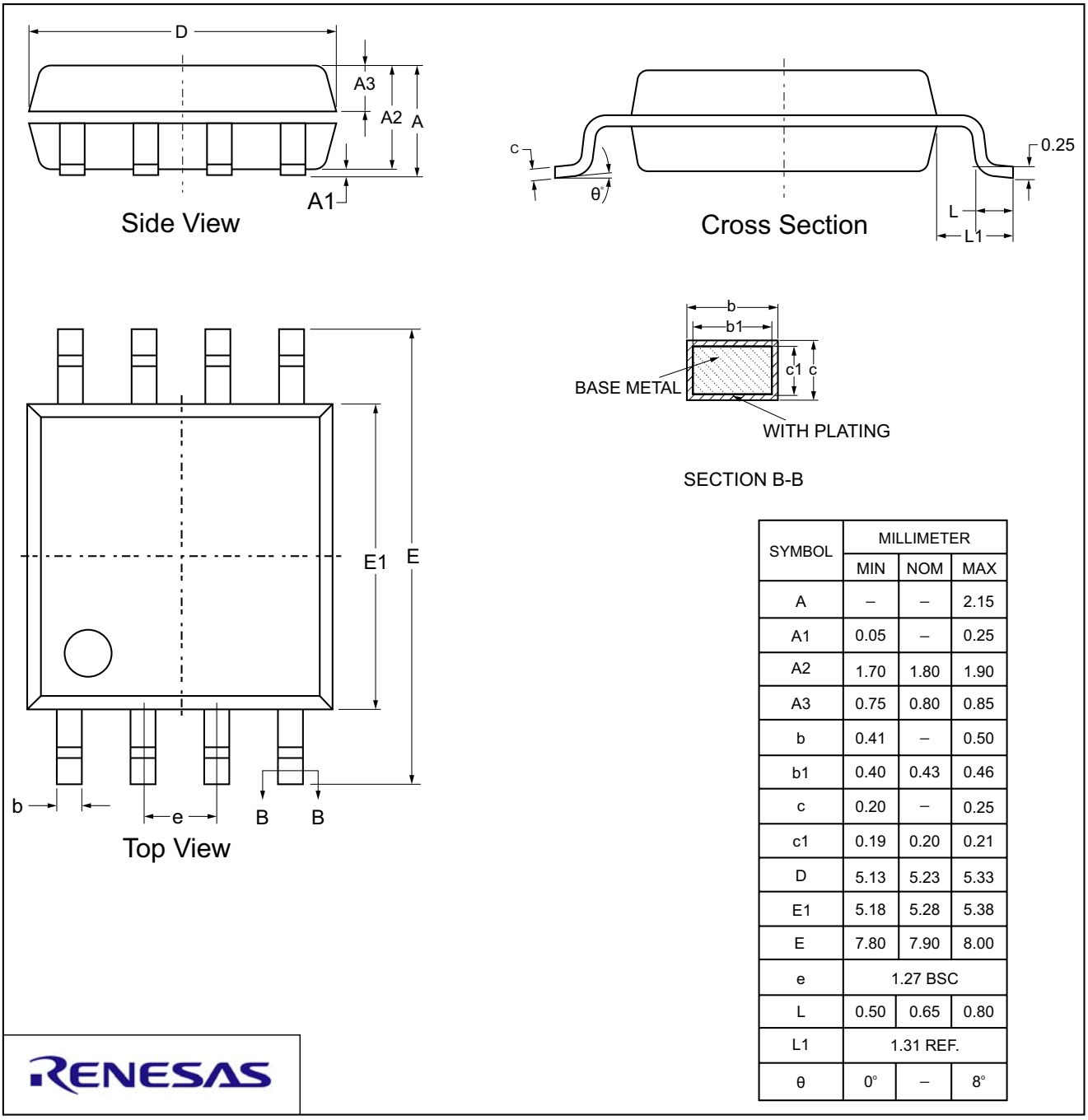
9. Ordering Information



Ordering Code	Package Type	Lead Finish	Operating Voltage	Delivery Option
AT25SF2561C-SUB-T AT25QF2561C-SUB-T	8-pin, 208-mil Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC).	Matte Sn or Sn alloy	2.7 V - 3.6 V	Tape and Reel
AT25SF2561C-MWUB-T AT25QF2561C-MWUB-T	8-pad, 6 x 8 x 0.8 mm body, Thermally Enhanced Plastic Dual Flat No-lead (DFN).			
AT25SF2561C-MUB-T AT25QF2561C-MUB-T	8-pad, 5 x 6 x 0.8 mm body, Thermally Enhanced Plastic Dual Flat No-lead (DFN).			
AT25SF2561C-SXUB-T AT25QF2561C-SXUB-T	16-pin, 300-mil SOIC.			

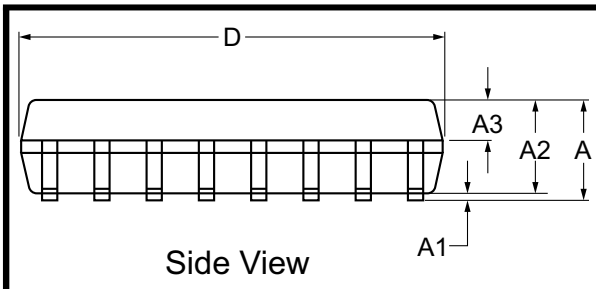
10. Packaging Information

10.1 8-Pin, 208-mil Wide EIAJ SOIC

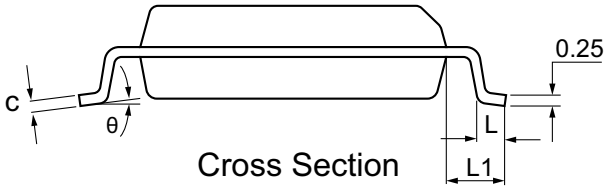


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	2.15
A1	0.05	–	0.25
A2	1.70	1.80	1.90
A3	0.75	0.80	0.85
b	0.41	–	0.50
b1	0.40	0.43	0.46
c	0.20	–	0.25
c1	0.19	0.20	0.21
D	5.13	5.23	5.33
E1	5.18	5.28	5.38
E	7.80	7.90	8.00
e	1.27 BSC		
L	0.50	0.65	0.80
L1	1.31 REF.		
θ	0°	–	8°

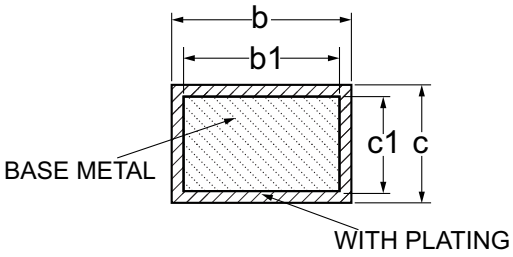
10.2 16-Pin, 300-mil Wide EIAJ SOIC



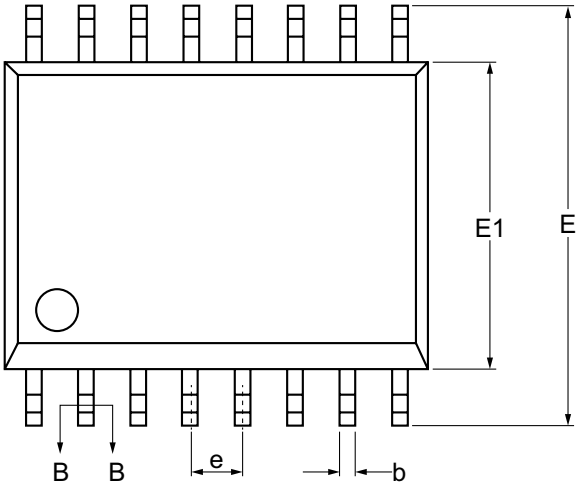
Side View



Cross Section



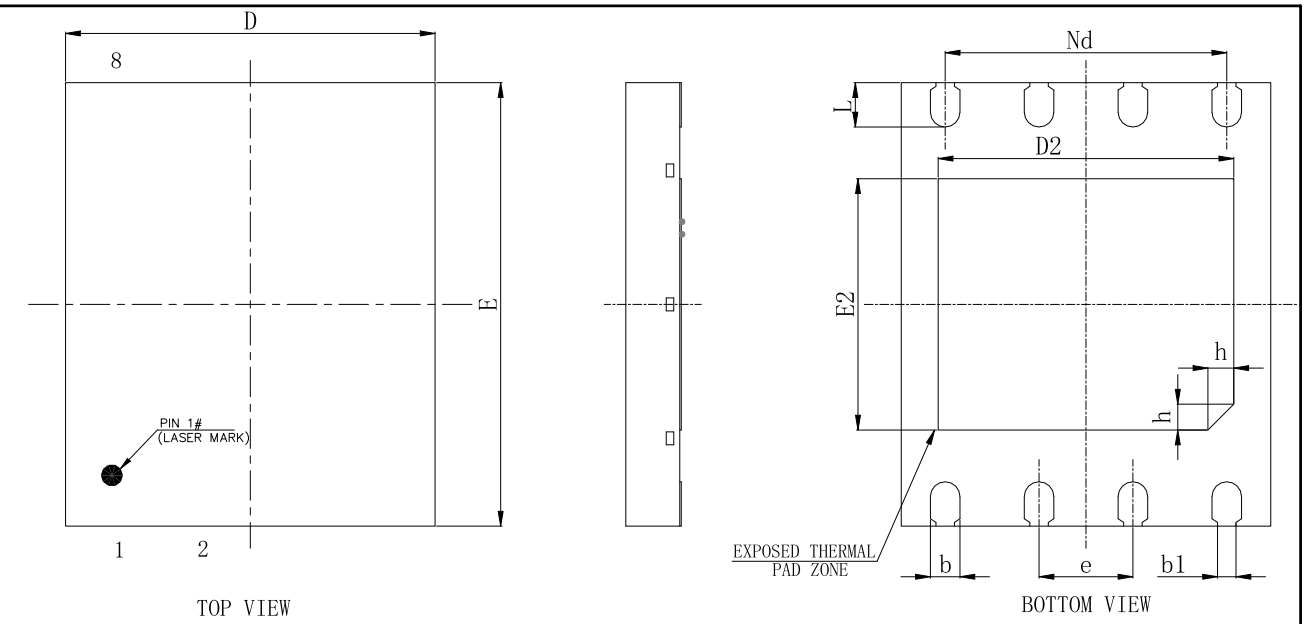
SECTION B-B

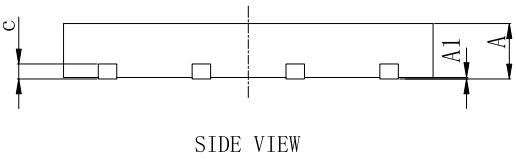


Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	2.65
A1	0.10	–	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	–	0.43
b1	0.34	0.37	0.40
c	0.25	–	0.29
c1	0.24	0.25	0.26
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 BSC		
L	0.55	–	0.85
L1	1.40REF		
θ	0	–	8°

10.3 8-Pad 5 x 6 x 0.8 mm DFN

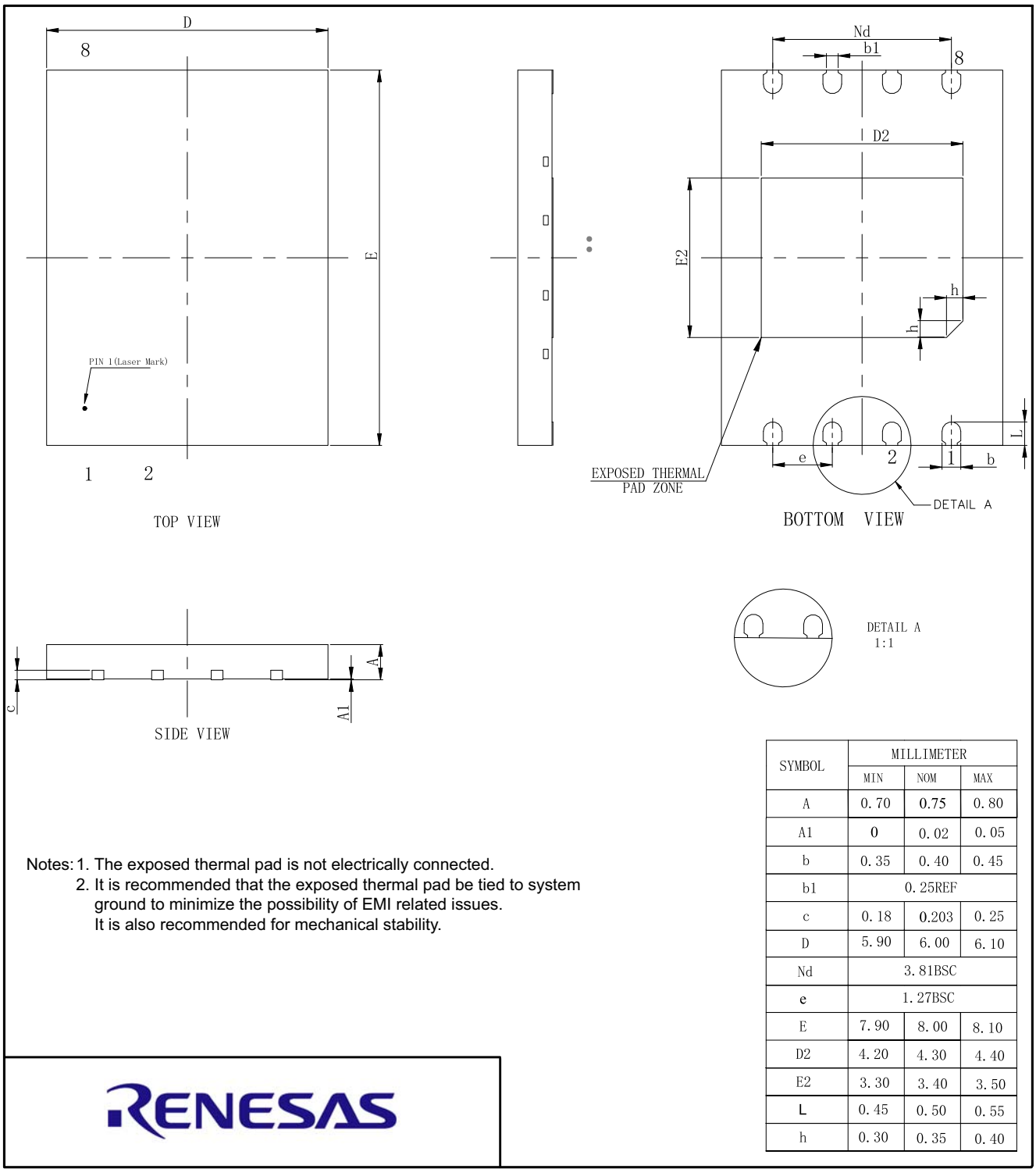




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.35	0.40	0.45
b1	0. 25REF		
c	0.18	0.203	0.25
D	4.90	5.00	5.10
Nd	3.81 BSC		
e	1.27 BSC		
E	5.90	6.00	6.10
D2	3.90	4.00	4.10
E2	3.30	3.40	3.50
L	0.55	0.60	0.65
h	0.30	0.35	0.40

Notes: 1. The exposed pad is not electrically connected.
2. It is recommended that the exposed thermal pad be tied to system ground to minimize the possibility of EMI related issues. It is also recommended for mechanical stability.

10.4 8-Pad 6 x 8 x 0.8 mm DFN



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.35	0.40	0.45
b1		0.25REF	
c	0.18	0.203	0.25
D	5.90	6.00	6.10
Nd		3.81BSC	
e		1.27BSC	
E	7.90	8.00	8.10
D2	4.20	4.30	4.40
E2	3.30	3.40	3.50
L	0.45	0.50	0.55
h	0.30	0.35	0.40

Notes: 1. The exposed thermal pad is not electrically connected.
2. It is recommended that the exposed thermal pad be tied to system ground to minimize the possibility of EMI related issues. It is also recommended for mechanical stability.

11. Revision History

Revision	Date	Change Description
A	08/2023	Initial release.
B	09-2023	Added AT25QF2561C specifications.
C	02-2024	Corrected cross-reference in Section 5.6.2.9. Corrected Figure 2. Changed all instance of WIP to RDY/BSY. Made Status Register section a top-level heading. Changed text for HOLD/RESET/IO_3. Added RESET to all timing diagrams that had HOLD.
D	05-2024	Changed document designation from Advanced to Preliminary. Made correction to Figure2. Made corrections to Sections 5.2.5, 7.2.1, 7.2.3.2, 7.2.11.3, 7.2.12.3, 7.2.13.2, 7.2.14.1, 7.3.2, and 7.3.3. Made corrections to Tables 6, 7, 8, 19, 30, 31, 37, 38, 45, and 47. Added two bullets under SPI compatible support in the Features List, front page. Altered text in the first two paragraphs of Section 7.6.12. Corrected device thickness to 0.8 mm for UDFN in the Features List, as well as Sections 9 and 10.
E	06-2024	Made corrections to Table 30.
F	08-2024	Removed ‘Preliminary’ from datasheet header. Changed title of Section 3 to ‘Memory Architecture.’ Updated Table 2. Updated Figure 6. Made corrections to Tables 44, 45, and 47. Updated Figure 154. Added Figure 155. Renamed UDFN to DFN. Added notes to ‘8-Pad 5 x 6 x 0.8 mm DFN’ and ‘8-Pad 6 x 8 x 0.8 mm DFN’ regarding the exposed thermal pad. Changed ‘Sector’ to ‘Block.’ Corrected pin symbols in various figures. Removed I/O_{0-3} from SPI figures and SI/SO from Dual or Quad operations. Combined Packaging Information and Ordering Information sections.
G	11-2024	Updated Section 6.1.1 ‘Operating Supply Voltage.’ Updated Figure 154 ‘Power-Up Timing and Voltage Levels.’ Corrected I_{CC2} maximum value in Table 45 ‘DC Electrical Characteristics.’ Added Section 10 ‘Packaging Information.’ Edited various graphics for clarity and consistency.
H	01-2025	Corrected Section 5 ‘Status Registers.’ Removed ‘S’ from status register bits and used SR1/SR2/SR3 to designate between registers.

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