# AT25SL1281C / AT25QL1281C

128-Mbit, 1.65 V – 1.95 V SPI Serial Flash Memory with Dual I/O, Quad I/O, and QPI Support

## Features

- Single 1.65 V - 1.95 V supply
- Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI) compatible support
  - Supports SPI Modes 0 and 3
  - Supports SPI dual output operations (1-1-2)
  - Supports Quad output operations (1-1-4)
  - Supports Quad I/O / XiP operations (1-4-4, 0-4-4)
  - Supports QPI I/O operations (4-4-4)
- Read Operations
  - Fast Read up to 133 MHz with 30 pF load
  - Clock-to-Output of 7 ns
  - Up to 266 Mb/s continuous data transfer rate (Dual I/O)
  - Up to 532 Mb/s continuous data transfer rate (Quad I/O and QPI)
  - XiP (eXecute in Place) operation: continuous read with 8/16/32/64-byte wrap
- Full Chip Erase
- Flexible Erase Architecture and Time
  - 22 ms Typical 4-kB Block Erase Time (Typical)
  - 85 ms Typical 32-kB Block Erase Time (Typical)
  - 160 ms Typical 64-kB Block Erase Time (Typical)
- Flexible Programming and Time
  - Byte/Page Program (1 to 256 Bytes)
  - Dual or Quad Input Byte/Page Program (1 to 256 Bytes)
- Erase/Program Suspend and Resume
- JEDEC Standard Manufacturer and Device ID
- Memory Protection Support
  - User-Definable Protected Area at Start or End of Memory Array
  - Enable/Disable Protection with $\overline{\text{WP}}$ Pin
- 3 x 1024-Byte One-Time Programmable (OTP) Security Registers
- Serial Flash Discoverable Parameters (SFDP) Register
- Low Power Dissipation
  - 0.3 µA Deep Power-Down Current (Typical)
  - 3.5 µA Standby current (Typical)
  - 3.2 mA Active Read Current (Typical)
- Endurance: 100,000 program/erase cycles (4-kB, 32-kB, or 64-kB blocks)
- Data Retention: 20 Years
- Temperature Range: -40 °C to +85 °C (Industrial)
- Industry Standard Green (Pb/Halide-free/RoHS Compliant) Package Options
  - 8-pad, 5 x 6 x 0.8 mm DFN
  - 8-pad, 6 x 8 x 0.8 mm DFN
  - 8-lead, 208-mil Wide SOIC
  - 16-lead, 300-mil SOIC
  - 14-ball, WLCSP


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# 1. Product Overview

The AT25SL1281C / AT25QL1281C is a 128-Mbit Serial Peripheral Interface (SPI) Flash memory device designed for use in a wide variety of high-volume industrial, consumer, and connected applications.

It can be used for storing program memory that is copied from Flash memory into embedded or external RAM during system boot; it also can be used for directly executing program code from Flash memory (Execute in Place [XiP]).

- XiP is specifically supported by features which enhance read speed:
- Quad-SPI, which allows reading four bits in one clock cycle.
- Continuous read mode (0-4-4 command format), which removes the need to send a command opcode.
- High SPI clock frequency.

These features allow fast response from the Flash memory whenever the host must fetch commands or data from it.


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# 2. Pinouts and Pin Descriptions

The following figures show the pinout of each available package type.

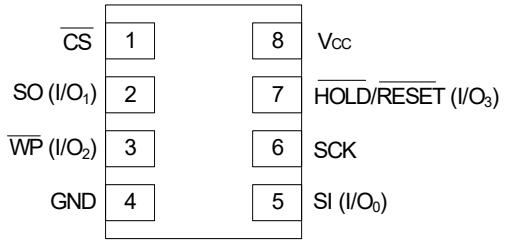


**Figure 1. 8-DFN (Top View)**

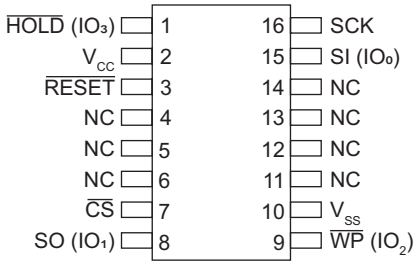


**Figure 2. 16-Lead 300-mil SOIC (Top View)**

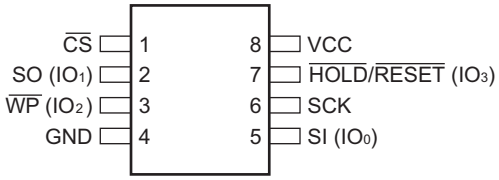


**Figure 3. 8-Lead 208-mil SOIC (Top View)**

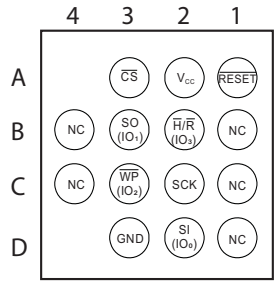


**Figure 4. 14-Ball WLCSP (Ball Side View)**

During all operations, $V_{CC}$ must be held stable and within the specified valid range: $V_{CC}$ (min) to $V_{CC}$ (max).

All of the input and output signals must be held high or low (according to voltages of $V_{IH}$, $V_{OH}$, $V_{IL}$ or $V_{OL}$).

**Table 1. Pin Descriptions**

| Symbol | Name and Function | Asserted State | Type |
|---|---|---|---|
| $\overline{CS}$ | **CHIP SELECT**<br>When this input signal is high, the device is deselected and serial data output pins are at high impedance. Unless an internal program, erase, or write status register cycle is in progress, the device is in the standby power mode (this is not the deep power-down mode). Driving Chip Select ($\overline{CS}$) low enables the device, placing it in the active power mode. After power-up, a falling edge on Chip Select ($\overline{CS}$) is required before the start of any command.<br>To ensure correct power-up sequencing, it is recommended to add a 10k Ohm pull-up resistor from $\overline{CS}$ to $V_{CC}$. This ensures $\overline{CS}$ ramps together with $V_{CC}$ during power-up. | Low | Input |
| SCK | **SERIAL CLOCK**<br>This input signal provides the timing for the serial interface. Commands, addresses, or data present at serial data input are latched on the rising edge of Serial Clock (SCK). Data are shifted out on the falling edge of the Serial Clock (SCK). | - | Input |


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**Table 1. Pin Descriptions *(Continued)***

| Symbol | Name and Function | Asserted State | Type |
|---|---|---|---|
| SI ($I/O_0$) | **SERIAL INPUT**<br>The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched in on the rising edge of SCK.<br>With the Dual-Output and Quad-Output Read commands, the SI Pin becomes an output pin ($I/O_0$) in conjunction with other pins to allow two or four bits of data on ($I/O_{3-0}$) to be clocked in on every falling edge of SCK<br>To maintain consistency with the SPI nomenclature, the SI ($I/O_0$) pin is referenced as the SI pin unless specifically addressing the Dual-I/O and Quad-I/O modes in which case it is referenced as $I/O_0$.<br>Data present on the SI pin is ignored whenever the device is deselected ($\overline{CS}$ is deasserted). | - | Input/Output |
| SO ($I/O_1$) | **SERIAL OUTPUT**<br>The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK.<br>With the Dual-Output Read commands, the SO Pin remains an output pin (I/O0) in conjunction with other pins to allow two bits of data on ($I/O_{1-0}$) to be clocked in on every falling edge of SCK.<br>To maintain consistency with the SPI nomenclature, the SO ($I/O_1$) pin is referenced as the SO pin unless specifically addressing the Dual-I/O modes in which case it is referenced as $I/O_1$. The SO pin is in a high-impedance state whenever the device is deselected ($\overline{CS}$ is deasserted). | - | Input/Output |
| $\overline{WP}$ ($I/O_2$) | **WRITE PROTECT**<br>This pin is used either for write-protection, in which case it is referred to as $\overline{WP}$, or as one of the quad-SPI I/O pins, in which case it is referred to as $IO_2$.<br>When the Quad Enable (QE) bit of Status Register 2 is 0 (default for the AT25SL1281C), and the SRP1 and SRP0 bits are 0 and 1, respectively, the pin can be used for write-protection. It then can be asserted (driven low) to protect the Status Registers from modification.<br>When the QE bit of Status Register 2 is 1 (default for the AT25QL1281C), quad-SPI communication is enabled, and the pin is used as I/O pin $IO_2$ in any command that makes use of quad-SPI. In this setting, do not use the pin for write-protection.<br>The $\overline{WP}$ pin does not have an internal pull-up; thus, it must either be driven or, if not used, pulled up with an external resistor to $V_{CC}$. | - | Input/Output |
| $\overline{HOLD}$ / $\overline{RESET}$($IO_3$) | **HOLD / RESET / $IO_3$**<br>This pin is used either for pausing communication (in which case it is referred to as $\overline{HOLD}$), as a hardware reset pin (in which case it is referred to as $\overline{RESET}$), or as one of the quad-SPI I/O pins (in which case it is referred to as $IO_3$).<br>When the Quad Enable (QE) bit of Status Register 2 is 0 (default for the AT25SL1281C), and the HOLD/RST bit in Status Register 3 is 0, this pin is used as a $\overline{HOLD}$ pin. When the Quad Enable (QE) bit of Status Register 2 is 0 and the HOLD/RST bit in Status Register 3 is 1, this pin is used as a $\overline{RESET}$ pin. When the QE bit of Status Register 2 is 1 (default for the AT25QL1281C), quad-SPI communication is enabled, and the pin is used as the $IO_3$ pin in any command that makes use of quad-SPI. In this setting, do not use the pin for pausing communication or for reset.<br>The $\overline{HOLD}$ pin is used to pause a SPI sequence without resetting the clocking sequence. To enable the HOLD mode, the $\overline{CS}$ must be low. The HOLD mode effect is on with the falling edge of the $\overline{HOLD}$ signal with SCK being low. The HOLD mode ends on the rising edge of $\overline{HOLD}$ signal with SCK being low.<br>If not used, the $\overline{HOLD}$ pin is internally pulled-high and can be left floating.<br>Note: When using the device in a 16-pin SOIC package, use the dedicated $\overline{RESET}$ (pin3) for a hardware reset. | - | Input/Output |


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**Table 1. Pin Descriptions *(Continued)***

| Symbol | Name and Function | Asserted State | Type |
|---|---|---|---|
| $V_{CC}$ | **DEVICE POWER SUPPLY:** $V_{CC}$ is the supply voltage. It is the single voltage used for all device functions including read, program, and erase. The $V_{CC}$ pin is used to supply the source voltage to the device. Operations at invalid $V_{CC}$ voltages may produce spurious results; do not attempt them. | - | Power |
| GND | **GROUND:** GND is the reference for the $V_{CC}$ supply voltage. The ground reference for the power supply. Connect GND to the system ground. | - | Power |


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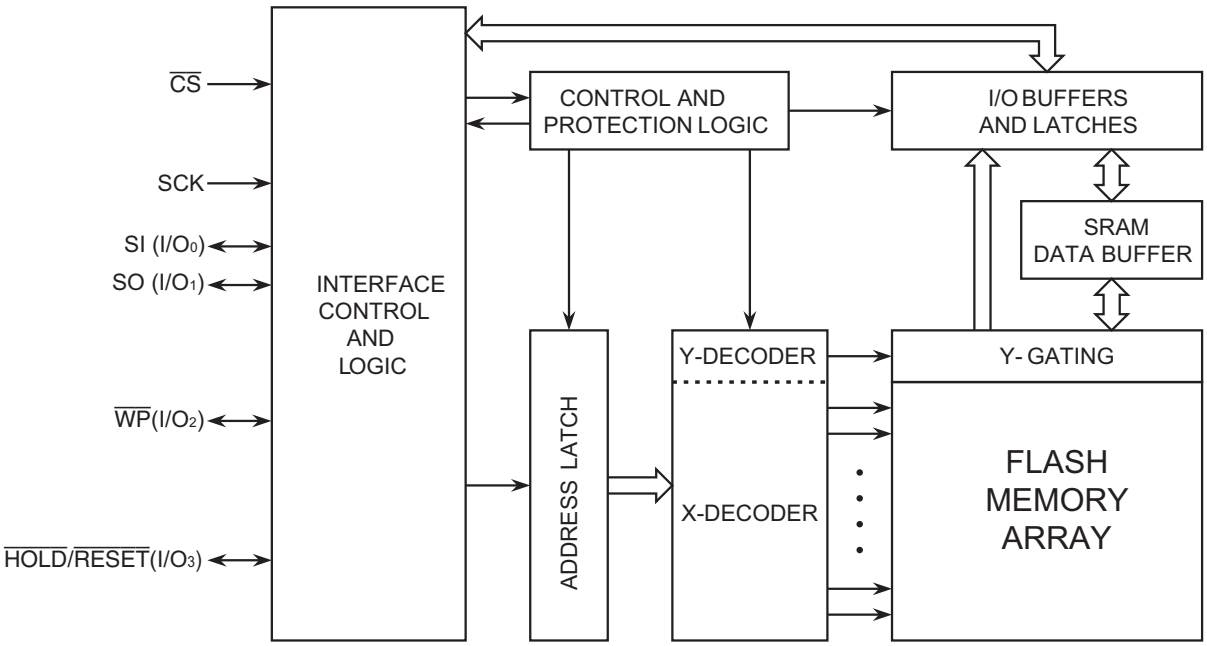
# 3. Block Diagram

Figure 5 shows a block diagram of the AT25SL1281C serial Flash.




Note: $I/O_{3-0}$ pin naming convention is used for Dual-I/O and Quad-I/O commands.

**Figure 5. AT25SL1281C Block Diagram**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# 4. Memory Array

To provide the greatest flexibility, the memory array of the AT25SL1281C / AT25QL1281C can be erased in four levels of granularity including a full chip erase. The size of the erase blocks is optimized for both code and data storage applications, allowing both code and data segments to reside in their own erase regions. Figure 6 shows of each erase level.

| 64 kB Block Erase (D8h) | 32 kB Block Erase (52h) | 4 kB Block Erase (20h) | Block Address Range |
|---|---|---|---|
| 64 kB (block 255) | 32 kB (block 511) | 4 kB (B4095) | FFF000h - FFFFFFh |
| | | 4 kB (B 4094) | FFE000h - FFEFFFh |
| | | 4 kB (B4093) | FFD000h - FFDFFFh |
| | | 4 kB (B4092) | FFC000h - FFCFFFh |
| | | 4 kB (B4091) | FFB000h - FFBFFFh |
| | | 4 kB (B4090) | FFA000h - FFAFFFh |
| | | 4 kB (B4089) | FF9000h - FF9FFFh |
| | | 4 kB (B4088) | FF8000h - FF8FFFh |
| | 32 kB (block 510) | 4 kB (B4087) | FF7000h - FF7FFFh |
| | | 4 kB (B4086) | FF6000h - FF6FFFh |
| | | 4 kB (B4085) | FF5000h - FF5FFFh |
| | | 4 kB (B4084) | FF4000h - FF4FFFh |
| | | 4 kB (B4083) | FF3000h - FF3FFFh |
| | | 4 kB (B4082) | FF2000h - FF2FFFh |
| | | 4 kB (B4081) | FF1000h - FF1FFFh |
| | | 4 kB (B4080) | FF0000h - FF0FFFh |
| 64 kB (block 254) to 64 kB (block 1) | 32 kB (block 509) to 32 kB (block 2) | 4 kB (B4079) to 4 kB (B16) | FEF000h - FEFFFFh to 010000h - 010FFFh |
| 64 kB (block 0 | 32 kB (block 1) | 4 kB (B15) | 00F000h - 00FFFFh |
| | | 4 kB (B14) | 00E000h - 00EFFFh |
| | | 4 kB (B13) | 00D000h - 00DFFFh |
| | | 4 kB (B12) | 00C000h - 00CFFFh |
| | | 4 kB (B11) | 00B000h - 00BFFFh |
| | | 4 kB (B10) | 00A000h - 00AFFFh |
| | | 4 kB (B9) | 009000h - 009FFFh |
| | | 4 kB (B8) | 008000h - 008FFFh |
| | 32 kB (block 0) | 4 kB (B7) | 007000h - 007FFFh |
| | | 4 kB (B6) | 006000h - 006FFFh |
| | | 4 kB (B5) | 005000h - 005FFFh |
| | | 4 kB (B4) | 004000h - 004FFFh |
| | | 4 kB (B3) | 003000h - 003FFFh |
| | | 4 kB (B2) | 002000h - 002FFFh |
| | | 4 kB (B1) | 001000h - 001FFFh |
| | | 4 kB (B0) | 000000h - 000FFFh |

**Figure 6. Memory Architecture Diagram**


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# 5. Device Operation

Standard/Dual/Quad SPI mode, and QPI mode are exclusive; only one of these two modes can be active at any given time.

## 5.1 Standard SPI Operation

The AT25SL1281C / AT25QL1281C features a serial peripheral interface on four signals: Serial Clock (SCK), Chip Select ($\overline{CS}$), Serial Data Input (SI) and Serial Data Output (SO). Standard SPI commands use the SI input pin to serially write commands, addresses or data to the device on the rising edge of SCK. The SO output pin is used to read data or status from the device on the falling edge of SCK.

SPI bus operation Modes 0 and 3 are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the SCK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the SCK signal is normally low on the falling and rising edges of $\overline{CS}$. For Mode 3 the SCK signal is normally high on the falling and rising edges of $\overline{CS}$.

## 5.2 Dual SPI Operation

The AT25SL1281C / AT25QL1281C supports Dual SPI operation. This command allows data to be transferred to or from the device at two times the rate of the standard SPI. The Dual Read command is ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed- critical code directly from the SPI bus (XiP). When using Dual SPI commands the SI and SO pins become bidirectional I/0 pins; $IO_0$ and $IO_1$.

## 5.3 Quad SPI Operation

The AT25SL1281C / AT25QL1281C supports Quad SPI operation. This command allows data to be transferred to or from the device at four times the rate of the standard SPI. The Quad Read command offers a significant improvement in continuous and random access transfer rates allowing fast code- shadowing to RAM or execution directly from the SPI bus (XiP). When using Quad SPI command the SI and SO pins become bidirectional $IO_0$ and $IO_1$, and the $\overline{WP}$ and $\overline{HOLD}$ pins become $IO_2$ and $IO_3$ respectively. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

## 5.4 QPI Operation (4-4-4)

The AT25SL1281C / AT25QL1281C supports Quad Peripheral Interface (QPI) operation when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the Enable QPI (38h) command. Before QPI mode can be enabled, the Quad Enable bit (QE) in Status Register-2 must be set. When using QPI commands, the SI and SO pins become bidirectional $IO_0$ and $IO_1$, and the $\overline{WP}$ and $\overline{HOLD}$ pins become $IO_2$ and $IO_3$, respectively.

The typical SPI protocol requires the byte-long command code to be shifted into the device only through the SI pin in eight serial clocks. The QPI mode uses all four I/O pins to input the command code; thus, only two serial clocks are required to send it. This can significantly reduce the SPI command overhead and improve system performance in an XiP environment. Address and data, if present in a command, are also sent over all four I/O pins; hence, QPI mode is also known as “4-4-4.”

Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one of the two modes can be active at any given time. The enable QPI (38h) and Disable QPI (FFh) commands are used to switch between these two modes. On power-up, or after a software or hardware reset, the default state of the device is Standard/Dual/Quad SPI mode.


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## 5.5 Switching Between SPI and QPI Operations

Figure 7 illustrates the process for switching between SPI and QPI operations.

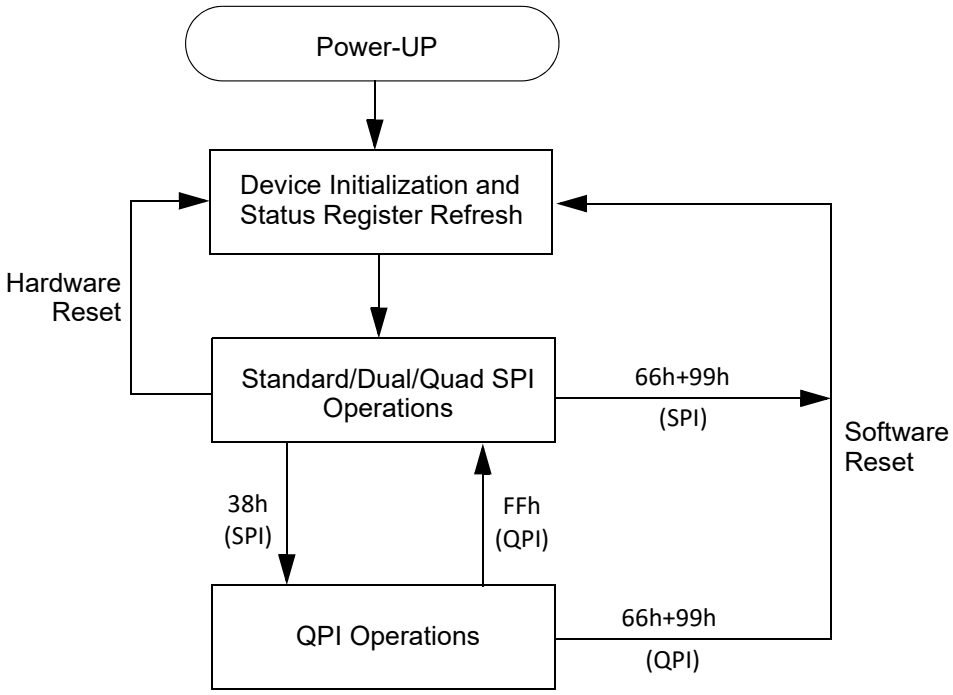


**Figure 7. Switching Between SPI and QPI Operations**


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# 6. Operation Features

## 6.1 Supply Voltage

### 6.1.1 Operating Supply Voltage

A valid and stable $V_{CC}$ voltage within the specified [$V_{CC}$(min), $V_{CC}$(max)] range must be applied before selecting the memory and issuing commands to it. To secure a stable DC supply voltage, decouple the $V_{CC}$ line with a 0.1 µF to 1 µF low ESR/ESL capacitor placed close to the $V_{CC}$/GND package pins.

### 6.1.2 Power-up Conditions

When the power supply is turned on, $V_{CC}$ rises continuously from GND to $V_{CC}$. During this time, the Chip Select ($\overline{CS}$) line is not allowed to float but should follow the $V_{CC}$ voltage; thus, it is recommended to connect the $\overline{CS}$ line to $V_{CC}$ via a suitable pull-up resistor.

Also, the $\overline{CS}$ input offers a built-in safety feature: the $\overline{CS}$ input is edge-sensitive and level-sensitive. After power-up, the device does not become selected until a falling edge has first been detected on $\overline{CS}$. This ensures that $\overline{CS}$ must have been high before going low to start the first operation.

### 6.1.3 Device Reset

To prevent inadvertent Write operations during power-up (continuous rise of $V_{CC}$), a power-on reset (POR) circuit is included. At power-up, the device does not respond to any command until $V_{CC}$ has reached the power-on reset threshold voltage (this threshold is lower than the minimum $V_{CC}$ operating voltage defined in the power-up timing).

When $V_{CC}$ is lower than $V_{WI}$, the device is reset.

### 6.1.4 Power-Down

At power-down (continuous decrease in $V_{CC}$), as soon as $V_{CC}$ drops from the normal operating voltage to below the power-on reset threshold voltage ($V_{WI}$), the device stops responding to any command sent to it. During power-down, the device must be deselected ($\overline{CS}$ must be allowed to follow the voltage applied on $V_{CC}$) and in Standby Power mode (no internal Write cycle is in progress).

### 6.1.5 Active Power and Standby Power Modes

When $\overline{CS}$ is low, the device is selected and in the Active Power mode. The device consumes $I_{CC}$.

When $\overline{CS}$ is high, the device is deselected. If a write cycle is not currently in progress, the device goes into Standby Power mode, and the device consumption drops to $I_{CC1}$.

### 6.1.6 Hold Condition

When QE=0 and HOLD/RST=0, the $\overline{HOLD}$ signal is used to pause any serial communications with the device without resetting the clocking sequence. During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCK) are Don't Care. To enter the Hold condition, the device must be selected, with $\overline{CS}$ Low. Normally, the device is kept selected for the duration of the Hold condition. Deselecting the device while it is in the Hold condition has the effect of resetting the state of the device. This mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the $\overline{HOLD}$ signal is driven low at the same time as SCK is already low (see Figure 8).The Hold condition ends when the $\overline{HOLD}$ signal is driven high at the same time as SCK is already low. Figure 8 also shows what happens if the rising and falling edges are not timed to coincide with SCK being low.


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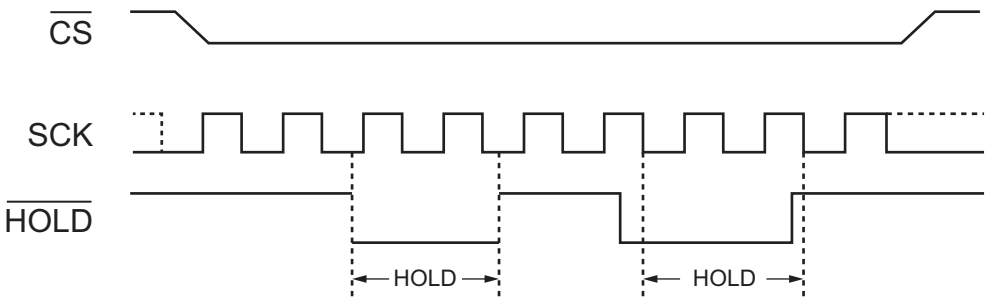


**Figure 8. Hold Condition Activation**

## 6.2 Software Reset

The AT25SL1281C / AT25QL1281C can be reset to the initial power-on state by a software reset sequence. This sequence must include two consecutive commands: Enable Reset (66h) and Reset (99h). If the command sequence is successfully accepted, the device takes approximately $t_{RST}$ to reset. No command is accepted during the reset period.

## 6.3 Hardware Reset ($\overline{\text{HOLD}}$ Pin)

The AT25SL1281C / AT25QL1281C can also be configured to use the hardware $\overline{\text{RESET}}$ pin. The HOLD/RST bit in Status Register 3 is the configuration bit for the $\overline{\text{HOLD}}$ pin function or the $\overline{\text{RESET}}$ pin function. When HOLD/RST=0 (factory default), the pin acts as a $\overline{\text{HOLD}}$ pin, as described above; when HOLD/RST=1, the pin acts as a $\overline{\text{RESET}}$ pin. Driving the $\overline{\text{RESET}}$ pin low for a minimum period of ~1 µs ($t_{RESET}$) resets the device to its initial power-on state. Any on-going Program/Erase operation is interrupted, and data corruption can happen. While $\overline{\text{RESET}}$ is low, the device does not accept any command input.

If QE bit is set to 1 (default for the AT25QL1281C), the $\overline{\text{HOLD}}$ or $\overline{\text{RESET}}$ function are disabled, and the pin becomes one of the four data I/O pins.

The hardware $\overline{\text{RESET}}$ pin has the highest priority among all the input signals. Driving $\overline{\text{RESET}}$ low for a minimum period of ~1 µs ($t_{RESET}$) interrupts any on-going external/internal operations, regardless the status of other SPI signals ($\overline{\text{CS}}$, SCK, IOs, $\overline{\text{WP}}$, and $\overline{\text{HOLD}}$). Note that while a faster $\overline{\text{RESET}}$ pulse (as short as a few hundred nanoseconds) often resets the device, a 1 µs minimum pulse is recommended to ensure reliable operation.

## 6.4 Write Protection

To protect inadvertent writes by the possible noise, several means of protection are applied to the Flash memory. Write protection features include:

- During power-on reset, all operations are disabled, and no command is recognized.
- An internal time delay of $t_{PUW}$ can protect the data against inadvertent changes while the power supply is outside the operating specification. This includes the Write Enable, Page program, Block Erase, Chip Erase, Write Security Register. and Write Status Register commands.
- For data changes, Write Enable command must be issued to set the Write Enable Latch (WEL) bit to 0. Power-up, Completion of Write Disable, Write Status Register, Page program, Block Erase, and Chip Erase are subject to this condition.
- Using the Status Register protect (SRP) and Block protect (BP4 – BP0) bits, a portion of memory can be configured as read only (this is called software protection).
- Write Protect ($\overline{\text{WP}}$) pin can control to change the Status Register under hardware control.
- The Deep Power-Down mode provides extra protection from unexpected data changes as all commands are ignored under this status except for Release Deep Power-Down command.


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- Device resets when $V_{CC}$ is below threshold: At power-up or power-down, the AT25SL1281C / AT25QL1281C maintains a reset condition while $V_{CC}$ is below the threshold value of $V_{WI}$. While reset, all operations are disabled, and no commands are recognized.
- Write Enable: The Write Enable command is set with the Write Enable Latch bit. The WEL bit returns to reset in the following situations:
  - Power–up
  - Write Disable
  - Write Status Register (Whether the SR is protected, WEL returns to reset)
  - Page Program (Whether the program area is protected, WEL returns to reset)
  - Block Erase/Chip Erase (Whether the erase area is protected, WEL returns to reset)
  - Software Reset
  - Hardware Reset
- One Time Program (OTP) write protection for array and Security Registers using the Status Register.


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# 7. Status Registers

**Table 2. Status Register 1 Format**

| Bit # | Acronym | Name | Type | Default | Volatile/ Non-Volatile | Description |
|---|---|---|---|---|---|---|
| 7 | SRP0 | Status Register Protect 0 | R/W | 0 | Non-Volatile | The Status Register Protect 0 bit is a non-volatile bit that, along with the SRP1, controls the method of status register write protection: software protection, hardware protection, power supply lock-down, or one time programmable protection. See Table 5. |
| 6:2 | BP4-BP0 | Block Protect Size | R/W | 0 | Non-Volatile | The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register command. When WPS=0, and the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (see Table 8 and Table 9) is protected against Page Program, and Block Erase commands. The Block Protect bits can be written if the Hardware Protected mode has not been set. The Chip Erase command is executed if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP=0, or the Block Protect (BP2, BP1, BP0) bits are 1 and CMP=1.<br>The factory default setting for the Block Protection Bits is 0; none of the array is protected. |
| 1 | WEL | Write Enable | R | 0 | Volatile | Write Enable Latch (WEL) is a read only bit in the status register that is set to a 1 after executing a Write Enable command. The WEL status bit is cleared to a 0 when device is write disabled. A write disable state occurs upon power-up or after any of the following commands: Write Disable, Page Program, Erase and Write Status Register. |
| 0 | RDY/BSY | Ready/Busy | R | 0 | Volatile | RDY/BSY is a read only bit in the status register that is set to a 1 state when the device is executing a Page Program, Erase, Write Status Register or Write Security Register command. During this time, the device ignores further commands except for the Read Status Register and Erase / Program Suspend command (see $t_W$, $t_{PP}$, $t_{BE}$, $t_{BE1}$, $t_{BE2}$ and $t_{CE}$ in AC Characteristics). When the Program, Erase, Write Status Register or Write Security Register command has completed, the RDY/BSY bit is cleared to a 0 state indicating the device is ready for further commands. |

**Table 3. Status Register 2 Format**

| Bit # | Acronym | Name | Type | Default | Volatile/ Non-Volatile | Description |
|---|---|---|---|---|---|---|
| 7 | SUS1 | Suspend Status | R | 0 | Volatile | The Suspend Status bit 1 is a read only bit in the Status Register that is set to 1 after executing a Suspend (75h) command during an erase operation. This bit is cleared to 0 after resuming an erase operation using the Resume (7Ah) command, as well as after power-up. |
| 6 | CMP | Complement Protect | R/W | 0 | Non-Volatile | The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register. It is used in conjunction with BP4 – BP0 bits to provide more flexibility for the array protection. See Table 8 and Table 9 for details. The default setting is CMP = 0. |


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**Table 3. Status Register 2 Format**

| | | | | | | |
|---|---|---|---|---|---|---|
| 5:3 | LB3-LB1 | Write-Protect and Control Status | R/W | 0 | Non-Volatile | The Security Register Lock (LB3/LB2/LB1) bits are non-volatile, One Time Program (OTP) bits that provide the write protect control and status to the Security Registers. Their default state is 0 (the security registers are unlocked). They can be set to 1 individually using the Write Register command. These bits are One Time Programmable: once they are set to 1, the Security Registers become read-only permanently. |
| 2 | SUS2 | Suspend Status | R | 0 | Volatile | The Suspend Status bit 2 is a read only bit in the Status Register that is set to 1 after executing a Suspend (75h) command during a program operation. This bit is cleared to 0 after resuming a program operation using the Resume (7Ah) command, as well as after power-up. |
| 1 | QE | Quad Enable | R/W | 0 | Non-Volatile | The Quad Enable (QE) bit is a non-volatile read/write bit in the status register that allows Quad SPI operations (including QPI). When the QE bit is set to 0 (default for the AT25SL1281C), the $\overline{WP}$ pin and $\overline{HOLD}$ are enabled. When the QE pin is set to 1(default for the AT25QL1281C), the Quad $IO_2$ and $IO_3$ pins are enabled instead and Quad SPI commands are available.<br>WARNING: Do not enable Quad SPI if the $\overline{WP}$ or $\overline{HOLD}$ pins are tied directly to the power supply or ground. |
| 0 | SRP1 | Status Register Protect 1 | R/W | 0 | Non-Volatile | The Status Register Protect 1 bit is a non-volatile bit that, along with the SRP0, controls the method of status register write protection: software protection, hardware protection, power supply lock-down, or one time programmable protection. See Table 5. |

**Table 4. Status Register 3 Format**

| Bit # | Acronym | Name | Type | Default | Volatile/ Non-Volatile | Description |
|---|---|---|---|---|---|---|
| 7 | HOLD/RST | $\overline{HOLD}$/$\overline{RESET}$ pin function | R/W | 0 | Non-Volatile | The $\overline{HOLD}$ or $\overline{RESET}$ Pin Function bit (HOLD/RST) is used to determine if a $\overline{HOLD}$ or $\overline{RESET}$ function is to be implemented on the hardware pin. When HOLD/RST=0 (factory default), the pin acts as $\overline{HOLD}$; when HOLD/RST=1, the pin acts as $\overline{RESET}$. The $\overline{HOLD}$ or $\overline{RESET}$ functions are only available when QE=0 (default for the AT25SL1281C). If QE is set to 1 (default for the AT25QL1281C), the $\overline{HOLD}$ and $\overline{RESET}$ functions are disabled, and the pin acts as a dedicated data pin ($IO_3$). |
| 6 | DRV1 | Output Driver Strength 1 | R/W | 1 | Non-Volatile | The Output Driver Strength (DRV1/DRV0) bits determine the drive strength of output signals used by any Read command (see Table 7). |
| 5 | DRV0 | Output Driver Strength 0 | R/W | 0 | Non-Volatile | |
| 4:2 | Reserved | | R | n/a | n/a | Reserved. |
| 1 | DC1 | Dummy Configuration 1 | R/W | 0 | Non-Volatile | The Dummy Configuration (DC) bits are non-volatile bits which select the number of dummy cycles between the end of address and the start of read data output. Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be transmitted to the host system. Some read commands require additional dummy cycles as the SPI clock frequency (SCK) increases.<br>Table 6 provides the decoding of the DC0/DC1 bits, and the number of required dummy cycles for different SPI clock frequencies. |
| 0 | DC0 | Dummy Configuration 0 | R/W | 0 | Non-Volatile | |


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**Table 5. Status Register Protection**

| SRP1 | SRP0 | $\overline{WP}$ | Status Register | Description |
|---|---|---|---|---|
| 0 | 0 | X | Software Protected | $\overline{WP}$ pin no control. The register can be written to after a Write Enable command, WEL = 1 (factory default). |
| 0 | 1 | 0 | Hardware Protected | When $\overline{WP}$ pin is low the Status Register locked and can not be written to. |
| 0 | 1 | 1 | Hardware Unprotected | When $\overline{WP}$ pin is high the Status register is unlocked and can be written to after a Write Enable command, WEL = 1. |
| 1 | 0 | X | Power Supply Lock-Down | Status Register is protected and cannot be written to again until the next power-down, power-up cycle. [1] |
| 1 | 1 | X | One Time Program [2] | Status Register is permanently protected and cannot be written to. |

1. When SRP1, SRP0 = (1,0), a power-down, power-up cycle changes SRP1, SRP0 to the (0,0) state.

2. OTP is available upon special order. Contact Renesas Electronics for details.

**Table 6. Dummy Configuration Matrix**

| Command | DC bits | No. of Dummy Cycles | Frequency (MHz) |
|---|---|---|---|
| BBh | 00 (default) | 4 | 108 |
| | 01 | 8 | 133 |
| | 10 | 4 | 108 |
| | 11 | 8 | 133 |
| EBh | 00 (default) | 6 | 108 |
| | 01 | 8 | 120 |
| | 10 | 10 | 133 |
| | 11 | 14 | 150 |

**Table 7. Status Register Protection**

| DRV1, DRV0 | Driver Strength |
|---|---|
| 00 | 100% |
| 01 | 75% |
| 10 (Default) | 50% |
| 11 | 25% |


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# 8. Array Memory Protection

Table 8 and Table 9 detail the protection scheme for the Status Register Memory.

**Table 8. Status Register Memory Protection (CMP = 0)**

| Status Register Bits | | | | | Memory Protection | | |
|---|---|---|---|---|---|---|---|
| BP4 | BP3 | BP2 | BP1 | BP0 | Addresses | Density | Portion |
| X | X | 0 | 0 | 0 | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | FC0000h - FFFFFFh | 256 kB | Upper 1/64 |
| 0 | 0 | 0 | 1 | 0 | F80000h - FFFFFFh | 512 kB | Upper 1/32 |
| 0 | 0 | 0 | 1 | 1 | F00000h - FFFFFFh | 1 MB | Upper 1/16 |
| 0 | 0 | 1 | 0 | 0 | E00000h - FFFFFFh | 2MB | Upper 1/8 |
| 0 | 0 | 1 | 0 | 1 | C00000h - FFFFFFh | 4 MB | Upper 1/4 |
| 0 | 0 | 1 | 1 | 0 | 800000h - FFFFFFh | 8 MB | Upper 1/2 |
| 0 | 1 | 0 | 0 | 1 | 000000h - 03FFFFh | 256 kB | Lower 1/64 |
| 0 | 1 | 0 | 1 | 0 | 000000h - 07FFFFh | 512 kB | Lower 1/32 |
| 0 | 1 | 0 | 1 | 1 | 000000h - 0FFFFFh | 1 MB | Lower 1/16 |
| 0 | 1 | 1 | 0 | 0 | 000000h - 1FFFFFh | 2 MB | Lower 1/8 |
| 0 | 1 | 1 | 0 | 1 | 000000h - 3FFFFFh | 4 MB | Lower 1/4 |
| 0 | 1 | 1 | 1 | 0 | 000000h - 7FFFFFh | 8 MB | Lower 1/2 |
| X | X | 1 | 1 | 1 | 000000h - FFFFFFh | 16 MB | ALL |
| 1 | 0 | 0 | 0 | 1 | FFF000h - FFFFFFh | 4 kB | Upper 1/4096 |
| 1 | 0 | 0 | 1 | 0 | FFE000h - FFFFFFh | 8 kB | Upper 1/2048 |
| 1 | 0 | 0 | 1 | 1 | FFC000h - FFFFFFh | 16 kB | Upper 1/1024 |
| 1 | 0 | 1 | 0 | X | FF8000h - FFFFFFh | 32 kB | Upper 1/512 |
| 1 | 0 | 1 | 1 | 0 | FF8000h - FFFFFFh | 32 kB | Upper 1/512 |
| 1 | 1 | 0 | 0 | 1 | 000000h - 000FFFh | 4 kB | Lower 1/4096 |
| 1 | 1 | 0 | 1 | 0 | 000000h - 001FFFh | 8 kB | Lower 1/2048 |
| 1 | 1 | 0 | 1 | 1 | 000000h - 003FFFh | 16 kB | Lower 1/1024 |
| 1 | 1 | 1 | 0 | X | 000000h - 007FFFh | 32 kB | Lower 1/512 |
| 1 | 1 | 1 | 1 | 0 | 000000h - 007FFFh | 32 kB | Lower 1/512 |

1. X = Don’t care.


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**Table 9. Status Register Memory Protection (CMP = 1)**

| Status Register Bits | | | | | Memory Protection | | |
|---|---|---|---|---|---|---|---|
| BP4 | BP3 | BP2 | BP1 | BP0 | Addresses | Density | Portion |
| X | X | 0 | 0 | 0 | 000000h - FFFFFFh | ALL | ALL |
| 0 | 0 | 0 | 0 | 1 | 000000h – FBFFFFh | 16,128 kB | Lower 63/64 |
| 0 | 0 | 0 | 1 | 0 | 000000h – F7FFFFh | 15,872 kB | Lower 31/32 |
| 0 | 0 | 0 | 1 | 1 | 000000h – EFFFFFh | 15 MB | Lower 15/16 |
| 0 | 0 | 1 | 0 | 0 | 000000h – DFFFFFh | 14 MB | Lower 7/8 |
| 0 | 0 | 1 | 0 | 1 | 000000h – BFFFFFh | 12 MB | Lower 3/4 |
| 0 | 0 | 1 | 1 | 0 | 000000h – 7FFFFFh | 8 MB | Lower 1/2 |
| 0 | 1 | 0 | 0 | 1 | 040000h - FFFFFFh | 16,128 kB | Upper 63/64 |
| 0 | 1 | 0 | 1 | 0 | 080000h - FFFFFFh | 15,872 kB | Upper 31/32 |
| 0 | 1 | 0 | 1 | 1 | 100000h - FFFFFFh | 15 MB | Upper 15/16 |
| 0 | 1 | 1 | 0 | 0 | 200000h - FFFFFFh | 14 MB | Upper 7/8 |
| 0 | 1 | 1 | 0 | 1 | 400000h - FFFFFFh | 12 MB | Upper 3/4 |
| 0 | 1 | 1 | 1 | 0 | 800000h - FFFFFFh | 8 MB | Upper 1/2 |
| X | X | 1 | 1 | 1 | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 1 | 000000h - FFEFFFh | 16,380 kB | Lower 4095/4096 |
| 1 | 0 | 0 | 1 | 0 | 000000h - FFDFFFh | 16,376 kB | Lower 2047/2048 |
| 1 | 0 | 0 | 1 | 1 | 000000h - FFBFFFh | 16,368 kB | Lower 1023/1024 |
| 1 | 0 | 1 | 0 | X | 000000h - FF7FFFh | 16,352 kB | Lower 511/512 |
| 1 | 0 | 1 | 1 | 0 | 000000h - FF7FFFh | 16,352 kB | Lower 511/512 |
| 1 | 1 | 0 | 0 | 1 | 001000h - FFFFFFh | 16,380 kB | Upper 4095/4096 |
| 1 | 1 | 0 | 1 | 0 | 002000h - FFFFFFh | 16,376 kB | Upper 2047/2048 |
| 1 | 1 | 0 | 1 | 1 | 004000h - FFFFFFh | 16,368 kB | Upper 1023/1024 |
| 1 | 1 | 1 | 0 | X | 008000h - FFFFFFh | 16,352 kB | Upper 511/512 |
| 1 | 1 | 1 | 1 | 0 | 008000h - FFFFFFh | 16,352 kB | Upper 511/512 |

1. X = don’t care.


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# 9. Device Identification

Three legacy commands are supported to access device identification; these indicate the manufacturer, device type, and capacity (density). The returned data bytes provide the information, as shown in Table 10 and Table 11.

**Table 10. Manufacturer and Device ID Information for the AT25SL1281C**

| Command | Opcode | Manufacturer ID | First Device ID Byte | Second Device ID Byte |
|---|---|---|---|---|
| Read Manufacturer and Device ID | 9Fh | 1Fh | 69h | 01h |
| Read ID (Legacy Command) | 90h | 1Fh | 69h | |
| Read ID (Quad I/O) | 94h | 1Fh | 69h | |
| Resume from Deep Power-Down and Read Device ID | ABh | | 69h | |

**Table 11. Manufacturer and Device ID Information for the AT25QL1281C**

| Command | Opcode | Manufacturer ID | First Device ID Byte | Second Device ID Byte |
|---|---|---|---|---|
| Read Manufacturer and Device ID | 9Fh | 1Fh | 69h | 81h |
| Read ID (Legacy Command) | 90h | 1Fh | 69h | |
| Read ID (Quad I/O) | 94h | 1Fh | 69h | |
| Resume from Deep Power-Down and Read Device ID | ABh | | 69h | |


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# 10. Commands

All commands, addresses, and data are shifted in and out of the device with the most significant bit on the first rising edge of SCK after $\overline{CS}$ is driven low. Then, the one byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCK.

Every command sequence starts with a one-byte command code. Depending on the command, this can be followed by address bytes, data bytes, or both, or none. $\overline{CS}$ must be driven high after the last bit of the command sequence has been shifted in. For the Read, Fast Read, Read Status Register, Release from Deep Power-Down, and Read Device ID commands, the shifted-in command sequence is followed by a data out sequence. $\overline{CS}$ can be driven high after any bit of the data-out sequence is being shifted out.

For the Page Program, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable, or Deep Power-Down command, $\overline{CS}$ must be driven high exactly at a byte boundary; otherwise, the command is not executed. That is, $\overline{CS}$ must drive high when the number of clock pulses after $\overline{CS}$ being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing happens, and WEL is not reset.


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## 10.1 Command Set Tables

**Table 12. Command Set Table 1 (Standard/Dual/Quad SPI Commands) [1]**

| Command | Byte 1 | Byte 2 | Byte3 | Byte4 | Byte 5 | Byte 6 |
|---|---|---|---|---|---|---|
| Write Enable | 06h | | | | | |
| Volatile SR Write Enable | 50h | | | | | |
| Write Disable | 04h | | | | | |
| Read Status Register 1 | 05h | (SR1 Bit 7–0) [2] | | | | |
| Write Status Register 1 | 01h | (SR1 Bit 7–0) [4] | | | | |
| Read Status Register 2 | 35h | (SR2 Bit 7–0) [2] | | | | |
| Write Status Register 2 | 31h | (SR2 Bit 7–0) | | | | |
| Read Status Register 3 | 15h | (SR3 Bit 7–0) [2] | | | | |
| Write Status Register 3 | 11h | (SR3 Bit 7–0) | | | | |
| Chip Erase | C7h / 60h | | | | | |
| Erase/Program Suspend | 75h | | | | | |
| Erase/Program Resume | 7Ah | | | | | |
| Power-Down | B9h | | | | | |
| Release Power-Down / ID | ABh | Dummy | Dummy | Dummy | (ID7–ID0) [2] | |
| Manufacturer / Device ID | 90h | Dummy | Dummy | 00h | (MF7–MF0) | (ID7–ID0) [2] |
| JEDEC ID | 9Fh | (MF7–MF0) | (ID15–ID8) | (ID7–ID0) [2] | | |
| Enter QPI Mode | 38h | | | | | |
| Enable Reset | 66h | | | | | |
| Reset Device | 99h | | | | | |
| Read Serial Flash Discoverable Parameter | 5Ah | A23–A16 | A15–A8 | A7–A0 | Dummy | (D7–D0) | Next bytes |

| Command | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 – Byte 21 |
|---|---|---|---|---|---|---|
| Read Unique ID | 4Bh | Dummy | Dummy | Dummy | Dummy | (UID127–UID0) |


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**Table 13. Command Set Table 2 (Standard/Dual/Quad SPI Commands) [1]**

| Command | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | Byte 7 | Byte 8 | Byte 9 |
|---|---|---|---|---|---|---|---|---|---|
| Page Program | 02h | A23–A16 | A15–A8 | A7–A0 | D7–D0 [3] | Next bytes | | | |
| Quad Page Program | 32h | A23–A16 | A15–A8 | A7–A0 | D7–D0 [3,9] | Next bytes | | | |
| Block Erase (4kB) | 20h | A23–A16 | A15–A8 | A7–A0 | | | | | |
| Block Erase (32kB) | 52h | A23–A16 | A15–A8 | A7–A0 | | | | | |
| Block Erase (64kB) | D8h | A23–A16 | A15–A8 | A7–A0 | | | | | |
| Read Data | 03h | A23–A16 | A15–A8 | A7–A0 | (D7–D0) | (D7–D0) | Next bytes | | |
| Fast Read | 0Bh | A23–A16 | A15–A8 | A7–A0 | Dummy | (D7–D0) | Next bytes | | |
| Fast Read Dual Output | 3Bh | A23–A16 | A15–A8 | A7–A0 | Dummy | (D7–D0)[7] | Next bytes | | |
| Fast Read Quad Output | 6Bh | A23–A16 | A15–A8 | A7–A0 | Dummy | (D7–D0)[9] | Next bytes | | |
| Erase Security Register [5] | 44h | A23–A16 | A15–A8 | A7–A0 | | | | | |
| Program Security Register [5] | 42h | A23–A16 | A15–A8 | A7–A0 | D7–D0 [3] | Next bytes | | | |
| Read Security Register [5] | 48h | A23–A16 | A15–A8 | A7–A0 | Dummy | (D7–D0) | Next bytes | | |
| Fast Read Dual I/O | BBh | A23–A16 [6] | A15–A8 [6] | A7–A0 [6] | M7–M0 [6] | (D7–D0)[7] | | | |
| Mftr./Device ID Dual I/O | 92h | A23–A16 [6] | A15–A8 [6] | A7–A0 [6] | M7–M0 [6] | (M7–M0) | (D7–D0)[7] | | |
| Set Burst With Wrap | 77h | Dummy | Dummy | Dummy | W8–W0 | | | | |
| Fast Read Quad I/O [10] | EBh | A23–A16 [8] | A15–A8 [3] | A7–A0 [8] | M7–M0 [8] | Dummy | Dummy | (D7–D0)[9] | Next byte |
| Word Read Quad I/O [11, 12] | E7h | A23–A16 [8] | A15–A8 [3] | A7–A0 [8] | M7–M0 [8] | Dummy | (D7–D0)[9] | Next bytes | |
| Mftr./Device ID Quad I/O | 94h | A23–A16 [8] | A15–A8 [3] | A7–A0 [8] | M7–M0 [8] | Dummy | Dummy | (M7–M0)[9] | (ID7–ID0)[9] |

**Table 14. Command Set Table 3 (QPI Commands)**

| Command | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 |
|---|---|---|---|---|---|---|
| Write Enable | 06h | | | | | |
| Volatile SR Write Enable | 50h | | | | | |
| Write Disable | 04h | | | | | |
| Read Status Register 1 | 05h | (SR1 Bit 7–0) [2] | | | | |
| Write Status Register 1 [4] | 01h | (SR1 Bit 7–0) [2] | | | | |
| Read Status Register 2 | 35h | (SR2 Bit 7–0) [2] | | | | |
| Write Status Register 2 | 31h | (SR2 Bit 7–0) [2] | | | | |
| Read Status Register 3 | 15h | (SR3 Bit 7–0) [2] | | | | |
| Write Status Register 3 | 11h | (SR3 Bit 7–0) [2] | | | | |
| Chip Erase | C7h / 60h | | | | | |
| Erase/Program Suspend | 75h | | | | | |
| Erase/Program Resume | 7Ah | | | | | |
| Power-Down | B9h | | | | | |
| Set Read Parameters | C0h | P7–P0 | | | | |
| Release Power-Down / ID | ABh | Dummy | Dummy | Dummy | (ID7–ID0) [2] | |
| Manufacturer / Device ID | 90h | Dummy | Dummy | 00h | (MF7–MF0) [2] | (MF7–MF0) [2] |
| JEDEC ID | 9Fh | (MF7–MF0) [2] | (ID15–ID8) [2] | (ID7–ID0) [2] | | |
| Exit QPI Mode | FFh | | | | | |
| Enable Reset | 66h | | | | | |
| Reset Device | 99h | | | | | |
| Page Program | 02h | A23–A16 | A15–A8 | A7–A0 | D7–D0 [3,9] | Next bytes |
| Block Erase (4kB) | 20h | A23–A16 | A15–A8 | A7–A0 | | |
| Block Erase (32kB) | 52h | A23–A16 | A15–A8 | A7–A0 | | |


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**Table 14. Command Set Table 3 (QPI Commands) *(Continued)***

| Command | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 |
|---|---|---|---|---|---|---|
| Block Erase (64kB) | D8h | A23–A16 | A15–A8 | A7–A0 | | |
| Fast Read | 0Bh | A23–A16 | A15–A8 | A7–A0 | Dummy [14] | (D7–D0) |
| Burst Read With Wrap [15] | 0Ch | A23–A16 | A15–A8 | A7–A0 | Dummy [14] | (D7–D0) |
| Fast Read Quad I/O | EBh | A23–A16 | A15–A8 | A7–A0 | M7–M0 [14] | (D7–D0) |
| Read Serial Flash Discoverable Parameter | 5Ah | A23–A16 | A15–A8 | A7–A0 | Dummy | (D7–D0) |
| Read Security Registers [5] | 48h | A23–A16 [8] | A15–A8 [8] | A7–A0 [8] | Dummy | D7–D0 |
| Erase Security Registers | 44h | A31–A24 | A23–A16 [8] | A15–A8 [8] | A7–A0 [8] | |
| Program Security Registers | 42h | A23–A16 [8] | A15–A8 [8] | A7–A0 [8] | D7–D0 | Next byte |

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "()" indicate data output from the device on 1, 2, or 4 IO pins.
2. The Status Register contents and Device ID repeats continuously until $\overline{CS}$ terminates the command.
3. At least one byte of data input is required for Page Program, Quad Page Program, and Program Security Register, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing wraps to the beginning of the page and overwrites previously sent data.
4. Write Status Register 1 (01h) also can be used to program Status Registers 1 and 2; see the previous tables.
5. Security Register address:

   | | | | |
   |---|---|---|---|
   | Security Register 1 | A23-16 = 00h | A15-8 = 10h | A7-0 = byte address |
   | Security Register 2 | A23-16 = 00h | A15-8 = 20h | A7-0 = byte address |
   | Security Register 3 | A23-16 = 00h | A15-8 = 30h | A7-0 = byte address |

6. Dual SPI address input format:
   $IO_0$ = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   $IO_1$ = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1
7. Dual SPI data output format:
   $IO_0$ = (D6, D4, D2, D0)
   $IO_1$ = (D7, D5, D3, D1)
8. Quad SPI address input format:
   $IO_0$ = A20, A16, A12, A8, A4, A0, M4, M0
   $IO_1$ = A21, A17, A13, A9, A5, A1, M5, M1
   $IO_2$ = A22, A18, A14, A10, A6, A2, M6, M2
   $IO_3$ = A23, A19, A15, A11, A7, A3, M7, M3
9. Quad SPI data input/output:
   $IO_0$ = (D4, D0…)
   $IO_1$ = (D5, D1…)
   $IO_2$ = (D6, D2…)
   $IO_3$ = (D7, D3…)
10. Fast Read Quad I/O data output format:
    $IO_0$ = (x, x, x, x, D4, D0, D4, D0)
    $IO_1$ = (x, x, x, x, D5, D1, D5, D1)
    $IO_2$ = (x, x, x, x, D6, D2, D6, D2)
    $IO_3$ = (x, x, x, x, D7, D3, D7, D3)
11. Word Read Quad I/O data output format:
    $IO_0$ = (x, x, D4, D0, D4, D0, D4, D0)
    $IO_1$ = (x, x, D5, D1, D5, D1, D5, D1)
    $IO_2$ = (x, x, D6, D2, D6, D2, D6, D2)
    $IO_3$ = (x, x, D7, D3, D7, D3, D7, D3)
12. For Word Read Quad I/O, the lowest address bit must be 0. (A0 = 0)
13. QPI command, address, data input/output format:

    | CLK# | 0,1 | 2,3 | 4,5 | 6,7 | 8,9 | 10,11 |
    |---|---|---|---|---|---|---|
    | $IO_0$ = | C4,C0 | A20,A16 | A12,A8 | A4,A0 | D4,D0 | D4,D0 |
    | $IO_1$ = | C5,C1 | A21,A17 | A13,A9 | A5,A1 | D5,D1 | D5,D1 |
    | $IO_2$ = | C6,C2 | A22,A18 | A14,A10 | A6,A2 | D6,D2 | D6,D2 |


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$IO_3$ = C7,C3 A23,A19 A15,A11 A7,A3 D7,D3 D7,D3

14. The number of dummy clocks for QPI Fast Read, QPI Fast Read Quad I/O, and QPI Burst Read with Wrap is controlled by the read parameter P7-P4.
15. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3-P0.

**Table 15. Commands that must send Write Enable/Write Enable for the Volatile Status Register Command**

| Command | | Write |
|---|---|---|
| Write Status Register | 01h / 31h / 11h | 06h / 50h |
| Erase Security Register | 44h | 06h |
| Program Security Register | 42h | 06h |
| Page Program | 02h | 06h |
| Quad Page Program | 32h | 06h |
| 4 kB Block Erase | 20h | 06h |
| 32 kB Block Erase | 52h | 06h |
| 64 kB Block Erase | D8h | 06h |
| Chip Erase | 60h / C7h | 06h |


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## 10.2 Write Enable (06h)

Write Enable command is for setting the Write Enable Latch (WEL) bit in the Status Register. The WEL bit must be set before every Program, Erase and Write Status Register command. To enter the Write Enable command, $\overline{CS}$ goes low before the command (06h) being driven onto the SI pin on the rising edge of SCK, and then driving $\overline{CS}$ high.

Note that the Write Enable command sent is not accepted when the Write Enable for Volatile Status Register command is valid. Thus, if it is not known if the Write Enable for Volatile Status Register command is valid, send the Write Disable command before sending the Write Enable command.

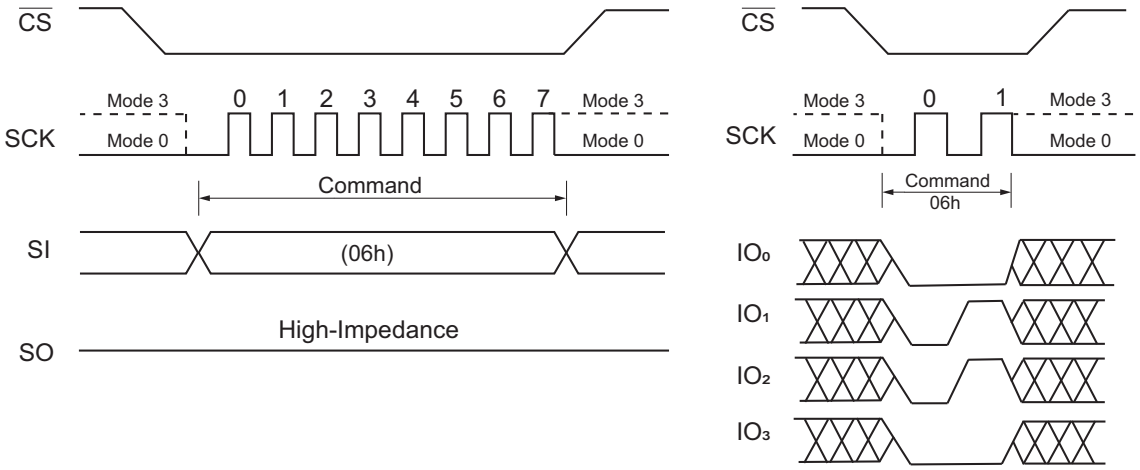


**Figure 9. Write Enable Command for SPI Mode (left) and QPI Mode (right)**


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## 10.3 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits can also be written to as volatile bits (DC, HOLD/RST, DRV1, DRV0, CMP, QE, SRP1, SRP0, BP4, BP3, BP2, BP1, BP0). This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command does not set the Write Enable Latch bit, it is only valid for the Write Status Registers command to change the volatile Status Register bit values. (After the software/hardware reset or power-down/up, the volatile Status Register bit values are restored to the default value or the value input by the Write Enable command.)

Note that the Write Enable command sent is not accepted when the Write Enable for Volatile Status Register command is valid. Thus, if it is not known if the Write Enable for Volatile Status Register command is valid, send the Write Disable command before sending the Write Enable command.

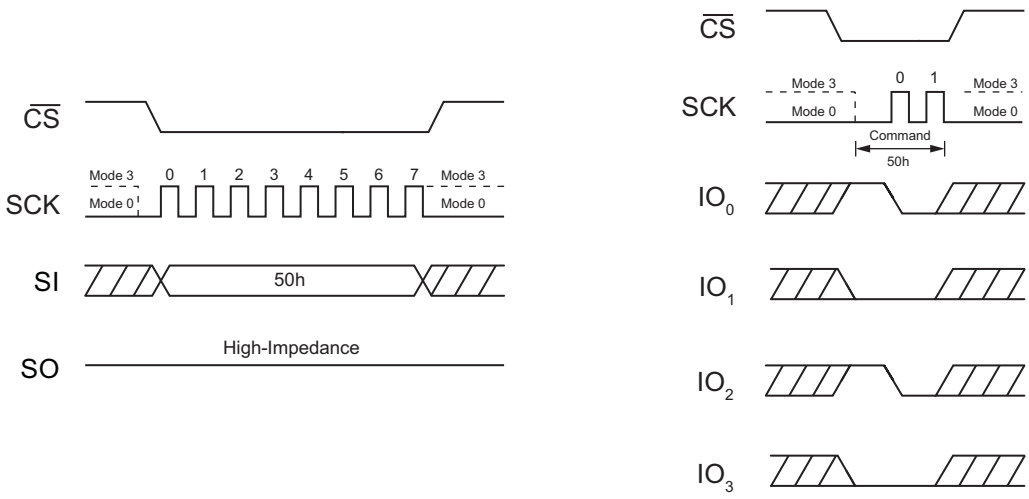


**Figure 10. Write Enable for Volatile Status Register Command for SPI Mode (left) and QPI Mode (right)**


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## 10.4 Write Disable (04h)

The Write Disable command resets the Write Enable Latch (WEL) bit in the Status Register or invalidate the Write Enable for Volatile Status Register command. To enter the Write Disable command, $\overline{CS}$ goes low before the command 04h being driven onto the SI pin on the rising edge of SCK, and then driving $\overline{CS}$ high. The WEL bit is reset by the following condition: power-up and upon completion of the Write Status Register, Page Program, Block Erase and Chip Erase, Program/Erase Security Registers, and Reset commands.

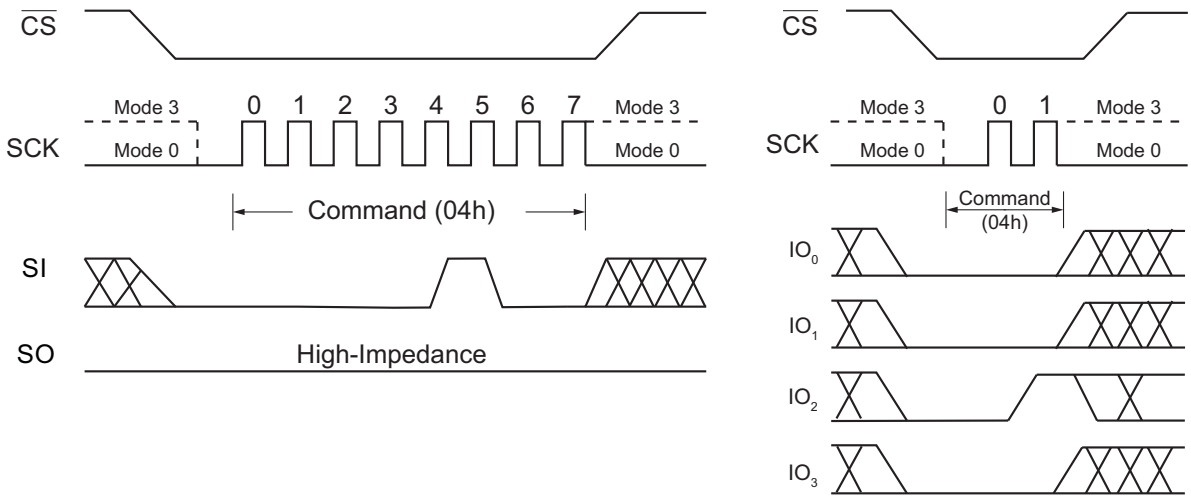


**Figure 11. Write Disable Command for SPI Mode (left) and QPI Mode (right)**


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## 10.5 Read Status Register (05h or 35h or 15h)

The Read Status Register commands 05h, 35h, 15h are used to read Status Registers 1, 2, and 3, respectively. The Read Status Register can be read at any time (even in program/erase/write Status Register and Write Security Register condition). It is recommended to check the RDY/BSY bit before sending a new command. Also, it is possible to read the Status Register continuously. For 05h, the SO outputs bits of Status Register 1; for 35h, the SO outputs Status Register 2; for 15h, the SO outputs Status Register 3.

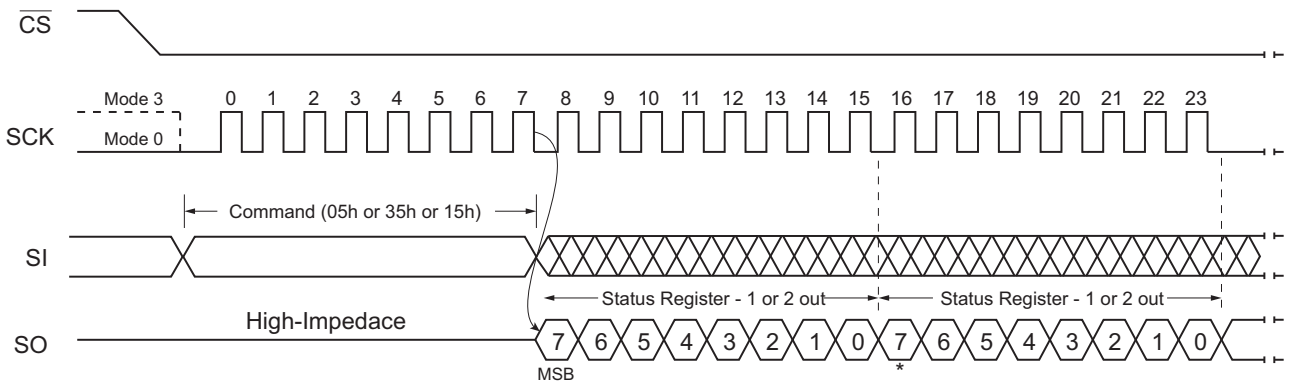


**Figure 12. Read Status Register Command (SPI Mode)**

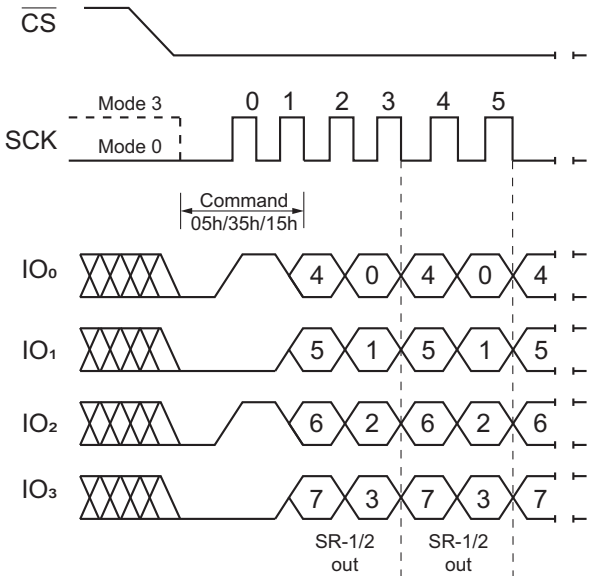


**Figure 13. Read Status Register Command (QPI Mode)**


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## 10.6 Write Status Register (01h or 31h or 11h)

The Write Status Register command allows the Status Registers to be written. Status Register-1 can be written by the Write Status Register 01h command; Status Register-2 can be written by the Write Status Register 01h or 31h command; Status Register-3 can be written by the Write Status Register 11h command. When the Write Status Register command 01h is followed by one byte of data, the data is written to Status Register-1. When the Write Status Register command 01h is followed by two bytes of data, the first byte data is written to Status Register-1, and the second byte data is written to Status Register-2. Write Status Register command 31h or 11h can only be followed by one byte of data; the data is written to Status Register-2 or Status Register-3, respectively. The writable Status Register bits include: SRP0, BP[4:0] in Status Register-1; CMP, LB[3:1], QE, SRP1 in Status Register- 2; DRV1, DRV0, HLD/RST, DC in Status Register- 3. All other Status Register bit locations are read-only and are not affected by the Write Status Register command. LB[3:1] are non-volatile OTP bits; once set to 1, they cannot be cleared to 0.

The Write Status Register command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable or Write Enable For Volatile SR command must previously have been executed. After the Write Enable command has been decoded and executed, the device sets the Write Enable Latch (WEL) bit.

The Write Status Register command has no effect on SUS1, SUS2, WEL, and RDY/BSY bits of the Status Register. $\overline{CS}$ must be driven high after the 8 or 16 bit of the data byte have been latched in. If not, the Write Status Register command is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Write Status Register cycle (whose duration is $t_W$) is initiated. While the Write Status Register cycle is in progress, the Status Register can be read to check the value of the Ready/Busy (RDY/BSY) bit. The Ready/Busy (RDY/BSY) bit is 1 during the self-timed Write Status Register cycle; it is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register command lets the user change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area. The Write Status Register command also lets the user set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the $\overline{WP}$ signal. The Status Register Protect (SRP1 and SRP0) bits and $\overline{WP}$ signal allow the device to be put in the Hardware Protected Mode. The Write Status Register command is not executed once the Hardware Protected Mode is entered.

The sequence of issuing a Write Status Register command is: $\overline{CS}$ goes low→ send Write Status Register command code→ Status Register data on SI→$\overline{CS}$ goes high.

The $\overline{CS}$ must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the command is not executed. The self-timed Write Status Register cycle time ($t_W$) is initiated as soon as $\overline{CS}$ goes high. The Ready/Busy (RDY/BSY) bit still can be checked while the Write Status Register cycle is in progress. The RDY/BSY is set 1 during the $t_W$ timing; it is set 0 when the Write Status Register cycle is completed and the Write Enable Latch (WEL) bit is reset.

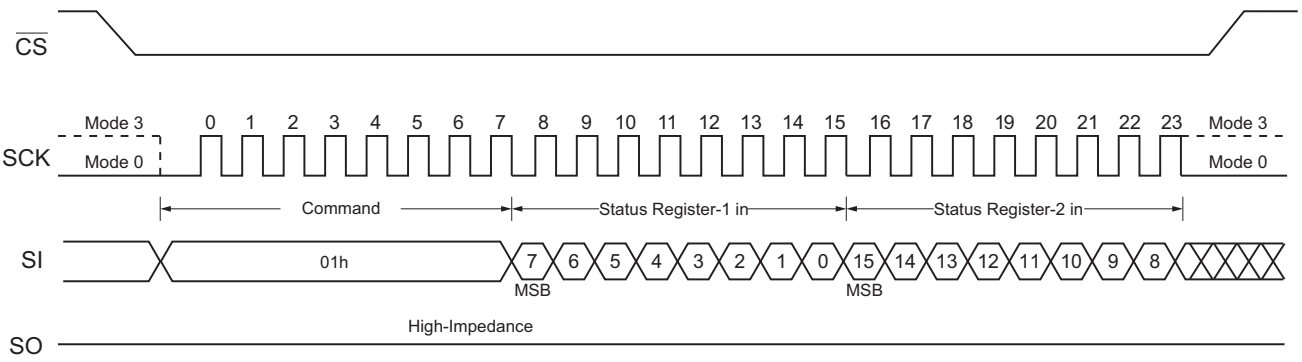


**Figure 14. Write Status Register Command (SPI Mode)**


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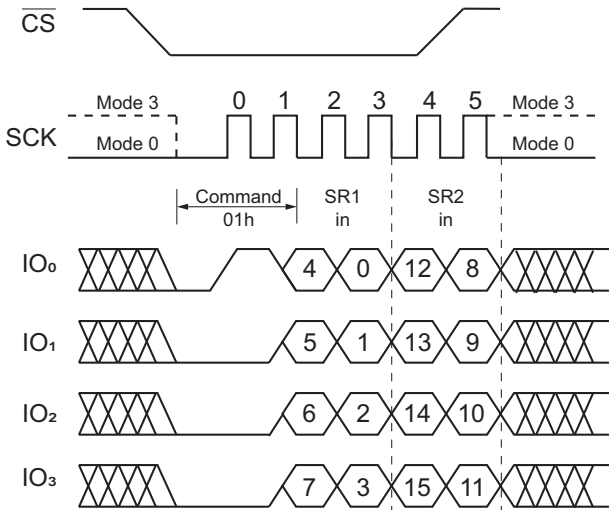


**Figure 15. Write Status Register Sequence Diagram - 01h 2-byte (QPI Mode)**

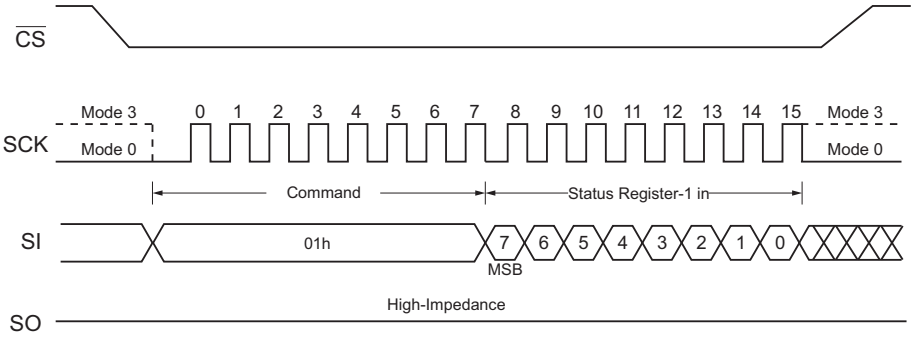


**Figure 16. Write Status Register Diagram - 01h/31h/11h 1-byte (SPI Mode)**

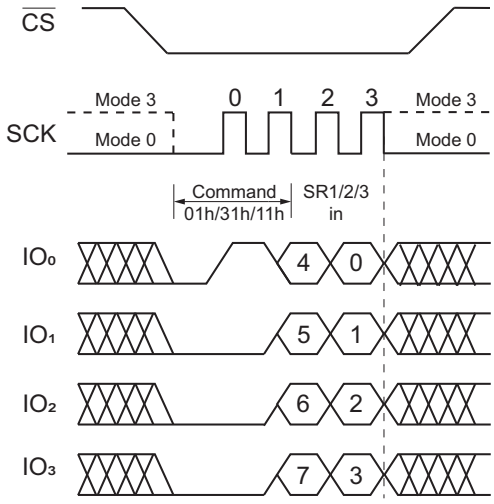


**Figure 17. Write Status Register Diagram - 01h/31h/11h 1-byte (QPI Mode)**


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## 10.7 Enable QPI (38h)

The AT25SL1281C / AT25QL1281C supports both the Standard/Dual/Quad Serial Peripheral interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. The Enable QPI command is used to switch the device from SPI mode to QPI mode.

To switch the device to QPI mode, the Quad Enable (QE) bit in Status Register 2 must be set, followed by an Enable QPI command. If the Quad Enable (QE) bit is 0 (default for the AT25SL1281C), the Enable QPI command is ignored and the device remains in SPI mode.

After power-up, the default state of the device is SPI mode. See Table 12 and Table 13 for all the commands supported in SPI mode; see the Table 14 for all the commands supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting remains unchanged.

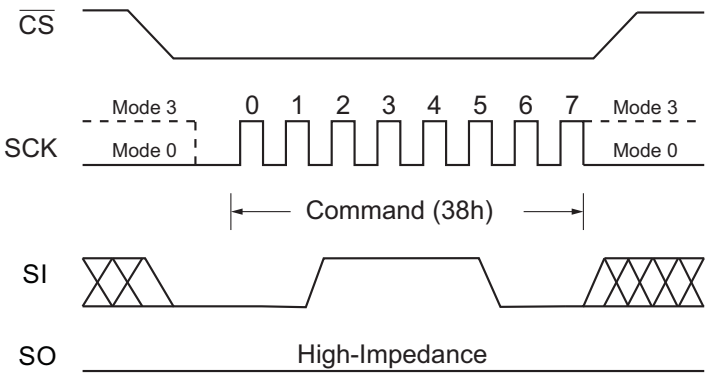


**Figure 18. Enable QPI Command (SPI Mode only)**

## 10.8 Disable QPI (FFh)

By issuing a Disable QPI (FFh) command, the device is reset to SPI mode. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length settings remains unchanged.

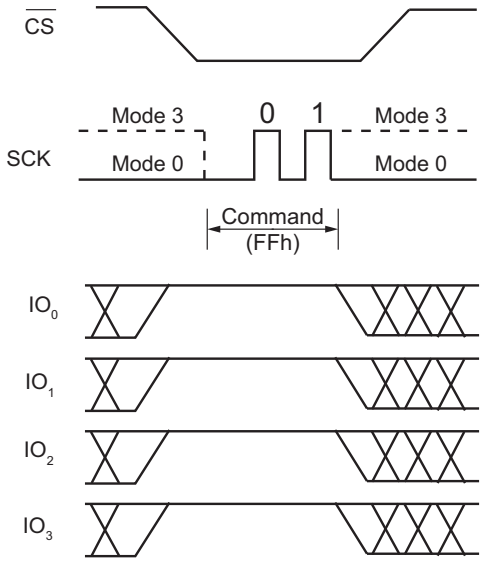


**Figure 19. Disable QPI Command for QPI Mode**


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## 10.9 Enable Reset (66h) and Reset (99h)

For eight-pin packages, the AT25SL1281C / AT25QL1281C provide a software Reset command (99h) instead of a dedicated RESET pin.

Once the Reset command is accepted, any on-going internal operations are terminated and the device returns to its default power-on state and loses all current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting, Read parameter setting and Wrap bit setting.

The Enable Reset (66h) and Reset (99h) commands can be issued in either SPI mode or QPI mode. To avoid accidental reset, both commands must be issued in sequence. The execution of any command other than Reset (99h) after the Reset Enable (66h) command is executed disables the reset enable state. A new sequence of Enable Reset (66h) and Reset (99h) would then be required to reset the device. Once the Reset command is accepted by the device, it takes approximately $t_{RST}$ to reset. During this period, no command is accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by device. It is recommended to check the RDY/BSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

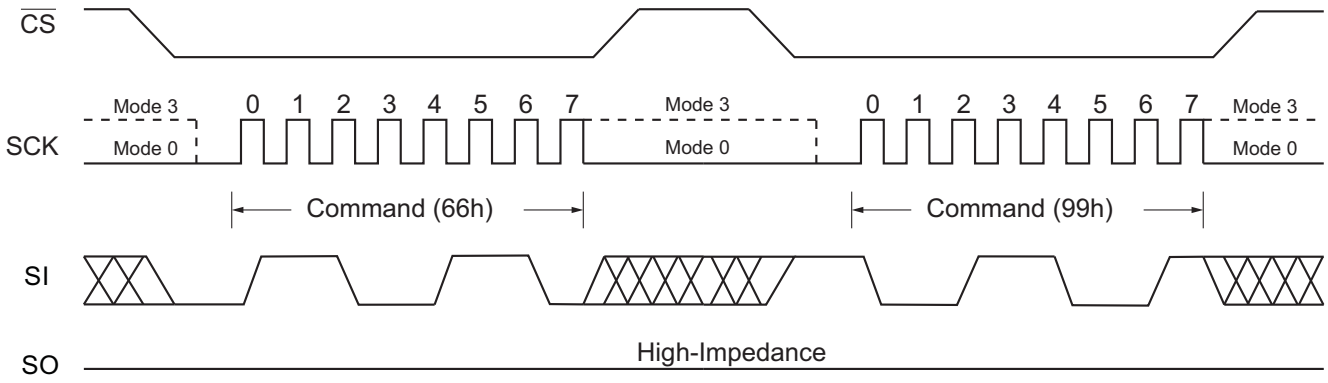


**Figure 20. Enable Reset and Reset Command (SPI Mode)**

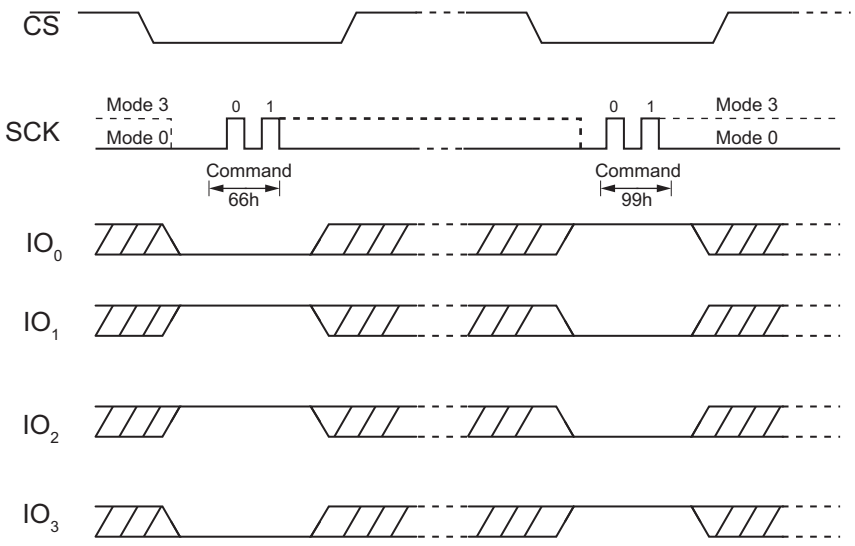


**Figure 21. Enable Reset and Reset Command (QPI Mode)**


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## 10.10 Read Data (03h)

The Read Data command is used to read data out from the device. The command is initiated by driving the $\overline{CS}$ pin low and then sending the command code 03h, followed by a 24-bit address (A23- A0), onto the SI pin. After the address is received, the data byte of the addressed memory location is shifted out on the SO pin at the falling edge of SCK with the most significant bit (MSB) first. The address is automatically incremented to the next higher address and the next byte of data is shifted out, allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues.

The command is completed by driving $\overline{CS}$ high. The Read Data command sequence is shown in Figure 22. If a Read Data command is issued while an Erase, Program, or Write Status Register cycle is in process (RDY/BSY = 1) the command is ignored and does not effect the current cycle. The Read Data command allows clock rates from D.C to a maximum of $f_R$ (see Section 11.7, AC Electrical Characteristics).

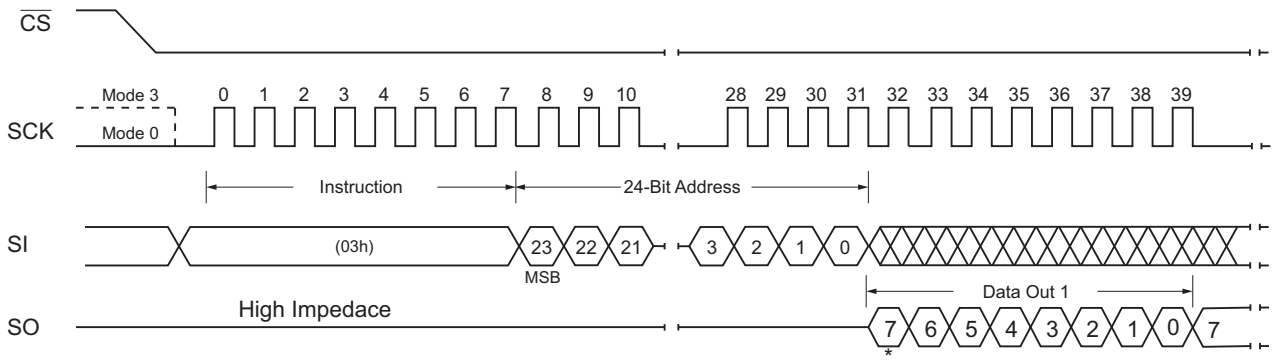


**Figure 22. Read Data Command**


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## 10.11 Fast Read (0Bh)

The Fast Read command is a high speed reading mode that can operate at the highest possible frequency of $F_R$. The address is latched on the rising edge of the SCK. After the 24-bit address, eight dummy clocks are shifted in (Figure 23). The dummy clocks allow the internal circuits the time required to set up the initial address. During the dummy clocks, the data value on the SO pin is a “don’t care”. Data of each bit shifts out on the falling edge of SCK.

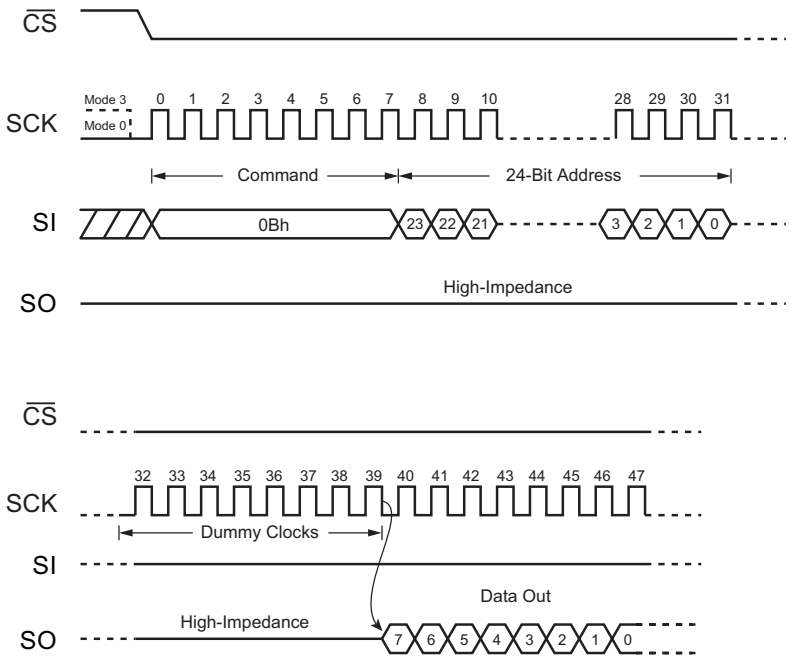
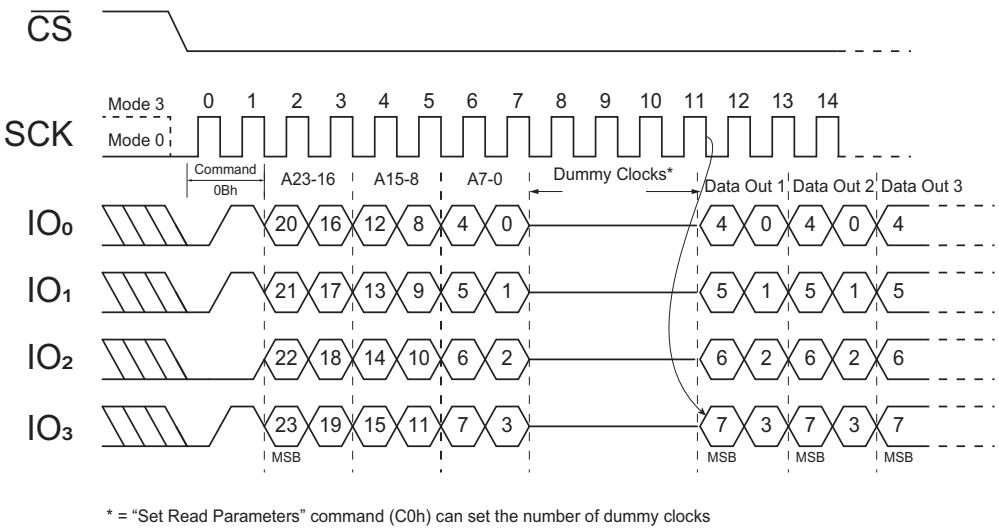



**Figure 23. Fast Read Command (SPI Mode)**

### 10.11.1 Fast Read in QPI Mode

When QPI mode is enabled, the number of dummy clock is configured by the Set Read Parameters (C0h) command to accommodate a wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. The number of dummy clock cycles can be configured as either 4, 6 or 8 by setting bits P[5:4] in the 8-bit parameter of the Set Read Parameters (C0h) command, as shown in Table 18. The default number of dummy clocks upon power-up or after a Reset command is 4. See Figure 24.




* = “Set Read Parameters” command (C0h) can set the number of dummy clocks

**Figure 24. Fast Read Command (QPI Mode)**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## 10.12 Fast Read Dual Output (3Bh)

By using two pins ($IO_0$ and $IO_1$, instead of just $IO_0$), the Fast Read Dual Output command allows data to be transferred from the AT25SL1281C / AT25QL1281C at twice the rate of standard SPI devices. The Fast Read Dual Output command is ideal for quickly downloading code from Flash to RAM upon power-up or for application that cache code-segments to RAM for execution.

The Fast Read Dual Output command can operate at the highest possible frequency of $F_R$ (see Section 11.7, AC Electrical Characteristics). After the 24-bit address, eight dummy clocks are driven on the SI pin, as shown in Figure 25. The dummy clocks allow the internal circuits the time required for setting up the initial address. During the dummy clocks, the data value on the SO pin is a “don’t care”. However, ensure the $IO_0$ pin is high-impedance before the falling edge of the first data out clock.

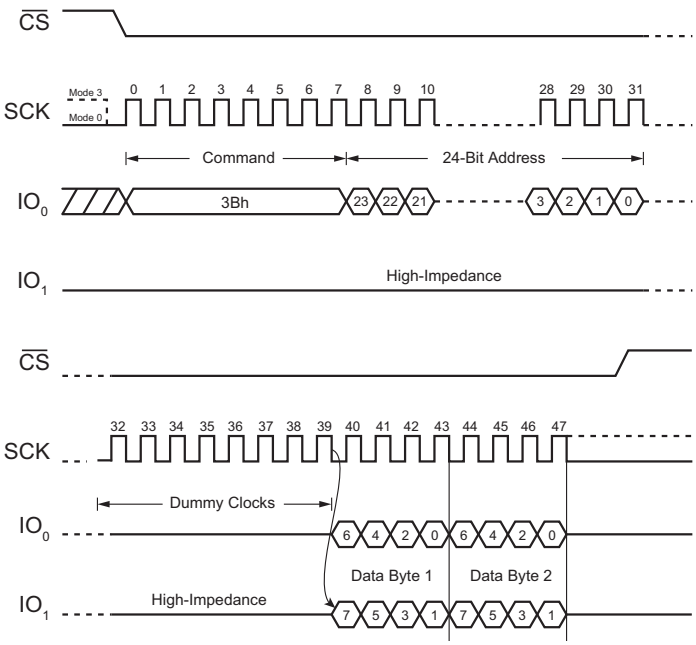


**Figure 25. Fast Read Dual Output command (SPI Mode)**


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## 10.13 Fast Read Quad Output (6Bh)

By using four pins ($IO_0$, $IO_1$, $IO_2$, and $IO_3$), the Fast Read Quad Output command allows data to be transferred from the AT25SL1281C / AT25QL1281C at four times the rate of standard SPI devices. Before executing the 6Bh command, the Quad Enable (QE) bit of Status Register 2 must be set.

The Fast Read Quad Output command can operate at the highest possible frequency of $F_R$ (see Section 11.7, AC Electrical Characteristics). This is done by adding eight dummy clocks after the 24- bit address, as shown in Figure 26. The dummy clocks allow the internal circuits the time required to set up the initial address. During the dummy clocks, the data value on the SO pin is a “don’t care”. However, ensure the $IO_0$ pin is high-impedance before the falling edge of the first data out clock.

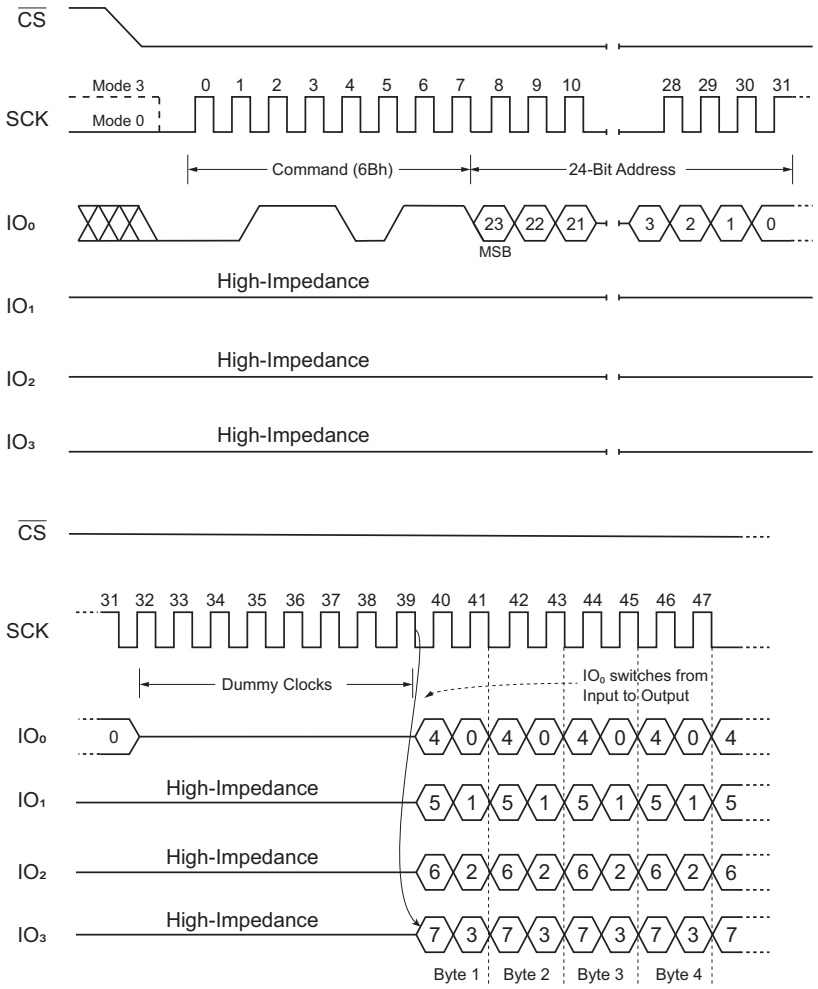


**Figure 26. Fast Read Quad Output Command (SPI Mode)**


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## 10.14 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O command reduces cycle overhead by using two IO pins: $IO_0$ and $IO_1$ to transfer data.

### 10.14.1 Continuous Read Mode

The Fast Read Dual I/O command supports a continuous read mode using the Mode bits (M7-0), which are shifted into the device after address bits (A23-0). Bits M5-4 of the Mode bits control whether an opcode is required in a subsequent command. If M5-4 are 1,0 then subsequent Fast Read Dual I/O command does not require an opcode, as shown in Figure 28. In this case the device enters continuous read mode and opcode BBh is implicitly used for the command. This reduces the command sequence by eight clocks and allows the address to be immediately entered after $\overline{CS}$ is asserted low.

If bits M5-4 of the Mode bits have any value other 1,0, the subsequent command requires an opcode as shown in Figure 27. In case the device is in continuous read mode, it will exit this mode and resume normal operation. At this point any command can be sent to the device.

Note: All Mode bits other than M5-4 are don't care ("X"). However, ensure the I/O pins are high-impedance before the falling edge of the first data out clock.

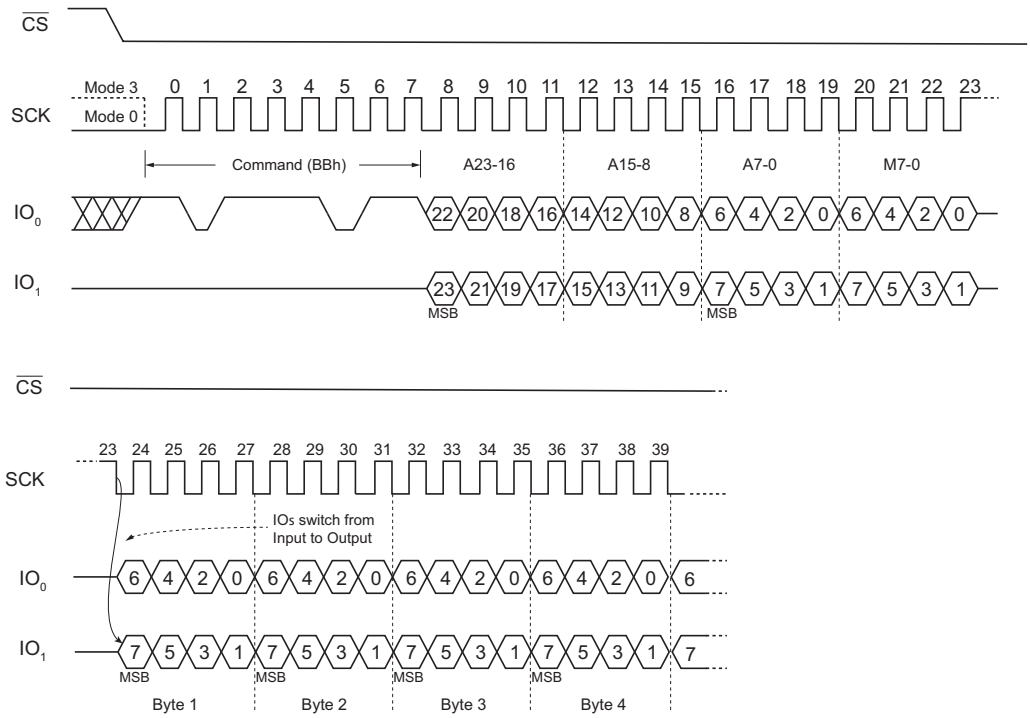


**Figure 27. Fast Read Dual I/O Command (first time or after previous command has Mode bits M5-4 not equal to 1,0)**


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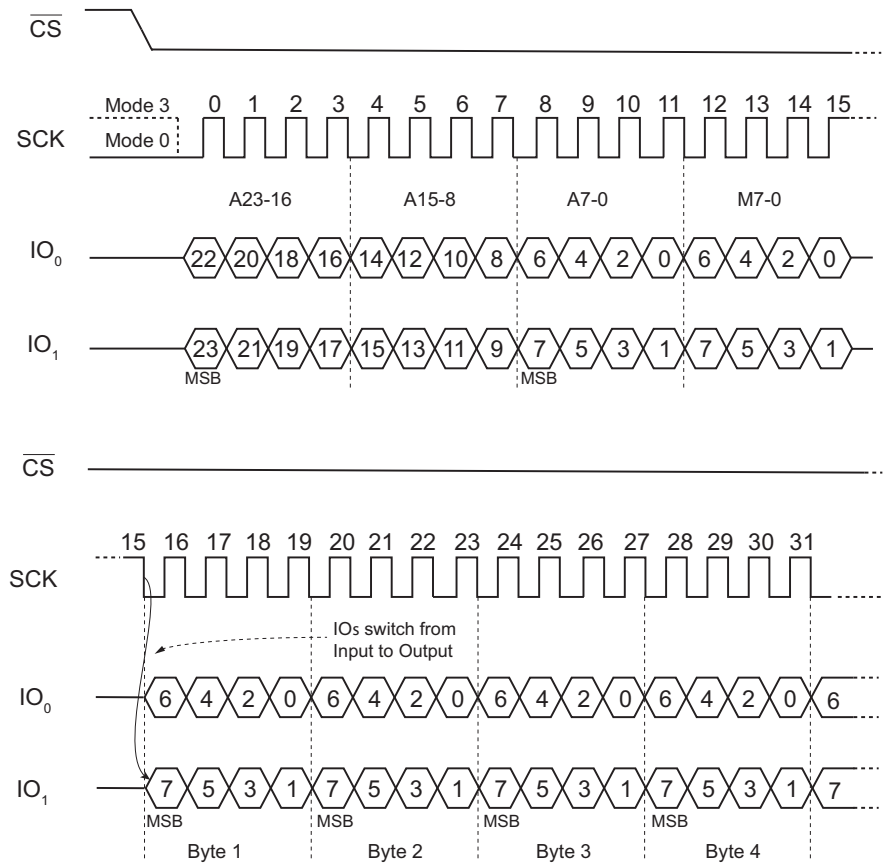


**Figure 28. Fast Read Dual I/O Sequence Diagram (previous M5-4 = 1,0) SPI Mode Only**


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## 10.15 Fast Read Quad I/O (EBh)

The Quad I/O Fast Read command has the capability to input the 3-byte address (A23-0) and output the data through the $IO_0$, $IO_1$, $IO_2$, and $IO_3$ signals, at four bits per clock cycle. The Quad Enable bit (QE) of the Status Register must be set to enable the Quad I/O Fast read command.

### 10.15.1 Continuous Read Mode

The Fast Read Quad I/O command supports a continuous read mode using the Mode bits (M7-0), which are shifted into the device after address bits (A23-0). Bits M5-4 of the Mode bits control whether an opcode is required in a subsequent command. If M5-4 are 1,0 then subsequent Fast Read Quad I/O command does not require an opcode, as shown in Figure 30. In this case the device enters continuous read mode and opcode EBh is implicitly used for the command. This reduces the command sequence by eight clocks and allows the address to be immediately entered after $\overline{CS}$ is asserted low.

If bits M5-4 of the Mode bits have any value other 1,0, the subsequent command requires an opcode as shown in Figure 29. In case the device is in continuous read mode, it will exit this mode and resume normal operation. At this point any command can be sent to the device.

Note: All Mode bits other than M5-4 are don't care ("X"). However, ensure the I/O pins are high-impedance before the falling edge of the first data out clock.

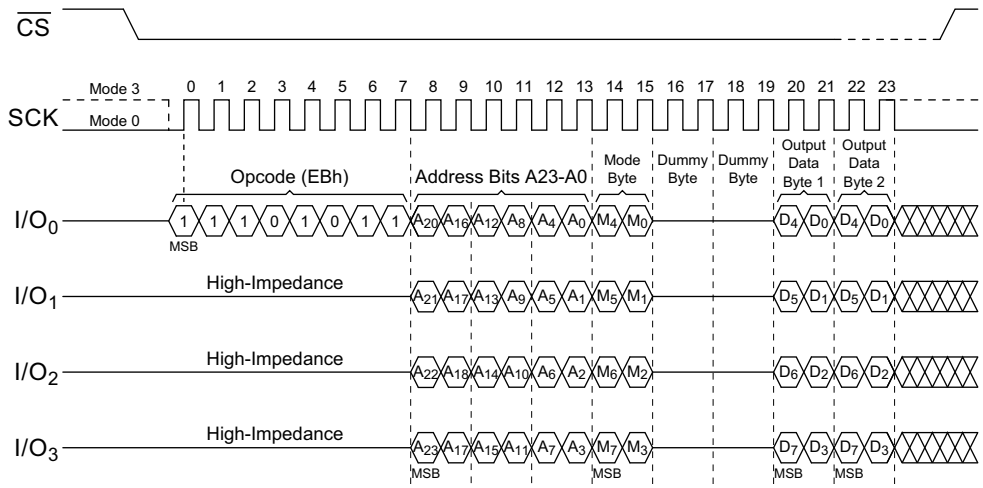


**Figure 29. Fast Read Quad I/O Command (first time or after previous command has mode bits M5-4 not equal to 1,0; SPI Mode)**

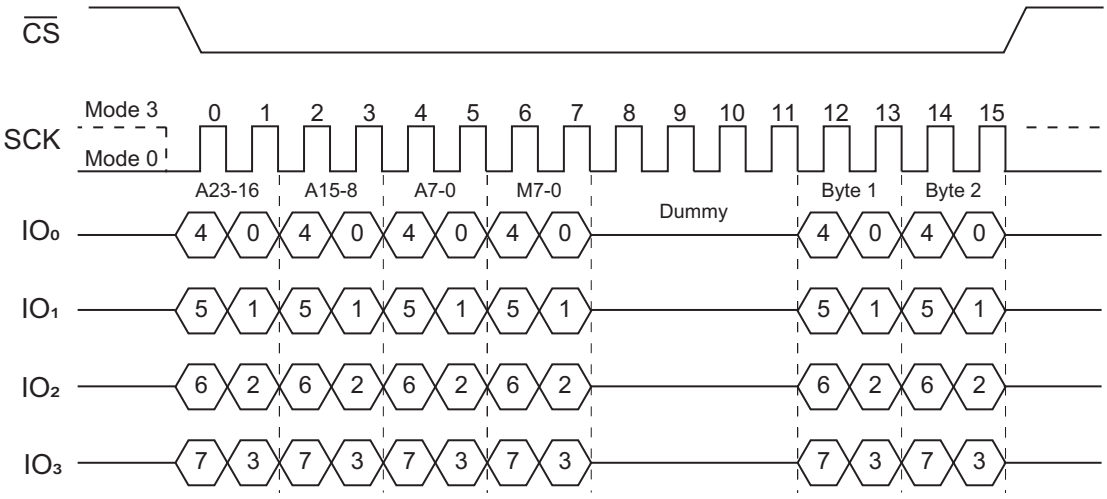


**Figure 30. Fast Read Quad I/O Command (initial command or previous M5-4 = 1,0; SPI mode)**


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### 10.15.2 Quad I/O Fast Read with 8/16/32/64-Byte Wrap Around

The Quad I/O Fast Read command also can be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) command before EBh. The Set Burst with Wrap (77h) command can either enable or disable the Wrap Around feature for the following EBh commands. When Wrap Around is enabled, the data accessed can be limited to either an 8-, 16-, 32-, or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the command. Once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. (See Section 10.17, Set Burst with Wrap (77h).)

The Set Burst with Wrap command allows three Wrap Bits, W6-4, to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-5 are used to specify the length of the wrap around section within a page.

### 10.15.3 Fast Read Quad I/O in QPI Mode

When QPI mode in enabled, the number of dummy clocks is configured by the Set Read Parameters (C0h) command to accommodate a wide range applications with different needs for either maximum fast read frequency or minimum data access latency. The number of dummy clock cycles can be configured as either 4, 6, or 8 by setting bits P[5:4] in the 8-bit parameter of the Set Read Parameters (C0h) command, as shown in Table 18. The default number of dummy clocks upon power-up or after a Reset (99h) command is four.

The Continuous Read Mode feature is also available in QPI mode for Fast Read Quad I/O command. Note that in QPI mode, the Mode bits M7-M0 are included in the dummy clock cycle count.

The Wrap Around feature is not available in QPI mode for Fast Read Quad I/O command. To perform a read operation with fixed data length wrap around in QPI mode, a Burst Read with Wrap (0Ch) command must be used. See Section 10.19, Burst Read with Wrap (0Ch).

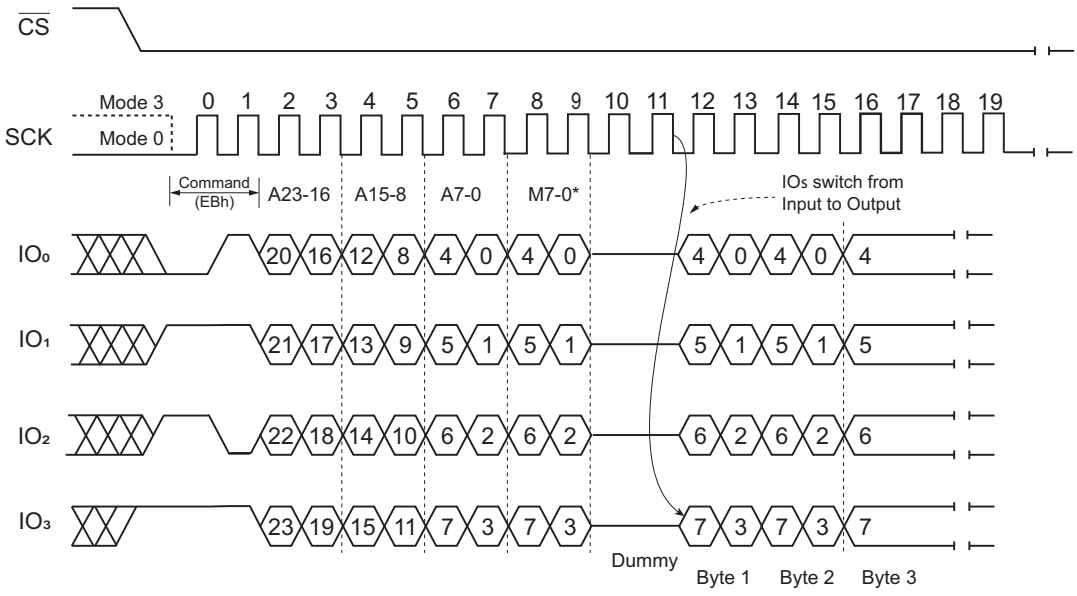


**Figure 31. Fast Read Quad I/O Command (first time or after previous command has mode bits M5-4 not equal to 1,0; QPI mode)**


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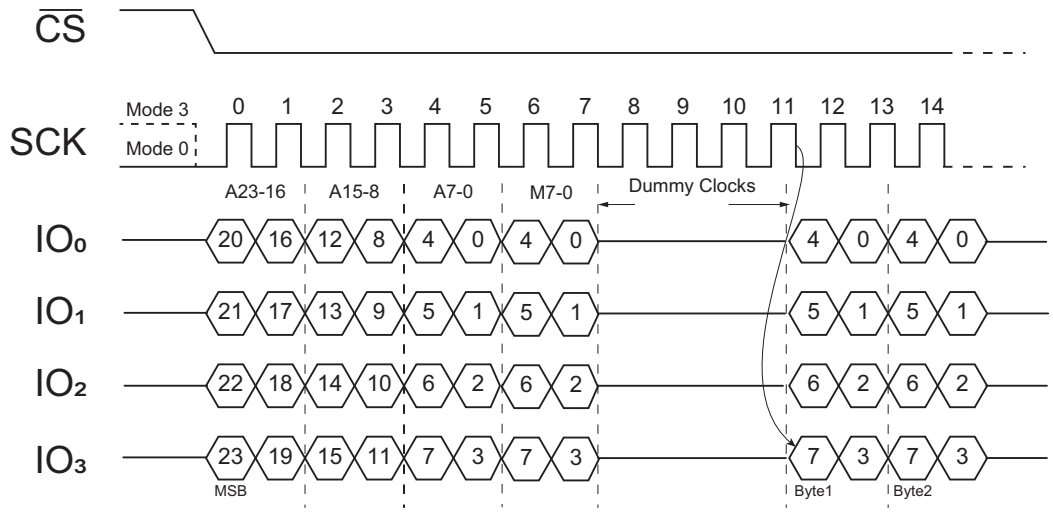


**Figure 32. Fast Read Quad I/O Command (Initial command or previous M5-4 = 1,0; QPI mode)**


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## 10.16 Word Read Quad I/O (E7h)

The Quad I/O significantly reduces command overhead, allowing faster random access for code execution (XiP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O command. The lowest Address bit (A0) must equal 0 and only two dummy clocks are required before the data output.

### 10.16.1 Continuous Read Mode

The Word Read Quad I/O command can further reduce command overhead through setting the Continuous Read Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 33. If the “Continuous Read Mode” bits M[7-4] = Ah, then the next Fast Read Quad I/O command (after $\overline{CS}$ is raised and then lowered) does not require the E7h command code, as shown in Figure 34. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after $\overline{CS}$ is asserted low. If the Continuous Read Mode bits M[5:4] do not equal to (1,0), the next command (after $\overline{CS}$ is raised and then lowered) requires the first E7h command code; thus, returning to normal operation.

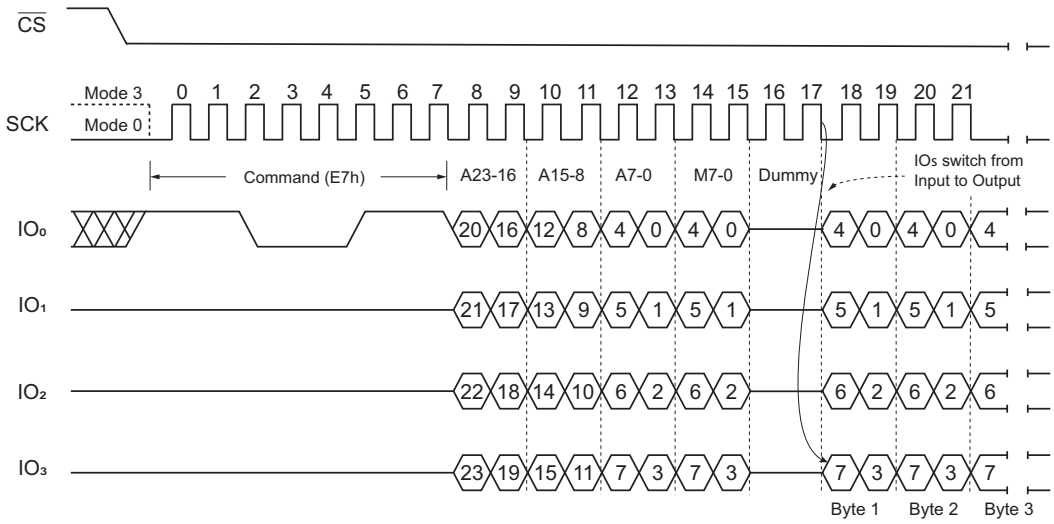


**Figure 33. Word Read Quad I/O Command (Initial command or previous set M5-4 ≠ 1,0; SPI Mode)**

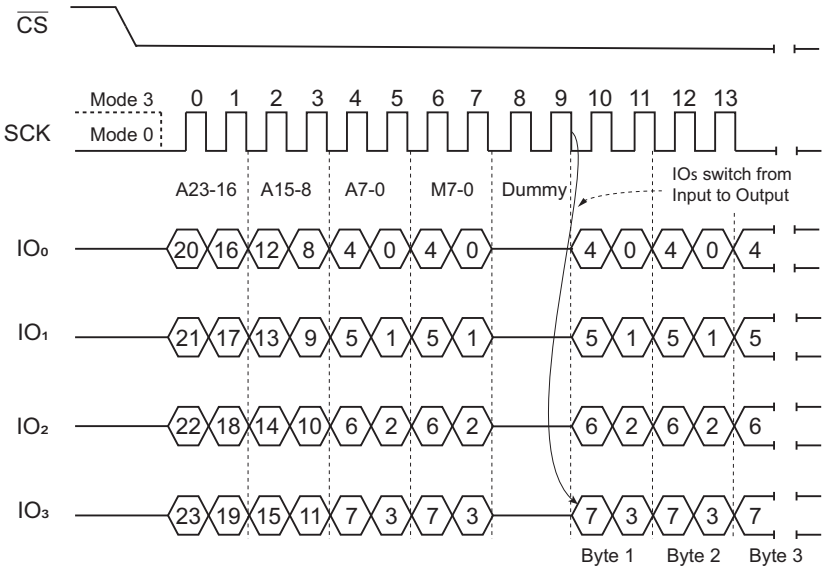


**Figure 34. Word Read Quad I/O Command (Previous command set M5-4 = 1,0; SPI Mode)**


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### 10.16.2 8/16/32/64-Byte Wrap Around in SPI mode

The Word Read Quad I/O command can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) command before E7h. The Set Burst with Wrap command can either enable or disable the Wrap Around feature for the following E7h commands. When Wrap Around is enabled, the output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing read commands.

The Set Burst with Wrap command allows three wrap bits, W6-4, to be set. The W4 bit is used to enable or disable the Wrap Around operation, while W6-5 is used to specify the length of the wrap around section within a page.


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## 10.17 Set Burst with Wrap (77h)

The Set Burst with Wrap command is used in conjunction with the EBh, E7h commands to access a fixed 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap command sequence is: $\overline{CS}$ goes low → Send Set Burst with Wrap command → Send 24 Dummy bits → Send 8 wrap bits" → $\overline{CS}$ goes high.

If W6-4 is set by a Set Burst with Wrap command, all the following EBH, E7H commands use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the Wrap Around function and return to normal read operation, another Set Burst with Wrap command must be issued to set W4=1. The default value of W4 at power on is 1.

**Table 16. Encoding of W6 - W4 Wrap Bits**

| W6, W5 | W4 = 0 | | W4 = 1(Default) | |
|---|---|---|---|---|
| | Wrap Around | Wrap Length | Wrap Around | Wrap Length |
| 0 0 | Yes | 8-byte | No | N/A |
| 0 1 | Yes | 16-byte | No | N/A |
| 1 0 | Yes | 32-byte | No | N/A |
| 1 1 | Yes | 64-byte | No | N/A |

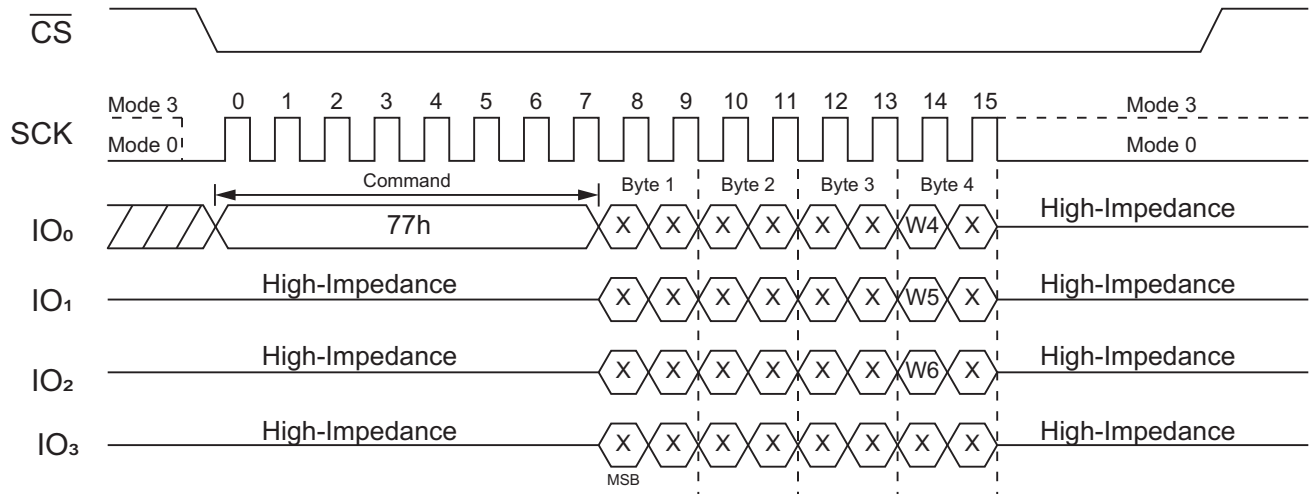


**Figure 35. Set Burst with Wrap Command Sequence, SPI Only**


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## 10.18 Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, the Set Read Parameters (C0h) command can be used to configure the number of dummy clocks for the Fast Read (0Bh), Fast Read Quad I/O (EBh), and Burst Read with Wrap (0Ch) commands, and to configure the number of bytes of wrap length for the Burst Read with Wrap (0Ch) command.

**Table 17. Commands that Configure Number of Dummy Clocks**

| Mode | Command | |
|---|---|---|
| QPI | Fast Read | 0Bh |
| | Fast Read Quad I/O | EBh |
| | Burst Read with Wrap | 0Ch |
| | Read Security Registers | 48h |
| | Read Serial Flash Discoverable Parameter | 5Ah |

In Standard SPI mode, the Set Read Parameters (C0h) command is not accepted. The dummy clocks for various Fast Read commands in Standard/Dual/Quad SPI mode are fixed. The wrap length is set by the W5-W4 bits in the Set Burst with Wrap (77h) command. This setting remains unchanged when the device is switched from Standard SPI mode to QPI mode.

The default wrap length after a power-up or a Reset command is 8 bytes, and the default number of dummy clocks is 4. The number of dummy clocks is only programmable for 0BH, EBH, 0CH, 48H, and 5AH commands in the QPI mode. Whenever the device is switched from SPI mode to QPI mode, the number of dummy clocks must be set again, prior to any 0BH, EBH, 0CH, 48H, and 5AH commands.

**Table 18. Encoding of the P[5:4] Bits**

| P5, P4 | Dummy Clocks | Maximum Read Frequency |
|---|---|---|
| 00 | 4 | 80 MHz |
| 01 | 6 | 108 MHz |
| 10 | 8 | 120 MHz |
| 11 | 10 | 133 MHz |

**Table 19. Encoding of the P[1:0] Bits**

| P1, P0 | Wrap Length |
|---|---|
| 0 0 | 8-byte |
| 0 1 | 16-byte |
| 1 0 | 32-byte |
| 1 1 | 64-byte |


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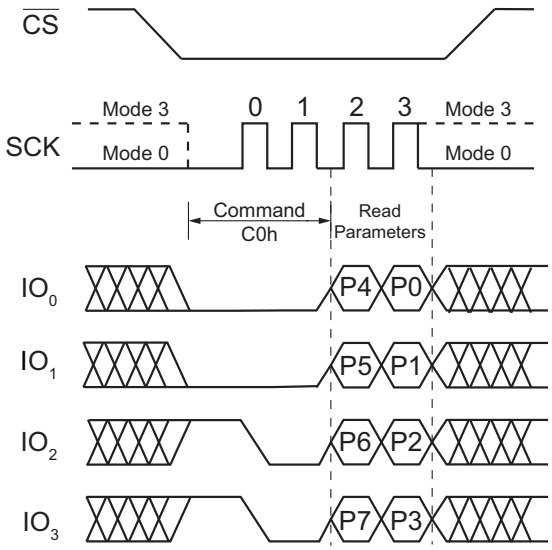
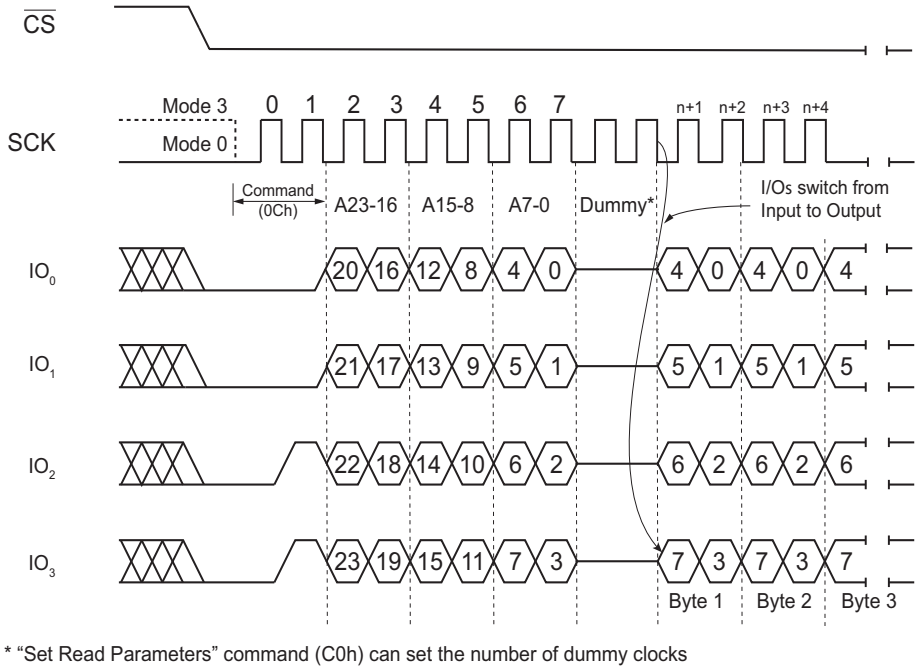



**Figure 36. Set Read Parameters Command (QPI Mode)**

## 10.19 Burst Read with Wrap (0Ch)

The Burst Read with Wrap (0Ch) command provides an alternative way to perform the read operation with Wrap Around in QPI mode. The command is similar to the Fast Read (0Bh) command in QPI mode, except the addressing of the read operation wraps around to the beginning boundary of the wrap length once the ending boundary is reached.

The wrap length and number of dummy clocks can be configured by the Set Read Parameters (C0h) command.




* “Set Read Parameters” command (C0h) can set the number of dummy clocks

**Figure 37. Burst Read with Wrap Command (QPI Mode)**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## 10.20 Read Manufacturer / Device ID (90h)

The Read Manufacturer/ Device ID command provides both the JEDEC assigned manufacturer ID and the specific device ID. It is an alternative to the Release from Power-Down/Device ID command. This command can be issued in both SPI mode and QPI mode.

The command is started by driving the CS pin low and shifting the opcode 90h, followed by a 24-bit address (A23-A0) of 000000h. If the 24-bit address is initially set to 000001h, the Device ID is read first.

Figure 38 shows the 90h command as executed in SPI mode. In this mode the command and address are driven on the SI pin.

Figure 39 shows the 90h command as executed in QPI mode. In this mode the command and address are driven on all four I/O pins.

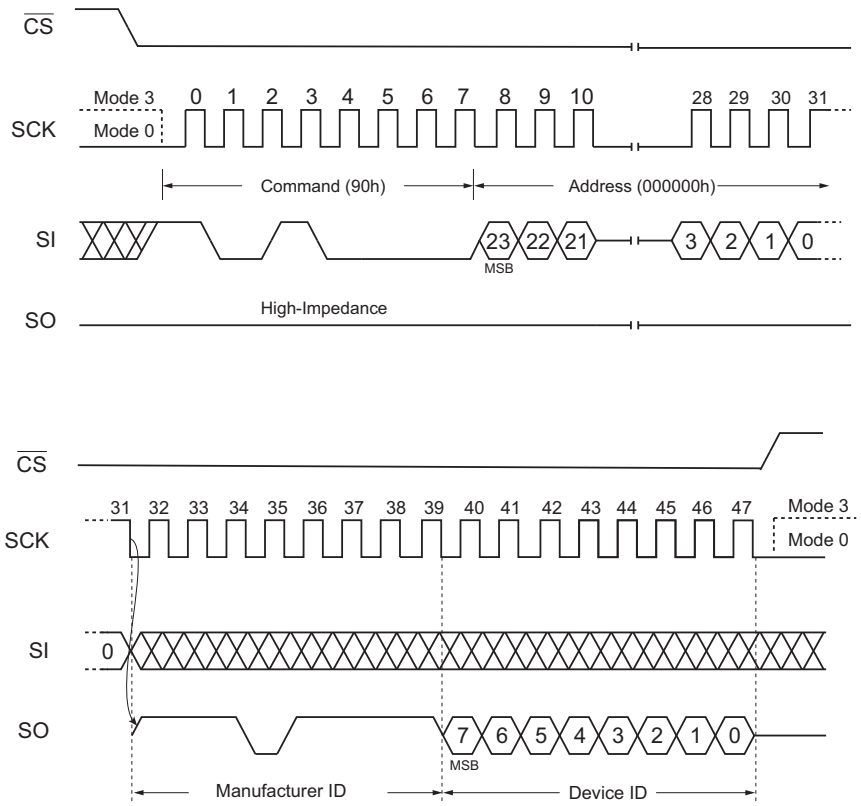


**Figure 38. Read Manufacturer/ Device ID Command (SPI Mode)**


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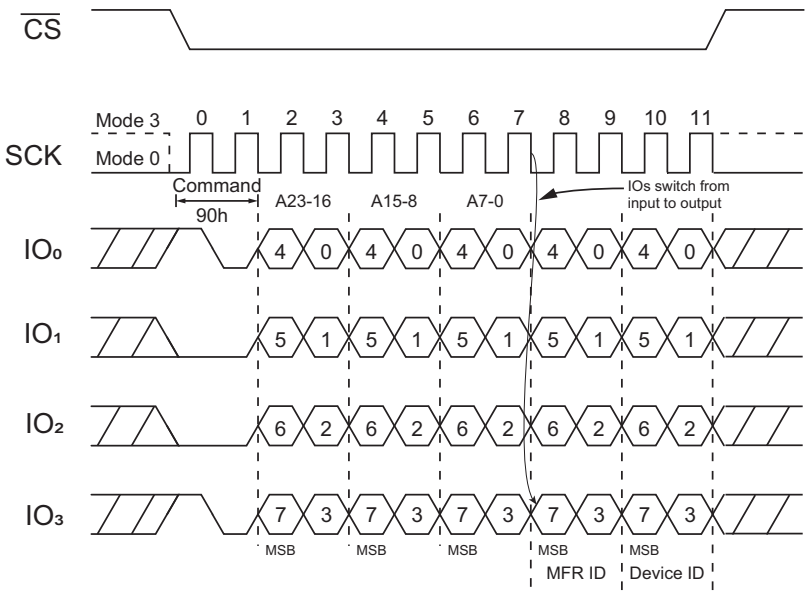


**Figure 39. Read Manufacturer/ Device ID Command (QPI Mode)**


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## 10.21 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer/ Device ID Dual I/O command provides both the JEDEC assigned manufacturer ID and the specific device ID. It is an alternative to the Release from Power-Down/Device ID command that provides both the JEDEC-assigned Manufacturer ID and the specific Device ID by Dual I/O.

The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 92h followed by a 24-bit address (A23-A0) of 000000h. The Manufacturer ID for Renesas Electronics (1Fh) and the Device ID(17h) are shifted out on the falling edge of SCK with most significant bit (MSB) first, as shown in Figure 40. If the 24-bit address is initially set to 000001h, the Device ID is read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The command is completed by driving $\overline{CS}$ high.

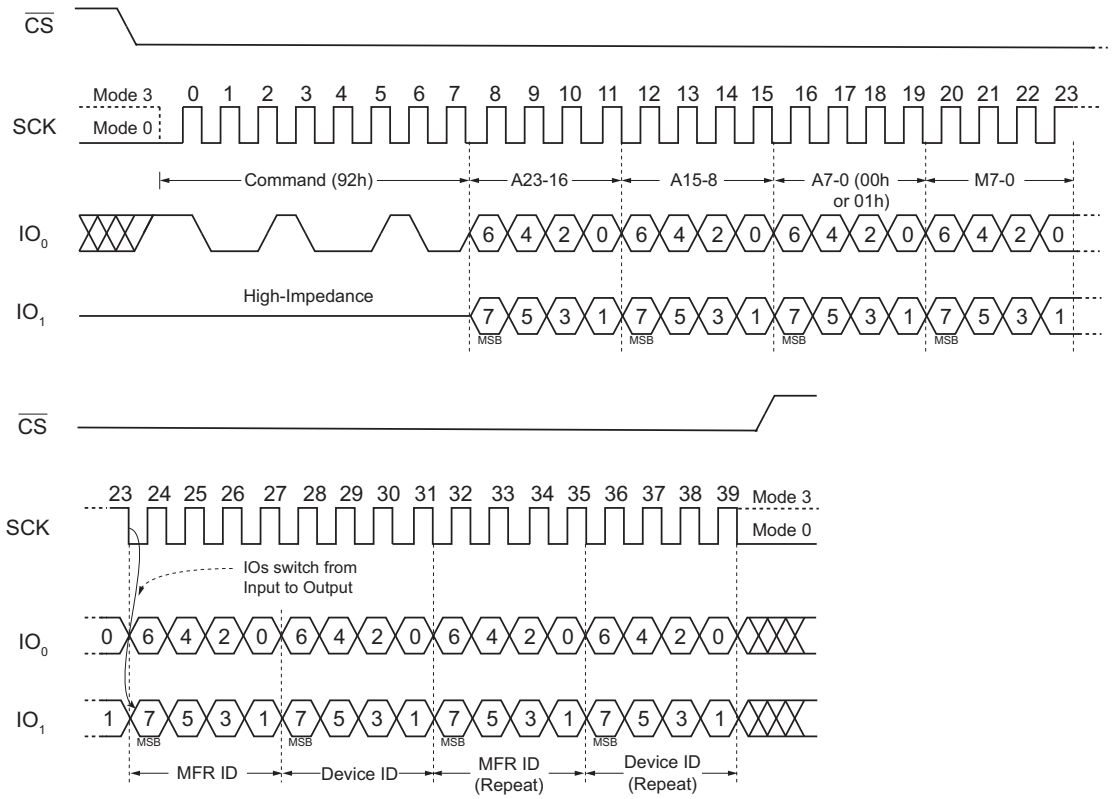


**Figure 40. Read Dual Manufacturer/ Device ID Dual I/O Command (SPI Mode)**


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## 10.22 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer/ Device ID Quad I/O command provides both the JEDEC assigned manufacturer ID and the specific device ID. It is an alternative to the Release from Power-Down/Device ID command that provides both the JEDEC-assigned Manufacturer ID and the specific Device ID by quad I/O. The Quad Enable bit (QE) of the Status Register must be set to enabled.

The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 94h followed by a 24-bit address (A23-A0) of 000000h and six dummy clocks. If the 24-bit address is initially set to 000001h, the Device ID is read first, followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The command is completed by driving $\overline{CS}$ high.

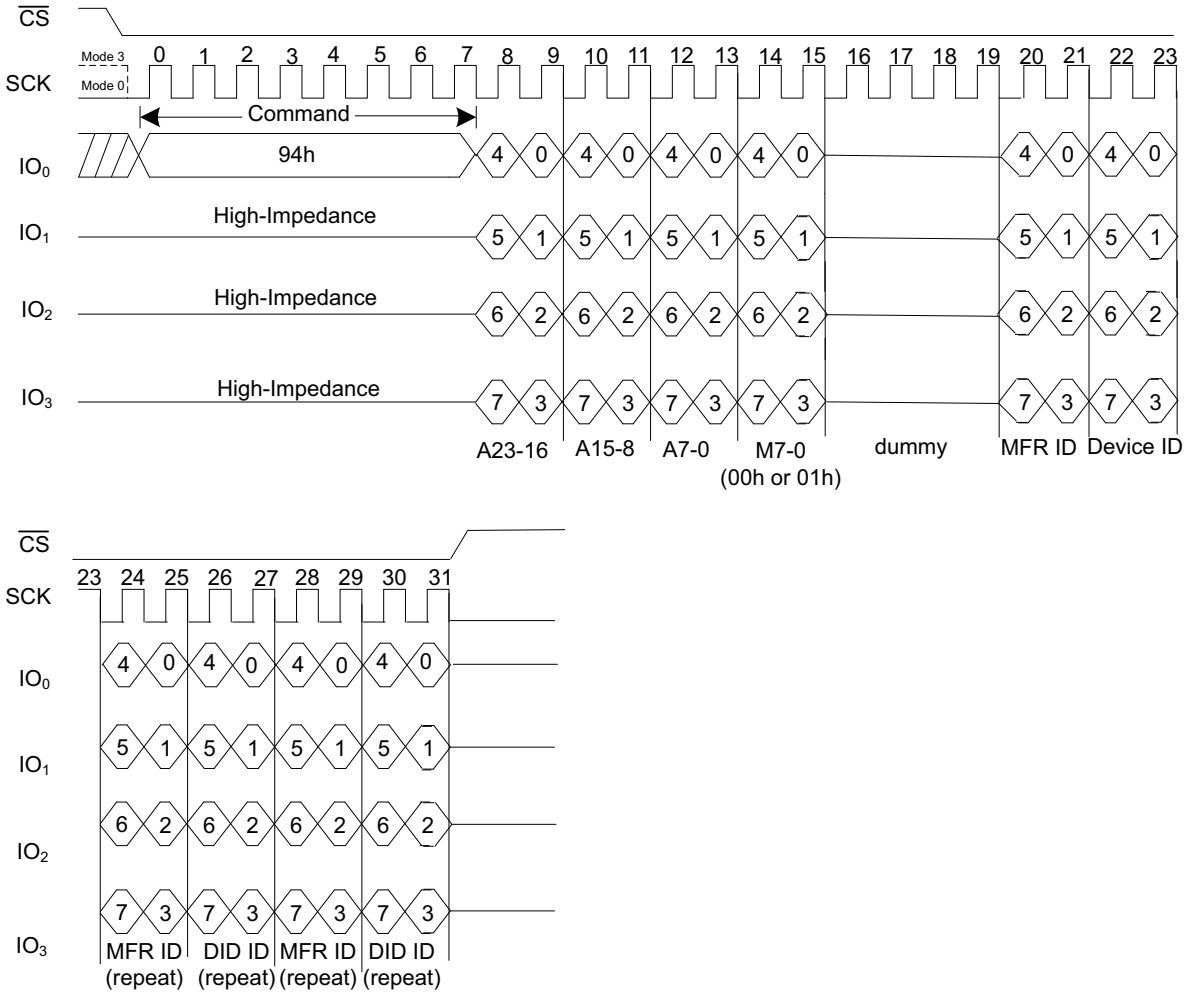


**Figure 41. Read Quad Manufacturer/ Device ID Quad I/O Command (SPI Mode)**


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## 10.23 JEDEC ID (9Fh)

The JEDEC ID command allows the 8-bit manufacturer ID to be read, followed by two bytes of device ID. The device ID indicates the memory type in the first byte, and the memory capacity of the device in the second byte. The JEDEC ID command is not decoded while an Erase or Program cycle is in progress; it has no effect on the cycle that is in progress. Do not issue the JEDEC ID command while the device is in Deep Power-Down Mode.

As shown in Figure 42 and Figure 43, the device is first selected by driving $\overline{CS}$ low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device ID, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of SCK. The JEDEC ID command is terminated by driving $\overline{CS}$ high at any time during data output. When $\overline{CS}$ is driven high, the device is put in Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode, and execute commands.

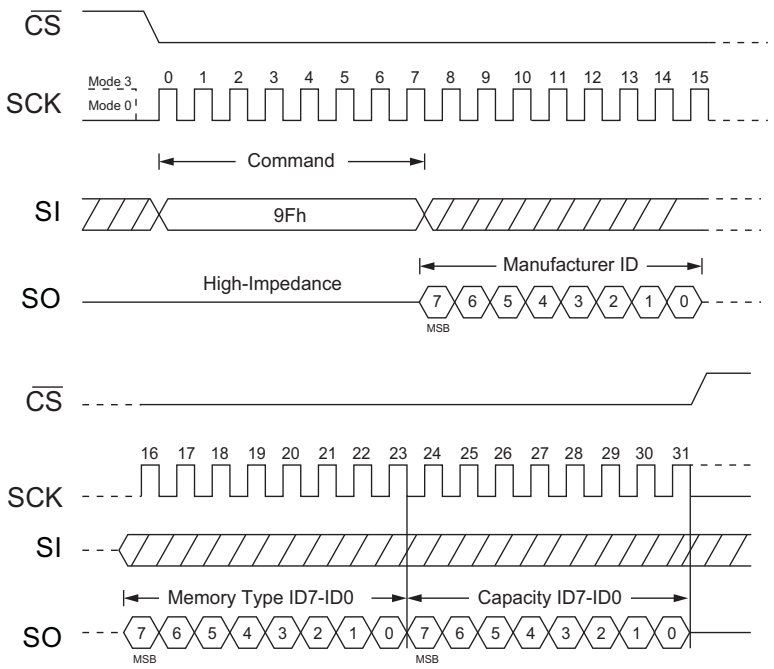


**Figure 42. Read JEDEC ID Command (SPI Mode)**


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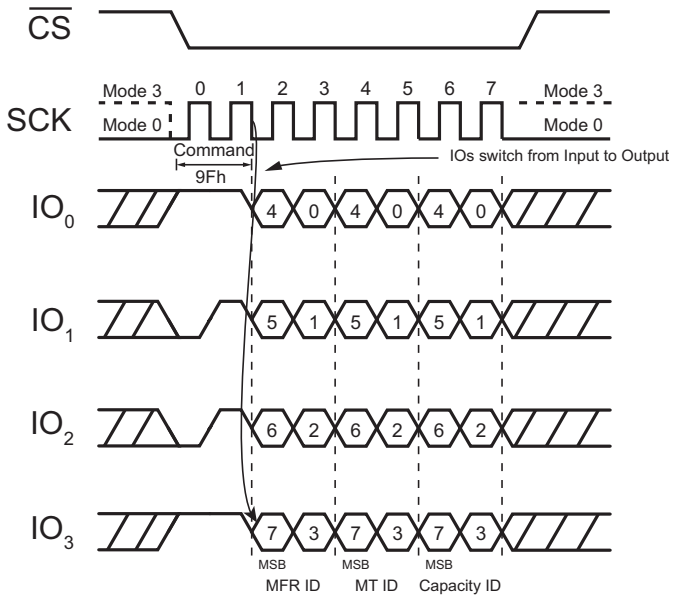


**Figure 43. Read JEDEC ID Command (QPI Mode)**

## 10.24 Read Unique ID Number (4Bh)

The Read Unique ID Number command accesses a factory-set, read-only 128-bit number that is unique to each AT25SL1281C / AT25QL1281C device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID command is started by driving the $\overline{CS}$ pin low and shifting the command code 4Bh, followed by four bytes of dummy clocks in SPI mode.

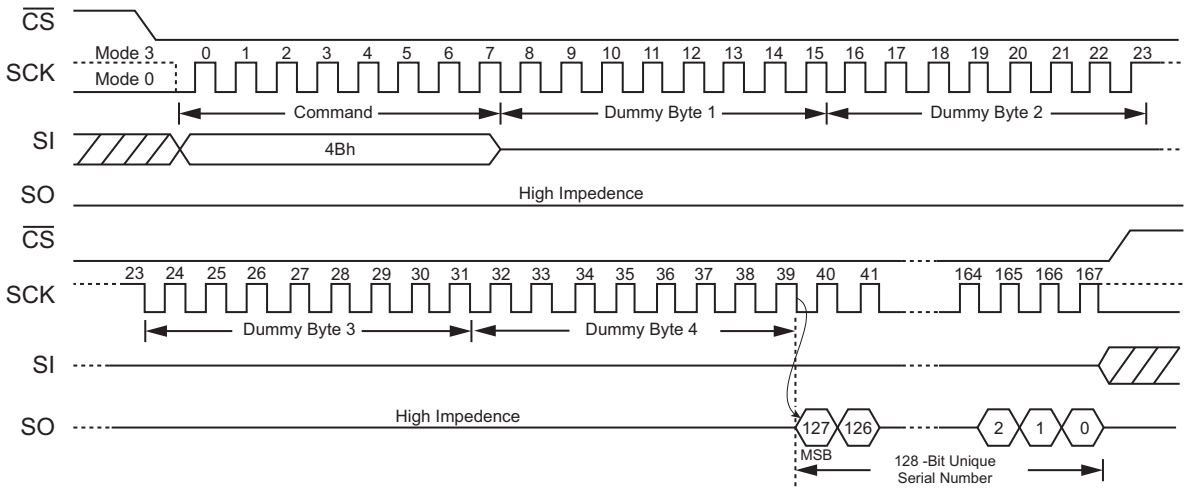


**Figure 44. Read Unique ID Sequence (SPI Mode only)**


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## 10.25 Deep Power-Down (B9h)

Executing the Deep Power-Down command is the best way to put the device in the lowest power consumption. The Deep Power-Down command reduces the standby current (from $I_{CC1}$ to $I_{CC2}$ as specified in Section 11.7). The command is entered by driving the $\overline{CS}$ pin low following execution of the B9h command. (See Figure 45 and Figure 46.)

The $\overline{CS}$ pin must go high exactly at the byte boundary (the latest eighth bit of command code been latched-in); otherwise, the Deep Power-Down command is not executed. After $\overline{CS}$ goes high, it requires a delay of $t_{DP}$ and the Deep Power-Down mode is entered. While in the Deep Power-Down mode, the Release Deep Power-Down / Device ID command is used to restore the device to normal operation. All other commands are ignored, including the Read Status Register command, which is always available during normal operation. The device always powers-up in the normal operation with the standby current of $I_{CC1}$.

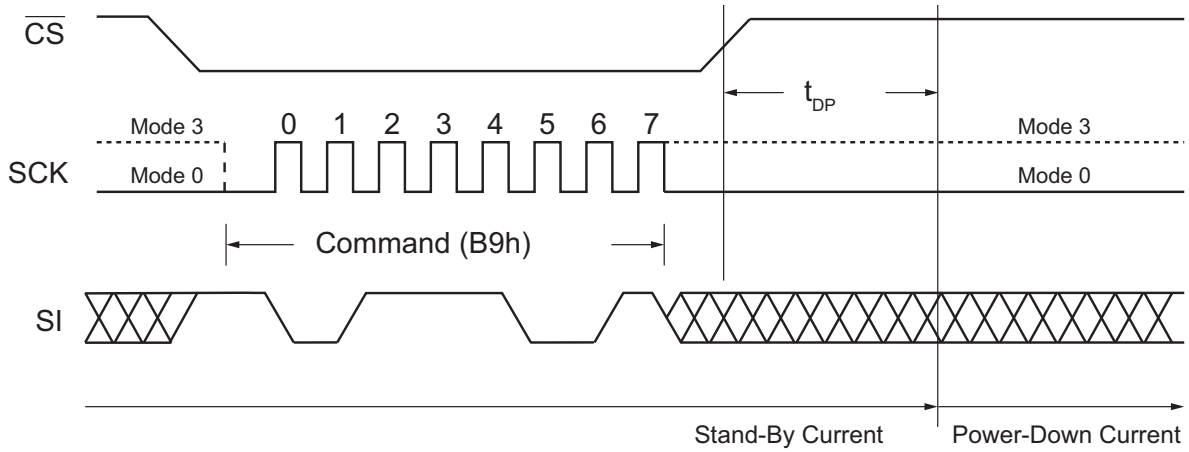


**Figure 45. Deep Power-Down Command (SPI Mode)**

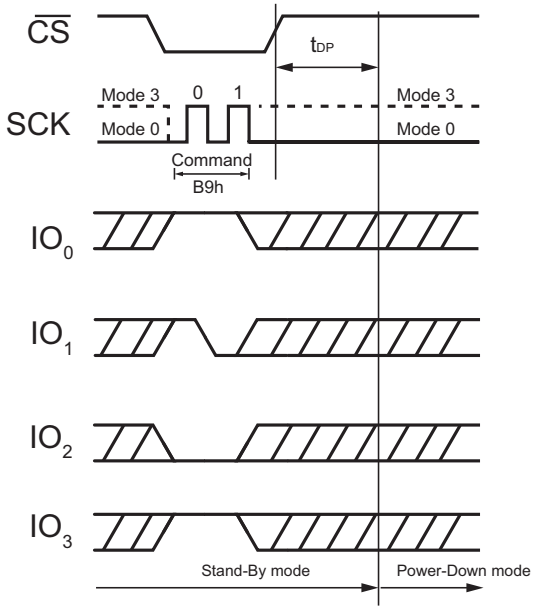


**Figure 46. Deep Power-Down Command (QPI Mode)**


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## 10.26 Release Deep Power-Down / Device ID (ABh)

The Release Deep Power-Down / Device ID command is a multi-purpose command. It can be used to release the device from the Deep Power-Down state or obtain the device identification (ID).

The command is issued by driving the $\overline{CS}$ pin low and driving a value of ABh onto the bus, then driving $\overline{CS}$ high, as shown in Figure 47 and Figure 48. The Release from Deep Power-Down command requires the time duration of $t_{RES1}$ (see Section 11.7, AC Electrical Characteristics) before accepting other commands. The $\overline{CS}$ pin must keep high during the $t_{RES1}$ time.

The Device ID can be read during SPI mode only. In other words, the Device ID feature is not available in QPI mode for the Release Deep Power-Down/Device ID command. To obtain the Device ID in SPI mode, the command is initiated by driving the $\overline{CS}$ pin low and sending the command code ABh followed by 3-dummy bytes. The Device ID bits are then shifted on the falling edge of SCK with most significant bit (MSB) first, as shown in Figure 49. After $\overline{CS}$ is driven high it must keep high for a time duration of $t_{RES2}$ (see Section 11.7, AC Electrical Characteristics). The Device ID can be read continuously. The command is completed by driving $\overline{CS}$ high.

If the Release from Deep Power-Down /Device ID command is issued while an Erase, Program, or Write cycle is in process (when RDY/BSY equals 1), the command is ignored and does not have any effect on the current cycle.

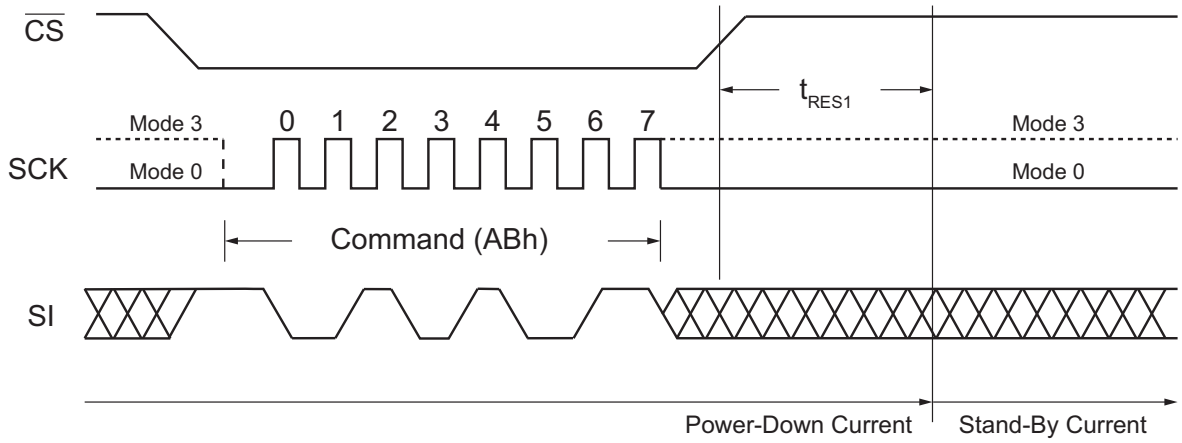


**Figure 47. Release Power-Down Command (SPI Mode)**

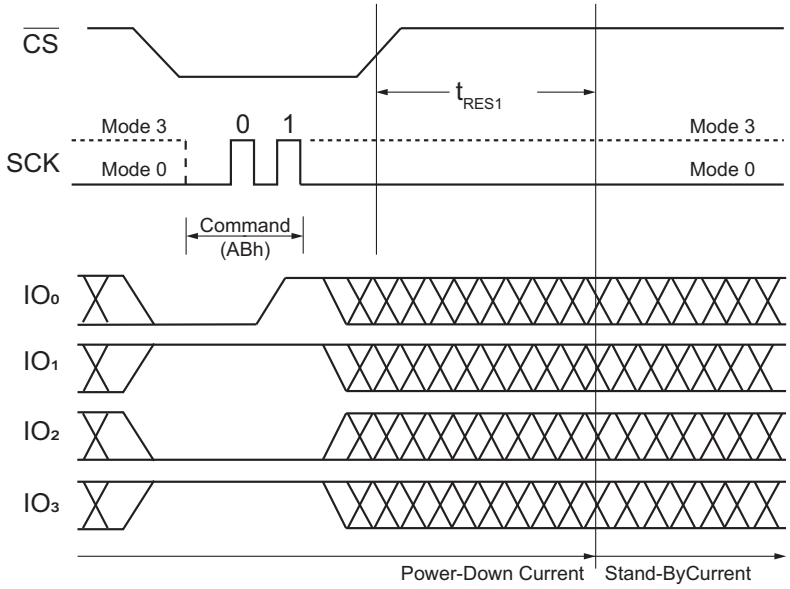


**Figure 48. Release Power-Down Command (QPI Mode)**


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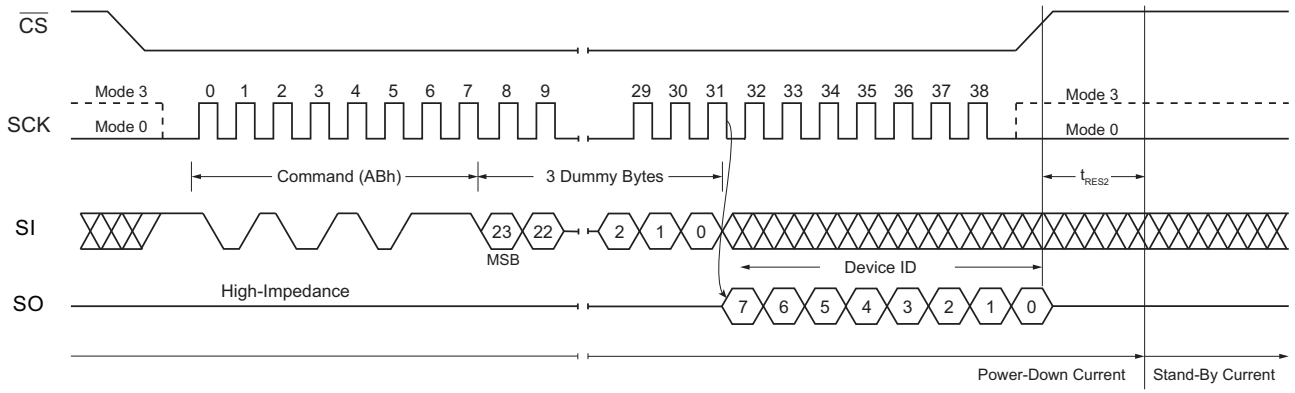


**Figure 49. Release Power-Down / Device ID Command (SPI Mode)**

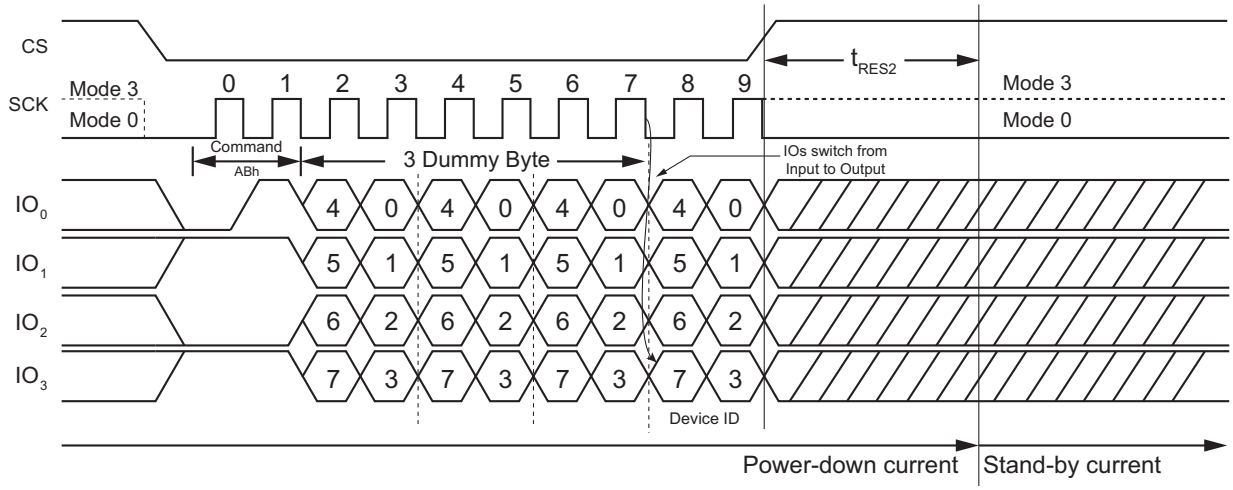


**Figure 50. Release Power-Down / Device ID Command (QPI Mode)**


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## 10.27 Read Security Register (48h)

This command is followed by a 3-byte address (A23-A0) and a dummy byte. In QPI mode, the number of dummy cycles can be configured by the C0h command. Each bit is latched in during the rising edge of SCK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency $f_C$, during the falling edge of SCK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (byte 3FFH), it resets to 000H. The command is completed by driving $\overline{CS}$ high.

**Table 20. Security Register Structure**

| Address | A23-A16 | A15-A12 | A11-A10 | A9-A0 |
|---|---|---|---|---|
| Security Register 1 | 00h | 0 0 0 1 | 0 0 | Byte Address |
| Security Register 2 | 00h | 0 0 1 0 | 0 0 | Byte Address |
| Security Register 3 | 00h | 0 0 1 1 | 0 0 | Byte Address |

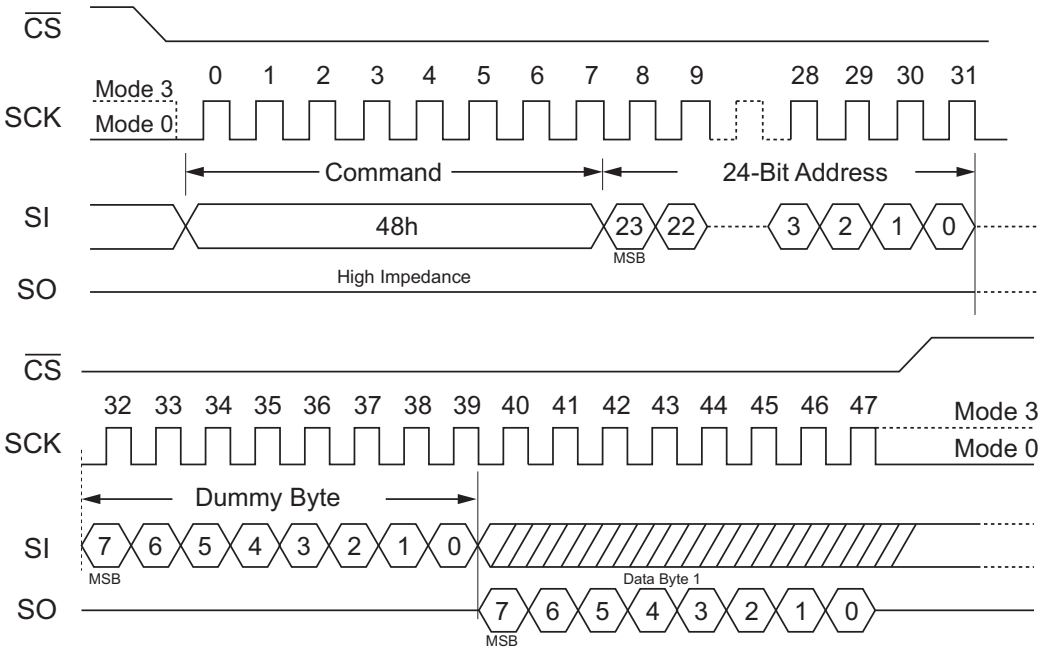
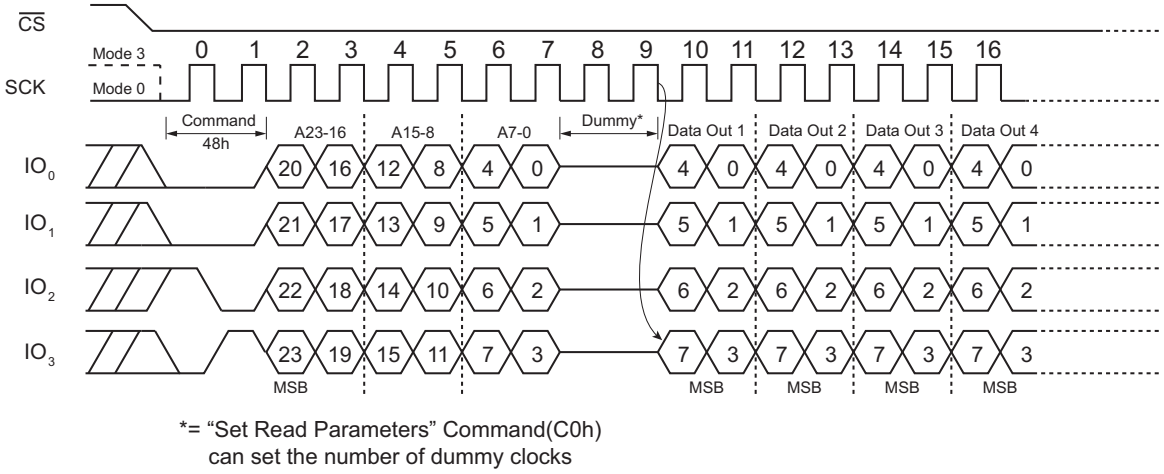



**Figure 51. Read Security Register, SPI Mode**




*= “Set Read Parameters” Command(C0h) can set the number of dummy clocks

**Figure 52. Read Security Register, QPI Mode**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## 10.28 Erase Security Register (44h)

The AT25SL1281C provides three 1024-byte Security Registers that can be erased and programmed individually. These registers can be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to the Block Erase command. A Write Enable command must previously have been executed to set the Write Enable Latch bit.

The Erase Security Registers command sequence is: $\overline{CS}$ goes low, sending Erase Security Registers command; then, $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the command code has been latched in; otherwise, the Erase Security Registers command is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Erase Security Registers cycle (with a duration of $t_{BE}$) is initiated. While the Erase Security Registers cycle is in progress, the Status Register can be read to check the value of the Ready/Busy (RDY/BSY) bit. The Ready/Busy (RDY/BSY) bit is 1 during the self-timed Erase Security Registers cycle; it is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the Security Registers. Once the LB bit is set to 1, the Security Registers are permanently locked; the Erase Security Registers command is ignored.

**Table 21. Security Register Structure**

| Address | A23-A16 | A15-A12 | A11-A10 | A9-A0 |
|---|---|---|---|---|
| Security Register 1 | 00h | 0 0 0 1 | 0 0 | Byte Address |
| Security Register 2 | 00h | 0 0 1 0 | 0 0 | Byte Address |
| Security Register 3 | 00h | 0 0 1 1 | 0 0 | Byte Address |

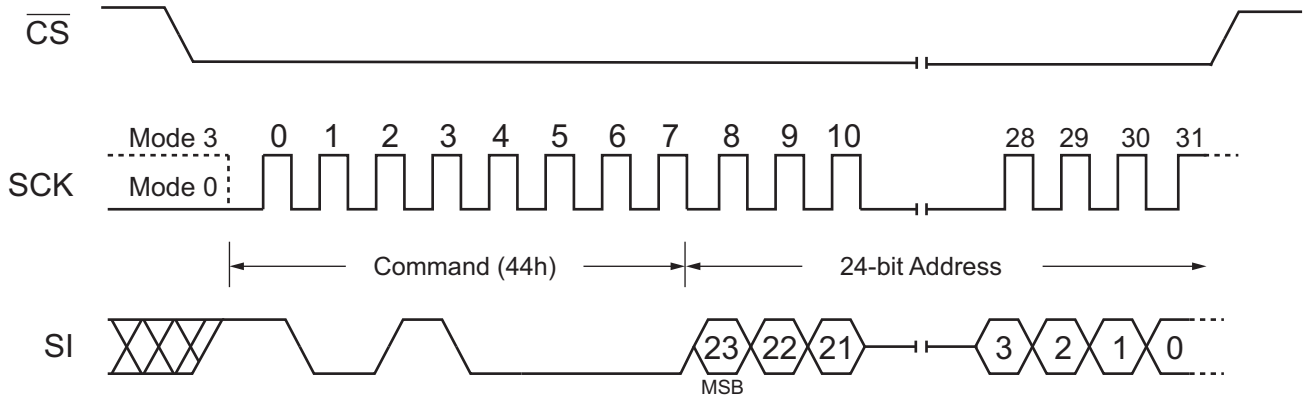


**Figure 53. Erase Security Register SPI Mode**


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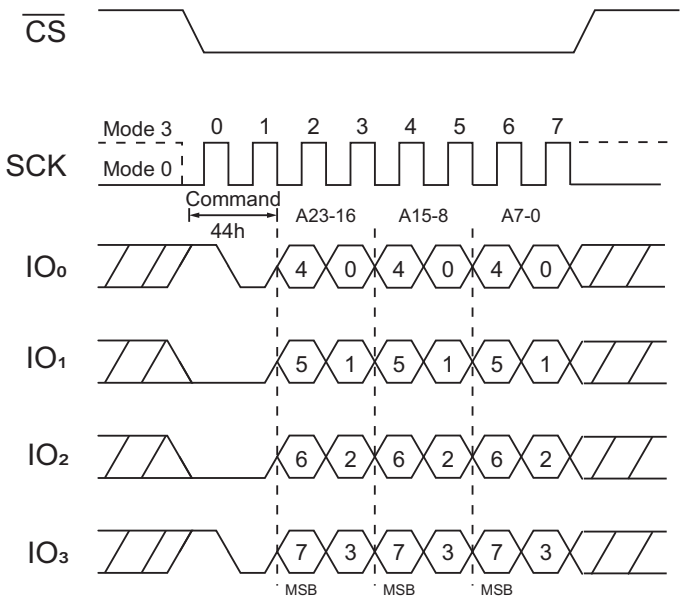


**Figure 54. Erase Security Register QPI Mode**


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## 10.29 Program Security Register (42h)

The Program Security Registers command is similar to the Page Program command. It allows from one byte to 1024 bytes of Security Register data to be programmed by four times (one time program 256 bytes). A Write Enable command must previously have been executed to set the Write Enable Latch bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving $\overline{CS}$ low, followed by the command code 42h, a 3-byte address, and at least one data byte on SI. As soon as $\overline{CS}$ is driven high, the self-timed Program Security Registers cycle (with a duration of $t_{PP}$) is started. While the Program Security Registers cycle is in progress, the Status Register can be read to check the value of the Ready/Busy (RDY/BSY) bit. The Ready/Busy (RDY/BSY) bit is 1 during the self-timed Program Security Registers cycle; it is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.

If the Security Registers Lock Bit (LB3/LB2/LB1) is set to 1, the Security Registers are permanently locked; the Program Security Registers command is ignored.

**Table 22. Security Register Structure**

| Address | A23-A16 | A15-A12 | A11-A10 | A9-A0 |
|---|---|---|---|---|
| Security Register 1 | 00h | 0 0 0 1 | 0 0 | Byte Address |
| Security Register 2 | 00h | 0 0 1 0 | 0 0 | Byte Address |
| Security Register 3 | 00h | 0 0 1 1 | 0 0 | Byte Address |

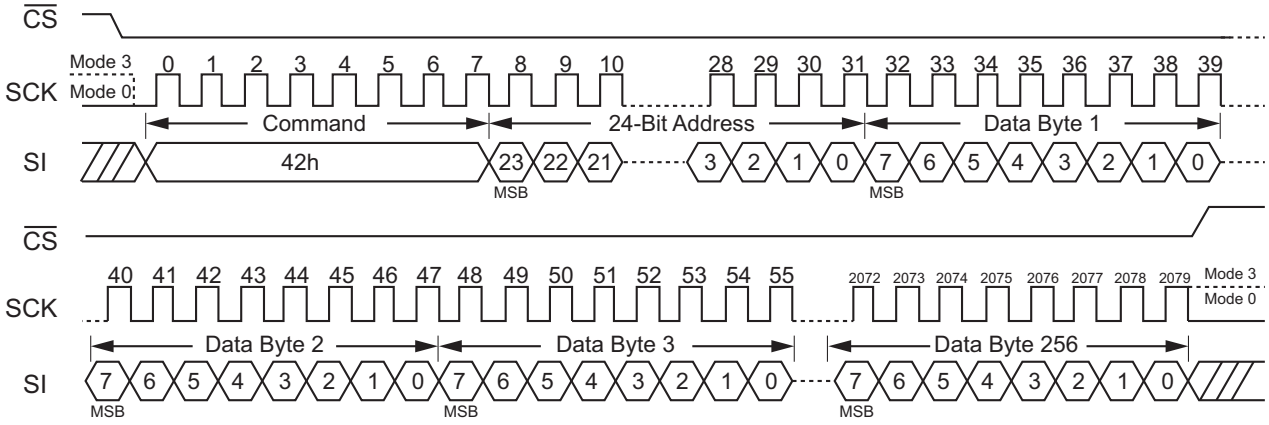


**Figure 55. Program Security Register SPI Mode**

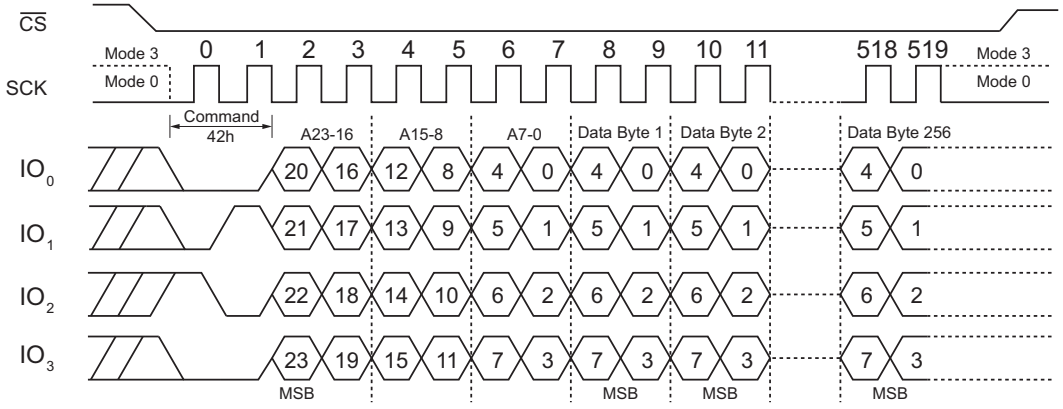


**Figure 56. Program Security Register QPI Mode**


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## 10.30 Read Serial Flash Discovery Parameter (5Ah)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

The Read SFDP command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 5Ah, followed by a 24-bit address (A23-A0), into the SI pin, regardless of the 3-byte or 4-byte Address Mode. Eight dummy clocks are also required in SPI mode. In QPI mode, the number of dummy clocks can be configured by the Set Read Parameters (C0h) command.

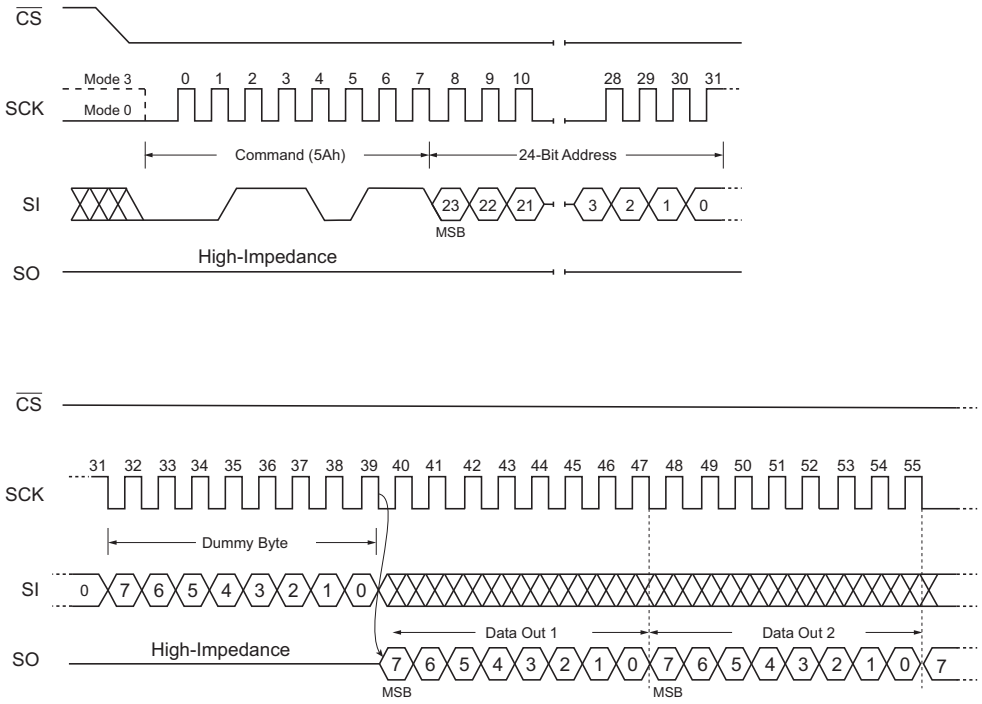
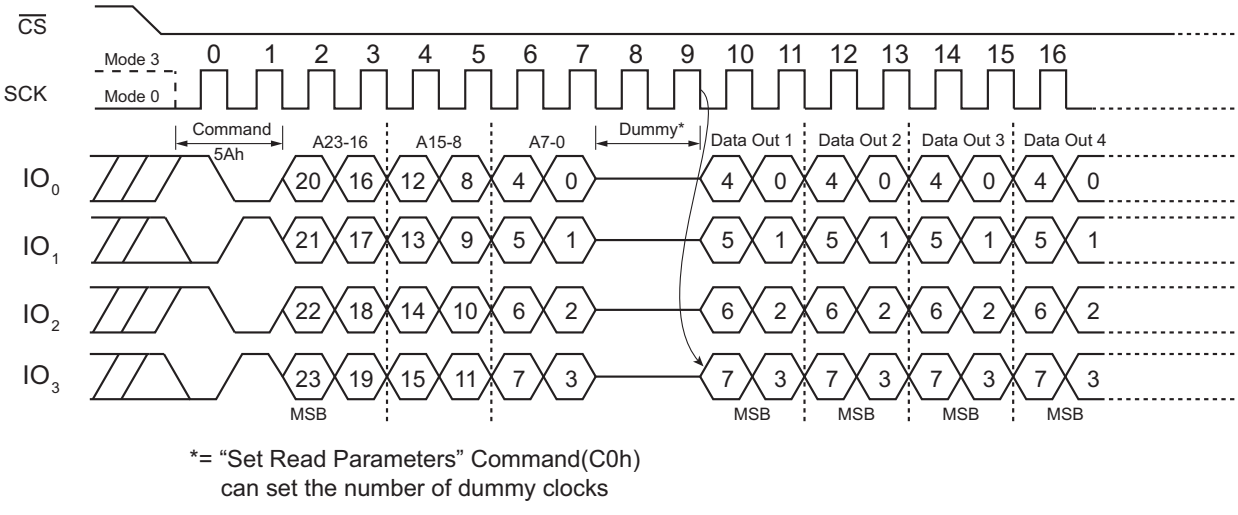



**Figure 57. Read SFDP Register Command SPI Mode**




*= "Set Read Parameters" Command(C0h) can set the number of dummy clocks

**Figure 58. Read Serial Flash Discoverable Parameter QPI Mode**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## 10.31 Page Program (02h)

The Page Program command is for programming the memory. A Write Enable command must previously have been executed to set the Write Enable Latch bit before sending the Page Program command.

The Page Program command is entered by driving $\overline{CS}$ low, followed by the command code, 3-byte address, and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). $\overline{CS}$ must be driven low for the duration of the sequence. The Page Program command sequence is: $\overline{CS}$ goes low → send Page Program command → 3-byte address on SI → at least 1 byte data on SI → $\overline{CS}$ goes high.

If more than 256 bytes are sent to the device, previously latched data are discarded, and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. $\overline{CS}$ must be driven high after the eighth bit of the last data byte has been latched in; otherwise, the Page Program command is not executed.

As soon as $\overline{CS}$ is driven high, the self-timed Page Program cycle (whose duration is $t_{PP}$) is initiated. While the Page Program cycle is in progress, the Status Register can be read to check the value of the Ready/Busy (RDY/BSY) bit. The Ready/Busy (RDY/BSY) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.

A Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are not executed.

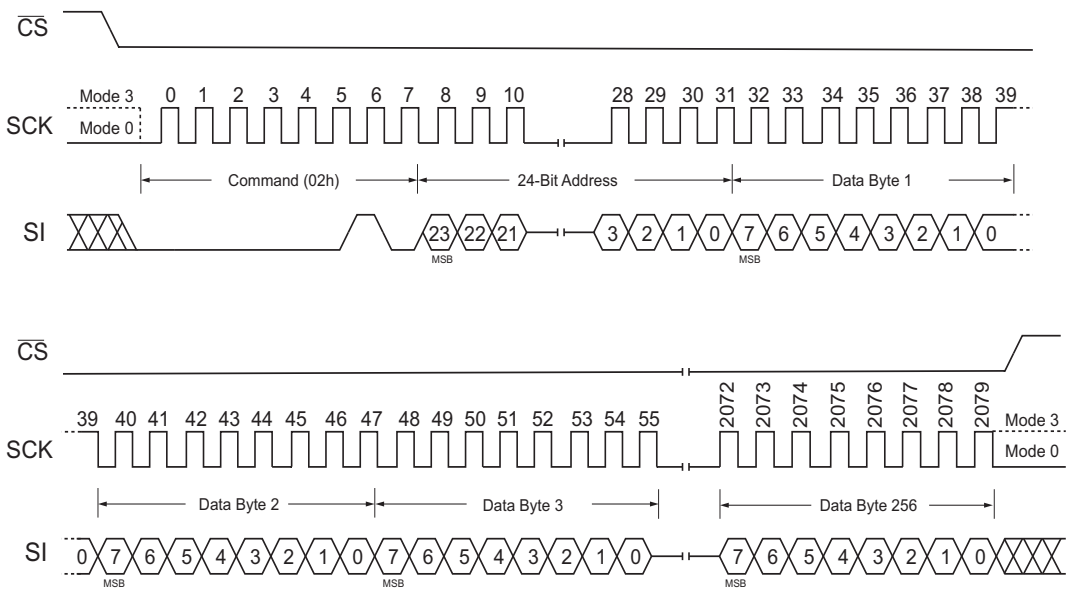


**Figure 59. Page Program Command (SPI Mode)**


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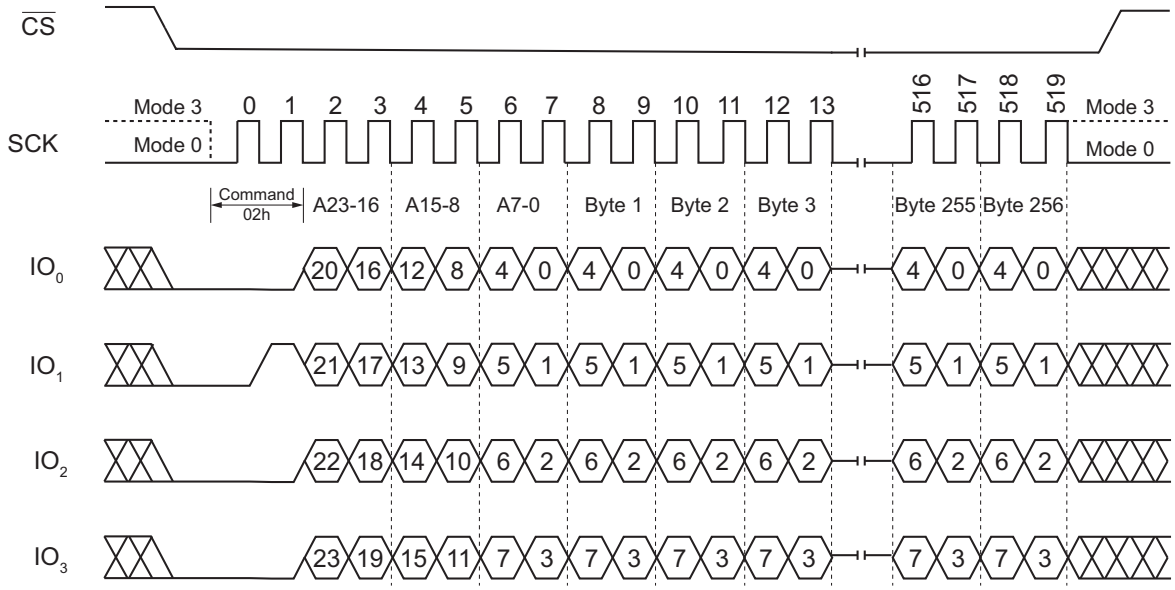


**Figure 60. Page Program Command (QPI Mode)**


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## 10.32 Quad Page Program (32h)

The Quad Page Program command is for programming the memory using four pins: $IO_0$, $IO_1$, $IO_2$, and $IO_3$. To use Quad Page Program, the Quad enable in Status Register QE bit must be 1 (default for the AT25QL1281C). A Write Enable command must previously have been executed to set the Write Enable Latch bit before sending the Page Program command. The Quad Page Program command is entered by driving $\overline{CS}$ Low, followed by the command code (32h), three address bytes, and at least one data byte on the I/O pins. The QE bit must be set to enable.

If more than 256 bytes are sent to the device, previously latched data are discarded, and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to the device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. $\overline{CS}$ must be driven high after the eighth bit of the last data byte has been latched in; otherwise, the Quad Page Program command is not executed.

As soon as $\overline{CS}$ is driven high, the self-timed Quad Page Program cycle (with a duration of $t_{PP}$) is initiated. While the Quad Page Program cycle is in progress, the Status Register can be read to check the value of the Ready/Busy (RDY/BSY) bit. The Ready/Busy (RDY/BSY) bit is 1 during the self-timed Quad Page Program cycle; it is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

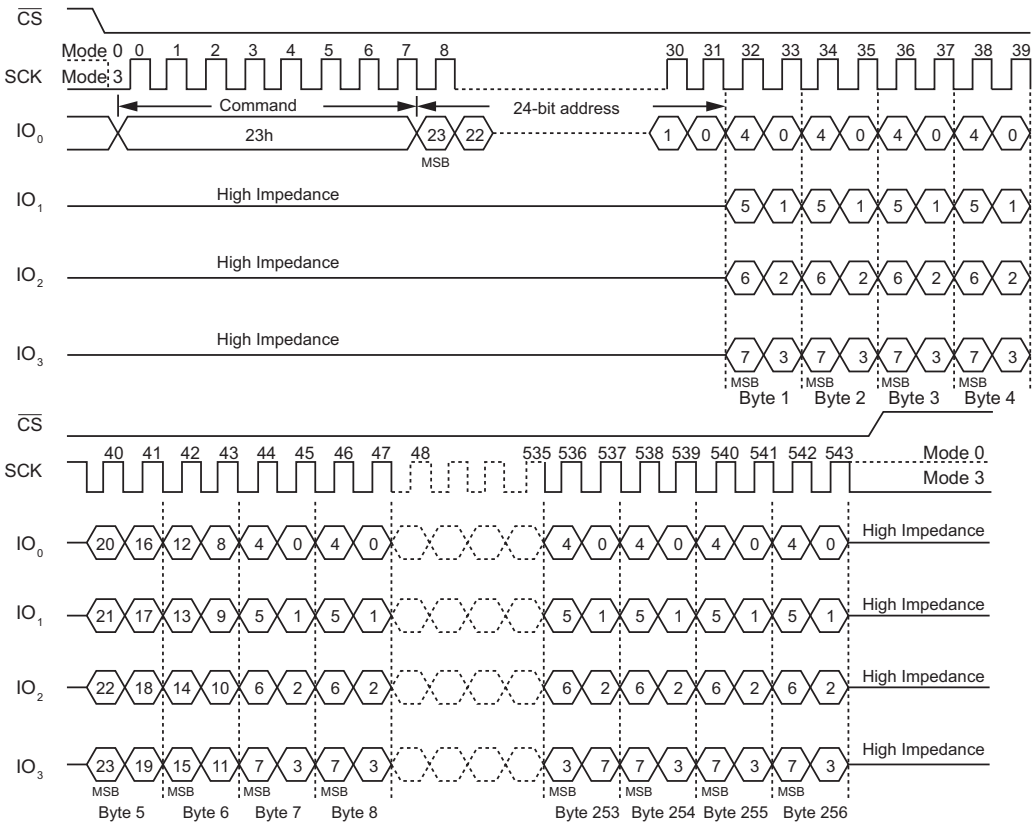


**Figure 61. Quad Page Program Command (SPI mode)**


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## 10.33 4-kB Block Erase (20h)

The Block Erase command is for erasing the all data of the chosen block. A Write Enable command must previously have been executed to set the Write Enable Latch bit. The Block Erase command is entered by driving $\overline{CS}$ low, followed by the command code and 3-address bytes on SI. Any address inside the block is a valid address for the Block Erase command. $\overline{CS}$ must be driven low for the duration of the sequence.

The Block Erase command sequence is: $\overline{CS}$ goes low → sending Block Erase instruction → 3-byte address on SI → $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the last address byte has been latched in; otherwise, the Block Erase command is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Block Erase cycle (with a duration of $t_{BE}$) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Ready/Busy (RDY/BSY) bit. The Ready/Busy (RDY/BSY) bit is 1 during the self-timed Block Erase cycle; it is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A Block Erase command applied to a block that is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

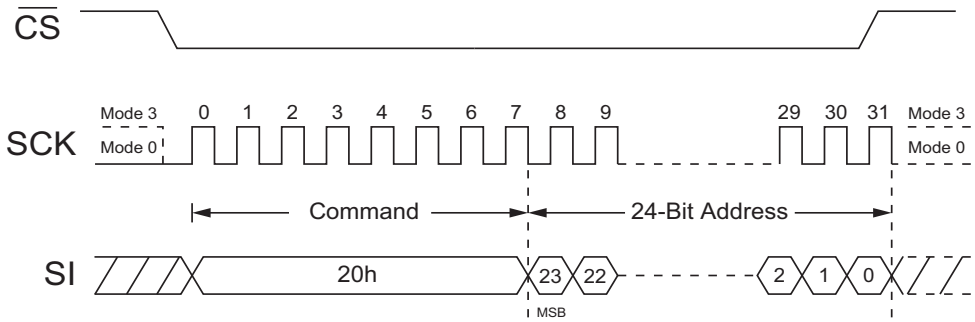


**Figure 62. 4-kB Block Erase Command (SPI Mode)**

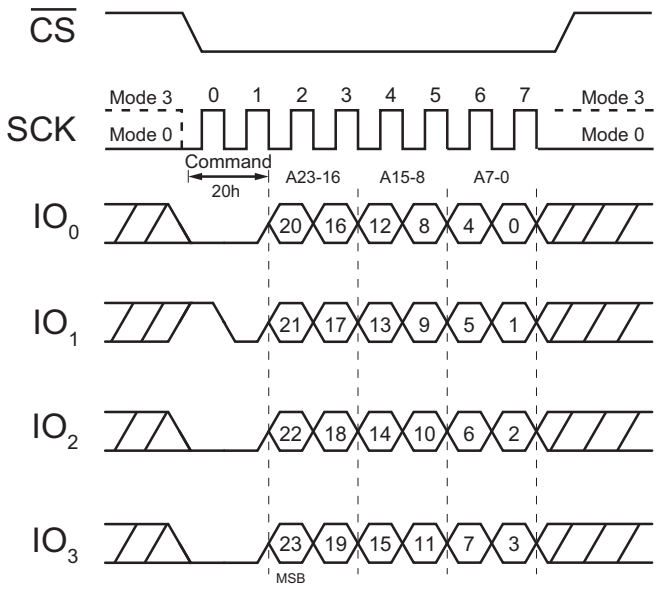


**Figure 63. 4-kB Block Erase Command (QPI Mode)**


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## 10.34 32-kB Block Erase (52h)

The 32kB Block Erase command is for erasing the all data of the chosen block. A Write Enable command must previously have been executed to set the Write Enable Latch bit. The 32kB Block Erase command is entered by driving $\overline{CS}$ low, followed by the command code and a 3-byte address on SI. Any address inside the block is a valid address for the 32kB Block Erase command. $\overline{CS}$ must be driven low for the duration of the sequence.

The 32kB Block Erase command sequence is: $\overline{CS}$ goes low → sending 32 kB Block Erase instruction → 3-byte address on SI → $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the last address byte has been latched in; otherwise, the 32 kB Block Erase command is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Block Erase cycle (with a duration of $t_{BE}$) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Ready/Busy (RDY/BSY) bit. The Ready/Busy (RDY/BSY) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 32 kB Block Erase command applied to a block that is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

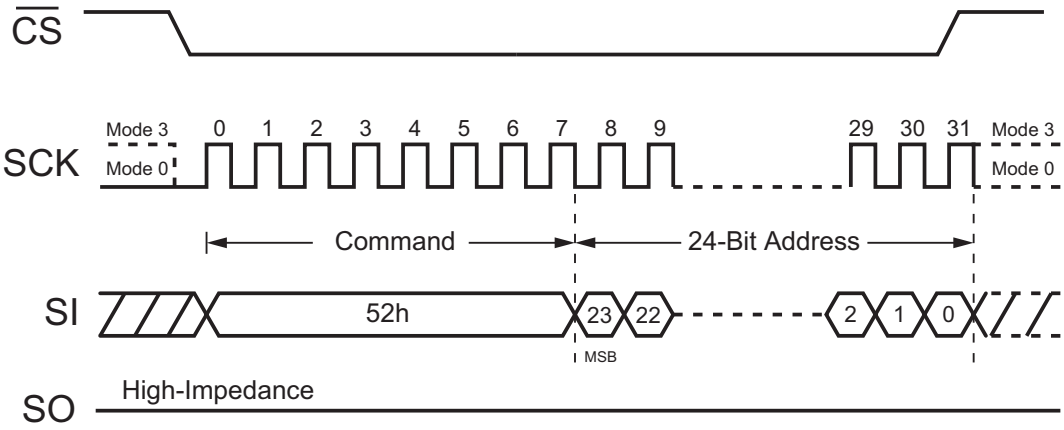


**Figure 64. 32-kB Block Erase Command (SPI Mode)**

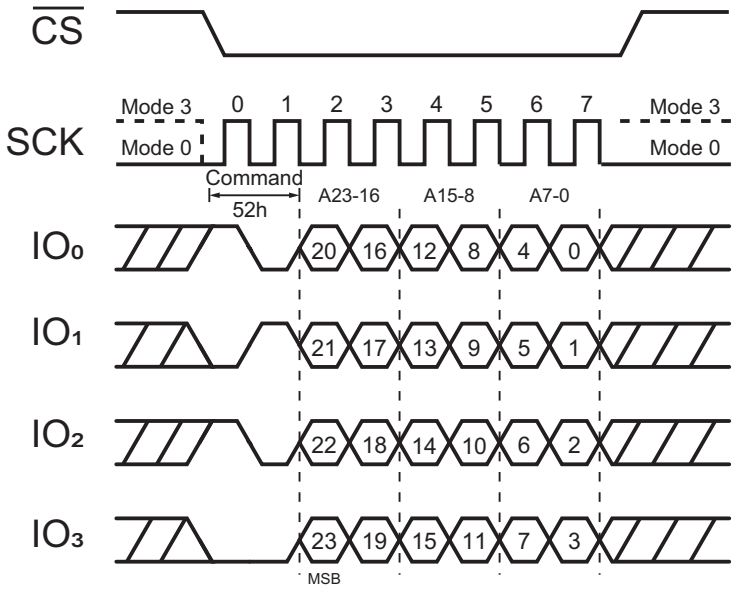


**Figure 65. 32-kB Block Erase Command (QPI Mode)**


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## 10.35 64-kB Block Erase (D8h)

The 64kB Block Erase command is for erasing the all data of the chosen block. A Write Enable command must previously have been executed to set the Write Enable Latch bit. The 64kB Block Erase command is entered by driving $\overline{CS}$ low, followed by the command code and a 3-byte address on SI. Any address inside the block is a valid address for the 64kB Block Erase command. $\overline{CS}$ must be driven low for the entire duration of the sequence.

The 64kB Block Erase command sequence is: $\overline{CS}$ goes low, sending 64kB Block Erase command and a 3-byte address on SI; $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the last address byte has been latched in; otherwise, the 64kB Block Erase command is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Block Erase cycle (whose duration is $t_{BE}$) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Ready/Busy (RDY/BSY) bit. The Ready/Busy (RDY/BSY) bit is 1 during the self-timed Block Erase cycle; it is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 64kB Block Erase command applied to a block that is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table 6-Table 7) is not executed.

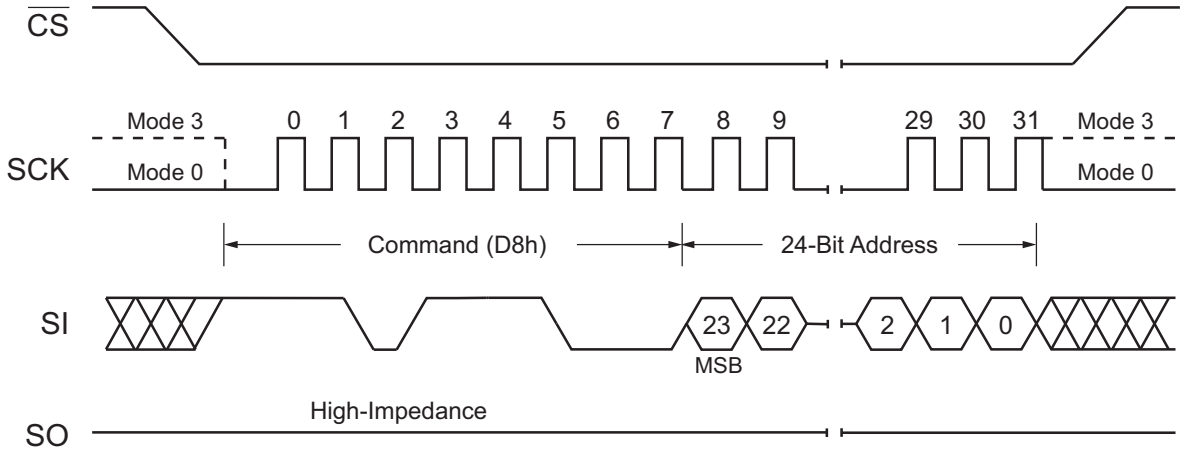


**Figure 66. 64-kB Block Erase Command (SPI Mode)**

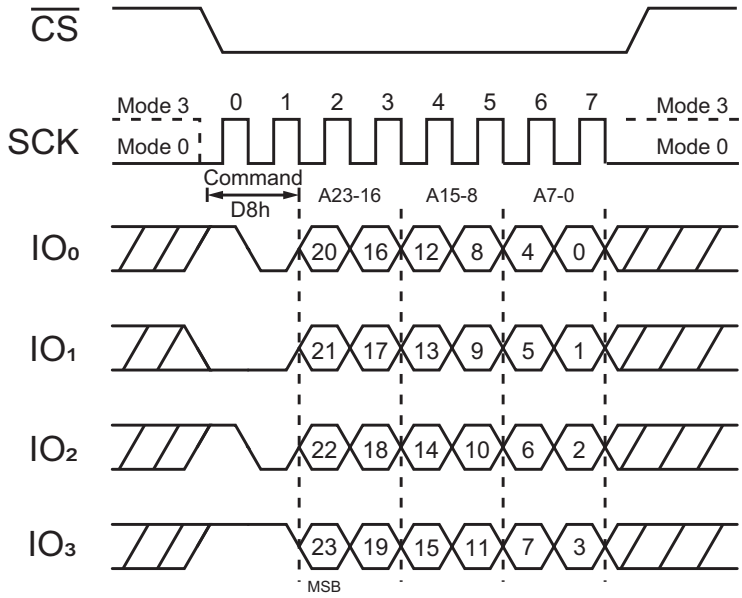


**Figure 67. 64-kB Block Erase Command (QPI Mode)**


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## 10.36 Chip Erase (C7h / 60h)

The Chip Erase command clears all bits in the device to FFh (all 1s). Before the Chip Erase Command, a Write Enable command must be issued. The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code C7h or 60h. See Figure 68.

The $\overline{CS}$ pin must go high after the eighth bit of the last byte has been latched in; otherwise, the Chip Erase command is not executed. After $\overline{CS}$ is driven high, the self-timed Chip Erase command commences for a duration of $t_{CE}$. See Section 11.7, AC Electrical Characteristics.

While the Chip Erase cycle is in progress, the Read Status Register command can be accessed to check the status of the RDY/BSY bit.

The RDY/BSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other commands again. After the Chip Erase cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase command is executed only if all Block Protect (BP2, BP1, and BP0) bits are 0; it is ignored if one or more blocks are protected.

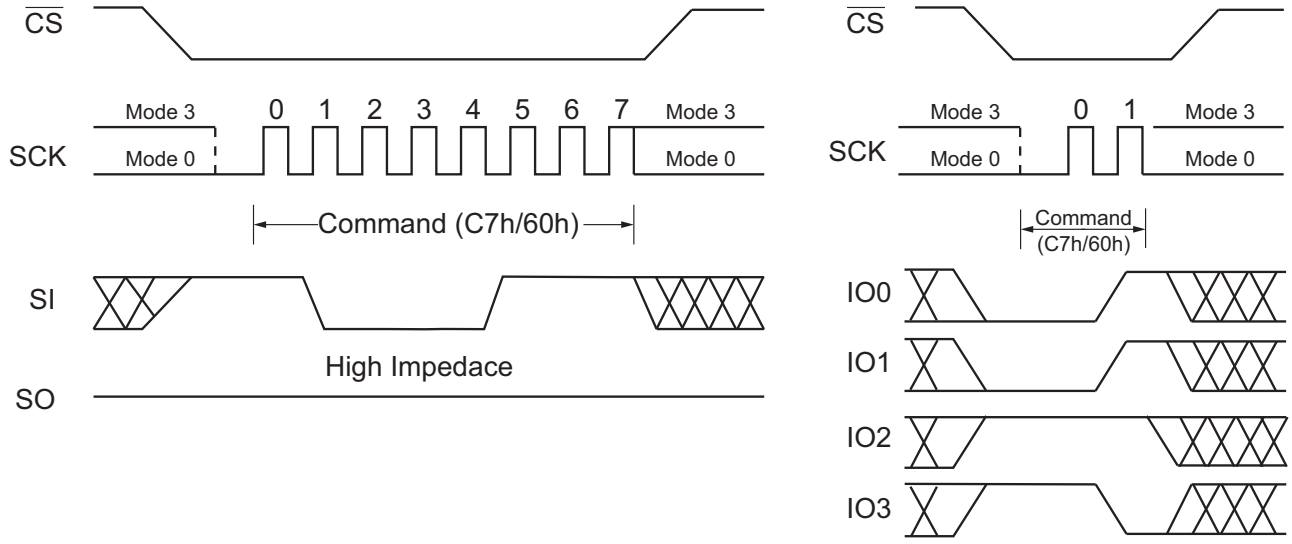


**Figure 68. Chip Erase Command for SPI Mode (left) and QPI Mode (right)**


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## 10.37 Erase / Program Suspend (75h)

The Program/Erase Suspend command instructs the system to interrupt a Page Program or a Block Erase operation. (The time between the Program/Erase command and the Program/Erase Suspend command is $t_{PS}$/$t_{ES}$). After the program operation has entered the suspended state, the memory array can be read except for the page being programmed. After the erase operation has entered the suspended state, the memory array can be read or programed, except for the 4kB/32kB/64kB block being erased. A Write Status Register operation cannot be suspended.

**Table 23. Readable Area of Memory While a Program Operation is Suspended**

| Suspended Operation | Readable Region of Memory Array |
|---|---|
| Page Program | All but the Page being programmed |
| Quad Page Program | All but the Page being programmed |

**Table 24. Readable or Programmable Area of Memory While an Erase Operation is Suspended**

| Suspended Operation | Readable or Programmable Region of Memory Array |
|---|---|
| Erase (4 kB) | All but the Block being erased |
| 32 kB Block Erase | All but the 32 kB Block being erased |
| 64 kB Block Erase | All but the 64 kB Block being erased |

When the AT25SL1281C receives the Suspend command, there is a latency of $t_{PSL}$ or $t_{ESL}$ before the Write Enable Latch (WEL) bit clears to 0 and the SUS2 or SUS1 sets to 1; after which, the device is ready to accept one of the commands listed in Table 25. See Section 11.7 for $t_{PSL}$ and $t_{ESL}$ timings. Table 25 lists the commands for which the $t_{PSL}$ and $t_{ESL}$ latencies do not apply. For example: 05h, 66h, and 99h can be issued at any time after the Suspend command.

Status Register bit 15 (SUS2) and bit 10 (SUS1) can be read to check the suspend status. The SUS2 (Program Suspend Bit) sets to 1 when a program command is suspended. The SUS1 (Erase Suspend Bit) sets to 1 when an erase operation is suspended. The SUS2 or SUS1 clears to 0 when the program or erase command is resumed.

**Table 25. Acceptable Commands During Program Erase Suspend after tPSL/tESL**

| Command Name | Command Code | Suspend Type | |
|---|---|---|---|
| | | Program | Erase |
| Write Enable | 06h | * | * |
| Write Disable | 04h | * | * |
| Read Data | 03h | * | * |
| Fast Read | 0Bh | * | * |
| Dual Output Fast Read | 3Bh | * | * |
| Quad Output Fast Read | 6Bh | * | * |
| Dual I/O Fast Read | BBh | * | * |
| Quad I/O Fast Read | EBh | * | * |
| Quad I/O Word Fast Read | E7h | * | * |
| Set Burst with Wrap | 77h | * | * |
| Read Mftr/Device ID | 90h | * | * |
| Dual I/O Read Mftr/Device ID | 92h | * | * |
| Quad I/O Read Mftr/Device ID | 94h | * | * |
| Read JEDEC ID | 9Fh | * | * |


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**Table 25. Acceptable Commands During Program Erase Suspend after tPSL/tESL *(Continued)***

| | | | |
|---|---|---|---|
| Read Unique ID Number | 4Bh | * | * |
| Release Power-Down/Device ID | ABh | * | * |
| Read Security Registers | 48h | * | * |
| Read SFDP | 5Ah | * | * |
| Page Program | 02h | | * |
| Quad Page Program | 32h | | * |
| Program/Erase Resume | 7Ah | * | * |

**Table 26. Acceptable Commands During Suspend (tPSL/tESL not required)**

| Command Name | Command Code | Suspend Type | |
|---|---|---|---|
| | | Program | Erase |
| Read Status Register 1 | 05h | * | * |
| Read Status Register 2 | 35h | * | * |
| Read Status Register 3 | 15h | * | * |
| Enable Reset | 66h | * | * |
| Reset Device | 99h | * | * |

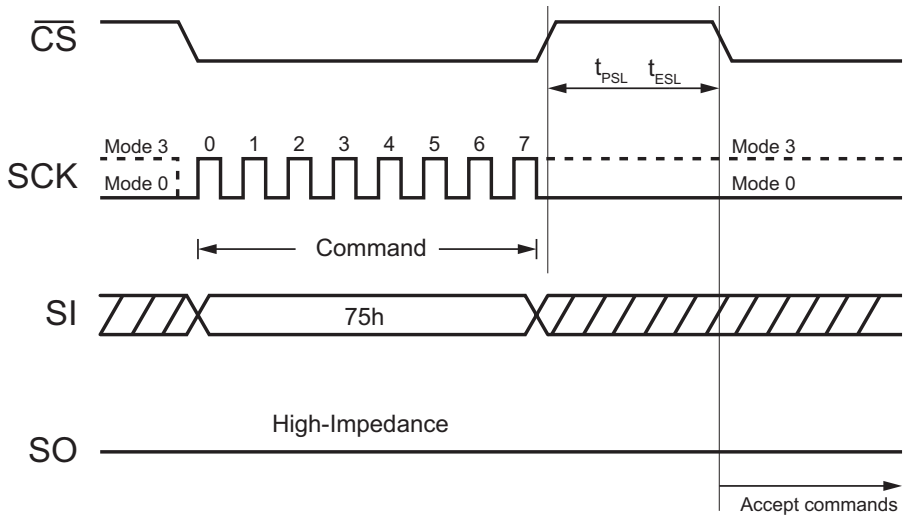


**Figure 69. Erase Suspend Command (SPI Mode)**


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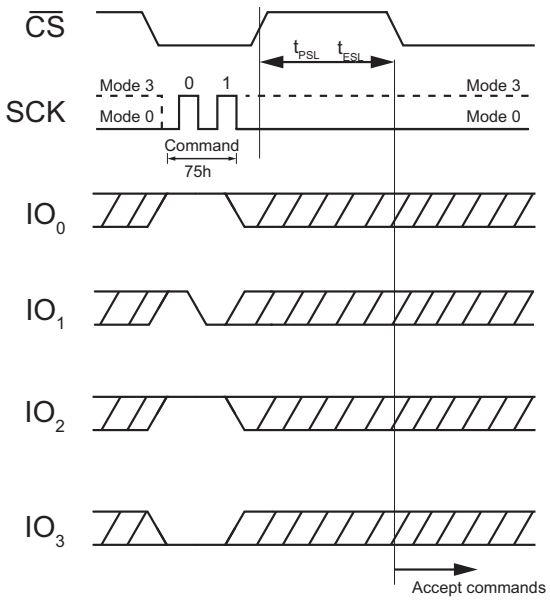


**Figure 70. Erase Suspend Command (QPI Mode)**

## 10.38 Erase / Program Resume (7Ah)

The Erase/Program Resume command 7Ah is used to restart the Block Erase operation or the Page Program operation after an Erase/Program Suspend (75h). The Resume command 7Ah is accepted by the device only if the SUS bit in the Status Register is set and the RDY/BSY bit is cleared.

After the 7Ah command is issued, hardware clears the SUS bit immediately and sets the RDY/BSY bit within 200 ns. The block completes the erase operation or the page completes the program operation. If either the SUS bit is cleared or the RDY/BSY bit is set, the Resume command 7Ah is ignored by the device.

The Resume command cannot be accepted if the previous Erase/Program Suspend operation was interrupted by unexpected power-off. It is also required that a subsequent Erase/Program Suspend command not be issued before a minimum time of $t_{ERS}$ or $t_{PRS}$ (for Erase or Program respectively) has elapsed since the previous Resume command (See Figure 71). In other words, if a Erase/Program operation is suspended multiple times, the host is required to resume for a period of at least $t_{ERS}$ or $t_{PRS}$ before issuing a subsequent suspend request.

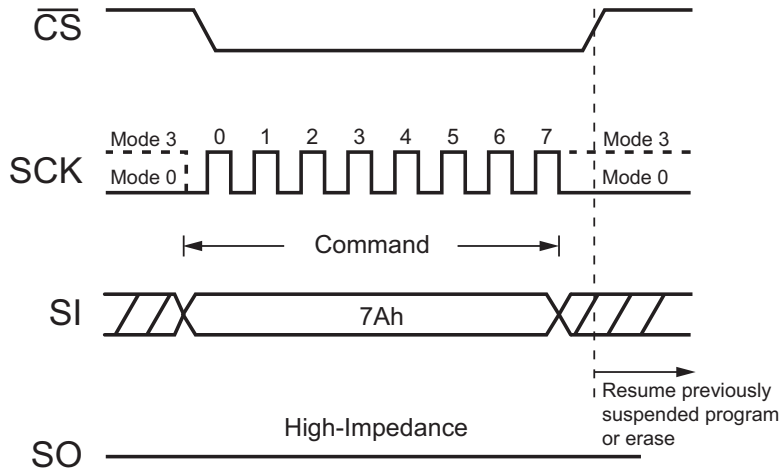


**Figure 71. Erase / Program Resume Command (SPI Mode)**


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# 11. Electrical Characteristics

## 11.1 Absolute Maximum Ratings

**Table 27. Absolute Maximum Ratings** [1]

| Parameter | Symbol | Conditions | Range | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | -0.6 to $V_{CC}$+0.6 | V |
| Voltage Applied to Any Pin | $V_{IO}$ | Relative to Ground | -0.6 to $V_{CC}$ +0.6 | V |
| Transient Voltage on any Pin | $V_{IOT}$ | <20 ns Transient Relative to Ground | -1.0 V to $V_{CC}$ +1.0 V | V |
| Storage Temperature | $T_{STG}$ | | -65 to +150 | ˚C |
| Lead Temperature | $T_{LEAD}$ | | See Note 2 | ˚C |
| Electrostatic Discharge Voltage | $V_{ESD}$ | Human Body Model [3] | -2000 to +2000 | V |

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. The “Absolute Maximum Ratings” are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Voltage extremes referenced in the “Absolute Maximum Ratings” are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).

## 11.2 Operating Ranges

**Table 28. Device Operating Rate**

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | $F_R$ = 133 MHz (Single/Dual/Quad SPI)<br>$f_R$ = 100 MHz (Read Data 03h) | 1.65 | 1.95 | V |
| Ambient Operating Temperature | $T_A$ | Industrial | -40 | +85 | ˚C |

## 11.3 Latch-up Characteristics

**Table 29. Latch-up Characteristics**

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Input Voltage with respect to GND on I/O Pins | -1.0 | $V_{CC}$ + 1.0 | V |
| $V_{CC}$ Current | -100 | +100 | mA |


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## 11.4 Power-Up Timing and Write Inhibit Threshold

**Table 30. Power-up Timing and Write Inhibit Threshold Parameters**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ (min) to $\overline{CS}$ Low | $t_{VSL}$ | 1.2 | | ms |
| Write Inhibit Threshold Voltage | $V_{WI}$ | 1 | 1.4 | V |
| $V_{CC}$ rise time (from 0 to $V_{CC}$ min). | $t_{VR}$ | | 6000 | µs/V |
| $V_{CC}$ Minimum time duration below $V_{PWDMAX}$ to guarantee reset. | $t_{PWD}$ | 300 | | µs |
| $V_{CC}$ level below which a reset is guaranteed. | $V_{PWDMAX}$ | | 0.2 | V |

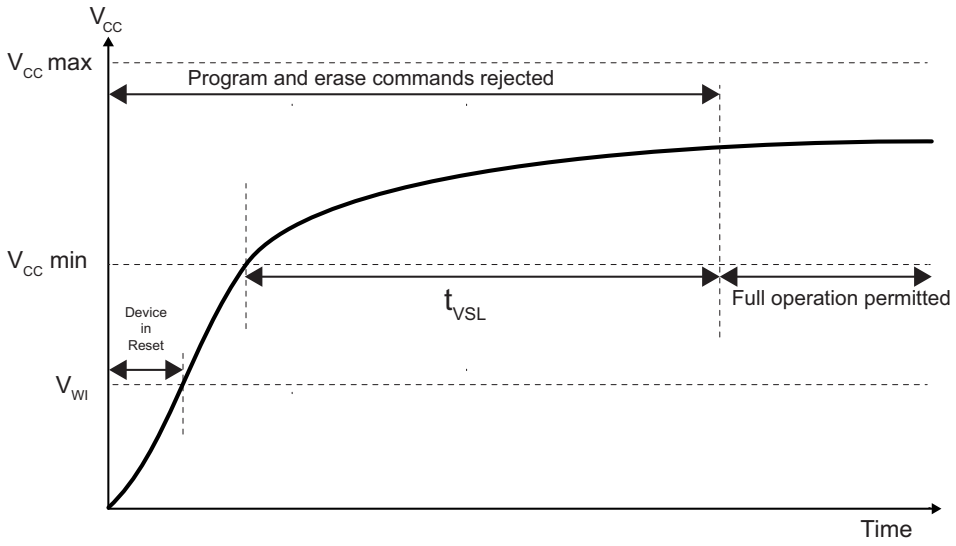


**Figure 72. Power-up Timing and Voltage Levels**

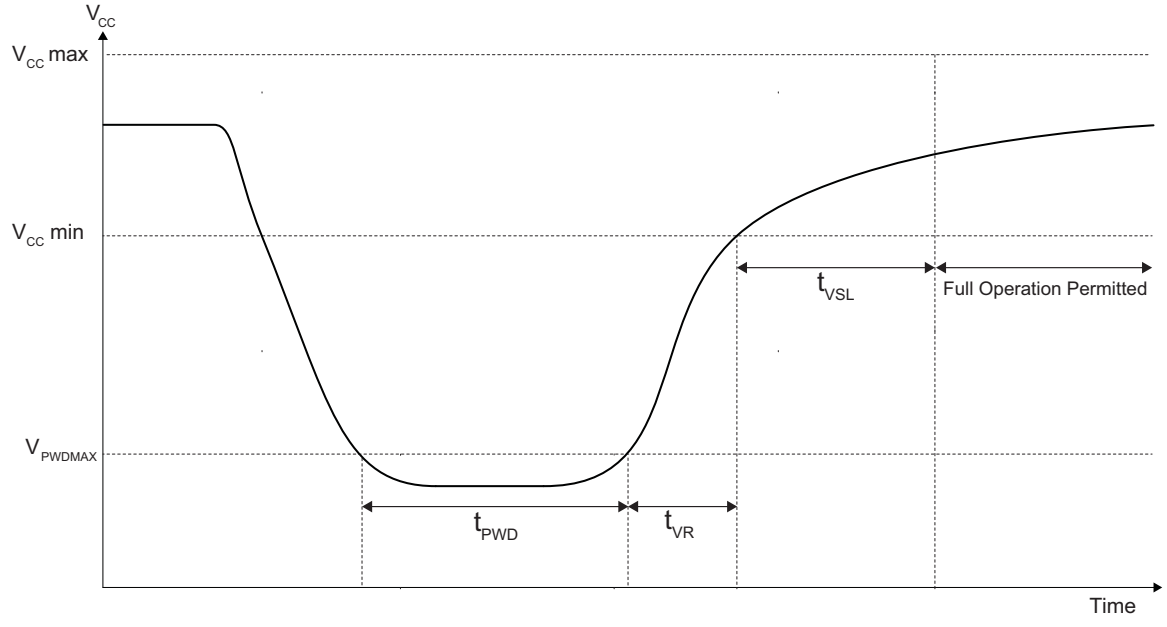


**Figure 73. Power-up Timing After Brown-Out**


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## 11.5 DC Electrical Characteristics

**Table 31. DC Electrical Characteristics for -40 ˚C to +85 ˚C**

| Parameter | Symbol | Condition | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| Input Leakage | $I_{LI}$ | | | | ±2 | µA |
| I/O Leakage | $I_{LO}$ | | | | ±2 | µA |
| Standby Current | $I_{CC1}$ | $\overline{CS}$ = $V_{CC}$, $V_{IN}$ = GND or $V_{CC}$ | | 3.5 | 30 | µA |
| Deep Power-Down Current | $I_{CC2}$ | $\overline{CS}$ = $V_{CC}$, $V_{IN}$ = GND or $V_{CC}$ | | 0.3 | 5 | µA |
| Current Read Data/ Dual/Quad 80 MHz | $I_{CC3}$ | C = 0.1 $V_{CC}$ / 0.9 $V_{CC}$ IO = Open (*1, *2, *4 IO) | | 3.2 | 5 | mA |
| Current Read Data/ Dual/Quad 133 MHz | | C = 0.1 $V_{CC}$ / 0.9 $V_{CC}$ IO = Open (*1, *2, *4 IO) | | 5.0 | 6 | mA |
| Current Page Program | $I_{CC4}$ | $\overline{CS}$ = $V_{CC}$ | | 3.8 | 7 | mA |
| Current Write Status Register | $I_{CC5}$ | $\overline{CS}$ = $V_{CC}$ | | 3 | 4.5 | mA |
| Current Block Erase (4 kB) | $I_{CC6}$ | $\overline{CS}$ = $V_{CC}$ | | 5 | 8.5 | mA |
| Current Block Erase (32/64 kB) | $I_{CC7}$ | $\overline{CS}$ = $V_{CC}$ | | 5 | 8.5 | mA |
| Current Chip Erase | $I_{CC8}$ | $\overline{CS}$ = $V_{CC}$ | | 5 | 8.5 | mA |
| Input Low Voltage | $V_{IL}$ | | -0.5 | | $V_{CC}$ x 0.2 | V |
| Input High Voltage | $V_{IH}$ | | $V_{CC}$ x 0.8 | | $V_{CC}$ + 0.4 | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 100 µA | | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -100 µA | $V_{CC}$ - 0.2 | | | V |

1. Typical values measured at 1.8 V, 25 ˚C.


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## 11.6 AC Measurement Conditions

**Table 32. AC Measurement Conditions**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Load Capacitance | $C_L$ | | 30 | pF |
| Input Rise and Fall Times | $T_R$, $T_F$ | | 5 | ns |
| Input Pulse Voltages | $V_{IN}$ | 0.2 $V_{CC}$ to 0.8 $V_{CC}$ | | V |
| Input Timing Reference Voltages | IN | 0.5 $V_{CC}$ | | V |
| Output Timing Reference Voltages | OUT | 0.5 $V_{CC}$ | | V |

1. Output Hi-Z is defined as the point where data out is no longer driven

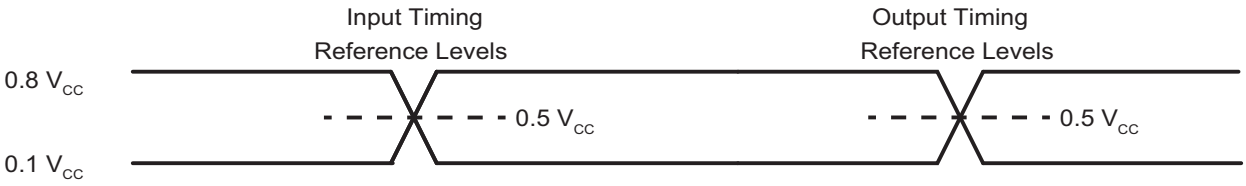


**Figure 74. AC Measurement I/O Waveform**


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## 11.7 AC Electrical Characteristics

**Table 33. AC Electrical Characteristics for -40 ˚C to +85 ˚C**

| Parameter | Symbol | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|
| Clock frequency for all commands, except Read Data command (03h) 1.7 V - 1.95 V $V_{CC}$ and industrial temperature | $F_R$ | D.C. | | 133 | MHz |
| Clock freq. Read Data command in SPI mode (03h) | $f_R$ | D.C. | | 100 | MHz |
| Clock High, Low Time | $t_{CLH}$, $t_{CLL}$ | 45% ($1/F_R$) | | | ns |
| Clock Rise Time peak to peak | $t_{CLCH}$[3] | 0.2 | | | V/ns |
| Clock Fall Time peak to peak | $t_{CHCL}$[3] | 0.2 | | | V/ns |
| $\overline{CS}$ Active Setup Time relative to Clock | $t_{SLCH}$ | 5 | | | ns |
| $\overline{CS}$ Active Hold Time relative to Clock | $t_{CHSH}$ | 5 | | | ns |
| $\overline{CS}$ Not Active Setup Time | $t_{SHCH}$ | 5 | | | ns |
| $\overline{CS}$ Not Active Hold Time | $t_{CHSL}$ | 5 | | | ns |
| $\overline{CS}$ High Time (read/write) | $t_{SHSL}$ | 20 | | | ns |
| Output Disable Time | $t_{SHQZ}$[3] | | | 8 | ns |
| Output Hold Time | $t_{CLQX}$ | 0.5 | | | ns |
| Data In Setup Time | $t_{DVCH}$ | 2 | | | ns |
| Data In Hold Time | $t_{CHDX}$ | 2 | | | ns |
| $\overline{HOLD}$ Active Setup Time relative to Clock | $t_{HLCH}$[3] | 5 | | | ns |
| $\overline{HOLD}$ Not Active Setup Time relative to Clock | $t_{HHCH}$[3] | 5 | | | ns |
| $\overline{HOLD}$ Not Active Hold Time relative to Clock | $t_{CHHL}$[3] | 5 | | | ns |
| $\overline{HOLD}$ Active Hold Time relative to Clock | $t_{CHHH}$[3] | 5 | | | ns |
| $\overline{HOLD}$ Low to High-Z | $t_{HLQZ}$[3] | | | 6 | ns |
| $\overline{HOLD}$ Low to Low-Z | $t_{HHQX}$[3] | | | 6 | ns |
| Clock Low to Output Valid | $t_{CLQV}$ | | | 7 | ns |
| Write Protect Setup Time Before $\overline{CS}$ Low | $t_{WHSL}$ | 20 | | | ns |
| Write Protect Setup Time After $\overline{CS}$ High | $t_{SHWL}$ | 100 | | | ns |
| $\overline{CS}$ High to Power-Down Mode | $t_{DP}$ | | | 1 | µs |
| $\overline{CS}$ High to Standby Mode after exit from Deep Power-Down Without Electronic Signature Read | $t_{RES1}$ | | | 20 | µs |
| $\overline{CS}$ High to Standby Mode after exit from Deep Power-Down With Electronic Signature Read | $t_{RES2}$ | | | 20 | µs |
| Erase Suspend Latency | $t_{ESL}$ | | | 45 | µs |
| Program Suspend Latency | $t_{PSL}$ | | | 30 | µs |
| Latency between Program Resume and next Suspend[5] | $t_{PRS}$ | 50 | | | µs |
| Latency between Erase Resume and next Suspend[6] | $t_{ERS}$ | 17000 | | | µs |
| $\overline{CS}$ High to next Command after Reset in standby/read | $t_{RST}$ | | | 1 | µs |
| $\overline{CS}$ High to next Command after Reset in program/erase/write SR | | | | 40 | |
| $\overline{CS}$ High to next Command after Reset in Deep Power-Down | | | | 25 | |


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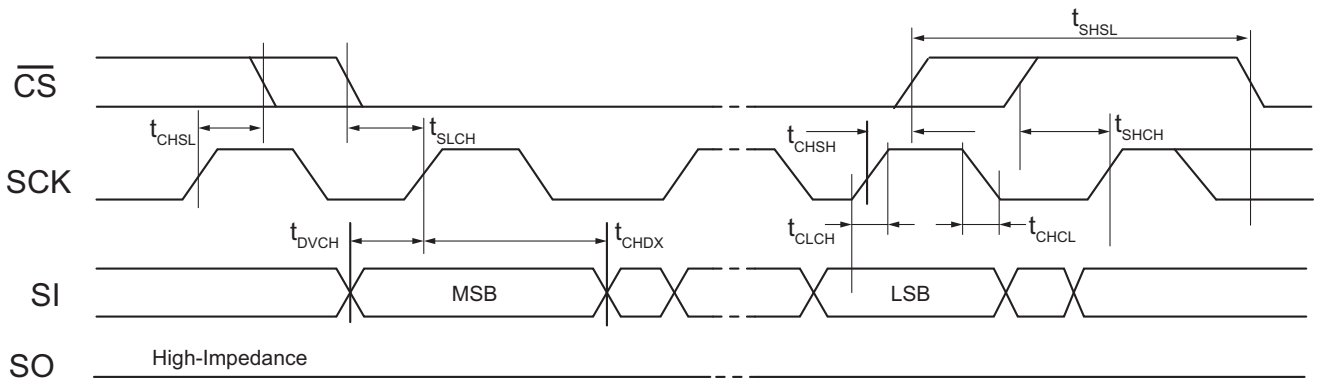
**Table 33. AC Electrical Characteristics for -40 ˚C to +85 ˚C *(Continued)***

| Parameter | Symbol | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|
| Write Status Register Cycle Time | $t_W$ | | 5 | 30 [6] | ms |
| Byte Program Time (first byte) [2] | $t_{BP1}$ | | 60 | 500 | µs |
| Byte Program Time (after first byte) [2] | $t_{BP2}$[4] | | 1.33 | 19.6 | µs |
| Page Program Time [2] | $t_{PP}$ | | 0.4 | 5.5 | ms |
| Block Erase Time (4 kB) [2] | $t_{BE}$ | | 22 | 200 | ms |
| Block Erase Time (32 kB) [2] | $t_{BE1}$ | | 85 | 800 | ms |
| Block Erase Time (64 kB) [2] | $t_{BE2}$ | | 160 | 1300 | ms |
| Chip Erase Time | $t_{CE}$ | | 40 | 80 | s |

1. Typical values measured at 1.8 V, 25 ˚C.
2. Unless specified otherwise, maximum is worst case after 100 k cycles.
3. Value guaranteed by design and/or characterization, not 100% tested in production.
4. The time to program N bytes can be calculated as follows: $t_{BP1}$ + (N-1) * $t_{BP2}$.
5. For $t_{PRS}$, there must be minimum timing before issuing the next program suspend command.
6. For $t_{ERS}$, there must be minimum timing before issuing the next erase suspend command.

## 11.8 Input Timing





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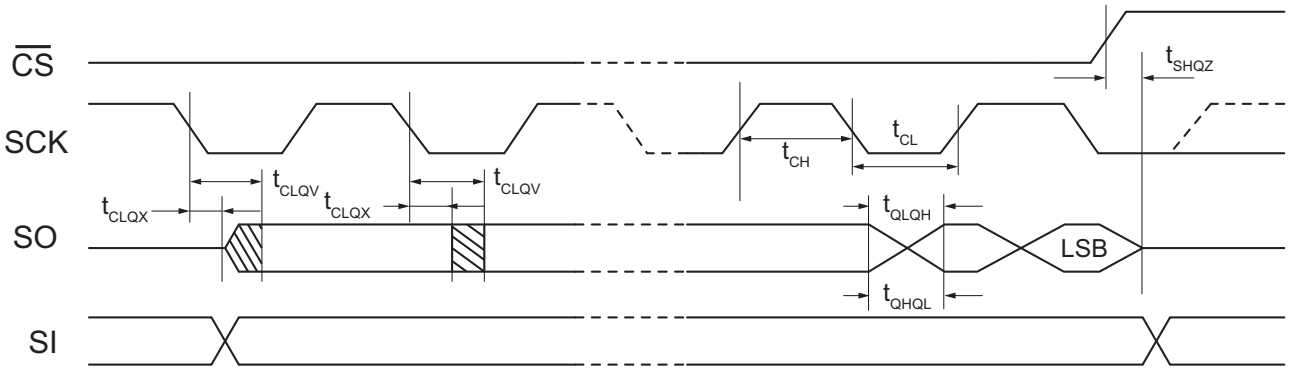
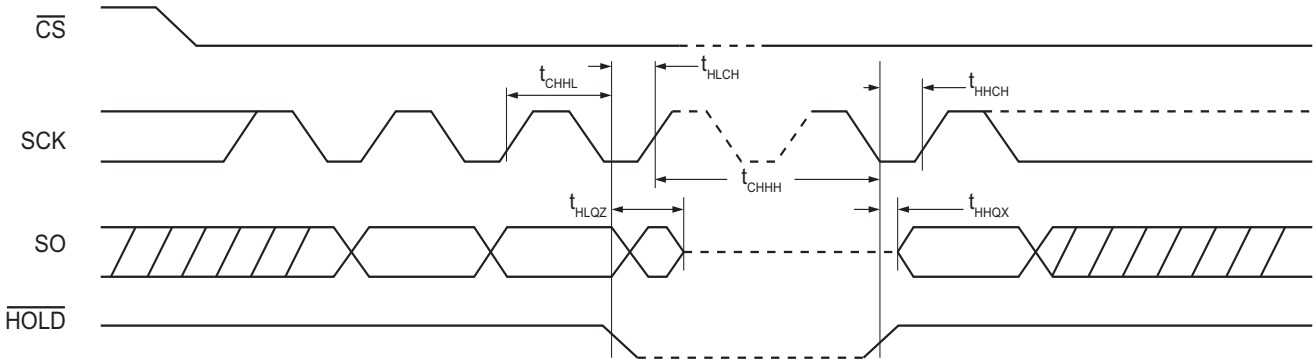
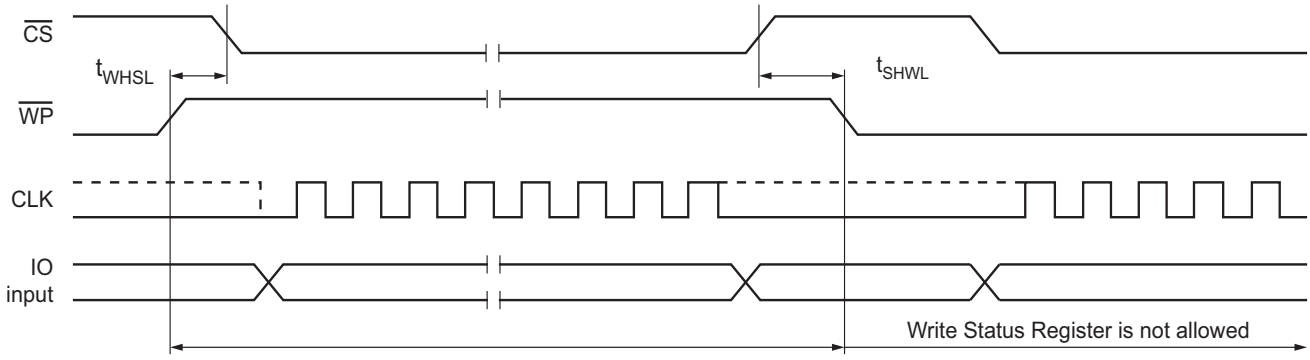
## 11.9 Output Timing




## 11.10 HOLD Timing




## 11.11 WP Timing





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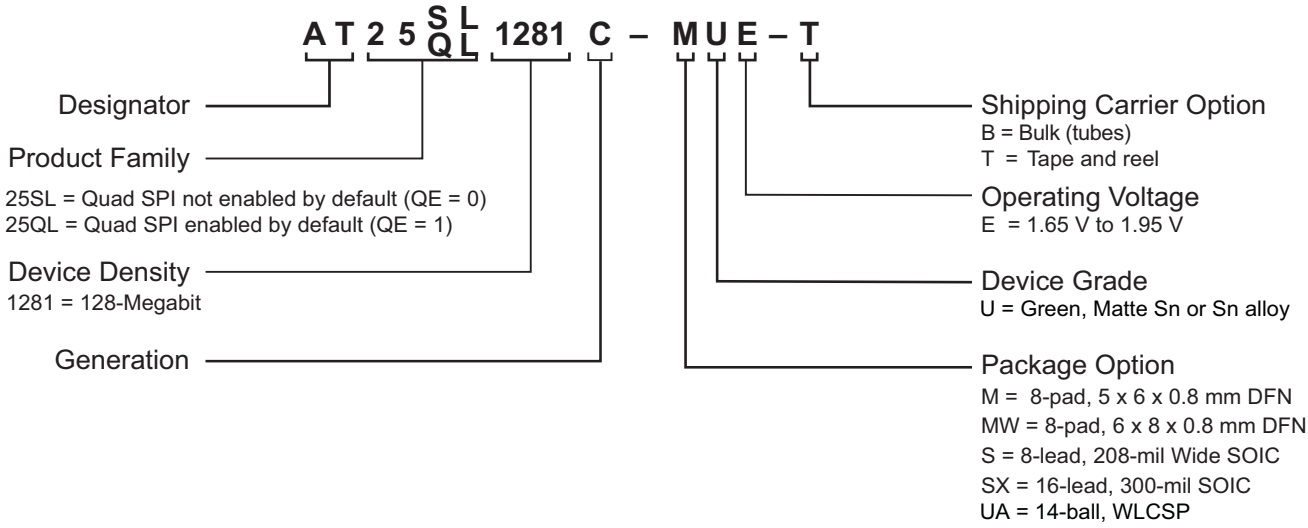
# 12. Ordering Information




| Ordering Code[1] | Package | Lead Finish | Operating Voltage | Max. Freq. | Operation Range |
|---|---|---|---|---|---|
| AT25SL1281C-MUE-T<br>AT25QL1281C-MUE-T | 8-pad, 5 x 6 x 0.8 mm DFN | Matte Sn | 1.65 V - 1.95 V | 133 MHz | -40 ˚C to 85 ˚C (Industrial Temperature Range) |
| AT25SL1281C-MWUE-T<br>AT25QL1281C-MWUE-T | 8-pad, 6 x 8 x 0.8 mm DFN | | | | |
| AT25SL1281C-SUE-T<br>AT25QL1281C-SUE-T | 8-lead, 208-mil Wide SOIC | | | | |
| AT25SL1281C-SXUE-T<br>AT25QL1281C-SXUE-T | 16-lead, 300-mil SOIC | | | | |
| AT25SL1281C-UAUE-T[2]<br>AT25QL1281C-UAUE-T[2] | 14-ball WLCSP | SnAgCu | | | |

1. The shipping carrier option code is not marked on the devices.
2. Three lot package qualification in progress.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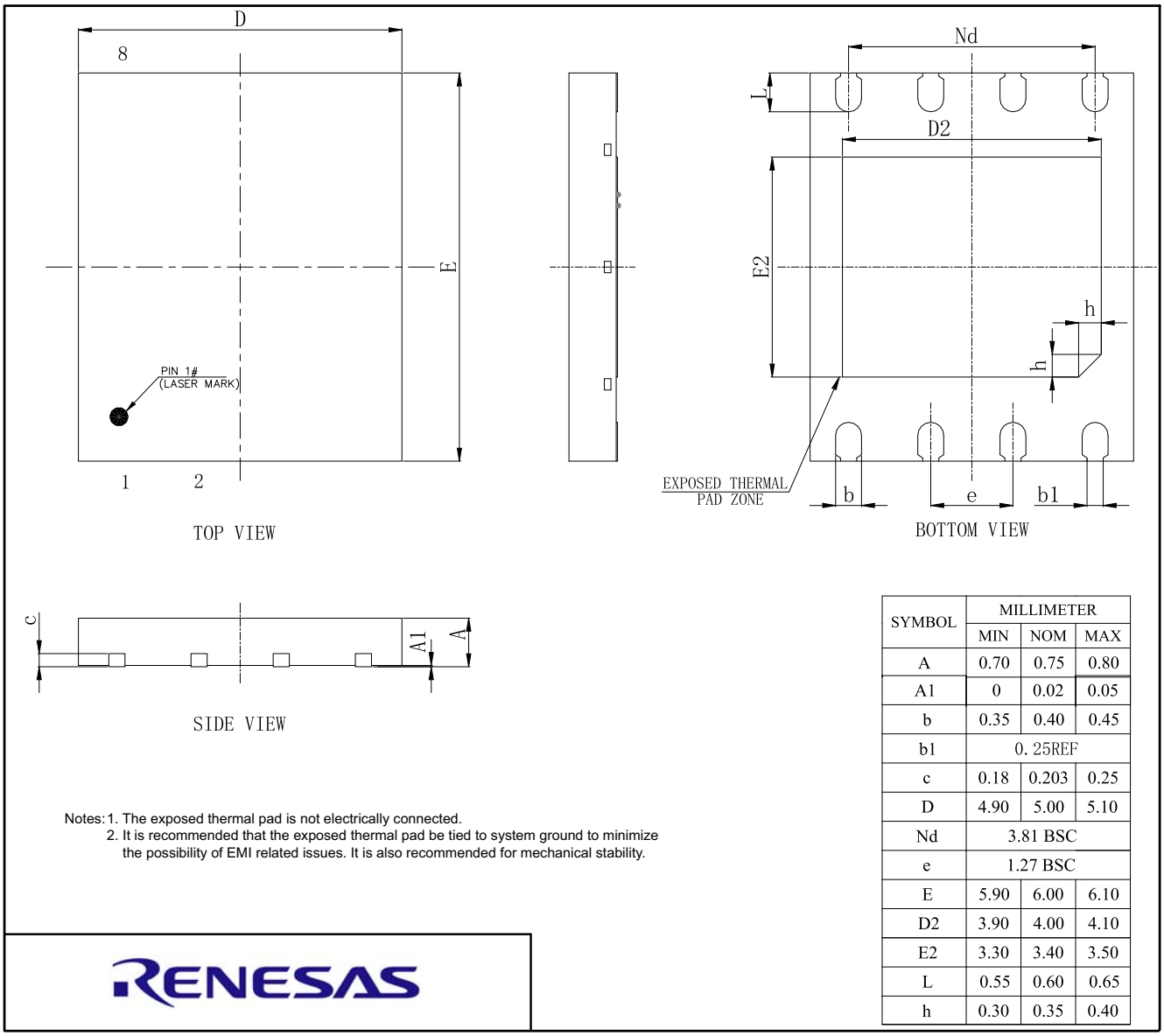
# 13. Packaging Information

## 13.1 8-Pad, 5 x 6 mm DFN




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.35 | 0.40 | 0.45 |
| b1 | 0. 25REF | | |
| c | 0.18 | 0.203 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| Nd | 3.81 BSC | | |
| e | 1.27 BSC | | |
| E | 5.90 | 6.00 | 6.10 |
| D2 | 3.90 | 4.00 | 4.10 |
| E2 | 3.30 | 3.40 | 3.50 |
| L | 0.55 | 0.60 | 0.65 |
| h | 0.30 | 0.35 | 0.40 |

Notes: 1. The exposed thermal pad is not electrically connected.
2. It is recommended that the exposed thermal pad be tied to system ground to minimize the possibility of EMI related issues. It is also recommended for mechanical stability.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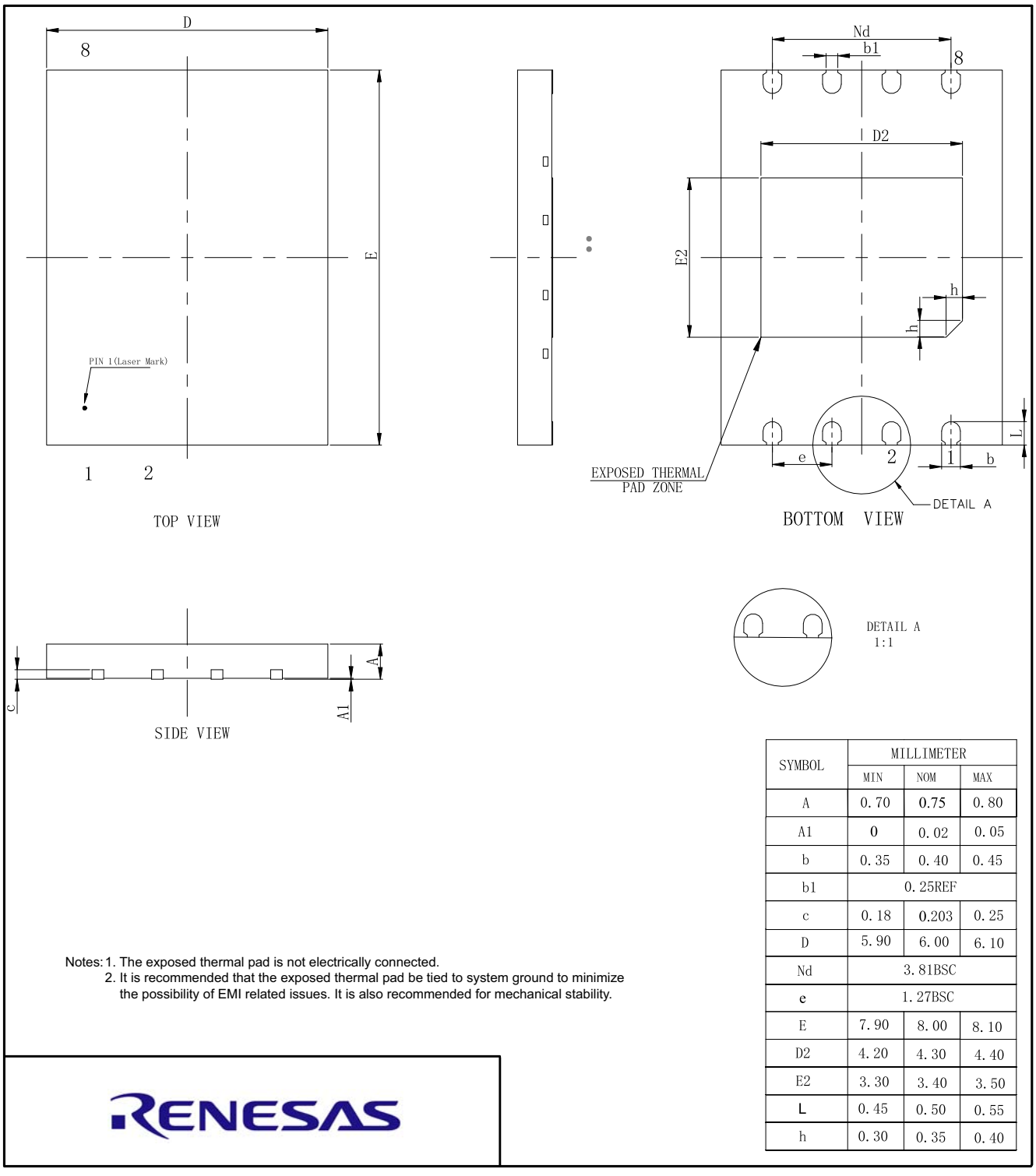
## 13.2 8-Pad, 6 x 8 mm DFN




Notes: 1. The exposed thermal pad is not electrically connected.
2. It is recommended that the exposed thermal pad be tied to system ground to minimize the possibility of EMI related issues. It is also recommended for mechanical stability.

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.35 | 0.40 | 0.45 |
| b1 | 0.25REF | | |
| c | 0.18 | 0.203 | 0.25 |
| D | 5.90 | 6.00 | 6.10 |
| Nd | 3.81BSC | | |
| e | 1.27BSC | | |
| E | 7.90 | 8.00 | 8.10 |
| D2 | 4.20 | 4.30 | 4.40 |
| E2 | 3.30 | 3.40 | 3.50 |
| L | 0.45 | 0.50 | 0.55 |
| h | 0.30 | 0.35 | 0.40 |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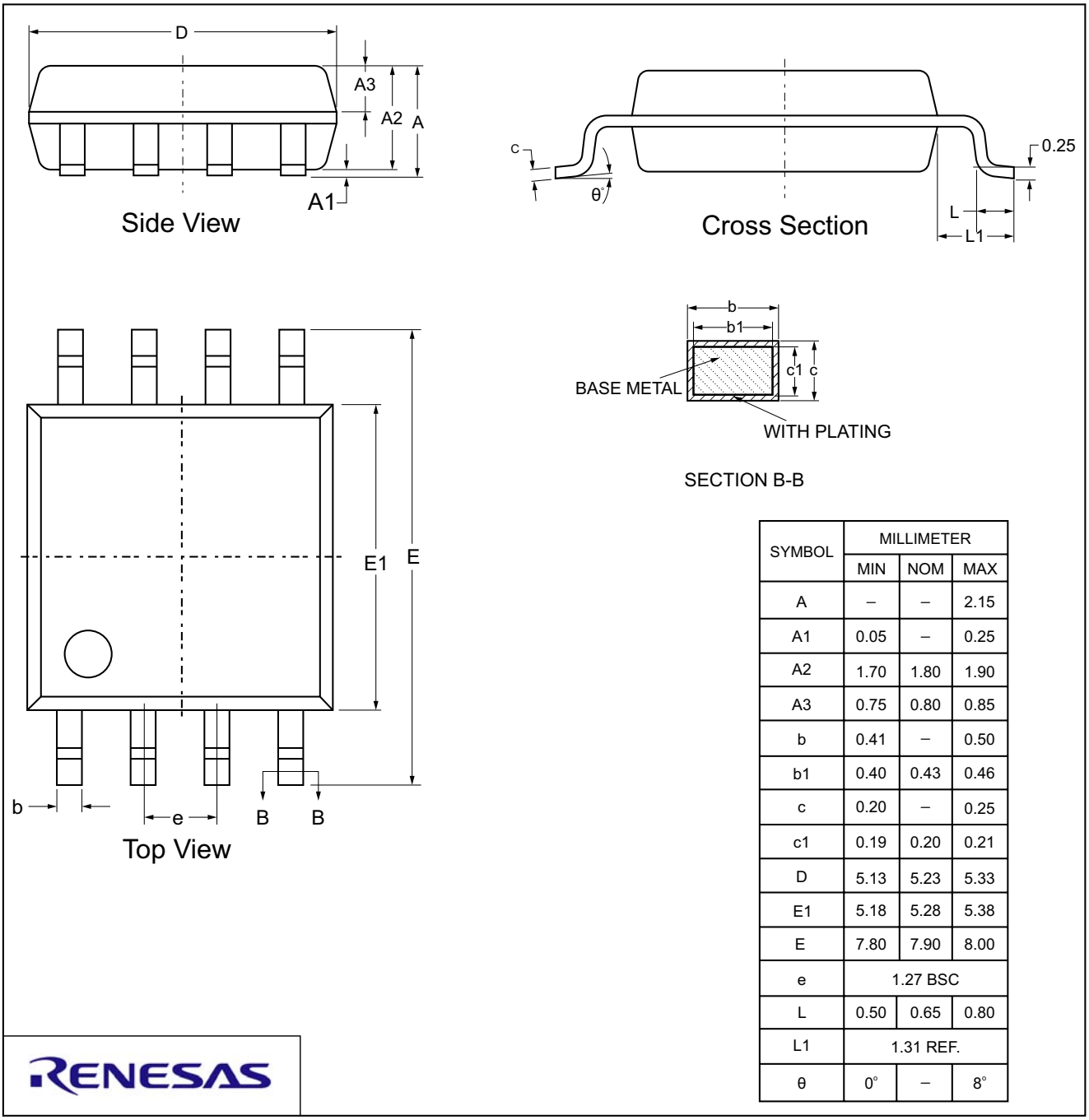
## 13.3 8-Lead, 208-mil Wide SOIC




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | – | – | 2.15 |
| A1 | 0.05 | – | 0.25 |
| A2 | 1.70 | 1.80 | 1.90 |
| A3 | 0.75 | 0.80 | 0.85 |
| b | 0.41 | – | 0.50 |
| b1 | 0.40 | 0.43 | 0.46 |
| c | 0.20 | – | 0.25 |
| c1 | 0.19 | 0.20 | 0.21 |
| D | 5.13 | 5.23 | 5.33 |
| E1 | 5.18 | 5.28 | 5.38 |
| E | 7.80 | 7.90 | 8.00 |
| e | 1.27 BSC | | |
| L | 0.50 | 0.65 | 0.80 |
| L1 | 1.31 REF. | | |
| θ | 0° | – | 8° |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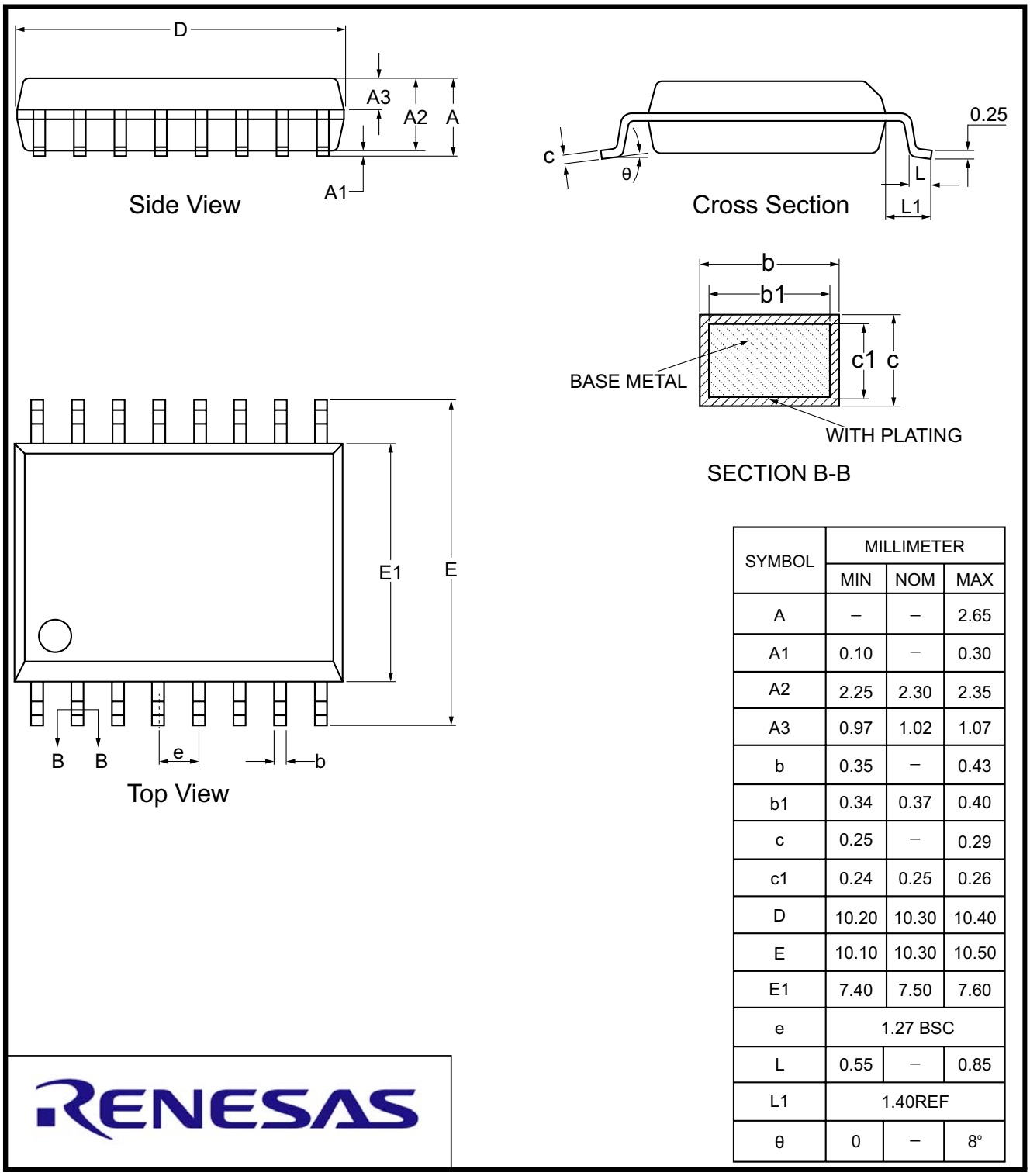
## 13.4 16-Lead, 300-mil SOIC




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | – | – | 2.65 |
| A1 | 0.10 | – | 0.30 |
| A2 | 2.25 | 2.30 | 2.35 |
| A3 | 0.97 | 1.02 | 1.07 |
| b | 0.35 | – | 0.43 |
| b1 | 0.34 | 0.37 | 0.40 |
| c | 0.25 | – | 0.29 |
| c1 | 0.24 | 0.25 | 0.26 |
| D | 10.20 | 10.30 | 10.40 |
| E | 10.10 | 10.30 | 10.50 |
| E1 | 7.40 | 7.50 | 7.60 |
| e | 1.27 BSC | | |
| L | 0.55 | – | 0.85 |
| L1 | 1.40REF | | |
| θ | 0 | – | 8° |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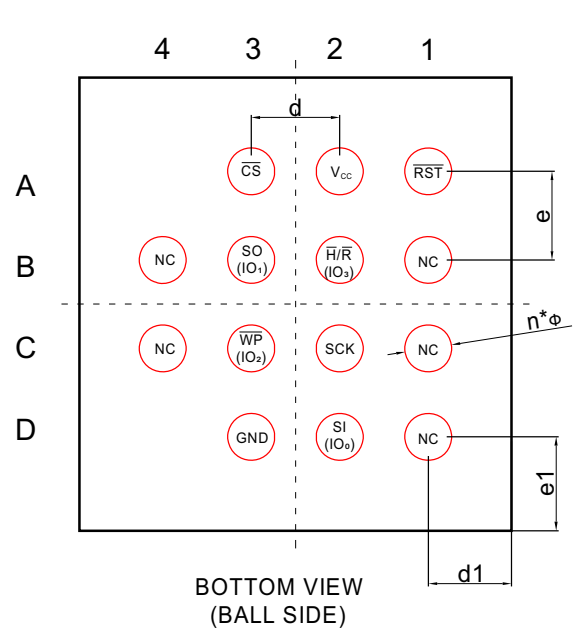
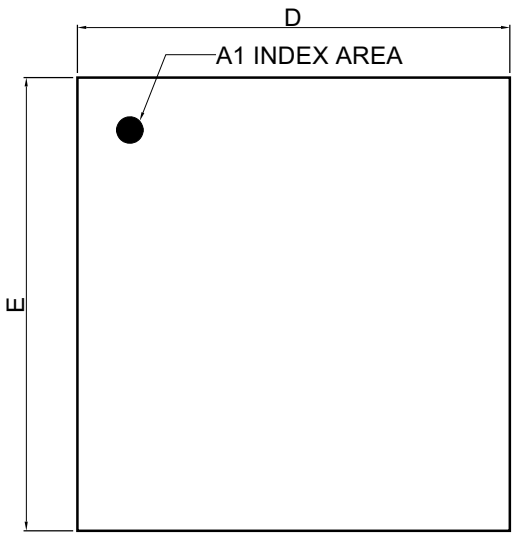
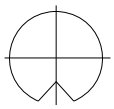
## 13.5 14-Ball, WLCSP



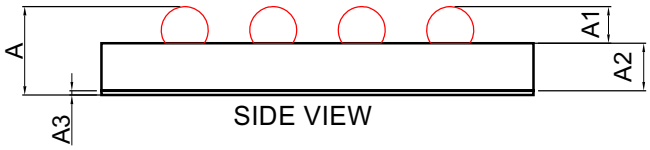

BOTTOM VIEW
(BALL SIDE)




TOP VIEW
(MARK SIDE)



NOTCH DIRECTION




SIDE VIEW

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | ITEM | MIN | NOM | MAX |
|---|---|---|---|---|
| A | PACKAGE HEIGHT | 0.480 | 0.517 | 0.554 |
| A1 | BALL HEIGHT | 0.153 | 0.173 | 0.193 |
| A2 | WAFER THICKNESS | 0.305 | 0.319 | 0.333 |
| A3 | BACKSIDE FILM THICKNESS | 0.022 | 0.025 | 0.028 |
| Φ | BALL DIAMETER | 0.280 | 0.300 | 0.320 |
| D | PACKAGE SIZE X | 2.428 | 2.443 | 2.458 |
| E | PACKAGE SIZE Y | 2.545 | 2.560 | 2.575 |
| d | MIN BALL PITCH X | 0.500 | | |
| d1 | MIN BALL CENTER TO PACKAGE SIZE X AXIS | 0.471 | | |
| e | MIN BALL PITCH Y | 0.500 | | |
| e1 | MIN BALL CENTER TO PACKAGE SIZE Y AXIS | 0.530 | | |
| n | BALL COUNT | 14 | | |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# 14. Revision History

| Revision Level | Date | Change History |
|---|---|---|
| A | 7/2024 | Initial release. |
| B | 02/2025 | Changed ‘UDFN’ to ‘DFN.’<br>Changed ‘$V_{SS}$’ to ‘GND.’<br>Changed ‘Write in Progress (WIP)’ to ‘Ready/Busy (RDY/BSY).’<br>Removed Figure 4 ‘14-WLCSP (Bottom View, Ball Side).’<br>In Table 2 ‘Status Register-1’ changed “Erase or Write in Progress” to “Erase or Program in Progress.”<br>Added “(Default)” to 50% value in Driver Strength column of Table 7 ‘Status Register Protection,’ and removed it from 100% value.<br>Updated wording and restructured tables in Section 7 ‘Status Registers.’<br>Updated Table 8 ‘Status Register Memory Protection (CMP = 0).’<br>Updated Table 9 ‘Status Register Memory Protection (CMP = 1).’<br>Clarified status register bit designations in Table 11 ‘Command Set Table 1 (Standard/Dual/Quad SPI Commands)’ and Table 13 ‘Command Set Table 3 (QPI Commands).’<br>Made corrections to Table 11 ‘Command Set Table 1 (Standard/Dual/Quad SPI Commands).’<br>Made corrections to Table 13 ‘Command Set Table 3 (QPI Commands).’<br>Updated Section 10.38 ‘Erase / Program Resume (7Ah).’<br>Removed Section 11.3 ‘Endurance and Data Retention.’<br>Updated Section 10.14.1 ‘Continuous Read Mode.’<br>Updated title and corrected Figure 26 ‘Fast Read Dual I/O Command (first time or after previous command has Mode bits M5-4 not equal to 1,0).’<br>Corrected Figure 27 ‘Fast Read Dual I/O Sequence Diagram (previous M5-4 = 1,0) SPI Mode Only.’<br>Updated Section 10.15 ‘Fast Read Quad I/O (EBh).’<br>Updated Section 10.15.1 ‘Continuous Read Mode.’<br>Updated title of Figure 28 ‘Fast Read Quad I/O Command (first time or after previous command has mode bits M5-4 not equal to 1,0; SPI Mode).’<br>Updated title of Figure 30 ‘Fast Read Quad I/O Command (first time or after previous command has mode bits M5-4 not equal to 1,0; QPI mode).’<br>Updated Table 29 ‘Power-up Timing and Write Inhibit Threshold Parameters.’<br>Updated Figure 71 ‘Power-up Timing and Voltage Levels.’<br>Added Figure 72 ‘Power-up Timing After Brown-Out.’<br>Updated footnotes of Table 30 ‘DC Electrical Characteristics for -40 ˚C to +85 ˚C.’<br>Updated footnotes of Table 32 ‘AC Electrical Characteristics for -40 ˚C to +85 ˚C.’<br>Removed WLCSP POD from Section 13.5.<br>Added notes regarding the exposed thermal pad to the ‘8-Pad, 5 x 6 mm DFN’ and ‘8-Pad, 6 x 8 mm DFN’ PODs.<br>Added note to “Contact Renesas Electronics for Availability” regarding the WLCSP package. |


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| Revision Level | Date | Change History |
|---|---|---|
| C | 12/2025 | Added data from the AT25QL1281C to the datasheet.<br>Removed ‘Advance’ status from the datasheet.<br>Removed ‘SEC’ and ‘TB’ from datasheet and replaced with ‘BP4’ and ‘BP3’ respectively.<br>Corrected device voltage from ‘1.65-2.00 V’ to ‘1.65-1.95 V.’<br>Updated Features page.<br>Updated Figure 4 ‘14-ball WLCSP (Ball Side View).’<br>Updated Section 5.1 ‘Standard SPI Operation.’<br>Updated Section 6.1.1 ‘Operating Supply Voltage.’<br>Updated Table 10 ‘Manufacturer and Device ID Information for the AT25SL1281C’<br>Added Table 11 ‘Manufacturer and Device ID Information for the AT25QL1281C’<br>Corrected Table 12 ‘Command Set Table 1 (Standard/Dual/Quad SPI Commands).’<br>Updated Table 13 ‘Command Set Table 2 (Standard/Dual/Quad SPI Commands).’<br>Corrected Table 28 ‘Device Operating Range.’<br>Updated Table 30 ‘Power-Up Timing and Write Inhibit Threshold Parameters.<br>Updated Table 31 ‘DC Electrical Characteristics for -40 ˚C to +85 ˚C.’<br>Updated Table 33 ‘AC Electrical Characteristics for -40 ˚C to +85 ˚C.’<br>Added part numbers for the AT25QL1281C to Section 12 ‘Ordering Information.’<br>Added POD to Section 13.5 ‘14-Ball, WLCSP.’ |


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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com


### Contact Information

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