CA91L862A (QSpan II)

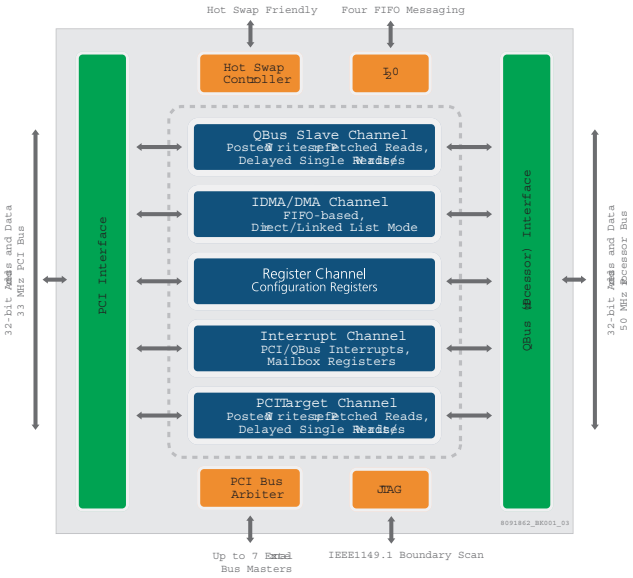
PowerQUICC-to-PCI Bridge

The CA91L862A is a PCI-to-Host processor bridge for the NXP® PowerQUICC (MPC860/850/821), the QUICC (MC68360), and the MC68040.

The CA91L862A operates at speeds up to 50 MHz on the Host processor bus, with programmable parity and burst/prefetch capability. Its 32-bit/33 MHz PCI 2.2 Interface support is ideal for embedded processor applications.

Another key feature of the CA91L862A is its integrated PCI bus arbiter. This arbiter supports up to seven external bus masters and uses a fairness algorithm to prevent deadlocks on the bus.

Block Diagram



Features

- High-Performance Processor Interface
  - MPC860 interface supports prefetched reads and burst writes
  - Operates up to 50 MHz
- High-Performance PCI Bus Interface
  - Zero-wait state bursts, prefetch reads and writes on PCI
  - Serial EEPROM interface for Plug and Play compatibility on PCI
  - Universal PCI signaling (3.3 and 5V compliant)
- PCI version 2.2 Enhancements
  - Vital Product Data: offers an improved method of communicating board-specific information to the system
  - PCI Power Management interface: enables operating systems to control the power supplied to CA91L862A related hardware (for example, an add-in card)
- Integrated PCI Bus Arbiter
  - Supports up to seven external bus masters
  - Fairness algorithm for preventing deadlocks
- CompactPCI Hot Swap Friendly
- High-performance DMA controller with support for Direct and Linked List modes
- Mailbox registers for passing parameters between host and embedded environments

Applications

- LAN/WAN Infrastructure
  - Network interface cards
  - Routers (including SOHO applications)
  - Servers
- Remote and Local Access Equipment
  - xDSL concentrators
  - VoIP gateways
- CPE Equipment
  - Process control equipment
  - Data acquisition systems

Contents

1. Overview

The CA91L862A™ chip is a member of Renesas' family of PCI bus-bridging devices. CA91L862A enables board designers to bring PCI-based embedded products to market faster, for less cost, and with high performance.

Developed as part of a strategic relationship with NXP, CA91L862A is designed to gluelessly bridge the MC68360 (QUICC™), the MPC860 (PowerQUICC™), other MPCxxx devices, and the M68040/M68060 to PCI (see Figure 1). With additional glue logic, CA91L862A can also be connected to lower-end communications controllers and processors, such as the MC68302 and MC68030.

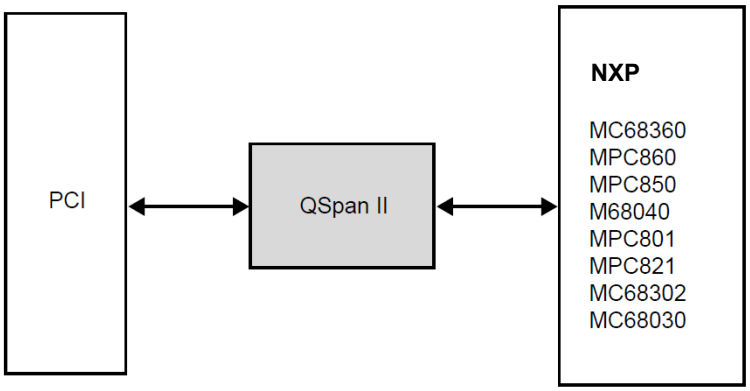


Figure 1. CA91L862A Bridging PCI and Processor Buses

1.1 Typical Applications

For typical applications information, see "Appendix C" in the *QSpan II User Manual*.

2. Pin Information

2.1 Terminology

The following abbreviations are used in this chapter:

in	Defines a signal as a standard input-only signal.
out	Defines a signal as a standard output-only signal.
t/s	Defines a signal as a bidirectional, tristate input/output signal.
s/t/s	Defines a signal as a sustained tristate signal that is driven by one owner at a time.
o/d	Defines a signal as an open drain.

2.2 Overview

CA91L862A's QBus Interface defines a number of signals that can be mapped to MC68360 (QUICC), MPC860 (PowerQUICC), or M68040 buses (see the following table).

Table 1. QBus Signal Names Compared to NXP Signals

QBus Interface	MC68360	MPC860	M68040
BB_/BGACK_	BGACK_	BB_	BB_
BERR_/TEA_	BERR_	TEA_	TEA_
BURST_/TIP_	N/A	BURST_	TIP_
DACK_/SDACK_	DACK_	SDACK_	N/A
DSACK1_/TA_	DSACK1_	TA_	TA_
SIZ[1:0]	SIZ[1:0]	TSIZ[0:1]	SIZ[1:0]
TC[3:0]	FC[3:0]	AT[0:3]	TT[1:0] TM[2:0][1]
HALT_/TRETRY_	HALT_	TRETRY_	N/A

1. TC[3:0] can be connected to four out of the five TT[1:0] and TM[2:0] M68040 signals. The unused TC pins, if any, must be connected to pull-up resistors (see Appendix C: "Typical Applications" in the *QSpan II User Manual*).

Note: MPC860 signals do not necessarily operate in the same manner as MC68360 signals of the same name.

2.3 Pin Assignments

Table 2. Pin Assignments – 17x17 mm Package

A1. N/C	D5. D[21]	G9. VSS	K13. TDO	P1. AD[30]
A2. D[25]	D6. A[23]	G10. VSS	K14. BDIP_	P2. AD[29]
A3. D[23]	D7. A[17]	G11. VSS	K15. TDI	P3. AD[26]
A4. D[22]	D8. QCLK	G12. VDD	K16. BG_	P4. EXT_GNT[4]#
A5. DP[0]	D9. D[14]	G13. DREQ_	L1. BR_	P5. AD[21]
A6. A[25]	D10. D[12]	G14. A[0]	L2. BB_/BGACK_	P6. AD[16]
A7. A[21]	D11. A[12]	G15. A[2]	L3. N/C	P7. FRAME#
A8. A[20]	D12. A[10]	G16. A[1]	L4. BURST_/TIP_	P8. PCLK
A9. A[16]	D13. N/C	H1. TMODE[1]	L5. VDD	P9. AD[15]
A10. D[17]	D14. D[7]	H2. HS_LED	L6. VSS	P10. AD[11]
A11. D[13]	D15. D[4]	H3. SCL	L7. VSS	P11. AD[9]
A12. A[14]	D16. D[3]	H4. IMSEL	L8. VSS	P12. AD[7]
A13. A[13]	E1. A[29]	H5. VDD	L9. VSS	P13. EXT_REQ[4]#
A14. TEST2	E2. N/C	H6. VSS	L10. VSS	P14. AD[6]
A15. A[9]	E3. A[27]	H7. VSS	L11. VSS	P15. AD[3]
A16. VH	E4. A[28]	H8. VSS	L12. VDD	P16. CSPCI_
B1. D[28]	E5. VDD	H9. VSS	L13. TC3	R1. EXT_GNT[1]#
B2. VH	E6. VDD	H10. VSS	L14. TC1	R2. AD[24]
B3. D[26]	E7. VDD	H11. VSS	L15. BERR_/TEA_	R3. AD[25]
B4. D[24]	E8. VDD	H12. VDD	L16. AS_	R4. EXT_GNT[2]#
B5. DP[2]	E9. VDD	H13. TCK	M1. HALT_/TRETRY_	R5. EXT_GNT[5]#
B6. D[20]	E10. VDD	H14. TRST_	M2. RST#	R6. AD[19]
B7. A[22]	E11. VDD	H15. ENID	M3. GNT#	R7. IRDY#
B8. A[18]	E12. VDD	H16. QINT_	M4. REQ#	R8. DEVSEL#
B9. D[18]	E13. D[6]	J1. PME#	M5. VDD	R9. CBE[1]
B10. D[15]	E14. D[2]	J2. HS_SWITCH	M6. VDD	R10. AD[12]
B11. A[15]	E15. D[1]	J3. TMODE[0]	M7. VDD	R11. CBE[0]
B12. TEST1	E16. A[5]	J4. RESETI_	M8. VDD	R12. EXT_REQ[2]#
B13. N/C	F1. DSACK1_/TA_	J5. VDD	M9. VDD	R13. EXT_REQ[6]#
B14. D[10]	F2. A[31]	J6. VSS	M10. VDD	R14. N/C
B15. D[11]	F3. A[30]	J7. VSS	M11. VDD	R15. VH
B16. A[7]	F4. SIZ[1]	J8. VSS	M12. VDD	R16. N/C
C1. A[26]	F5. VDD	J9. VSS	M13. CSREG_	T1. AD[23]
C2. D[31]	F6. VSS	J10. VSS	M14. INT#	T2. CBE[3]
C3. D[27]	F7. VSS	J11. VSS	M15. SERR#	T3. EXT_GNT[3]#
C4. PCI_ARB_EN	F8. VSS	J12. VDD	M16. TC[2]	T4. EXT_GNT[6]#
C5. DP[1]	F9. VSS	J13. DACK_/SDACK_	N1. VH	T5. AD[18]
C6. A[24]	F10. VSS	J14. BM_EN/FIFO_RDY_	N2. AD[31]	T6. AD[17]
C7. A[19]	F11. VSS	J15. DONE_	N3. AD[27]	T7. STOP#
C8. D[19]	F12. VDD	J16. TMS	N4. AD[28]	T8. AD[14]
C9. D[16]	F13. D[5]	K1. RESETO_	N5. AD[22]	T9. AD[13]
C10. DS_	F14. A[3]	K2. TS_	N6. AD[20]	T10. AD[8]
C11. A[11]	F15. D[0]	K3. PCI_DIS	N7. CBE[2]	T11. EXT_REQ[1]#
C12. TEST3	F16. A[4]	K4. HS_HEALTHY_	N8. TRDY#	T12. EXT_REQ[5]#
C13. A[6]	G1. SDA	K5. VDD	N9. PERR#	T13. AD[5]
C14. A[8]	G2. SIZ[0]	K6. VSS	N10. PAR	T14. AD[4]
C15. D[9]	G3. DSACK0_	K7. VSS	N11. AD[10]	T15. N/C
C16. D[8]	G4. ENUM#	K8. VSS	N12. IDSEL	T16. AD[2]
D1. R/W_	G5. VDD	K9. VSS	N13. EXT_REQ[3]#	
D2. D[30]	G6. VSS	K10. VSS	N14. AD[1]	
D3. D[29]	G7. VSS	K11. VSS	N15. AD[0]	
D4. DP[3]	G8. VSS	K12. VDD	N16. TC[0]	

Table 3. Pin Assignments – 27x27 mm Package

A1. VSS
A2. D[26]
A3. D[22]
A4. DP[2]
A5. VDD
A6. A[24]
A7. A[22]
A8. VSS
A9. A[17]
A10. QCLK
A11. D[17]
A12. VSS
A13. DS_
A14. A[13]
A15. N/C
A16. N/C
A17. N/C
A18. A[8]
A19. D[11]
A20. D[9]
B1. D[28]
B2. VDD
B3. D[25]
B4. PCI_ARB_EN
B5. DP[1]
B6. D[20]
B7. A[23]
B8. A[20]
B9. N/C
B10. D[18]
B11. D[15]
B12. D[14]
B13. A[15]
B14. A[12]
B15. TEST1
B16. A[9]
B17. A[7]
B18. D[10]
B19. D[7]
B20. D[6]
C1. D[30]
C2. D[27]
C3. N/C
C4. D[23]
C5. DP[3]
C6. DP[0]
C7. A[25]
C8. A[21]
C9. A[18]
C10. D[19]
C11. D[16]
C12. D[13]
C13. A[14]
C14. A[11]
C15. TEST3
C16. A[10]
C17. A[6]
C18. D[8]
C19. VDD
C20. D[4]
D1. VSS
D2. VDD
D3. D[29]
D4. VSS
D5. D[24]
D6. VDD
D7. D[21]
D8. VSS
D9. A[19]
D10. A[16]
D11. VDD
D12. D[12]
D13. VSS
D14. TEST2
D15. VDD
D16. VDD
D17. VSS
D18. D[5]
D19. VSS
D20. VDD
E1. A[27]
E2. VDD
E3. A[26]
E4. D[31]
E17. D[3]
E18. D[2]
E19. D[1]
E20. A[4]
F1. VSS
F2. A[28]
F3. N/C
F4. VDD
F17. VDD
F18. D[0]
F19. A[3]
F20. A[2]
G1. N/C
G2. A[29]
G3. R/W_
G4. N/C
G17. A[5]
G18. VDD
G19. A[1]
G20. A[0]
H1. DSACK1_/TA_
H2. A[31]
H3. A[30]
H4. VSS
H17. VSS
H18. N/C
H19. VSS
H20. N/C
J1. SDA
J2. SIZ[0]
J3. SIZ[1]
J4. DSACK0_
J17. DREQ_
J18. ENID
J19. QINT_
J20. TCK
K1. ENUM#
K2. N/C
K3. SCL
K4. VDD
K17. DONE_
K18. TRST_
K19. DACK_/SDACK_
K20. TMS
L1. IMSEL
L2. HS_LED
L3. TMODE[1]
L4. HS_SWITCH
L17. VDD
L18. TDI
L19. N/C
L20. VSS
M1. TMODE[0]
M2. PME#
M3. RESETI_
M4. PCI_DIS
M17. BDIP_
M18. BG_
M19. TDO
M20.BM_EN/FIFO_RDY
N1. RESETO_
N2.HS_HEALTHY_
N3. BURST_/TIP_
N4. VSS
N17. VSS
N18. TC[3]
N19. BERR_/TEA_
N20. AS_
P1. N/C
P2. TS_
P3. VSS
P4. RST#
P17. N/C
P18. TC[0]
P19. TC[1]
P20. TC[2]
R1. BB_/BGACK_
R2. BR_
R3. VH
R4. VDD
R17. VDD
R18. N/C
R19. N/C
R20. CSPCI_
T1. HALT_/TRETRY_
T2. VDD
T3. REQ#
T4. AD[31]
T17. VSS
T18. INT#
T19. CSREG_
T20. N/C
U1. VSS
U2. GNT#
U3. AD[29]
U4. VSS
U5. AD[23]
U6. VDD
U7. EXT_GNT[5]#
U8. VSS
U9. AD[17]
U10. VDD
U11. PERR#
U12. VDD
U13. VSS
U14. AD[7]
U15. VDD
U16. EXT_REQ[5]#
U17. VSS
U18. AD[1]
U19. VDD
U20. SERR#
V1. VSS
V2. AD[30]
V3. VDD
V4. N/C
V5. EXT_GNT[1]#
V6. EXT_GNT[4]#
V7. AD[22]
V8. AD[20]
V9. VSS
V10. IRDY#
V11. STOP#
V12. AD[15]
V13. AD[12]
V14. AD[8]
V15. N/C
V16. EXT_REQ[2]#
V17. EXT_REQ[6]#
V18. AD[5]
V19. AD[3]
V20. AD[0]
W1. AD[28]
W2. AD[27]
W3. AD[24]
W4. CBE[3]
W5. EXT_GNT[2]#
W6. EXT_GNT[6]#
W7. VSS
W8. AD[19]
W9. AD[16]
W10. FRAME#
W11. PCLK
W12. CBE[1]
W13. AD[13]
W14. AD[10]
W15. CBE[0]
W16. N/C
W17. EXT_REQ[3]#
W18. AD[6]
W19. VSS
W20. AD[2]
Y1. AD[26]
Y2. AD[25]
Y3. N/C
Y4. N/C
Y5. EXT_GNT[3]#
Y6. N/C
Y7. AD[21]
Y8. AD[18]
Y9. CBE[2]
Y10. TRDY#
Y11. DEVSEL#
Y12. PAR
Y13. AD[14]
Y14. AD[11]
Y15. AD[9]
Y16. IDSEL
Y17. EXT_REQ[1]#
Y18. EXT_REQ[4]#
Y19. VDD
Y20. AD[4]

2.4 Pin Descriptions

Table 4. Pin Descriptions

Pin Name	Pin Type	Description
MC68360 Signals: QUICC (see Note 1)		
A[31:0]	Tristate bidirectional	Address Bus: address for the current bus cycle. It is driven by the CA91L862A when it is the QBus master and input when QBus slave. It is qualified at the start of a transaction by AS_. As a slave, the CA91L862A samples A[31:0] on the same falling edge of the QCLK as AS_. Both A[31:0] and AS_ must meet the synchronous set-up and hold time parameters about the falling edge of the QCLK to ensure correct operation. As a master, the CA91L862A maintains the correct asynchronous timing relationships between A[31:0] and AS_. The address bus is driven valid after the rising edge of the QCLK, while the AS_ is driven only after the subsequent falling edge of the same clock period, ensuring the correct address before AS_ timing. When accesses are made to CA91L862A registers from the QBus, only the lower 12 bits of the address bus are used to determine the offset.
AS_	Rescinding Tristate bidirectional	Address Strobe: indicates the beginning (and duration) of a transaction on the QBus. As an output AS_ is driven by the CA91L862A when the CA91L862A is the QBus master, and is tristated at all other times. The Address Strobe is driven low after a falling edge of the QCLK. The Address Strobe qualifies the following signals as valid when it is asserted: A[31:0], TC[3:0], SIZ[1:0], and R/W_. CA91L862A guarantees a minimum set-up time for the qualified signals before AS_ is asserted (all qualified signals are driven from the rising edge of QCLK preceding the assertion of AS_). QSpan II rescinds AS_ prior to tristate. As an input, AS_ is sampled on the falling edge of the QCLK. AS_ must meet a minimum set-up and hold time around the falling edge of the clock for correct operation. CA91L862A recognizes a transaction as intended for it, and acknowledges it accordingly, only if one of CSREG_ or CSPCI_ is sampled low in conjunction with AS_. CA91L862A does not require that the input signals qualified by the AS_ be valid when it is asserted.
BB_/BGACK_	Rescinding Tristate bidirectional	Bus Busy: indicates ownership of the QBus. It, along with BR_ and BG_, provides the three-wire handshake for QBus arbitration. BB_/BGACK_ is intended to connect to the BGACK_ bus. As an output the CA91L862A asserts BB_/BGACK_ from the falling edge of QCLK (while master). QSpan II rescinds BB_/BGACK_ prior to tristate. As an input, the CA91L862A double-samples BB_/BGACK_ on the falling edge of QCLK: when it is master. CA91L862A can also be programmed to use a synchronous mode for QBus arbitration.
BGACK_	Rescinding Tristate bidirectional	See BB_/BGACK_
BDIP_	Input (MC68360 mode) / Bidirectional (MPC860)	Burst Data In Progress: On the MC68360 interface, this pin is used only to determine the QBus master mode of the CA91L862A. This is determined at reset by sensing the level of this pin. If BDIP_ is sampled as low (at power-up or reset) the QBus master module will operate as an MC68360 master. If the BDIP_ signal is sampled as high — at power-up or reset — the CA91L862A will operate as an MPC860 master (see Table 48 in the *QSpan II User Manual*).
BERR_/TEA_	Rescinding tristate bidirectional pin	Bus Error: used to indicate a bus error that occurs during a transaction. It can be used in conjunction with HALT_/TRETRY_ to indicate a busy-retry to the bus master. As an MC68360 master, the CA91L862A samples BERR_/TEA_ on the falling edge of QCLK during cycles in which it is a QBus master. As an MC68360 slave, BERR_/TEA_ is driven by the CA91L862A from the falling edge of QCLK. CA91L862A negates BERR_/TEA_ prior to tristate.

Table 4. Pin Descriptions (Cont.)

Pin Name	Pin Type	Description
BG_	Input	Bus Grant: indicates that the CA91L862A may become the next QBus master. BG_, along with BR_ and BB_/BGACK_, provide the three-wire handshake for QBus arbitration. BG_ is doubled-sampled on the falling edge of QCLK. CA91L862A can be programmed to use a synchronous mode for QBus arbitration.
BM_EN/ FIFO_RDY_	Bidirectional	Bus Master Enable/FIFO Ready: If this input is asserted — set as 1 — during a PCI Reset, the Bus Master Enable bit in the PCI_CS register will be set.
BR_	Output	Bus Request: used by the CA91L862A to request ownership of the QBus. BR_, along with BG_ and BB_/BGACK_, provide the three-wire handshake for QBus arbitration. BR_ is asserted and negated from the falling edge of QCLK in MC68360 mode.
CSPCI_	Input	PCI Chip Select: indicates that the current transaction on the QBus is an access to the PCI Bus. During IDMA cycles, if this is sampled high, a single address transfer is indicated; if sampled low, a dual address transfer is indicated. It is sampled on the falling edge of clock.
CSREG_	Input	Register Chip Select: indicates that the current transaction on the QBus is an access to the CA91L862A's registers.It is sampled on the falling edge of clock.
D[31:0]	Tristate bidirectional	Data Bus: provides the data information for the CA91L862A's inputs and outputs on the QBus. As an MC68360 slave the CA91L862A does not use DS_ to qualify data on writes. It also provides data on reads without decoding DS_, since DS is output only. As an MC68360 master, the CA91L862A does use DS to qualify data on writes and to request data on reads.
DACK_/ SDACK_	Input	IDMA Acknowledge: indicates to the CA91L862A that the current transaction is an IDMA transaction. The timing of DACK_ should be the same as for AS_. Using the IDMA handshakes, the CA91L862A is capable of supporting MC68360 fast termination cycles.
DONE_	Input	IDMA Done: indicates that the IDMA controller has completed the current sequence of IDMA operations, and that the CA91L862A should no longer use DREQ_ to request transactions. Setup for DONE is to falling edge of QCLK.
DREQ_	Output	IDMA Request: request to the MC68360 IDMA to either transfer data to CA91L862A IFIFO (PCI Write) or remove data from I-FIFO (PCI Read). It is asserted from the falling edge of QCLK in MC68360 mode.
DSACK0_	Rescinding tristate bidirectional	Data and Size Acknowledge 0: in conjunction with DSACK1_/TA_, is driven by the addressed slave to acknowledge the completion of a data transfer on the QBus DSACK0_ has the same timing and characteristics as DSACK1_/TA_ (see the following description).
DSACK1_/TA_	Rescinding tristate bidirectional	Data and Size Acknowledge 1: Used in conjunction with DSACK0_. This signal is driven by the addressed slave to acknowledge the completion of a data transfer on the QBus. CA91L862A terminates all normal bus cycles by asserting both DSACK1_/TA_ and DSACK0_ (indicating a 32-bit port width at all times). The DSACK1_/TA_ output is driven high (inactive) after the release of AS_ until the next falling edge of the clock, at which point it is tristated.

Table 4. Pin Descriptions (Cont.)

Pin Name	Pin Type	Description
DS_	Rescinding tristate output	Data Strobe: used to indicate valid data on the data bus during write transactions, and to request data during read transactions. DS_ is driven by the CA91L862A when it is a QBus master, and is tristated otherwise. As a slave the CA91L862A assumes write data is valid on the rising edge of QCLK following the clock edge where AS_ is sampled asserted. For read transactions, the CA91L862A provide information independent of DS_. DS_ is output only. As a master on the QBus, the CA91L862A asserts DS_ to qualify data during reads and writes. For write transactions, the DS_ is driven from the falling edge of QCLK one half a clock period after the data is driven onto the Data bus. For read transactions, DS is driven at the same time as AS_. CA91L862A negates DS_ prior to tristate.
HALT_/TRETRY_	Rescinding tristate bidirectional	Halt: Suspends external bus activity. It is used for generating retries. As an MC68360 slave CA91L862A uses HALT_/TRETRY_ as stated in Table 11 in the *QSpan II User Manual*. As an MC68360 master CA91L862A uses HALT_/TRETRY_ as stated in Table 27 in the *QSpan II User Manual*.
IMSEL	Input	Image Select: selects which QBus Slave Image to use when CSPCI_ is asserted. The timing requirements for IMSEL are the same as those of the address bus when the CA91L862A is a QBus slave.
QCLK	Input	QBus Clock: All devices intended to interface with QBus side of the CA91L862A must be synchronized to this clock. The QCLK can operate up to 33 MHz (with an MC68360 bus). During IDMA fast termination cycles the maximum MC68360 QCLK frequency is 30 MHz.
QINT_	Open drain bidirectional	QBus Interrupt: as an output, this open drain signal is asserted by the CA91L862A when an interrupt event occurs,. As an input, this signal can be mapped to the PCI INT# output.
RESETI_	Input	QBus Reset Input: resets the CA91L862A from the QBus side of the CA91L862A. RESETI_ does not reset PCI configuration and status registers.
RESETO_	Open drain output	QBus Reset Output: asserted whenever the CA91L862A's PCI RST# input is asserted, or the internal software reset bit is set.
R/W_	Tristate bidirectional	Read Write: indicates the direction of the data transfer on the Data bus. High indicates a read transaction; low indicates a write. It has the same timing as the Address bus. As a **master**, the CA91L862A drives R/W_, and tristates it otherwise. As a slave, the R/W_ pin is an input.
SIZ[1:0]	Tristate bidirectional	Size: indicates the number of bytes to be transferred during a bus cycle. The value of the Size bits, along with the lower two address bits and the port width, define the byte lanes that are active. Table 5 in the *QSpan II User Manual* shows the encoding for the Size bits.
TC[3:0]	Tristate bidirectional	Transaction Code: provides additional information about a bus cycle when the CA91L862A is a QBus master. Driven by the CA91L862A when it is a QBus master, and tristated otherwise. As a slave, the CA91L862A samples TC[3:0] on the first falling edge of the QCLK after AS_ is asserted. TC[3:0] can optionally be used with DACK_/SDACK_ to decode an IDMA operation. For use in IDMA transfers, TC[3:0] should be set to all ones. The timing for the TC[3:0] outputs is the same as the timing for the address bus when the CA91L862A is a QBus master. The values output on the TC[3:0] bus during a transaction in which the CA91L862A is the bus master is determined by the value programmed in the Transaction Code field of the corresponding CA91L862A PCI target image. TC[3:0] is intended to connect to the MC68360's FC[3:0], but may be used for other special decoding purposes.

Table 4. Pin Descriptions (Cont.)

Pin Name	Pin Type	Description
MPC860 Signals: PowerQUICC (see Note 1)		
A[31:0]	Tristate bidirectional	Address bus: address for the current bus cycle. It is driven by the CA91L862A when it is the QBus master and input as slave. It is qualified at the start of a transaction by TS_. As a slave, the CA91L862A samples A[31:0] on the rising edge of QCLK, and is qualified by Transaction Start (TS_) on the same rising clock edge. As a master, the address is driven out following a rising edge of the QCLK. When accesses are made to CA91L862A registers from the QBus, only the lower 12 bits of the address bus are used to determine the register offset.
AT[0:3]	Tristate bidirectional	See TC[3:0]
BB_/BGACK_	Rescinding tristate bidirectional	Bus Busy: indicates ownership of the QBus. BB_ is asserted low by a master to show that it owns the bus. BB_, along with BR_ and BG_, provides the three-wire handshake for QBus arbitration. As an output the CA91L862A asserts BB_/BGACK_ from the rising edge of QCLK (while master). QSpan II drives BB_/BGACK_ to the prior to tristate. Note in the MPC860 mode, the CA91L862A asserts BB_ one clock after receiving BG_: in compliance with the MPC860 arbiter. As an input, the CA91L862A samples BB_/BGACK_ on the rising edge of QCLK. CA91L862A can also be programmed to use a asynchronous mode for QBus arbitration.
BDIP_	Bidirectional	Burst Data In Progress: As MPC860 master, the CA91L862A uses BDIP_ in burst writes to indicate the second last data beat of a transaction. This allows the CA91L862A to perform burst writes of two, three, or four beats. CA91L862A does not use BDIP_ in the same manner for burst reads. Burst reads are always cacheline aligned and four beats in length. As MPC860 slave, the CA91L862A monitors BDIP_ as a signal indicating the second last data beat in the burst. This allows the CA91L862A to support bursts of two, three, or four data beats. The QBus master mode of the CA91L862A is determined at power-up and reset by sensing the level of this pin. If BDIP_ is sampled as low (at reset) the QBus master module will operate as a MC68360 master. At reset, if the BDIP_ signal is sampled as high the CA91L862A will operate as an MPC860 or M68040 master (see Table 48 in the *QSpan II User Manual*).
BERR_/TEA_	Rescinding tristate bidirectional	Transfer Error Acknowledge: indicates that a bus error occurred in the current transaction. Driven by the CA91L862A when it is a QBus slave, and tristated otherwise. As an output BERR_/TEA_ is driven by the CA91L862A from the rising edge of QCLK. CA91L862A negates BERR_/TEA_ prior to tristate. As an input, the CA91L862A samples BERR_/TEA_ on the rising edge of QCLK during cycles in which it is a QBus master.
BG_	Input	Bus Grant: indicates that the CA91L862A may become the next QBus master. BG_, along with BR_ and BB_/BGACK_, provide the three-wire handshake for QBus arbitration. BG_ is sampled on the rising edge of QCLK. CA91L862A can be programmed to use a asynchronous mode for QBus arbitration.
BR_	Output	Bus Request: used by the CA91L862A to request ownership of the QBus. BR_, along with BG_ and BB_/BGACK_, provide the three-wire handshake for QBus arbitration. BR_ is asserted and released from the rising edge of QCLK.
BM_EN/ FIFO_RDY_	Bidirectional	Bus Master Enable: If this input is asserted — set as 1 — during a PCI Reset, the Bus Master Enable bit in the PCI_CS register will be set. (FIFO_RDY) FIFO Ready functionality is not relevant to MPC860 applications.

Table 4. Pin Descriptions (Cont.)

Pin Name	Pin Type	Description
BURST_/TIP	Tristate bidirectional	Burst: indicates that the current initiated transfer is a burst cycle. This signal matches the MPC860 signal of the same name.
CSPCI_	Input	PCI Chip Select: indicates that the current transaction on the QBus is an access to the PCI Bus. CSPCI_ can be sampled on the same clock as TS or up to three clocks following TS_ assertion. During IDMA cycles, if this is sampled high, a single address transfer is indicated; otherwise, a dual address transfer is indicated.
CSREG_	Input	Register Chip Select: indicates that the current transaction on the QBus is an access to the QSpan II's registers. CSREG_ can be sampled on the same clock as TS_ or up to three clocks following TS_ assertion. This signal is sampled synchronously on the rising edge of clock after TS_.
DP[3:0]	Bidirectional	Data Parity: provides the parity information for the data on D[31:0]. It is valid on the same clock as the data.
D[31:0]	Tristate bidirectional	Data Bus: provides the general-purpose data path between the QSpan II, the MPC860, and other devices.
DACK_/SDACK_	Input	IDMA Acknowledge: indicates to the CA91L862A that the current transaction is an IDMA transaction.
DONE_	Input	IDMA Done: This signal is not used with MPC860 transfers.
DREQ_	Output	IDMA Request: request to the MPC860 IDMA to either transfer data to CA91L862A IFIFO (PCI Write) or remove data from I-FIFO (PCI Read). It is asserted from the rising edge of QCLK in MPC860 mode.
DSACK1_/TA_	Rescinding tristate bidirectional	Transaction Acknowledge: driven by the addressed slave to acknowledge the completion of a data transfer on the QBus. As a slave the CA91L862A terminates all normal bus cycles by asserting TA_. CA91L862A negates DSACK1_/TA_ prior to tristate.
HALT_/TRETRY_	Rescinding tristate bidirectional	Transfer Retry: used for generating retries. As a MPC860 slave, CA91L862A uses HALT_/TRETRY_ as stated in Table 12 in the *QSpan II User Manual*. As a MPC860 master, CA91L862A uses HALT_/TRETRY_ as stated in Table 28 in the *QSpan II User Manual*. As a slave, HALT_/TRETRY_ has the same timing as DSACK1_/TA_. CA91L862A negates HALT_/TRETRY_ prior to tristate.
IMSEL	Input	Image Select: selects which QBus Slave Image to use when CSPCI_ is asserted. The timing requirements for IMSEL are the same as those of the address bus when the CA91L862A is a QBus slave.
QCLK	Input	QBus Clock: All devices intended to interface with QBus side of the CA91L862A must be synchronized to this clock. The maximum QCLK frequency with a MPC860 is 50 MHz.
QINT_	Open drain bidirectional	QBus Interrupt: as an output, this open drain signal is asserted by the CA91L862A when an interrupt event occurs,. As an input, this signal can be mapped to the PCI INT# output.
RESETI_	Input	QBus Reset Input: resets the CA91L862A from the QBus side of the CA91L862A. Note that RESETI_ does not reset PCI configuration and status registers.
RESETO_	Open drain output	QBus Reset Output: asserted whenever the CA91L862A's PCI RST# input is asserted, or the internal software reset bit is set.
R/W_	Tristate bidirectional	Read Write: indicates the direction of the data transfer on the Data bus. High indicates a read transaction; low indicates a write. It has the same timing as the Address bus. As an active master, the CA91L862A drives R/W_, and tristates it otherwise. As an addressed slave, the R/W_ pin is an input.

Table 4. Pin Descriptions (Cont.)

Pin Name	Pin Type	Description
SIZ[1:0]	Tristate bidirectional	Size: indicates the number of bytes to be transferred during a bus cycle. The value of the Size bits, along with the lower two address bits and the port width, define the byte lanes that are active. Table 5 in the *QSpan II User Manual* shows the encoding for the Size bits. SIZ[1:0] is intended to connect to MPC860 TSIZ[0:1].
TA_	Rescinding tristate bidirectional	See DSACK1_/TA_
TC[3:0]	Tristate bidirectional	Transaction Code Bus: provides additional information about a bus cycle when the CA91L862A is a QBus master. Driven by the CA91L862A when it is a QBus master, and tristated otherwise. As a slave, the CA91L862A samples TC[3:0] on the first rising edge of the QCLK after TS_ is asserted. TC[3:0] can optionally be used with DACK_/SDACK_ to decode an IDMA operation. For use in IDMA transfers, TC[3:0] should be set to all ones. The timing for the TC[3:0] outputs is the same as the timing for the address bus when the CA91L862A is a QBus master. The values output on the TC[3:0] bus during a transaction in which the CA91L862A is the bus master is determined by the value programmed in the Transaction Code field of the corresponding CA91L862A PCI target image. TC[3:0] is intended to connect to the MPC860's AT[0:3], but can be used for other special decoding purposes.
TEA_	Rescinding tristate bidirectional	See BERR_/TEA_
TRETRY_	Rescinding tristate bidirectional	See HALT_/TRETRY_
TS_	Rescinding Tristate bidirectional	Transfer Start: TS_ is a three state bi-directional signal used to indicate the beginning of an MPC860 bus transaction on the QBus. The TS_ output is driven by the CA91L862A when the CA91L862A is the QBus master, and is tri-stated at all other times. As an output, TS_ is driven low after a rising edge of the QCLK. Transfer Start indicates the following signals will be valid on the next rising edge of the QCLK: A[31:0], TC[3:0], SIZ[1:0], and R/W_. QSpan II rescinds TS_ prior to tri-state. As an input, TS_ is sampled on the rising edge of the QCLK. CA91L862A samples the address bus and other TS_ qualified signals on the same rising edge of QCLK in which it samples TS_ asserted. CSPCI_ and CSREG_ may have up to three wait states after TS_ is sampled.
M68040 Signals (see Note 2)		
A[31:0]	Tristate bidirectional	Address bus: Address for the current bus cycle. It is driven by the CA91L862A when the CA91L862A is the M68040 master and input when the CA91L862A is the slave. It is qualified at the start of a transaction by TS_. As a slave, the CA91L862A samples A[31:0] on the rising edge of QCLK, and is qualified by Transaction Start (TS_). As a master, the address is driven out following a rising edge of the QCLK. When accesses are made to CA91L862A registers from the QBus, only the lower 12 bits of the address bus are used to determine the register offset.

Table 4. Pin Descriptions (Cont.)

Pin Name	Pin Type	Description
BB_/BGACK_	Rescinding tristate bidirectional	Bus Busy: This signal is asserted by the current bus master to indicate ownership of the M68040 bus. BB_, along with BR_ and BG_, provide the three-wire handshake for M68040 bus arbitration. As a**n** output the CA91L862A asserts BB_/BGACK_ from the rising edge of QCLK (while master). QSpan II negates BB_/BGACK_ prior to tristate. As an input, the CA91L862A samples BB_/BGACK_ on the rising edge of QCLK (while master). CA91L862A can also be programmed to use an asynchronous mode for M68040 bus arbitration.
BDIP_	Bidirectional	Burst Data In Progress: This signal is only used in the 68040 mode at reset. CA91L862A Master/Slave mode is determined at reset by sensing the level of this pin in conjunction with SIZ[1]. See Table 48 in the *QSpan II User Manual*.
BERR_/TEA_	Rescinding tristate bidirectional	Transfer Error Acknowledge: indicates an error condition exists for a bus transfer. Driven by the CA91L862A when it is a M68040 bus slave to signal an errored transaction. As an input, the CA91L862A samples BERR_/TEA_ during M68040-style cycles in which it is a M68040 bus master on the rising edge of QCLK. Target retries are indicated by the simultaneous assertion of DSACK1_/TA_ and BERR_/TEA_.
BG_	Input	Bus Grant: indicates that the CA91L862A may become the next M68040 bus master. BG_, along with BR_ and BB_/BGACK_, provide the three-wire handshake for M68040 bus arbitration. BG_ is sampled on the rising edge of QCLK. CA91L862A can be programmed to use an asynchronous mode for M68040 bus arbitration.
BM_EN/ FIFO_RDY_	Bidirectional	Bus Master Enable: If this input is asserted (set as 1) during a PCI Reset, the Bus Master Enable bit in the PCI_CS register will be set.
BR_	Output	Bus Request: asserted by the CA91L862A to request ownership of the M68040 bus. BR_, along with BG_ and BB_/BGACK_, provide the three-wire handshake for M68040 bus arbitration. BR_ is asserted and released from the rising edge of QCLK.
BURST_/TIP_	Tristate bidirectional	Transaction In Progress: asserted for the length of an M68040 transfer. This signal uses the same pin as the MPC860 BURST_ signal.
CSPCI_	Input	PCI Chip Select: indicates that the current transaction on the QBus is an access to the PCI Bus.
CSREG_	Input	Register Chip Select: indicates that the current transaction on the QBus is an access to the QSpan II's registers.
D[31:0]	Tristate bidirectional	Data Bus: provides the data information for the CA91L862A's inputs and outputs on the M68040 bus.
DSACK1_/ TA_	Rescinding tristate bidirectional	Transaction Acknowledge: asserted by the addressed slave to acknowledge a bus transfer. As a slave the CA91L862A terminates all normal bus cycles by asserting DSACK1_/TA_. QSpan II negates DSACK1_/TA_ prior to tristate. Target retries are indicated by the simultaneous assertion of DSACK1_/TA_ and BERR_/TEA_.
IMSEL	Input	Image Select: selects which QBus Slave Image to use when CSPCI_ is asserted. The timing requirements for IMSEL are the same as those of the address bus when the QSpan II is a M68040 bus slave.

Table 4. Pin Descriptions (Cont.)

Pin Name	Pin Type	Description
QCLK	Input	QBus Clock: All devices intended to interface with QBus side of the CA91L862A must be synchronized to this clock. QCLK can operate up to 40MHz.
QINT_	Open drain bidirectional	QBus Interrupt: as an output, this open drain signal is asserted by the CA91L862A when an interrupt event occurs. As an input, this signal can be mapped to the PCI INT# output.
RESETI_	Input	QBus Reset Input: resets the CA91L862A from the QBus side of the CA91L862A. RESETI_ does not reset PCI configuration and status registers.
RESETO_	Open drain output	QBus Reset Output: asserted whenever the CA91L862A's PCI RST# input is asserted, or the internal software reset bit is set.
R/W_	Tristate bidirectional	Read Write: indicates the direction of the data transfer on the Data bus. High indicates a read transaction; a low indicates a write. It has the same timing as the Address bus. As a master, the CA91L862A drives R/W_, and tristates it otherwise. As a slave, the R/W_ pin is an input.
SIZ[1:0]	Tristate bidirectional	Size: indicates the number of bytes to be transferred during a bus cycle. The value of the Size bits, along with the lower two address bits and the port width, define the byte lanes that are active. Table 6 in the *QSpan II User Manual* shows the encoding for the Size bits. SIZ[1:1] indicates a M68040 burst cycle.
TA_	Rescinding tristate bidirectional	See DSACK1_/TA_
TC[3:0]	Tristate bidirectional	Transaction Code Bus: provides additional information about a bus cycle when the CA91L862A is a M68040 bus master. Driven by the CA91L862A when it is a M68040 bus master. As a slave, the CA91L862A samples TC[3:0] on the rising edge of QCLK, and is qualified by Transfer Start (TS_). The timing for the TC[3:0] outputs is the same as the timing for the address bus when the CA91L862A is a M68040 bus master. The values output on the TC[3:0] bus during a transaction in which the CA91L862A is the bus master is determined by the value programmed in the Transaction Code field of the corresponding PCI target image. TC[3:0] may be connected to a subset of the TT[1:0] and TM[2:0] M68040 pins. Unused TC[3:0] pins, if any, should be connected to pull-up resistors.
TEA_	Rescinding tristate bidirectional	See BERR_/TEA_
TIP_	Tristate bidirectional	See BURST_/TIP_
TS_	Tristate bidirectional	Transfer Start: asserted for one clock period to indicate the start of a transfer.
PCI Bus Signals		
AD [31:0]	Bidirectional (t/s)	PCI Address/Data Bus: address and data are multiplexed over these pins providing a 32-bit address/data bus. A bus transaction consists of an address phases followed by one or more data phases.
C/BE# [3:0]	Bidirectional (t/s)	PCI Bus Command and Byte Enable Lines: command information during address phase and byte line enables during data phase.
DEVSEL#	Bidirectional (s/t/s)	PCI Device Select: driven by the CA91L862A when it is accessed as PCI slave. Sampled by the QSpan II when it is PCI master.
EXT_GNT#[6:1]	Output	External Grant: used by the QSpan II to indicate to an external device that it has been granted access to the PCI bus (this is an output).

Table 4. Pin Descriptions (Cont.)

Pin Name	Pin Type	Description
EXT_REQ#[6:1]	Bidirectional	External Request: used by an external device to indicate to the QSpan II PCI bus arbiter that it wants ownership of the PCI bus. The QSpan II drives the unused EXT_REQ#[6:1] pins high when an external arbiter is used.
FRAME#	Bidirectional (s/t/s)	Cycle Frame for PCI Bus: driven by the CA91L862A when it is PCI master, and is monitored by the CA91L862A when it is PCI target. This signal indicates the beginning and duration of an access.
GNT#	Bidirectional	PCI Grant: As an input, when the QSpan II uses an external arbiter, it indicates to the QSpan II that it has been granted ownership of the PCI bus. GNT# can be parked at QSpan II to improve its PCI master performance. As an output, when the QSpan II is the PCI bus arbiter, it indicates to an external device that it has been granted access to the PCI bus.
IDSEL	Input (in)	PCI Initialization Device Select: used as a chip select during configuration read and write transactions
INT#	Bidirectional (o/d)	PCI Interrupt: As an output, it indicates that the CA91L862A is generating an internal interrupt. As an input, this signal will cause QINT# to be asserted on the QBus bus (if enabled).The signal can be used as an input for an application where the MPC860 is the system host.
IRDY#	Bidirectional (s/t/s)	Initiator Ready: used by the CA91L862A to indicate that it is ready to complete the current data phase of the transaction. As PCI target, the CA91L862A monitors this signal during reads to determine when the PCI master is ready to accept data.
PAR	Bidirectional (t/s)	Parity: parity is even across AD [31:0] and C/BE# [3:0] (the number of 1s summed across these lines and PAR equal an even number).
PCLK	Input (in)	PCI Clock input for PCI interface used to generate fixed timing parameters. PCLK can operate up to 33MHz.
PERR#	Bidirectional (s/t/s)	Parity Error: reports parity errors during all PCI transactions except a special cycle. CA91L862A asserts PERR# within two clocks of receiving a parity error on incoming data, and holds PERR# for at least one clock for each errored data phase.
REQ#	Bidirectional (t/s)	Bus Request: used by the QSpan II to indicate that it requires the use of the PCI bus; this is an output when the QSpan II uses an external arbiter. REQ# is also used by an external device to indicate to the QSpan II PCI bus arbiter that this device wants use of the PCI bus; this signal is an input when the QSpan II PCI bus arbiter is used.
RST#	Input	PCI Reset: Asynchronous Reset that is used to bring PCI-specific registers, state machines, and signals to a consistent state.
SERR#	Bidirectional	System Error: reports address parity errors during all transactions. CA91L862A asserts SERR# within two clocks of receiving a parity error on incoming address, and holds SERR# for at least one clock for each errored data phase.
STOP#	Bidirectional	Stop: used by the CA91L862A as PCI target when it wishes to signal the PCI master to stop the current transaction. As PCI master, the CA91L862A terminates the transaction if it receives STOP# from the PCI target.
TRDY#	Bidirectional (s/t/s)	Target Ready: used by the CA91L862A as PCI target to indicate that it is ready to complete the current data phase. During a read with CA91L862A as PCI master, the target asserts TRDY# to indicate to the CA91L862A that valid data is present on the data bus.
Hot Swap Signals		
ENUM#	Open Drain Output	Hot Swap Event Interrupt: notifies the PCI host that either a board has been inserted or is about to be extracted.
HS_HEALTHY_	Input	Hot Swap Healthy: CA91L862A internally OR's this input with PCI reset (RST#) to determine when back-end power is stable.

Table 4. Pin Descriptions (Cont.)

Pin Name	Pin Type	Description
HS_LED	Output	Hot Swap LED Control: This signal is driven by QSpan II to control the status of the LED. The signal is driven low to turn on the LED during the hardware and software connection stages. The signal is tri-stated during normal operation to turn off the LED.
HS_SWITCH	Input	Hot Swap Switch: CA91L862A uses this input to monitor the state of the Hot Swap board ejector latch. A low value on this signal indicates that the ejector latch is open.
Miscellaneous Signals		
ENID	Input	ENID: EEPROM Loading Reset Option. If ENID is sampled high after a PCI reset, then the CA91L862A will download register information from the EEPROM.
PCI_ARB_EN	Input	PCI Arbiter Enable: If PCI_ARB_EN is sampled high at the negation of Reset, the CA91L862A's PCI bus arbiter is enabled and will function as the PCI bus arbiter.
PCI_DIS	Input	PCI Configuration Disable: This is a power-up option which makes the CA91L862A hold off on ENUM# assertion and retry PCI configuration cycles to allow the Host processor to perform local configuration. CA91L862A accepts PCI configuration cycles after the PCI_DIS bit is cleared in the MISC_CTL2 register.
PME#	Open Drain Output	Power Management Event Interrupt: This signal is asserted to request a change in its current power management state and/or to indicate that a power management event has occurred.
SCL	Output	Serial Clock: EEPROM Serial clock. The frequency of the SCL is the PCLK frequency divided by 2^{10}.
SDA	Bidirectional	Serial Data: EEPROM Serial data line. If SDA is sampled high after a PCI reset, then the CA91L862A will download register information from the EEPROM.
TEST1	Input	This is a manufacturing test input which should be left open. This pin has an internal pull-up resistor.
TEST2	Input	This is a manufacturing test input which should be left open. This pin has an internal pull-down resistor.
TEST3	Input	This is a manufacturing test input which should be left open. This pin has an internal pull-down resistor.
TMODE[1:0]	Input	Test Mode: Selects the CA91L862A test mode. These pins have internal pull-down resistors.
VH	Power	Highest I/O Voltage: VH is a power pin which must be connected to the highest voltage level that the CA91L862A I/Os will observe on either the QBus or the PCI bus.
JTAG Signals		
TMS	Input	Test Mode Select: Used to control the state of the Test Access Port controller
TDI	Input	Test Input: Used (in conjunction with TCK) to shift data and instructions into the Test Access Port (TAP) in a serial bit stream.
TDO	Output	Test Output: Used (in conjunction with TCK) to shift data and instructions into the Test Access Port (TAP) in a serial bit stream.
TRST_	Input	Test Reset: Used to force the Test Access Port (TAP) into a initialized state.
TCK	Input	Test Clock: Used to clock state information and data into and out of the device during boundary scan.

Notes:

1. The following table applies to MC68360 and MPC860 SIZ[1:0] signals.

Table 5. MC68360/MPC860 Encoding for the SIZ[1:0] Signal

SIZ[1]	SIZ[0]	CA91L862A Master	CA91L862A MC68360 slave	CA91L862A MPC860 slave
0	0	4 bytes	4 bytes	4 bytes
0	1	1 byte	1 byte	1 byte
1	0	2 bytes	2 bytes	2 bytes
1	1	Reserved	3 bytes	3 bytes

2. The following table describes the signal encoding for M68040 SIZ[1:0] signals. Byte lane enabling is combined with A[1:0] as described in the *NXP M68040 User's Manual*.

Table 6. M68040 Encoding for the SIZ[1:0] Signal

SIZ[1]	SIZ[0]	CA91L862A as M68040 Master	CA91L862A as M68040 Slave
0	0	4 bytes	4 bytes
0	1	1 byte	1 byte
1	0	2 bytes	2 bytes
1	1	Reserved	Line (burst)

3. Signals and DC Characteristics

3.1 Terminology

The following abbreviations are used in this chapter:

2S	Two-state output
3S	Tristate output
B	Bidirectional
I	Input
O	Output
OD	Open Drain
PD	Internal pull-down
PU	Internal pull-up
TTL	Input with TTL threshold
TTL PU	Input with TTL threshold (the pull-up resistor is internal)
TTL Sch.	TTL Schmitt trigger input

3.2 Packaging and Voltage Level Support

QSpan II is available in two packages:

- 17 mm x 17 mm, 1.0 mm ball pitch, 256 PBGA
- 27 mm x 27 mm, 1.27 mm ball pitch, 256 PBGA

Both packages require a 3.3V power supply and provide 3.3V or 5V I/O signaling characteristics on the PCI bus. Both devices are also 5V tolerant. For more information on QSpan II packaging, see Package Outline Drawings.

3.3 Signals and DC Characteristics

Table 7. Non-PCI DC Electrical Characteristics (V_{DD} ±5%)

Symbols[1]	Parameters	Test conditions	Min	Max
V_{IH}	Voltage Input high	TTL, TTL Sch	2.0V	-
V_{IH}	Voltage Input high	CMOS	0.7 V_{DD}	-
V_{IL}	Voltage Input low	TTL, TTL Sch	-	0.8V
V_{IL}	Voltage Input low	CMOS	-	0.3V_{DD}
V_{HY}	Hysteresis for Schmitt	TTL Sch	0.3V	-
V_{OL}	Voltage Output low	I_{OL} = 8.0 mA V_{DD} = 3.0 V	-	0.4V
V_{OH}	Voltage Output high	I_{OH} = -8.0 ma V_{DD} = 3.0 V	2.4V	-
I_{IL}	Input Leakage Current low	With no pull-up or pull-down resistance (V_{IN} = V_{SS} or V_{DD})	-10.0µA	10.0µA
I_{IL_PU}	Input Leakage Current Low with Pull-up	-	-100.0µA	-4µA
I_{IH_PD}	Input Leakage Current High with Pull-down	-	4µA	100µA

Table 7. Non-PCI DC Electrical Characteristics (V_{DD} ±5%)

Symbols[1]	Parameters	Test conditions	Min	Max
I_{OZ}	Tristate Output Leakage	$V_{OUT} = V_{DD}$ or V_{SS}	-10.0µA	10.0µA
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{SS}$ or V_{DD}	-	80µA[2]
C_{IN}	Input Capacitance	-	-	10pF

1. For more information on PCI signal characteristics, see the *PCI Local Bus Specification (Revision 2.2)*.
2. Depends on customer design.

Table 8. 3.3V PCI I/O Signaling AC/DC Characteristics (V_{DD} ±5%)

Symbols	Parameters	Test Conditions	Min	Max	Units
V_{IL}	Input low voltage	-	-0.5	$0.3*V_{DD}$	V
V_{IH}	Input high voltage	-	$0.5*V_{DD}$	$V_{DD}+0.5$	V
I_{IH}	Input high current	$0<V_{IN}<V_{DD}$	-10	+10	µA
I_{IL}	Input low current	$0<V_{IN}<V_{DD}$	-10	+10	µA
V_{OL}	Output low voltage	I_{OL}=1500 µA	-	$0.1*V_{DD}$	V
V_{OH}	Output high voltage	I_{OH}=-500 µA	$0.9*V_{DD}$	-	V
I_{OZ}	Output leakage current tristate condition	$V_{OH}=V_{SS}$ or V_{DD}	-10	10	µA
I_{OH} (AC)	Switching current high	$0<V_{OUT}\leq 0.3V_{DD}$	$-12*V_{DD}$	-	mA
		$0.3V_{DD}<V_{OUT}<0.9V_{DD}$	$-17.1 (V_{DD}-V_{OUT})$	-	mA
		$0.7V_{DD}<V_{OUT}<V_{DD}$	-	Eqn A[1]	mA
	(Test Point)	$V_{OUT}=0.7V_{DD}$	-	$-32V_{DD}$	mA
I_{OL} (AC)	Switching current low	$V_{DD}>V_{OUT}>0.6V_{DD}$	$16V_{DD}$	-	mA
		$0.6V_{DD}>V_{OUT}>0.1V_{DD}$	$26.7V_{OUT}$	-	mA
		$0.18V_{DD}>V_{OUT}>0$	-	Eqn B[2]	mA
	(Test Point)	$V_{OUT}=0.18V_{DD}$	-	$38V_{DD}$	mA
I_{CL}	Low clamp current	$-3<V_{IN}\leq -1$	$-25+(V_{IN}-V_{DD}-1)/0.015$	-	mA
I_{CH}	High clamp current	$V_{DD}+4>V_{IN}>V_{DD}+1$	$25+(Vin-V_{DD}-1)/0.015$	-	mA
slewr	Output rise slew rate	$0.2V_{DD}$-$0.6V_{DD}$ load	1	4	V/ns
slewf	Output fall slew rate	$0.6V_{DD}$-$0.2V_{DD}$ load	1	4	V/ns

1. Equation A: $I_{OH}=(98.0/V_{DD})*(V_{OUT}-V_{DD})*(V_{OUT}+0.4V_{DD})$ for $V_{DD} > V_{OUT} > 0.7V_{DD}$
2. Equation B: $I_{OL}=(256/V_{DD}) * V_{OUT} * (V_{DD} - V_{OUT})$ for $0v < V_{OUT} < 0.18V_{DD}$

Table 9. 5V PCI I/O Signaling AC/DC Electrical Characteristics

Symbols	Parameters	Test Conditions	Min	Max	Units
V_{IL}	Input low voltage	-	-0.5	0.8	V
V_{IH}	Input high voltage	-	2.0	5.3[1]	V
I_{IH}	Input high current	V_{IN}=2.7	-	+70	µA
I_{IL}	Input low current	V_{IN}=0.5	-	-70	µA
V_{OL}	Output low voltage	I_{OL}=3 mA, 6 mA	-	0.55	V
V_{OH}	Output high voltage	I_{OH}=-2 mA	2.4	-	V
I_{OZ}	Output leakage current tristate condition	V_{OH}=V_{SS} or V_{DD}	-70	70	µA
I_{OH} (AC)	Switching current high	$0<V_{OUT}\leq1.4$	-44	-	mA
		$1.4<V_{OUT}<2.4$	-44 + (V_{OUT} - 1.4)/0.024	-	mA
		$3.1<V_{OUT}<V_{DD}$	-	Eqn C[2]	mA
	(Test Point)	V_{OUT}=3.1	-	-142	mA
I_{OL} (AC)	Switching current low	$V_{OUT}\geq2.2$	95	-	mA
		$2.2>V_{OUT}>0.55$	V_{OUT}/0.023	-	mA
		$0.71>V_{OUT}>0$	-	Eqn D[3]	mA
	(Test Point)	V_{OUT}=0.71	-	206	mA
I_{CL}	Low clamp current	$-5<V_{IN}\leq-1$	-25 + (V_{IN}+1)/0.015	-	mA
slewr	Output rise slew rate	0.4 to 2.4 load	1	5	V/ns
slewf	Output fall slew rate	2.4 to 0.4 load	1	5	V/ns

1. All signals are 5V tolerant.
2. Equation C: $I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$ for $V_{DD} > V_{OUT} > 3.1V$
3. Equation D: $I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$ for $0V < V_{OUT} < 0.71V$

Table 10. Pin List for QSpan II Signals

Pin Name	17 mm PBGA Ball #	27 mm PBGA Ball #	Type	Input Type	Output Type	Reset State	IOL (mA)	IOH (mA)	Interface	Signal Description
A[31:0]	See Table 12	See Table 12	B	TTL	3S	Hi-Z	8	-8	QBus	Address Lines
AD[31:0]	See Table 11	See Table 11	B	PCI	3S	Hi-Z	-	-	PCI	Address/data Lines
AS_	L16	N20	B	TTL Sch.	3S	Hi-Z	8	-8	QBus	Address Strobe
BB_/BGACK_	L2	R1	B	TTL Sch.	3S	Hi-Z	8	-8	QBus	Bus Busy/bus Grant Acknowledge
BDIP_	K14	M17	B	TTL	3S	Hi-Z	8	-8	QBus	Burst Data In Progress (And QSpan II Master Mode)
BERR_/TEA_	L15	N19	B	TTL Sch.	3S	Hi-Z	8	-8	QBus	Bus Error/ Transfer Error Acknowledge

Table 10. Pin List for QSpan II Signals (Cont.)

Pin Name	17 mm PBGA Ball #	27 mm PBGA Ball #	Type	Input Type	Output Type	Reset State	IOL (mA)	IOH (mA)	Interface	Signal Description
BG_	K16	M18	I	TTL	-	-	-	-	QBus	Bus Grant
BGACK_	See BB_/BGACK_									
BM_EN/ FIFO_RDY_	J14	M20	B	TTL (PD)	2S	Hi-Z	8	-8	QBus	Bus Master Enable
BR_	L1	R2	O	TTL	2S	Hi-Z	8	-8	QBus	Bus Request
BURST_/TIP_	L4	N3	B	TTL	3S	Hi-Z	8	-8	QBus	Burst/transaction In Progress
C/BE[0]	R11	W15	B	PCI	3S	Hi-Z	-	-	PCI	Command And Byte Enables
C/BE[1]	R9	W12								
C/BE[2]	N7	Y9								
C/BE[3]	T2	W4								
CSPCI_	P16	R20	I	TTL	-	-	-	-	QBus	PCI Chip Select
CSREG_	M13	T19	I	TTL	-	-	-	-	QBus	QSpan Register Chip Select
D[31:0]	See Table 13	See Table 13	B	TTL	3S	Hi-Z	8	-8	QBus	Data Lines
DP[0]	A5	C6	B	TTL	3S	Hi-Z	8	-8	QBus	Data Parity Line
DP[1]	C5	B5								
DP[2]	B5	A4								
DP[3]	D4	C5								
DACK_/ SDACK_	J13	K19	I	TTL Sch.	-	-	-	-	QBus	IDMA Acknowledge
DEVSEL#	R8	Y11	B	PCI	3S	Hi-Z	8	-8	PCI	Device Select
DONE_	J15	K17	I	TTL	-	-	-	-	QBus	IDMA Done
DREQ_	G13	J17	O	TTL	3S	Hi-Z	8	-8	QBus	IDMA Request
DS_	C10	A13	O	TTL	3S	Hi-Z	8	-8	QBus	Data Strobe
DSACK0_	G3	J4	B	TTL Sch.	3S	Hi-Z	8	-8	QBus	Data And Size Acknowledge 0
DSACK1_/ TA_	F1	H1	B	TTL Sch.	3S	Hi-Z	8	-8	QBus	Data And Size Acknowledge 1/ Transfer Acknowledge
ENID	H15	J18	I	TTL PD	-	-	-	-	-	EEPROM Loading Reset Options
ENUM#	G4	K1	O	-	OD	Hi-Z	8	-8	-	CompactPCI Hot Swap event output
EXT_GNT# [6:1]	See Table 14	See Table 14	O	PCI	3S	Hi-Z	-	-	PCI	External Grant
EXT_REQ# [6:1]	See Table 14	See Table 14	B	PCI	3S	Hi-Z	-	-	PCI	External Request
FRAME#	P7	W10	B	PCI	3S	Hi-Z	-	-	PCI	Cycle Frame

Table 10. Pin List for QSpan II Signals (Cont.)

Pin Name	17 mm PBGA Ball #	27 mm PBGA Ball #	Type	Input Type	Output Type	Reset State	IOL (mA)	IOH (mA)	Interface	Signal Description
GNT#	M3	U2	B	PCI	3S	Hi-Z	-	-	PCI	Grant (External Grant 7)
HALT_/ TRETRY_	M1	T1	B	TTL Sch.	3S	Hi-Z	8	-8	QBus	Halt/Transfer Retry
HS_ HEALTHY_	K4	N2	I	TTL (PD)	-	-	-	-	-	Hot Swap Healthy Signal
HS_LED	H2	L2	O	-	OD	Low	8	-8	-	LED control output for Hot Swap
HS_SWITCH	J2	L4	I	TTL (PD)	-	-	-	-	-	Switch input for Hot Swap
IDSEL	N12	Y16	I	PCI	-	-	-	-	PCI	Initialization Device Select
IMSEL	H4	L1	I	TTL	-	-	-	-	QBus	Slave Image Select
INT#	M14	T18	B	PCI	OD	Hi-Z	8	-8	PCI	Interrupt
IRDY#	R7	V10	B	PCI	3S	Hi-Z	-	-	PCI	Initiator Ready
PAR	N10	Y12	B	PCI	3S	Hi-Z	-	-	PCI	Parity
PCI_ARB_EN	C4	B4	I	TTL (PD)	-	-	-	-	PCI	Power up option to enable PCI Bus Arbiter
PCI_DIS	K3	M4	I	TTL (PD)	-	-	-	-	PCI	Power up option to disable PCI config accesses to Universe II II
PCLK	P8	W11	I	PCI	-	-	-	-	PCI	PCI Clock
PERR#	N9	U11	B	PCI	3S	Hi-Z	-	-	PCI	Parity Error
PME#	J1	M2	O	-	OD	Hi-Z	8	-8	-	Power management event
QCLK	D8	A10	I	TTL	-	-	-	-	QBus	QBus clock
QINT_	H16	J19	B	TTL	OD	Hi-Z	8	-8	QBus	Interrupt
REQ#	M4	T3	B	PCI	3S	Hi-Z	-	-	PCI	Request (External Request 7)
RESETI_	J4	M3	I	TTL Sch.	-	-	-	-	QBus	Reset Input
RESETO_	K1	N1	O	TTL	OD	Hi-Z	8	-8	QBus	Reset Output
RETRY_	See HALT_/TRETRY_									
RST#	M2	P4	I	PCI	-	-	-	-	PCI	Reset
R/W_	D1	G3	B	TTL	3S	Hi-Z	8	-8	QBus	Read/Write
SCL	H3	K3	O	TTL	3S	Hi-Z	8	-8	EEPROM	Serial Clock
SDA	G1	J1	B	TTL	OD	Hi-Z	8	-8	EEPROM	Serial Data
SDACK_	See DSACK_/SDACK_									

Table 10. Pin List for QSpan II Signals (Cont.)

Pin Name	17 mm PBGA Ball #	27 mm PBGA Ball #	Type	Input Type	Output Type	Reset State	IOL (mA)	IOH (mA)	Interface	Signal Description
SERR#	M15	U20	B	TTL	OD	Hi-Z	8	-8	PCI	System Error
SIZ[0]	G2	J2	B	TTL	3S	Hi-Z	8	-8	QBus	Size
SIZ[1]	F4	J3								
STOP#	T7	V11	B	PCI	3S	Hi-Z	-	-	PCI	Stop
TA_	See DSACK1_/TA_									
TC[0]	N16	P18	B	TTL	3S	Hi-Z	8	-8	QBus	Transaction Code
TC[1]	L14	P19								
TC[2]	M16	P20								
TC[3]	L13	N18								
TCK	H13	J20	I	TTL	-	Hi-Z	-	-	JTAG	JTAG Test Clock Input
TDI	K15	L18	I	TTL (PU)	-	Hi-Z	-	-	JTAG	JTAG Test Data Input
TDO	K13	M19	O	TTL	3S	Hi-Z	8	-8	JTAG	JTAG Test Data Output
TEA_	See BERR_/TEA_									
TEST1	B12	B15	I	CMOS (PU)	-	-	-	-	-	Manufacturing Test Pin
TEST2	A14	D14	I	TTL (PD)	-	-	-	-	-	Manufacturing Test Pin
TEST3	C12	C15	I	TTL (PD)	-	-	-	-	-	Manufacturing Test Pin
TIP_	See BURST_/TIP_									
TMODE[0]	J3	M1	I	TTL (PD)	-	-	-	-	-	Test Mode Pins
TMODE[1]	H1	L3								
TMS	J16	K20	I	TTL (PU)	-	-	-	-	JTAG	JTAG Mode Select
TRDY#	N8	Y10	B	PCI	3S	Hi-Z	-	-	PCI	Target Ready
TRST_	H14	K18	I	TTL (PU)	-	-	-	-	JTAG	JTAG Test Reset
TS_	K2	P2	B	TTL Sch.	3S	Hi-Z	8	-8	QBus	Transfer Start

Table 11. PCI Bus Address/Data Pins

Signal	17 mm PBGA	27 mm PBGA		Signal	17 mm PBGA	27 mm PBGA
AD0	N15	V20		AD16	P6	W9
AD1	N14	U18		AD17	T6	U9
AD2	T16	W20		AD18	T5	Y8
AD3	P15	V19		AD19	R6	W8
AD4	T14	Y20		AD20	N6	V8
AD5	T13	V18		AD21	P5	Y7
AD6	P14	W18		AD22	N5	V7
AD7	P12	U14		AD23	T1	U5
AD8	T10	V14		AD24	R2	W3
AD9	P11	Y15		AD25	R3	Y2
AD10	N11	W14		AD26	P3	Y1
AD11	P10	Y14		AD27	N3	W2
AD12	R10	V13		AD28	N4	W1
AD13	T9	W13		AD29	P2	U3
AD14	T8	Y13		AD30	P1	V2
AD15	P9	V12		AD31	N2	T4

Table 12. QBus Address Pins

Signal	17 mm PBGA	27 mm PBGA		Signal	17 mm PBGA	27 mm PBGA
A0	G14	G20		A16	A9	D10
A1	G16	G19		A17	D7	A9
A2	G15	F20		A18	B8	C9
A3	F14	F19		A19	C7	D9
A4	F16	E20		A20	A8	B8
A5	E16	G17		A21	A7	C8
A6	C13	C17		A22	B7	A7
A7	B16	B17		A23	D6	B7
A8	C14	A18		A24	C6	A6
A9	A15	B16		A25	A6	C7
A10	D12	C16		A26	C1	E3
A11	C11	C14		A27	E3	E1
A12	D11	B14		A28	E4	F2
A13	A13	A14		A29	E1	G2
A14	A12	C13		A30	F3	H3
A15	B11	B13		A31	F2	H2

Table 13. QBus Data Pins

Signal	17 mm PBGA	27 mm PBGA		Signal	17 mm PBGA	27 mm PBGA
D0	F15	F18		D16	C9	C11
D1	E15	E19		D17	A10	A11
D2	E14	E18		D18	B9	B10
D3	D16	E17		D19	C8	C10
D4	D15	C20		D20	B6	B6
D5	F13	D18		D21	D5	D7
D6	E13	B20		D22	A4	A3
D7	D14	B19		D23	A3	C4
D8	C16	C18		D24	B4	D5
D9	C15	A20		D25	A2	B3
D10	B14	B18		D26	B3	A2
D11	B15	A19		D27	C3	C2
D12	D10	D12		D28	B1	B1
D13	A11	C12		D29	D3	D3
D14	D9	B12		D30	D2	C1
D15	B10	B11		D31	C2	E4

Table 14. External Request and Grant Pins

Signal	17 mm PBGA	27 mm PBGA		Signal	17 mm PBGA	27 mm PBGA
EXT_REQ[1]#	T11	Y17		EXT_GNT[1]#	R1	V5
EXT_REQ[2]#	R12	V16		EXT_GNT[2]#	R4	W5
EXT_REQ[3]#	N13	W17		EXT_GNT[3]#	T3	Y5
EXT_REQ[4]#	P13	Y18		EXT_GNT[4]#	P4	V6
EXT_REQ[5]#	T12	U16		EXT_GNT[5]#	R5	U7
EXT_REQ[6]#	R13	V17		EXT_GNT[6]#	T4	W6

Table 15. Pin Assignments for Power (V_{DD})

17 mm PBGA				27 mm PBGA		
A16[a]	F12	M5		D2	D15	T2
B2[a]	G5	M6		V3	F4	D20
E5	G12	M7		U12	F17	B2
E6	H5	M8		Y19	K4	R3 [1]
E7	H12	M9		U19	L17	-
E8	J5	M10		G18	R4	-
E9	J12	M11		C19	R17	-
E10	K5	M12		D16	U6	-
E11	K12	N1 [1]		A5	U10	-
E12	L5	R15 [1]		D6	U15	-
F5	L12	-		D11	E2	-

1. These power pins are called VH. These pins must be connected to the highest voltage level that the QSpan II I/Os will observe on either the QBus or the PCI bus (see Table 16).

Table 16. Voltage Required to be Applied to VH

PCI Bus Voltage (V)	QBus Voltage (V)	VH Voltage (V)
3.3	3.3	3.3
5	5	5
3.3	5	5
5	3.3	5
VIO [1]	3.3	VIO [1]
VIO [1]	5	5

1. VIO denotes the signal connection to the PCI bus connector for Universal Signaling.

Table 17. Pin Assignments for Ground (V_{SS})

17 mm PBGA				27 mm PBGA		
F6	H6	K6		F1	A12	U8
F7	H7	K7		U1	A8	U13
F8	H8	K8		V1	A1	U17
F9	H9	K9		V9	D4	-
F10	H10	K10		H19	D8	-
F11	H11	K11		D19	D13	-
G6	J6	L6		D1	D17	-
G7	J7	L7		P3	H4	-
G8	J8	L8		W7	H17	-
G9	J9	L9		W19	N4	-
G10	J10	L10		T17	N17	-
G11	J11	L11		L20	U4	-

Table 18. No-connect Pin Assignments [1]

17 mm PBGA		27 mm PBGA		
A1		A15	H18	T20
B13		A16	H20	V4
D13		A17	K2	V15
E2		B9	L19	W16
L3		C3	P1	Y3
R14		F3	P17	Y4
R16		G1	R18	Y6
T15		G4	R19	-

1. Route all N/C signals out to vias on your board to allow for future migration to new QSpan II variants.

4. Specifications

4.1 Absolute Maximum Ratings

Table 19. 3.3 Volt Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}	DC Supply Voltage	-0.5 to 7.0	V
V_{IN}	DC Input Voltage	-0.3 to 5.3[1] [2]	V
I_{IN}	DC Input Current	±10	mA
T_{STG}	Storage Temperature	-40 to +125	°C

1. Power available on V_{IO} without power to V_{DD} (V_{IN}) can result in reliability impact.
2. QSpan II is 5V tolerant on all pins.

4.2 Recommended Operating Conditions

Table 20. 3.3 Volt Recommended Operating Conditions

Symbol	Parameter	Rating	Units
V_{DD}	DC Supply Voltage	3.0 to 3.6	V
T_C	Commercial Temperature	0 to 70	°C
T_I	Industrial Temperature	-40 to 85	°C

4.3 Thermal Specifications

The maximum ambient temperature of the QSpan II can be calculated as follows:

$Ta \leq Tj - \theta_{ja} * P$

Where,

T_a = Ambient temperature (°C)

T_j = Maximum QSpan II Junction temperature (°C) = 125°C

θ_{ja} = Junction to Ambient Thermal Impedance (°C / Watt) see Table 21.

P = QSpan II power consumption (Watts), see Table 22.

The junction to ambient thermal impedance (θ_{ja}) is dependent on the air flow in meters per second over the QSpan II (see Table 21).

Table 21. Junction to Ambient Characteristics

Wind Speed (m/s)	Package		Unit
	27 mm	17 mm	
0	35.0	29.7	θ_{ja} °C/W
1	32.4	25.8	θ_{ja} °C/W
2	29.9	24.2	θ_{ja} °C/W

4.4 Power Dissipation

Table 22. Power Dissipation

QCLK[1]	Minimum	Typical	Maximum
25 MHz	0.28W	0.50W	0.63W
40 MHz	0.33W	0.58W	0.75W
50 MHz	0.38W	0.63W	0.90W

1. PCI clock always runs at 33 MHz.

5. Package Outline Drawings

This appendix discusses mechanical (packaging) information for the QSpan II. The following mechanical information is discussed:

- QSpan II PBGA: 256-ball configuration, 17 mm package
- QSpan II PBGA: 256-ball configuration, 27 mm package

5.1 256 PBGA — 17 mm

Table 23. 256 PBGA — 17 mm Packaging Features

Feature	Description
Package Type	2 layer, 256 terminal Plastic Ball Grid Array (PBGA)
Package Body Size	17 X 17 mm
JEDEC Specification	MO-151 Variation AAF-1

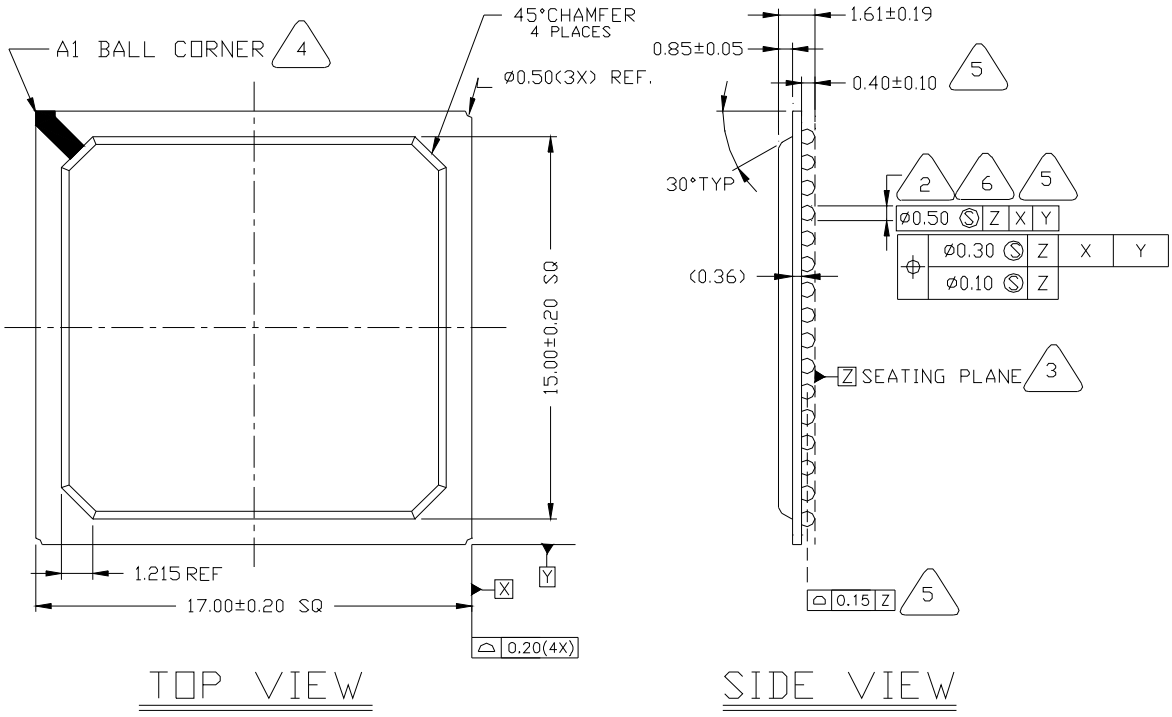


Figure 2. 256 PBGA, 17 mm — Top and Side Views

PBGA Notes — 17 mm

1. All dimensions conform to ANSI Y14.5-1994. Dim in millimeters (mm).
2. Measured at the maximum solder ball diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls.
4. A1 Corner is identified by chamfer, ink mark, metalized mark, indentation or other feature of the package body or lid.
5. Reference Specification: QSpan II conforms to Jedec Registered Outline drawing MO-151 Variation AAF-1, except for these dimensions.
6. Ball pad is 0.4 mm diameter. Renesas recommends customer's PCB pad have same diameter.

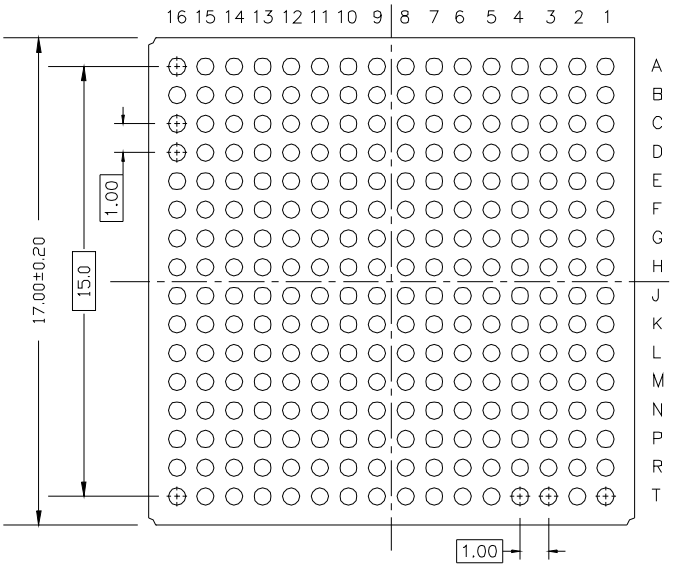


Figure 3. 256 PBGA, 17 mm — Bottom View

5.2 256 PBGA — 27 mm

Table 24. 256 PBGA — 27 mm Packaging Features

Feature	Description
Package Type	256 terminal Plastic Ball Grid Array (PBGA), (1) power and (1) ground plane
Package Body Size	27 X 27 mm
JEDEC Specification	MO-151 Variation BAL-2

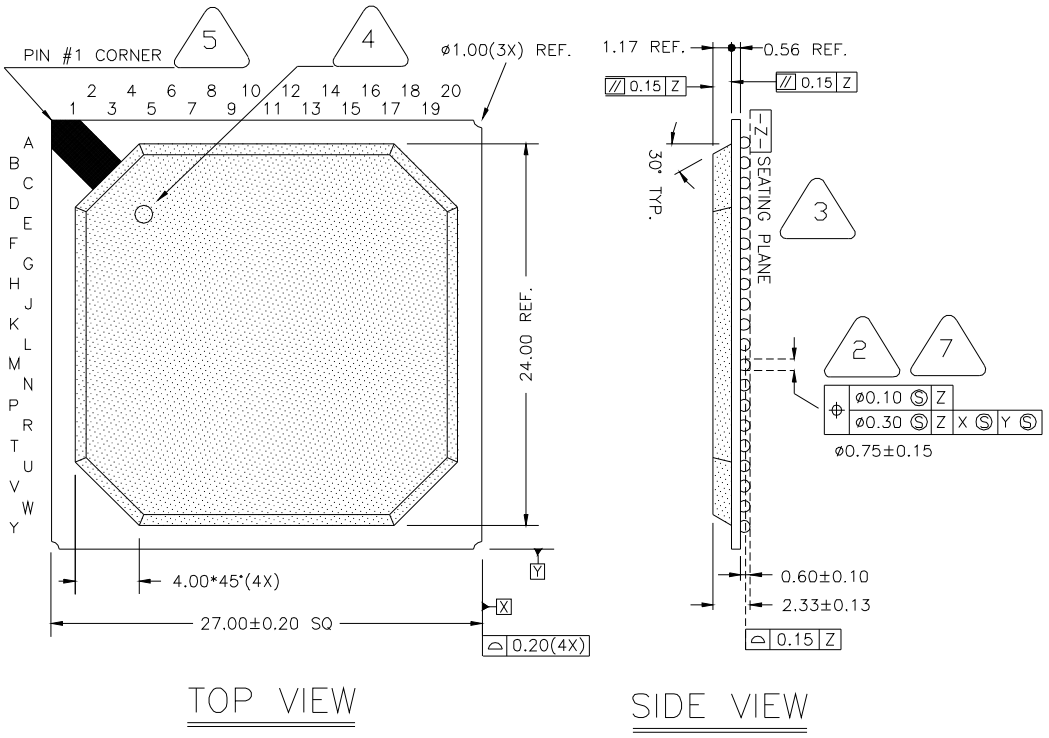


Figure 4. 256 PBGA, 27 mm — Top and Side Views

PBGA Notes — 27 mm

1. All dimensions conform to ANSI Y14.5-1994. Dim in millimeters (mm).
2. Measured at the maximum solder ball diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls.
4. A1 Ball Corner ID. Marked in ink for plate mold. Indent if Automold.
5. A1 Corner is identified by chamfer, ink mark, metallized mark, indentation or other feature of the package body or lid.
6. Reference Specification: QSpan II conforms to Jedec Registered Outline drawing MO-151.
7. Ball pad is 0.60 mm diameter. Renesas recommends customer's PCB pad has same diameter.

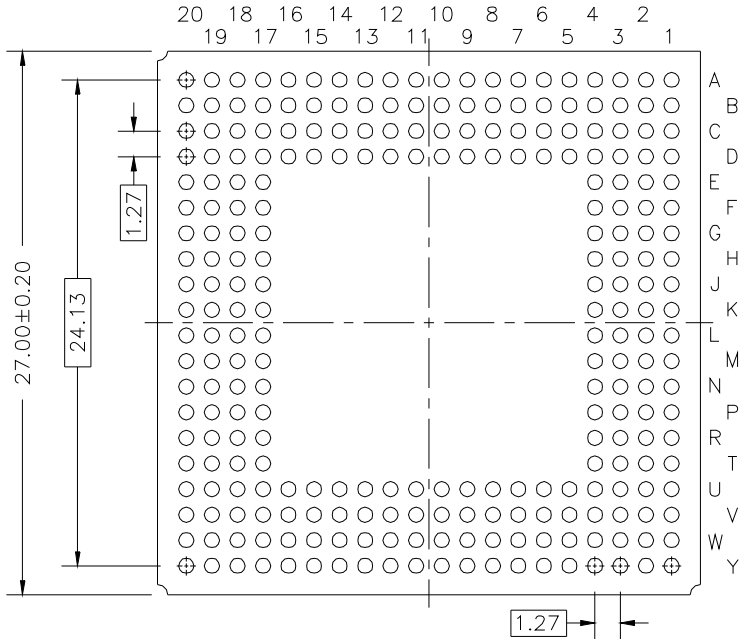


Figure 5. 256 PBGA, 27 mm — Bottom View

6. Ordering Information

Part Number	Frequency [1]	Voltage [2]	Temperature	Package
CA91L862A-50IE	33MHz MC68360 50MHz MPC860	3.3V	-40° to 85°C	27 mm PBGA
CA91L862A-50IEV	33MHz MC68360 50MHz MPC860	3.3V	-40° to 85°C	27 mm PBGA

1. The CA91L862A is compatible with all M68040 variants in large buffer mode up to 40 MHz. The QSpan is compatible with all M68040 variants in small buffer mode up to 33 MHz.
2. The CA91L862A supports universal PCI (3.3/5V tolerant inputs and 3.3/5V compliant output signaling).

7. Revision History

Revision	Date	Description
1.01	Jul 24, 2024	Removed obsolete part numbers from the Ordering Information section.
1.00	Jul 10, 2024	Initial release. ▪ The information in this document used to reside exclusively in the *QSpan II User Manual*. ▪ No technical changes were made in the creation of the datasheet.

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