1 V3.5 (07-Jan-2022

Rebranded datasheet from Dialog to Renesas

2 V3.4 (09-Nov-2016)

- Bluetooth Smart changed to Bluetooth low energy as per Bluetooth SIG directive.
- Section 4.3.1 (OTP Header), p.11 and p.12:
  - 0x7FDC to 0x7FF0: Changed to Customer Specific Field (6 32-bit words).
  - 0x7FD4 to 0x7FDB: Bluetooth Device Address corrected from 8 32-bit words to 2 32-bit words.
- Section 13.6.2 (I2C - Master Mode Operation), p.43:
  - Changed section number from 13.7 to 13.6.2.
  - Added missing sub-section ‘Master Transmit and Master Receive’.
  - Changed sub-section ‘Disabling the I2C Controller’ to section 13.6.3.
- Figure 56 (Block Diagram of the Analog Power Block and Internal Interconnections), p.69:
  - Minimum battery voltage for Lithium coin cell corrected from 2.2 V to 2.35 V.
- Language and title capitalization changed to US English.
- Back page:
  - Definition for datasheet status Final clarified.
  - Disclaimer updated with trademarks statement.
  - RoHS statement updated.

3 V3.3 (08-Jun-2016)

- DA14580 qualified to Bluetooth Specification 4.2. Datasheet title and document content changed accordingly.
- Section 17 (Wake-up timer), p.55: Added minimum pulse width of 2 sleep clock cycles for wake-up via GPIO.
- Table 196 (SPI_CTRL_REG), p.174: Definition of SPI_MINT corrected:
  - ICU changed to Interrupt Controller.
  - Note on shared interrupts (SPI_INT and AD_INT) removed: not applicable.
- Table 326 (Absolute maximum ratings), p.220: Maximum value of $V_{PIN(LIM)}$(VDCDC_RF) changed from min(2,VBAT_RF+0.2) to min(3.3,VBAT_RF+0.2).
- Table 327 (Recommended operating conditions), p.221: Maximum value of V_{PIN}(VDCDC_RF) changed from 2 V to 3.3 V.
- Table 342 (RCX Oscillator: Timing characteristics), p.229: Added parameters ΔT_A/t(RCX)100ms, ΔT_A/t(RCX)4s:

ΔT_A/ Δt(RCX)100ms	ambient temperature gradient	buck mode only; connection interval 100 ms			0.66	°C/s
$\Delta T_A/\Delta$t(RCX)4s	ambient temperature gradient	buck mode only; connection interval 4 s			0.33	°C/s

- Figure 72 (WLSCSP34 Package Outline Drawing), p.233: drawing updated to Rev F (Min and Max values added to body size).

4 V3.2 (18-Dec-2015)

- Table 1 (Pin Description), p.8:
  - Programming voltage on pin VPP corrected to 6.7 V ± 0.1 V.
- Ordering information moved to new section 3 (p.9):

- Table 2: Ordering information (samples).
- Table 3: Ordering information (production).
- Table 4: Ordering information (preprogrammed OTP); previously in separate Addendum document.

- Table 5 (OTP Header), p.4:
  - 0x7F94 to 0x7FCC: Signature length corrected from 16 words to 15 words.
  - 0x7F70: Added value 0x99 for KGD.
  - 0x7F0C: Changed from ‘Reserved’ to ‘CRC for Trim and Calibration values’.
  - 0x7F10 to 0x7F60: Changed from ‘Reserved’ to ‘Customer Specific Field (21 32-bit words)’.
- Figure 71 (p.235): Package outline drawing of QFN40 updated.
- Section 21 (General purpose ADC), p.68:
  - Added section 21.9 (Delay counter).
- Table 291 (P01_PADPWR_CTRL_REG), p.210:
  - Notes 19 and 20 updated with limited output current capability in Boost mode.
- Table 292 (P2_PADPWR_CTRL_REG), p.210:
  - Note 21 updated with limited output current capability in Boost mode.
- Table 293 (P3_PADPWR_CTRL_REG), p.211:
  - Note 22 updated with limited output current capability in Boost mode.
- Table 336 (Digital Input/Output: DC characteristics), p.225:
  - Note 33 added for V_{OH}(VBAT3V): In Boost mode the output source current is limited to Iout = -250 uA.
  - Note 34 added for V_{OL}(VBAT3V): In Boost mode the output sink current is limited to Iout = 250 uA.
- Template updated to new branding guidelines.
- Back page: Contact information updated.

5 V3.1 (January 29, 2015)

- General description partly rephrased.
- Features (p.1):
  - Corrected nominal package size for WLCSP34 package.
  - Package added: KGD (wafer, dice).
- Ordering information (p.6):
  - Reformatted into separate tables for samples and production orders.
  - Table 1 (samples):
    - Discontinued: DA14580-01UN6 (WLCSP34 samples in waffle pack).
    - Replacement: DA14580-01UNA (WLCSP34 samples on mini-reel).
  - Table 2 (production):
    - Added: DA14580-01WO4 (KGD, wafer)
    - Added: DA14580-01WC4 (KGD, dice)
- Figure 9 (BootROM sequence), p.16: flow corrected to jump back to top after 5 loops in Development mode.
- Figure 17 (Clock generation block diagram) p.31: label ‘sys_clk’ added, generation of ‘tmr2_clk’ corrected.
- Section 14 (SPI+ interface), p.50: text and figures corrected for single SPI interface (SPIx -> SPI).
- Section 17 (p.56):
  - Section title changed to ‘General purpose timers’.
  - Section 17.1 (Timer 0): formulas for output frequency, duty cycle and interrupt time reformatted.

- Section 17.2 (Timer 2), p.58 and p.59:
  - Input clock frequency: corrected from 16 MHz (fixed) to sys_clk/N with N = 1, 2, 4 or 8 and sys_clk = 16 MHz or 32 kHz. Formula reformatted.
  - Output frequency: formula reformatted.
  - Figure 48 and following paragraph: input clock frequency corrected.
  - Figure 49: clock signal corrected to TMR2_CLK.
- Section 22 (Power management), p.68 to p.70:
  - Feature ‘On/off control’ removed. Not supported for normal operation.
  - Minimum voltage for Buck mode operation changed from 2.2 V to 2.35 V.
  - Figures 57 and 59 updated accordingly.
- Section 25 (Registers):
  - Table 101 (CLK_AMBA_REG), p.110: descriptions of fields PCLK_DIV and HCLK_DIV rephrased.
  - Tables 309, 310 and 311 (Px_PADPWR_CTRL_REG), p.212: Note added:
    “For buck mode the output must be powered by the 3V rail, for boost mode by the 1V rail.”
- Section 26 (Specifications), p.220:
  - Definition of MIN/MAX specifications rephrased.
  - Default measurement conditions added.
  - Table 350 (Recommended operating conditions), p.223:
    - V_{BAT}(VBAT3V)NO_OTP: parameter removed. V_{BAT}(VBAT3V) also applies when OTP is not programmed.
  - Table 351 (DC characteristics), p.223 and 224:
    - Max value added for: I_{BAT}(DP_SLP)_BOOST_8kB, I_{BAT}(EXT_SLP)_BOOST_50kB, I_{BAT}(ACT_RX)_BOOST, I_{BAT}(ACT_TX)_BOOST, I_{BAT}(DP_SLP)_BUCK_8kB, I_{BAT}(EXT_SLP)_BUCK_50kB, I_{BAT}(ACT_RX)_BUCK, I_{BAT}(ACT_TX)_BUCK.
    - Supply voltage condition removed for: I_{BAT}(DP_SLP)_BUCK_1kB, I_{BAT}(DP_SLP)_BUCK_2kB, I_{BAT}(DP_SLP)_BUCK_8kB, I_{BAT}(ACT_RX)_BOOST, I_{BAT}(ACT_TX)_BOOST, I_{BAT}(ACT_RX)_BUCK, I_{BAT}(ACT_TX)_BUCK. Default measurement conditions apply.
  - Table 364 (Radio: AC characteristics), p.229: Note 31 (reference to AN-B-017) removed.

6 V3.0 (September 25, 2014)

6.1 CRITICAL CHANGES

- Product status changed to Production, datasheet status changed to Final.
- Section 26 (Specifications), p.220: added MIN/MAX definitions and reference diagrams for Boost and Buck mode (Figures 68 and 69).
- Table 348 (Absolute maximum ratings), p.223:
  - $V_{PIN(LIM)}$(default): condition text corrected, maximum value changed from 3.6 V to min(3.6, VBAT_RF+0.2) V.
  - $V_{BAT(LIM)}$VBAT1V: minimum value changed from 0.9 V to -0.1 V.
  - $V_{BAT(LIM)}$VBAT3V: minimum value changed from 1.8 V to -0.1 V.
  - $V_{PIN(LIM)}$(1V2): minimum value changed from 0 V to -0.2 V, maximum value changed from 1.2 V to min(1.2, VBAT_RF+0.2) V.
  - Added parameter $V_{PIN(LIM)}$(VDCDC_RF) with minimum value -0.2 V, maximum value min(2, VBAT_RF+0.2) V.
  - Added parameter $V_{PIN(LIM)}$(XTAL32Kp) with minimum value -0.2 V, maximum value min(1.5, VBAT_RF+0.2) V.
  - $V_{ESD(MM)}$(WLCSP34): maximum value changed from 175 V to 200 V.
- Table 349 (Recommended operating conditions), p.224:

- V_{PP}: specification changed from 6.55 V, 6.8 V, 7.05 V (Min, Typ, Max) to 6.6 V, 6.7 V, 6.8 V (Min, Typ, Max); added condition $T_J \leq 50$ °C.
- V_{BAT}(VBAT3V): also applies to pin VBAT_RF, conditions updated accordingly.
- Added parameter V_{BAT}(VBAT3V)NO_OTP with minimum value 1.8 V, maximum value 3.3 V and condition 'OTP not programmed'.
- V_{PIN}(default): maximum value changed from 3.3 V to min(3.3, VBAT_RF+0.2).
- Added parameter V_{PIN}(VDCDC_RF) with minimum value 0 V, maximum value 2 V.
- Note 20: added text 'Trim values programmed in the OTP as well as the application image, should be copied into RAM while VBAT3V >= 2.5 V.'.

- Table 351 (Timing characteristics), p.226:
  - Added Note 21 to typical values of t_{STA}(BOOST) and t_{STA}(BUCK): 'Worst-case value under Normal Operating Conditions.'
- Table 352 (16 MHz Crystal Oscillator: Recommended operating conditions), p.226:
  - Δf_{XTAL}(16M): Min/Max values changed from -15/+15 ppm to -20/+20 ppm. Added Note 22: 'Using the internal varicaps a wide range of crystals can be trimmed to the required tolerance.'
  - Added parameter Δf_{XTAL}(16M)UNT with Min/Max values -40/+40 ppm, condition 'untrimmed' and Note 23: 'Maximum allowed frequency tolerance for compensation by the internal varicap trimming mechanism.'
- Table 363 (Radio: AC characteristics), p.230:
  - P_{SENS}(EOC) specification changed from -89 dBm (Max) to -87 dBm (Max).

6.2 NON CRITICAL CHANGES

- Figure 3 and Figure 4 (system diagrams for Boost mode and Buck Mode) moved from section 1 (Block diagram) to section 26 (Specifications) and renamed to Figure 68 and Figure 69.
- Figure 9 (BootROM sequence), p.16:
  - Timeout loop (64 ms) for checking OTP LDO voltage clarified.
  - Added step 'Switch to XTAL16M' to Development mode.
- Table 6 (Power domains), p.17: description of power domain PD_RAD (Radio) rephrased.
- Figure 17 (Clock generation block diagram), p.31: enable signal for Divide by 10 function corrected from TIMER0_CTRL_REG[TIM0_CLK_SEL] to TIMER0_CTRL_REG[TIM0_CLK_DIV].
- Figure 30 (UART block diagram), p.44: updated to only show implemented flow control signals RTS and CTS.
- Section 14 (SPI+ interface), p.50: DMA functionality removed (not supported), Figure 36 updated accordingly.
- Section 15 (Quadrature decoder), p.54:
  - Figures 41, 42 and 43 updated: pin names corrected.
  - Last paragraph removed: 'The interrupt block monitors ...'.
- Figure 50 (Watchdog timer block diagram), p.60: date removed.
- Figures 57 and 58 (Supply overview), p.69: component values removed.
- Section 23 (BLE core), p.71: redundant feature bullet on Bluetooth Smart compliance removed.
- Figure 61 (Exchange memory mapping possibilities), p.72: text edited.
- Section 25 (Registers), p.78: added references to ARM Cortex-M0 documentation.
- Table 43 (BLE_DIAGCNTL_REG), p.94: references to chapter 2.15 removed (internal design document).
- Table 108 (TRIM_CTRL_REG), p.113: Note 17 added: 'The period duration of 250 us is derived by dividing the RC16M clock signal by 4000. Consequently, the period duration may vary over temperature.'.
- Table 111 (CLK_RCX20K_REG), p.115: oscillator name 'RCX32K' corrected to 'RCX'.
- Table 137 (UART_MCR_REG), p.123: description of bit UART_AFCE clarified, reference to section "Auto Flow Control" removed (internal design document).

- Table 163 (UART_SRTS_REG), p.146: description of bit UART_SHADOW_REQUEST_TO_SEND clarified.
- Table 177 (UART2_MCR_REG), p.152: description of bit UART_AFCE clarified, reference to section “Auto Flow Control” removed (internal design document).
- Table 203 (UART2_SRTS_REG), p.175: description of bit UART_SHADOW_REQUEST_TO_SEND clarified.
- Table 338 (GP_CONTROL_REG), p.219: description of bit EM_MAP: text ‘Case <n>, available’ removed.
- Figure 68 (System diagram: Boost mode) updated, p.221:
  - Pin RST not connected
  - Pin VDCDCA renamed to VDCDC_RF
  - Pin VBATA renamed to VBAT_RF
  - C8 = 1 µF (was: 100 nF)
  - C9 = 1 µF (was: NP)
- Figure 69 (System diagram: Buck mode) updated, p.222:
  - Pin RST not connected
  - Pin VDCDCA renamed to VDCDC_RF
  - Pin VBATA renamed to VBAT_RF
  - C8 = 1 µF (was: 100 nF)
  - Added C9 = 1 µF on pin VBAT_RF
  - 32.768 kHz XTAL oscillator optional
- Table 349 (Recommended operating conditions), p.224:
  - V_{BAT}(VBAT3V) and V_{BAT}(VBAT3V)NO_OTP: reference to Note 19 moved from Conditions to Min column.
- Table 350 (DC characteristics), p.224 and p.225:
  - I_{BAT}(DP_SLP)_BOOST_1kB and I_{BAT}(DP_SLP)_BOOST_2kB: condition changed from ‘Typical boost-application’ to ‘Boost configuration’.
  - I_{BAT}(DP_SLP)_BUCK_1kB and I_{BAT}(DP_SLP)_BUCK_2kB: condition changed from ‘Typical buck-application’ to ‘Buck configuration’.
- Table 362 (Radio: DC characteristics), p.229:
  - Note 29: text ‘(VBAT3V = 3 V)’ appended.
- Back page: contact information updated.

7 V1.63 February 25 2013

7.1 CRITICAL CHANGES

- Added note about WLCSP light sensitivity at the package information chapter
- Updated Ordering Information table
- Updated clocking diagram to include GPADC and ON timer0 clocks
- Updated BootROM flow chart in system’s overview chapter
- Added Note about manual cold boot if power supply is less than 2.4V in the Power Management chapter
- Added Note on VBAT1V and VBAT3V voltage ramp up requirement in Absolute Maximum Ratings and increased max voltage levels to 3.6V
- Added Note on PSENS measurement details in specifications chapter **(only for FS!)**
- Added Near Field Mode on the features list and programming on the Specifications chapter

7.2 NON CRITICAL CHANGES

- Corrected TIM0_CLK_DIV register field description
- Corrected DEBUG_REG bit 0 reset value

- Corrected reference to Direct Test Mode at chapter 24.6
- Changed OTP header regarding the sleep clock source flag
- Removed feature “Selectable Push-pull or open drain per pin” from the Input/Output ports chapter
- Added note at the end of chapter 18 about the watchdog operation in non-remapped systems.
- Merged various notes, in the specifications chapter
- Removed RCX frequency from Block Diagram
- Revised RCX parameters in specifications chapter and added note on maximum recommended connection interval time.
- Removed DCDC registers description.

8 V1.62 January 14 2013

8.1 CRITICAL CHANGES

- Changed status to “Preliminary”
- Updated Ordering Information table
- Added IQ Trim value in OTP header (0x4708)
- Added I_{BAT}(EXT_SLP)_BOOST_43KB and I_{BAT}(EXT_SLP)_BUCK_43KB in specifications chapter

8.2 NON CRITICAL CHANGES

- Corrected various typos in several sections
- Removed VPP_EN from system diagrams
- Updated Retention RAM naming in the block diagram to follow the power domain naming (PD_xx)
- Corrected current consumption of GP_ADC to 5uA when rate at 100 ksamples

9 V1.61 December 5 2013

9.1 CRITICAL CHANGES

- Changed CLK_16M_REG[XTAL16_BIAS_SH_DISABLE] to XTAL16_BIAS_SH_ENABLE. Changed recommended usage in the register description **(Applies to ES4, FS document)**
- Changed the reset value of the CLK_16M_REG[XTAL16_CUR_SET] to 0x5 **(Applies to ES4, FS document)**
- Added Absolute Maximum Ratings table in the Specifications section
- Updated Specification tables with ES3 measured and characterized values

9.2 NON CRITICAL CHANGES

- Updated text in almost all sections regarding spelling or grammar mistakes
- Updated front page with correct number of available GPIOs for all packages

10 V1.50 September 6 2013

10.1 CRITICAL CHANGES

- Added 6KBytes of Retention RAM - 4 difference RAM cells. Total RAM size is now 50KB including SysRAM
- Changed BootROM code to search for specific values and not any values to identify the mode of operation (Normal, Development)
- Increased number of pads to support more GPIOs. QFN48 package is now also supported with 32 GPIOs. QFN40 and WLCSP34 remain unchanged
- Changed Baudrate of UART pin pairs while booting from UART in Development Mode
- Decreased power consumption in Extended Sleep mode
- Added a third Quadrature Decoder Axis for supporting the mouse scrolling wheel
- Added 3 extra PWM signals that can be mapped in any GPIO

- Added RCX oscillator with precision <500ppm and immune at temperature/voltage changes

10.2 NON CRITICAL CHANGES

- Added ble_rf_diag interrupt for debugging capabilities
- Decreased XTAL Oscillator settle and trim time
- Added description for the General Purpose ADC
- Changed Booting flow charts for HW and SW (BootROM code)

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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