General Description

The DA1470x is a family of multi-core wireless microcontrollers, combining the latest Arm Cortex M33™ application processor with floating-point unit, advanced power management functionality, a Graphic Processing Unit (GPU) for advanced graphics processing, a cryptographic security engine, analog and digital peripherals, a dedicated sensor node controller, and a software configurable protocol engine with a radio that is compliant to the Bluetooth® 5.2 low energy standard.

The DA1470x is based on an Arm Cortex-M33™ CPU with an eight-segments Memory Protection Unit (MPU), DSP extensions and a single-precision Floating Point Unit (FPU) offering up to 240 dMIPS. The dedicated application processor executes code from an external Octa/Quad SPI FLASH device equipped with an on-the-fly decrypting engine, via an 8 kB four-way set associative instruction cache controller. It has a software-configurable Bluetooth® low energy protocol engine (MAC) with an ultra-low-power radio transceiver, capable of +6 dBm output power, and -97 dBm sensitivity offering a total link budget of 103 dB.

DA1470x comprises a 2D GPU, successfully combining ultra-low power capabilities with advanced graphic processing. It also has an integrated two-layer display controller with multiple display output options like Parallel DPI/DBI/JDI and Single/Dual/Quad SPI.

An optimized programmable sensor node controller based on Arm Cortex M0+ allows sensor node operations and data acquisition with the rest of the system in shut down mode, achieving best-in-class power consumption.

The advanced power management unit (PMU) of the DA1470x enables it to run on primary and secondary batteries, as well as provide power to external devices through the integrated low quiescent current (Iq) SIMO DCDC and integrated LDOs. The on-chip JEITA-compliant hardware charger makes it possible to safely charge rechargeable batteries over USB.

A variety of standard and advanced peripherals enable interaction with other system components and the development of advanced user interfaces and feature-rich applications.

Key Features

- Compatible with Bluetooth® 5.2, ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan)
- Flexible processing power
  - 32 kHz up to 160 MHz 32-bit Arm Cortex-M33 with 8 kB, four-way associative cache, FPU and eight-segments MPU
  - A flexible and configurable Bluetooth® Low Energy MAC engine implementing the controller stack up to HCI
  - An Arm Cortex M0+ based sensor node controller for sensors manipulation
  - A 2D GPU for advanced graphics processing
  - Optimized power modes (Extended sleep, Deep sleep, and Hibernation)
- Memories
  - 1.5 MB Data SRAM with retention
  - 4 kB One-Time-Programmable (OTP) memory for secure key storage
  - 8 kB ICache SRAM with retention
  - 8 kB DCache SRAM with retention
  - 32 kB ROM (boot, PKI routines)
- Power management
  - Low Iq SIMO Buck DC-DC converter
  - Boost DC-DC converter (4.5 V – 5.0 V)
  - Four power supply pins for external devices DCDC supported
  - Hardware charger (up to 5.0 V) with programmable curves and JEITA support
  - Integrated Power Path Management

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- Digital controlled oscillators
  - High Speed RC 32/64/96 MHz (RCHS) with 1.5 % precision
  - 32 MHz crystal oscillator
  - Low Power RC 32/512 kHz (RCLP)
  - RCX oscillator (±500 ppm max) and optional 32 kHz crystal oscillator
- Real Time Clock with 10 ms resolution
- Six General purpose, 24-bit up/down timers with PWM
- Application cryptographic engine with AES-128/192/256, SHA-224/256/384/512 and a True Random Number Generator (TRNG)
- Digital interfaces
  - Up to 79 General Purpose I/Os
  - Decrypt-on-the-fly Octa/Quad SPI FLASH interface
  - Dedicated QSPI PSRAM and QSPI FLASH interfaces
  - eMMC interfaces supporting up to 48 MHz SDR mode
  - Parallel-DPI/DBIB/JDI, SPI/DualSPI/QSPI Display Controller with own DMA and two layers support
  - 3 x UARTs up to 6 Mbps, one UART extended to support ISO7816
  - 3 x SPI+™ controllers
  - MIPI I3C controller at 12.5 MHz
  - 3 x I2C controllers at 100 kHz, 400 kHz, or 3.4 MHz
  - PDM interface with dual HW sample rate converter (SRC)
  - I2S/PCM master/slave interface up to eight channels
  - USB 1.1 Full Speed device interface
- Analog interfaces
  - Ultra-Low Power Voice Activity Detection (VAD) enabling seamless audio processing with system-on current < 26 µA
  - Four-channel 10-bit SAR General Purpose ADC, 2.6 Msps
  - 11 ENOB, 16 Ksps Audio ADC with Programmable Gain Amplifier
  - Three matched White LED drivers
- Radio transceiver
  - Single wire antenna: no RF matching or RX/TX switching required
  - Supply current at VBAT: TX: 3 mA, RX: 1.85 mA (with ideal DC-DC)
  - Configurable transmit output power -18 to +6 dBm
  - -97 dBm receiver sensitivity
- Packages:
  - VFBGA142, 6.2x6, 0.45 mm pitch

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Applications

- Fitness trackers
- Sport watches
- Smartwatches
- Consumer medical devices
- Consumer and home appliances
- Home automation
- Industrial automation and security systems
- Gaming consoles

Key Benefits

- Highest level of performance for advanced applications
- Highest level of integration to drive system cost down
- Lowest power consumption to optimize battery life

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1 Block Diagram

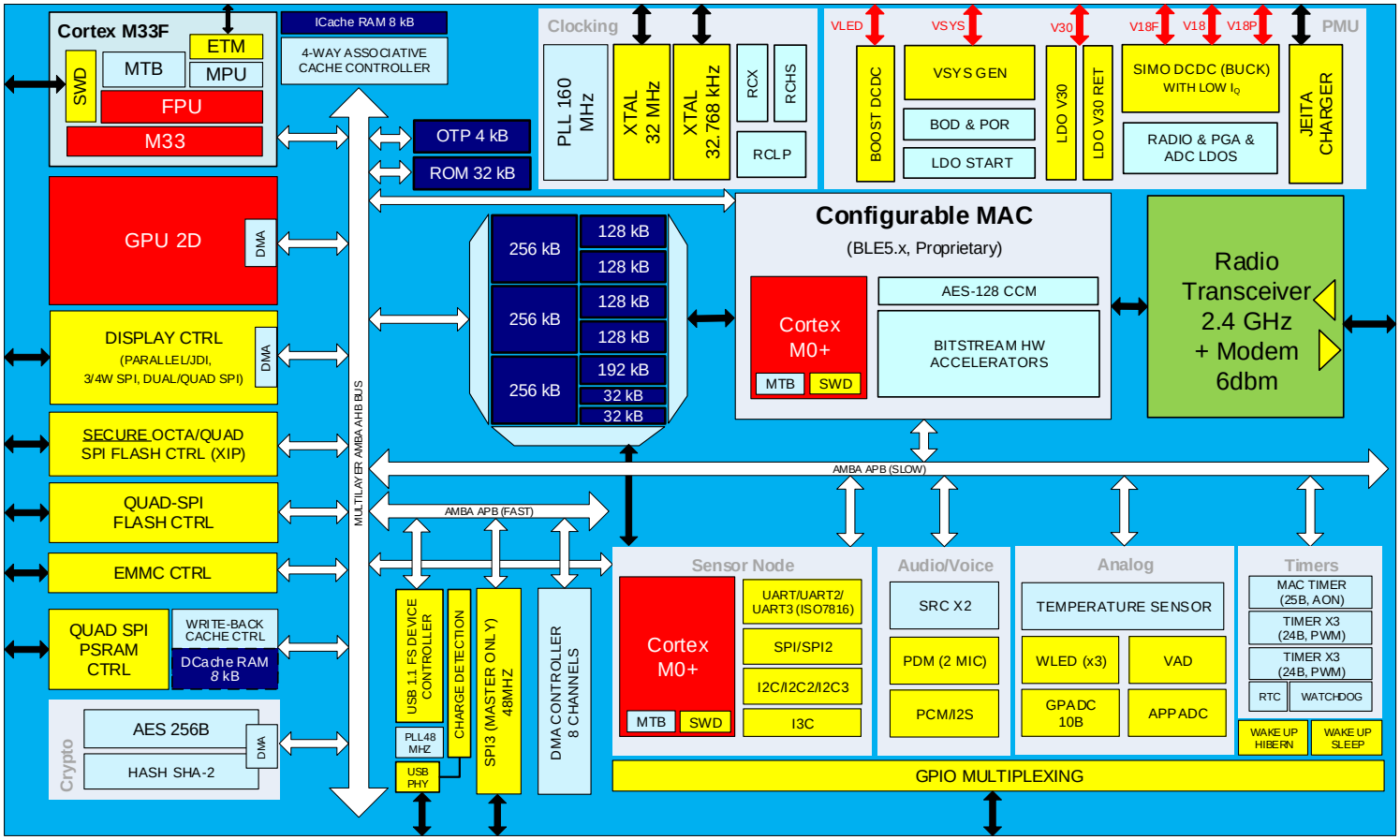

Figure 1: DA1470x Block Diagram

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2 DA1470x Product Family

Table 1 presents the differentiation among the members of the DA1470x product family.

Table 1: DA1470x Product Family Differentiation

Features	DA14701	DA14705	DA14706	DA14708
External PSRAM with Data Cache	✓	✗	✓	✓
JEITA Charger	✗	✓	✓	✓
Boost DCDC converter	✗	✓	✓	✓
eMMC	✓	✗	✗	✓
Rest of features	✓	✓	✓	✓

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3 Pinout

The DA1470x comes in a VFBGA142 6.2x6 mm package with 0.45 mm pitch and 0.25 mm ball diameter. The actual pin/ball assignment is depicted in the following section.

3.1 VFBGA142 Pinout

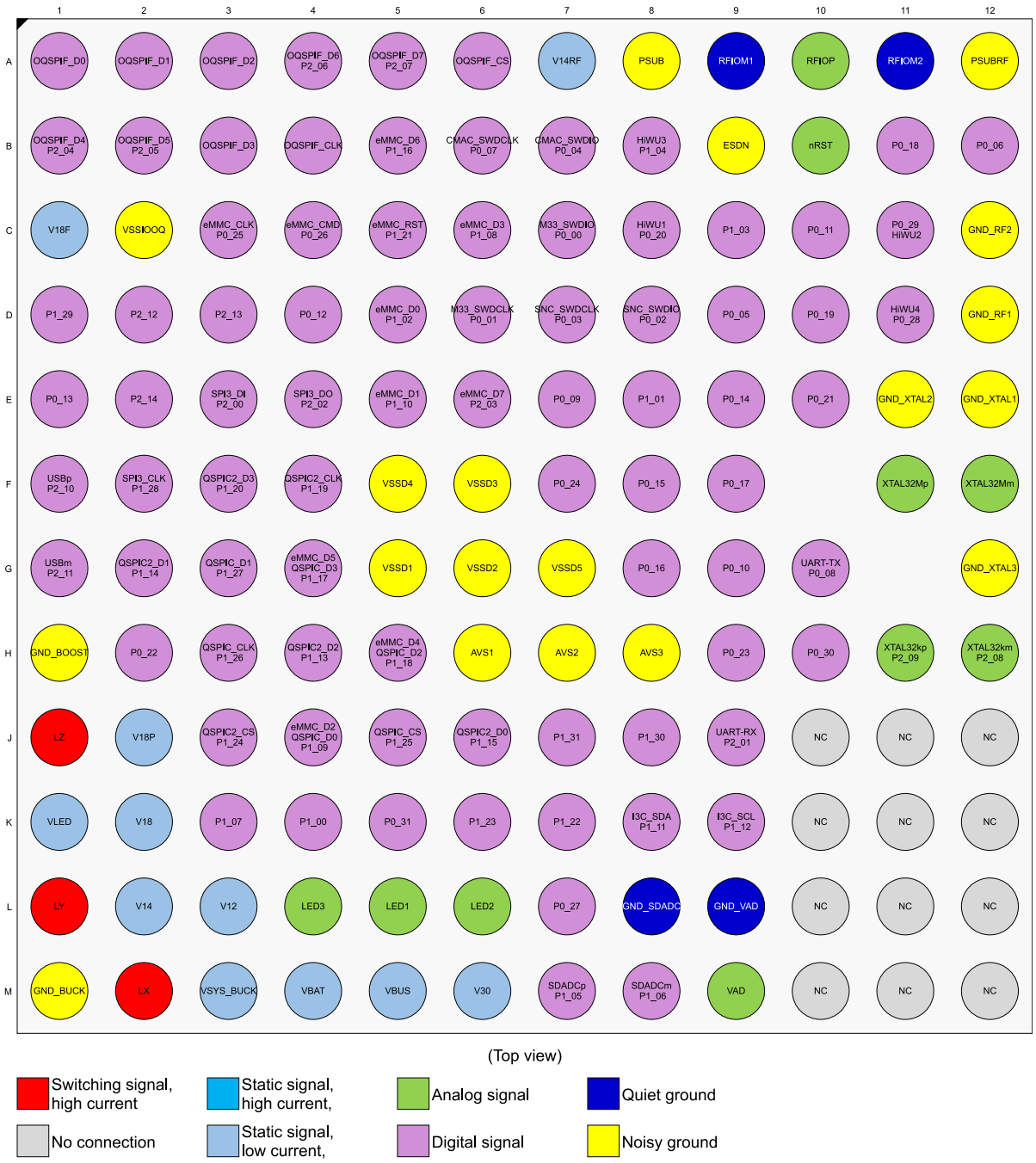

Figure 2: VFBGA142 Ball Assignment

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Table 2: DA1470x Pin Description

Ball No.	Pin Name	Type	Reset State	Description
General Purpose I/Os and fixed pin assignment				
A4	P2_06	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	OQSPIF_D6	DIO		INPUT/OUTPUT. OQSPI Flash I/O data 6.
A5	P2_07	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	OQSPIF_D7	DIO		INPUT/OUTPUT. OQSPI Flash I/O data 7.
B1	P2_04	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	OQSPIF_D4	DIO		INPUT/OUTPUT. OQSPI Flash I/O data 4.
B2	P2_05	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	OQSPIF_D5	DIO		INPUT/OUTPUT. OQSPI Flash I/O data 5.
B5	P1_16	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	eMMC_D6	DIO		INPUT/OUTPUT. eMMC I/O data 6.
B6	P0_07	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	CMAC_SWDCLK	DI		INPUT. Arm Cortex-M0+ (CMAC) SWD clock signal.
B7	P0_04	DIO	I-PU	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-up enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	CMAC_SWDIO	DI		INPUT. ARM Cortex-M0+ (CMAC) SWD data I/O signal.
B8	P1_04	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	HiWU3	DI		INPUT. Hibernation wake-up trigger 3.

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Ball No.	Pin Name	Type	Reset State	Description
B11	P0_18	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	JDI_ENB	DO		OUTPUT. JDI Write enable signal for the pixel memory.
	LCD_CS	DO		OUTPUT. Display Chip select.
B12	P0_06	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	GPADC2	AI		INPUT. Analog input for the general-purpose ADC, channel 2.
C3	P0_25	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	eMMC_CLK	DO		OUTPUT. eMMC Host to card clock signal.
C4	P0_26	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	eMMC_CMD	DIO		INPUT/OUTPUT. eMMC Bidirectional Command/Response signal.
C5	P1_21	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	eMMC_RST	DO		OUTPUT. eMMC Reset signal.
C6	P1_08	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	eMMC_D3	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 3.
C7	P0_00	DIO	I-PU	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-up enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	M33_SWDIO	DIO		INPUT/OUTPUT. ARM Cortex-M33 SWD data I/O signal.
C8	P0_20	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	DIVN	DO		OUTPUT. DIVN clock signal output (square wave).

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Ball No.	Pin Name	Type	Reset State	Description
	HiWU1	DI		INPUT. Hibernation wake-up trigger 1.
C9	P1_03	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
C10	P0_11	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	NTC Supply	AO		OUTPUT. Power supply for the battery NTC sensor.
C11	P0_29	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	NTC Sense	AI		INPUT. Analog input for battery NTC (feedback).
	HiWU2	DI		INPUT. Hibernation wake-up trigger 2.
D1	P1_29	DIO	I-PU	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-up enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
D2	P2_12	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
D3	P2_13	DIO	I-PU	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-up enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
D4	P0_12	DIO	I-PU	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-up enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
D5	P1_02	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	eMMC_D0	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 0.
D6	P0_01	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	M33_SWDCLK	DI		INPUT. Arm Cortex-M33 SWD clock signal.

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Ball No.	Pin Name	Type	Reset State	Description
D7	P0_03	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	SNC_SWDCLK	DI		INPUT. SNC ARM Cortex-M0+ SWD clock signal.
D8	P0_02	DIO	I-PU	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-up enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	SNC_SWDIO	DIO		INPUT/OUTPUT. SNC ARM Cortex-M0+ SWD data I/O signal.
D9	P0_05	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	GPADC1	AI		INPUT. Analog input for the general-purpose ADC, channel 1.
D10	P0_19	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	JDI_VCOM/FRP	DO		OUTPUT. JDI Common electrode driving signal (62.5 Hz).
	LCD_EXTCOMIN	DO		OUTPUT. Display COM Inversion Signal Input (1 Hz).
D11	P0_28	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	HiWU4	DI		INPUT. Hibernation wake-up trigger 4.
E1	P0_13	DIO	I-PU	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-up enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
E2	P2_14	DIO	I-PU	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-up enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
E3	P2_00	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	SPI3_DI	DI		INPUT. SPI3 data input signal (MISO).

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Ball No.	Pin Name	Type	Reset State	Description
E4	P2_02	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	SPI3_DO	DO		OUTPUT. SPI3 data output signal (MOSI).
E5	P1_10	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	eMMC_D1	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 1.
E6	P2_03	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	eMMC_D7	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 7.
E7	P0_09	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	JDI_VCK	DO		OUTPUT. JDI Shift clock for the vertical driver.
	XTAL32M	DO		OUTPUT. XTAL32M clock signal output (square wave).
E8	P1_01	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	JDI_BLUE0	DO		OUTPUT. JDI Blue image data output, bit 0.
E9	P0_14	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	JDI_HCK	DO		OUTPUT. JDI Shift clock signal for the horizontal driver.
	LCD_SPI_SCLK	DO		OUTPUT. Display serial clock signal.
E10	P0_21	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	JDI_BLUE1	DO		OUTPUT. JDI Blue image data output, bit 1.

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Ball No.	Pin Name	Type	Reset State	Description
F1	P2_10	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Does not contain state retention mechanism during power down.
	USBp	AIO		INPUT/OUTPUT. Analog USB Full Speed D+ signal.
F2	P1_28	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	SPI3_CLK	DO		OUTPUT. SPI3 clock signal.
F3	P1_20	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	QSPIC2_D3	DIO		INPUT/OUTPUT. QSPIC2 Bidirectional data signal, bit 3.
F4	P1_19	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	QSPIC2_CLK	DO		OUTPUT. QSPIC2 clock signal.
F7	P0_24	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	JDI_GREEN0	DO		OUTPUT. JDI Green image data output, bit 0.
F8	P0_15	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	JDI_HST	DO		OUTPUT. Start signal for the horizontal driver.
	LCD_SPI_SD/SI	DIO		INPUT/OUTPUT. Display Bidirectional Serial data 0 (SPI3, SPI4, DualSPI, QuadSPI).
F9	P0_17	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	JDI_RED0	DO		OUTPUT. JDI Red image data output, bit 0.
	LCD_SPI_SD3	DO		OUTPUT. Display Serial data 3 (QuadSPI)

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Ball No.	Pin Name	Type	Reset State	Description
G1	P2_11	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Does not contain state retention mechanism during power down.
	USBm	AIO		INPUT/OUTPUT. Analog USB Full Speed D- signal.
G2	P1_14	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	QSPIC2_D1	DIO		INPUT/OUTPUT. QSPIC2 Bidirectional data signal, bit 1.
G3	P1_27	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	QSPIC_D1	DIO		INPUT/OUTPUT. QSPIC Bidirectional data signal, bit 1.
G4	P1_17	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	eMMC_D5	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 5.
	QSPIC_D3	DIO		INPUT/OUTPUT. QSPIC Bidirectional data signal, bit 3.
G8	P0_16	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	JDI_VST	DO		OUTPUT. JDI display Row pointer reset indication signal to top of the display.
	LCD_SPI_SD1/DC	DO		OUTPUT. Dispaly Serial data 1 (DualSPI, QuadSPI) - Data/Command select (SPI4).
G9	P0_10	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	JDI_XFRP	DO		OUTPUT. Display Liquid crystal driving signal (62.5Hz inverted).
	LCD_TE	DI		INPUT. Display Tearing effect signal. Used to synchronize the CPU to the frame memory writing.
G10	P0_08	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	UART Boot TX	DO		OUTPUT. UART Transmit data output during boot.

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Ball No.	Pin Name	Type	Reset State	Description
H2	P0_22	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	JDI_XRST	DO		OUTPUT. Display Reset signal for the horizontal and vertical driver.
	LCD_SPI_SD2	DO		OUTPUT. Display Serial data 2 (QuadSPI).
H3	P1_26	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	QSPIC_CLK	DO		OUTPUT. QSPIC clock signal.
H4	P1_13	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	QSPIC2_D2	DIO		INPUT/OUTPUT. QSPIC2 Bidirectional data signal, bit 2.
H5	P1_18	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	eMMC_D4	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 4.
	QSPIC_D2	DIO		INPUT/OUTPUT. QSPIC Bidirectional data signal, bit 2.
H9	P0_23	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	JDI_RED1	DO		OUTPUT. JDI Red image data output, bit 1.
H10	P0_30	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	GPADC4	AI		INPUT. Analog input for the general-purpose ADC, channel 4.
	Timer.PWM	DO		OUTPUT. Timer/PWM output (PWM) in Sleep mode.
H11	P2_09	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	XTAL32kp	AI		INPUT. Analog input of the XTAL32K crystal oscillator.
		DI		INPUT. Digital input for an external clock (square wave).

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Ball No.	Pin Name	Type	Reset State	Description
H12	P2_08	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	XTAL32km	AO		OUTPUT. Analog output of the XTAL32K crystal oscillator.
J3	P1_24	DIO	I-PU	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-up enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	QSPIC2_CS	DO		OUTPUT. QSPIC2 chip select signal.
J4	P1_09	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	eMMC_D2	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 2.
	QSPIC_D0	DIO		INPUT/OUTPUT. QSPIC Bidirectional data signal, bit 0
J5	P1_25	DIO	I-PU	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-up enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	QSPIC_CS	DO		OUTPUT. QSPIC chip select signal.
J6	P1_15	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down (Note 3).
	QSPIC2_D0	DIO		INPUT/OUTPUT. QSPIC2 Bidirectional data signal, bit 0.
J7	P1_31	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	TRACE_DATA[2]	DO		INPUT/OUTPUT. ETM data signal, bit 2.
	Timer4.PWM	DO		OUTPUT. Timer4/PWM output (PWM) in Sleep mode.
J8	P1_30	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	TRACE_DATA[0]	DO		INPUT/OUTPUT. ETM data signal, bit 0.
	Timer3.PWM	DO		OUTPUT. Timer3/PWM output (PWM) in Sleep mode.

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Ball No.	Pin Name	Type	Reset State	Description
J9	P2_01	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	UART Boot RX	DI		INPUT. UART Receive data input during boot.
K3	P1_07	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
K4	P1_00	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	JDI_GREEN1	DO		OUTPUT. JDI Green image data output, bit 1.
K5	P0_31	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	TRACE_CLK	DO		INPUT. ETM clock signal.
	XTAL32k	DO		OUTPUT. XTAL32k clock signal output (square wave).
K6	P1_23	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	TRACE_DATA[3]	DO		INPUT/OUTPUT. ETM data signal, bit 3.
	RCLP	DO		OUTPUT. RCLP clock signal output (square wave).
K7	P1_22	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	TRACE_DATA[1]	DO		INPUT/OUTPUT. ETM data signal, bit 1.
	RCX	DO		OUTPUT. RCX clock signal output (square wave).
K8	P1_11	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	I3C_SDA	DIO		INPUT/OUTPUT. I3C Bidirectional data signal.
K9	P1_12	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	I3C_SCL	DO		OUTPUT. I3C clock signal.

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Ball No.	Pin Name	Type	Reset State	Description
L7	P0_27	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	GPADC3	AI		INPUT. Analog input for the general-purpose ADC, channel 4.
M7	P1_05	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	SDADCp/PGAp	AI		INPUT. Programmable gain amplifier positive input (SDADC positive input).
M8	P1_06	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	SDADCm/PGAm	AI		INPUT. Programmable gain amplifier negative input (SDADC negative input).
Debug Interfaces				
C7	M33_SWDIO	DIO	I-PU	INPUT/OUTPUT. ARM Cortex-M33 SWD data I/O signal.
D6	M33_SWDCLK	DI	I-PD	INPUT. Arm Cortex-M33 SWD clock signal.
B7	CMAC_SWDIO	DIO	I-PU	INPUT/OUTPUT. ARM Cortex-M0+ SWD data I/O signal.
B6	CMAC_SWDCLK	DI	I-PD	INPUT. ARM Cortex-M0+ SWD clock signal.
D8	SNC_SWDIO	DIO	I-PU	INPUT/OUTPUT. ARM Cortex-M0+ SWD data I/O signal.
D7	SNC_SWDCLK	DI	I-PD	INPUT. ARM Cortex-M0+ SWD clock signal.
K5	TRACE_CLK	DO	I-PD	INPUT/OUTPUT. ETM clock signal.
J8	TRACE_DATA[0]	DO	I-PD	INPUT/OUTPUT. ETM data signal, bit 0.
K7	TRACE_DATA[1]	DO	I-PD	INPUT/OUTPUT. ETM data signal, bit 1.
J7	TRACE_DATA[2]	DO	I-PD	INPUT/OUTPUT. ETM data signal, bit 2.
K6	TRACE_DATA[3]	DO	I-PD	INPUT/OUTPUT. ETM data signal, bit 3.
Octa and Quad SPI Interfaces				
A1	OQSPIF_D0	DIO	I-PD	INPUT/OUTPUT. OQSPIF Bidirectional data signal, bit 0.
A2	OQSPIF_D1	DIO	I-PD	INPUT/OUTPUT. OQSPIF Bidirectional data signal, bit 1.
A3	OQSPIF_D2	DIO	I-PD	INPUT/OUTPUT. OQSPIF Bidirectional data signal, bit 2.
B3	OQSPIF_D3	DIO	I-PD	INPUT/OUTPUT. OQSPIF Bidirectional data signal, bit 3.
B1	OQSPIF_D4	DIO	I-PD	INPUT/OUTPUT. OQSPIF Bidirectional data signal, bit 4.

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Ball No.	Pin Name	Type	Reset State	Description
B2	OQSPIF_D5	DIO	I-PD	INPUT/OUTPUT. OQSPIF Bidirectional data signal, bit 5.
A4	OQSPIF_D6	DIO	I-PD	INPUT/OUTPUT. OQSPIF Bidirectional data signal, bit 6.
A5	OQSPIF_D7	DIO	I-PD	INPUT/OUTPUT. OQSPIF Bidirectional data signal, bit 7.
B4	OQSPIF_CLK	DO	I-PD	OUTPUT. OQSPIF clock signal.
A6	OQSPIF_CS	DO	I-PU	OUTPUT. OQSPIF chip select signal (active LOW).
J4	QSPIC_D0	DIO	I-PD	INPUT/OUTPUT. QSPIC Bidirectional data signal, bit 0.
G3	QSPIC_D1	DIO	I-PD	INPUT/OUTPUT. QSPIC Bidirectional data signal, bit 1.
H5	QSPIC_D2	DIO	I-PD	INPUT/OUTPUT. QSPIC Bidirectional data signal, bit 2.
G4	QSPIC_D3	DIO	I-PD	INPUT/OUTPUT. QSPIC Bidirectional data signal, bit 3.
J5	QSPIC_CS	DO	I-PU	OUTPUT. QSPIC chip select signal (active LOW).
H3	QSPIC_CLK	DO	I-PD	OUTPUT. QSPIC clock signal.
J6	QSPIC2_D0	DIO	I-PD	INPUT/OUTPUT. QSPIC2 Bidirectional data signal, bit 0.
G2	QSPIC2_D1	DIO	I-PD	INPUT/OUTPUT. QSPIC2 Bidirectional data signal, bit 1.
H4	QSPIC2_D2	DIO	I-PD	INPUT/OUTPUT. QSPIC2 Bidirectional data signal, bit 2.
F3	QSPIC2_D3	DIO	I-PD	INPUT/OUTPUT. QSPIC2 Bidirectional data signal, bit 3.
J3	QSPIC2_CS	DO	I-PU	OUTPUT. QSPIC2 chip select signal (active LOW).
F4	QSPIC2_CLK	DO	I-PD	OUTPUT. QSPIC2 clock signal.
Clocks				
H12	XTAL32km	AO		OUTPUT. Analog output of the 32.768 kHz XTAL oscillator.
H11	XTAL32kp	AI DI		INPUT. Analog input of the 32.768 kHz XTAL crystal oscillator. INPUT. Digital input for an external clock (square wave).
F12	XTAL32Mm	AO		OUTPUT. Crystal output for the 32 MHz XTAL oscillator.
F11	XTAL32Mp	AI		INPUT. Crystal input for the 32 MHz XTAL oscillator.
E12	GND_XTAL1	AI		INPUT. Analog input ground of the 32 MHz XTAL oscillator.
E11	GND_XTAL2	AI		INPUT. Analog input ground of the 32 MHz XTAL oscillator.
G12	GND_XTAL3	AI		INPUT. Analog input ground of the 32 MHz XTAL oscillator.
SPI/SPI2 Bus Interface (mapped on port Px_yy) and SPI3 Bus Interface				
	SPI_DI	DI		INPUT. SPI data input. (Note 1)
	SPI_DO	DO		OUTPUT. SPI data output. (Note 2)
	SPI_CLK	DIO		INPUT/OUTPUT. SPI clock.

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Ball No.	Pin Name	Type	Reset State	Description
	SPI_EN	DI		INPUT. SPI clock enable (chip select).
	SPI2_DI	DI		INPUT. SPI2 data input. (Note 1)
	SPI2_DO	DO		OUTPUT. SPI2 data output. (Note 2)
	SPI2_CLK	DIO		INPUT/OUTPUT. SPI2 clock.
	SPI2_EN	DI		INPUT. SPI2 clock enable (chip select).
E3	SPI3_DI	DI		INPUT. SPI3 data input (MISO)
E4	SPI3_DO	DO		OUTPUT. SPI3 data output (MOSI)
F2	SPI3_CLK	DIO		INPUT/OUTPUT. SPI3 clock.
	SPI3_EN	DI		INPUT. SPI3 clock enable (chip select).
I2C/I3C Bus Interface (mapped on port Px_yy)				
	I2C_SCL	DIO/ DIOD		INPUT/OUTPUT. I2C bus clock with open drain port. Supports bit stretching by a slave in open drain mode.
	I2C_SDA	DIO/ DIOD		INPUT/OUTPUT. I2C bus data with open drain port.
	I2C2_SCL	DIO/ DIOD		INPUT/OUTPUT. I2C bus clock with open drain port. Supports bit stretching by a slave in open drain mode.
	I2C2_SDA	DIO/ DIOD		INPUT/OUTPUT. I2C bus data with open drain port.
	I2C3_SCL	DIO/ DIOD		INPUT/OUTPUT. I2C bus clock with open drain port. Supports bit stretching by a slave in open drain mode.
	I2C3_SDA	DIO/ DIOD		INPUT/OUTPUT. I2C bus data with open drain port.
K9	I3C_SCL	DO		OUTPUT. I3C clock signal.
K8	I3C_SDA	DIO		INPUT/OUTPUT. I3C Bidirectional data signal.
UART Interface (mapped on port Px_yy)				
	UART_RX	DI		INPUT. UART receive data.
	UART_TX	DO		OUTPUT. UART transmit data.
	UART2_RX	DI		INPUT. UART 2 receive data.
	UART2_TX	DO		OUTPUT. UART 2 transmit data.
	UART2_CTS	DI		INPUT. UART 2 clear to send.
	UART2_RTS	DO		OUTPUT. UART 2 request to send.
	UART3_RX	DI		INPUT. UART 3 receive data.
	UART3_TX	DO		OUTPUT. UART 3 transmit data.
	UART3_CTS	DI		INPUT. UART 3 clear to send.
	UART3_RTS	DO		OUTPUT. UART 3 request to send.
ISO7816 Bus Interface (mapped on port Px_yy)				
	ISO7816_CLK	DO		OUTPUT. Smart card (ISO7816) clock signal.
	ISO7816_DATA	DIO		INPUT/OUTPUT. Smart card (ISO7816) I/O data signal.
	ISO7816_RST	DO		OUTPUT. Smart card (ISO7816) reset signal.
	ISO7816_CI	DI		INPUT. Smart card (ISO7816) inserted signal.

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Ball No.	Pin Name	Type	Reset State	Description
PCM Interface (mapped on port Px_yy)				
	PCM_DI	DI		INPUT. PCM input data.
	PCM_DO	DO		OUTPUT.PCM output data.
	PCM_FSC	DIO		INPUT/OUTPUT. PCM Frame synchronization.
	PCM_CLK	DIO		INPUT/OUTPUT. PCM Clock
PDM Interface (mapped on port Px_yy)				
	PDM_DATA	DIO		INPUT/OUTPUT. PDM data.
	PDM_CLK	DO		OUTPUT. PDM clock output.
eMMC Interface				
C4	eMMC_CMD	DIO		INPUT/OUTPUT. Bidirectional Command/Response signal.
C3	eMMC_CLK	DO		OUTPUT. eMMC Host to card clock signal.
D5	eMMC_D0	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 0.
E5	eMMC_D1	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 1.
J4	eMMC_D2	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 2.
C6	eMMC_D3	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 3.
H5	eMMC_D4	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 4.
G4	eMMC_D5	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 5.
B5	eMMC_D6	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 6.
E6	eMMC_D7	DIO		INPUT/OUTPUT. eMMC Bidirectional data signal, bit 7.
C5	eMMC_RST	DO		OUTPUT. eMMC Reset signal.
JDI Parallel Display Interface				
E9	JDI_HCK	DO		OUTPUT. JDI Shift clock signal for the horizontal driver.
B11	JDI_ENB	DO		OUTPUT. JDI Write enable signal for the pixel memory.
F8	JDI_HST	DO		OUTPUT. Start signal for the horizontal driver.
G8	JDI_VST	DO		OUTPUT. JDI Display Row pointer reset indication signal to top of the display.
H2	JDI_XRST	DO		OUTPUT. Display Reset signal for the horizontal and vertical driver.
E7	JDI_VCK	DO		OUTPUT. JDI Shift clock for the vertical driver.
F9	JDI_RED0	DO		OUTPUT. JDI Red image data output, bit 0.
H9	JDI_RED1	DO		OUTPUT. JDI Red image data output, bit 1.
F7	JDI_GREEN0	DO		OUTPUT. JDI Green image data output, bit 0.
K4	JDI_GREEN1	DO		OUTPUT. JDI Green image data output, bit 1.
E8	JDI_BLUE0	DO		OUTPUT. JDI Blue image data output, bit 0.
E10	JDI_BLUE1	DO		OUTPUT. JDI Blue image data output, bit 1.
D10	JDI_VCOM/FRP	DO		OUTPUT. JDI Common electrode driving signal (62.5 Hz).
G9	JDI_XFRP	DO		OUTPUT. Display Liquid crystal driving signal (62.5 Hz inverted).

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Ball No.	Pin Name	Type	Reset State	Description
Quad, Dual and SPI3/4 Display Interface				
E9	LCD_SPI_SCLK	DO		OUTPUT. Display serial clock signal.
B11	LCD_CS	DO		OUTPUT. Display Chip select.
F8	LCD_SPI_SD/SI	DIO		INPUT/OUTPUT. Display Bi-Directional Serial data 0 (SPI3, SPI4, DualSPI, QuadSPI).
G8	LCD_SPI_SD1/DC	DO		OUTPUT. Display Serial data 1 (DualSPI, QuadSPI) - Data/Command select (SPI4).
H2	LCD_SPI_SD2	DO		OUTPUT. Display Serial data 2 (QuadSPI).
F9	LCD_SPI_SD3	DO		OUTPUT. Display Serial data 3 (QuadSPI).
D10	EXTCOMIN	DO		OUTPUT. Display COM Inversion Signal Input (1 Hz).
G9	LCD_TE	DI		INPUT. Display Tearing effect signal. Used to synchronize the CPU to the frame memory writing.
Analog				
M9	VAD	AI		INPUT. Analog Input of the Voice Activity Detection Engine.
L9	GND_VAD			Voice Activity Detection Engine Ground.
D9	GPADC1	AI		INPUT. Analog input for the general-purpose ADC, channel 1.
B12	GPADC2	AI		INPUT. Analog input for the general-purpose ADC, channel 2.
L7	GPADC3	AI		INPUT. Analog input for the general-purpose ADC, channel 3.
H10	GPADC4	AI		INPUT. Analog input for the general-purpose ADC, channel 4.
M7	PGAp/SDADCp	AI		INPUT. Programmable gain amplifier (PGA) positive input (SD-ADC).
M8	PGAm/SDADCm	AI		INPUT. Programmable gain amplifier (PGA) negative input (SD-ADC).
L8	GND_SDADC			SD ADC Ground.
L11	NC			No Connection.
M11	NC			No Connection.
M12	NC			No Connection.
L12	NC			No Connection.
K12	NC			No Connection.
K11	NC			No Connection.
L10	NC			No Connection. It is recommended to connect it to GND.
M10	NC			No Connection. It is recommended to connect it to GND.
J11	NC			No Connection.
J12	NC			No Connection. It is recommended to connect it to GND.
K10	NC			No Connection. It is recommended to connect it to GND.

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Ball No.	Pin Name	Type	Reset State	Description
J10	NC			No Connection.
Miscellaneous				
B10	nRST	AI		INPUT. Reset signal (active LOW).
L5	LED1	AO		OUTPUT. LED 1 driver output (open drain, 20 mA maximum).
L6	LED2	AO		OUTPUT. LED 2 driver output (open drain, 20 mA maximum).
L4	LED3	AO		OUTPUT. LED 3 driver output (open drain, 20 mA maximum).
C11	NTC Sense	AI		INPUT. Analog input for battery NTC (feedback).
C10	NTC Supply	AO		OUTPUT. Power supply for battery NTC sensor.
USB Interface				
F1	USBp	AIO		INPUT/OUTPUT. Analog USB Full Speed D+ signal.
G1	USBm	AIO		INPUT/OUTPUT. Analog USB Full Speed D- signal.
Radio Interface				
A10	RFIOP	AIO		RF input/output. Impedance 50 Ω.
A9	RFIOM1			RF Ground
A11	RFIOM2			RF Ground
A8	PSUB			RF Ground.
A12	PSUBRF			RF Ground.
D12	GND_RF1			RF Ground.
C12	GND_RF2			RF Ground.
B9	ESDN			RF Ground.
Power Supply				
M4	VBAT	AI		INPUT. Battery supply rail.
M5	VBUS	AI AI		INPUT. USB bus voltage. INPUT. Battery charge voltage.
M3	VSYS	AO		OUTPUT. Variable output voltage power rail. Maximum current 1000 mA. 10 µF decoupling capacitor required.
M6	V30	AO		OUTPUT. 3.0 V power rail. Maximum current 150 mA. 4.7 µF decoupling capacitor required.
C1	V18F	AO		OUTPUT. 1.8 V power rail. Maximum current 30 mA. 0.1 µF decoupling capacitor required.
J2	V18P	AO		OUTPUT. 1.8 V power rail. Maximum current 100 mA. 22 µF decoupling capacitor required.
K2	V18	AO		OUTPUT. 1.8 V power rail. Maximum current 100 mA. 22 µF decoupling capacitor required.
L2	V14	AO		OUTPUT. 1.4 V power rail. Maximum current 20 mA. 10 µF decoupling capacitor required.
A7	V14RF	AI		INPUT. Radio supply voltage. Connect to V14 externally. 10 µF decoupling capacitor required.

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Ball No.	Pin Name	Type	Reset State	Description
L3	V12	AO		OUTPUT. 1.2 V power rail. Maximum current 150 mA. 10 µF decoupling capacitor required.
M2	LX	AIO		INPUT/OUTPUT. Connection for the external DCDC Buck converter inductor.
L1	LY	AIO		INPUT/OUTPUT. Connection for the external DCDC Buck converter inductor.
J1	LZ	AIO		INPUT/OUTPUT. Connection for the external DCDC Boost converter inductor.
K1	VLED	AI		INPUT. LEDs supply voltage. 10 µF decoupling capacitor required.
M1	GND_BUCK			DCDC Buck Converter Ground.
H1	GND_BOOST			DCDC Boost Converter Ground.
H6	AVS1			Analog Ground.
H7	AVS2			Analog Ground.
H8	AVS3			Analog Ground.
C2	VSSIOOQ			OQSPI Ground.
G5	VSSD1			Digital Ground.
G6	VSSD2			Digital Ground.
F6	VSSD3			Digital Ground.
F5	VSSD4			Digital Ground.
G7	VSSD5			Digital Ground.

Note 1 Data input only. MOSI in SPI slave mode, MISO in SPI master mode.

Note 2 Data output only. MISO in SPI slave mode, MOSI in SPI master mode.

Note 3 This pin can only be used as a GPIO in 1.8 V voltage level since it is a QSPI type of pad.

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4 Specifications

All MIN/MAX specification limits are guaranteed by design, production testing and/or statistical characterization. Typical values are based on characterization results at default measurement conditions and are informative only. Default measurement conditions (unless otherwise specified): VBAT = 3.6 V, T_A = 25 ˚C. MIN and MAX values are based on characterization results over the temperature range, unless otherwise specified. All radio measurements are performed with standard RF measurement equipment providing a source/load impedance of 50 Ω.

The specified MIN and MAX capacitor values define the range of the effective capacitance, which may vary over the applied voltage due to voltage derating. Refer to the component manufacturer for the capacitor specifications.

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4.1 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
$V_{PIN\_LIM\_DEF}$	Limiting voltage on a pin	Except VBUS, VBAT, VSYS and VLED pins	-0.1	3.6	V
V_{BAT_LIM}	Limiting battery supply voltage	Pin VBAT	0	6	V
V_{BUS_LIM}	Limiting bus supply voltage	Pin VBUS	0	6.5	V
t_{R_SUP}	Power supply rise time			30	ms
$V_{PIN\_LIM\_3V0}$	Limiting voltage on a pin	3.0 V I/O pins	0	3.45	V
$V_{PIN\_LIM\_1V8}$	Limiting voltage on a pin	1.8 V I/O pins	0	1.98	V
$V_{ESD\_HBM\_BGA142}$	Electrostatic discharge voltage (Human Body Model)			2200	V
$V_{ESD\_CDM\_BGA142}$	Electrostatic discharge voltage (Charged Device Model)			500	V
T_{STG}	Storage temperature		-50	150	°C

4.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{BUS}	Bus supply voltage	Pin VBUS	4.2		5.75	V
V_{BAT}	Battery supply voltage	Pin VBAT	2.9		4.75	V
$V_{BAT\_OTP(Program)}$	Battery supply voltage	Voltage range for OTP programming. Required temperature for programming is between -20 °C and 85 °C	2.9		4.75	V
V_{PIN_3V0}	Voltage on a pin	3.0 V I/O pins	0		3.3	V
V_{PIN_1V8}	Voltage on a pin	1.8 V I/O pins	0		1.8	V
C_{L_VBAT}	Effective load capacitance		2.2	10	100	µF
C_{L_USB}	Effective load capacitance		2.2	10	100	µF
C_{L_VSYS}	Effective load capacitance		10	10	100	µF
C_{L_VLED}	Effective load capacitance		9	10	11	µF
C_{L_V30}	Effective load capacitance		2.2	5	100	µF
C_{L_V12}	Effective load capacitance		9	10	11	µF
C_{L_V14}	Effective load capacitance		9	10	11	µF
C_{L_V14RF}	Effective load capacitance		9	10	11	µF

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Parameter	Description	Conditions	Min	Typ	Max	Unit
C_{L_V18}	Effective load capacitance		18	20	22	µF
C_{L_V18P}	Effective load capacitance		18	20	22	µF
C_{L_V18F}	Effective load capacitance	C_{L_V18F} < 0.1* C_{L_V18P}	0.1	0.1	2	µF
ESR_{CL_VBUS}	Equivalent series resistance		0		100	mΩ
ESR_{CL_VBAT}	Equivalent series resistance		0		100	mΩ
ESR_{CL_VSYS}	Equivalent series resistance		0		100	mΩ
ESR_{CL_V12}	Equivalent series resistance		0		100	mΩ
ESR_{CL_V14}	Equivalent series resistance		0		100	mΩ
ESR_{CL_V18}	Equivalent series resistance		0		100	mΩ
ESR_{CL_V18p}	Equivalent series resistance		0		100	mΩ
$L_{\_BOOST}$	External Inductor			1		µH
ESR_{L_BOOST}	External Inductor ESR				0.15	Ω
I_{LBOOST_SAT}	External Inductor Saturation Current		1			A
T_A	Ambient temperature	Note 1	-40		85	°C
$I_{L\_V30\_BOOTING}$	Maximum external DC load current on V30 rail during booting/wake up from hibernation	Booting/wake-up from hibernation			500	µA

Note 1 High power dissipation cases (high charging current, high external load on VSYS) in combination with small application PCB design (high R_{TH}) during high T_{AMB} can result in activation of the die-temp protection circuit with subsequent prolonged charging times. Charger and/or LDO_VSYS will automatically go into duty cycled on/off mode to keep the die temperature within reasonable limits.

4.3 DC Characteristics

Table 5: DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{BAT_IDLE}	Battery supply current	CPU is idle (Wait for Interrupt - WFI); hclk = 32 MHz (RCHS); PLL off; slow PCLK = 2 MHz; fast PCLK = 4 MHz; DC-DC on; FLASH off; peripherals off; VDD = 0.9 V; V_{BAT} = 3 V		1.55		mA
$I_{BAT\_RUN\_32MHz}$	Average active battery supply current	CPU is executing code from RAM; hclk = 32 MHz (RCHS); PLL off; slow PCLK = 2 MHz; fast PCLK = 4 MHz; DC-DC on; FLASH off; Peripherals off; VDD = 0.9 V; V_{BAT} = 3 V.		2.7		mA

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Parameter	Description	Conditions	Min	Typ	Max	Unit
		Note 1				
$I_{BAT\_RUN\_96MHz}$	Average active battery supply current	CPU is executing code from RAM; hclk = 96 MHz (RCHS); PLL off; slow PCLK = 2 MHz; fast PCLK = 12 MHz; DC-DC on; FLASH off; Peripherals off; VDD = 1.2 V; VBAT = 3 V. Note 1		8.87		mA
$I_{BAT\_RUN\_160MHz}$	Average active battery supply current	CPU is executing code from RAM; hclk = 160 MHz; PLL on; XTAL32M on; slow PCLK = 2 MHz; fast PCLK = 20 MHz; DC-DC on; FLASH off; Peripherals off; VDD = 1.2 V; VBAT = 3 V. Note 1		13.77		mA
I_{BAT_HIBERN}	Battery supply current	Hibernation mode; no RAM retained; all clocks off; DCDC off; Vclamp default values; FLASH off; V_{BAT} = 3 V.		0.4		µA
$I_{BAT\_DP\_SLP}$	Battery supply current	Deep Sleep mode; No RAM retained; RCX on; RTC on; RCLP = 32 kHz; DC-DC on; VDD = 0.9 V; LDO_V30_RET on; Default Bandgap Refresh value; V_{BAT} = 3 V.		16.9		µA
I_{BAT_VAD}	Battery supply current	Voice Activity Detection Sleep mode; 8 kB iCache and 256 kB (data) RAM retained; RCX on; RTC on; RCLP = 32 kHz; DC-DC on; VDD = 0.9 V; LDO_V30_RET on; FLASH in Power Down mode; Default Bandgap Refresh value; V_{BAT} = 3 V.		25.9		µA
$I_{BAT\_EX\_SLP\_caches\_256K}$	Battery supply current	Extended Sleep mode; 8kB iCache and 256 kB (data) RAM retained; RCX on; RTC on; RCLP = 32 kHz; DC-DC on; VDD = 0.9 V; LDO_V30_RET on; FLASH in Power Down mode; Default Bandgap Refresh value; V_{BAT} = 3 V.		19.7		µA
$I_{BAT\_EX\_SLP\_caches\_512K}$	Battery supply current	Extended Sleep mode; 8kB iCache and 512 kB (data) RAM retained; RCX on; RTC on; RCLP = 32 kHz; DCDC on; VDD = 0.9 V; LDO_V30_RET on; FLASH in Power Down mode;		22.5		µA

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Parameter	Description	Conditions	Min	Typ	Max	Unit
		Default Bandgap Refresh value; V_{BAT} = 3 V.				
$I_{BAT\_EX\_SLP\_caches\_1MB}$	Battery supply current	Extended Sleep mode; 8kB iCache and 1024 kB (data) RAM retained; RCX on; RTC on; RCLP = 32 kHz; DCDC on; VDD = 0.9 V; LDO_V30_RET on; FLASH in Power Down mode; Default Bandgap Refresh value; V_{BAT} = 3 V.		27.9		µA
$I_{BAT\_EX\_SLP\_caches\_1.5MB}$	Battery supply current	Extended Sleep mode; 8kB iCache and 1536 kB (data) RAM retained; RCX on; RTC on; RCLP = 32 kHz; DCDC on; VDD = 0.9 V; LDO_V30_RET on; FLASH in Power Down mode; Default Bandgap Refresh value; V_{BAT} = 3 V.		33.2		µA
$I_{BAT\_SensorNode}$	Average battery supply current	Sensor Node is running code from RAM; hclk = 32 MHz (RCHS); slow PCLK = 32 MHz; fast PCLK = 4 MHz; DC-DC on; CPU off; FLASH off; Peripherals off; VDD = 0.9 V; V_{BAT}= 3 V. Note 2		2.05		mA
$I_{BAT\_BLE\_RX\_32M}$	Peak battery supply current	BLE receive mode; f_{CLK} = 32 MHz; CPU off; DC-DC on; FLASH in Power Down mode; V_{BAT}= 3 V.		4.6		mA
$I_{BAT\_BLE\_TX\_32M}$	Peak battery supply current	BLE transmit mode; f_{CLK} = 32 MHz; CPU off; DC-DC on; FLASH in Power Down mode; V_{BAT} = 3 V.		5.71		mA

Note 1 CPU is running continuously a loop performing read/modify/write on RAM data.

Note 2 Sensor Node is running continuously a loop performing SPI writes of 16 Bytes and SPI reads of 128 Bytes.

4.4 Timing Characteristics

Table 6: Timing Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{STA_SLOW}	Wake-up time	Time from wake-up trigger to application execution start.All rails restored. RCLP@512kHz. VDD during sleep is 0.9 V.			75	µs

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Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{STA_FAST}	Wake-up time	Time from wake-up trigger to application execution start. VDD should be 1.2 during sleep to avoid ramping up the voltage when waking up.		10	15	µs
t_{STA_BOOT}	Power-up time	BootROM code execution time without authentication Note 1		9	220	ms
t_{CLF_FLA}	Cache line fetch time	From QSPI FLASH; line size = 8 B; QSPI FLASH clock = sys_clk (for example, 96 MHz)			43	clock

Note 1 The boot time with authentication enabled is given by the following equation: TSTA_BOOT_SEC(ms) = 33 + STX_Timeout + 7*Image_Size(kB)/100, where STX_Timeout is the UART timeout time.

4.5 Thermal Characteristics

Table 7: Thermal Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$R_{TH\_J\text{-}A\_jPCB}$	Device thermal resistance junction to ambient	VFBGA142 package; JEDEC standard PCB; Zero number of thermal vias		25.67		°C/W

4.6 Reset Characteristics

Table 8: Reset PAD - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage	V_{12} = 0.9 V	0.63			V
V_{IL}	LOW level input voltage	V_{12} = 0.9 V			0.27	V

Table 9: Reset PAD - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{IL\_PU\_RSTN}$	LOW level input current with pull-up	V_I=V_{SS} = 0 V, V_{12} = 0.9 V	-50		-22	µA

4.7 Brown-Out Detector Characteristics

Table 10: Brown-out Detector - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{TH\_VBUS\_PLUGIN\_HL}$	High threshold voltage, low to high transition			2.5		V

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Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{TH\_VBUS\_PLUGIN\_LH}$	High threshold voltage, low to high transition			2.5		V
$V_{TH\_VBUS\_ABOVE\_VSYS}$	Comparator determines if VBUS is above VSYS		0.005	0.05	0.085	V
$V_{TH\_VBUS\_OK\_LH}$	Low threshold voltage, low to high transition		3.98	4.075	4.15	V
$V_{TH\_VBUS\_OK\_HL}$	Low threshold voltage, high to low transition		3.3	3.4	3.5	V
$V_{TH\_VBAT\_OK\_HL}$	Threshold voltage Vbat_ok comparator		2.64	2.7	2.76	V
$V_{TH\_VBAT\_OK\_LH}$	Threshold voltage Vbat_ok comparator		2.64	2.7	2.76	V
$V_{TH\_VSYS\_MODE\_0\_HL}$	Threshold voltage Vsys_ok comparator		4.15	4.25	4.35	V
$V_{TH\_VSYS\_MODE\_0\_LH}$	Threshold voltage Vsys_ok comparator		4.15	4.25	4.35	V
$V_{TH\_VSYS\_MODE\_1\_HL}$	Threshold voltage Vsys_ok comparator		4.4	4.5	4.6	V
$V_{TH\_VSYS\_MODE\_1\_LH}$	Threshold voltage Vsys_ok comparator		4.4	4.5	4.6	V
$V_{TH\_VSYS\_MODE\_2\_HL}$	Threshold voltage Vsys_ok comparator		4.65	4.75	4.85	V
$V_{TH\_VSYS\_MODE\_2\_LH}$	Threshold voltage Vsys_ok comparator		4.65	4.75	4.85	V
$V_{TH\_VSYS\_OK\_HL}$	Threshold voltage Vsys_ok comparator		2.4	2.45	2.5	V
$V_{TH\_VSYS\_OK\_LH}$	Threshold voltage Vsys_ok comparator		2.4	2.45	2.5	V
$V_{RST\_VDD\_sleep\_HL}$	Reset voltage	V12_LEVEL = 0	0.62	0.67	0.715	V
$V_{RST\_VDD\_sleep\_LH}$	Reset voltage	V12_LEVEL = 0	0.64	0.67	0.715	V
$V_{RST\_VDD\_0V9\_HL}$	Reset voltage	V12_LEVEL = 1	0.72	0.75	0.78	V
$V_{RST\_VDD\_0V9\_LH}$	Reset voltage	V12_LEVEL = 1	0.72	0.75	0.78	V
$V_{RST\_VDD\_1V2\_HL}$	Reset voltage	V12_LEVEL = 2	1.02	1.05	1.08	V
$V_{RST\_VDD\_1V2\_LH}$	Reset voltage	V12_LEVEL = 2	1.02	1.05	1.08	V

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Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{RST\_V14\_0\_HL}$	Reset voltage	V14_LEVEL = 0	1.01	1.05	1.09	V
$V_{RST\_V14\_0\_LH}$	Reset voltage	V14_LEVEL = 0	1.01	1.05	1.09	V
$V_{RST\_V14\_1\_HL}$	Reset voltage	V14_LEVEL = 1	1.11	1.15	1.19	V
$V_{RST\_V14\_1\_LH}$	Reset voltage	V14_LEVEL = 1	1.11	1.15	1.19	V
$V_{RST\_V14\_2\_HL}$	Reset voltage	V14_LEVEL = 2	1.21	1.25	1.29	V
$V_{RST\_V14\_2\_LH}$	Reset voltage	V14_LEVEL = 2	1.21	1.25	1.29	V
$V_{RST\_V14\_3\_HL}$	Reset voltage	V14_LEVEL = 3	1.305	1.35	1.395	V
$V_{RST\_V14\_3\_LH}$	Reset voltage	V14_LEVEL = 3	1.305	1.35	1.395	V
$V_{RST\_V18P\_HL}$	Reset voltage		1.61	1.65	1.69	V
$V_{RST\_V18P\_LH}$	Reset voltage		1.61	1.65	1.69	V
$V_{RST\_V18F\_HL}$	Reset voltage		1.61	1.65	1.69	V
$V_{RST\_V18F\_LH}$	Reset voltage		1.61	1.65	1.69	V
$V_{RST\_V18\_0\_HL}$	Reset voltage	V18_LEVEL = 0	1.01	1.05	1.09	V
$V_{RST\_V18\_0\_LH}$	Reset voltage	V18_LEVEL = 0	1.01	1.05	1.09	V
$V_{RST\_V18\_1\_HL}$	Reset voltage	V18_LEVEL = 1	1.6	1.65	1.7	V
$V_{RST\_V18\_1\_LH}$	Reset voltage	V18_LEVEL = 1	1.6	1.65	1.7	V

4.8 General Purpose ADC Characteristics

Table 11: GP-ADC - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Differential						
INL_{DIF}	Integral non-linearity	Differential Note 1	-2		2	LSB
DNL_{DIF}	Differential non-linearity	Differential	-2		2	LSB

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Parameter	Description	Conditions	Min	Typ	Max	Unit
E_{G_DIF}	Gain error	Differential, no chopping, trimmed bandgap	-1		4	%
E_{OFS_DIF}	Offset error	Differential, no chopping, trimmed bandgap	-30		30	LSB
$E_{G\_DIF\_COR}$	Gain error after correction	Differential, chopping, trimmed bandgap, and software correction applied	-1		1.3	%
$E_{OFS\_DIF\_COR}$	Offset error after correction	Differential, chopping, trimmed bandgap, and software correction applied	-4		4	LSB
$E_{G\_DIF\_ATTN}$	WC gain error of the attenuator	Attenuator in combination with the GPIO only, excludes errors from the ADC		0.83		%
Single-Ended						
INL_{SE}	Integral non-linearity	Single-Ended Note 1	-2		2	LSB
DNL_{SE}	Differential non-linearity	Single-Ended	-2		2	LSB
E_{G_SE}	Gain error	Single-Ended, no chopping, trimmed bandgap	-2		3	%
E_{OFS_SE}	Offset error	Single-Ended, no chopping, trimmed bandgap	-35		25	LSB
$E_{G\_SE\_COR}$	Gain error after correction	Single-Ended, chopping, trimmed bandgap, and software correction applied	-1		1	%
$E_{OFS\_SE\_COR}$	Offset error after correction	Single-Ended, chopping, trimmed bandgap, and software correction applied	-4		7	LSB
$E_{G\_SE\_ATTN}$	WC gain error of the attenuator	Attenuator in combination with the GPIO only, excludes errors from the ADC		0.83		%

Note 1 INL is the deviation of a code from a straight line passing through the actual endpoints of the transfer curve.

Table 12: GP-ADC - AC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Differential						
$ENOB_{DIF\_AVG1}$	Effective number of bits	Differential, no averaging, no chopping, $V_{IN,PP}$ = 1680 mV		9		bits
$ENOB_{DIF\_AVG128}$	Effective number of bits	Differential, 128x averaging, chopping, $V_{IN,PP}$ = 1680 mV		11		bits

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Parameter	Description	Conditions	Min	Typ	Max	Unit
Single-Ended						
$ENOB_{SE\_AVG1}$	Effective number of bits	Single-Ended, no averaging, no chopping, $V_{IN,PP}$ = 840 mV		9		bits
$ENOB_{SE\_AVG128}$	Effective number of bits	Single-Ended, 128x averaging, chopping, $V_{IN,PP}$ = 840 mV		11		bits

Table 13: GP-ADC - Electrical performance

Parameter	Description	Conditions	Min	Typ	Max	Unit
Overview						
N_{BIT_ADC}	Number of bits (resolution)			10		bit

4.9 Application ADC Characteristics

Table 14: Application ADC - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_s	Output sample rate	OSR = 125x (fixed)		16		kHz
$V_{IN\_FS\_DIF}$	Differential full-scale input voltage (peak-to-peak)	ACL is Closed Loop Gain		2*VREF/ACL		V
$V_{IN\_FS\_SE}$	Single-Ended full-scale input voltage (peak-to-peak)	ACL is Closed Loop Gain		VREF/ACL		V
V_{IN_CM}	Common mode input voltage	Internally generated		600		mV

Table 15: Application ADC - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{SUP_VBAT}	Supply current	T = 25 °C, DCDC enabled, VBAT = 3.0 V		300		µA
V_{REF}	Reference voltage			1.2		V

Table 16: Application ADC - AC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$PSRR_{DIF}$	Power supply rejection ratio	V30, A_{CL} = 0 dB, 20 Hz <= fdist <= 8 kHz	60			dB
$PSRR_{SE}$	Power supply rejection ratio	V30, A_{CL} = 0 dB, 20 Hz <= fdist <= 8 kHz	60			dB

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Parameter	Description	Conditions	Min	Typ	Max	Unit
Z_I	Input impedance	Differential mode, A_{CL} = 0 dB to +30 dB		10		kΩ

Table 17: Application ADC - External Electrical Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
N_{BIT}	Number of bits output word			16		bits

Table 18: Application ADC - Electrical Performance

Parameter	Description	Conditions	Min	Typ	Max	Unit
A_{DROOP}	Passband droop	A_{CL} = 0dB, 20 Hz <= freq <= 7 kHz (decimation filter f_{cutoff} is at 7 kHz)	0.38		0.4	dB
A_{CL_min}	Closed loop gain	PGA_GAIN = 0x0 (-12 dB) f_{signal} = 1 kHz		-12		dB
A_{CL_max}	Closed loop gain	PGA_GAIN = 0x7 (+30 dB) f_{signal} = 1 kHz		30		dB
A_{STP}	Gain step	f_{signal} = 1 kHz	5.8	6	6.2	dB
SINAD_DIF	Signal-to-noise and distortion ratio in Differential mode	f_{signal} = 1 kHz, A_{CL} = 0 dB, V_{IN} = -1 dBFS	69			dB
SINAD_SE	Signal-to-noise and distortion ratio in Single-Ended mode	f_{signal} = 1 kHz, A_{CL} = 0 dB, V_{IN} = -1 dBFS	66			dB
SNR_DIF	Signal to noise ratio in Differential mode	f_{signal} = 1 kHz, A_{CL} = 0 dB, V_{IN} = -1 dBFS	70			dB
SNR_SE	Signal to noise ratio in Single-Ended mode	f_{signal} = 1 kHz, A_{CL} = 0 dB, V_{IN} = -1 dBFS	66			dB
THD_DIF	Total harmonic distortion in Differential mode	f_{signal} = 1 kHz, A_{CL} = 0 dB, V_{IN} = -1 dBFS			-73	dB
THD_SE	Total harmonic distortion in Single-Ended mode	f_{signal} = 1 kHz, A_{CL} = 0 dB, V_{IN} = -1 dBFS			-72	dB
SFDR_DIF	Spurious-free dynamic range in Differential mode	f_{signal} = 1 kHz, A_{CL} = 0 dB, V_{IN} = -1 dBFS	70			dBFS
SFDR_SE	Spurious-free dynamic range in Single-Ended mode	f_{signal} = 1 kHz, A_{CL} = 0 dB, V_{IN} = -1 dBFS	70			dBFS
V_{IN_OFS}	Input offset voltage	f_{signal} = 1 kHz, A_{CL} = 0 dB, V_{IN} = -1 dBFS	-4	0	4	mV

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4.10 DC-DC Converter Characteristics

Table 19: DCDC - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage		2.5		4.8	V
$I_{L\_1V2\_0}$	Load Current	VDD_LEVEL = 0			75	mA
$I_{L\_1V2\_1}$	Load Current	VDD_LEVEL = 1			100	mA
$I_{L\_1V2\_2}$	Load Current	VDD_LEVEL = 2			100	mA
I_{L_1V4}	Load Current				20	mA
I_{L_1V8}	Load Current				100	mA
I_{L_1V8P}	Load Current				100	mA

Table 20: DCDC - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_Q	Quiescent Current	No load, room temperature			1	µA
$V_{O\_1V2\_0}$	VDD1V2 Output Voltage	VDD_LEVEL = 0	0.7	0.75	0.8	V
$V_{O\_1V2\_1}$	VDD1V2 Output Voltage	VDD_LEVEL = 1	0.85	0.9	1	V
$V_{O\_1V2\_2}$	VDD1V2 Output Voltage	VDD_LEVEL = 2	1.15	1.2	1.25	V
$V_{O\_1V4\_0}$	VDD1V4 Output Voltage	V14_LEVEL = 0	1.15	1.2	1.25	V
$V_{O\_1V4\_1}$	VDD1V4 Output Voltage	V14_LEVEL = 1	1.25	1.3	1.35	V
$V_{O\_1V4\_2}$	VDD1V4 Output Voltage	V14_LEVEL = 2	1.35	1.4	1.45	V
$V_{O\_1V4\_3}$	VDD1V4 Output Voltage	V14_LEVEL = 3	1.45	1.5	1.55	V
$V_{O\_1V8\_0}$	VDD1V8 Output Voltage	V18_LEVEL = 0	1.15	1.2	1.25	V
$V_{O\_1V8\_1}$	VDD1V8 Output Voltage	V18 LEVEL = 1	1.75	1.8	1.85	V
V_{O_1V8P}	VDD1V8P Output Voltage		1.75	1.8	1.85	V
η_{CONV_TYP}	Conversion Efficiency	Typical use case		77		%

Table 21: DCDC - AC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{RPL_1V2}	VDD1V2 Ripple Voltage		0		100	mV
V_{RPL_1V4}	VDD1V4 Ripple Voltage		0		20	mV
V_{RPL_1V8}	VDD1V8 Ripple Voltage		0		50	mV

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Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{RPL_1V8P}	VDD1V8P Ripple Voltage		0		50	mV
$\Delta V_O/V_{O\_NEG\_1V8\_0}$	Output Voltage Undershoot	V18_LEVEL = 0 Load step on V18 only	-2.2		0	%
$\Delta V_O/V_{O\_POS\_1V8\_0}$	Output Voltage Overshoot	V18_LEVEL = 0 Load step on V18 only	0		2.2	%
$\Delta V_O/V_{O\_NEG\_1V8\_1}$	Output Voltage Undershoot	V18_LEVEL = 1 Load step on V18 only	-1.4		0	%
$\Delta V_O/V_{O\_POS\_1V8\_1}$	Output Voltage Overshoot	V18_LEVEL = 1 Load step on V18 only	0		1.4	%
$\Delta V_O/V_{O\_NEG\_1V8P}$	Output Voltage Undershoot	Load step on V18P only	-1.4		0	%
$\Delta V_O/V_{O\_POS\_1V8P}$	Output Voltage Overshoot	Load step on V18P only	0		1.4	%

4.11 Boost DC-DC Converter Characteristics

Table 22: Boost DCDC - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IN}	Input (supply) voltage of the boost converter		2.5		4.8	V
I_L	Load Current		0		150	mA
I_{L_SLEEP}	Load current	Sleep mode (duty cycled operation)			300	µA
C_{OUT}	External capacitor on VLED	Effective Capacitance at 5 V	9	10	11	µF
ESR_{CAP}	External Capacitor ESR				0.1	Ω
L	External Inductor			1		µH
ESR_L	External Inductor ESR				0.15	Ω
I_{L_SAT}	External Inductor Saturation Current		1			A

Table 23: Boost DCDC - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{Q_SLP}	Quiescent current @ 25 °C	V_{IN} = 3.4 V, no-load, booster-only, duty-cycled operation Temp = 25 °C			10	µA
I_Q	Quiescent current	V_{IN} = 3.4 V, no-load		100	120	µA

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Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{RPL_PP}	Ripple voltage	V_{IN} = 3.4 V, ESR_COUT = 20 mΩ, ILOAD = 150 mA			75	mV
$V_{RPL\_PP\_SLP}$	Ripple voltage	V_{IN} = 3.4 V, ESR_COUT = 20 mΩ, ILOAD = 300 µA			150	mV
η_{CONV}	Conversion efficiency	V_{IN} = 3.4 V, I_{LOAD} = 20 - 150 mA, Normal Mode	70			%

4.12 Clamps Characteristics

Table 24: Clamp V30 - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_O	Output voltage of clamp		1.8		3.6	V
I_{O_MAX}	Maximum output current				500	µA

Table 25: Clamp VDD - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{O\_CLAMP\_VDD}$	Output voltage of clamp		0.7		0.85	V

4.13 Vsys Generator Characteristics

Table 26: Vsys Generator - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
C_L	Effective load capacitance of Vsys rail		10		100	µF
ESR	Equivalent series resistance		1		100	mΩ
I_L	Output load current of LDO_VSYS		0		1	A

Table 27: Vsys Generator - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{LDO}	LDO output voltage (default setting)	Iload on VSYS = 1 mA	4.6	4.8	5	V

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Table 28: Vsys Generator - Electrical Performance

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{LIM\_acc\_abs}$	Current limit accuracy (abs.)	For settings < 100 mA	-20		20	mA
$I_{LIM\_acc\_rel}$	Current limit accuracy (rel.)	For settings > 100 mA	-20		20	%
I_{LIM}	Range of configurable current limit of LDO output Programmable in steps of 10 mA (nom)		0.01		1	A
R_{ON}	On resistance when LDO is in triode mode	150 mV < (VBUS-VSYS) < Ron x Iload_vsys. Iload < Icurlim setting	0		0.5	Ω

Table 29: VBAT Switch - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_Q	Quiescent current	System in sleep or Hibernation mode; Tj = 25 °C		50		nA
R_{ON}	On resistance of switch	VSYS supplied from VBAT; Iload = 1 A	0		0.3	Ω

4.14 LDOs Characteristics

Table 30: LDO V30 - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{L\_LDO\_V30}$	Load current				150	mA

Table 31: LDO V30 - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{LDO\_V30\_0}$	Output voltage in setting "0"	Vbat = 4.2 V V30 = Unloaded	2.8	3	3.15	V
$V_{LDO\_V30\_1}$	Output voltage in setting "2" or "3"	Vbat = 4.2 V V30 = Unloaded	3.05	3.3	3.47	V
REG_{LOAD}	Load regulation $(((\Delta V_O/V_O)*100\%)/\Delta I_L)$	10 mA < Iload < 150 mA	-0.03		0.03	%/mA
REG_{LINE}	Line regulation $(((\Delta V_O/V_O)*100\%)/\Delta V_I$	Vi >= (Vo + 200 mV)	-0.5		0.5	%/V
$I_{LK\_LDO\_V30}$	Clamping load current	Output pulled down by 15 % or more; VBAT = 4.2 V	150	220	420	mA

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Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{Q\_LDO\_V30}$	Quiescent current	No Load		65		µA
$V_{DROP\_V30\_MAX}$	Maximum dropout voltage	I_L = 150 mA	0		400	mV

Table 32: LDO V30 RET - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{LDO\_V30\_RET\_0}$	Output voltage in setting "0"	Vin = 4.2 V; Vout = Unloaded	2.8	3	3.2	V
$V_{LDO\_V30\_RET\_1}$	Output voltage in setting "2" or "3"	Vin = 4.2 V; Vout = Unloaded	3.1	3.3	3.56	V
$I_{Q\_LDO\_V30\_RET}$	Quiescent current	Unloaded		80		nA
REG_{LOAD}	Load regulation $(((\Delta V_O/V_O)*100\%)/\Delta I_L)$	1 mA < Iload < 10 mA	-0.07		0.07	%/mA
REG_{LINE}	Line regulation $(((\Delta V_O/V_O)*100\%)/\Delta V_I$	Vin-Vout > 450 mV Iload = (I_int+3 mA)	-0.5		0.5	%/V
V_{DROP}	Maximum dropout voltage	Iload = 10 mA			450	mV

Table 33: LDO V30 RET - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{L\_LDO\_V30\_RET}$	Load current				10	mA

4.15 Power On Reset Vsys Characteristics

Table 34: POR VSYS - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	VSYS voltage when not in reset		2.48			V
V_{IL}	VSYS voltage when not in reset				2.3	V

Table 35: POR VSYS - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{TH_HI}	High threshold voltage	Max load on Vsys during coldboot < 0.6 A	2.3	2.47	2.6	V
V_{TH_LO}	Low threshold voltage		2.3	2.43	2.56	V

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4.16 Power On Reset V30 Characteristics

Table 36: POR V30 - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	V30 voltage level when no reset		1.75			V
V_{IL}	V30 voltage level when in reset				1.6	V

Table 37: POR V30 - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{TH_HI}	High threshold voltage		1.63	1.74	1.83	V
V_{TH_LO}	Low threshold voltage		1.6	1.7	1.8	V

4.17 32 kHz Crystal Oscillator Characteristics

Table 38: XTAL32k - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{CLK_EXT}	External clock frequency	At pin 32KXTAL1/P0_3 in GPIO mode	10		100	kHz
f_{XTAL}	Crystal oscillator frequency		30	32.768	35	kHz
ESR	Equivalent series resistance				100	kΩ
C_L	Load capacitance	No external capacitors are required for a 6 pF or 7 pF crystal	6	7	9	pF
C_0	Shunt capacitance			1	2	pF
Δf_{XTAL}	Crystal frequency tolerance (including aging)	Timing accuracy is dominated by crystal accuracy. A much smaller value is preferred	-250		250	ppm
P_{DRV_MAX}	Maximum drive power	Note 1	0.1			µW

Note 1 Select a crystal that can handle a drive level of at least this specification.

Table 39: XTAL32k - Timing Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{STA_XTAL}	Crystal oscillator startup time	Time until 1000 clocks are detected	30	100	300	ms

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4.18 32 MHz Crystal Oscillator Characteristics

Table 40: XTAL32M - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{XTAL}	Crystal oscillator frequency			32		MHz
ESR	Equivalent series resistance				100	Ω
C_L	Load capacitance	No external capacitors are required	5	6	8	pF
C_0	Shunt capacitance				7	pF
Δf_{XTAL}UNT	Crystal frequency tolerance	Untrimmed; including aging and temperature drift. C_L = 6 pF Note 1	-40		40	ppm
Δf_{XTAL}	Crystal frequency tolerance	After optional trimming; including aging and temperature drift Note 2	-15		15	ppm
$P_{DRV(MAX)}$	Maximum drive power	Note 3	100			µW
$V_{CLK(EXT)}$	External clock voltage	In case of external clock source on XTAL16Mp (XTAL16Mm floating or connected to mid-level 0.6 V)		1.2		V
φ_N(EXTERNAL)	Phase noise	f_C = 50 kHz; in case of external clock source			-130	dBc/Hz

Note 1 Maximum allowed frequency tolerance for compensation by the internal varicap trimming mechanism.

Note 2 Using the internal varicaps a wide range of crystals can be trimmed to the required tolerance.

Note 3 Select a crystal which can handle a drive level of at least this specification.

Table 41: XTAL32M - Timing Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$t_{STA(XTAL)}$(fast)	Crystal oscillator startup time (fast mode)	XTAL32M_TRIM_REG.XTAL32M_BOOST_TRIM = 9 (C_0 = 1 pF)		140		µs
$t_{STA(XTAL)}$(normal)	Crystal oscillator startup time (normal mode)	XTAL32M_TRIM_REG.XTAL32M_BOOST_TRIM = 0 (C_0 = 1 pF)		350		µs

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4.19 RCX Oscillator Characteristics

Table 42: RCX - Timing Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$\Delta f_{RC}/\Delta T_{\_1}$		Temperature range from 0 °C to 60 °C, RCX_BIAS at preferred value	-150		150	ppm/deg
$\Delta f_{RC}/\Delta T_{\_2}$		Temperature range from -40 °C to 105 °C, RCX_BIAS at preferred value	-200		200	ppm/deg
$\Delta f_{RC}/\Delta V_{\_V30}$	Only relevant if Vsys < 3 V			200		ppm/V
$\Delta f_{RC}/\Delta V_{\_VDD}$				250		ppm/V
f_{RCX_RANGE}	RC oscillator frequency range		13	15	300	kHz
f_{RCX_TRIM}	RC oscillator frequency	At target fixed trim setting	13	15	17	kHz
ODC_{RCX}	Output duty cycle		45	50	55	%
t_{JIT}	Jitter				500	ns
t_{STA_RC}	RC oscillator startup time				5	ms

4.20 RCHS 64/96 MHz RC Oscillator Characteristics

Table 43: RCHS - Timing Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$f_{RC64M\_TRIMMED}$	RC64 oscillator frequency	After calibration at target frequency (for calibration see the respective section)	63.04	64	64.96	MHz
$f_{RC96M\_TRIMMED}$	RC96 oscillator frequency	After calibration at target frequency (for calibration see the respective section)	94.56	96	97.44	MHz

Table 44: RCHS - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD_ACTIVE}	Digital supply voltage		0.85		1.25	V
V_{DD_SLEEP}	Digital supply voltage in sleep mode		0.7		0.95	V
V_{SUP}	Supply voltage		2		3.45	V

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4.21 RCLP 32/512 kHz RC Oscillator Characteristics

Table 45: RCLP - Timing Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{RCLP_1}	RC oscillator frequency	At target fixed trim setting	24	32	50	kHz
f_{RCLP_2}	RC oscillator frequency	At target fixed trim setting	384	512	800	kHz

4.22 PLL 160 MHz Characteristics

Table 46: PLL 160 MHz - AC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{PLL}	Output frequency	When in lock	158	160	162	MHz

Table 47: PLL 160 MHz - Timing Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{LOCK}	Frequency settling time	200 ppm accuracy		30	100	µs

4.23 PLL 48 MHz Characteristics

Table 48: PLL 48 MHz - AC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{PLL}	Output frequency	When in lock	47	48	49	MHz

Table 49: PLL 48 MHz - Timing Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{LOCK}	Frequency settling time	200 ppm accuracy		30	100	µs

4.24 Charger Characteristics

Table 50: Charger - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DROP}	Dropout voltage (VBUS - VBAT)	Max. charge current	500			mV
I_{CHARGE_RANGE}	Range of typical programmable charge currents 5 - 80 mA: stepsize 5 mA 90 - 240 mA: stepsize 10 mA	Charger in CC-mode	5		720	mA

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Parameter	Description	Conditions	Min	Typ	Max	Unit
	270 - 720 mA: Stepsze 30 mA					
$I_{PRECHARGE\_RANGE}$	Precharge range is normal range / 10 Range of typical programmable charge currents 0.5 - 8 mA: stepsize 0.5 mA 9 - 24 mA: stepsize 1 mA 27 - 72 mA: Stepsze 3 mA	Vbat < precharge level	0.5		72	mA
$I_{CHARGE\_accuracy\_reduced\_range}$	Charge current accuracy of current from 80 mA to 360 mA with > 500 mV voltage headroom for Tdie from 0 °C to 95 °C	Charger in CC-mode	-5		5	%
$I_{CHARGE\_accuracy}$	Charge current accuracy of all typical values	Charger in CC-mode: 0 °C < Tdie < 95 °C	-10		10	%
$I_{PRECHARGE\_accuracy}$	Charge current accuracy in precharge mode	Vbat < precharge level; Iprecharge > 5 mA; 0 °C < Tdie < 95 °C	-15		15	%
$I_{PRECHARGE\_accuracy\_low}$	Charge current accuracy in precharge mode for low current settings	Vbat < precharge level, Iprecharge < 5 mA; 0 °C < Tdie < 95 °C	-15		22	%
$I_{EOCratio\_RANGE}$	Ratio [%] between EOC current and normal charge current. 6 - 20 %: stepsize 2 % (low range with CHARGER_CURRENTS_PARAMETER_REG.I_EOC_DOUBLE_RANGE = 0) 12 - 40 %: stepsize 4 % (high range with CHARGER_CURRENTS_PARAMETER_REG.I_EOC_DOUBLE_RANGE = 1)	For normal Charge current range (no pre-charge)	6		40	%
$I_{EOCratio\_RANGE1\_accuracy}$	Absolute accuracy of ratio between EOC current and normal charge current in Range1 (Setting 0 to 7 = 6 to 20 %) Bit "CHARGER_CURRENTS_PARAMETER_REG.I_EOC_DOUBLE_RANGE" = 0 x 0	For normal Charge current range (no pre-charge) 0 °C < Tdie < 95 °C	-2		2	%
$I_{EOCratio\_RANGE2\_accuracy}$	Absolute accuracy of ratio between EOC current and normal charge current in Range2 (setting 0 to 7 = 12 - 20 %) Bit "CHARGER_CURRENTS_P	For normal Charge current range (no pre-charge) 0 °C < Tdie < 95 °C	-4		4	%

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Parameter	Description	Conditions	Min	Typ	Max	Unit
	ARAMETER_REG.I_EOC_DOUBLE_RANGE" = 0 x 1					
V_{CHARGE_43}	Charge voltage setting for trimming	Forced charge current = 1 mA Temp = 25 °C	4.226	4.26	4.294	V
$V_{CHARGE\_ACCURACY}$	Charge voltage accuracy [%]	Forced charge current = 1 mA	-1.5		1.5	%
V_{CHARGE_RANGE}	Range of typical programmable charge voltages 2.8 - 3.8 V: stepsize 50 mV 3.8 - 4.6 V: stepsize 20 mV 4.6 - 4.8 V: stepsize 100 mV	Forced charge current = 1 mA	2.8		4.8	V
$V_{REPLENISH\_range}$	Replenish voltage (where charging starts again)	Range is equal to whole "Vcharge" range	2.8		4.8	V
$V_{REPLENISH\_ACC}$	Accuracy of programmable replenish voltages		-3		3	%
$V_{PRECHARGE\_range}$	Precharge voltage threshold	Range is equal to whole "Vcharge" range	2.8		4.8	V
$V_{PRE\_CHG\_ACC}$	Accuracy of programmable precharge voltages	0 °C < Tdie < 95 °C	-3		3	%
V_{OVP_RANGE}	Overvoltage Protection level 2.8 - 3.8 V: stepsize 50 mV 3.82 - 4.6 V: stepsize 20 mV 4.7 - 4.9 V: stepsize 100 mV	Range is equal to whole "Vcharge" range, added with 4.9 V	2.8		4.9	V
V_{OVP_ACC}	Accuracy of programmable OVP voltages	0 °C < Tdie < 95 °C	-2		2	%
$T_{BAT\_nr\ of\ temp\ zones}$	Temperature zones according to enhanced JEITA standard	HOT, WARMER, WARM, NORMAL, COOL, COOLER, COLD		7		°C
$T_{BAT\_nr\ of\ temperature\ settings}$	Nr. of battery temperature protection settings per zone	Measured with external NTC		64		°C
$T_{BAT\_accuracy}$	Battery temperature protection accuracy	External NTC has 1 % accuracy "B" = 3380 (describes non linearity of NTC)	-2		2	°C
NTC_{ratio_0}	Voltage ratio between NTC-tap and ladder-top Sens = 0.9 %/°C	Tab setting = 0; THOT comp. from 0 to 1	73.4	74.4	75.4	%
NTC_{ratio_10}	Voltage ratio between NTC-tap and ladder-top Sens = 0.95 %/°C	Tab setting = 10; THOT comp. from 0 to 1	63.7	64.7	65.7	%
NTC_{ratio_20}	Voltage ratio between NTC-tap and ladder-top	Tab setting = 20; THOT comp. from 0 to 1	53.4	54.4	55.4	%

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Parameter	Description	Conditions	Min	Typ	Max	Unit
	Sens = 1.0 %/°C					
NTC_{ratio_45}	Voltage ratio between NTC-tap and ladder-top Sens = 0.8 %/°C	Tab setting = 45; THOT comp. from 0 to 1	30.3	31.3	32.3	%
NTC_{ratio_55}	Voltage ratio between NTC-tap and ladder-top Sens = 0.6 %/°C	Tab setting = 55; THOT comp. from 0 to 1	23.5	24.5	25.5	%
NTC_{ratio_63}	Voltage ratio between NTC-tap and ladder-top Sens = 0.45 %/°C	Tab setting = 63; THOT comp. from 0 to 1	19	20	21	%
$T_{DIETEMP\_PROT\_RANGE}$	Programmable range of the die-temperature protection. Stepsize: 10 °C	All charge modes	80		130	°C
$T_{DIETEMP\_PROT\_accuracy}$	Accuracy of the die-temperature protection	All charge modes	-13		13	°C

4.25 Battery Check Characteristics

Table 51: Battery Check - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{ACC\_BATCHECK}$	Current accurac. For load current = 1 mA, spec is reduced to +/- 7.5 %	Battery Check, Load current (BATCHECK_ILOAD + 1)mA	-5		5	%

4.26 Digital I/O Characteristics

Table 52: PAD I/O LowDrive - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage	V_{18P} = 1.8 V	1.26			V
V_{IL}	LOW level input voltage	V_{18P} = 1.8 V			0.54	V

Table 53: PAD I/O LowDrive - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH level input current	V_I=V_{30} = 3.0 V	-0.3		0.3	µA
I_{IL}	LOW level input current	V_I=V_{SS} = 0 V	-0.3		0.3	µA
I_{IH_PD}	HIGH level input current	V_I=V_{30} = 3.0 V	60		180	µA
$I_{IL\_PU\_3V0}$	LOW level input current	V_I=V_{SS} = 0 V, V_{30} = 3.0 V	-180		-60	µA
$I_{IL\_PU\_1V8}$	LOW level input current	V_I=V_{SS}= 0 V, V_{18P} = 1.8 V	-110		-35	µA

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Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{OH\_1V8\_LOW\ DRV}$	HIGH level output voltage, limited drive	I_O = 150 uA, V_{18P} = 1.8 V, low drive enabled	1.44			V
$V_{OL\_1V8\_LOW\ DRV}$	LOW level output voltage, limited drive	I_O = 150 uA, V_{18P} = 1.8 V, low drive enabled			0.36	V
V_{OH_1V8}	HIGH level output voltage	I_O = 4.8 mA, V_{18P} = 1.8 V	1.44			V
V_{OL_1V8}	LOW level output voltage	I_O = 4.8 mA, V_{18P} = 1.8 V			0.36	V
V_{OH_3V0}	HIGH level output voltage	I_O = 4.8 mA, V_{30} = 2.0 V	1.6			V
V_{OL_3V0}	LOW level output voltage	I_O = 4.8 mA, V_{30} = 2.0 V			0.4	V
SR_R	Rising slew rate	C_L = 15 pF; I_L = 4.8 mA	0.4		3.2	V/ns
SR_F	Falling slew rate	C_L = 15 pF; I_L = 4.8 mA	0.4		3.3	V/ns
C_{IN}	Input capacitance			0.75		pF

Table 54: PAD I/O Wake-up - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage	V_{12} = 0.9 V	0.63			V
V_{IL}	LOW level input voltage	V_{12} = 0.9 V			0.27	V

Table 55: PAD I/O Wake-up - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH level input current	V_I=V_{30} = 3.0 V	-0.3		0.3	µA
I_{IL}	LOW level input current	V_I=V_{SS} = 0 V	-0.3		0.3	µA
I_{IH_PD}	HIGH level input current	V_I=V_{30} = 3.0 V	60		180	µA
$I_{IL\_PU\_3V0}$	LOW level input current	V_I=V_{SS} = 0 V, V_{30} = 3.0 V	-180		-60	µA
$I_{IL\_PU\_1V8}$	LOW level input current	V_I=V_{SS}= 0 V, V_{18P} = 1.8 V	-110		-35	µA
$V_{OH\_1V8\_LOW\ DRV}$	HIGH level output voltage, limited drive	I_O = 150 uA, V_{18P} = 1.8 V, low drive enabled	1.44			V
$V_{OL\_1V8\_LOW\ DRV}$	LOW level output voltage, limited drive	I_O = 150 uA, V_{18P} = 1.8 V, low drive enabled			0.36	V
V_{OH_1V8}	HIGH level output voltage	I_O = 4.8 mA, V_{18P} = 1.8 V	1.44			V
V_{OL_1V8}	LOW level output voltage	I_O = 4.8 mA, V_{18P} = 1.8 V			0.36	V
V_{OH_3V0}	HIGH level output voltage	I_O = 4.8 mA, V_{30} = 2.0 V	1.6			V
V_{OL_3V0}	LOW level output voltage	I_O = 4.8 mA, V_{30} = 2.0 V			0.4	V
SR_R	Rising slew rate	C_L = 15 pF; I_L = 4.8 mA	0.4		3.2	V/ns
SR_F	Falling slew rate	C_L = 15 pF; I_L = 4.8 mA	0.4		3.3	V/ns

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Parameter	Description	Conditions	Min	Typ	Max	Unit
C_{IN}	Input capacitance			0.75		pF

Table 56: PAD I/O Display SPI - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage	V_{18P} = 1.8 V	1.26			V
V_{IL}	LOW level input voltage	V_{18P} = 1.8 V			0.54	V

Table 57: PAD I/O Display SPI - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH level input current	V_I=V_{30} = 3.0 V	-0.3		0.3	µA
I_{IL}	LOW level input current	V_I=V_{SS} = 0 V	-0.3		0.3	µA
I_{IH_PD}	HIGH level input current	V_I=V_{30} = 3.0 V	60		180	µA
$I_{IL\_PU\_3V0}$	LOW level input current	V_I=V_{SS} = 0 V, V_{30} = 3.0 V	-180		-60	µA
$I_{IL\_PU\_1V8}$	LOW level input current	V_I=V_{SS} = 0 V, V_{18P} = 1.8 V	-110		-35	µA
$V_{OH\_1V8\_LOW\ DRV}$	HIGH level output voltage, limited drive	I_O = 150 uA, V_{18P} = 1.8 V, low drive enabled	1.44			V
$V_{OL\_1V8\_LOW\ DRV}$	LOW level output voltage, limited drive	I_O = 150 uA, V_{18P} = 1.8 V, low drive enabled			0.36	V
V_{OH_1V8}	HIGH level output voltage	I_O = 4.8 mA, V_{18P}= 1.8 V	1.44			V
V_{OL_1V8}	LOW level output voltage	I_O = 4.8 mA, V_{18P} = 1.8 V			0.36	V
V_{OH_3V0}	HIGH level output voltage	I_O = 4.8 mA, V_{30} = 2.0 V	1.6			V
V_{OL_3V0}	LOW level output voltage	I_O = 4.8 mA, V_{30} = 2.0 V			0.4	V
SR_R	Rising slew rate	C_L = 20 pF; I_L = 4.8 mA	0.5		2.4	V/ns
SR_F	Falling slew rate	C_L = 20 pF; I_L = 4.8 mA	0.5		2.3	V/ns
C_{IN}	Input capacitance			0.75		pF

4.27 Quad SPI I/O Characteristics

Table 58: PAD OQSPIF - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage	V_{18F} = 1.8 V	1.26			V
V_{IL}	LOW level input voltage	V_{18F} = 1.8 V			0.54	V

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Table 59: PAD OQSPIF - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OH_4mA}	HIGH level output voltage	I_O = 4 mA, V_{18F} = 1.8 V	1.44			V
V_{OH_8mA}	HIGH level output voltage	I_O = 8 mA, V_{18F} = 1.8 V	1.44			V
V_{OH_12mA}	HIGH level output voltage	I_O = 12 mA, V_{18F} = 1.8 V	1.44			V
V_{OH_16mA}	HIGH level output voltage	I_O = 16 mA, V_{18F} = 1.8 V	1.44			V
V_{OL_4mA}	LOW level output voltage	I_O = 4 mA, V_{18F} = 1.8 V			0.36	V
V_{OL_8mA}	LOW level output voltage	I_O = 8 mA, V_{18F} = 1.8 V			0.36	V
V_{OL_12mA}	LOW level output voltage	I_O = 12 mA, V_{18F} = 1.8 V			0.36	V
V_{OL_16mA}	LOW level output voltage	I_O = 16 mA, V_{18F} = 1.8 V			0.36	V
I_{IH}	HIGH level input current	V_I=V_{18F} = 1.8 V	-0.3		0.3	µA
I_{IL}	LOW level input current	V_I=V_{SS}, V_{18F} = 1.8 V	-0.3		0.3	µA
I_{IH_PD}	HIGH level input current with pull-down	V_I=V_{18F}, V_{18F} = 1.8 V	25		75	µA
I_{IL_PU}	LOW level input current with pull-up	V_I=V_{SS}, V_{18F} = 1.8 V	-75		-25	µA
SR_{R_0}	Rising slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x0		1.7		V/ns
SR_{R_1}	Rising slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x1		2		V/ns
SR_{R_2}	Rising slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x2		2.3		V/ns
SR_{R_3}	Rising slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x3		2.4		V/ns
SR_{F_0}	Falling slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x0		1.9		V/ns
SR_{F_1}	Falling slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x1		2.3		V/ns
SR_{F_2}	Falling slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x2		2.6		V/ns
SR_{F_3}	Falling slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x3		2.7		V/ns
C_{IN}	Input capacitance			0.87		pF

Table 60: PAD QSPIC/QSPIC2 - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage	V_{18P} = 1.8 V	1.26			V

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Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW level input voltage	V_{18P} = 1.8 V			0.54	V

Table 61: PAD QSPIC/QSPIC2 - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OH_4mA}	HIGH level output voltage	I_O = 4 mA, V_{18P} = 1.8 V	1.44			V
V_{OH_8mA}	HIGH level output voltage	I_O = 8 mA, V_{18P} = 1.8 V	1.44			V
V_{OH_12mA}	HIGH level output voltage	I_O = 12 mA, V_{18P} = 1.8 V	1.44			V
V_{OH_16mA}	HIGH level output voltage	I_O = 16 mA, V_{18P} = 1.8 V	1.44			V
V_{OL_4mA}	LOW level output voltage	I_O = 4 mA, V_{18P} = 1.8 V			0.36	V
V_{OL_8mA}	LOW level output voltage	I_O = 8 mA, V_{18P} = 1.8 V			0.36	V
V_{OL_12mA}	LOW level output voltage	I_O = 12 mA, V_{18P} = 1.8 V			0.36	V
V_{OL_16mA}	LOW level output voltage	I_O = 16 mA, V_{18P} = 1.8 V			0.36	V
I_{IH}	HIGH level input current	V_I=V_{18P} = 1.8 V	-0.3		0.3	µA
I_{IL}	LOW level input current	V_I=V_{SS}, V_{18P} = 1.8 V	-0.3		0.3	µA
I_{IH_PD}	HIGH level input current with pull-down	V_I=V_{18P} = 1.8 V	25		75	µA
I_{IL_PU}	LOW level input current with pull-up	V_I=V_{SS}, V_{18P} = 1.8 V	-75		-25	µA
SR_{R_0}	Rising slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x0		1.7		V/ns
SR_{R_1}	Rising slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x1		2		V/ns
SR_{R_2}	Rising slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x2		2.3		V/ns
SR_{R_3}	Rising slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x3		2.4		V/ns
SR_{F_0}	Falling slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x0		1.9		V/ns
SR_{F_1}	Falling slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x1		2.3		V/ns
SR_{F_2}	Falling slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x2		2.6		V/ns
SR_{F_3}	Falling slew rate	QSPIC_GP_REG[QSPIC_PADS_SLEW] = 0x3		2.7		V/ns
C_{IN}	Input capacitance			0.87		pF

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4.28 LED Characteristics

Table 62: LED - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{OFF_LED}	Off-state current	Driver disabled	-0.2		0.2	µA
$I_{O\_MAX\_LED}$	Maximum sink current	PWM 100 %, V_{LED} = 500 mV; full temp range	18		22	mA
$I_{O\_MAX\_LED\_RT}$	Maximum sink current	PWM 100 %, V_{LED} = 500 mV; 25 °C	19		21	mA
$I_{MATCH\_UPTO\_5mA}$	Relative matching; difference from the average of 3 outputs	PWM 100 %, load select 2.5 mA	-7.5		7.5	%
$I_{MATCH\_5mA\_TO\_10mA}$	Relative matching; difference from the average of 3 outputs	PWM 100 %, load select 5 mA to 10 mA	-5		5	%
$I_{MATCH\_10mA\_TO\_20mA}$	Relative matching; difference from the average of 3 outputs	PWM 100 %, load select 10 mA to 20 mA	-5		5	%
V_{SAT_LED}	Saturation voltage	PWM 100 %, load select 20 mA	500			mV
$I_{ACC\_LED\_PWM}$	PWM current accuracy	PWM accuracy at 10 % duty cycle and above relative to $I_{O\_MAX\_LED}$ (100 % duty cycle), f_{PWM} = 500 Hz	-2		2	%

Table 63: LED - AC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{PWM_LED}	PWM frequency		30.5		7812.5	Hz

Table 64: LED - Programmable Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{ACC\_LED\_LOAD\_SEL[K]}$	Absolute current accuracy; 2.575 mA + (LOAD_SEL[k]*2.575 mA)	k= 0 to 7, V_{LED} = 500 mV; full temp range	-10		10	%
$I_{ACC\_LED\_LOAD\_SEL[K]\_RT}$	Absolute current accuracy; 2.575 mA + (LOAD_SEL[k]*2.575 mA)	k= 0 to 7, V_{LED} = 500 mV; 25 °C	-5		5	%

4.29 USB Characteristics

Table 65: PAD I/O USB PHY - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH level input current	V_I=V_{30} = 3.0 V	-20		20	µA

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Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{IL}	LOW level input current	V_I=V_{SS} = 0 V	-0.3		0.3	µA
I_{IH_PD}	HIGH level input current	V_I=V_{30} = 3.0 V	60		180	µA
$I_{IL\_PU\_3V0}$	LOW level input current	V_I=V_{SS} = 0 V, V_{30} = 3.0 V	-180		-60	µA
$I_{IL\_PU\_1V8}$	LOW level input current	V_I=V_{SS} = 0 V, V_{18P} = 1.8 V	-110		-35	µA
V_{OH_1V8}	HIGH level output voltage	I_O = 4.8 mA, V_{18P} = 1.8 V	1.44			V
V_{OL_1V8}	LOW level output voltage	I_O = 4.8 mA, V_{18P} = 1.8 V			0.36	V
V_{OH_3V0}	HIGH level output voltage	I_O = 4.8 mA, V_{30} = 2.0 V	1.6			V
V_{OL_3V0}	LOW level output voltage	I_O = 4.8 mA, V_{30} = 2.0 V			0.4	V
SR_R	Rising slew rate	C_L = 15 pF; I_L = 4.8 mA	0.4		3.2	V/ns
SR_F	Falling slew rate	C_L = 15 pF; I_L = 4.8 mA	0.4		3.3	V/ns
C_{IN}	Input capacitance			0.75		pF

Table 66: PAD I/O USB PHY - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage		1.26			V
V_{IL}	LOW level input voltage				0.54	V

4.30 USB Charger Detection Characteristics

Table 67: USB Charger Detection - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{IH\_CHG\_DET}$	HIGH level input voltage	CHG_DET_SW_CTRL_REG [VDP_SRC_ON] = 1	0.4			V
$V_{IL\_CHG\_DET}$	LOW level input voltage	CHG_DET_SW_CTRL_REG [VDP_SRC_ON] = 1			0.25	V
$V_{IH\_DCP\_DET}$	HIGH level input voltage	CHG_DET_SW_CTRL_REG [VDM_SRC_ON] = 1	0.4			V
$V_{IL\_DCP\_DET}$	LOW level input voltage	CHG_DET_SW_CTRL_REG [VDM_SRC_ON] = 1			0.25	V
$V_{IH\_DM\_VAL}$	HIGH level input voltage		1.5			V
$V_{IL\_DM\_VAL}$	LOW level input voltage				0.8	V
$V_{IH\_DP\_VAL}$	HIGH level input voltage		1.5			V
$V_{IL\_DP\_VAL}$	LOW level input voltage				0.8	V
$V_{IH\_DM\_VAL2}$	HIGH level input voltage		2.5			V

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Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{IL\_DM\_VAL2}$	LOW level input voltage				2.3	V
$V_{IH\_DP\_VAL2}$	HIGH level input voltage		2.5			V
$V_{IL\_DP\_VAL2}$	LOW level input voltage				2.3	V
$V_{O\_DM\_SRC}$	Output voltage	CHG_DET_SW_CTRL_REG = 0x19	0.5		0.7	V
$V_{O\_DP\_SRC}$	Output voltage	CHG_DET_SW_CTRL_REG = 0x25	0.5		0.7	V
I_{DM_SINK}	D- sink current	CHG_DET_SW_CTRL_REG = 0x25	25		175	µA
I_{DP_SINK}	D+ sink current	CHG_DET_SW_CTRL_REG = 0x19	25		175	µA
I_{DP_SRC}	D+ source current	CHG_DET_SW_CTRL_REG = 0x3	5		13	µA
R_{DM_DWN}	D- resistance to ground	CHG_DET_SW_CTRL_REG = 0x3	14.25		24.8	kΩ

4.31 Voice Activity Detection Characteristics

Table 68: VAD - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IN_MAX}	Maximum input voltage	Power Level Sensitivity set to 3 dB			280	mV
V_{IN_MIN}	Minimum detection input voltage	Power Level Sensitivity set to 3 dB			35	µV

4.32 Temperature Sensor Characteristics

Table 69: Temperature Sensor - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_{SENSE_RANGE}	Sense temperature range		-40		105	°C
$T_{SENSE\_ACC\_OTP}$	Absolute temperature sensor accuracy using OTP value	$T_{AMBIENT}$ = 25 °C	-4		4	°C

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Table 70: Temperature Sensor - Electrical Performance

Parameter	Description	Conditions	Min	Typ	Max	Unit
TC_{SENSE}	Temperature coefficient of the internal temperature sensor	Reading via GP_ADC (10 bit result)		2.6		LSB/°C

4.33 Radio Characteristics

Table 71: Radio BLE 1M - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{OPER}	Operating frequency		2400		2483.5	MHz
N_{CH}	Number of channels			40		1
f_{CH}	Channel frequency	K = 0 to 39		2402+K*2		MHz

Table 72: Radio BLE 1M - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{BAT\_RF\_RX}$	Battery supply current	Radio receiver and synthesizer active; ideal DC-DC converter with V_{BAT} = 3 V and V_{14RF} = 1.4 V; T_A = 25 °C Note 1		1.85		mA
$I_{BAT\_RF\_TX\_+6dBm}$	Battery supply current	Radio transmitter and synthesizer active; power setting = 15; ideal DC-DC converter with V_{BAT} = 3 V and V_{14RF} = 1.4 V; T_A = 25 °C Note 1		5.2		mA
$I_{BAT\_RF\_TX\_0dBm}$	Battery supply current	Radio transmitter and synthesizer active; power setting = 8; ideal DC-DC converter with V_{BAT} = 3 V and V_{14RF} = 1.4 V; T_A = 25 °C Note 1		3		mA
$I_{BAT\_RF\_TX\_-3dBm}$	Battery supply current	Radio transmitter and synthesizer active; power setting = 6; ideal DC-DC converter with V_{BAT} = 3 V and V_{14RF} = 1.4 V; T_A = 25 °C Note 1		2.2		mA
$I_{BAT\_RF\_TX\_-6dBm}$	Battery supply current	Radio transmitter and synthesizer active; power setting = 4; ideal DC-DC converter with V_{BAT} = 3 V and V_{14RF} = 1.4 V; T_A = 25 °C Note 1		1.9		mA

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Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{BAT\_RF\_TX\_-12dBm}$	Battery supply current	Radio transmitter and synthesizer active; power setting = 2; ideal DC-DC converter with V_{BAT} = 3 V and V_{14RF} = 1.4 V; T_A = 25 °C Note 1		1.4		mA
$I_{BAT\_RF\_TX\_-18dBm}$	Battery supply current	Radio transmitter and synthesizer active; power setting = 1; ideal DC-DC converter with V_{BAT} = 3 V and V_{14RF} = 1.4 V; T_A = 25 °C Note 1		1.1		mA

Note 1 The DC-DC converter efficiency is assumed to be 100 % to enable benchmarking of the radio currents at battery supply domain.

Table 73: Radio BLE 1M - AC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
P_{SENS_CLEAN}	Sensitivity level	Dirty Transmitter disabled; DC-DC converter disabled; PER = 30.8 %; V_{14RF} = 1.4 V Note 1		-97		dBm
P_{SENS_EPKT}	Sensitivity level	Extended packet size (255 octets)		-94.5		dBm
P_{SENS}	Sensitivity level	Normal Operating Conditions; DC-DC converter disabled; PER = 30.8 % Note 1		-96.5		dBm
P_{INT_IMD}	Intermodulation distortion interferer power level	Worst-case interferer level @ f_1, f_2 with $2*f_1 - f_2 = f_0$, $\|f_1 - f_2\|$ = n MHz and n = 3, 4, 5; P_{WANTED} = -64 dBm @ f_0; PER = 30.8 % Note 2		-28		dBm
CIR_0	Carrier to interferer ratio	n = 0; interferer @ $f_1 = f_0 + n*1$ MHz Note 3		7		dB
CIR_{M1}	Carrier to interferer ratio	n = -1; interferer @ $f_1 = f_0 + n*1$ MHz Note 3		-5		dB
CIR_{P1}	Carrier to interferer ratio	n = +1; interferer @ $f_1 = f_0 + n*1$ MHz Note 3		-3		dB
CIR_{P2}	Carrier to interferer ratio	n = +2; interferer @ $f_1 = f_0 + n*1$ MHz Note 3		-30		dB

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Parameter	Description	Conditions	Min	Typ	Max	Unit
CIR_{M2}	Carrier to interferer ratio	n = -2 (image frequency); interferer @ $f_1 = f_0 + n*1$ MHz Note 3		-37		dB
CIR_{P3}	Carrier to interferer ratio	n = +3; interferer @ $f_1 = f_0 + n*1$ MHz Note 3		-42		dB
CIR_{M3}	Carrier to interferer ratio	n = -3 (image frequency + 1 MHz); interferer @ $f_1 = f_0 + n*1$ MHz Note 3		-47		dB
CIR_{P4}	Carrier to interferer ratio	n = +4; interferer @ $f_1 = f_0 + n*1$ MHz Note 3		-48		dB
CIR_{M4}	Carrier to interferer ratio	n = -4; interferer @ $f_1 = f_0 + n*1$ MHz Note 3		-51		dB
CIR_5	Carrier to interferer ratio	$\|n\| \geq 5$ (any other BLE channel); interferer @ $f_1 = f_0 + n*1$ MHz Note 3		-52		dB
P_{BL_I}	Blocker power level	30 MHz ≤ f_{BL} ≤ 2000 MHz; P_{WANTED} = -67 dBm Note 4		5		dBm
P_{BL_II}	Blocker power level Note 5	2003 MHz ≤ f_{BL} ≤ 2399 MHz; P_{WANTED} = -67 dBm Note 4		0		dBm
P_{BL_III}	Blocker power level	2484 MHz ≤ f_{BL} ≤ 2997 MHz; P_{WANTED} = -67 dBm Note 4		0		dBm
P_{BL_IV}	Blocker power level	3000 MHz ≤ f_{BL} ≤ 12.75 GHz; P_{WANTED} = -67 dBm Note 4		5		dBm
L_{ACC_RSSI}	Level accuracy	Tolerance at 5 % to 95 % confidence interval of P_{RF}: when RXRSSI[7:0] = *X*, 50 < *X* < 175; burst mode, 1500 packets		2		dB
L_{RES_RSSI}	Level resolution	Gradient of monotonous range for RXRSSI[7:0] = *X*, 50 < *X* < 175; burst mode, 1500 packets		0.5		dB/LSB
ACP_{2M}	Adjacent channel power level	f_{OFS} = 2 MHz Note 6		-49		dBm
ACP_{3M}	Adjacent channel power level	f_{OFS} ≥ 3 MHz Note 6		-56		dBm

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Parameter	Description	Conditions	Min	Typ	Max	Unit
P_{O_15}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 15		6		dBm
P_{O_14}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 14		5		dBm
P_{O_13}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 13		4.5		dBm
P_{O_12}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 12		4		dBm
P_{O_11}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 11		3		dBm
P_{O_10}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 10		2		dBm
P_{O_09}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 9		1.5		dBm
P_{O_08}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 8		0.5		dBm
P_{O_07}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 7		-1		dBm
P_{O_06}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 6		-2		dBm
P_{O_05}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 5		-3.5		dBm
P_{O_04}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 4		-5.5		dBm
P_{O_03}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 3		-8		dBm
P_{O_02}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 2		-11.5		dBm
P_{O_01}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 1		-17.5		dBm
P_{O_01A1}	Output power level	Power set to -22 dBm		-22		dBm
P_{O_01A2}	Output power level	Power set to -26 dBm		-26		dBm
P_{O_ULP}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 0;		-51		dBm

Note 1 Measured according to Bluetooth® Low Energy Test Specification RF-PHY.TS/4.0.1, section 6.4.1.

Note 2 Measured according to Bluetooth® Core Technical Specification document, version 4.0, volume 6, section 4.4. Published value is for n = IXIT = 4. IXIT = 5 gives the same results, IXIT = 3 gives results that are 5 dB lower.

Note 3 Measured according to Bluetooth® Core Technical Specification document, version 4.0, volume 6, Section 4.2.

Note 4 Measured according to Bluetooth® Core Technical Specification document, version 4.0, volume 6, section 4.3. Due to limitations of the measurement equipment, levels of -5 dBm should be interpreted as > -5 dBm.

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Note 5 Frequencies close to the ISM band can show slightly worse performance

Note 6 Measured according to Bluetooth® Low Energy Test Specification RF-PHY.TS/4.0.1, section 6.2.3.

Table 74: Radio BLE 2M - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{OPER}	Operating frequency		2400		2483.5	MHz
N_{CH}	Number of channels			40		1
f_{CH}	Channel frequency	K = 0 to 39		2402+ K*2		MHz

Table 75: Radio BLE 2M - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{BAT\_RF\_RX}$	Battery supply current	Radio receiver and synthesizer active; ideal DC-DC converter with V_{BAT} = 3 V and V_{14RF} = 1.4 V; T_A = 25 °C Note 1		2.2		mA
$I_{BAT\_RF\_TX\_+6dBm}$	Battery supply current	Radio transmitter and synthesizer active; power setting = 15; ideal DC-DC converter with V_{BAT} = 3 V and V_{14RF} = 1.4 V; T_A = 25 °C Note 1		5.2		mA
$I_{BAT\_RF\_TX\_0dBm}$	Battery supply current	Radio transmitter and synthesizer active; power setting = 8; ideal DC-DC converter with V_{BAT} = 3 V and V_{14RF} = 1.4 V; T_A = 25 °C Note 1		3		mA
$I_{BAT\_RF\_TX\_-3dBm}$	Battery supply current	Radio transmitter and synthesizer active; power setting = 6; ideal DC-DC converter with V_{BAT} = 3 V and V_{14RF} = 1.4 V; T_A = 25 °C Note 1		2.2		mA
$I_{BAT\_RF\_TX\_-6dBm}$	Battery supply current	Radio transmitter and synthesizer active; power setting = 4; ideal DC-DC converter with V_{BAT} = 3 V and V_{14RF} = 1.4 V; T_A = 25 °C Note 1		1.9		mA
$I_{BAT\_RF\_TX\_-12dBm}$	Battery supply current	Radio transmitter and synthesizer active; power setting = 2; ideal DC-DC converter with V_{BAT} = 3 V and V_{14RF} = 1.4 V; T_A = 25 °C Note 1		1.4		mA

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Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{BAT\_RF\_TX\_-18dBm}$	Battery supply current	Radio transmitter and synthesizer active; power setting = 1; ideal DC-DC converter with V_{BAT} = 3 V and V_{14RF} = 1.4 V; T_A = 25 °C Note 1		1.1		mA

Note 1 The DC-DC converter efficiency is assumed to be 100 % to enable benchmarking of the radio currents at battery supply domain.

Table 76: Radio BLE 2M - AC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
P_{SENS_CLEAN}	Sensitivity level	Dirty Transmitter disabled; DC-DC converter disabled; PER = 30.8 %; V_{14RF} = 1.4 V Note 1		-94.5		dBm
P_{SENS_EPKT}	Sensitivity level	Extended packet size (255 octets)		-92.5		dBm
P_{SENS}	Sensitivity level	Normal Operating Conditions; DC-DC converter disabled; PER = 30.8 % Note 1		-94		dBm
P_{INT_IMD}	Intermodulation distortion interferer power level	Worst-case interferer level @ f_1, f_2 with $2*f_1 - f_2 = f_0$, $\|f_1 - f_2\|$ = n x 2 MHz and n = 3, 4, 5; P_{WANTED} = -64 dBm @ f_0; PER = 30.8 % Note 2		-27		dBm
CIR_0	Carrier to interferer ratio	n = 0; interferer @ $f_1 = f_0 + n*2$ MHz Note 3		6		dB
CIR_{P1}	Carrier to interferer ratio	n = +1; interferer @ $f_1 = f_0 + n*2$ MHz Note 3		-4		dB
CIR_{M1}	Carrier to interferer ratio	n = -1; interferer @ $f_1 = f_0 + n*2$ MHz Note 3		-4		dB
CIR_{P2}	Carrier to interferer ratio	n = +2; interferer @ $f_1 = f_0 + n*2$ MHz Note 3		-31		dB
CIR_{M2}	Carrier to interferer ratio	n = -2 (image frequency); interferer @ $f_1 = f_0 + n*2$ MHz Note 3		-36		dB
CIR_{P3}	Carrier to interferer ratio	n = +3; interferer @ $f_1 = f_0 + n*2$ MHz Note 3		-41		dB

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Parameter	Description	Conditions	Min	Typ	Max	Unit
CIR_{M3}	Carrier to interferer ratio	n = -3 (image frequency + 2 MHz); interferer @ $f_1 = f_0 + n*2$ MHz Note 3		-47		dB
CIR_{M4}	Carrier to interferer ratio	n = -4; interferer @ $f_1 = f_0 + n*2$ MHz Note 3		-47		dB
CIR_{P4}	Carrier to interferer ratio	n = +4; interferer @ $f_1 = f_0 + n*2$ MHz Note 3		-41		dB
CIR_5	Carrier to interferer ratio	|n| ≥ 5 (any other BLE channel); interferer @ $f_1 = f_0 + n*2$ MHz Note 3		-53		dB
P_{BL_I}	Blocker power level	30 MHz ≤ f_{BL} ≤ 2000 MHz; P_{WANTED} = -67 dBm Note 4		5		dBm
P_{BL_II}	Blocker power level Note 5	2003 MHz ≤ f_{BL} ≤ 2399 MHz; P_{WANTED} = -67 dBm Note 4		0		dBm
P_{BL_III}	Blocker power level	2484 MHz ≤ f_{BL} ≤ 2997 MHz; P_{WANTED} = -67 dBm Note 4		0		dBm
P_{BL_IV}	Blocker power level	3000 MHz ≤ f_{BL} ≤ 12.75 GHz; P_{WANTED} = -67 dBm Note 4		5		dBm
L_{ACC_RSSI}	Level accuracy	Tolerance at 5 % to 95 % confidence interval of P_{RF}: when RXRSSI[7:0] = *X*, 50 < *X* < 175; burst mode, 1500 packets		2		dB
L_{RES_RSSI}	Level resolution	Gradient of monotonous range for RXRSSI[7:0] = *X*, 50 < *X* < 175; burst mode, 1500 packets		0.5		dB/LSB
ACP_{4M}	Adjacent channel power level	f_{OFS} = 4 MHz Note 6		-54		dBm
ACP_{5M}	Adjacent channel power level	f_{OFS} = 5 MHz Note 6		-61		dBm
ACP_{6M}	Adjacent channel power level	f_{OFS} ≥ 6 MHz Note 6		-60		dBm
P_{O_15}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 15		6		dBm

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Parameter	Description	Conditions	Min	Typ	Max	Unit
P_{O_14}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 14		5		dBm
P_{O_13}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 13		4.5		dBm
P_{O_12}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 12		4		dBm
P_{O_11}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 11		3		dBm
P_{O_10}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 10		2		dBm
P_{O_09}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 9		1.5		dBm
P_{O_08}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 8		0.5		dBm
P_{O_07}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 7		-1		dBm
P_{O_06}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 6;		-2		dBm
P_{O_05}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 5		-3.5		dBm
P_{O_04}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 4		-5.5		dBm
P_{O_03}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 3		-8		dBm
P_{O_02}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 2		-11.5		dBm
P_{O_01}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 1		-17.5		dBm
P_{O_01A1}	Output power level	Power set to -22 dBm		-22		dBm
P_{O_01A2}	Output power level	Power set to -26 dBm		-26		dBm
P_{O_ULP}	Output power level	RF_ATTR_REG[PA_POWER_SETTING] = 0		-51		dBm

Note 1 Measured according to Bluetooth® Low Energy Test Specification RF-PHY.TS/4.0.1, section 6.4.1.

Note 2 Measured according to Bluetooth® Core Technical Specification document, version 4.0, volume 6, section 4.4. Published value is for n = IXIT = 4. IXIT = 5 gives the same results, IXIT = 3 gives results that are 5 dB lower.

Note 3 Measured according to Bluetooth® Core Technical Specification document, version 4.0, volume 6, section 4.2.

Note 4 Measured according to Bluetooth® Core Technical Specification document, version 4.0, volume 6, section 4.3. Due to limitations of the measurement equipment, levels of -5 dBm should be interpreted as > -5 dBm.

Note 5 Frequencies close to the ISM band can show slightly worse performance

Note 6 Measured according to Bluetooth® Low Energy Test Specification RF-PHY.TS/4.0.1, section 6.2.3.

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5 System Overview

5.1 Internal Blocks

The DA1470x family contains the following blocks:

Arm® Cortex®-M33 CPU: This processor provides 1.5 dMIPS/MHz (240 dMIPS when operating at the maximum clock speed of 160 MHz) and is used for the application but also implementing the upper layers of the Bluetooth® Low Energy protocol (Host). It has a powerful cache controller with four-way associativity, 8 B cache line size, and 8 kB of cache RAM. The CPU executes code from the external FLASH via the cache controller. Code in the FLASH might be encrypted; so, decryption happens while in progress without extra wait states.

Configurable MAC: This is a Configurable MAC (CMAC) based on the ARM Cortex-M0+ CPU and hardware accelerators implementing all timing critical tasks of the Bluetooth® LE (5.x) Controller stack.

Sensor Node Controller (SNC): This controller includes an Arm Cortex M0+ and primarily serves as a local master for sensors control and as a DMA for fetching data from sensors directly to RAM while the rest of the system is completely shut down. Furthermore, it can perform processing on the sensor data before storing to RAM.

ROM: This is a 32 kB ROM containing the booter code as well as the routines for implementing authentication of the FLASH image (using Elliptic Curves).

OTP: This is a 4 kB One Time Programmable memory array that contains the symmetric keys for the FLASH image decryption, the symmetric keys for the application AES operations, and the public keys for the authentication of the FLASH image during boot. It also contains trim values programmed during production testing. It allows for a small secondary bootloader (if required).

Data RAM: Up to 1.5 MB Data RAM (DataRAM) which is shared among all masters of the system. It is used for storing code and data of the Configurable MAC, the Sensor Node Controller and application data (Cortex-M33). It comprises RAM cells of 32 kB, 128 kB, 192 kB, and 256 kB, all with content retaining as well as complete power switch-off capability. Note that two of the RAM cells used for Bluetooth® LE code and data are always running at a 32 MHz clock although the system clock speed can reach 160 MHz, so accessing those cells by the Cortex M33 will be slower compared to others.

OCTA/QUAD-SPI Flash Controller: This controller is used to communicate to FLASH supporting XiP. It can be programmed in the Quad or Octa mode. The FLASH controller supports decrypt on-the-fly while reading from the FLASH, using a dedicated AES-256-bit decryption unit, without introducing extra delays toward the CPU.

QSPI Controllers: There are two additional QSPI controllers. Both controllers support communication with external FLASH and PSRAM. An 8 kB data cache with write-back capabilities, is integrated into one of the two QSPI controllers for increased read/write performance for use with an external PSRAM only.

eMMC: This controller is used to connect to an external eMMC NAND storage card. It has an 8-bit interface and supports SDR mode up to 48 MHz. The maximum throughput of the interface is 48 MB/s.

Display Controller: This controller supports Parallel DPI/DBI-B/JDI, 3/4w SPI, and Dual/Quad SPI display interfaces. All the SPI interfaces are supported through a dedicated SPI controller with a maximum interface clock of 80 MHz. It incorporates a DMA that allows autonomous operation without CPU intervention and two layers that can natively support the blending of two framebuffers before displaying.

GPU 2D: This block is used for complex 2D graphics processing. The GPU can utilize both, internal RAM as well as external PSRAM. It supports various graphics primitives and attributes such as circles, lines, triangles, ellipses, anti-aliasing, blending, textures, and linear Alpha gradient. The GPU supports also various input and output color formats (ARGB, RGBA, ALPHA, and so on).

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Cryptography Controllers: They consist of an AES 128/192/256 bits block and a HASH controller implementing MD5, SHA-1, and SHA-2. This accelerates any application security requirements. An SW True Random Number Generator (TRNG) that enables secure key generation is also provided.

UART, UART2, and UART3: Asynchronous serial interfaces. UART2 and UART3 implement hardware flow control while UART3 is amended with ISO7816 functionality for connecting to a secure element. All UARTs are equipped with a FIFO of 16 bytes depth supporting up to 6 Mbps data rate.

SPI, SPI2, and SPI3: The SPI and SPI2 are serial peripheral interfaces with Master/Slave capability. They have separate RX/TX FIFOs (32 bytes) and support SPI clock up to 24 MHz. SPI3 is a high-speed master-only controller which supports up to 48 MHz SPI clock and includes a four bytes RX/TX FIFO.

I2C, I2C2, and I2C3: These are Master/Slave I2C interfaces used for sensors and/or host MCU communication. Each controller includes a 32 locations deep FIFO (8-bits Rx, 9-bits Tx). They can all achieve up to 3.4 Mbps with maximum 96 MHz system clock.

I3C: This is a Master-only SDR I3C interface used for sensors. It includes a 32 words deep FIFO for the RX and a 32 words deep FIFO for the TX (each word is 32-bit). The controller can achieve up to 12.5 Mbps with maximum 160 MHz system clock. It is backward compatible with I2C.

Audio blocks: This part enables audio streaming by means of a Pulse Density Modulation (PDM), dual Sample Rate Converter (SRC), and a Pulse Code Modulation (PCM) interface. Two SRC blocks, supporting simultaneous inbound and outbound audio streams, can support up to two digital microphones or two digital loudspeakers using the PDM interface or connect an external CODEC at the PCM/I2S interface.

General Purpose (GP) ADC: This is a 10-bit analog to digital converter with four external input channels and averaging circuitry, which increases the effective number of bits (ENOB) to 11 using oversampling up to 128 times.

Application ADC: This is a ΣΔ analog to digital converter used mainly for Audio/Voice with an increased effective number of bits (>11 bits ENOB). It integrates a Programmable Gain Amplifier (PGA) to adjust the input level of the microphone to the ADC input range.

Radio Transceiver: This block implements the digital and analog PHY of the Bluetooth® Low Energy protocol at 2.4 GHz.

General Purpose Timers: Six general-purpose timers of 24-bit width each are available for the user, all in their own power domain (timer power domain). They provide a number of features like PWM generation, two capture channels that save a snapshot of the timer, up/down counting with free-running mode, selectable clock source, and one-shot pulse generation with a configurable width, and edge detection counter mode. All timers support the OneShot mode and two of them support automatic switching from OneShot to the Counter mode.

Real-Time Clock: This is a hardware controller that supports the complete time of a day clock: 12/24 hours, minutes, seconds, milliseconds, and hundredths of milliseconds. It comprises a configurable alarm function and can be programmed to generate an interrupt on any event like a rollover of the month, day, hour, minute, second, or hundredths of milliseconds.

Watchdog Timers: The system comprises three watchdog timers, 13-bit wide each. One for CMAC SW monitoring (CMAC Wdog), one for the Sensor Node Controller SW monitoring (SNC Wdog), and another for the System CPU (System Wdog). The System watchdog is constantly counting down, automatically started right after POWERUP, it is powered by the sleep domain and generates an NMI and an HW Reset when 0 and -16 are reached respectively. Its maximum counting time is 84 seconds or 3 minutes depending on the clock used (RCLP32k or RCX). The CMAC Watchdog resides in the Radio power domain and generates an interrupt to the CMAC CPU and System CPU when 16 and 0 are reached respectively. The CMAC Watchdog also generates an HW reset if -16 is reached. Finally, the SNC Watchdog resides in the SNC power domain and generates an interrupt to the SNC Arm Cortex M0+ and an HW reset when 16 and -16 are reached. All watchdogs are automatically frozen when either of the three CPUs is in debug mode.

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Wake-Up Controller: This is a controller for capturing external events that can be used as a wake-up trigger on any of the GPIO ports with programmable polarity. It comprises a single debouncing structure for generating a wake-up interrupt upon a button press.

Wake-Up from Hibernation Controller: This is a small controller unit that wakes up the system from the Hibernation mode. The unit generates a wake-up signal when the trigger on any of the four dedicated GPIOs or when the presence of the signal at the VBUS power line is detected.

White LED Drivers: There are three *white* LED drivers able to sink up to 20 mA current. Their intensity is controlled by a dedicated configurable PWM signal. It provides programmability regarding the amount of sinking current while sustaining an accuracy of +/- 5%.

USB FS Device: This is a 12 Mbit/s USB device controller, which is mainly used for software upgrades. It is also used for recharging the system's battery. It supports seven endpoints with endpoint 0 having a 64 Bytes FIFO while endpoints from 1 to 6 having 512 Bytes FIFOs.

DMA Engine: This is a general-purpose DMA engine with eight channels that can be multiplexed to support data transfers between memory resources but also between memory and peripherals in single or burst modes (where applicable). It is also used when secure features are enabled to perform key transfers from OTP to registers without the CPU having access.

5.2 Digital Power Domains

The DA1470x supports a number of digital power domains that can be turned ON and OFF independently from one another.

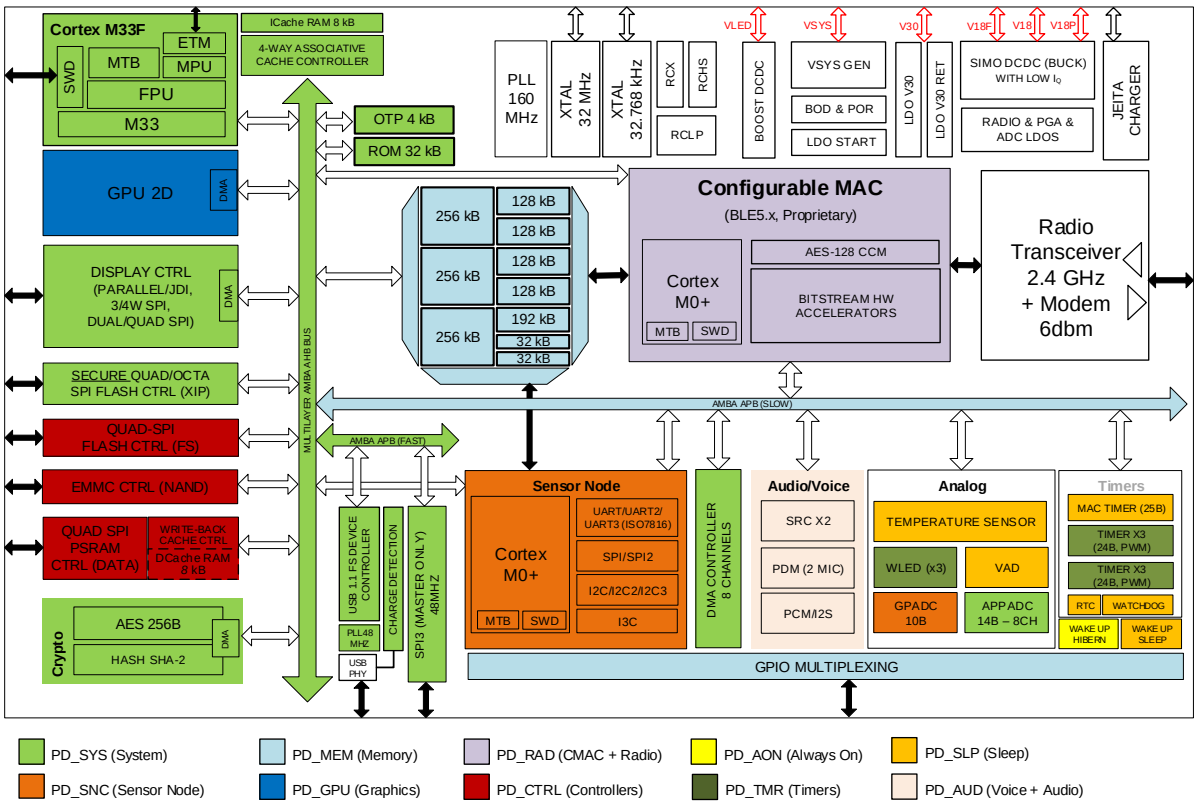

Figure 3: Digital Power Domains

The description and domain names used throughout this document are shown in Table 77.

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Table 77: Power Domains Description

#	Abbreviation	Description	Contains
1	PD_SYS	System power domain	Arm Cortex M33, Cache Controller, Octa/Quad SPI controller (XiP), OTP Controller, ROM, Crypto Block, USB Controller, Charge Detection, Charger FSM, SPI3, DMA controller, APP ADC, Display Controller (Parallel/JDI, 3/4w SPI, Dual/Quad SPI), AMBA AHB, APB-32 fast
2	PD_MEM	Memory power domain	Memory Controller, XTAL32M FSM, PLL160M regs, PLL48M regs, GPIO multiplexing, APB-32 slow, Clock calibration
3	PD_RAD	Radio power domain	CMAC, Modem, RFMON, RFCU
4	PD_AON	Always On power domain	Wake up from Hibernation controller
5	PD_SLP	Sleep power domain	MAC Timer, RTC, System Watchdog, Wake up from Sleep controller, Buck DCDC FSM, Boost DCDC FSM, WLEDs, VAD digital FSM, clock-tree
6	PD_SNC	Sensor Node Controller power domain	SNC Cortex M0+, all serial interfaces (except SPI3), GP ADC
7	PD_GPU	GPU power domain	2D GPU
8	PD_CTRL	External Memory Controller power domain	Quad SPI controllers for flash and PSRAM, write-back cache controller, and eMMC host controller
9	PD_AUD	Audio power domain	Audio/Voice interface controllers
10	PD_TMR	Timers power domain	Timer, Timer2, Timer3, Timer4, Timer5, Timer6

5.3 POWERUP, WAKEUP, and GOTO Sleep

5.3.1 Analog PMU FSM

The Analog PMU FSM is responsible for the POWERUP, WAKEUP, and GOTO sleep processes of the system, and they are presented in Figure 4.

The WOKENUP signal indicates that the Analog PMU FSM has finished, and the digital power domains will be initialized through the Digital PMU FSMs. This signal can be monitored at the register bit field SYS_STAT_REG[POWER_IS_UP].

5.3.2 Digital PMU FSM

The digital PMU FSM handles:

- Power control
- Isolation
- Retention (save, restore + reset)
- Clock enable
- Reset for non-retention flops

It is responsible for enabling the supply at the various digital power domains and letting the domain operate smoothly with the clock.

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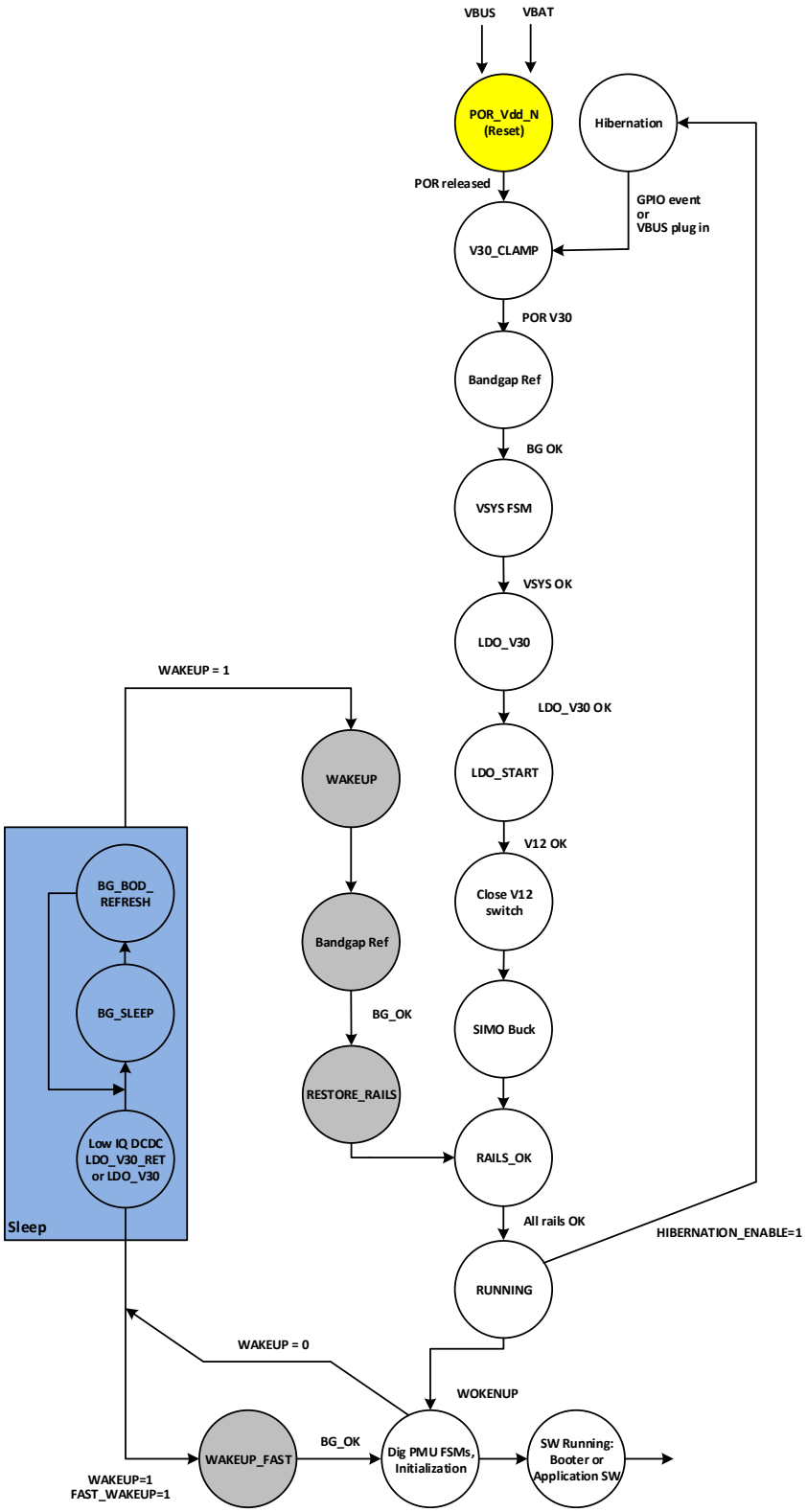

Figure 4: POWERUP, WAKEUP, GOTO Sleep

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5.3.3 POWERUP

After POR is released, the Analog PMU FSM enters state V30_Clamp, as shown in Figure 5, where the following actions are taken:

- The COLD_BOOT bit is asserted indicating that the system recovers from a POR (previous state has to be POR_Vdd_N). In this state, the RCLP will be enabled (the default speed is 32 kHz). The time required for the RCLP and the biasing of the RCLP to settle is typically 1 ms
- The V30 clamp is enabled. The clamp requires some time to settle so the voltage is stable at its output. This time can be up to 180 ms and depends on the external capacitor

The next state (BG) enables Bandgap. The latency of this state is less than 100 µs. In the next state (VSYS), the VSYS supply is generated from VBAT or VBUS by the Vsys Generation block. This state does not exceed 150 µs.

In the next step, the LDO_V30 is enabled and it takes up to 300 µs time to settle. Once the V30 rail is settled, the LDO_START is enabled and takes less than 30 ms, depending on the external capacitor. After the V12 rail is settled in the state “Close V12 switch”, the switch V12 is closed, which takes around two RCLP clk cycles.

After that, the SIMO Buck is enabled (1 RCLP clk cycle) and the LDO_START is disabled by the Analog PMU FSM. During the “RAILS_OK” state the rails are settled in less than 500 µs. In the RUNNING state, the digital state machine starts with initialization where the RCHS clock and the power domains are enabled, followed by the SW Running state (Booter).

The total time required for power-up is about 213 ms.

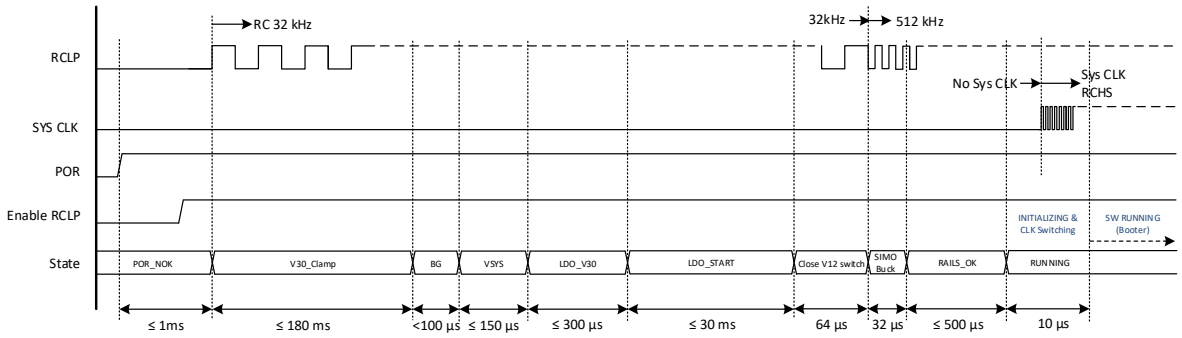

Figure 5: POWERUP Timing Diagram

5.3.4 WAKEUP Options

The complete flow of the various wake-up options is presented in Figure 6 where different stages are explained until the system is powered up and released from reset to start executing code.

There are a few hardware blocks involved in this process, namely the Wake-up Controller, the Wake-up from Hibernation Controller, the Power Domain Controller (PDC), the Analog PMU FSM, and the Digital PMU FSMs (one per each digital power domain).

NOTE
The Power Domain Controller (PDC) is responsible for taking action after waking up or before going to sleep regarding the activation/deactivation of the digital power domains of the system.

The trigger sources on the left side of the figure are driven to the PDC LUT which in turn decides what needs to be done according to the respective LUT entries. It also enables the fast clock (RCHS) and switches it in the clock tree as a system clock based on the configuration.

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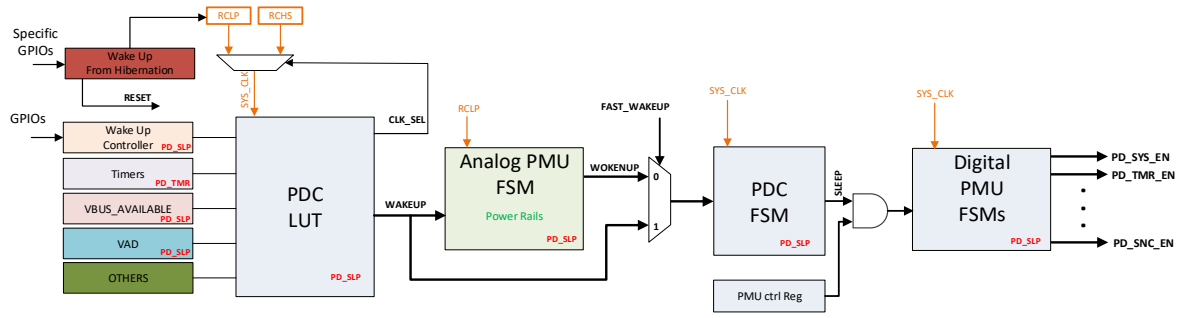

Figure 6: Wake-Up Process Flow

The PDC LUT generates a WAKEUP signal towards the Analog PMU FSM which is responsible for regulating the power supply rails of the system. If FAST WAKEUP is selected, then this FSM is practically bypassed to the next stage. Note that the bypass is done assuming the levels on power rails are good, and the Analog PMU FSM is also started in the background.

The PDC FSM then takes over triggering the Digital PMU FSMs to start enabling the power domains accordingly.

The system supports four different wake-up options: Wake-Up from Hibernation, Wake-Up, Fast Wake-Up, and VAD Wake-Up (wake-up from VAD). A user can configure which one to select depending on the application requirements and constraints. In Table 78 the wake-up modes' characteristics are summarized.

Table 78: Wake-Up Modes

Wake-up Mode	Latency	Description	Remarks
Wake-Up from Hibernation	~213 ms	Intended for the shipping mode of the product	Wake-up is possible only by specific IOs, POR, or VBUS plug-in
Wake-Up	56 – 74 µs	SW is released to run after all rails are OK	56 µs can be achieved if all the rails are maintained V12 SLEEP level 0.9 V or 1.2 V
Fast Wake-Up	~10 µs	SW is released to run before all rails are OK	No heavy load (that is >0.5 mA) should be applied for the first 100 µs. V12 SLEEP level 0.9 V or 1.2 V
VAD Wake-Up	<20 ms	SW is released to run after all rails are OK	PGA and AppADC to be able to power up and sample the voice in 1 ms. V12 SLEEP level 0.9 V or 1.2 V

In sleep mode, the low-power clock RCX is used for the timing critical blocks (such as Bluetooth® LE timer), while the RCLP is used at 32 kHz/512 kHz as a system clock.

5.3.4.1 Wake-Up from Hibernation

To support extremely low-power hibernation a wake-up mechanism is included in the system using a minimum number of gates that are powered by a clamp. This circuit is the only one that resides in the PD_AON domain. To further reduce the power consumption only four pins of the device with special pad structures are allowed to wake up the device from the hibernation state. The timing diagram for the wake-up from hibernation, shown in Figure 7, is the same as the power-up sequence.
The difference from the power-up sequence is in the wake-up trigger. The wake-up from hibernation is done by detecting a GPIO event or when VBUS is plugged in. The RCLP is enabled after any of these events.

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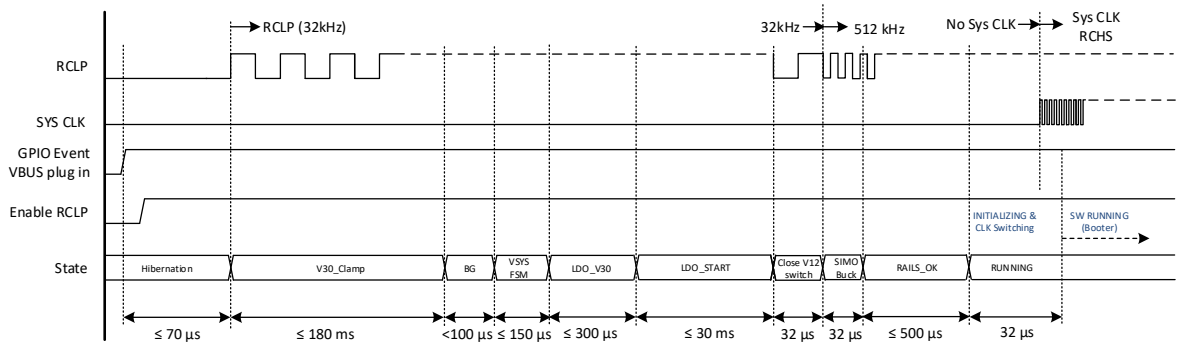

Figure 7: WAKEUP from Hibernation

5.3.4.2 Wake-Up

The WAKEUP timing diagrams for RCLP at 512 kHz and 32 kHz are presented in Figure 8 and Figure 9 respectively.

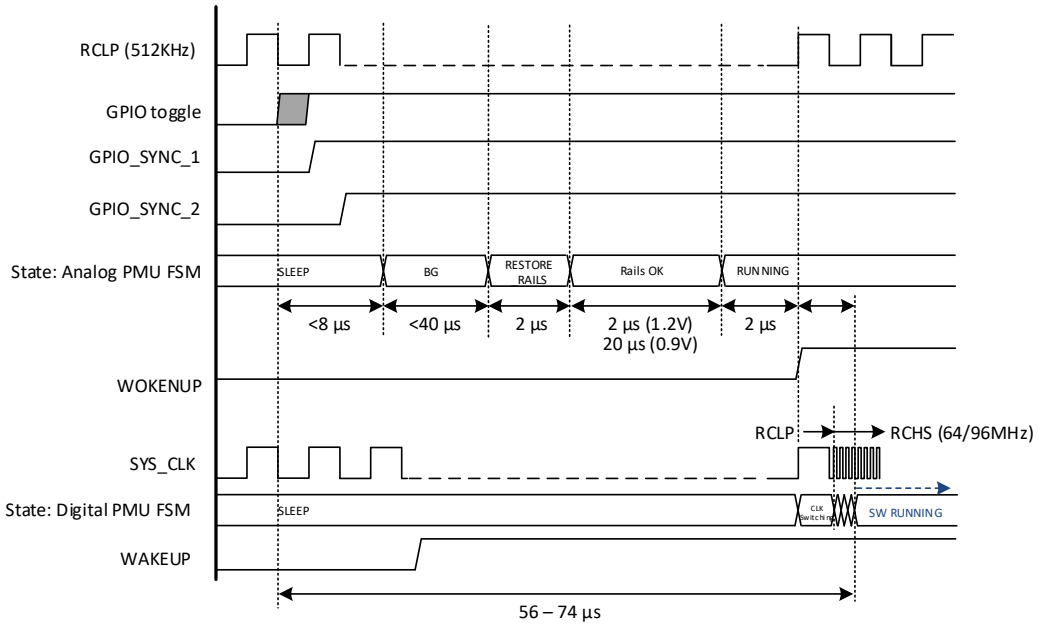

Figure 8: WAKEUP Timing Diagram (RCLP 512 kHz)

A typical latency of the wake-up, for RCLP at 512 kHz, is ~56 us when VDD (V12) is 1.2 V or ~74 µs and when VDD is 0.9 V during sleep. It takes ~20 µs for the VDD rail to restore from 0.9 V to 1.2 V. If the required system clock after the wake-up is higher than 32 MHz then a VDD of 1.2 V is required.

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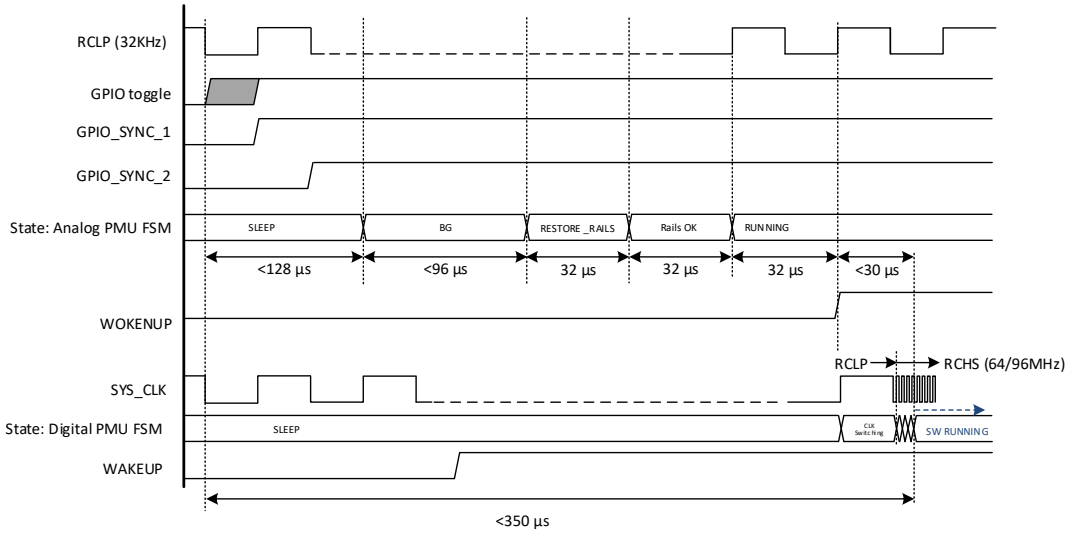

Figure 9: WAKEUP Timing Diagram (RCLP 32 kHz)

When the RCLP at 32 kHz is used, the latency of the wake-up is no more than 350 µs for either VDD at 1.2 V or 0.9 V in sleep mode.

Note that in these cases, the Digital PMU FSM follows the completion of the Analog PMU FSM which is signaled by asserting the WOKENUP line.

5.3.4.3 Fast Wake-Up

The Fast WAKEUP timing diagram is presented in Figure 10. The digital FSM starts without waiting for the analog FSM, assuming the power rails are ok. The latency of this mode (from GPIO toggle to SW running) is no more than 10 µs. If the required system clock after the wakeup is higher than 32 MHz then the VDD level should be 1.2 V during sleep.

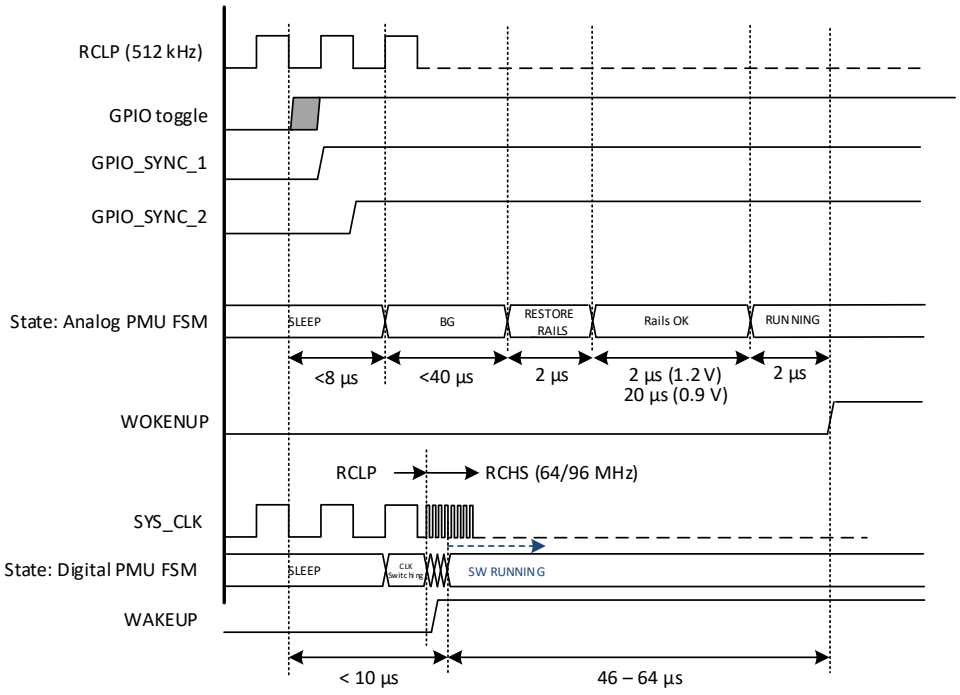

Figure 10: Fast WAKEUP Timing Diagram

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5.3.4.4 VAD Wake-Up

In this mode, the system is woken up from the VAD IRQ. The V12 rail is set at 0.9 V or 1.2 V. The timing diagram is presented in Figure 11 and includes only the wake-up of the system after VAD IRQ is generated until the Cortex-M33 or SNC is running code.

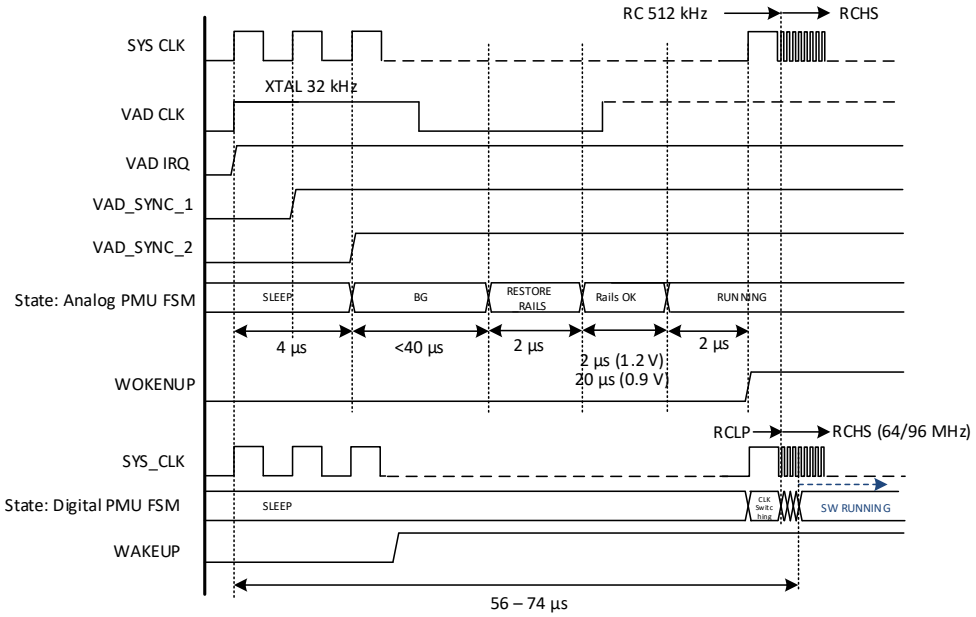

Figure 11: VAD WAKEUP Timing Diagram

5.3.5 Go-To-Sleep

The DA1470x can go to sleep only if the PDC has no pending activity from any of the three masters of the system. If this is the case, then the system enters the sleep state with the option to refresh the voltage reference by activating the bandgap periodically, as shown in Figure 12. The amount of time for switching between the two states is programmable.

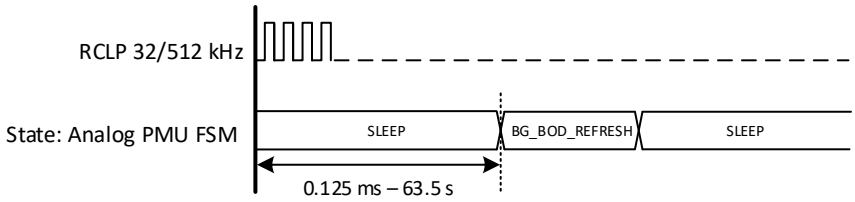

Figure 12: GOTO Sleep Timing Diagram

5.4 Power Modes and Rails

There are four main power modes in the DA1470x:

- **Hibernation mode**. This is the “Shipping mode”. There is nothing retained, no clocks running (so no RTC), and all domains are off. The system can only be woken up by a VBUS plug-in, POR, or a GPIO trigger on four **specific** GPIOs

NOTE
All domains are off, including PD_SYS meaning that the CPU will wake up in a reset state.

- **Extended Sleep mode.** This is the “Bluetooth® LE connection sleep mode”. There can be programmable RAM cells retained, slp_clk is running (so RTC is on), PD_SLP is enabled, the PD_TMR can be enabled, Bandgap will be periodically enabled to refresh the LDO’s reference voltage (LDO_V30_RET). Low IQ SIMO DCDC supplies the rails. The system can only be woken

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up by VBUS attached, POR, RTC alarm, MAC timer, another Timer, or a GPIO trigger. PD_SYS should be off

- **Deep Sleep mode.** No RAM is retained, slp_clk is running (so RTC is on), PD_SLP is enabled the PD_TMR can be enabled. The bandgap is periodically enabled to refresh the LDO's reference voltage (LDO_V30_RET). Low IQ SIMO DCDC supplies the rails. The system can only be woken up by VBUS attached, POR, RTC alarm, another Timer, or a GPIO trigger. After the wake-up, a reset will be issued because the application data are not retained in RAM
- **VAD Sleep mode.** This is the "voice activation sleep mode". During this mode, the PD_SLP and the analog VAD are enabled and the Bandgap is periodically enabled to refresh the LDO's reference voltage (LDO_V30_RET). Furthermore, the PD_TMR can be enabled and there can be programmable RAM cells retained. The other power domains of the chip are off. The VAD front end is sampling the output of an external analog microphone to generate a wake-up interrupt towards the Power Domains Controller as soon as a detectable audible peak is detected. The system can only be woken up by VAD interrupt, GPIO, or Timer trigger, and when the VBUS is attached
- **Active/Idle.** The system is up and running with a number of power domains enabled according to the use case. In the Sensor Node use case, for instance, it is just the Serial Interfaces, the Arm Cortex M0+ (PD_SNC), and the Memory PDs (PD_MEM), if Arm Cortex M33 processing power is needed then all domains might be enabled

Note that in any of the two different sleep modes, LDO_V30 could be kept running (instead of automatically switching to LDO_V30_RET by the Analog PMU FSM). Moreover, the same holds for the Boost DCDC converter.

The various configurations of the power mode are presented in Table 79.

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Table 79: Power Modes and Various Configurations

Power Mode	Power Domains	LDOs and DCDC Converters	Clocks Available	Real-Time Clock	Wake-Up From
Active	PD_SYS=Optional PD_SNC=Optional PD_MEM=Active PD_GPU=Optional PD_RAD=Optional PD_CTRL=Optional PD_AON=Active PD_TMR=Optional PD_SLP=Active PD_AUD=Optional	VSYS Generation = ON LDO_V30 = ON, LDO_V30_RET = OFF LDO_START = OFF V30 CLAMP = OFF, VDD clamp ON (sw V12 closed) BUCK = ON BOOST = OPTIONAL	All	Running	N/A
VAD Sleep	PD_SYS=OFF PD_SNC=OFF PD_MEM=OFF PD_GPU=OFF PD_RAD=OFF PD_CTRL=OFF PD_AON=ON PD_TMR=Optional PD_SLP=ON PD_AUD=OFF	VSYS Generation = ON LDO_V30 = OPTIONAL, LDO_V30_RET = ON LDO_START = OFF V30 CLAMP = OFF, VDD clamp ON (sw V12 closed) BUCK = low IQ (sleep) mode BOOST = OPTIONAL (refreshing mode if the Boost is needed in the sleep mode)	RCX RCLP XTAL32K	Running	VAD interrupt GPIO Toggle RTC Alarm Timer Expiration MAC Timer Expiration VBUS Available nRST pin
Extended Sleep	PD_SYS=OFF PD_SNC=OFF PD_MEM=OFF PD_GPU=OFF PD_RAD=OFF PD_CTRL=OFF PD_AON=ON PD_TMR=Optional PD_SLP=ON PD_AUD=OFF	VSYS Generation = ON LDO_V30 = OPTIONAL, LDO_V30_RET = ON LDO_START = OFF V30 CLAMP = OFF, VDD clamp ON (sw V12 closed) BUCK = ON (low IQ sleep mode) BOOST = OPTIONAL (refreshing mode if the Boost is needed in the sleep mode)	RCX RCLP XTAL32K	Running	GPIO Toggle RTC Alarm Timer Expiration MAC Timer Expiration VBUS Available nRST pin

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Power Mode	Power Domains	LDOs and DCDC Converters	Clocks Available	Real-Time Clock	Wake-Up From
Deep Sleep	PD_SYS=OFF PD_SNC=OFF PD_MEM=OFF PD_GPU=OFF PD_RAD=OFF PD_CTRL=OFF PD_AON=ON PD_TMR=Optional PD_SLP=ON PD_AUD=OFF	VSYS Generation = ON LDO_V30 = OPTIONAL, LDO_V30_RET = ON LDO_START = OFF V30 CLAMP = OFF, VDD clamp ON (sw V12 closed) BUCK = ON (low IQ sleep mode) BOOST = OFF	RCX RCLP XTAL32K	Running	GPIO Toggle RTC Alarm Timer Expiration MAC Timer Expiration VBUS Available nRST pin
Hibernation	PD_SYS=OFF PD_SNC=OFF PD_MEM=OFF PD_GPU=OFF PD_RAD=OFF PD_CTRL=OFF PD_AON=ON PD_TMR=OFF PD_SLP=OFF PD_AUD=OFF	VSYS Generation = OFF LDO_V30 = OFF, LDO_V30_RET = OFF LDO_START = OFF V30 CLAMP = OFF, VDD clamp ON (sw V12 open) BUCK = OFF BOOST = OFF	None	No RTC	GPIO Toggle VBUS Available

Note that the amount of retainable RAM is totally decoupled from the actual power mode. Each sleep mode can have RAM retained or not, except hibernation and deep sleep. The power modes are depicting the power domains, the analog blocks, and the clock resource configurations.

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5.5 OTP

5.5.1 Layout

The OTP layout is presented in Table 80.

Table 80: OTP Layout

Bytes	Words	Description	OTP Address
1024	256	**Configuration Script** ~100 registers write operations	0x00000C00
256	64	**OQSPI FW Decryption Keys Area – Payload** Write/read-protected when secure mode enabled in CS Secure mode connects those (8 * 256-bits) keys to OQSPI Controller	0x00000B00
256	64	**User Data Encryption Keys – Payload** Write/read-protected when secure mode is enabled in CS. Secure mode connects those (8 * 256-bits) keys to the AES engine	0x00000A00
32	8	**OQSPI FW Decryption Keys Area – Index** Eight entries for eight 256-bit keys	0x000009E0
32	8	**User Data Encryption Keys – Index** Eight entries for eight 256-bit keys	0x000009C0
256	64	**Signature Keys Area – Payload**	0x000008C0
32	8	**Signature Keys Area – Index**	0x000008A0
2208	552	**Customer Application Area** Secondary bootloader, Scratchpad, binaries, and so on	0x00000000

Using the Customer Application Area as a secondary bootloader is an option but the remapping and SW reset should be programmed in the CS.

5.5.2 Keys and Indexing

There are three different groups of keys in the OTP:

- The OQSPI FW decryption keys group
- The user application symmetric keys group
- The signature keys group

The first contains the keys that can be used for decryption-on-the-fly while the CPU is executing code in place from the FLASH with help of the cache controller. The second contains user-defined keys that can/will be used by the application with help of the crypto block (AES accelerator). The last contains public keys used for authentication of the FLASH image while booting (Secure Boot).

Each group has its own index section. There are eight entries in every index section, each entry is initially 0xFF. Every index entry corresponds to a 256-bit key. If an entry is written with 0x00, then the respective key is revoked and hence not used anymore. Revocation is only done through the booter.

5.5.3 Customer Application Area

A 2 kB space can be used for a small secondary bootloader that runs a limited amount of software. The system can be programmed to remap address zero to the OTP base address. So right after booting, the CPU starts executing code from the OTP base address.

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5.6 Booting

The booter is always executed when a POR, an HW Reset, or the RESET_ON_WAKEUP feature is configured. Different booting flavors are supported:

- Boot from cached OQSPI FLASH without secure features, configuration script in OTP
- Boot from cached OQSPI FLASH without secure features, configuration script in FLASH
- Boot from cached OQSPI FLASH with secure features, configuration script in OTP
- Boot from UART without FLASH or secure features

The booter will also detect available software updates and apply them according to the FLASH header. Note that the booter cannot boot a flash image if the Product Header or the active image partition is below the 128 Mbit address (0x1000000) in the flash. This happens because the flash opcode that allows for reading addresses larger than 24 bits is not unified across all flash vendors.

The Boot flow is divided into five separate phases:

- Initialization
- Run configuration script
- Retrieve application code
- Device administration
- Load image

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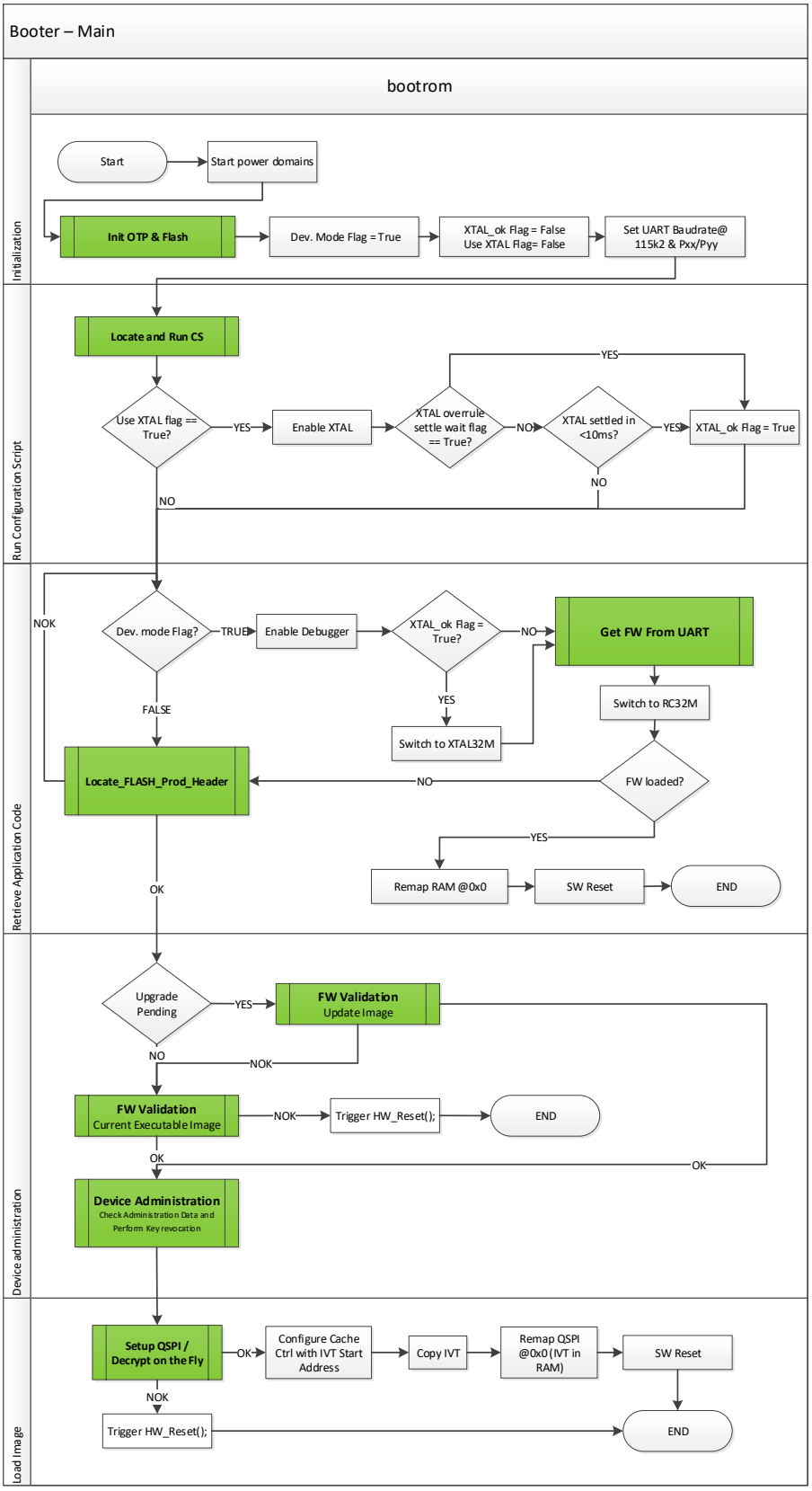

Figure 13: BootROM Flowchart

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5.6.1 Initialization

The initialization phase takes care of enabling the Power domains. Then it initializes the OTP Controller, SPI flash interface, and Clocks. Following this, it enables Development mode. This is done so that it can be disabled by the CS in the next phase if desired. Development mode can be used to be able to have the debugger on by default and update the device firmware using UART. Next, it initializes the internal booter flags.

Finally, the booter initializes the UART (but not enable it yet) with the default settings, which can be overwritten by the user, using the CS.

5.6.2 Configuration Script

This phase is to locate and execute the Configuration Script (CS) from OTP or FLASH. It is expected to be at address 0x00000C00 in OTP, or at the start of the OQSPI FLASH. If none is found, the booter just continues to the next step assuming that there is no configuration script in place.

The CS can be used to disable Development mode, which is set to true by the initialization phase of the Booter by default. Once development is finished and security is needed, the Development mode should be disabled.

The way a CS is detected is by looking at the location where it is expected and verifying if the CS Start command is found. If a CS is found, either in OTP or FLASH, it will be parsed and executed. It will stop parsing when any of the following happens:

- It reaches the stop command
- It reaches the first empty entry
- It reaches the maximum length

The stop command (0x00000000) is used to lock the CS and the booter will not evaluate any entries after this command except the minimum FW version keyword. This can be used by the rollback prevention feature to tell the booter the minimum allowed FW version it can accept. There can be multiple entries, but only the one with the highest FW version number will be decisive.

After the CS is parsed it will evaluate the “use XTAL flag”. If not set in the CS, the booter will continue the RCHS 32 MHz clock.

5.6.3 Retrieve Application Code Phase

During this phase, the booter scans to check if the development mode flag is disabled or not. If it is still in development mode, it will enable the Debug interface and try to boot from UART. If booting from UART is successful, then it will issue an SW reset after having remapped address zero to RAM. If not, then it will try to locate a valid FLASH header, trying to boot from FLASH.

If not in development mode, the booter will continue to the next phase after having identified a valid product header in the FLASH. A valid product header is identified by a programmed “FLASH programmed identifier” and an “Active FW Image Address”.

5.6.4 Device Administration

The device administration phase is used to check for pending updates and validate the FLASH images. It also processes corresponding image headers and revokes keys, if needed.

The booter will check if the “Active FW Image address” and the “Upgrade Image address” fields of the FLASH product header are the same. If not, an upgrade image is available. The FW validation is executed to see if the image header is valid. If the secure boot bit is set by the CS, validation is extended by identifying the public key, checking if the key is already revoked, and if not, proceeds with invoking the Ed25519 verification algorithm.

After the verification algorithm is completed, the booter checks if the FW version in the image header is acceptable by the minimum FW version stored in the CS. When the size is acceptable the image will be authenticated, and the booter checks for any “key revocation record” in the FLASH image.

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This triggers the revocation of the key that is currently in use. Note that the key revocation requires an OTP write as explained in Section 5.5.2.

5.6.5 Load Image

In this final phase, the actual FW image is loaded. This is done by setting up the OQSPI and cache controllers and executing the OQSPI Loader, which is located in the Product header of the FLASH. If secure boot is enabled, the OQSPI controller initializes to decrypt on the fly. The cache controller is then configured to point to the interrupt vector table (copied in RAM) and address zero is remapped to OQSPI FLASH. Any error condition during this or previous phases results in an HW reset.

5.7 Memory Map

The mapping of the system's internal resources is presented in Table 81. Note that *_C defines a Controller (registers) while *_M defines Memory (RAM) space. All resources are 32-bit aligned.

Table 81: Memory Map

Device	Start Addr	End Addr	Size (kB)	PD	BUS	Comments
Remapped Devices	0	8000000	131072	PD_SYS	AHB	Remapped M33 code
IVT&others	F000000	F002000	8	PD_MEM	AHB	
ROM	F020000	F030000	64	PD_SYS		Remapped at 0x0
SYSRAM (code)	10000000	10050000	320	PD_MEM		
CACHE_RAM	10060000	10070000	64	PD_SYS	AHB	Remapped at 0x0
OTPC_C	10070000	10080000	64	PD_SYS	AHB	
OTPC_M	10080000	10090000	64	PD_SYS	AHB	The first 4 kB Remapped at 0x0
CACHE_SYS_MON_DATA	100B0000	100B2000	8	PD_SYS		Locally decoded in the CACHE. Used for monitoring SYS Cache Data (for debugging)
CACHE_SYS_MON_TAG	100B2000	100B6000	16	PD_SYS		Locally decoded in the CACHE. Used for monitoring SYS Cache TAG (for debugging)
CACHE_C	100C0000	100C0100	0.25	PD_SYS	AHB	
OQSPIF_C	16000000	17000000	16384	PD_SYS	AHB	
OQSPIF_M	18000000	20000000	131072	PD_SYS	AHB	Remapped at 0x0. Support up to 128 MB XiP FLASH
SYSRAM (data)	20000000	20180000	1536	PD_MEM	AHB	The first 320 kB have the same physical address as SYSRAM (code). RAM3

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Device	Start Addr	End Addr	Size (kB)	PD	BUS	Comments
						and RAM1 can be remapped at 0x0
MTB	20180000	20183000	12	PD_MEM		
QSPIC2_C	26000000	27000000	16384	PD_CTRL	AHB	
QSPIC2_M	28000000	30000000	131072	PD_CTRL	AHB	Supports up to 128 MB PSRAM
AHB_DMA_B	30020000	30020400	1	PD_SYS	AHB	
LCD_C	30030000	30040000	64	PD_SYS	AHB	
AES_HASH_C	30040000	30050000	64	PD_SYS	AHB	
CACHE_RAM	30060000	30070000	64	PD_SYS	AHB	Same physical address as 0x10060000
OTPC_C	30070000	30080000	64	PD_SYS	AHB	Same physical address as 0x10070000
OTPC_M	30080000	30090000	64	PD_SYS	AHB	Same physical address as 0x10080000
DCACHE_C	30100000	30104000	16	PD_CTRL	AHB	
DCACHE_M	30104000	30108000	16	PD_CTRL	AHB	
OQSPIC_C	36000000	37000000	16384	PD_SYS	AHB	Same physical address as 0x16000000
OQSPIC_M	38000000	40000000	131072	PD_SYS	AHB	Same physical address as 0x18000000
CMAC	40000000	40003200	12.5	PD_RAD	AHB	
RFCU	40003200	40003400	0.5	PD_RAD	AHB	
RFCU_POWER	40003400	40003600	0.5	PD_RAD	AHB	
DEM	40003600	40003A00	1	PD_RAD	AHB	
SYNTH	40003A00	40004200	2	PD_RAD	AHB	RFPLL is inside PD_SYNTH, a digital island in the radio analog
RFMON	40010000	40010200	0.5	PD_RAD	AHB	
QSPIC_C	46000000	47000000	16384	PD_CTRL	AHB	
QSPIC_M	48000000	50000000	131072	PD_CTRL	AHB	Supports up to 128 MB ext FLASH
CRG_TOP	50000000	50000100	0.25	PD_SLP	APB32-slow	
PDC	50000200	50000300	0.25	PD_SLP	APB32-slow	
DCDC	50000300	50000400	0.25	PD_SLP	APB32-slow	
DCDC Booster	50000500	50000600	0.25	PD_SLP	APB32-slow	

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Device	Start Addr	End Addr	Size (kB)	PD	BUS	Comments
WDOG	50000700	50000800	0.25	PD_SLP	APB32-slow	
RTC	50000800	50000900	0.25	PD_SLP	APB32-slow	
WKUP	50000900	50000A00	0.25	PD_SLP	APB32-slow	
CMAC_SLP	50000A00	50000B00	0.25	PD_SLP	APB32-slow	
CRG_VSYS	50000B00	50000C00	0.25	PD_SLP	APB32-slow	
VAD	50000C00	50000D00	0.25	PD_SLP	APB32-slow	
TIMER	50010000	50010100	0.25	PD_TMR	APB32-slow	
TIMER2	50010100	50010200	0.25	PD_TMR	APB32-slow	
TIMER3	50010200	50010300	0.25	PD_TMR	APB32-slow	
TIMER4	50010300	50010400	0.25	PD_TMR	APB32-slow	
TIMER5	50010400	50010500	0.25	PD_TMR	APB32-slow	
TIMER6	50010500	50010600	0.25	PD_TMR	APB32-slow	
PWMLED	50010600	50010700	0.25	PD_TMR	APB32-slow	
UART	50020000	50020100	0.25	PD_SNC	APB32-slow	
UART2	50020100	50020200	0.25	PD_SNC	APB32-slow	
UART3	50020200	50020300	0.25	PD_SNC	APB32-slow	
SPI	50020300	50020400	0.25	PD_SNC	APB32-slow	
SPI2	50020400	50020500	0.25	PD_SNC	APB32-slow	
I2C3	50020500	50020600	0.25	PD_SNC	APB32-slow	
I2C	50020600	50020700	0.25	PD_SNC	APB32-slow	
I2C2	50020700	50020800	0.25	PD_SNC	APB32-slow	
GPADC	50020800	50020900	0.25	PD_SNC	APB32-slow	
CRG_SNC	50020900	50020A00	0.25	PD_SNC	APB32-slow	
I3C	50020C00	50020F00	0.75	PD_SNC	APB32-slow	

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Device	Start Addr	End Addr	Size (kB)	PD	BUS	Comments
SNC_C	50021000	50021100	0.25	PD_SNC	APB32-slow	
CRG_AUD	50030000	50030100	0.25	PD_AUD	APB32-slow	
SRC1	50030100	50030200	0.25	PD_AUD	APB32-slow	
SRC2	50030200	50030300	0.25	PD_AUD	APB32-slow	
PCM	50030300	50030400	0.25	PD_AUD	APB32-slow	
VERSION	50040000	50040100	0.25	PD_SYS	APB32-slow	
GPREG	50040100	50040200	0.25	PD_SYS	APB32-slow	
GHARGER Detection	50040300	50040400	0.25	PD_SYS	APB32-slow	
CRG_SYS	50040400	50040500	0.25	PD_SYS	APB32-slow	
SDADC	50040500	50040600	0.25	PD_SYS	APB32-slow	
SYSBUS_ICM	50040600	50040700	0.25	PD_SYS	APB32-slow	
MEMCTRL_C	50050000	50050100	0.25	PD_MEM	APB32-slow	
GPIOMUX	50050100	50050300	0.5	PD_MEM	APB32-slow	
CRG_XTAL	50050400	50050500	0.25	PD_MEM	APB32-slow	
ANAMISC	50050600	50050700	0.25	PD_MEM	APB32-slow	
CRG_CTRL	50060000	50060100	0.25	PD_CTRL	APB32-slow	
USB_C	51000000	51000200	0.5	PD_SYS	APB32-fast	
SPI3	51000200	51000300	0.25	PD_SYS	APB32-fast	
GPDMA	51000400	51000600	0.5	PD_SYS	APB32-fast	
CHARGER	51000600	51000700	0.25	PD_SYS	APB32-fast	
CRG_GPU	51001000	51001100	0.25	PD_GPU	APB32-fast	
GPU	51001100	51001300	0.5	PD_GPU	APB32-fast	
ARM Internal Bus	E0000000	FFFFFFFF	524288.0	PD_SYS		

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5.8 Busy Status Registers

The DA1470x has three processing units that might request access to one or more of the system's peripheral controllers. The application software can map certain resources to one of the processing units. There are cases that more than one processing unit might request access to the same peripheral controller. An example is when the SNC accessing a UART interface and the Application Processor (Arm Cortex M33) wants to access the same UART controller.

To avoid race conditions and provide all three processing units with a robust way of identifying who the owner of the peripheral is, a hardware mutex is implemented. The DA1470x has two 32-bit Busy Status Registers (BUSY_STAT_REG, BUSY_STAT_REG2) which can be set/reset by using write-only registers (BUSY_SET/RESET_REG, BUST_SET/RESET_REG2). This can eliminate the race conditions from happening because only one processing unit can write (set or reset) the register at any given time. Two bits are reserved per resource so that the value represents the owner of the resource:

- 0x0: resource is available for use
- 0x1: resource is busy, controlled by the SNC M0+
- 0x2: resource is busy, controlled by the Cortex-M33
- 0x3: resource is busy, controlled by the CMAC

Such a mutex register, which decides resources that require sharing, can be defined by application software. Table 82 and Table 83 show a possible configuration for the two BSR registers.

Table 82: Busy Status Register 1

31-30	28-29	26-27	24-25	22-23	20-21	18-19	16-17	14-15	12-13	10-11	8-9	6-7	4-5	2-3	0-1	Bit
SDADC	GPADC	SRC2	SRC	PDM	PCM	I3C	I2C3	I2C2	I2C	SPI3	SPI2	SPI	UART3	UART2	UART	**controller**

Table 83: Busy Status Register 2

31-12	10-11	8-9	6-7	4-5	2-3	0-1	Bit
RESERVED	Timer6	Timer5	Timer4	Timer3	Timer2	Timer	**controller**

Note that BSRs are in the PD_MEM power domain, which is automatically activated if one of the three masters is alive. However, if the system is in sleep, these registers are not retained, and their contents need to be restored from retention RAM.

5.9 Remapping

Remapping options are explained in Table 84.

Table 84: Remapping Options

Remap Field in the SYS_CTRL_REG – 3 bits	
0x0	Remap ROM to address 0
0x1	Remap OTP to address 0
0x2	Remap FLASH cached area
0x3	Remap SysRAM1 to address 0

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0x4	Reserved
0x5	Remap SysRAM3 to address 0
0x6	Remap to CACHE_DATA_RAM
0x7	Reserved

In the case of FLASH cached (default use case), CACHE_FLASH_REG contains the base address, the offset, and the size of the FLASH image.

5.10 Security Features

The DA1470x supports a number of security features that can be configured. This is done using the configuration script to program the following write-one-only (sticky) register bits (Note that these bits can only be reset by HW or POReset).

Table 85: Security Configuration Options

Bit Field	Description
FORCE_M33_DEBUGGER_OFF	This bit will permanently disable the M33 debugger
FORCE_CMAC_DEBUGGER_OFF	This bit will permanently disable the CMAC debugger
PROT_OQSPIF_KEY_READ	This bit will permanently disable CPU read capability at OTP offset 0x00000B00 and for the complete segment (see Table 80)
PROT_OQSPIF_KEY_WRITE	This bit will permanently disable ANY write capability at OTP offset 0x00000B00 and for the complete segment (see Table 80)
PROT_AES_KEY_READ	This bit will permanently disable CPU read capability at OTP offset 0x00000A00 and for the complete segment (see Table 80). The AES sections are only used by the application SW, but protecting the key area from read/write makes it secure after leaving the manufacturing facilities
PROT_AES_KEY_WRITE	This bit will permanently disable ANY write capability at OTP offset 0x00000A00 and for the complete segment. The AES sections are only used by the application SW, but protecting the key area from read/write makes it secure after leaving the manufacturing facilities
PROT_SIG_KEY_WRITE	This bit will permanently disable ANY write capability at OTP offset 0x000008C0 and for the complete segment (see Table 80). This is for protecting public keys from being written (used by ECC only)
SECURE_BOOT	This bit will enable authentication of the image in the FLASH while the system is booting and expect the image to be encrypted
FORCE_SNC_DEBUGGER_OFF	This bit will permanently disable the SNC (M0+) debugger
PROT_CS_WRITE	This bit will permanently disable ANY write capability at OTP offset 0x00000C00 and for the complete segment of the CS (see Table 80)

5.10.1 Secure Keys Manipulation

This feature allows for programming up to eight different 256-bit symmetric keys for each of the encrypted images or the user application cases and up to eight different 256-bit ECC keys for the authentication of the FLASH image. A revocation mechanism is supported through the booter as explained in previous sections allowing for changing the current key of any of the three operations while the product is in the field.

5.10.2 Secure Boot

The feature is enabled by programming the SECURE_BOOT_REG[SECURE_BOOT] bit in the configuration script in the OTP.

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This forces authentication of the FLASH image before booting is finished. The booter code configures the RCHS clock to 96 MHz and then executes the Ed25519 verification algorithm. If the generated signature and the signature are stored in the FLASH match, authentication is successful, and booting is continued. If not, an HW reset is issued.

The aforementioned process represents the “FW Validation” state in Figure 13.

5.10.3 Secure Access

Permanently disabling the JTAG interface, prevents unwanted access to the DA1470x. This is done by programming the SECURE_BOOT_REG[FORCE_DEBUGGER_OFF] in the configuration script. This disconnects the SWD signals from the CPU’s SWD controller.

Except for the sticky bit, the debugger has its own enable bit; namely, the SYS_CTRL_REG[DEBUGGER_ENABLE] which is by default disabled. This bit is enabled during booting, at the “Retrieve Application Code” phase (see Figure 13).

If nothing is programmed in the configuration script, JTAG is enabled a few microseconds after POWERUP. If the sticky bit is programmed, JTAG is permanently disabled.

5.10.4 Validation

Every device can be uniquely identified using the Position, Package, and Time Stamp information put in the configuration script during the production test. This is a 64-bit word, which contains information about the position of the die, the wafer number, the package, and the time stamp of the production testing that is compared to the Tester ID and site.

5.10.5 Cryptography Operations

The DA1470x is equipped with HW acceleration for supporting all modern cryptography operations. More specifically, it comprises:

- A 128/192/256-bit capable AES encryption/decryption and key expansion engine that implements ECB/CBC/CTR modes covering all symmetric key application needs
- A complete HASH block supporting up to SHA 512 bits

A real True Random Number Generation that is capable of generating 1024 random bits in 64k clock cycles is implemented in the software.

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6 Power

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

6.1 Introduction

The DA1470x has a completely integrated Power Management Unit (PMU). This includes a Single Inductance Multiple Output (SIMO) DC-DC converter with four outputs, a DC-DC boost converter, a number of LDOs for the different power rails of the system, a Constant-Current-Constant-Voltage (CCCV) charger for battery recharging, a charge detection circuit, and power path management. The PMU can supply external devices even when the DA1470x is in sleep mode. Figure 14 shows the system diagram of the analog Power Management Unit (PMU).

Features

- Synchronous Single Inductance Multiple Output Buck DC-DC converter with four output power rails
  - Active during sleep mode with low quiescent current
  - Internal 1.2 V and 1.4 V rails
  - One output at 1.8 V with 100 mA load capability for powering external devices
  - One output programmable at 1.2 V or 1.8 V with 100 mA load capability for powering external devices
- Boost DC-DC converter at 4.5 V to 5 V
  - 150 mA load capability
  - Duty cycled during sleep mode with 300 µA maximum load capability
- Active and Sleep modes current limited LDOs
- CC/CV Charger
  - Battery/die-temperature protection according to JEITA
  - Hardware charge detection FSM
  - Protection of charging register in control of charging characteristics
- Power path management
  - Decoupling of VSYS and VBAT to avoid system loads on the battery while charging
  - 1 A capably VSYS node
- Control over and undershoots on rails within specific boundaries
- Battery check circuit for calculating internal resistance
- Power rails fast discharge, to power cycle external components supplied by these rails

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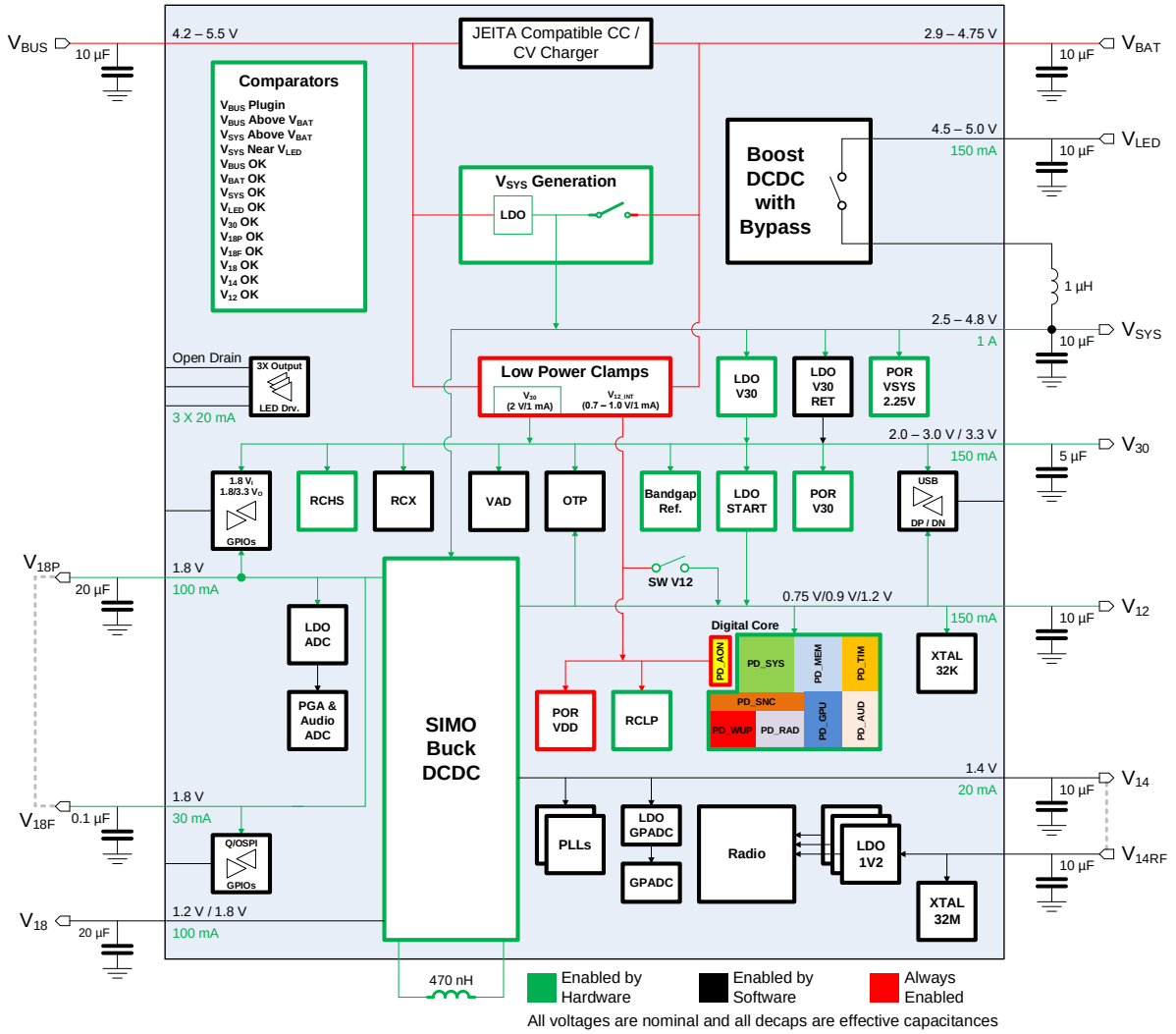

Figure 14: Power Management Unit Architecture

Note that all decoupling capacitor values listed in Figure 14 are effective values.

6.2 Architecture

6.2.1 Low IQ SIMO DC-DC Converter

The SIMO DC-DC converter supplies the V18, V18P, V14, and V12 rails. It can supply 100 mA to both 1.8 V rails, up to 100 mA to the digital core, and 20 mA to the radio, and has a quiescent current of less than 1 µA typical.

A block diagram of the converter is shown in Figure 15. It consists of four low-power continuous-time comparators that monitor the output rails and compare directly to reference voltages from the bandgap. These references are continuously generated in active mode and are maintained using a sample and hold structure during sleep operation.

When an undervoltage is detected, the asynchronous controller places it in a FIFO buffer and triggers activation of the P side switch and appropriate output select switch. The P side switch is kept closed until either the undervoltage is no longer present on the rail in question or the maximum allowable inductor current is reached. It then opens the P side switch and closes the N side switch.

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This switch opens together with the output select switch when the inductor current reaches zero, and then the converter enters idle mode.

At that point, the FIFO buffer in the controller is shifted by one position and if another output is queued, a new charge cycle is triggered, and so on.

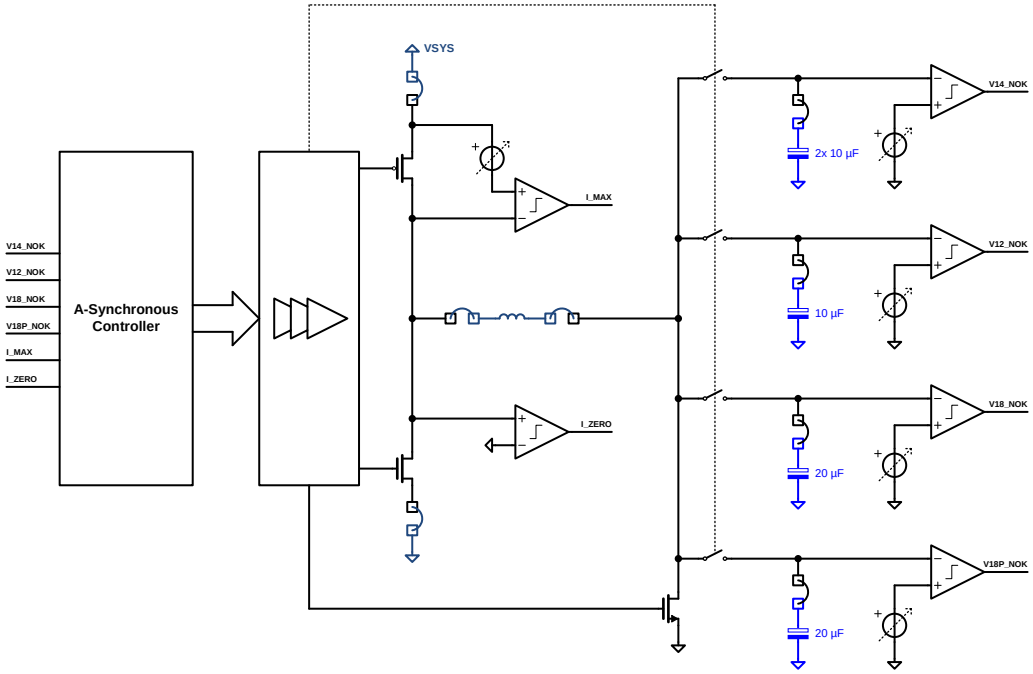

Figure 15: SIMO Buck Converter Block Diagram

6.2.2 Boost DC-DC Converter

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	×	✓	✓	✓

The boost converter is supplied by VSYS and steps up the battery voltage to the selected output voltage when needed. If the VSYS voltage becomes too high and is close to the booster output voltage, then it is bypassed. The decision is based on the VSYS domain comparator. The VSYS comparator threshold level is selectable and “tracks” the booster programmed output voltage level.

The booster can drive up to 150 mA current in normal conversion mode and up to 300 µA in sleep-mode operation.

The supply pin (VLED) is supplied by either the boost converter in active conversion mode or when the VSYS is near VLED, the boost converter is bypassed by keeping the high-side power active. In low-power sleep-mode operation, a dedicated switch (described in Section 7) is available to directly connect VLED and VSYS when VSYS becomes too close to VLED.

Figure 16 shows the block diagram of the Boost DC-DC Converter.

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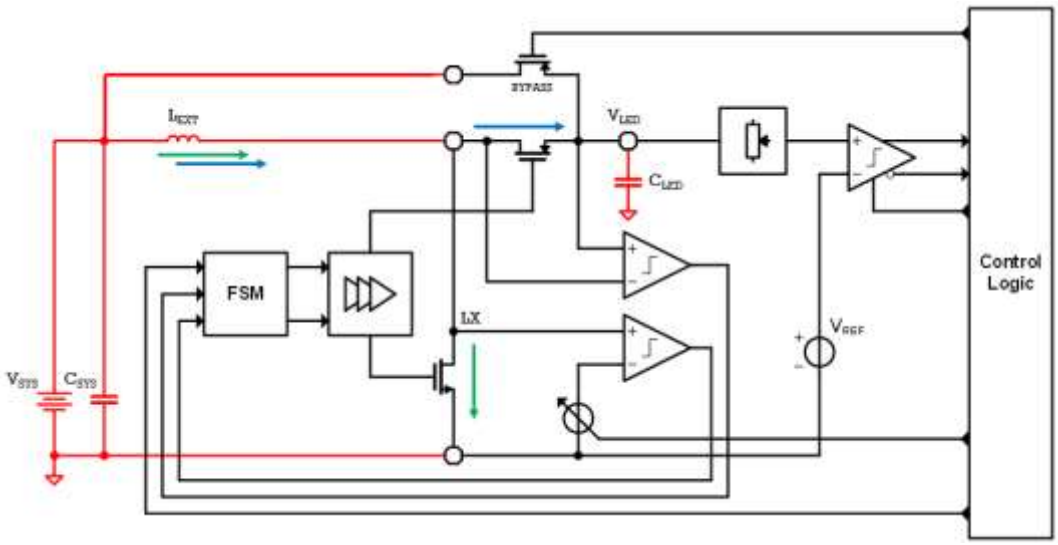

Figure 16: DC-DC Boost Converter Block Diagram

Figure 17 shows the way of working. The orange curve shows the current through the inductor. In the first phase, the NMOST is conducting and the current is ramping up until a predefined limit. In the second phase, the PMOST is conducting and the current goes into the load. The zero crossing of the current is detected and the PMOST switch is opened. The next charging cycle starts when the output voltage (blue line) drops below a predefined level.

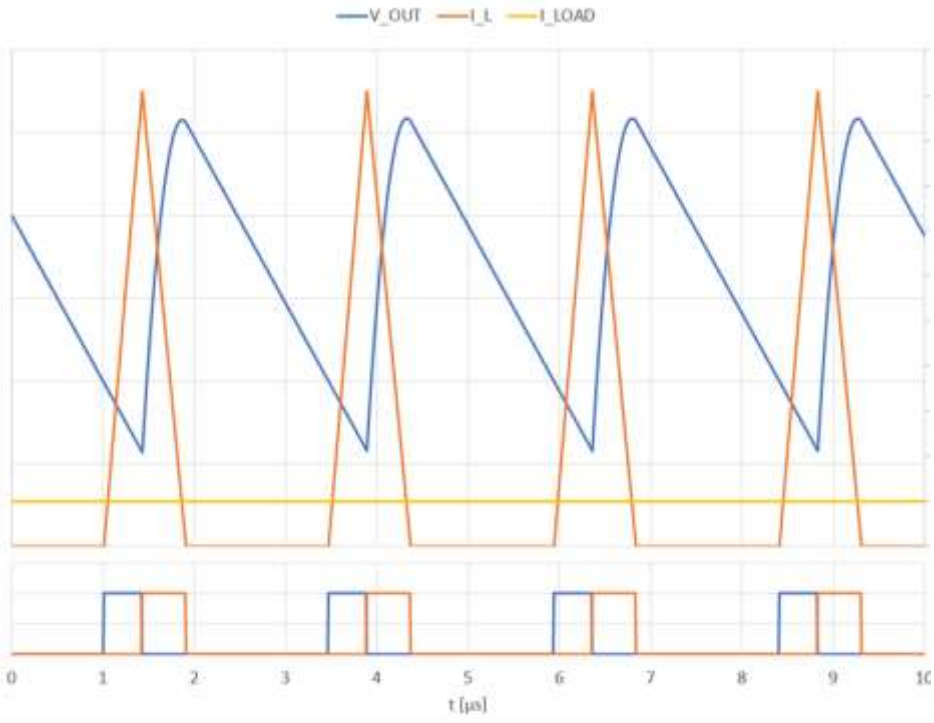

Figure 17: DC-DC Boost Principle

Note that there is no backdrive diode in the series with the booster. That means VLED output is pre-charged to almost VSYS's level and it cannot drop lower than VSYS - 0.7 V.

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6.2.3 Analog Switch

The Analog Switch is responsible for controlling the supply source of the VLED pin output. The two available power sources are the DC-DC boost converter and the VSYS pin. The switch is primarily controlled by an HW FSM but it can always be overridden by SW.

The FSM includes the following features:

- Uses the systems comparator ($V_{SYS\_NEAR\_VLED}$) to check if a VSYS voltage is near VLED
- A debouncing scheme of 256 steps, 10 ms each step
- Debouncing threshold register, configurable
- Enable/disable the FSM

Assuming that VSYS is available, the debouncing scheme is triggered to wait for the programmable amount of time before re-sensing the comparator's output. If VSYS is still near VLED after this time, the switch connects the VLED to the VSYS pin. Otherwise, it keeps connecting the VLED to the Boost converter.

6.2.4 LDOs

The DA1470x includes LDOs to provide a stable power supply to specific rails. The LDO_V30 supplies the V30 rail from VSYS with a 3.0 V/3.3 V output setting. Uses the bandgap as reference voltage when the system is started up and VDD during boot, because the bandgap is supplied from V30 which would result in a deadlock. The output is back-drive protected and high-impedance when disabled.

The LDO_V30_RET is a low-power LDO that supplies the V30 rail from VSYS in sleep mode (or in active mode at low load). It supports the 3.0 V/3.3 V output setting and the output is back-drive protected and high-impedance when disabled. Finally, the LDO_START supplies the V12 rail from V30 only during start-up and the output is high impedance when disabled.

6.2.5 Vsys Generation

Vsys is the main supply for the system as all other rails are supplied from Vsys in active. The function of the Vsys generation block is to generate Vsys from either Vbat and/or Vbus and make sure that when a switch from/to Vbat/Vbus is made, no dips occur.

The Vsys generation block consists of two subblocks, namely LDO_VSYS and SWITCH_VBAT. LDO_VSYS is enabled when Vsys is generated from Vbus and SWITCH_VBAT is enabled when Vsys is generated from Vbat.

LDO_VSYS is dependent on the bandgap for a voltage reference and a stable 1 µA reference. Its supply is Vbus. The output voltage of LDO_VSYS is set to 4.8 V. LDO_VSYS can only be enabled when Vbus > Vbat and has a configurable current limit to set the maximum current drawn from Vbus, it is programmable from 0 to 1 A with 10 mA steps.

SWITCH_VBAT is biased by a 10 nA current reference and its supply is Vbat. The quiescent current of SWITCH_VBAT is low (~40 nA) as it is on during sleep.

The maximum current that can be drawn from Vsys is 1 A, therefore the maximum R_{ON} from Vbat to Vsys is 0.3 Ω, while the maximum R_{ON} from Vbus to Vsys is 0.5 Ω.

NOTE
A user should always make sure that VSYS level (POWER_LVL_REG[VSYS_LEVEL]) is always higher than V_CHARGE level + 200 mV (CHARGER_VOLTAGE_PARAM_REG[V_CHARGE]).

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6.2.6 Low Power Clamps

The Low Power Clamps (LPCs) consists of two clamps, namely CLAMP_V30 and CLAMP_V12. The clamps do not use a voltage reference and are biased with 10 nA current. The CLAMP_V12 supplies the PD_AON during hibernation and cold boot. The CLAMP_V30 is used to generate the supply for the bandgap block during cold boot. The CLAMP_V30 is controlled by hardware, whereas CLAMP_V12 is always on. Both clamps can supply an output current of 1 mA.

The clamps are supplied by a max selector that selects either Vbus or Vbat as the supply, whichever is the highest.

6.2.7 Charger

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	×	✓	✓	✓

The battery charger is suitable for charging different types of batteries (Li-phosphate, Li-Co, Li-Mn, NMC, NCA). The charger uses an internal pass-device, which limits the external components to a minimum. Only external buffer capacitors (at VBUS and VBAT) and a temperature-sensor string (NTC + Rseries) are needed.

The charger has a CCCV (Constant Current Constant Voltage) architecture and has battery temperature, chip temperature, and overvoltage protection. Extra safety is obtained by programmable timers which limit the charge time. The charger also fully supports JEITA charging. The programmable charge levels are between 2.9 and 4.8 V while the charge currents can be set between 0.5 to 72 mA (pre-charging) and 5 to 720 mA (normal charging).

Enabling, disabling, and functional states of the charger are controlled by an HW state machine; exceptions and error handling are done via software on an interrupt basis. All the protections and loops for current, voltage, and temperature are autonomous and implemented in hardware. There are status signals towards the system for Charge state (Pre-charge, CC-mode, CV-mode, End of Charge) Die-temp protection, Bat-temp protection, Bat-temp measurement, and Error state. In this way, the software can track what is going on in the charger, but the functionality of the charger doesn't require a time-based software interaction. The charger also has a setting in which the control can be fully taken over by software if desired (Bypass mode).

A battery temperature sense function is embedded, which uses an external NTC resistor (either in the battery pack or on the PCB, to make the charger JEITA compliant. This function determines in which temperature zone the battery is (temperatures are programmable) and for each zone, the charge level and charge current can be programmed (over the full range). If the battery is too cold or too hot it will disable the charging. The internal die-temperature protection disables charging when the measured die temperature exceeds the programmed value.

The essential measurement circuits for measuring the Battery voltage and Charge current are in the internal hardware; the GP_ADC is not needed. The charger uses the bandgap reference voltage (1.2 V) and an internal reference current (also obtained from the bandgap). These references are trimmed in production for optimal accuracy.

The actual charger HW FSM is presented in Figure 18.

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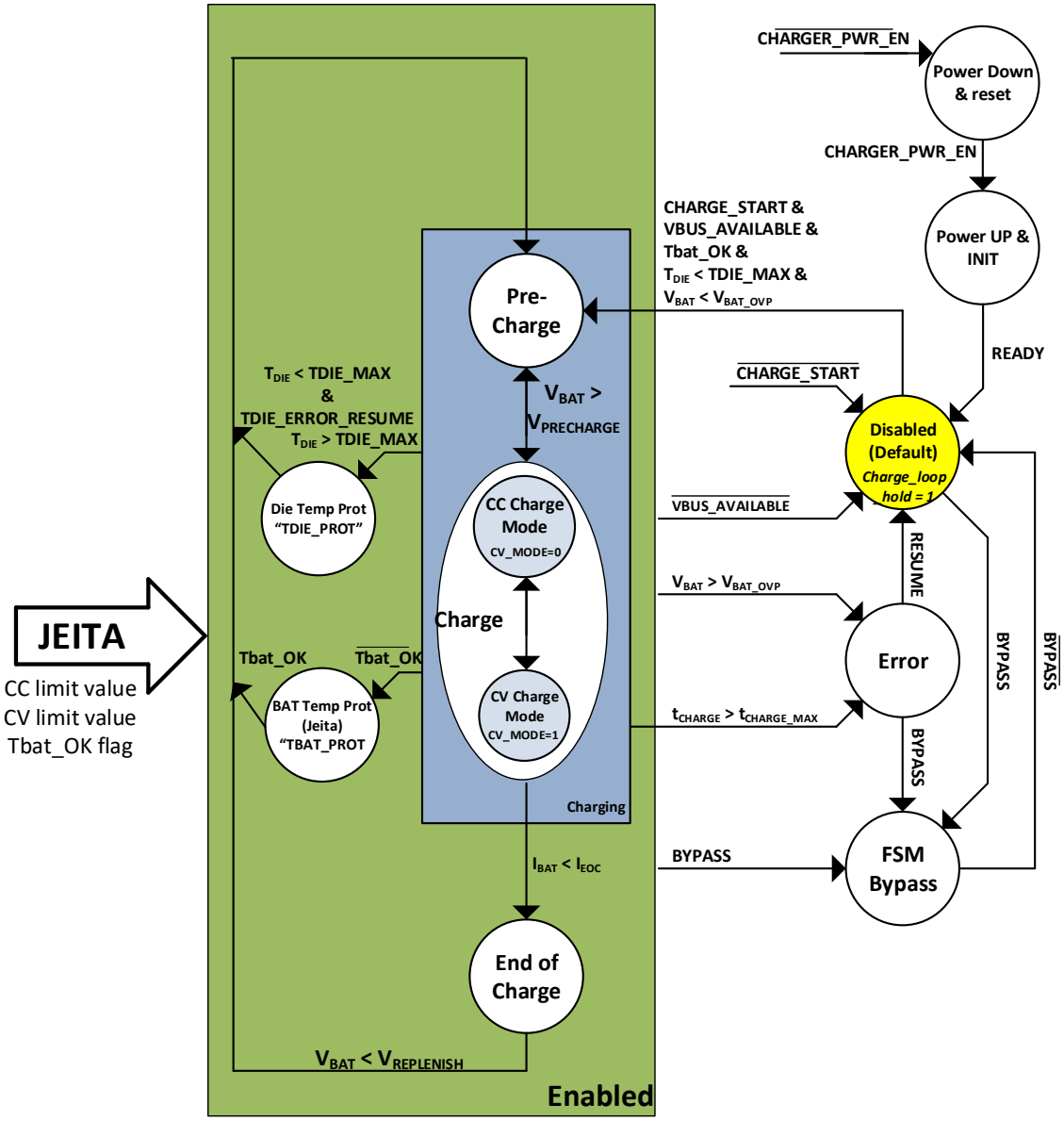

Figure 18: Charger FSM

6.2.7.1 Battery Temperature and JEITA

The JEITA standard defines a battery temperature-dependent charge profile. In the normal temperature range, the charge current and voltage are at the maximum level for the selected battery. Above and below this normal temperature range, there are two ranges in which the current (and optionally voltage) is reduced. At very low and very high battery temperatures, charging is stopped altogether. The battery temperature is determined using the NTC in the battery pack. This NTC is placed in series with an external resistor and a voltage is applied across them, creating a voltage divider. The output of this divider is compared to an internal reference that is created using a programmable resistor ladder that mimics the behavior of the NTC/resistor combination and has programmable taps at ~1 °C intervals. The min and max temperature values can be adapted based on the external R1 resistor (for example, for 12 kΩ R1 resistor the range is from -5 °C to +60 °C). The NTC battery monitoring connections are shown in Figure 19.

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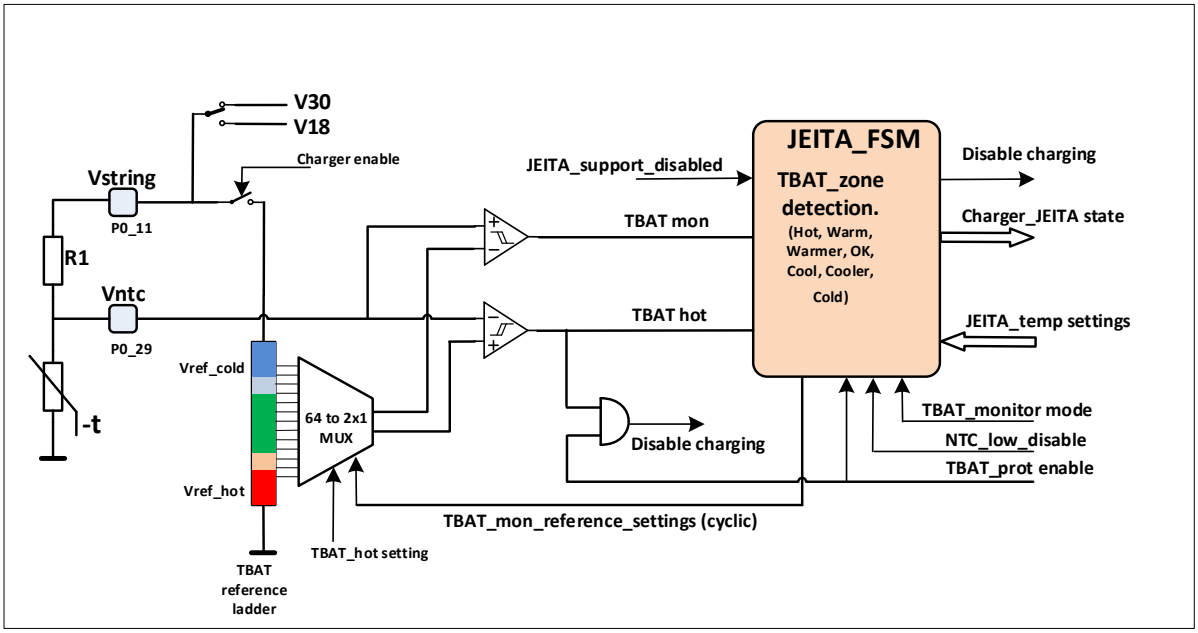

Figure 19: NTC Battery Monitoring Connections

The Battery temperature monitoring FSM (JEITA_FSM) is illustrated in Figure 20.

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Figure 20: Battery Temperature Monitoring FSM

6.2.7.2 Errors and Flags

The following error conditions can be detected:

- Pre-charge timeout
- CC Charge timeout
- CV charge timeout
- Total charge timeout
- Battery over-voltage
- Die temperature protection (error flag but not error state)
- Tbat_HOT and Tbat_COLD: Meaning that the Battery temperature is not OK
- Vbus available: Meaning that VBUS has been removed

The voltage and temperature errors have a direct path to shut down the charger loop. This is done to make these functions robust and independent of logic and the clock.

The error flags are debounced before triggering a state change. Moreover, dedicated error handling routines can start on the assertion of these debounced signals.

Table 86 describes the error flags and when they are asserted.

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Table 86: Charger Error Interrupts

Error IRQ	When	Remarks
TBAT_ERROR	Battery temperature is either “HOT” or “COLD”.	External NTC sensor needed; Activated by “TBAT_PROT_ENABLE”. An error directly disables charging (direct hardware path).
TDIE_ERROR	Die temperature above the threshold.	Protection can be disabled by making “TDIE_PROT_ENABLE” = 0. An error directly disables charging (direct hardware path).
VBAT_OVP_ERROR	Battery voltage above OVP-level.	Protection cannot be disabled. An error directly disables charging (direct hardware path).
TOTAL_CHARGE_TIMEOUT	Total time, spent in charge modes exceeds the programmed maximum time.	Maximum time can be set in the range from 1 to 65535 seconds. Effective Charge time can be different from the counted time when “CHARGE_TIMERS_HALT_ENABLE” is 0 or 1.
CV_CHARGE_TIMEOUT	Time, spent in CV mode exceeds the programmed maximum time.	Maximum time can be set in the range from 1 to 32767 seconds. Effective Charge time can be different from the counted time when “CHARGE_TIMERS_HALT_ENABLE” is 0 or 1.
CC_CHARGE_TIMEOUT	Time, spent in CC mode exceeds the programmed maximum time.	Maximum time can be set in the range from 1 to 32767 seconds. Effective Charge time can be different from the counted time when “CHARGE_TIMERS_HALT_ENABLE” is 0 or 1.
PRECHARGE_TIMEOUT	Time, spent in the PRECHARGE mode exceeds the programmed maximum time.	Maximum time can be set in the range from 1 to 32767 seconds. Effective Charge time can be different from the counted time when “CHARGE_TIMERS_HALT_ENABLE” is 0 or 1.

The flags are debounced with 1 MHz clock.

Upon a timeout or overvoltage or a Vbus problem, the FSM goes to the “Error” state. At this point the charger is disabled, and an IRQ is generated. An interrupt status register contains information on which error occurred to trigger the IRQ.

6.2.7.3 Timers

Four timers are running on a base clock of 1 Hz:

- Total charge time is up to 10.5 hours; for this reason, it is 16 bits
- Pre-charge time is up to 6 hours; for this reason, it is 15 bits
- CC mode charge time is up to 6 hours; for this reason, it is 15 bits
- CV mode charge time is up to 6 hours; for this reason, it is 15 bits

Timers are cleared in EoC when leaving the DISABLED state.

6.2.7.4 Interrupts

There are interrupts generated for each transition in the FSM regarding normal charging. This is done to make it possible for the software to monitor the charging process and take action when this is needed for the application.

Table 87 gives an overview of these “CHARGER_STATE_IRQ” signals:

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Table 87: Overview of Charger State Transition Interrupts

State IRQ	When	Remarks
CV_TO_PRECHARGE	“1” when charger FSM switches from CV_CHARGE to PRE_CHARGE	This transfer is unlikely to happen under normal conditions.
CC_TO_PRECHARGE	“1” when charger FSM switches from CC_CHARGE to PRE_CHARGE	Happens when the battery voltage drops below the V_PRECHARGE level.
CV_TO_CC	“1” when charger FSM switches from CV_CHARGE to CC_CHARGE	Happens when the battery voltage drops and the CC loop becomes dominant.
TBAT_STATUS_UPDATE	“1” when the battery temperature monitoring FSM has been checked and the TBAT_STATUS register field has been updated.	TBAT_STATUS does not need to be changed; it is just refreshed (could be refreshed with the same value).
TBAT_PROT_TO_ PRECHARGE	“1” when charging is resumed because the battery temperature is recovered from a HOT or COLD condition.	TBAT_PROT_ENABLE needs to be high and for COLD condition, NTC_LOW_DISABLE must be low.
TDIE_PROT_TO_ PRECHARGE	“1” when charging is resumed from a die-temperature error condition.	TDIE_PROT_ENABLE and TDIE_ERROR_RESUME need to be high.
EOC_TO_PRECHARGE	“1” when charging is resumed from out of the EOC state.	Happens when the battery voltage drops below the V_REPLENISH level.
CV_TO_EOC	“1” when charger FSM has moved from CV_CHARGE to EOC.	Happens when the charge current drops below the programmed EOC level.
CC_TO_EOC	“1” when charger FSM switches from CC_CHARGE to EOC.	This transfer is very unlikely to happen under normal conditions.
CC_TO_CV	“1” when the charger FSM has moved from CC_CHARGE to CV_CHARGE.	Happens when the battery voltage rises and the CV loop becomes dominant.
PRECHARGE_TO_CC	“1” when the charger FSM moves from PRECHARGE to CC_CHARGE	Happens when the battery voltage rises above the programmed V_PRECHARGE level.
DISABLED_TO_ PRECHARGE	“1” when charger FSM moves from the DISABLED state to PRECHARGE.	There may be no voltage or temperature error conditions, VBUSAVAILABLE and CHARGE_START must be high.

6.2.7.5 Charger Registers Protection

This block implements a mechanism to protect the battery charger settings to avoid out-of-spec charging which may lead to the physical breakdown of the system. The charger settings must be protected from firmware writing out-of-spec values to the V-I-T parameters of the charger.

There are two levels of protection implemented:

- **Permanent protection.** This level locks write access to specific registers once and for all
- **Flexible protection.** This level allows for locking/unlocking specific registers by programming special sequences of words. It only applies to registers not hardened by the Permanent Protection

The overall architecture for the protection mechanism is presented in Figure 21.

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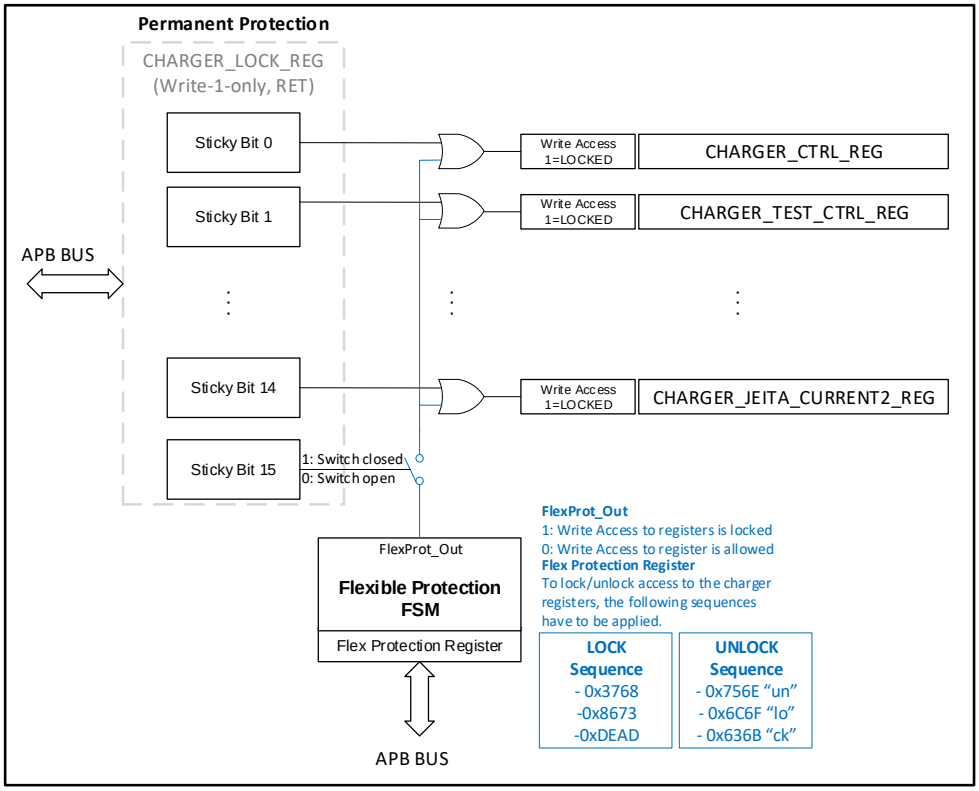

Figure 21: Charger Protection Mechanism Diagram

There is a state machine that evaluates any data written into the CHARGER_SWLOCK_REG address. If the data values conform to the sequence as illustrated in Figure 21, then the FSM asserts a signal (FlexProt_Out) designating lock/unlock. Note that, this signal is asserted, meaning that the registers become by default software protected as soon as the "Sticky" bit 15 of CHARGER_LOCK_REG is also set to 1.

Sticky-bit 15 is used to permanently enable flexible protection. That enables programming the registers at boot time by the Configuration Script (CS), then enables flexible protection (which is by default activated).

6.2.8 Charger Detection

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	×	✓	✓	✓

The USB controller has built-in hardware to determine the charger type to which it is connected. Depending on the charger type, battery state, and USB connection state, a defined current can be drawn from the charger. The main features of the charger detection circuit are listed below:

- Complies to "Battery Charging Specification" Revision V1.2 December 7, 2010 (BC1.2)
- Charger type detection: Dedicated Charging Port (DCP), Charging Downstream Port (CDP), Standard Downstream Port, PS2 port, and Proprietary charger
- Dead battery provision
- Compatible with various smartphone chargers

The details of the charger detection circuit are shown in Figure 22.

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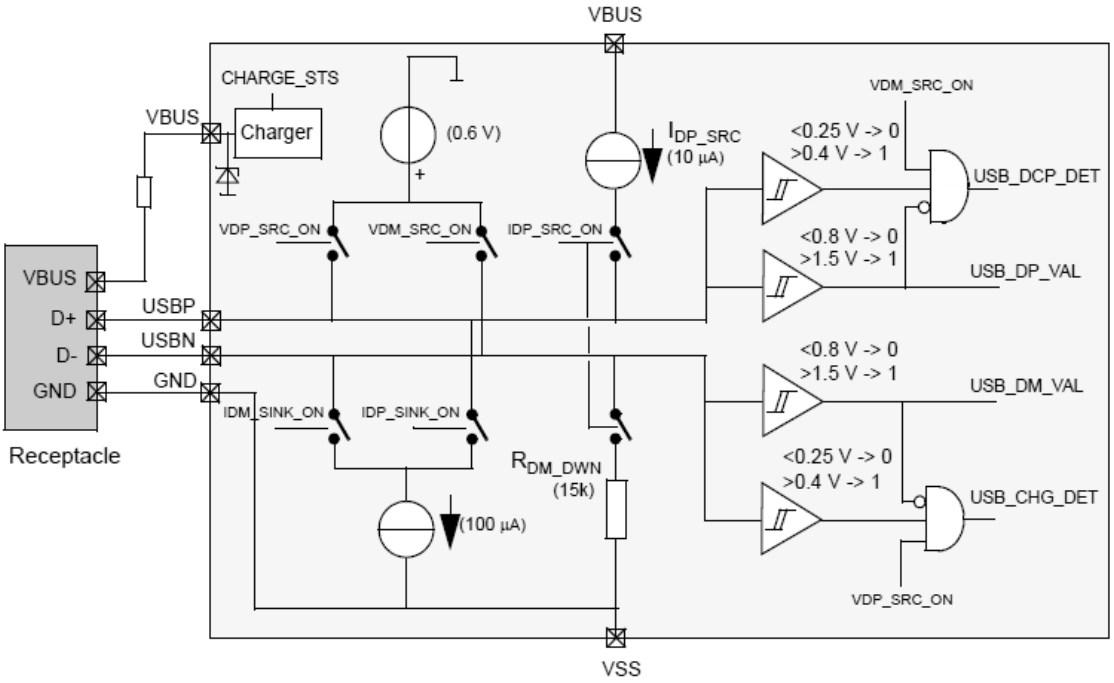

Figure 22: Charger Detection Circuit

The USB interface supports battery charging with the following hardware blocks as shown in Figure 22:

- A voltage source of 0.6 V can be switched to USBP or USBN with CHG_DET_SW_CTRL_REG bits VDP_SRC_ON resp. VDM_SRC_ON
- A current sink of 100 uA can be switched to USBP or USBN with CHG_DET_SW_CTRL_REG bits IDP_SINK_ON resp. IDM_SINK_ON. (Note that internal logic prevents both switches from being enabled at the same time)
- A current source I_{DP_SRC} and R_{DM_DWN} can be enabled with bit IDP_SRC_ON of the CHG_DET_SW_CTRL_REG
- A logic level Schmitt trigger is used for USBN, USBP read in USB_CHARGER_STAT_REG bits USB_DM_VAL, resp. USB_DP_VAL logic level (0: <0.8 V 1: >2 V)
- A comparator output CHG_DET read in USB_CHARGER_STAT_REG[USB_CHG_DET] to detect a level of 0.4 V < USBN < 1.5 V to indicate that a DCP or CDP is connected
- A comparator output DCP_DET read in USB_CHARGER_STAT_REG[USB_DCP_DET] to detect a level of 0.4 V < USBP < 1.5 V to indicate that a DCP is connected

Initially, all bits of CHG_DET_SW_CTRL_REG must be set to reset value 0.

The presence of VBUS can be checked by reading bit ANA_STATUS_REG[VBUS_AVAILABLE].

The charger detection hardware can operate in polling mode or can generate a USB interrupt to the Cortex-M33. A change in one of the bits [3:0] of register USB_CHARGER_STAT_REG sets bits USB_MAEV_REG[USB_CH_EV] if the corresponding bits [7:4] are set to 1. If USB_CHARGER_STAT_REG is read, bit USB_CH_EV interrupt is cleared. The interrupt “set” conditions have priority over the “clear” condition of the read access.

6.2.8.1 Contact Detection

If CHG_DET_SW_CTRL_REG [IDP_SRC_ON] is set, bit USB_CHARGER_STAT_REG[USB_DP_VAL] indicates that the data pins make contact (see Table 88). It is the responsibility of SW to wait until the USBN and USBP contact bouncing is finished before the register is read.

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Table 88: USBP, USBN Contact Detection

Port	USBP	USBN	USB_DP_VAL
Nothing Connected	>1.5 V	0	1
Standard Downstream	<0.8 V	0	0
Dedicated Charger	<0.8 V	<0.8 V	0
Charging Downstream	<0.8 V	<0.8 V	0

6.2.8.2 Primary Charger Detection

Primary charger detection is used to detect whether the downstream port has charging capabilities or not. The detection is initiated by setting bits CHG_DET_SW_CTRL_REG [VDP_SRC_ON] and CHG_DET_SW_CTRL_REG [IDM_SINK_ON]. This enables the voltage source VDP_SRC on USBP and the current source IDM_SINK on USBN. The measured levels on USBP and USBN shown in Table 89 determine the value of bit USB_CHARGER_STAT_REG[USB_CHG_DET].

Table 89: Charger Type Detection

Port	USBP	USBN	USB_CHG_DET
Dedicated Charger	0.6 V	>0.4 V <1.5 V	1
Charging Downstream	0.6 V	First <0.25 V then 0.6 V	0 then 1 after 1 ms – 20 ms
Standard Downstream	0.6 V	2 V	0
PS2	2 V		0

Note that, if the charger detection is done before enabling the charging downstream port V_{DM_SRC} (so before 20 ms), a standard downstream port is detected, which is safe but incorrect. When the V_{DM_SRC} is enabled in the charging downstream port, a charger port is detected.

6.2.8.3 Secondary Charger Detection

Secondary charger detection can be used to distinguish a dedicated charger or a charging downstream port. The detection is initiated by setting bits CHG_DET_SW_CTRL_REG [VDM_SRC_ON] and CHG_DET_SW_CTRL_REG [IDP_SINK_ON]. This enables V_{DM_SRC} and I_{DP_SINK}. The difference between a DCP and a CDP is shown in Table 90.

Table 90: Secondary Charger Detection

Port	USBP	USBN	USB_DCP_DET
Dedicated Charger	>0.4 V <1.5 V	0.6 V	1
Charging Downstream	<0.25 V	0.6 V	0

6.2.8.4 Smartphone Charger Detection

The battery charger detection circuit can detect smartphone chargers with the characteristics shown in Table 91.

Table 91: Smartphone Charger Characteristics

USBP	USBN	Load Current
2.0 V	2.0 V	Up to 500 mA
2.0 V	2.9 V	Up to 1 A
2.9 V	2.0 V	Up to 2 A
2.9 V	2.9 V	Not defined

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The smartphone charger circuit can be enabled by the USB_CHARGE_ON bit of the CHG_DET_SW_CTRL_REG register. The results of the detection are available on the USB_CHARGER_STAT_REG register.

6.2.8.5 Charger Detection HW FSM

The DA1470x includes an HW FSM for the charger detection process. This FSM is responsible to perform the Contact, Primary Contact, and Secondary Contact detections without any software intervention. The Charger detection HW FSM also supports bypass operation for full SW implementation of the detection process. The HW FSM is shown in Figure 23.

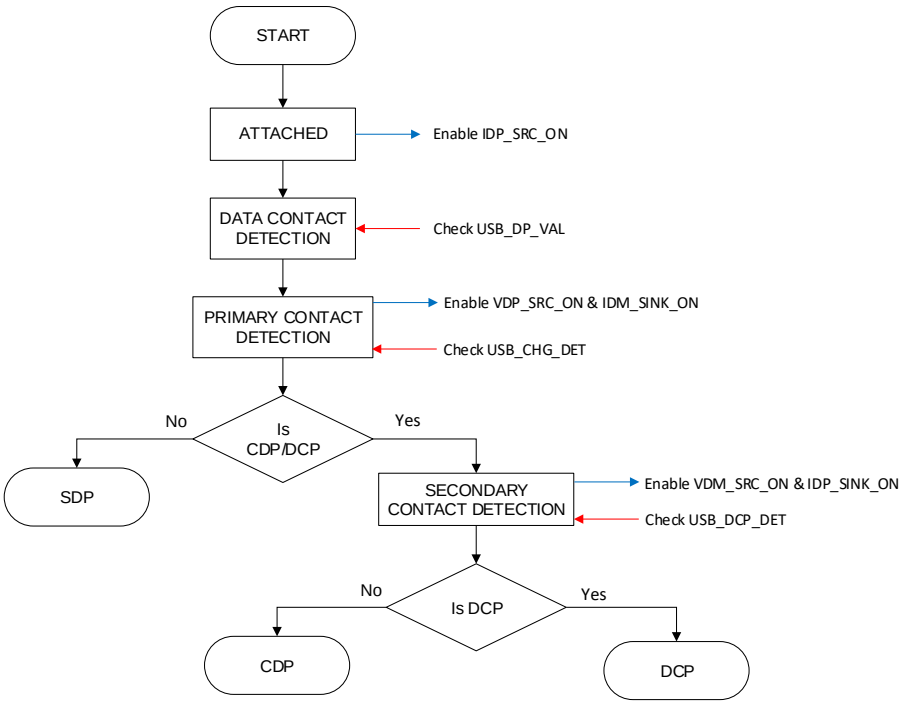

Figure 23: Charger Detection HW FSM

6.2.9 Battery Check

The Battery Check (BATCHECK) features a programmable VBAT load current, which can be used to modulate the battery (Figure 24). The constant load is a programmable current source from 0 to 8 mA in steps of 1 mA. The accuracy is +/-2.7 %. The internal resistance of a battery can be monitored in this way.

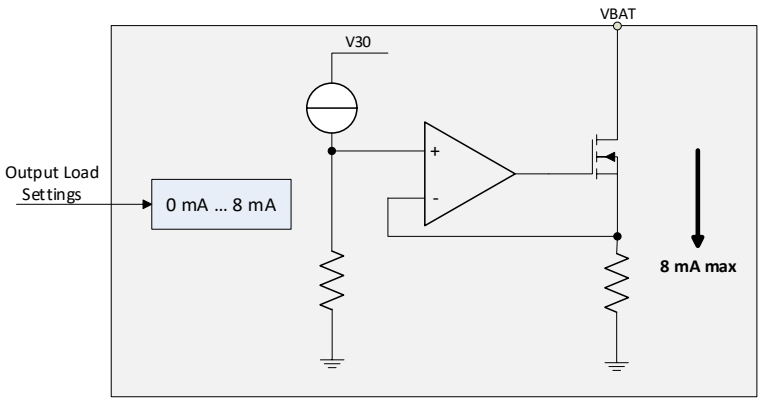

Figure 24: Battery Check Block Diagram

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The Battery Check contains the following functional blocks:

- Output load setting. Input is an accurate reference current from a bandgap; outputs are a number of (mirrored) currents
- High gain op-amp
- Matched resistor network

It provides a reference current, coming from the bandgap, which is mirrored into a selectable output current(s). This current is routed through a resistor, resulting in a reference voltage on the positive input of the op-amp. Due to the negative feedback and the high gain, the op-amp in combination with the output transistor forces the same voltage on the negative input as well as over the output resistor, resulting in the selected output load current.

Register BATCHECK_REG controls the setting, fine-tuning, and feature enablement.

6.2.10 Rails Discharge

The power rails have a software-controlled discharge capability that practically uses multiple NMOS transistors to rapidly discharge the external decoupling capacitors. This feature enables power cycling of the external components when the system is resetting.

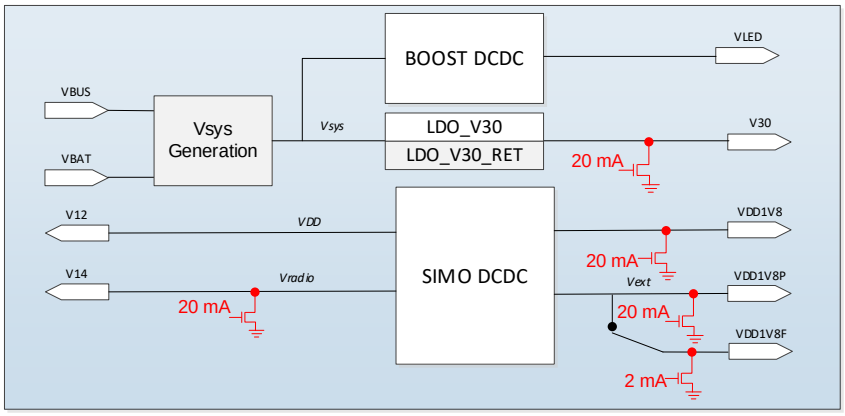

Figure 25: Transistors for Discharging Rails by SW

There is a hardwired configuration for the allowed discharging current of each rail which is either 2 or 20 mA. The proposed configuration for the discharging elements is illustrated in Figure 25.

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7 Power Domain Controller (PDC)

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

7.1 Introduction

The Power Domains Controller (PDC) is a block responsible for taking action after waking up or before going to sleep with regard to the power domains of the system. It follows the Analog PMU FSM for start-up/wake-up and it is preceding the Goto sleep FSM. It is a digital hardware state machine that defines in a flexible and programmable way:

- Which master, power domains, and clocks to activate or enable after a wake-up trigger occurs
- If the system is allowed to go to sleep (switching off everything)

The PDC can be triggered by GPIOs (programmable level, any Px_y), general-purpose timers, RTC, the MAC timer, VBUS or SWD presence, or by a Software trigger issued by one of the three masters of the system (Cortex-M33, CMAC Cortex M0+ or SNC Cortex M0+).

Features

- 16 places of 13-bit words Look-Up Table (LUT) for defining what the system should do upon any wake-up trigger
- Triggers from IOs, internal timers/controllers, or SW
- Triggers from internal diagnostic signals
- Monitors if a power domain is actively used by any master before shutting it down
- Allows the system to go to sleep if all masters' domains are off
- System wake-up can be overridden by accessing the PMU_CTRL_REG

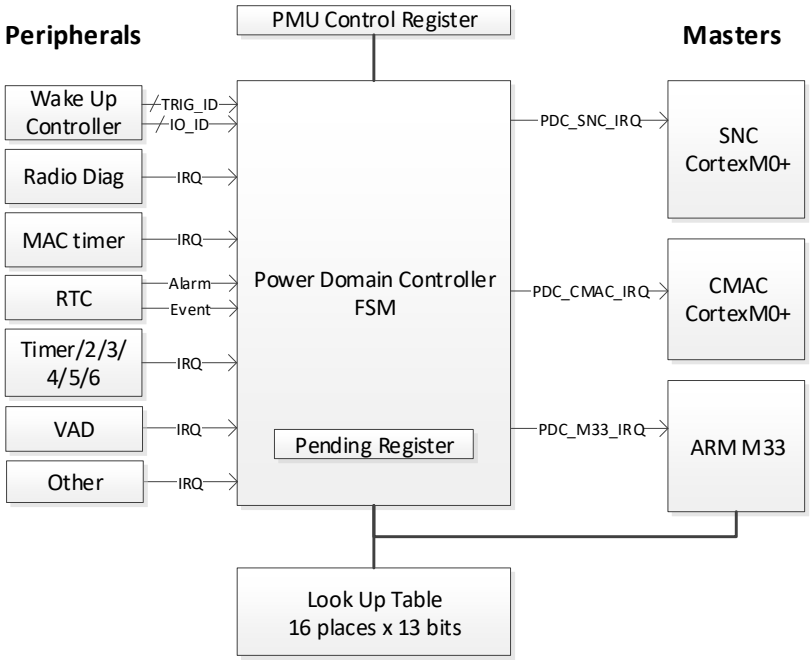

Figure 26: Power Domain Controller Block Diagram

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7.2 Architecture

The Look-Up Table (LUT) is initialized at cold boot by the Cortex-M33. It instructs the PDC which digital power domains to activate based on the triggering source.

The format of the LUT is presented in Table 92.

Table 92: PDC LUT format

	Bit	Function			
Triggers	0	if 0x00 then P0 GPIO	if 0x01 then P1 GPIO	if 0x02 then P2 GPIO	if 0x03 then Peripheral
	1				
	2	Pin_ID	Pin_ID	Pin_ID	Periph_ID0
	3	Pin_ID	Pin_ID	Pin_ID	Periph_ID1
	4	Pin_ID	Pin_ID	Pin_ID	Periph_ID2
	5	Pin_ID	Pin_ID	Pin_ID	Periph_ID3
	6	Pin_ID	Pin_ID	Pin_ID	Periph_ID4
What to Do	7	Enable XTAL32M			
	8	Enable PD_TMR			
	9	Reserved			
	10	Enable PD_SNC (Needed for using the serial interfaces)			
	11	Wake-up Master_ID			
	12	Wake-up Master_ID			

The depth of the LUT is 16 places, so the system supports up to 16 different wake-up configurations but could be changed dynamically by application software.

Four different trigger types are evaluated when a trigger comes according to the value on bit0 and bit1 of each LUT entry:

- If Bits [1:0] = 00 then it is a GPIO toggle from P0. Bits [6:2] contain the pin number that triggered
- If Bits [1:0] = 01 then it is a GPIO toggle from P1. Bits [6:2] contain the pin number that triggered
- If Bits [1:0] = 10 then it is a GPIO toggle from P2. Bits [6:2] contain the pin number that triggered
- If Bits [1:0] = 11 then it is a trigger from some peripheral. Bits [6:2] define the peripheral according to Table 93

Table 93: Peripheral Trigger Encoding

ID (Decimal)	Peripheral
0	Timer
1	Timer2
2	Timer3
3	Timer4
4	Timer5
5	Timer6
6	RTC Alarm/Rollover
7	RTC Timer
8	MAC Timer || SYS2CMAC_IRQ

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ID (Decimal)	Peripheral
9	VAD
10	XTAL32MRDY_IRQ
11	RFDIAG_IRQ
12	VBUS Present IRQ || Debounced IO || JTAG IRQ
13	CMAC2SYS_IRQ
14	SNC2SYS_IRG
15	Software Trigger
16	GPIO P0
17	GPIO P1
18	GPIO P2
19	CMAC2SNC_IRQ
20	SNC2CMAC_IRQ
21	SYS2CMAC_IRQ
22	SYS2SNC_IRQ
23	SYS2SNC_IRQ || CMAC2SNC_IRQ
24	SNC2SYS_IRQ || CMAC2SYS_IRQ
25- 31	Reserved

The IDs 16, 17, and 18 are indicating that an OR of the specific GPIO port is the trigger for an action. That OR also respects the mask register of the wake-up controller before generating the respective signal towards the PDC.

Bits [12:7] explain what needs to be done upon a trigger from the triggering sources as explained so far. More specifically, a triggering source might request to:

- Enable the XTAL32MHz. This bit is set if clock precision is required by the application (for example, Bluetooth® LE operation, USB operation which needs the PLL48, and high-performance mode which needs the PLL160). Note that, the PDC state machine only enables the XTAL32MHz block but switching the system clock to the XTAL32M is not done. This has to be done by software. Since multiple masters might want to switch to XTAL32, switching to this clock can be done by any master but switching back should not be allowed. Turning off the XTAL32M is done automatically when the system enters deep sleep
- Enable PD_TMR or PD_SNC. The PD_SNC is needed for using the serial interfaces. The PD_MEM is always enabled since all masters are using this power domain. This can be used if the M33 needs to access a serial interface in the PD_SNC without woken up the ARM Cortex M0+ in the PD_SNC
- Issue a wake-up IRQ/Signal to any other master. Hence a master can wake up another master with the use of a LUT entry. The master encoding is presented in Table 94

Table 94: PDC Masters Encoding

ID	Master
0	Reserved
1	Cortex M33
2	CMAC M0+
3	SNC M0+

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Note that when the SW trigger is used, a master that wants to wake up another master should write (SW) to the internal (PDC) register storing the PENDING directly rather than trigger interrupt lines. The PENDING register is protected with a SET hardware mechanism to avoid race conditions. The usage of activating the PDC PENDING register through the SW trigger is limited to a specific PDC entry. By using triggers 19-24 (see Table 93) any master can trigger the other two through the PDC, by using the SYS_IRQ_CTRL_REG.

7.2.1 Operation

The PDC re-evaluates all available information every time there is a trigger input. It does the same every time there is feedback from one of the three masters indicating that they have finished what they were triggered to do. The latter is implemented using signaling between the masters and the PDC. A sleep signal coming from Cortex-M33, SNC, or CMAC is asserted when the CPU SCR bit is set and the WFI command is executed.

Every time a trigger occurs, the PDC follows the action plan as programmed in the LUT. It also asserts the respective bit number in the PENDING register that keeps one bit per LUT entry (for example, if LUT entry #2 was triggered, PENDING[2] will also be asserted). The master that has been woken up, acknowledges the PENDING bit and after finishing its tasks, it notifies the PDC that any request for power domains activation is not valid anymore. The PDC cross-checks the complete LUT to see if there is any other active entry that still uses any of the power domains requested. If not, these power domains are shut down. If other masters still use one of the domains, then it does not allow this domain to be powered down.

Note that, the PENDING register should be acknowledged as soon as possible and well before issuing a WFI command.

If there is no active LUT entry where one of the three masters is still up and running, then the PDC allows the system to go to sleep (for example, invoke the Analog PMU FSM). Any power domain can be turned off, depending on the value of the respective field in the PMU_CTRL_REG. Hence, if for example, PMU_CTRL_REG[RADIO_SLEEP] = 1 then given the fact that no LUT entry is active, the power domain is turned off.

7.3 Programming

There is a simple sequence of steps that needs to be followed to program and use the Power Domain controller:

1. Add a PDC entry by writing the PDC_CTRLx_REG:
   a. Select Trigger (TRIG_SELECT):
      i. 0: Trigger is a GPIO on Port 0 (selectable through Wake-Up Controller).
      ii. 1: Trigger is a GPIO on Port 1 (selectable through Wake-Up Controller).
      iii. 2: Trigger is a GPIO on Port 2 (selectable through Wake-Up Controller).
      iv. 3: Trigger is another Master (see register description).
   b. Select Trigger ID (TRIG_ID).
   c. Enable extra options if needed (EN_SNC, EN_TMR, EN_XTAL).
   d. Select the master to wake up (PDC_MASTER):
      i. 0: PDC entry is disabled.
      ii. 1: Wake up Arm Cortex M33.
      iii. 2: Wake up CMAC.
      iv. 3: Wake up Sensor Node Controller.
2. Check if a PDC entry has been triggered (PDC_PENDING_REG).
   a. If needed check the register for a specific master (PDC_PENDING_CM33_REG, PDC_PENDING_CMAC_REG, or PDC_PENDING_SNC_REG).
3. If needed, trigger a PDC by SW (PDC_SET_PENDING_REG).
4. Clear any pending requests and/or IRQs (PDC_ACKNOWLEDGE_REG).

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8 Brown-Out Detector

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

8.1 Introduction

The brown-out detector (BOD) is a voltage monitoring circuit that triggers an HW reset if supply voltages go below a certain threshold.

The BOD is active in either Active or Sleep mode with periodically a programmable interval (PMU_SLEEP_REG[BOD_SLEEP_INTERVAL]).

While the system is in any sleep mode, the detector is regularly activated for a voltage comparison of the supply sources after which it goes in sleep mode again. The amount of time BOD is active is one sleep clock period.

Features

- Comparator based implementation
- Independent voltage monitoring of all power rails
- Periodic detection mechanism, available during active and sleep periods
- Programmable VSYS, V12 (VDD), V14, V18, and V30 levels
- Different programmable levels for sleep and active modes for V12 (VDD) and V30

8.2 Architecture

The BOD is implemented with several comparators. In the hibernation mode, every comparator, except the vbus_plugin, is off, while in sleep mode operation, the comparators operate on a low enough speed such that the current consumption is a very small fraction of the total leakage current of the system.

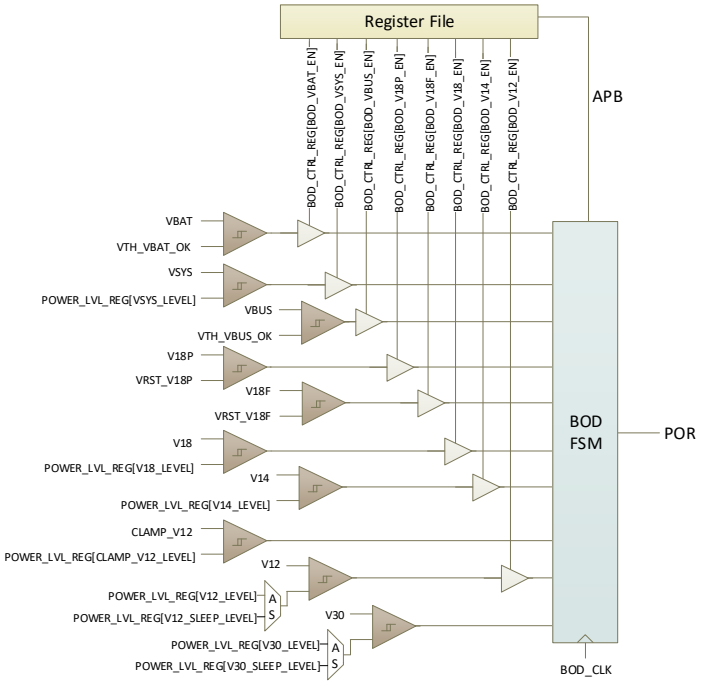

Figure 27: BOD Block Diagram

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The VSYS, V18, V14, V12 (VDD), and V30 levels in the BOD are programmable through the POWER_LVL_REG register, with reset values shown in Table 95.

Table 95: BOD Levels – Reset Values

Rail	Reset Value (V)
VSYS	4.8
V18	1.8
V14	1.4
V12_SLEEP	0.9
V12	1.2
V30_SLEEP	3.0
V30	3.0

The thresholds for the non-programmable rails are shown in the electrical characteristics table of the BOD.

NOTE
Since V18P and V18F rails are externally connected, the BOD sense to those rails should be enabled or disabled at the same time.

8.3 Programming

There is a simple sequence of steps that needs to be followed to configure the Brown-Out Detector:

1. Set up the interval when Brown Out Detection is activated to check on the power rails voltage (PMU_SLEEP_REG[BOD_SLEEP_INTERVAL]).
2. Configure the BOD voltage levels for the chosen power rails (POWER_LVL_REG).
3. Enable the BOD monitoring for the chosen power rails (BOD_CTRL_REG[BOD_xxxx_EN]).

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9 Reset

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

9.1 Introduction

The DA1470x has an RSTN pad which is active low. It contains an RC filter for spikes suppression with 400 kΩ resistor and a 2.8 pF capacitor. It also includes a 25 kΩ pull-up resistor. This pad should be driven externally using a FET or a single button connected to Ground. The typical latency of the RSTN pad is about 2 µs.

Additionally, a configurable Power-on Reset circuitry is included, to allow for a programmable time delayed POR functionality from a configurable reset source. By default, this circuitry is connected to the RSTN pin, but SW can remap it to any GPIO.

A software reset is available. This is done by either programming a specific register or triggering it via the debugger interface.

Features

- RC spike filter on RSTN to suppress external spikes (400 kΩ, 2.8 pF)
- Three different reset lines (SW, HW, and POR)
- Reset cause is latched in a specific register
- Configurable POR circuitry

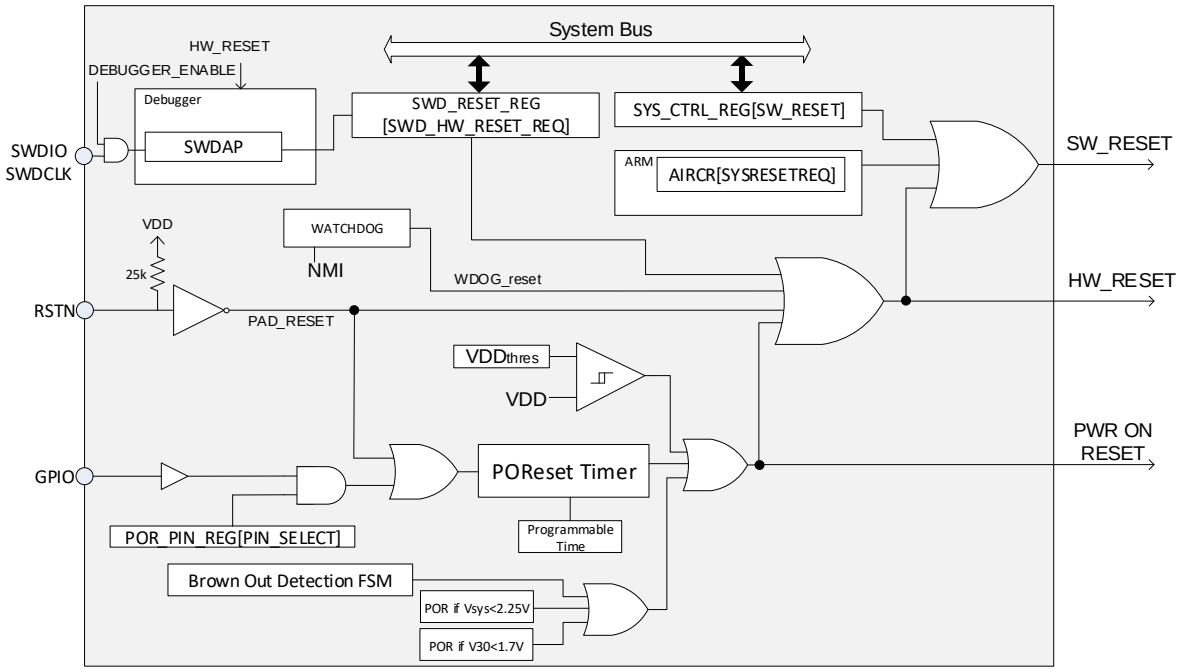

Figure 28: Reset Block Diagram

There are three main reset signals in the DA1470x:

- The PWR ON reset, triggered by a GPIO set as POR source with selectable polarity and/or the RSTN pad, after a programmable time delay
- The HW reset, triggered by the RSTN pad when it becomes active for a short period (less than the programmable delay for POR)

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- The SW reset, triggered by writing the SYS_CTRL_REG[SW_RESET] bit or Arm's AIRCR[SYSRESETREQ] register

9.2 Architecture

The Power-on Reset (POR) signal is generated as follows:

- Internally; it will release the system's flip flops as soon as the VDD voltage crosses the minimum threshold value
- Brown-Out Detection FSM senses the various internal voltage levels to be higher than the programmed thresholds. There are two additional POR signals which are triggered if the Vsys or V30 voltages cross the minimum threshold values
- Externally by a Power-on Reset source (RSTN pad or GPIO)

The HW reset can be automatically triggered at system wakeup from the Extended or Deep Sleep mode by programming bit PMU_CTRL_REG[RESET_ON_WAKEUP]. The PWR ON reset and the HW reset run the power-up sequence and the BootROM code is executed.

The SW reset is the logical OR of a signal from the Arm CPU (triggered by writing SCB->AIRCR = 0x05FA0004), and the SYS_CTRL_REG[SW_RESET] bit. This is mainly used to reboot the system after the base address is remapped.

Certain registers are reset only by Power-on Reset, HW Reset, or SW Reset only. These registers that reset with specific reset are listed in Table 96. Note that with the Power-on Reset all the POR Reset, HW Reset, and SW Reset registers will be reset, with the HW Reset only the HW and SW Reset registers will be reset and with SW Reset only the SW Reset registers will be reset. Furthermore, there are three bit-fields in the RESET_STAT_REG which will be reset with a watchdog event (reset).

Table 96: Reset Signals and Registers

Reset Source	Registers
POR Reset	BANDGAP_REG CLK_RTCDIV_REG CLK_XTAL32K_REG POR_CTRL_REG POR_PIN_REG POR_TIMER_REG POWER_LVL_REG RST_CTRL_REG RTC_CONTROL_REG RTC_EVENT_CTRL_REG RTC_KEEP_RTC_REG RTC_PDC_EVENT_PERIOD_REG SYS_STAT_REG[POWER_IS_UP]
HW Reset	BIAS_VREF_SEL_REG BOD_CTRL_REG CACHE_CTRL2_REG[CACHE_FLUSHED] CACHE_CTRL2_REG[CACHE_FLUSH_DISABLE] CACHE_CTRL2_REG[CACHE_USE_FULL_DB_RANGE] CACHE_CTRL2_REG[CACHE_MHCLKEN_DISABLE] CACHE_CTRL2_REG[CACHE_CWF_DISABLE] CACHE_CTRL2_REG[CACHE_WEN] CACHE_CTRL2_REG[CACHE_LEN]

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Reset Source	Registers
	CACHE_FLASH_REG CHARGER_CTRL_REG CHARGER_CC_CHARGE_TIMER_REG[MAX_CC_CHARGER_TIME] CHARGER_CURRENT_PARAM_REG CHARGER_ERROR_IRQ_MASK_REG CHARGER_JEITA_CURRENT_REG CHARGER_JEITA_CURRENT2_REG CHARGER_JEITA_V_CHARGE_REG CHARGER_JEITA_V_OVP_REG CHARGER_JEITA_V_PRECHARGE_REG CHARGER_JEITA_V_REPLENISH_REG CHARGER_LOCK_REG CHARGER_PRE_CHARGE_TIMER_REG[MAX_PRE_CHARGE_TIME] CHARGER_PWR_UP_TIMER_REG[CHARGER_PWR_UP_SETTLING] CHARGER_STATE_IRQ_MASK_REG CHARGER_TBAT_COMP_TIMER_REG[TBAT_COMP_SETTLING] CHARGER_TDIE_COMP_TIMER_REG[TDIE_COMP_SETTLING] CHARGER_THOT_COMP_TIMER_REG[THOT_COMP_SETTLING] CHARGER_TEMPSET_PARAM_REG CHARGER_TEMPSET2_PARAM_REG CHARGER_TOTAL_CHARGE_TIMER_REG[MAX_TOTAL_CHARGE_TIME] CHARGER_VBAT_COMP_TIMER_REG[VBAT_COMP_SETTLING] CHARGER_VOLTAGE_PARAM_REG CHARGER_VOVP_COMP_TIMER_REG[OVP_INTERVAL_CHECK_THRES] CHARGER_VOVP_COMP_TIMER_REG[VBAT_OVP_COMP_SETTLING] CLK_AMBA_REG CLK_CMAC_SWITCH_REG CLK_CTRL_REG CLK_RADIO_REG CLK_RCHS_REG CLK_RCLP_REG CLK_RCX_REG DCACHE_BASE_ADDR_REG DCACHE_CTRL_REG DEBUG_REG OQSPIF_BURSTBRK_REG OQSPIF_BURSTCMDA_REG OQSPIF_BURSTCMDB_REG OQSPIF_CHCKERASE_REG OQSPIF_CTR_CTRL_REG OQSPIF_CTR_EADDR_REG OQSPIF_CTR_KEY_0_3_REG OQSPIF_CTR_KEY_4_7_REG OQSPIF_CTR_KEY_8_11_REG OQSPIF_CTR_KEY_12_15_REG OQSPIF_CTR_KEY_16_19_REG OQSPIF_CTR_KEY_20_23_REG OQSPIF_CTR_KEY_24_27_REG

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Reset Source	Registers
	OQSPIF_CTR_KEY_28_31_REG OQSPIF_CTR_NONCE_0_3_REG OQSPIF_CTR_NONCE_4_7_REG OQSPIF_CTR_SADDR_REG OQSPIF_CTRLBUS_REG OQSPIF_CTRLMODE_REG OQSPIF_DUMMYDATA_REG OQSPIF_ERASECMDA_REG OQSPIF_ERASECMDB_REG OQSPIF_ERASECMDC_REG OQSPIF_ERASECTRL_REG OQSPIF_GP_REG OQSPIF_READDATA_REG OQSPIF_RECVDATA_REG OQSPIF_STATUS_REG OQSPIF_STATUSCMD_REG OQSPIF_WRITEDATA_REG OTPC_MODE_REG OTPC_PADDR_REG OTPC_PWORD_REG OTPC_STAT_REG OTPC_TIM1_REG OTPC_TIM2_REG P0_PAD_LATCH_REG P0_RESET_PAD_LATCH_REG P0_SET_PAD_LATCH_REG P1_PAD_LATCH_REG P1_RESET_PAD_LATCH_REG P1_SET_PAD_LATCH_REG P2_PAD_LATCH_REG P2_RESET_PAD_LATCH_REG P2_SET_PAD_LATCH_REG PDC_ACKNOWLEDGE_REG PDC_CTRL0_REG PDC_CTRL1_REG PDC_CTRL2_REG PDC_CTRL3_REG PDC_CTRL4_REG PDC_CTRL5_REG PDC_CTRL6_REG PDC_CTRL7_REG PDC_CTRL8_REG PDC_CTRL9_REG PDC_CTRL10_REG PDC_CTRL11_REG PDC_CTRL12_REG PDC_CTRL13_REG PDC_CTRL14_REG

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Reset Source	Registers
	PDC_CTRL15_REG
	PDC_PENDING_CM33_REG
	PDC_PENDING_CMAC_REG
	PDC_PENDING_REG
	PDC_PENDING_SNC_REG
	PDC_SET_PENDING_REG
	PLL_SYS_CTRL1_REG
	PLL_SYS_CTRL2_REG
	PLL_SYS_CTRL3_REG
	PLL_SYS_STATUS_REG
	PLL_USB_CTRL1_REG
	PLL_USB_CTRL2_REG
	PLL_USB_CTRL3_REG
	PLL_USB_STATUS_REG
	PMU_CTRL_REG
	PMU_SLEEP_REG
	POWER_CTRL_REG
	QSPIC_AWRITECMD_REG
	QSPIC_BURSTBRK_REG
	QSPIC_BURSTCMDA_REG
	QSPIC_BURSTCMDB_REG
	QSPIC_CHCKERASE_REG
	QSPIC_CTRLBUS_REG
	QSPIC_CTRLMODE_REG
	QSPIC_DUMMYDATA_REG
	QSPIC_ERASECMDA_REG
	QSPIC_ERASECMDB_REG
	QSPIC_ERASECTRL_REG
	QSPIC_MEMBLEN_REG
	QSPIC_READDATA_REG
	QSPIC_RECVDATA_REG
	QSPIC_STATUS_REG
	QSPIC_STATUSCMD_REG
	QSPIC_WRITEDATA_REG
	QSPIC2_AWRITECMD_REG
	QSPIC2_BURSTBRK_REG
	QSPIC2_BURSTCMDA_REG
	QSPIC2_BURSTCMDB_REG
	QSPIC2_CHCKERASE_REG
	QSPIC2_CTRLBUS_REG
	QSPIC2_CTRLMODE_REG
	QSPIC2_DUMMYDATA_REG
	QSPIC2_ERASECMDA_REG
	QSPIC2_ERASECMDB_REG
	QSPIC2_ERASECTRL_REG
	QSPIC2_MEMBLEN_REG
	QSPIC2_READDATA_REG
	QSPIC2_RECVDATA_REG

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Reset Source	Registers
	QSPIC2_STATUS_REG QSPIC2_STATUSCMD_REG QSPIC2_WRITEDATA_REG RAM_PWR_CTRL_REG RESET_STAT_REG[SWD_HWRESET_STAT] RESET_STAT_REG[HWRESET_STAT] SECURE_BOOT_REG SW_V18F_REG SWD_RESET_REG SYS_CTRL_REG SYS_STAT_REG USB_RXC2_REG[USB_FLUSH] VSYS_GEN_CTRL_REG VSYS_GEN_IRQ_CLEAR_REG VSYS_GEN_IRQ_MASK_REG VSYS_GEN_IRQ_STATUS_REG WATCHDOG_REG[WDOG_VAL_NEG] WATCHDOG_REG[WDOG_VAL] WATCHDOG_CTRL_REG XTAL32M_CAP_MEAS_REG XTAL32M_CTRL_REG XTAL32M_FSM_REG XTAL32M_IRQ_CTRL_REG XTAL32M_IRQ_STAT_REG XTAL32M_SETTLE_REG XTAL32M_START_REG XTAL32M_STAT0_REG XTAL32M_TRIM_REG[XTAL32M_CMP_LVL] XTAL32M_TRIM_REG[XTAL32M_AMPL_SET] XTAL32M_TRIM_REG[XTAL32M_CUR_SET]
Watchdog Reset	RESET_STAT_REG[CMAC_WDOGRESET_STAT] RESET_STAT_REG[WDOGRESET_STAT] RESET_STAT_REG[SNC_WDOGRESET_STAT]
SW Reset	The rest of the Register File

9.2.1 Power-On Reset from Pin

The Power-on Reset function can be triggered at timer expiration. It is available at two sources:

- Reset Pad (RSTN): The reset pad is always capable of producing a Power-on Reset
- GPIO Pin: A GPIO can be selected by the user application to act as POR source

The POR_TIMER_REG configures the time needed for the POReset signal to be active. The register field POR_TIME is a 7-bits field (maximum value is 0x7F), which holds a multiplication factor for counting RCLP clock periods. This is explained in the following formula:

Total time for POR = POR_TIME x 4096 x RCLP clock period,

where RCLP clock period equals to 31.25 ns or 1.95 ns at 25 °C.

When RCLP runs at 32 kHz, the maximum time for issuing a POR is ~16.2 seconds at 25 °C, while the default value is ~3 seconds (POR_TIME=0x18).

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It should be noted that the RCLP clock is temperature dependent and as such drift over the temperature should be expected.

The Power-on Reset timer is clocked by the RCLP clock. If the application disables the RCLP, then hardware takes care of enabling the RCLP clock when the POR source (Reset pad or GPIO) is asserted. Note that, if POR is generated from the Reset pad, RCLP will operate with the default (reset) trim value. If a GPIO is used as a POR source, the RCLP clock will be trimmed. The timing deviation between both cases is expected to be minor if the RCLP is configured at 32 kHz mode.

When a GPIO is used as a Power-on Reset source, the selected pin retains its capability to act as GPIO. The POR_PIN_REG[PIN_SELECT] field holds the required GPIO pin number. If the value of the PIN_SELECT field equals to 0 the POR over GPIO functionality is disabled. The polarity of the pin can be configured by the POR_PIN_REG [POR_POLARITY] bit where 0 means Active Low and 1 Active High.

The operation of the Power-on Reset for both Reset pad and GPIO is depicted in Figure 29.

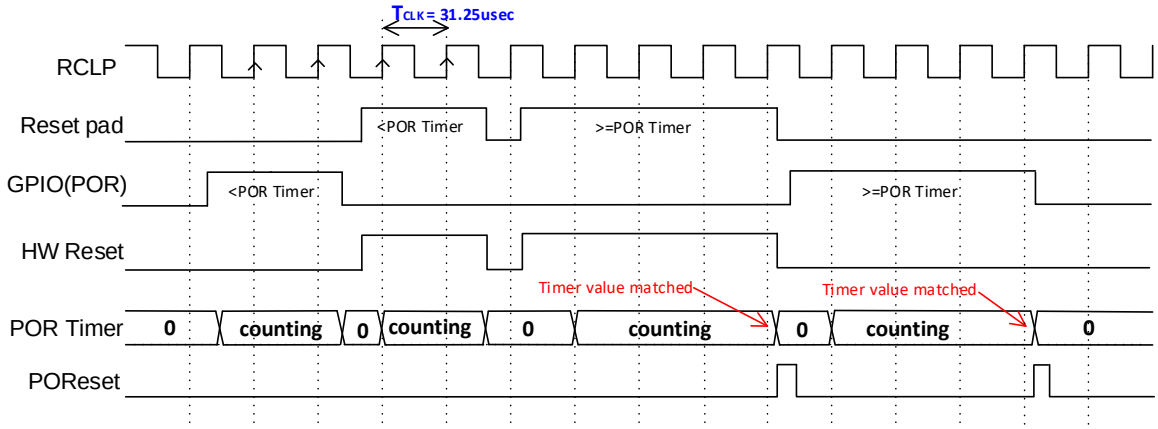

Figure 29: Power-on Reset Timing Diagram

If any of the POR sources is asserted, then the POR timer starts to count. When a POR source is released before the timer has expired, the POR timer will reset to 0. If a second source is asserted while the first is already asserted and the first is released after that point, POR will occur, assuming that the total time of both sources kept asserted is larger or equal than the POR_TIME.

The POR_PIN_REG[PIN_SELECT] field cannot survive any Reset (POR, HW, SW) hence the user must take special care on setting up the GPIO POR source right after a reset. This also applies to the POR_TIMER_REG[POR_TIME] field after a Power-on Reset.

Users should consider that if a GPIO is used as a POR source, the dynamic current of the system increases, due to the dynamic current consumed by the RCLP oscillator. This increase is calculated to be ~100 nA and it is also present during a sleep time period. POR from Reset pin does not add this dynamic current consumption.

9.3 Programming

There is a simple sequence of steps that needs to be followed to configure the POR from GPIO functionality:

1. Select the GPIO to be set as a POR source (POR_PIN_REG[POR_PIN_SELECT]).
2. Set up the input polarity of the GPIO that causes POR (POR_PIN_REG[POR_PIN_POLARITY]).
3. Configure the time for the POR to happen (POR_TIMER_REG[POR_TIME]). Default time is ~3 seconds.

Remember that to set up the time that the Reset pin produces a POR, only POR_TIMER_REG has to be set.

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10 Arm Cortex-M33

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

10.1 Introduction

The Cortex-M33 processor is a low gate count, highly energy-efficient processor that is intended for microcontrollers and deeply embedded applications. The processor is based on the Armv8-M architecture and is primarily for use in environments where security is an important consideration. The interfaces that the processor supports include:

- Code AHB (C-AHB) interface
- System AHB (S-AHB) interface
- External PPB (EPPB) APB interface
- Debug AHB (D-AHB) interface

Arm Cortex-M33 does not retain its status when going to any sleep modes that switch off its power domain. So, the CPU always wakes up in reset. Restoration of the CPU state is done by SW.

Features

- Supports the Armv8-M Main Extension. The processor has optional support for one or more of the following extensions:
  - The Floating-point Extension
  - The Digital Signal Processing (DSP) Extension
  - The Debug Extension
- An in-order issue pipeline
- Thumb-2 technology
- Configurable to perform data accesses as either big or little endian
- Nested Vectored Interrupt Controller (NVIC)
- Floating Point Unit (FPU) supporting single-precision arithmetic
  - Combined multiply-add instructions for increased precision (Fused MAC)
  - Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
  - Hardware support for denormals and all IEEE Standard 754-2008 rounding modes
  - 32 32-bit single-precision registers or 16 64-bit double-precision registers
  - Lazy floating-point context save
- Support for exception-continuable instructions
- Micro Trace Buffer (MTB) with 4 kB MTB memory
- Embedded Trace Macrocell (ETM)

10.2 Architecture

In Figure 30, the ETM and MTB integration on the ARM M33 is shown. The TRACEDATA is 4-bit and the TRACECLK supports up to 80 MHz speed.

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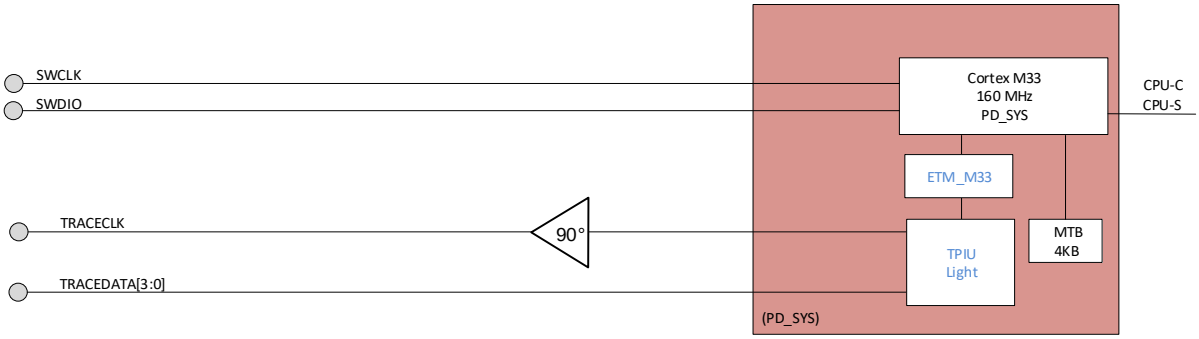

Figure 30: ARM M33 ETM and MTB Integration

10.2.1 Interrupts

This section lists all 53 interrupt lines, except the NMI interrupt, and describes their source and functionality. The overview of the interrupts is illustrated in Table 97.

Table 97: Interrupt List

#	Name	Pulse/Level	Polarity	Description
0	CMAC2SYS_IRQ	Level	Active High	CMAC and mailbox interrupt line
1	SNC2SYS_IRQ	Level	Active High	SNC M0+ interrupt to Cortex M33
2	M33Cache_MRM_IRQ	Pulse	Active High	M33 Instruction Cache miss rate monitor interrupt
3	PDC_M33_IRQ	Level	Active High	This is an interrupt coming from the PDC indicating that the M33 needs to be woken up due to a GPIO/Peripheral/another master request
4	KEY_WKUP_GPIO_IRQ	Level	Active High	Debounced button press interrupt. This interrupt is first driven to the PDC and then directed to the required masters to be woken up/notified
5	VBUS_IRQ	Pulse	Active High	VBUS presence interrupt
6	CHARGER_STATE_IRQ	Pulse	Active High	Serves both the Charger FSM and the JEITA FSM
7	CHARGER_ERROR_IRQ	Pulse	Active High	Charger error interrupt line
8	DCDC_BOOST_IRQ	Pulse	Active High	DCDC Boost interrupt. Generated upon time out threshold reach
9	PLL48_LOCK_IRQ	Level	Active High	Indicates that the PLL48 is locked at 48MHz
10	CRYPTO_IRQ	Level	Active High	Crypto interrupt. Sources: AES or HASH function interrupt
11	PLL_LOCK_IRQ	Level	Active High	Indicates that PLL is locked at 160 MHz
12	XTAL32MDRY_IRQ			Indicates that the XTAL32M oscillator is trimmed and settled and can provide a reliable 32 MHz clock
13	RFDIAG_IRQ	Pulse	Active High	Baseband or Radio Diagnostics Interrupt. Required for signaling Radio or Baseband internal events. Two signals per Radio and 2 per BB
14	GPIO_P0_IRQ	Level	Active High	GPIO port 0 toggle interrupt line

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#	Name	Pulse/Level	Polarity	Description
15	GPIO_P1_IRQ	Level	Active High	GPIO port 1 toggle interrupt line
16	GPIO_P2_IRQ	Level	Active High	GPIO port 2 toggle interrupt line
17	TIMER_IRQ	Level	Active High	TIMER interrupt line
18	TIMER2_IRQ	Level	Active High	TIMER2 interrupt line
19	TIMER3_IRQ	Level	Active High	TIMER3 interrupt line
20	TIMER4_IRQ	Level	Active High	TIMER4 interrupt line
21	TIMER5_IRQ	Level	Active High	TIMER5 interrupt line
22	TIMER6_IRQ	Level	Active High	TIMER6 interrupt line
23	RTC_IRQ	Level	Active High	RTC interrupt line
24	RTC_EVENT	Level	Active High	RTC event interrupt line
25	CAPTIMER_IRQ	Level	Active High	GPIO triggered Timer Capture interrupt
26	ADC_IRQ	Level	Active High	General Purpose analog-digital converter interrupt
27	ADC2_IRQ	Level	Active High	Application analog-digital converter interrupt
28	DMA_IRQ	Pulse	Active High	General Purpose DMA interrupt line
29	UART_IRQ	Level	Active High	UART interrupt line
30	UART2_IRQ	Level	Active High	UART2 interrupt line
31	UART3_IRQ	Level	Active High	UART3 interrupt line
32	SPI_IRQ	Level	Active High	SPI interrupt line
33	SPI2_IRQ	Level	Active High	SPI2 interrupt line
34	SPI3_IRQ	Level	Active High	SPI3 interrupt line
35	I2C_IRQ	Level	Active High	I2C interrupt line
36	I2C2_IRQ	Level	Active High	I2C2 interrupt line
37	I2C3_IRQ	Level	Active High	I2C3 interrupt line
38	I3C_IRQ	Level	Active High	I3C interrupt line
39	USB_IRQ	Pulse	Active High	USB interrupt line
40	PCM_IRQ	Pulse	Active High	PCM interrupt line
41	SRC_IN_IRQ	Level/Pulse	Active High	SRC input interrupt line
42	SRC_OUT_IRQ	Level/Pulse	Active High	SRC output interrupt line
43	SRC2_IN_IRQ	Level/Pulse	Active High	SRC2 input interrupt line
44	SRC2_OUT_IRQ	Level/Pulse	Active High	SRC2 output interrupt line
45	VAD_IRQ	Level	Active High	VAD interrupt line (programmable: default is a high level or a pulse 8 internal clk cycles)
46	eMMC_IRQ	Level	Active High	eMMC Controller interrupt line
47	Reserved			
48	GPU_IRQ	Level	Active High	GPU interrupt line
49	LCD_IRQ	Level	Active High	Display controller interrupt line
50	Reserved			
51	CHARGER_DET_IRQ	Level	Active High	Charger detection interrupt line

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#	Name	Pulse/Level	Polarity	Description
52	DCACHE_MRM_IRQ	Level	Active High	Data cache MRM interrupt line
53	CLK_CALIBRATION_IRQ	Level	Active High	Indicates that the calibration of the selected clock has been performed successfully
54	VSYS_GEN_IRQ	Level	Active High	Indicates when the LDO_VSYS (in VSYS generator module) is too hot or when VBUS drive strength is too low for the set LDO_VSYS current limit

10.2.2 Reference

The register descriptions for the Nested Vectored Interrupt Controller (NVIC), the System Control Block (SCB), and the System Timer (SysTick) of the Arm Cortex-M33 can be found in the following documents, available on the Arm website:

Devices Generic User Guide:
https://developer.arm.com/docs/100235/latest/preface

Technical Reference Manual:
https://developer.arm.com/docs/100230/0004

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11 Cache Controller

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

11.1 Introduction

The cache controller is used to accelerate the system performance of the Arm Cortex-M33 executing from OQSPI FLASH. It also conserves power by reducing the number of accesses to the external OQSPI FLASH. The cache dynamically loads program and data code into the cache Data RAM and executes from there.

The cache controller is controlled via the CACHE_*_REGs. The cache administration is kept in the TAG memory region. The cache RAM is initialized when the cache controller is enabled.

The cache controller supports four-way set associativity with an 8-Bytes cache line and a total of 8 kB of cache RAM. The cache line replacement strategy is used in the Least Recently Used (LRU).

For debugging, the Data and TAG memory can be monitored on the AHB-SYS bus (See Section 5.7). The cache is used for dynamic code and data caching. As an alternative for fast code executions, the data-RAM can be used for static code storage. This code must be copied from OQSPI FLASH.

Features

- Four-way set-associative implementation
- Zero delay cache hit on Most Recently Used (MRU) words, one cycle delay cache hit on LRU words
- Low cache miss-delay and configurable critical-word first functionality
- LRU replacement strategy for reduced miss-rates to minimize the costly, in terms of power, read accesses to the external FLASH
- Hit/Miss monitoring functionality

11.2 Architecture

The cache controller block diagram is shown in Figure 31.

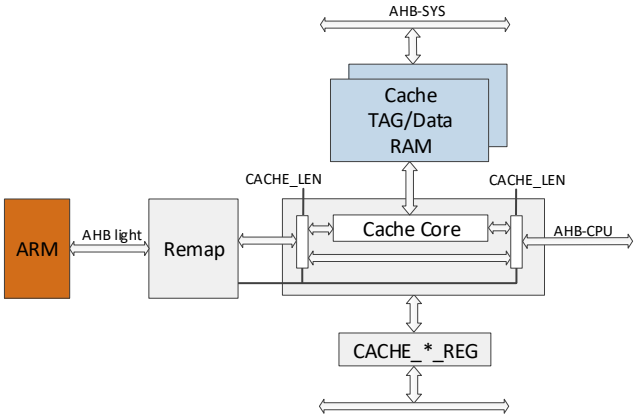

Figure 31: Cache Controller Block Diagram

11.2.1 Hit/Miss Rate Monitor

The system includes a monitoring block, which gives real-time information on the number of cache hits and misses within a certain amount of time. When a programmable threshold is reached, an

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interrupt is sent to the CPU to act. The block only operates while the system is in active mode. The main features are:

- Up to 10 ms active time interval counter
- Registered amount of cache misses
- Registered amount of cache hits
- Programmable threshold of cache hits or misses that generates an interrupt

The CACHE_MRM_HITS_REG contains the number of cache hits. The CACHE_MRM_MISSES_REG contains the number of misses counted within the time interval programmed at the CACHE_MRM_TINT_REG in CPU clock cycles. Note that for two sequential requests in the same cache-line, in which the first produces a cache miss the CACHE_MRM_MISSES_REG will be increased by 2, counting a second miss on the second request.

11.2.2 Miss Latency

This section describes the amount of time (in clock cycles) required from a cache miss up to the point the required code/data are fetched back to the CPU and execution continues. The cache miss latency (T_{CML}) can be split into the following intervals:

T_{CM2R}: Time from the cache miss up to request from the QSPI Controller.

T_{R2QA}: Time from the request up to actual access start.

T_{RDFL}: Time for reading data from the FLASH.

T_{CLAT}: Time required to get data to the CPU (cache latency).

The final amount of clock cycles is calculated by the following equation:

$T_{CML} = T_{CM2R}+T_{R2QA}+T_{RDFL}+T_{CLAT}$

where T_{RDFL} depends on the amount of data requested and is provided by the following formula:

$T_{RDFL} = [T_{CMD}+T_{ADDR}+T_{DUM}+(N_{CACHELINE}*2)+T_{PIPE}]*(sys\_clk/spi\_clk)$ where $N_{CACHELINE}$ is 8 Bytes.

For example, the amount of clock cycles required to read the data from the FLASH is:

$T_{RDFL} = 2+6+4+(8*2)+3 = 31$ spi clock cycles, for a QSPI FLASH.

An overview of the cache miss latency calculation, assuming that the ARM M33 and OQSPI interface are running at the same speed (for example, 96 MHz), is shown in Table 98 for Quad-SPI Flash and in Table 99 for Octa-SPI Flash device.

Table 98: QSPI FLASH Cache Miss Latency

Time Interval	Clock Cycles	Example
T_{CM2R}	7	7
T_{R2QA}	1	1
T_{RDFL}	$[T_{CMD}+T_{ADDR}+T_{DUM}+(N_{CACHELINE}*2)+T_{PIPE}]$	31
T_{CLAT}	4 (Note 1)	4
T_{CML}	**for one cache line (QPI mode)**	**43**

Note 1 This is the worst-case delay (request for the second word of a cache-line).

Table 99: OSPI FLASH Cache Miss Latency

Time Interval	Clock Cycles	Example
T_{CM2R}	7	7

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Time Interval	Clock Cycles	Example
T_{R2QA}	1	1
T_{RDFL}	[T_{CMD}+T_{ADDR}+T_{DUM}+($N_{CACHELINE}$*2)+T_{PIPE}]	27
T_{CLAT}	4 (Note 1)	4
T_{CML}	**for one cache line (QPI mode)**	**39**

Note 1 This is the worst-case delay (request for the second word of a cache-line).

11.3 Programming

11.3.1 Cache Controller Programming

There is a simple sequence of steps that needs to be followed to configure the Cache Controller:

1. Disable the Cache by clearing the CACHE_CTRL2_REG[CACHE_LEN] bit field.
2. Enable the cache (CACHE_CTRL2_REG[CACHE_LEN] != 0).
   The size of the cacheable external Flash memory can be specified in CACHE_CTRL2_REG[CACHE_LEN] when CACHE_CTRL2_REG[CACHE_LEN] != 1. If CACHE_CTRL2_REG [CACHE_LEN] = 1, then the memory space is specified by CACHE_FLASH_REG [FLASH_REGION_OFFSET].

11.3.2 Miss Rate Monitor Programming

There is a simple sequence of steps that needs to be followed to configure the Miss Rate Monitor:

1. Freeze all counters by clearing the CACHE_MRM_CTRL_REG[MRM_START] bit.
2. Set up the thresholds that produce interrupts:
   a. Cache Misses threshold: CACHE_MRM_MISSES_THRES_REG[MRM_MISSES_THRES]
   b. Cache Hits threshold: CACHE_MRM_HITS_THRES_REG[MRM_HITS_THRES]
   c. Time passed threshold: CACHE_MRM_TINT_REG[MRM_TINT]
3. Unmask all interrupts by setting the CACHE_MRM_CTRL_REG[MRM_IRQ_MASK] bit.
4. Enable the chosen interrupts:
   a. CACHE_MRM_CTRL_REG[MRM_IRQ_HITS_THRES_STATUS]: The number of cache hits reached the programmed threshold.
   b. CACHE_MRM_CTRL_REG[MRM_IRQ_MISSES_THRES_STATUS]: The number of cache misses reached the programmed threshold.
   c. CACHE_MRM_CTRL_REG[MRM_IRQ_TINT_STATUS]: The time interval counter reached the end.
5. Enable all counters by setting the CACHE_MRM_CTRL_REG[MRM_START] bit.
6. Read the results (misses and/or hits) in the CACHE_MRM_MISSES_REG and CACHE_MRM_HITS_REG registers.

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12 Data Cache Controller

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	×	✓	✓

12.1 Introduction

The data cache controller is used to access data from an external PSRAM. This cache can be used by GPU when accessing graphics resources and/or by the CPUs when accessing data that are stored in the external PSRAM.

Features

- Write-back cache policy with forced write flush capability
- Four-way set associative
- Random (LFSR-based) replacement policy
- Two words (8 bytes) cache line configuration
- 8 kB of total cache size
- Bypass functionality
- Enable/Disable cache functionality, cache memory is used as regular RAM when the cache is disabled
- Miss rate monitor functionality
- Programmable Cacheable address space
- Data/Tag RAM can be retained in any sleep mode

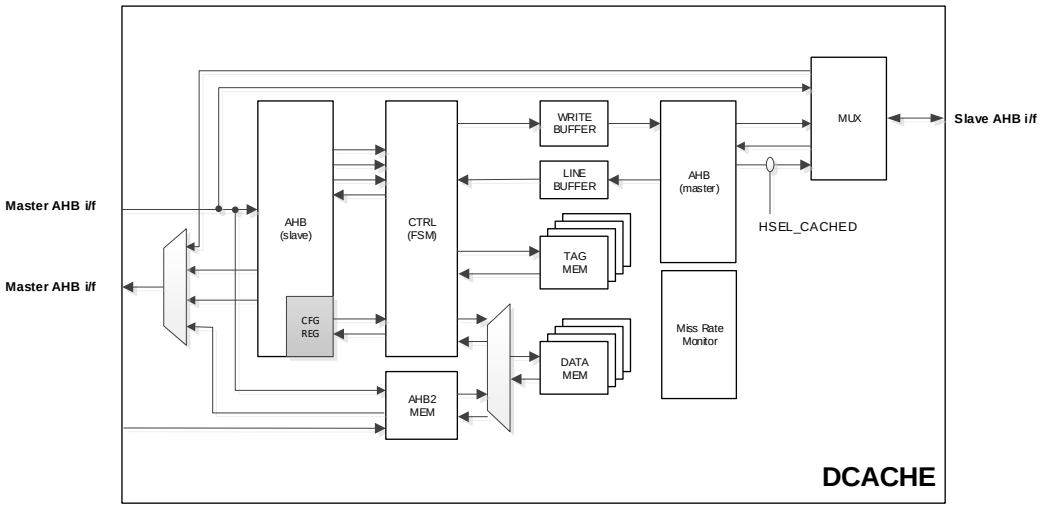

Figure 32: Data Cache Controller Block Diagram

12.2 Architecture

12.2.1 Overview

The data cache controller can handle read and write transactions from the CPU/GPU (Slave AHB port) to the PSRAM Quad SPI controller (Master AHB port). The block is organized in a four-way set associative manner, while the cache line size is 8 bytes wide. Two distinct memories are used to implement the four-way associativity, one of 8 kB for data and one of 3 kB for the TAG information. That results in 256 lines per associative way. The TAG ram consists of the tag address, a “valid” bit indicating if a word in the line is valid or not, and a “dirty” bit indicating whether the line needs to be

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written back to the external PSRAM or not, because it contains a word that is not synchronized with the actual values in the PSRAM.

The controller supports the following basic operations:

- **Cache read miss:** A read request on the slave port for an address that is not included in the cache memory (cache read miss) results in a read request on the master port for the specific cache line, which contains the requested word. The cache controller stalls the CPU/GPU until the requested data are available in the cache memory
- **Cache read hit:** A read request on the slave port for an address that is included in the cache memory (cache read hit) is served by the cache controller within a couple of clock cycles
- **Cache write requests:** A write request on the slave port does not result in a write request on the master port (write-back) unless a “dirty” cache-line replacement is required. The cache controller serves the request with minimum delays (store data to the cache memory and mark the data as “dirty”). If the data is already marked as “dirty” then the cache controller updates only the data
- **Cache wflush:** The controller checks for “dirty” bits in all available lines and triggers the write back operation towards the QuadSPI controller (and eventually the external PSRAM device)
- **Cache (re)initialization:** The controller invalidates all tag lines by clearing the tag memory, namely setting “dirty” and “valid” bit to zero. Note that the cache write-flush and cache reinitialization can be triggered together. In this case, the cache write-flush (wflush) is done first followed by the cache initialization

When a cache-line is to be replaced, after a read or write the request on the slave port, then the cache controller writes back (evict from cache) the “dirty” marked cache line to the QSPI PSRAM and then replaces the cache line with a new one. If the cache line is not marked “dirty”, then the cache controller replaces the contents immediately (no write transactions to QSPI controller required).

The latency on various operations of the cache controller in clock cycles is presented in Table 100.

Table 100: Data Cache Controller Operations Latency (Clocks) for Quad SPI Mode

	DCACHE	QSPI WRITE		QSPI READ		
Cache Controller Operation	*(overhead)*	*Word1*	*Word2*	*Word1*	*Word2*	*TOTAL*
MISS	7			50	15	72
HIT	1					1
ENVICT (write back)	17	4	33	79	15	148

Note that the table displays the complete operation latency, including the one related to the QuadSPI controller for reading/writing data to the external PSRAM component. All numbers are in clock cycles of the hclk being the clock of this block.

The cache controller and related RAMs reside in the controller’s power domain (PD_CTRL). When this power domain is switched off, both data and TAG RAMs can be retained so that cached data are not lost.

Note that, before the system goes to any sleep mode without the cache data and TAG RAMs retained, a cache write flush must be triggered and awaited until the complete transaction of writing back “dirty” cache lines into the external PSRAM is completed, to avoid data loss.

12.2.2 Enable/Disable

When the cache controller is disabled, the cache memory can be used as a regular RAM, while all the transactions from the slave port are forwarded to the master port, as is, with minimum delays. When the disable configuration signal is asserted the cache controller first completes all the pending writes (if any) to the master port. All cache lines which are marked as “dirty” are written back to PSRAM through the master port of the cache controller (forced write flush). After the successful flush

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of the cache memory, the cache controller can be disabled. SW is responsible to initialize the RAM after disabling the cache controller.

When the enable configuration signal is asserted, the cache controller clears all extra information (TAG, dirty-bits, etc.) in the cache memory and all the cache memory should be assumed empty. A ready status signal is asserted when the cache controller is ready to handle incoming transactions on the slave port.

12.2.3 Bypass

There is a complete cache controller bypass capability with the use of a multiplexer (ICM) which allows for direct access to the external PSRAM through the relative controller. When the bypass configuration signal is asserted, the cache controller forwards all transactions from the slave port to the master port, as is, with zero delay, without changing/updating the cache memory.

12.2.4 Flush

When the “write flush” configuration signal is asserted, the cache controller writes back (evict) all the cache lines, which are marked as “dirty”, to the PSRAM through the master port (QSPI controller).

12.2.5 Miss Rate Monitor

The data cache controller includes a miss rate monitor, similar to the one of the instruction cache. The miss rate monitor block monitors the cache read misses, cache read hits, and the cache evicts.

12.3 Programming

12.3.1 Data Cache Controller Programming

There is a simple sequence of steps that needs to be followed to configure the Cache Controller:

1. Disable the Cache by clearing the DCACHE_CTRL_REG[DCACHE_LEN] and the DCACHE_CTRL_REG[DCACHE_ENABLE] bit fields.
2. Configure the base address and the length of the cacheable area in the PSRAM in the DCACHE_BASE_ADDR_REG register.
3. Perform an initialization on the cache RAM (DCACHE_CTRL_REG[DCACHE_INIT]=1) and wait for the initialization to finish (DCACHE_CTRL_REG[DCACHE_READY]=1).
4. Enable the Data cache controller (DCACHE_CTRL_REG[DCACHE_ENABLE] = 1.

   The Data Cache controller is ready when DCACHE_CTRL_REG[DCACHE_READY] = 1.

12.3.2 Miss Rate Monitor Programming

There is a simple sequence of steps that needs to be followed to configure the Miss Rate Monitor:

1. Freeze all counters by clearing the DCACHE_MRM_CTRL_REG[MRM_START] bit.
2. Set up the thresholds that produce interrupts:
   a. Cache Misses threshold: DCACHE_MRM_MISSES_THRES_REG[MRM_MISSES_THRES]
   b. Cache Hits threshold: DCACHE_MRM_HITS_THRES_REG[MRM_HITS_THRES]
   c. Cache Evicts threshold: DCACHE_MRM_EVICTS_THRES_REG[MRM_EVICTS_THRES]
   d. Time passed threshold: DCACHE_MRM_TINT_REG[MRM_TINT]
3. Unmask all interrupts by setting the DCACHE_MRM_CTRL_REG[MRM_IRQ_MASK] bit.
4. Enable the chosen interrupts:
   a. DCACHE_MRM_CTRL_REG[MRM_IRQ_HITS_THRES_STATUS]: The number of cache hits reached the programmed threshold.
   b. DCACHE_MRM_CTRL_REG[MRM_IRQ_MISSES_THRES_STATUS]: The number of cache misses reached the programmed threshold.

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c. DCACHE_MRM_CTRL_REG[MRM_IRQ_EVICTS_THRES_STATUS]: The number of cache evicts reached the programmed threshold.
d. DCACHE_MRM_CTRL_REG[MRM_IRQ_TINT_STATUS]: The time interval counter reached the end.

5. Enable all counters by setting the DCACHE_MRM_CTRL_REG[MRM_START] bit.
6. Read the results (misses and/or hits) in the DCACHE_MRM_MISSES_REG, DCACHE_MRM_HITS_REG, and DCACHE_MRM_EVICTS_REG registers.

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13 Bus

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

13.1 Introduction

The DA1470xx is equipped with a multi-layer AMBA bus which enables parallel data paths between different masters and slaves. The bus matrix comprises three main busses:

- AHB-CPUC bus where the Cache controller is master. This is the primary bus for executing code from
- AHB-CPUS bus where the ARM M33 is master. This is the bus for the system
- AHB-DMA bus where the GPU 2D, the Generic-Purpose DMA, the Display Controller, the Crypto, and the eMMC host controller can be masters

The APB bus consists of two parts:

- APB32 slow for the peripheral blocks which require PCLK up to 32 MHz
- APB32 fast for the peripheral blocks which require high-speed PCLK = HCLK up to 160 MHz

There are several slaves which are sitting behind interconnection multiplexers (ICMs) allowing access from different AHB busses namely:

- Quad/Octa SPI FLASH memory controller
- QSPI Flash/RAM controllers
- 32-bit APB slow and fast peripheral registers
- The OTP controller
- The ROM controller
- The AHB register file containing registers

Features

- Enables parallelization of data transfers from:
  - Peripherals to memory (GP DMA)
  - Cortex-M33 data read/writes from/to RAM
  - Cortex-M33 executing code from O/Q-SPI FLASH

13.2 Architecture

The architecture of the AMBA bus matrix is shown in Figure 33. There are four potential masters for the APB32 slow, namely: Sensor Node Controller, CMAC, Cortex-M33, and the DMA engine. A multiplexer is required there to allow access to a single master on the APB32 slow. Multiplexing is before the APB32 bridge. There are three potential masters for the APB32 fast, namely: Sensor Node Controller, Cortex-M33, and the DMA engine.

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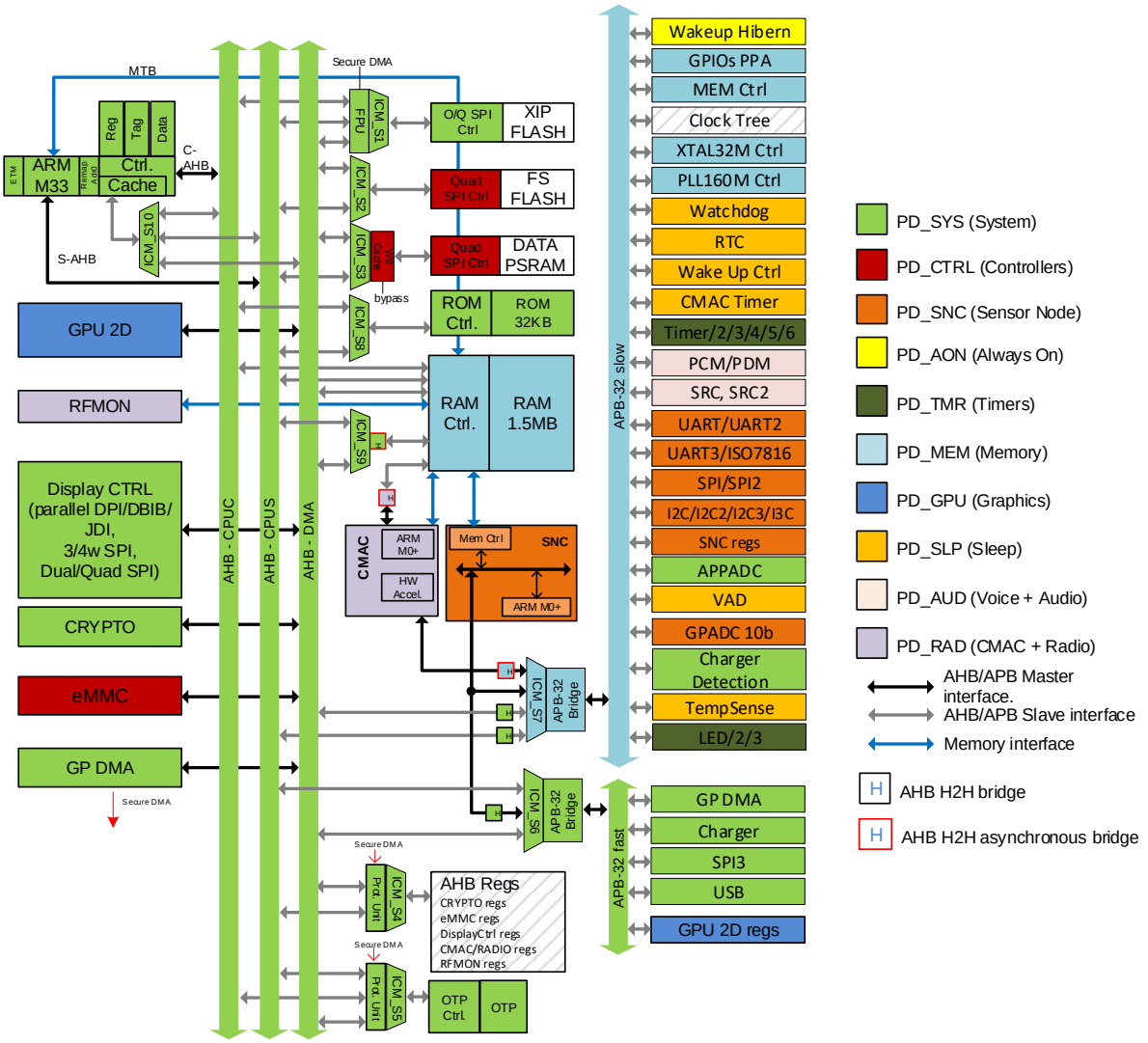

Figure 33: Bus Architecture

There are two protection units - (1) the OTP Protection Unit (OPU), and (2) the FLASH Controller Protection Unit (FPU)] – that form part of the system's security perimeter:

- The OPU protects the OTP section where keys are stored; keys that the CPU cannot read. Access to this space is only allowed when a special signal (secure channel). Read/Write protection strategy should follow the sticky bits definition
- The FPU protects the OQSPI FLASH Controller registers that keep the AES key (write only) from being written by the CPU and the AES/HASH registers from being read by the CPU. Access is only allowed by the GP DMA and only if the respective secure channel signal is activated. The rest of accesses to other register files are completely transparent and will not be gated by the FPU. Read/Write protection strategy should follow the sticky bits definition

The priorities of the arbitration on the AHB-DMA bus are programmable. The default priorities are listed in Table 101.

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Table 101: AHB-DMA Master Default Priorities

Priority	Master
1 (highest)	Display CTRL
2	GPU 2D
3	GPDMA
4	Crypto (AES/HASH)
5	eMMC
6	Reserved
7 (lowest)	CPU-S (H2H bridge)

The arbitration priorities for the ICM blocks are listed in the following tables.

Table 102: ICM_S1 Arbitration Priorities

Priority	AHB Bus
1 (highest)	CPU-C
2	CPU-S
3 (lowest)	DMA

Table 103: ICM_S2 Default Arbitration Priorities

Priority	AHB Bus
1 (highest)	DMA
2 (lowest)	CPU-S

Note: The priorities of the ICM_S2 are programmable.

Table 104: ICM_S3 Default Arbitration Priorities

Priority	AHB Bus
1 (highest)	DMA
2 (lowest)	CPU-S

Note: The priorities of the ICM_S3 are programmable.

Table 105: ICM_S4 Default Arbitration Priorities

Priority	AHB Bus
1 (highest)	DMA
2 (lowest)	CPU-S

Note: The priorities of the ICM_S4 are programmable.

Table 106: ICM_S5 Arbitration Priorities

Priority	AHB Bus
1 (highest)	CPU-S
2	CPU-C
3 (lowest)	DMA

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Table 107: ICM_S6 Default Arbitration Priorities

Priority	AHB Bus
1 (highest)	CPU-S
2	SNC
3 (lowest)	DMA

Note: The priorities of the ICM_S6 are programmable.

Table 108: ICM_S7 Default Arbitration Priorities

Priority	Master/Bus
1 (highest)	CMAC Master
2	SNC Master
3	DMA Bus
4 (lowest)	CPU-S Bus

Note: The priorities of the ICM_S7 are programmable.

Table 109: ICM_S8 Arbitration Priorities

Priority	AHB Bus
1 (highest)	CPU-C
2 (lowest)	CPU-S

Table 110: ICM_S9 Arbitration Priorities

Priority	AHB Bus
1 (highest)	CPU-S
2 (lowest)	DMA

Table 111: ICM_S10 Arbitration Priorities

Priority	AHB Bus
1 (highest)	CPU-C
2	CPU-S
3 (lowest)	DMA

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14 Configurable MAC (CMAC)

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

14.1 Introduction

The Configurable Medium Access Controller (CMAC) is a Flexible MAC HW block, based on Arm Cortex-M0+ that can be programmed to support multiple protocols.

The CMAC executes code from the system RAM with zero wait states. It also has access to all peripherals in the APB32-slow bus of the system.

Features

- Implements Bluetooth® LE 5.x controller stack, including HCI
- Optional Bluetooth® LE 5.x Features supported:
  - 2 Mbps
  - Advertising Extensions
  - Channel selection algorithm #2
  - Periodic Advertising
  - High Duty Cycle Non-Connectable Advertising
- Autonomous operation for Advertising or keep-alive connections
- Autonomous execution and sleep cycles
- Rapid wake-up and go-to-sleep operation
- Size and base address of RAM for code execution is configurable
- Bluetooth® LE Audio
- Accelerators in hardware:
  - Link Layer and framing Timers
  - AES-128-bit crypto engine
  - Configurable Whitening engine, compliant with Bluetooth® LE and 802.15.4 standards
  - Configurable CRC engine, up to 32-bit order primitive polynomials. Compliant with Bluetooth® LE and other standards
  - 32 bits wide Correlator
  - AoA/AoD support in hardware
  - Coexistence interface

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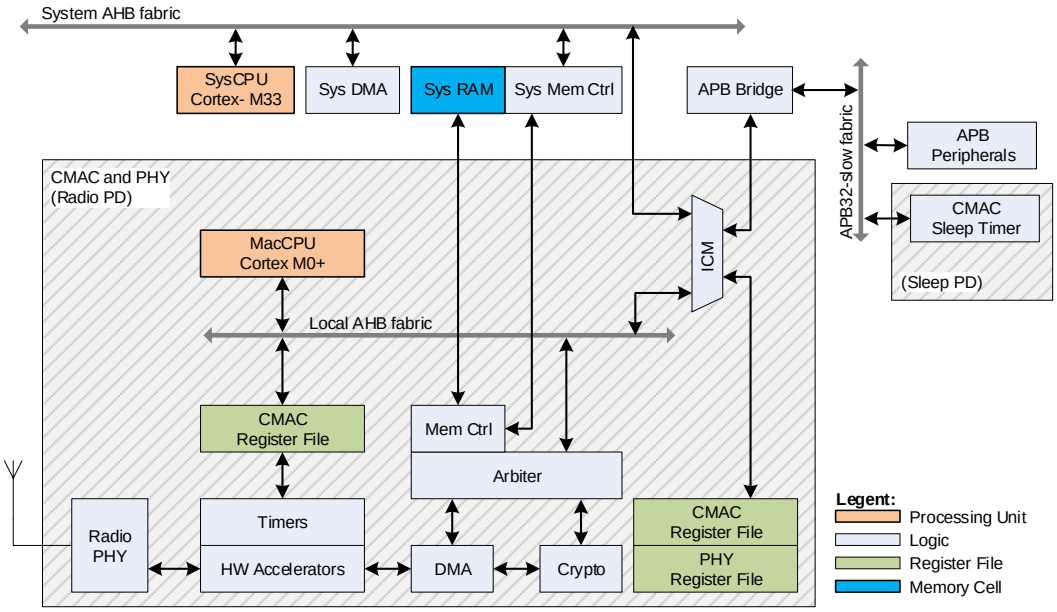

Figure 34: Configurable MAC Block Diagram

14.2 Architecture

The CMAC block is an autonomous system that can execute Bluetooth® LE and other protocols if there are enough HW accelerators and Firmware throughput.

A dedicated Cortex-M0+ executes code through the local memory controller, which reuses the system memory RAM for storing code and data. A hardware bit stream controller performs all real-time functions by using hardware accelerators like whitening, CRC, and crypto engines. A Link Layer Timer schedules protocol operations and radio transactions. The radio transactions are programmed to the CMAC registers. The HW executes them automatically at the scheduled moment, activating the proper accelerators.

Radio Register File and CMAC Sleep Timer Register Files are accessible by both CMAC Cortex-M0+ and ARM Cortex-M33 processors, but typically only CMAC CPU access them.

14.2.1 Dataflow

CMAC can implement the Bluetooth® LE Data Link Layer, providing an HCI interface towards the system processor Cortex-M33.

The communication of the CMAC processor Cortex-M0+ with the system processor Cortex-M33 is performed via IRQ signals and the common system memory RAM. A mailbox mechanism can be used to exchange command and data structures between the two CPUs.

14.2.2 Diagnostics

Table 112 shows available CMAC diagnostics signals.

Table 112: CMAC Diagnostic Signals

Diagnostics	Signal	Description
CMAC_DIAG_0	TX EN	Data transmit enable signal
CMAC_DIAG_1	RX EN	Data receive enable signal
CMAC_DIAG_2	DATA EN	Tx/Rx Data Enable pulse
CMAC_DIAG_3	DATA COMB	TX and RX data bits (combined on the same line)

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Diagnostics	Signal	Description
CMAC_DIAG_4	Reserved	-
CMAC_DIAG_5	Reserved	-
CMAC_DIAG_6	Reserved	-
CMAC_DIAG_7	CORR COMB	Indicates that the correlator is active
CMAC_DIAG_8	CRC	RX CRC LFSR is zero to indicate correctly received packet
CMAC_DIAG_9 to 15	Reserved	-

The functionality of the diagnostic signals is depicted in Figure 35.

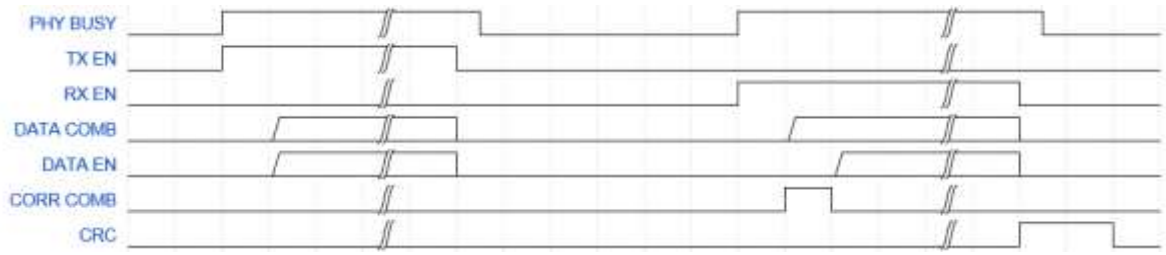

Figure 35: CMAC Diagnostics Timing Diagram

14.2.3 CoExistence Interface

The DA1470x implements a coexistence interface for signaling radio activity to external 2.4 GHz co-located devices. A three-wire interface is delivering information on the priority and the RF transmit/receive events.

The CoEx interface and its connection to the rest of the system are displayed in Figure 36.

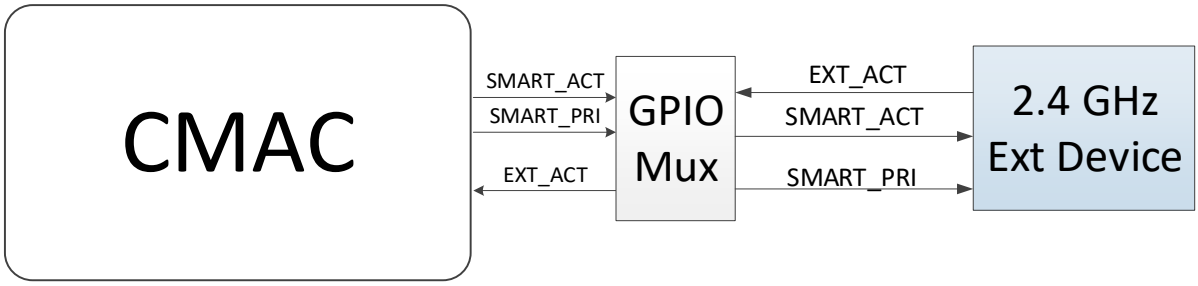

Figure 36: Coexistence Interface

Features

- 2.4 GHz Radio activity indication
- Priority indication
- Sensing of external module RF activity
- Supports up to two external 2.4 GHz devices

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14.2.3.1 Architecture

The coexistence external interface contains three signals:

- EXT_ACT: This is an input to the DA1470x and when asserted, it designates that an external 2.4 GHz device is about to issue RF activity
- SMART_ACT: This is an output from the DA1470x and when asserted it designates that the DA1470x is transmitting or receiving hence an external 2.4 GHz device should be aware of the radio activity. The exact timing of the assertion of this signal is depicted in Figure 37
- SMART_PRI: This signal is communicating whether the DA1470x has priority over the external device or not. If asserted, then the external device could adjust its RF activity accordingly

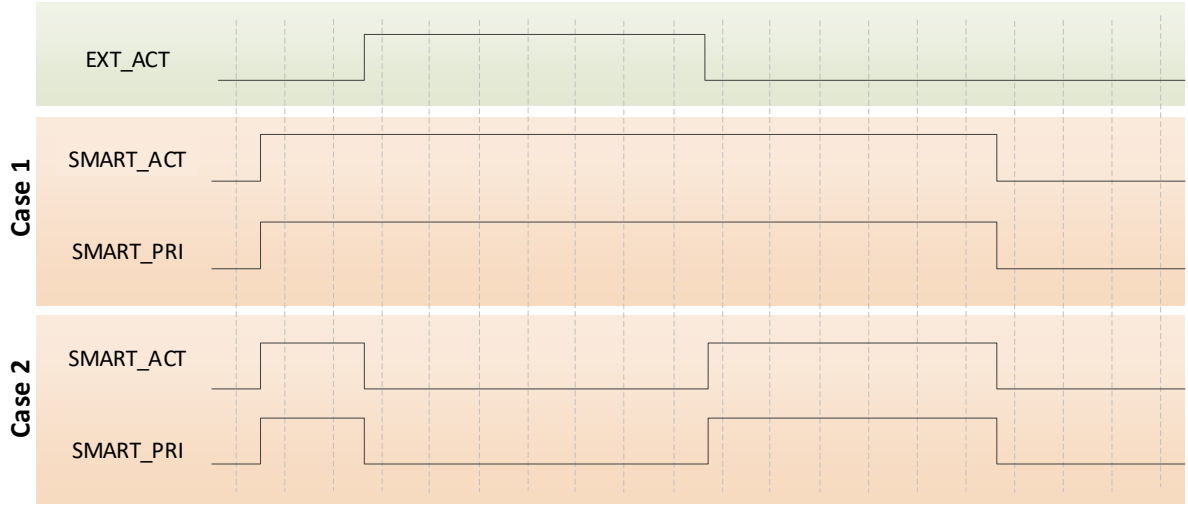

Figure 37: Coexistence Signaling Cases

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15 Sensor Node Controller (SNC) with Arm Cortex M0+

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

15.1 Introduction

The Sensor Node Controller comprises an ARM Cortex M0+, and it is used to manipulate communication controllers and the sensors connected to them. It can operate autonomously, without waking up the rest of the system.

Features

- The code executed by the ARM Cortex M0+ is stored in the system RAM and it is accessed through the SNC AHB interface (dedicated AHB interface on the memory controller)
- Supports clock frequencies up to 32 MHz
- Supports state retention. One retainable register is used for the indication of a previously saved state in the RAM. The SW running in the SNC is responsible to save/load the processor state when the SNC power domain is switched off/on
- Supports CPU freeze functionality when debugging is on
- A dedicated watchdog timer is used with a connection to the NMI of the Arm Cortex M0+
- Supports 4 kB MTB dedicated RAM for debugging purposes

15.2 Architecture

The block diagram of the SNC with Arm Cortex M0+ is shown in Figure 38. An internal AHB bus is used to connect Arm Cortex M0+ with the memory controller (dedicated interface) and two APB buses.

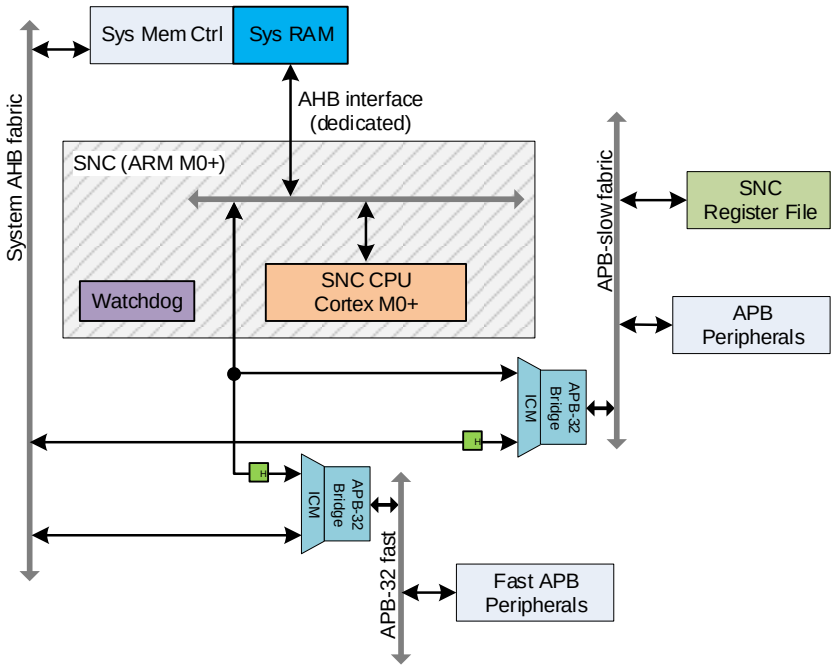

Figure 38: SNC with Arm Cortex M0+ Block Diagram

The Arm Cortex M0+ has access to the APB32-fast and APB32-slow fabrics, through APB32 bridges. The register file of the SNC is placed in the APB32-slow bus while the Cortex M0+ AHB interface is

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connected (through the internal bus) to a dedicated AHB port of the memory controller, for fast instruction and data accessing.

A dedicated watchdog timer is included in the SNC subsystem. The watchdog timer informs the SNC ARM M0+ (through NMI) when the timer is going to be expired (16 clock cycles before expiration) and generates an HW reset when the timer is at -16.

15.2.1 Interrupts

The SNC Arm Cortex M0+ has access to the complete set of APB bus peripheral controllers. As such, a significant number of interrupts must be evaluated by the SNC Arm Cortex M0+ to efficiently serve the interfaces accordingly. The list of interrupts is presented in Table 113.

Table 113: SNC Arm Cortex M0+ Interrupts

#	Name	Edge/Level	Polarity	Description
0	SYS2SNC_IRQ	Level	Active High	System interrupt line
1	CMAC2SNC_IRQ	Level	Active High	CMAC interrupt line
2	PDC_SNC_IRQ	Level	Active High	This is an interrupt coming from the PDC indicating that the SNC M0+ needs to be woken up due to a GPIO/Peripheral/another master request
3	KEY_WKUP_GPIO_IRQ	Level	Active High	Debounced button press interrupt. This interrupt is first driven to the PDC and then directed to the required masters to be woken up/notified
4	GPIO_P0_IRQ	Level	Active High	GPIO port 0 toggle interrupt line
5	GPIO_P1_IRQ	Level	Active High	GPIO port 1 toggle interrupt line
6	GPIO_P2_IRQ	Level	Active High	GPIO port 2 toggle interrupt line
7	TIMER_IRQ	Level	Active High	TIMER interrupt line
8	TIMER3_IRQ	Level	Active High	TIMER3 interrupt line
9	TIMER4_IRQ	Level	Active High	TIMER4 interrupt line
10	TIMER5_IRQ	Level	Active High	TIMER5 interrupt line
11	TIMER6_IRQ	Level	Active High	TIMER6 interrupt line
12	RTC_IRQ	Level	Active High	RTC interrupt line
13	RTC_EVENT	Level	Active High	RTC event interrupt line
14	CAPTIMER_IRQ	Level	Active High	GPIO triggered Timer Capture interrupt
15	ADC_IRQ	Level	Active High	General Purpose ADC interrupt
16	UART_IRQ	Level	Active High	UART interrupt line
17	UART2_IRQ	Level	Active High	UART2 interrupt line
18	UART3_IRQ	Level	Active High	UART3 interrupt line
19	SPI_IRQ	Level	Active High	SPI interrupt line
20	SPI2_IRQ	Level	Active High	SPI2 interrupt line
21	SPI3_IRQ	Level	Active High	SPI3 interrupt line
22	I2C_IRQ	Level	Active High	I2C interrupt line
23	I2C2_IRQ	Level	Active High	I2C2 interrupt line
24	I2C3_IRQ	Level	Active High	I2C3 interrupt line

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#	Name	Edge/Level	Polarity	Description
25	I3C_IRQ	Level	Active High	I3C interrupt line
26	PCM_IRQ	Pulse	Active High	PCM interrupt line
27	SRC_IN_IRQ	Level/Pulse	Active High	SRC input interrupt line
28	SRC_OUT_IRQ	Level/Pulse	Active High	SRC output interrupt line
29	SRC2_IN_IRQ	Level/Pulse	Active High	SRC2 input interrupt line
30	SRC2_OUT_IRQ	Level/Pulse	Active High	SRC2 output interrupt line
31	VAD_IRQ	Level	Active High	VAD interrupt line (programmable: default is a high level or a pulse 8 internal clk cycles)

15.2.2 Memory Map

SNC Arm Cortex M0+ can access RAM1 (32 kB) and RAM2 (32 kB) memories for code execution and data storage, while it can use RAM8 (128 kB) for sharing data with the other processors in the system (Arm Cortex M33, CMAC). Furthermore, RAM13 can be used as MTB. The start/end addresses for the RAMs are shown in Table 114.

Table 114: Memory Access

RAM Cells	SNC Start Address	SNC End Address
RAM1	0x000000	0x008000
RAM2	0x008000	0x010000
RAM8	0x030000	0x050000
RAM13 (MTB)	0x080000	0x081000

SNC Cortex M0+ can access all peripherals at the same addresses as the Cortex M33, shown in the memory map.

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16 RAM Controller

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

16.1 Introduction

The RAM controller allows access to the 1.5 MB RAM pool by the system's masters namely the SysCPU, the CMAC CPU, the SNC CPU, and the General-Purpose DMA controller.

The RAM controller implements an intelligent addressing scheme so that RAM is not fragmented by various data or code allocations while at the same time allowing for parallel access of multiple data streams on different RAM cells transparently to the application software. Thus, it allows the System CPU storing application variables, the CMAC CPU running code, the DMA transferring RAM data and Sensor Node storing sensors data all at the same time with arbitration to minimize the wait states.

Features

- Supports flexible memory allocation per master to avoid fragmentation
- Supports two RAM cells (RAM10/RAM9) for CMAC code and data, operated at the CMAC clock frequency and not in the system clock
- Parallelizes data flows from/to various masters on the system
- Allows for programmable priority scheme per RAM cell
- Can generate wait cycles to AHB in case of higher priority access

16.2 Architecture

There are five different masters accessing the memory RAM cells. Where two or more masters need access to the same RAM cell but different addresses (each on its own segment), then arbitration is used. To reduce multiplexing and timing constraints as much as possible different masters have access to a specific memory space range. An overview of the basic metrics of each master accessing a specific memory space range is shown in Table 115.

In general, grey areas designate that there is no actual access from the specific master to those cells. In this sense, no extra hardware is required to protect the corruption of the code space from SNC or CMAC Cortex M0+. Protection from the M33 point of view is achieved by means of the MPU. A single RAM cell (RAM8) is used as the common RAM space for inter-processor communication (mailboxes etc). Two memory cells (RAM9 and RAM10) can be used for CMAC code and data and they are in the CMAC clock domain (max frequency of 32 MHz). The access of these cells from the Cortex M33 is through an H2H bridge with wait states due to clock domain crossing. Furthermore, for the same reason, the shared memory cell (RAM8) is accessed from the CMAC Cortex M0+ through an H2H bridge with additional wait states.

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Table 115: Memory Access by Each System Master

RAM Cells	RAM Size (KB)	Main Use	AHB CPUC (M33 Cache Controller) (Note 2)		AHB CPUS (M33)		AHB DMA Masters		CMAC Cortex M0+ (Note 1)		SNC Cortex M0+	
			Start	End	Start	End	Start	End	Start	End	Start	End
RAM0	8	IVT& others	F000000	F002000								
RAM 1	32	SNC code	10000000	10008000	20000000	20008000	20000000	20008000			0	8000
RAM 2	32	SNC data	10008000	10010000	20008000	20010000	20008000	20010000			8000	10000
RAM 3	256		10010000	10050000	20010000	20050000	20010000	20050000				
RAM 4	128				20050000	20070000	20050000	20070000				
RAM 5	256				20070000	200B0000	20070000	200B0000				
RAM 6	256				200B0000	200F0000	200B0000	200F0000				
RAM 7	128				200F0000	20110000	200F0000	20110000				
RAM 8	128	All CPUs shared RAM			20110000	20130000	20110000	20130000	20100000	20120000	30000	50000
RAM 9	128	Extra CMAC code			20130000	20150000	20130000	20150000	30000	50000		
RAM 10	192	BLE stack code			20150000	20180000			0	30000		
RAM 11	4	MTB CMAC			20180000	20181000			80000	81000		
RAM 12	4	MTB M33			20181000	20182000						
RAM 13	4	MTB SNC			20182000	20183000					80000	81000

Note 1 RAM10/RAM9 and RAM11 are running in the CMAC clock.

Note 2 The remapping functionality in DA1470x supports remap RAM1 and RAM3 to address 0.

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All masters support a “Ready” like signal functionality so that they can be stalled for a specific amount of clock cycles. This makes the arbitration signals for the AHB interfaces (SysCPU, Display controller, GPU, and GP DMA) HREADY, while the memory interfaces (MTB) should also support a respective input (MREADY) and should only proceed in reading/writing the RAM cell if this signal is high. The CMAC CMI interface does not support any MREADY functionality, so it always has the highest priority.

An overview of the basic metrics of each master accessing the memory controller is shown in Table 116.

Table 116: Memory Controller Masters Access Metrics

Master	Frequency Range	Stall Mechanism	Access Rate	Wait States Tolerance
ARM M33 (AHB – CPUC)	32 MHz – 160 MHz	AHB HREADY	Non-burst accesses for data and/or code	Should be less than 4 AHB clocks to avoid performance degradation
ARM M33 (AHB – CPUS)	32 MHz – 160 MHz	AHB HREADY	Non-burst accesses for data and/or code	Should be less than 4 AHB clocks to avoid performance degradation
CMAC	32 MHz	None	Non-burst accesses for data and/or code	0
Sensor Node (SNC M0+)	2 MHz – 32 MHz	AHB HREADY	Non-burst accesses for data and/or code	It is application dependent.
AHB-DMA	32 MHz – 160 MHz	AHB HREADY	16-beat	Should be less than 6 AHB clocks to avoid performance degradation

The arbitration scheme is round robin which respects the wait states tolerance of each master. The maximum wait states tolerance for each of the master is programmable through the memory controller register file. Furthermore, the priorities of the masters for each of the eight arbitration engines (RAM1 to RAM8) are also programmable by SW.

16.3 Programming

Programmability is required for the range (Start and Stop addresses) of segments that need to be defined in the memory, depending on the type and size of the application. The following list contains the least number of segments needed for the proper operation of the system.

Table 117: Memory Segments Description

Segment Name	Description	Access	Start/Stop Address Registers
CMAC stack	Controller stack code and temporary variables	CMAC Cortex-M0+ (read, write) Cortex-M33 (write) DMA (write)	CMI_CODE_BASE_REG (Note 1) CMI_DATA_BASE_REG CMI_END_REG
CMAC Mailbox	Implements the structure which is used for exchanging commands and data between the 2 CPUs	CMAC Cortex-M0+ (read, write) Cortex-M33 (read, write)	
Cortex-M33 Code	Special code segment for SysCPU.	Cortex-M33 (read, write)	
Cortex-M33 Data	Application data space	Cortex-M33 (read, write)	

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Segment Name	Description	Access	Start/Stop Address Registers
		GP DMA (read, write)	
SNC	SNC space	SNC Cortex-M0+ (read) Cortex-M33 (read, write) GP DMA (read. write)	
SNC Data	Buffers for storing data read from Sensor Node Operation	SNC Cortex-M0+ (read, write) Cortex-M33 (read) GP DMA (read)	
System	IVT and others	0xF000000 – 0xF002000	

Note 1 This value should also be programmed in the Cortex-M33 MPU region 1 to ensure the Application does not corrupt CMAC code/data.

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17 Clock Generation

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

17.1 Clock Tree

The generation of the system's clocks is described in Figure 39.

The diagram shows the possible clock sources and all different divisions and multiplexing paths towards the generation of each block's clock. Also, the required registers that must be programmed are labeled on the same diagram. There are some main clock lines that are of interest:

- slp_clk (black bold line): this is the clock used for the sleep modes and can only be RCX, RCLP, or XTAL32K. In Table 118, the sleep clocks and their divided derivatives are summarized
- sys_clk (green line): this is the system clock, – used for the AMBA clock (hclk) – which runs the CPU, memories, and the bus. The source of this clock can be any oscillator, the PLL, or even an externally supplied digital clock
- divn_clk (red line): this is a clock that automatically adjusts the division factor on the sys_clk to always generate 32 MHz. This enables the dynamic activation of the PLL to provide more processing power at the CPU, without affecting the operation of blocks designed for 32 MHz

In general, the default clock of the system (sys_clk) is RCHS running at 96 MHz. XTAL32M is only enabled by CMAC or M33 if radio or PLL operations are needed respectively.

In Table 119 the system clocks and their divided derivatives are summarized.

Table 118: slp_clk Sources

Source	Speed	RCLP32k_Clk Divide Ratio
RCLP	32 kHz/512 kHz	1 or 16
RCX	~15 kHz	
XTAL32K	32 kHz	
External clock (XTAL32KP pin)	Any	

Table 119: Sys_clk Sources

Source	Speed	DivN_clk Divide Ratio
Xtal32M	32 MHz	1
PLL160M	160 MHz	5
RCHS	32 MHz/64 MHz/96 MHz	1/2/3
RCLP512K	512 kHz	

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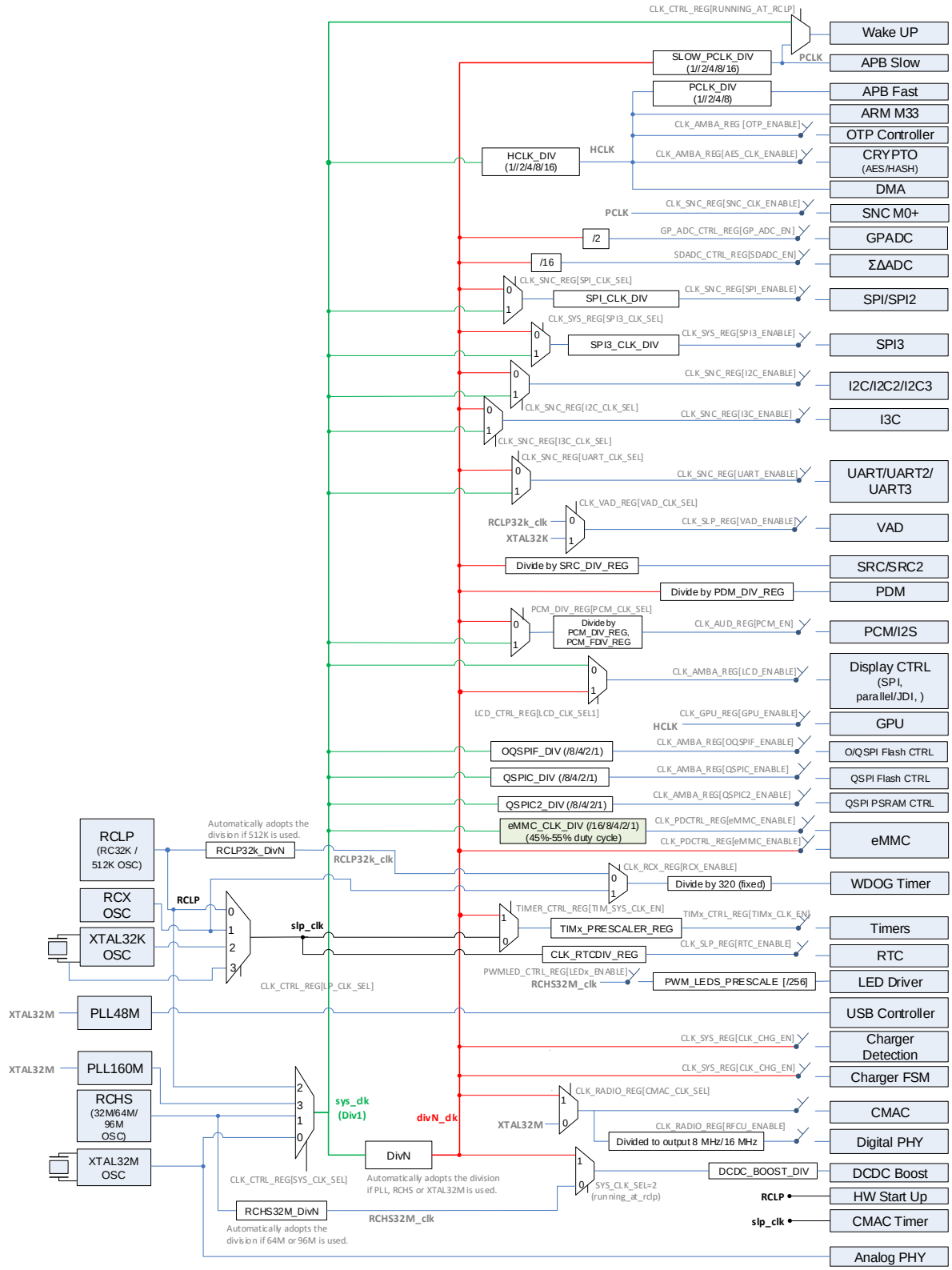

Figure 39: Clock Tree Diagram

17.2 Crystal Oscillators

The Digital Controlled Xtal Oscillators (DXCO) are designed for low-power consumption and high stability. There are two such crystal oscillators in the system, one at 32 MHz (XTAL32M) and a

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second at 32.768 kHz (XTAL32K). The 32.768 kHz oscillator has no trimming capabilities and is used as the clock of the Extended Sleep mode. The 32 MHz oscillator can be trimmed.

The principal schematic of the two oscillators is shown in Figure 40. No external components to the DA1470x are required other than the crystal itself. If the crystal has a case connection, it is advised to connect the case to the ground.

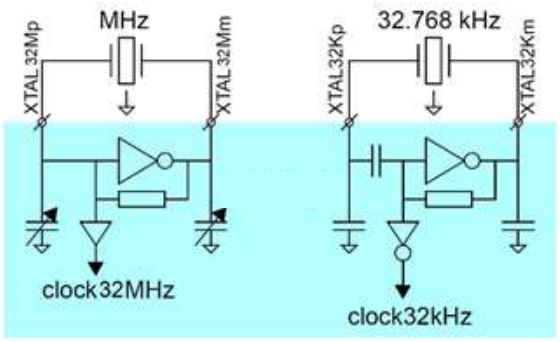

Figure 40: Crystal Oscillator Circuits

17.2.1 Frequency Control (32 MHz Crystal)

Register XTAL32M_TRIM_REG controls the trimming of the 32 MHz crystal oscillator. The frequency is trimmed by two on-chip variable capacitor banks. Both capacitor banks are controlled by the same register.

With XTAL32M_TRIM_REG[XTAL32M_TRIM] = 0x2BF the maximum capacitance, and minimum frequency is selected. With XTAL32M_TRIM_REG[XTAL32M_TRIM] = 0x000 the minimum capacitance, and maximum frequency is selected.

The ten least significant bits of the XTAL32M_TRIM_REG register (XTAL32M_TRIM bit field) directly control ten binary-weighted capacitors, as shown in Figure 41.

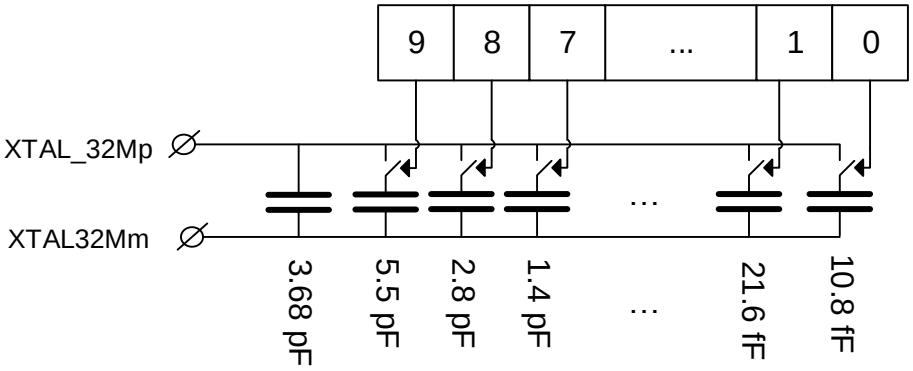

Figure 41: XTAL32MHz Oscillator Frequency Trimming

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17.3 RC Oscillators

The DA1470x has three RC oscillators:

- RCHS generates 32 MHz, 64 MHz, or 96 MHz
- RCLP generates 32 kHz or 512 kHz
- RCX generates ~15 kHz

The RCHS oscillator is powered by the LDO_V30 or LDO_V30_RET, during Active or Sleep Mode. The RCHS at 96 MHz is the default system clock and it has low jitter, when trimmed, to be able to be used for UART operations.

The RCLP oscillator operates on VDD (V12) and generates 32 kHz or 512 kHz. The main usage of the RCLP oscillator is for internal clocking during power-up or startup. The 512 kHz mode is used as a default system clock in the sleep mode, but it can be programmed to use the 32 kHz mode during sleep. It clocks the HW state machine which brings up the power management system of the chip. The enhanced RC oscillator (RCX) generates 15 kHz. The RCX oscillator can be used to replace the 32.768 kHz crystal, since it has a precision of < 500 ppm, while its output frequency is quite stable over temperature.

17.3.1 Frequency Calibration

The output frequency of the 32 kHz crystal oscillator and the three RC-oscillators can be measured relative to the DivN clock, using the on-chip reference counter.

The measurement procedure is as follows:

- REF_CNT_VAL = N (the higher N, the more accurate and longer the calibration will be)
- CLK_REF_SEL_REG[REF_CLK_SEL] = 0 (RCLP) or
  CLK_REF_SEL_REG[REF_CLK_SEL] = 1 (RCHS) or
  CLK_REF_SEL_REG[REF_CLK_SEL] = 2 (XTAL32K) or
  CLK_REF_SEL_REG[REF_CLK_SEL] = 3 (RCX)
  CLK_REF_SEL_REG[REF_CLK_SEL] = 5 (DIVN)
- Start the calibration: CLK_REF_SEL_REG[REF_CAL_START] = 1
- Wait until CLK_REF_SEL_REG[REF_CAL_START] = 0
- Read CLK_REF_VAL_REG = M (32-bits value)
- Frequency = (N/M) * 32 MHz

In the case of using the RCX as a sleep clock, the frequency calibration should be implemented at a frequency that ensures Bluetooth® LE connection maintenance.

17.4 PLL

There are two PLLs in DA1470x:

- PLL160M: The low-power PLL160M produces a 160 MHz clock with very high precision within a few us. It is used as a system clock to provide more processing power to the CPU, enabling 240 dMIPS, for computational hungry applications. The reference clock for this PLL is the XTAL32M
- PLL48M: The low-power PLL48M provides a 48 MHz clock for the operation of the USB Controller. The reference clock for this PLL is the XTAL32M

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18 OTP Controller

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

18.1 Introduction

The OTP controller realizes all functions of the 4-kB OTP macrocell. The controller facilitates all data transfers (reading and programming). The controller comprises two AHB slave interfaces, one for the configuration registers and the second for the actual OTP memory cell. The OTP memory space is transparently read by the CPU, but not transparently programmed.

The OTP controller operates on the AHB system clock. It takes care of the timing requirements of the various OTP cell operations using system clock tick values in configurable registers. The actual accesses to the OTP cell are performed at no more than 20 MHz, with the controller making sure this frequency constraint is always respected.

Features

- Implements all timing constraints for any access to the physical memory cell in a configurable manner
- Automatic Error Code Correction (ECC) – 6 bits (implemented by the OTP cell)
- 32-bits read in a single clock cycle from the OTP cell
- Single-word buffer for programming. No burst programming supported
- Empty words are 0xFFFFFFFF. Zeros are programmed per 32-bit word

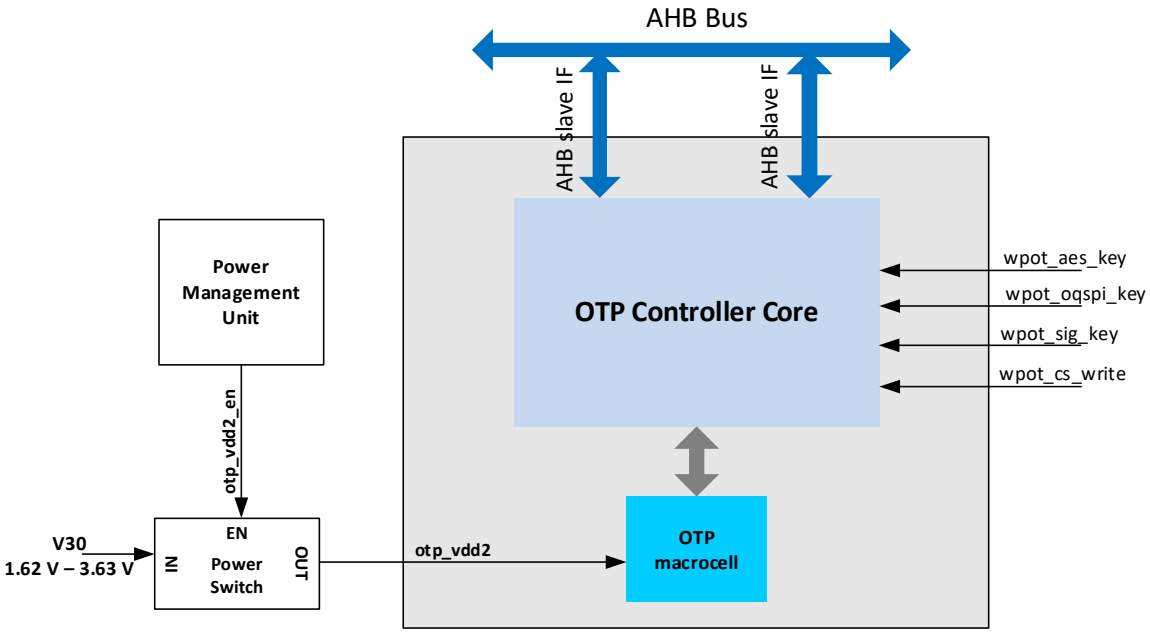

Figure 42: OTP Controller Block Diagram

18.2 Architecture

The OTP controller block includes the OTP macro-cell and pure digital logic implementing the controlling functions. The OTP memory communicates with the controller, through a proprietary interface. A power switch is used to control the power of the OTP cell driven by the power management unit of the system.

The internal organization of the OTP cell is 32 bits data + 6 bits ECC for each of the 1024 addressable positions. The 6 bits of the ECC are not accessible outside of the OTP cell. The ECC is

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generated during the programming by the OTP cell and is used during the reading again by the OTP cell, in a transparent way.

The system supplies four signals that enable write protection of four address ranges in the OTP memory. This protection prevents four specific address ranges of the OTP memory from being programmed. The request comes from four interface signals. The four address ranges (in byte address) and their corresponding interface signal that enables protection are:

- Range1: 0x0B00 – 0x0BFF, is protected when PROT_OQSPIF_KEY_WRITE is asserted
- Range2: 0x0A00 – 0x0AFF, is protected when PROT_AES_KEY_WRITE is asserted
- Range3: 0x08C0 – 0x09BF, is protected when PROT_SIG_KEY_WRITE is asserted
- Range4: 0x0C00 – 0x0FFF, is protected when RPOT_CS_WRITE is asserted

The first three address ranges host various encryption keys in the OTP cell: the encryption key of the AES algorithm in the OQSPIC, the encryption key for the general-purpose AES engine, and the signature public key. The fourth section host the configuration script.

The OTP controller configures the OTP cell to be in one of the following modes:

- **Deep Standby Mode (DSTBY).** In this mode, the required power supplies are applied to the OTP cell. However, the internal LDO of the OTP cell is inactive. The otp_vdd2_en signal is 1 and the otp_vdd2 should be at a functional voltage level (the VDD2 of the OTP cell is powered)
- **Standby Mode (STBY).** In this mode, the OTP cell is disabled by deactivating the chip select signal. The OTP cell is powered and the internal LDO is enabled. The power consumption of the OTP cell is not the lowest possible but is less than the power consumption in active mode. This is the state from which any active mode of operation (READ, PROG, PVFY, RINI) happens with the least delay
- **Read Mode (RD).** In this mode, the contents of the OTP cell are read at the respective AHB address space. This mode can be used for software execution in place (XIP). The OTP controller translates a read request into the corresponding control sequence for the OTP cell, to retrieve the requested data
- **Programming Mode (PROG).** The PROG mode provides the functionality for programming a 32-bit word into an OTP position. The OTP cell expands the 32-bit word by calculating and automatically appending a 6-bit checksum (ECC). Note that there is no way to access these extra 6-bits of the ECC information. Programming is performed only for bits equal to 0. Bits that are equal to 1 are bypassed to save on programming time. Because the ECC value is unknown to the controller, there are always six extra programming pulses applied for the ECC bits. Programming is done by issuing a programming request stored in the Programming Buffer (PBUF). PBUF consists of two configuration registers storing the 32-bit data value and the 10-bit address in the OTP cell where the value should be programmed. A new request can only be stored in PBUF when the previous is served. A status bit indicates if this has already been done and should therefore be monitored by SW before issuing a new programming request
- **Programming Verification Mode (PVFY).** The PVFY mode forces the OTP cell to enter in a special margin read mode. This mode is used to verify the content of the OTP positions that have been programmed using the PROG mode and that the programmed data is retrieved correctly under all the corner cases. When this mode is used, the contents of the OTP cell can be read, at the respective AHB address space. The CPU must read all OTP positions that have been programmed by accessing the corresponding addresses and verify that all the retrieved words are equal to the expected values
- **Read Initial State Mode (RINI).** The RINI mode implements a production test of the initial margin read, which should be performed in the OTP cell before the first programming is applied. This test verifies that the OTP cell is empty (all the bits are equal to 1). The OTP controller sends to the OTP cell the required control sequence to enables the test mode. Following that, the CPU should read all the content of the OTP cell at the respective AHB address space and verify that all the retrieved words are equal to 0xFFFFFFFF
  This specific read mode is a margin read, which means that is not equivalent to the normal read and should only be used for this purpose.

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18.3 Programming

There is a simple sequence of steps that needs to be followed to configure the OTP Controller:

1. Enable clock for OTP controller by setting the CLK_AMBA_REG[OTP_ENABLE] bit.
2. Put the OTP in standby mode (OTPC_MODE_REG[OTPC_MODE_MODE] = 0x1).
3. Wait OTP mode to change (OTPC_STAT_REG[OTPC_STAT_MRDY] = 1).
   a. Set OTP speed by writing OTPC_TIM1_REG and OTPC_TIM2_REG.
4. Perform an OTP access:
   a. Programming:
      i. Set up OTP write mode (OTPC_MODE_REG[OTPC_MODE_MODE] = 0x3).
      ii. Wait OTP mode to change (OTPC_STAT_REG[OTPC_STAT_MRDY] = 1).
      iii. Check OTPC_STAT_REG[OTPC_STAT_PBUF_EMPTY] = 1
      iv. Write OTPC_PWORD_REG the data to be programmed.
      v. Write OTPC_PADDR_REG the address that the data will be programmed to.
      vi. Wait until the programming is finished (OTPC_STAT_REG[OTPC_STAT_PRDY] = 1).
      vii. Switch to OTP verify mode (OTPC_MODE_REG[OTPC_MODE_MODE] = 0x4).
      viii. Wait OTP mode to change (OTPC_STAT_REG[OTPC_STAT_MRDY] = 1).
      ix. Read back and compare the data written.
      x. Put the OTP in standby mode (OTPC_MODE_REG[OTPC_MODE_MODE] = 0x1).
      xi. Wait OTP mode to change (OTPC_STAT_REG[OTPC_STAT_MRDY] = 1).
   b. Reading:
      i. Set up OTP read mode (OTPC_MODE_REG[OTPC_MODE_MODE] = 0x2).
      ii. Wait OTP mode to change (OTPC_STAT_REG[OTPC_STAT_MRDY] = 1).
      iii. Read OTP word.
      iv. Put the OTP in standby mode (OTPC_MODE_REG[OTPC_MODE_MODE] = 0x1).
      v. Wait OTP mode to change (OTPC_STAT_REG[OTPC_STAT_MRDY] = 1).

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19 Octa/Quad SPI FLASH Controller

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

19.1 Introduction

The Octa/Quad SPI Controller (OQSPIC) provides a low-pin count interface to FLASH memory devices. The OQSPIC supports the standard Serial Peripheral Interface (SPI) and a high-performance Dual/Quad/Octa SPI Interface. The OQSPIC gives the ability to read data from an octa/quad FLASH memory, transparently through the SPI bus. This Execute-In-Place (XIP) feature combined with the CPU cache provides comparable performance to executing code from embedded FLASH. In this case, the OQSPIC generates all the control signals for the SPI bus that are needed to read data from the serial FLASH memory. Additionally, the software can easily control the serial FLASH memory via a memory-mapped register file which is contained in the OQSPIC. All instructions supported by the FLASH memory can be programmed using the above register file.

Features

- SPI Modes:
  - Single: Data transfer via two unidirectional pins
  - Dual: Data transfer via two bidirectional pins
  - Quad: Data transfer via four bidirectional pins
  - Octa: Data transfer via eight bidirectional pins
- Auto Mode: up to 128 MB transparent Code access for XIP (Execute-In-Place) and Data access with 3-byte and 4-byte addressing modes
- Manual Mode: Direct register access using the QSPIC register file
- Up to 96 MHz OQSPI clock. Clock modes 0 and 3. Master mode only
- Vendor independent Instruction Sequencer
- Support for single access and high-performance burst mode, in combination with the cache controller (in Auto Mode)
- Use of a special read instruction in the case of a specific (programmable) wrapping burst access
- Erase suspend/resume support
- Support for Code and Data storage
- Decrypt on-the-fly (AES-256b-CTR) capability while in auto mode operation

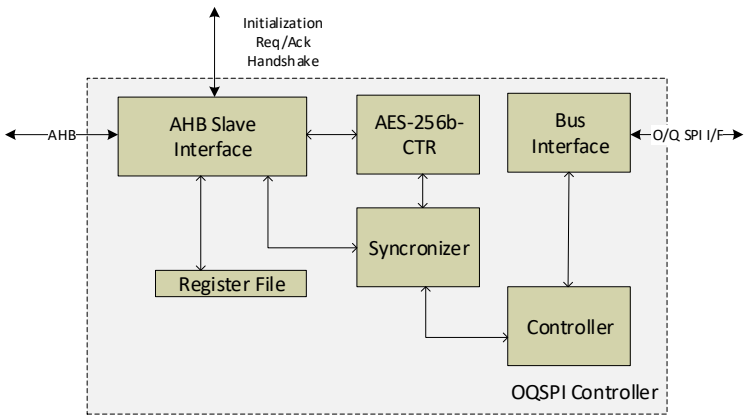

Figure 43: OQSPI FLASH Controller Block Diagram

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19.2 Architecture

The AHB slave block implements the AHB Slave interface which enables access to the register file. The Controller implements all protocols related to the functionality of the FLASH memory. It contains a finite state machine (FSM) that generates all necessary signaling to the OQSPI bus and realizes all features of the Auto mode operation. Moreover, it manages all data transfers between the two interfaces (the AHB and the O/Q SPI).

The Bus Interface block controls the O/Q SPI signals at the lowest level while the Synchronizer implements "stretching" or "shortening" of the signals that cross the two clock domains.

19.2.1 Interface

The Octa/Quad SPI Controller uses the following signals:

- OQSPIF_SCK: output serial clock
- OQSPIF_CS: Active Low output Chip select
- OQSPIF_IO0:
  - MOSI (output) in single SPI mode
  - IO0 (bidirectional) in Quad/Octa SPI mode
- OQSPIF_IO1:
  - MISO (input) in single SPI mode
  - IO1 (bidirectional) in Quad/Octa SPI mode
- OQSPIF_IO2:
  - WPn Write Protect output in single SPI mode
  - IO2 (bidirectional) in Quad/Octa SPI mode
- OQSPIF_IO3:
  - HOLDn/Resetn output in Single SPI mode
  - IO3 (bidirectional) at Quad/Octa SPI mode
- OQSPIF_IO4:
  - IO4 (bidirectional) at Octa SPI mode
- OQSPIF_IO5:
  - IO5 (bidirectional) at Octa SPI mode
- OQSPIF_IO6:
  - IO6 (bidirectional) at Octa SPI mode
- OQSPIF_IO7:
  - IO7 (bidirectional) at Octa SPI mode

The output drive of the pads is programmable via register bits OQSPIF_GP_REG[QSPI_PADS_DRV] and slew via OQSPIF_GP_REG[QSPI_PADS_SLEW].

The Octa/Quad SPI Controller (OQSPIC) drives all data pins constantly except for the case when a read is performed. The time for changing the direction of the pads is at least 1.5 x OQSPIF_CLK (OQSPIF_CLK being the clock that the FLASH operates on). In this way, data lines are always terminated thus reducing unnecessary power consumption.

The default state of the OQSPIF_IOx pins is 1. This state is applied at the pins as soon as the OQSPIC clock is enabled even if no access to the external FLASH has yet been triggered. The value of the pins might be changed by programming the respective registers (fields OSPIC_IOx_DAT, OSPIC_IOx_OEN of the OQSPIF_CTRLMODE_REG register). These values are applied immediately (delayed only by the pipeline of the controller).

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19.2.2 SPI Modes

The Octa/Quad SPI Controller (OQSPIC) supports the following SPI standards:

- Single: Data transfer via two unidirectional pins. The OQSPIC supports communication to any single/dual/quad or octa SPI FLASH memory. However, the Single SPI interface does not support bus modes 1 and 2, full-duplex communication, and any SPI slave mode
- Dual: Data transfer via two bidirectional pins
- Quad: Data transfer via four bidirectional pins
- Octa: Data transfer via eight bidirectional pins

19.2.3 Access Modes

The access to a serial FLASH connected to the O/Q SPI, use one of the modes:

- Auto mode
- Manual mode

These modes are mutually exclusive. The serial FLASH can operate only in one of the two modes. In auto mode, 3-bytes and 4-bytes addressing modes are supported. With OQSPIF_CTRLMODE_REG[OSPIC_USE_32BA]=0, up to 16 MB O/Q SPI (3-bytes addressing) can be accessed. If OSPIF_USE_32BA=1, 4-bytes addressing is enabled for accessing up to 128 Mbyte O/Q SPI FLASH.

Auto mode

In auto mode, read access from the serial FLASH memory is fully transparent to the CPU. Read access at the interface is translated by the OQSPIC into the respective SPI bus control commands needed for the FLASH memory access. When the Auto mode is disabled, any access (reading or writing) is ignored. When the Auto Mode is enabled, only read access is supported. Write access causes a hard fault. Read access can be single access, incremental burst, or wrapping burst. Wrapping burst is supported even when the FLASH device does not support any special instruction for wrapping burst. A special read instruction can be used in the case of a specific (programmable) wrapping burst access. When a FLASH supports a special instruction for wrapping burst access, it reduces access time (fewer wait states). For maximizing the utilization of the bus and minimizing the number of wait states, it is recommended to use burst accesses. However, non-sequential random accesses are supported with the cost of more wait states.

Manual Mode

In manual mode, the FLASH memory is controlled via a register file. All instructions that are supported by a FLASH memory can be programmed using the register file. Moreover, the mode of the interface (SPI, Dual SPI, Quad SPI, or Octa SPI) and the mode of operation (Auto or Manual mode) can be configured via this register file. The register file supports the following data sizes for reading and writing accesses: 8 bits, 16 bits, and 32 bits.

19.2.4 Endianness

The OQSPIC operates in little-endian mode. For 32-bit or 16-bit access (for read and write operations) to serial FLASH memory, the least significant byte comes first. For 32-bit access, the byte ordering is: data [7:0], data [15:8], data [23:16], data [31:24] while for 16-bit access the byte ordering is: data [7:0], data [15:8].

19.2.5 Erase Suspend/Resume

The OQSPI FLASH can be used for Data Storage, combining the EEPROM functionality + Program storage in one single device. For this purpose, the O/Q SPI ERASE/SUSPEND ERASE/RESUME commands are automatically executed as shown in Figure 44.

To store data in OQSPI FLASH, execution from O/Q SPI must temporarily be stopped by running directly from RAM or a cached program part. The sector selected for storage must be erased first, in

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case it contained data already. The process is implemented in an HW FSM and consists of the following steps:

1. The controller is in Auto mode and read requests are served. The Erase procedure is initiated by setting OSPIC_ERASE_EN=1, on the OQSPIF_ERASECTRL_REG register. The address of the sector that will be erased is defined at OSPIC_ERS_ADDR. When an Erase procedure is requested, the controller jumps to state 2.
2. Read requests are still served. As soon as the Read requests stop (also possible due to late bus master change, for example, DMA) and there is no new Read request for a few AHB clock cycles equal to OSPIC_ERSRES_HLD (OQSPIF_ERASE_CMDB_REG register), then OSPIC_WEN_INST and OSPIC_ERS_INST (OQSPIF_ERASECMDA_REG register) instructions are sent to the FLASH. The OSPIC_RESSUS_DLY (OQSPIF_ERASECMDB_REG register) counter is started and the controller jumps to state 3.
3. Erasing is in progress in FLASH and the OQSPI controller waits until one of the following events occur:
    a. A status check request. This request can be forced by writing OQSPIF_CHCKERASE_REG. The OQSPI controller then reads the status of the FLASH memory and check if erasing has finished. Reading of the status is delayed by OSPIC_RESSTS_DLY (OQSPIF_STATUSCMD_REG register) cycles or by OSPIC_RESSUS_DLY (OQSPIF_ERASECMDB_REG register) cycles. The first is based on the clock of the SPI bus, while the latter is on an internal 222 kHz clock. The selection between the two delays is configured by the OSPIC_STSDLY_SEL bit of the OQSPIF_STATUSCMD_REG register. If erasing has finished, the OQSPI controller returns to the normal operation (state 1) and sets OSPIC_ERASE_EN= 0, otherwise, it remains at state 3.
    b. A FLASH read data request on the AHB bus. The OQSPI controller reads the status of the FLASH memory and checks if erasing is done. The reading of the status is delayed again as in the previous case by OSPIC_RESSTS_DLY or OSPIC_RESSUS_DLY. If erasing has ended, the controller returns to normal operation (state 1) and sets OSPIC_ERASE_EN= 0. The read request is served as soon as the controller reaches state 1. If erasing has not ended, the controller proceeds to state 4.
4. The OSPIC_SUS_INST (OQSPIF_ERASECMDA_REG register) is sent as soon as the OSPIC_RESSUS_DLY/OSPIC_RESSTS_DLY counter is 0. The controller jumps to state 5.
5. The controller polls the FLASH status register until the FLASH device becomes ready (erasing is suspended). The controller then proceeds to state 6.
6. The erasing process in the FLASH is now suspended and the controller may read the FLASH. The requested data are retrieved from the FLASH device. If the reading on the AHB stops, (for example, Cache hit), and there are no new Read requests for a number of AHB clock cycles equal to OSPIC_ERSRES_HLD (OQSPIF_ERASECMDB_REG register), the controller goes to state 7.
7. The OSPIC_RES_INST instruction is applied, and the controller jumps back to state 3. Also, the OSPIC_RESSUS_DLY counter is started. As a result, the erase procedure is resumed.

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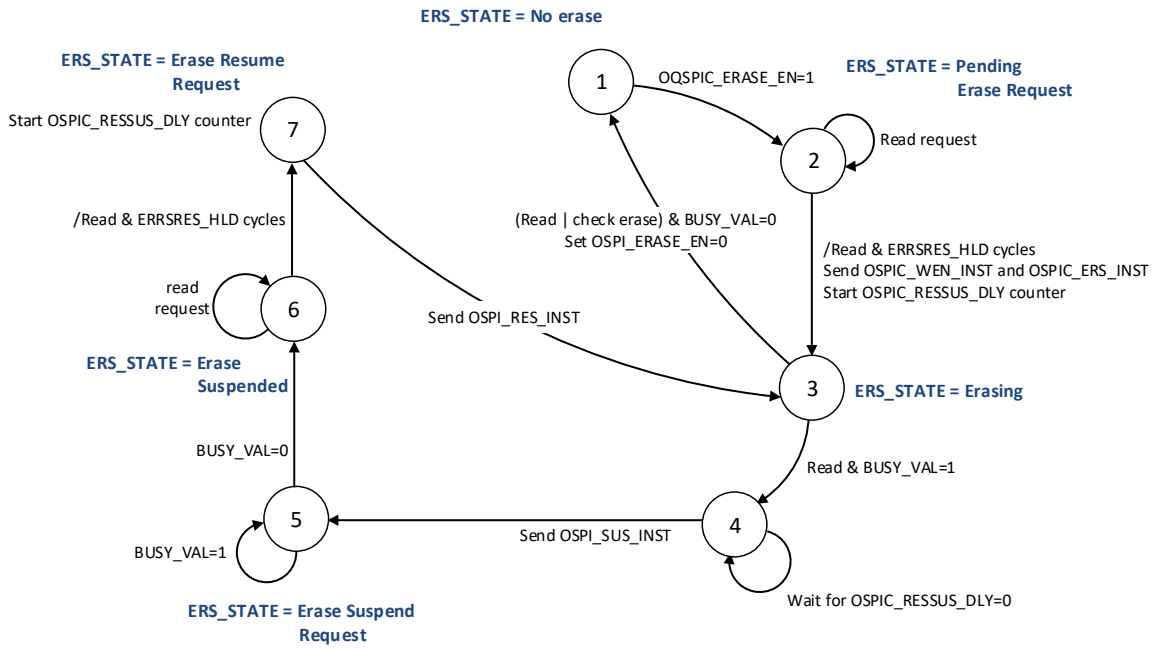

Figure 44: Erase Suspend/Resume in Auto Mode

Note that OSPI_RESSTS_DLY counts OQSPIF_CLK cycles, so before changing the OQSPIF_CLK, make sure that OSPI_RESSTS_DLY is set large enough to meet the timing parameter requirements of the FLASH device used.

19.2.6 On-the-Fly Decryption

The OQSPIC supports decryption of the data retrieved from the FLASH device, only when in Auto mode. FLASH contents should be encrypted already, using the same algorithm.

The address range that will be decrypted automatically by the controller, is defined in the OQSPIC by using two configuration registers, one for the start address (OQSPIF_CTR_SADDR_REG register), and one for the end address (OQSPIF_CTR_EADDR_REG register). The defined address range is 1024 bytes aligned. All addresses that are outside of this range are not be automatically decrypted, but fetched as is.

The on-the-fly decryption feature is based on the CTR mode of the AES encryption algorithm. The AES algorithm processes blocks of 128 bits. That means that the input and the output block of the AES are 128 bits or 16 bytes and as a result, data to be processed by the algorithm, are fragmented into blocks of 16 bytes. The key size that is used for the AES algorithm is 256 bits.

For the AES-256-CTR algorithm, only the cipher part of the AES algorithm is required. The general idea of the encryption process is based on the encryption of a 128-bit counter block (CTR). The initial value of the CTR is labeled as CTR0. The first counter block (CTR0) is encrypted with the help of the AES cipher, and the encrypted result is XORed with the first 16 bytes of the plaintext data (P0) to be encrypted. The counter block is incremented by one (CTR1 = CTR0 + 1) and is encrypted again. The result is XORed, with the next 16 bytes of the plaintext (P1), and so on, until all plaintext data are encrypted.

The AES CTR decryption is the same process as the encryption. By XORing again the ciphertext with the same encrypted counter value, the plaintext is retrieved. The decryption process can be described by equations as bellow:

For j=1 to m, do $CTR_j = CTR_{j-1} + 1$

For j=0 to m, do $P_j' = AES\_CIPH_k(CTR_j) \oplus C_j$

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Because accesses to the FLASH memory are random, the structure of the CTR block is selected to simplify the process. The total size of the counter block is 128 bits or 16 bytes namely: $CTRB_0$, $CTRB_1$, $CTRB_2$, $CTRB_3$, …, $CTRB_{14}$, $CTRB_{15}$.

The first 8 bytes ($CTRB_0$ - $CTRB_7$) of the counter block comprise the NONCE value and are programmed in the OQSPI Controller in configuration registers (OQSPIF_CTR_NONCE_*_REG). This is typically a random value and is the same for all the CTR_i blocks.

The next 4 bytes of the counter block ($CTRB_8$-$CTRB_{11}$) are always zero.

The last 4 bytes of the counter block ($CTRB_{12}$-$CTRB_{15}$), are produced automatically by the hardware, based on the 32-bit address offset OFFSET_ADDR [31:0] inside the encrypted range, where the data that should be decrypted are placed. If FLASH_ADDR[31:0] is the absolute address of a specific byte inside the encrypted range, the offset address is OFFSET_ADDR = FLASH_ADDR – OQSPIF_CTR_SADDR_REG[OSPIC_CTR_SADDR]. The four least significant bits of the address offset are truncated and the four most significant bits of the CTRB12 are padded with zeros. Thus, the zero value in bytes $CTRB_{12}$-$CTRB_{15}$ of the CTR is used for the first 16 bytes of the address range that is encrypted, the value 1 is used for the second 16 bytes of the address range, and so forth.

The final form of the counter block is the following:

{64 bits NONCE, 32 bits 0x0, 4 bits 0x0, OFFSET_ADDR[31:4]}

The four least significant bits of the address offset OFFSET_ADDR[3:0] define which of the AES_CIPHk(CTR_j) bytes should be used for the decryption of a specific byte of the encrypted block C_i.

In this way, the CTR block that should be used for the decryption of a specific byte, can be calculated immediately by the address of the byte in the FLASH and the start address of the encrypted range. This counter block supports up to 4 GB data, which covers the maximum supported size for the FLASH devices.

19.3 Programming

19.3.1 Auto Mode

In the case of Auto Mode of operation, the OQSPIC generates a sequence of control signals in SPI BUS. This sequence of control signals is analyzed to the following phases: instruction phase, address phase, extra byte phase, dummy clocks phase, and read data phase. These phases can be programmed via registers

- OQSPIF_BURSTCMDA_REG
- OQSPIF_BURSTCMDB_REG

Bits OSPIC_INST are used to set the selected instruction for the cases of incremental burst or single read access. If bit OSPIC_WRAP_MD is equal to 1, bit OSPIC_INST_WB can be used to set the used instruction for the case of a wrapping burst read access of length and size described by the bits OSPIC_WRAP_LEN and OSPIC_WRAP_SIZE respectively. In all other cases, the OSPIC_INST is the selected instruction.

If the instruction must be transmitted only in the first access after the selection of Auto Mode, then the OSPIC_INST_MD must be equal to 1.

To enable the extra byte phase set OSPIC_EXT_BYTE_EN=1 register. The transmitted byte during the extra byte phase is specified by the OSPIC_EXT_BYTE register. To disable (hi-Z) the output pads during the transmission of bits [3:0] of extra byte, set OSPIC_EXT_HF_DS = 1.

The number of dummy bytes during the dummy clocks phase is specified by OSPIC_DMY_NUM and enabled by OSPIC_DMY_EN in the OQSPIF_BURSTCMDB_REG register.

The SPI BUS mode during each phase can be set with register bits:

- OSPIC_INST_TX_MD for the instruction phase
- OSPIC_ADR_TX_MD for the address phase
- OSPIC_EXT_TX_MD for the extra byte phase

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- OSPIC_DMY_TX_MD for the dummy byte phase
- OSPIC_DAT_RX_MD for the read data phase

If the Quad SPI mode is selected in any of the above phases, write 0 to the OSPIC_IO3_OEN and OSPIC_IO2_OEN.

If the FLASH Memory needs to be accessed with any instruction but the read instruction, then the Manual Mode must be used. The final step to enable the use of Auto Mode of operation is to set the OSPIC_AUTO_MD equal to 1.

19.3.2 Manual Mode

For the Manual mode, OSPIC_AUTO_MD must be equal to zero. Manual operation of the bus signals is done via OQSPIF_CTRLBUS_REG:

- The start/end of access can be controlled using bits OSPIC_EN_CS and OSPIC_DIS_CS respectively
- The SPI bus mode of operation can be configured with bits OSPIC_SET_SINGLE, OSPIC_SET_DUAL and OSPIC_SET_QUAD

Writing to the OQSPIF_WRITEDATA register is generating a data transfer from the OQSPIC to the SPI bus. Read access at the OQSPIF_READDATA register is generating a data transfer from the SPI bus.

Writing to the OQSPIF_DUMMYDATA register is generating a few dummy clock pulses to the SPI bus.

When access to the SPI bus via OQSPIF_WRITEDATA, OQSPIF_READDATA, and OQSPIF_DUMMYDATA is very slow, most probably the delay in accessing the internal AHB is large. In this case, set the OSPIC_HRDY_MD register equal to 1 to increase priority when accessing the required registers. All masters of the SoC can access the AHB bus interface without waiting for the SPI Bus access completion. Polling of the OSPIC_BUSY register must be done to check the end of the activity at the SPI bus, before issuing any more accesses. If a read transaction is finished, OQSPIF_RECVDATA contains the received data.

The state and the value of the OSPI_IO[3:2] are specified by the following registers bits:

- OSPIC_IO3_OEN, OSPIC_IO3_DAT (Used for the WPn, Write Protect function)
- OSPIC_IO2_OEN, OSPIC_IO2_DAT respectively (Used for the HOLDn function)

19.3.3 Clock Selection

The SPI clock mode as set with bit OSPIC_CLK_MD The supported modes for the generated SPI clock is:

- 0 = Mode 0. The OQSPI_SCK is low when the bus is idle (OQSPI_CS is high)
- 1 = Mode 3. The OQSPI_SCK is high when the bus is idle (OQSPI_CS is high)

The OQSPI_CLK frequency has a programmable divider CLK_AMBA_REG[OQSPIF_DIV] which divides SYS_CLK by 1,2,4,8. The OQSPI_CLK can be faster or slower than HCLK.

19.3.4 Receiving Data

The standard method to sample received data is by using the positive edge of the OQSPI_SCK. However, when the output delay of the FLASH memory is high, a timing problem on the read path is very likely. For this reason, the QSPIC can be programmed to sample the received data with the negative edge of the OQSPI_SCK. This is configured with the OSPIC_RXD_NEG register.

Furthermore, the receive data can be pipelined by setting OSPIC_RPIPE_EN = 1 and the sampling clock can be delayed using OSPIC_PCLK_MD. This enables sampling the received data later than the actual clock edge allows.

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19.3.5 Delay Line Configuration

When VDD = 0.9 V (POWER_LVL _REG[V12_LEVEL] = 0x1) and OQSPI_CLK = 32 MHz, the OQSPIF_CTRLMODE_REG[OSPIC_PCLK_MD] bit field should be equal to 2. On the contrary, if VDD = 1.2 V then OQSPIF_CTRLMODE_REG[OSPIC_PCLK_MD] bit field should be equal to 7.

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20 Quad SPI FLASH/RAM Controllers

Device	DA14701	DA14705	DA14706	DA14708
Number of QSPI controllers	2	1	2	2

20.1 Introduction

The two Quad SPI FLASH/RAM Controllers (QSPIC and QSPIC2) provide a low-pin count interface to serial QSPI FLASH/RAM devices. The controllers support the standard Serial Peripheral Interface (SPI) and a high-performance Dual/Quad SPI Interface. The RAM feature provides a low-cost RAM extension for infrequently used data.

The QSPIC/QSPIC2 automatically generates all the control signals for the QSPI bus needed to access data from the serial quad memory. The controller has a vendor-independent register file that provides a rich set of control fields for a wide range of the FLASH/RAM devices.

Features

- SPI modes:
  - Single: Data transfer via two unidirectional pins
  - Dual: Data transfer via two bidirectional pins
  - Quad: Data transfer via four bidirectional pins
- Auto mode: up to 128 MB memory-mapped Read/Write Data access with 3-byte and 4-byte addressing modes
- Manual mode: Direct register access using the QSPIC/QSPIC2 register file
- QSPI clock up to 96 MHz. Clock modes 0 and 3. Master mode only
- Vendor independent Instruction Sequencer
- In Auto mode, the FLASH control signals are fully programmable
- Use of a special read instruction in the case of a specific (programmable) wrapping burst access
- Erase suspend/resume support
- Support for Code and Data storage

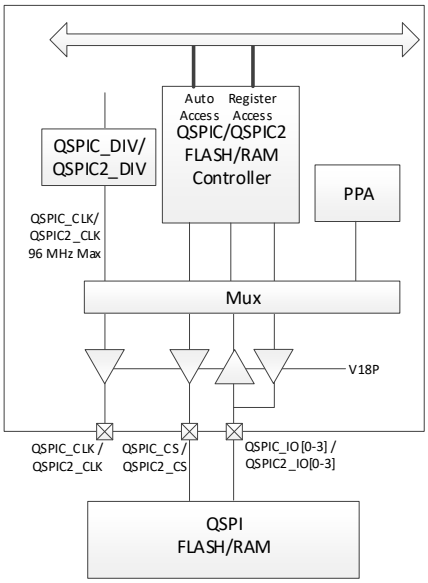

Figure 45: QSPIC FLASH Controller Block Diagram

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20.2 Architecture

20.2.1 Interface

The Quad SPI Controllers use the following signals:

- QSPIC_CLK/QSPIC2_CLK: output serial clock
- QSPIC_CS/QSPIC2_CS: Active Low output Chip select
- QSPIC_IO0/QSPIC2_IO0:
  - DO (output) in Single SPI mode
  - IO0 (bidirectional) in Dual/Quad SPI mode
- QSPIC_IO1/QSPIC2_IO1:
  - DI (input) in Standard SPI mode
  - IO1 (bidirectional) in Dual/Quad SPI mode
- QSPIC_IO2/QSPIC2_IO2:
  - General-purpose (output) (for example, WPn Write Protect) in Standard SPI mode
  - IO2 (bidirectional) in Quad SPI mode
- QSPIC_IO3/QSPIC2_IO3:
  - General-purpose (output) (for example, HOLDn) in Single SPI mode
  - IO3 (bidirectional) in Quad SPI mode

20.2.2 SPI Modes

The Quad SPI Controllers (QSPIC/QSPIC2) support the following SPI standards:

- Single: Data transfer via two unidirectional pins. The QSPIC/QSPIC2 supports communication to any single/dual or Quad SPI FLASH memory. In contradiction to the Standard SPI interface, the supported Single SPI interface does not support the bus modes 1 and 2, full-duplex communications, and any SPI slave mode
- Dual: Data transfer via two bidirectional pins
- Quad: Data transfer via four bidirectional pins

20.2.3 Access Modes

Access to a serial memory (FLASH or RAM) connected to the QSPIC/QSPIC2 can be done in two modes:

- Auto mode
- Manual mode

These modes are mutually exclusive. The serial memory can be controlled only in one of the two modes. The registers which control the mode of operation can be used at any time. In the following sections, the registers of the QSPIC are used as references. The register names for QSPIC2 are the same with the prefix QSPIC2 instead of QSPIC.

In Auto mode, 3-byte and 4-byte addressing modes are supported. With QSPIC_USE_32BA = 0, up to 16 MB serial memory (3-byte addressing) can be accessed. If QSPIC_USE_32BA = 1, the 4-byte addressing is enabled for accessing up to 128 MB serial memory.

Auto Mode FLASH Access

In auto mode (QSPIC_AUTO_MD = 1), the read access to a serial FLASH memory is performed in a fully transparent way through the SPI bus. Read access to the memory space, where the external memory is mapped, is translated by the controller to the respective SPI bus command sequence, which is needed for the retrieving of the requested data from the serial FLASH memory.

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When the auto mode is disabled (QSPIC_AUTO_MD = 0), any access (reading or writing) to the mapped memory space is ignored by the controller.

Only read accesses are supported when the connected external device is a FLASH memory (QSPIC_SRAM_EN = 0). Write access causes a hard fault at the CPU.

The read access can be single access or incremental burst or wrapping burst access. The wrapping burst is supported even when the controlled serial FLASH doesn't support any special instruction for wrapping burst. A special read instruction can be used in the case of a specific (programmable) wrapping burst access. When a serial FLASH supports a special instruction for wrapping burst access, this feature saves access time (fewer wait states). For maximizing the utilization of the bus and minimizing the number of wait states, it is recommended to be used burst accesses. However, non-sequential random accesses are supported with the cost of more wait states.

Auto Mode RAM Access

In the case where it is connected to a serial RAM device, the QSPIC/QSPIC2 controller can provide read/write functionality.

The special configuration register must be programmed to enable the RAM functionality (QSPIC_SRAM_EN = 1). As in the case where the external device is a FLASH, the auto mode must also be enabled (QSPIC_AUTO_MD = 1). In the case where the auto mode is disabled (QSPIC_AUTO_MD = 0), any access (reading or writing) in the memory space, where the external device has been mapped, is ignored by the QSPI controller.

The read access in the memory space of the external serial RAM is done in a fully transparent way through the QSPI bus. The capability of the controller to handle the various types of read accesses is the same as in the case of the FLASH device. Single access, incremental burst, or wrapping burst are all supported.

Write access to the memory space where the external memory is mapped, does not cause a hard fault to the CPU. On the contrary, the write access is interpreted by the QSPIC/QSPIC2 in the respective QSPI bus protocol, and the write data is stored in the external RAM device.

The controller is capable of handling write accesses of all kinds of burst: single access, incremental burst, or wrapping burst access. The throughput that can be achieved varies depending on the burst length, the word width, the cost of the protocol of the external memory device, and the frequency of the QSPI clock.

Burst accesses provide the highest throughput. The non-sequential random accesses are supported at the cost of more wait states. The maximum throughput that can be achieved, depends on the burst length.

Manual Mode

In manual mode, the external serial memory is controlled via a register file. All instructions that are supported by the serial memory can be programmed by using the register file. Moreover, the mode of the interface (SPI, Dual SPI, Quad SPI) and the mode of operation (Auto or Manual mode) can be configured via this register file. The register file supports the following data sizes for reading and writing accesses: 8-bits, 16-bits, and 32 bits.

20.2.4 Endianness

The QSPIC/QSPIC2 controllers operate in little-endian mode. For 32-bit or 16-bit access (for read and write operations) to a serial memory, the least significant byte comes first. For 32-bit access, the byte ordering is: data [7:0], data [15:8], data [23:16], data [31:24] and for 16-bit access the byte ordering is: data [7:0], data [15:8].

20.2.5 Erase Suspend/Resume

A QSPI FLASH memory can be used for data storage, combining the EEPROM functionality + Program storage in one single device.

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For this purpose, the QSPI ERASE/SUSPEND ERASE/RESUME are automatically executed as shown in Figure 46.

To store data in QSPI FLASH memory, the sector designated for storage must be erased first.

The ERASE/SUSPEND ERASE/RESUME process is only meaningful if the external device is a serial FLASH memory (QSPIC_SRAM_EN=0).

Erase procedure

1. The controller is in Auto mode and the read requests are served. The Erase procedure is initiated by setting QSPIC_ERASE_EN=1. The address of the sector that is erased is defined by the QSPIC_ERS_ADDR. When an Erase procedure is requested, the controller enters state 2.
2. The read requests are still served. As soon as the Read requests stop (also possible due to late bus master change, for example, DMA) and there is no new Read request for a number of AHB clock cycles equal to QSPIC_ERSRES_HLD, the QSPIC_WEN_INST, and the QSPIC_ERS_INST instructions are sent to the QSPI FLASH. The QSPIC_RESSUS_DLY counter is started. After this, the controller enters state 3.
3. The erasing is in progress in the QSPI FLASH memory. The QSPI controllers wait for one of the following:
   a. A status check request. This request can be forced by writing QSPIC_CHCKERASE_REG. This makes the QSPIC/QSPIC2 controller read the FLASH memory status and checks the end of *erasing*. Reading the status is delayed by QSPIC_RESSTS_DLY cycles or by QSPIC_RESSUS_DLY cycles. The QSPIC_RESSTS_DLY delay is based on the SPI bus clock, while the QSPIC_RESSUS_DLY delay is based on a 288 kHz clock. The selection between the two delays is configured with the help of the QSPIC_STSDLY_SEL bit. After erasing, the QSPIC/QSPIC2 controller returns to the normal operation (state 1) and sets QSPIC_ERASE_EN = 0, otherwise, it remains in state 3.
   b. A read data request on the AHB bus. The QSPIC/QSPIC2 controller reads the status of the FLASH memory and checks the end of erasing. Status reading is delayed again by QSPIC_RESSTS_DLY cycles or QSPIC_RESSUS_DLY cycles. The QSPIC_STSDLY_SEL bit does the Selection between the two delays. At the end of erasing, the controller returns to normal operation (state 1) and sets QSPIC_ERASE_EN = 0. The read request is served in state 1. If the erasing has not ended, the controller proceeds to state 4.
4. The QSPIC_SUS_INST is sent as soon as the QSPIC_RESSUS_DLY counter is 0. The controller enters state 5.
5. The controller reads the status register until the FLASH device is ready (erasing is suspended). When the FLASH device is ready, the controller enters state 6.
6. Erasing process in the FLASH is suspended and the controller can read the FLASH. The requested data is retrieved from the FLASH device. If the reading on the AHB stops and there is no new Read request for a number of AHB clock cycles equal to QSPIC_ERSRES_HLD, the controller enters state 7.
7. The QSPIC_RES_INST instruction is applied and state 3 is entered. Also, the QSPIC_RESSUS_DLY counter is started. The QSPIC_RES_INST makes sure the erase procedure is continued (erase resume) in the flash device.

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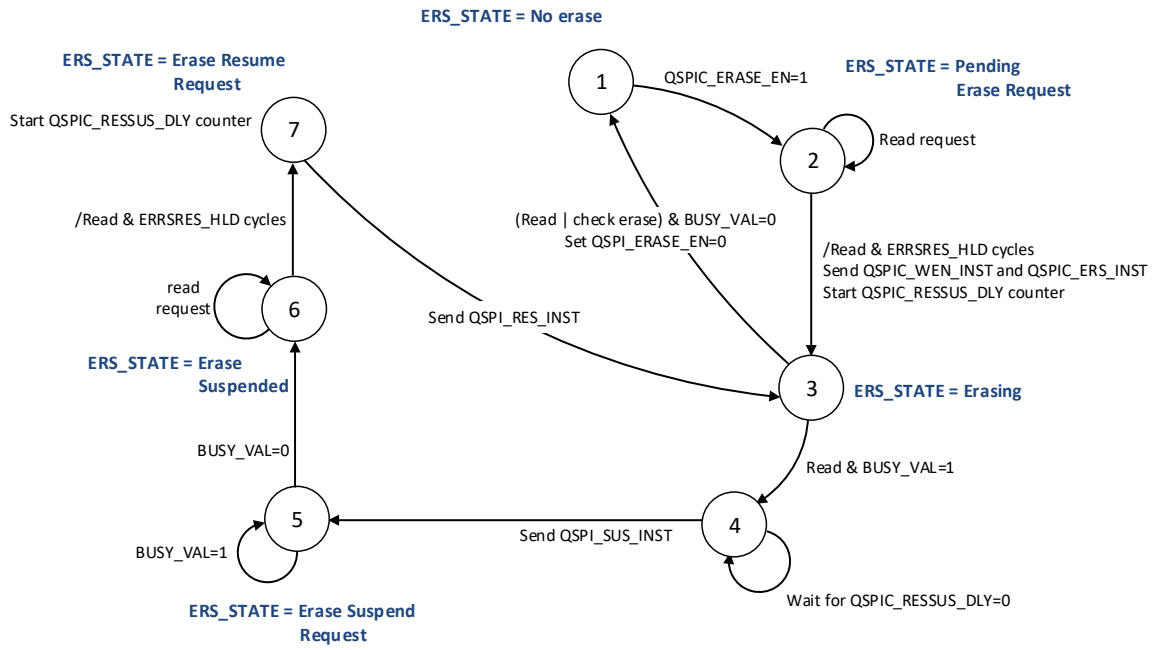

Figure 46: Erase Suspend/Resume in Auto Mode

Note that QSPIC_RESSTS_DLY is counted with the QSPIC_CLK, so before changing the QSPIC_CLK, make sure that QSPIC_RESSTS_DLY is set large enough to meet the timing parameter requirements.

QSPI FLASH Programming Procedure

Sectors are programmed in manual mode by polling the status bit in the QSPI FLASH. During programming, the CPU should not run code from this FLASH device. Also, interrupts must be disabled while executing the write command to the FLASH.

Byte programming is relatively short, so a polling loop could be acceptable to meet system latency requirements.

20.2.6 Low Power Considerations

To reduce the power dissipation in the QSPI FLASH, the QSPIC_CLK must always be the highest possible system clock to keep the burst access to the FLASH as short as possible. The CPU must run as slow as possible for minimum power.

For the lowest power with a slow CPU (for example, 2 MHz) and high QSPIC_CLK (for example, 32 MHz) bit, QSPIC_CTRLMODE_REG[QSPIC_FORCENSEQ_EN] must be set to 1. This enables split burst mode, reducing the power dissipation during active burst only while disabling the FLASH when the burst is done compared to high-efficiency burst. These two modes are explained in Figure 47 and Figure 48.

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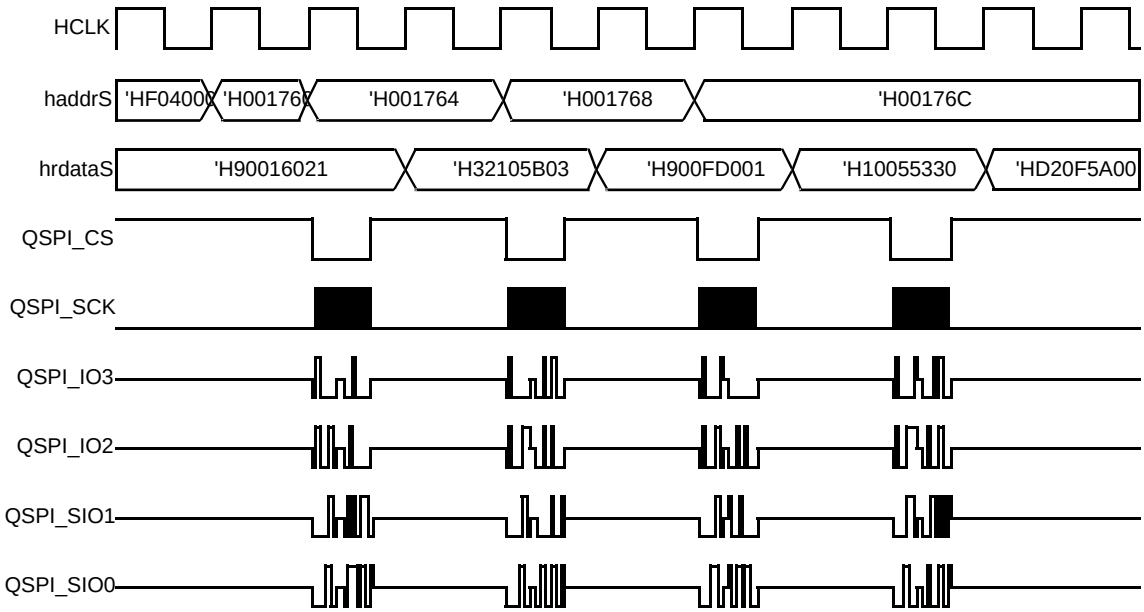

Figure 47: QSPI Split Burst Timing for Low Power (QSPIC_FORENSEQ_EN = 1)

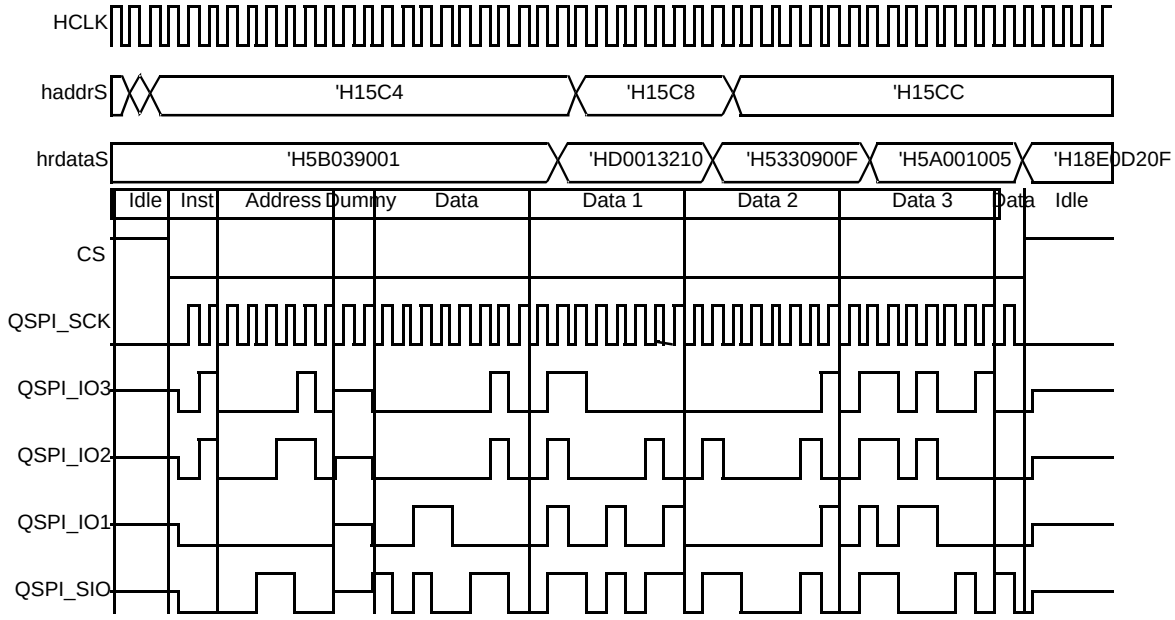

Figure 48: QSPI Burst Timing for High Performance (QSPIC_FORENSEQ_EN = 0)

If QSPIC_FORCENSE_EN = 0, the QSPIC reads data in a burst address1/extra/dummy/data1, data2, dataN, keeping the QSPIC_CS low during the complete burst. If set to 1, the burst is split into non-sequential accesses address1/extra/dummy/data1, address2/extra/dummy/data2, and so forth, making the QSPIC_CS high between the accesses.

20.3 Programming

In the following sections, the registers of the QSPIC are used as reference. The register names for QSPIC2 are the same with the prefix QSPIC2 instead of QSPIC.

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20.3.1 QSPI Flash Operation

20.3.1.1 Auto Mode

In the case of Auto Mode of operation, the QSPIC/QSPIC2 generates a sequence of control signals in SPI BUS. This sequence of control signals is analyzed into the following phases: instruction phase, address phase, extra byte phase, dummy clocks phase, and read data phase. These phases can be programmed via registers:

- QSPIC_BURSTCMDA_REG
- QSPIC_BURSTCMDB_REG

Bits QSPIC_INST are used to set the selected instruction for the cases of incremental burst or single read access. If bit QSPIC_WRAP_MD is equal to 1, bit QSPIC_INST_WB can be used to set the used instruction for the case of a wrapping burst read access of length and size described by the bits QSPIC_WRAP_LEN and QSPIC_WRAP_SIZE respectively. In all other cases, the QSPIC_INST is the selected instruction.

If the instruction must be transmitted only in the first access after the selection of Auto Mode, then the QSPIC_INST_MD must be equal to 1.

To enable the extra byte phase set QSPIC_EXT_BYTE_EN = 1 register. The transmitted byte during the extra byte phase is specified by the QSPIC_EXT_BYTE register. To disable (hi-Z) the output pads during the transmission of bits [3:0] of extra byte, set QSPIC_EXT_HF_DS = 1.

The number of dummy bytes during the dummy clocks phase is specified by the register QSPIC_DMY_NUM and enabled by QSPIC_DMY_FORCE.

The SPI BUS mode during each phase can be set with register bits:

- QSPIC_INST_TX_MD for the instruction phase
- QSPIC_ADR_TX_MD for the address phase
- QSPIC_EXT_TX_MD for the extra byte phase
- QSPIC_DMY_TX_MD for the dummy byte phase
- QSPIC_DAT_RX_MD for the read data phase

If the Quad SPI mode is selected in any of the above phases, write 0 to the QSPIC_IO3_OEN and QSPIC_IO2_OEN.

If the FLASH Memory needs to be accessed with any instruction but the read instruction, then the Manual Mode must be used. The final step to enable the use of the Auto mode of operation is to set the QSPIC_AUTO_MD equal to 1.

20.3.1.2 Manual Mode

For the Manual mode, QSPIC_AUTO_MD must be equal to zero. Manual operation of the bus signals is done via QSPIC_CTRLBUS_REG:

- The start/end of access can be controlled using bits QSPIC_EN_CS and QSPIC_DIS_CS respectively
- The SPI bus mode of operation can be configured with bits QSPIC_SET_SINGLE, QSPIC_SET_DUAL and QSPIC_SET_QUAD

Writing to the QSPIC_WRITEDATA register is generating a data transfer from the QSPIC to the SPI bus. Read access at the QSPIC_READDATA register, is generating a data transfer from the SPI bus.

Writing to the QSPIC_DUMMYDATA register is generating a few dummy clock pulses to the SPI bus.

When access to the SPI bus via QSPIC_WRITEDATA, QSPIC_READDATA, and QSPIC_DUMMYDATA is very slow, most probably the delay in accessing the internal AHB is large. In this case, set the QSPIC_HRDY_MD register equal to 1 to increase priority when accessing the required registers. All masters of the SoC can access the AHB bus interface without waiting for the SPI Bus access completion. Polling of the QSPIC_BUSY register must be done to check the end of the activity at the SPI bus, before issuing any more accesses. If a read transaction is finished, QSPIC_RECVDATA contains the received data.

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The state and the value of the QSPI_IO[3:2] are specified by the following registers bits:

- QSPIC_IO3_OEN, QSPIC_IO3_DAT (Used for the WPn, Write Protect function)
- QSPIC_IO2_OEN, QSPIC_IO2_DAT respectively (Used for the HOLDn function)

20.3.1.3 Clock Selection

The SPI clock mode is set with bit QSPIC_CLK_MD. The supported modes for the generated SPI clock are:

- 0 = Mode 0. The QSPI_SCK is low when the bus is idle (QSPI_CS is high)
- 1 = Mode 3. The QSPI_SCK is high when the bus is idle (QSPI_CS is high)

The QSPI_CLK frequency has a programmable divider CLK_AMBA_REG[QSPIC_DIV/QSPIC2_DIV] which divides the SYS_CLK by 1,2,4,8.

The QSPI_CLK can be faster or slower than HCLK.

20.3.1.4 Receiving Data

The standard method to sample received data is by using the positive edge of the QSPI_SCK. However, when the output delay of the FLASH memory is high, a timing problem on the read path is very likely. For this reason, the QSPIC can be programmed to sample the received data with the negative edge of the QSPI_SCK. This is configured with the QSPIC_RXD_NEG register.

Furthermore, the receive data can be pipelined by setting QSPI_RPIPE_EN=1 and the sampling clock can be delayed using QSPI_PCLK_MD. This enables sampling of the received data later than the actual clock edge allows.

20.3.1.5 Delay Line Configuration

When VDD = 0.9 V (POWER_LVL_REG[V12_LEVEL] = 0x1) and QSPI_CLK = 32 MHz, the QSPIC_CTRLMODE_REG[QSPIC_PCLK_MD] bit field should be equal to 2. On the contrary, if VDD = 1.2 V, then QSPIC_CTRLMODE_REG[QSPIC_PCLK_MD] bit field should be equal to 7.

20.3.2 QSPI PSRAM Operation

20.3.2.1 Auto Mode

Chip Selection

In Auto mode, QSPI executes from address 0. Notice that certain PSRAM RAM devices (for example, APmemory APS6404L) connected to the QSPI interface have a minimum time t_{CEM} that the #CE may stay low. SW must make sure that the QSPI CLK is not going too slow during a burst, otherwise, RAM data might get lost.

Read Burst in Auto Mode

In the case of a read from the external device, in Auto mode, the QSPI controller generates a sequence of control signals. This is analyzed in the following phases: instruction phase, address phase, extra byte phase, dummy clocks phase, and read data phase. These phases can be programmed via registers QSPIC_BURSTCMDA_REG and QSPIC_BURSTCMDB_REG.

Bits QSPIC_INST are used to set the selected instruction for the cases of incremental burst or single read access. If bit QSPIC_WRAP_MD is equal to 1, bits QSPIC_INST_WB can be used to set the used instruction for a wrapping burst read access. The length and size are described by the bits QSPIC_WRAP_LEN and QSPIC_WRAP_SIZE respectively. In all other cases, the QSPIC_INST is the selected instruction.

If an instruction is to be transmitted only during the first access after the selection of Auto mode, the QSPIC_INST_MD must be equal to 1.

To enable the extra byte phase, set 1 to the QSPIC_EXT_BYTE_EN register. The transmitted byte during the extra byte phase is specified from the QSPIC_EXT_BYTE register. To disable (hi-z) the

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output pads during the transmission of bits [3:0] of extra byte, write 1 to the QSPIC_EXT_HF_DS register.

The number of dummy bytes during the dummy clocks phase is specified at QSPIC_DMY_NUM.

The SPI BUS mode during each phase can be configured as follows:

- QSPIC_INST_TX_MD for the instruction phase
- QSPIC_ADR_TX_MD for the address phase
- QSPIC_EXT_TX_MD for the extra byte phase
- QSPIC_DMY_TX_MD for the dummy byte phase
- QSPIC_DAT_RX_MD for the read data phase.

If the Quad SPI mode is selected in any of the above phases, write 0 to the QSPIC_IO3_OEN and QSPIC_IO2_OEN.

If the serial FLASH Memory must be prepared for reading with the use of any instruction except the read instruction, then the Manual mode must be used for the programming of the above instructions.

The final step to enable the use of the Auto mode of operation is to set the QSPIC_AUTO_MD equal to 1.

Write Bursts in Auto Mode

In the case where the connected memory is a serial PSRAM, the controller can serve requests for write accesses. This is implemented, as in the case of the read burst, when the Auto mode of operation is active (QSPIC_AUTO_MD = 1). Additionally, the external device must be declared to the QSPI controller as a serial RAM (QSPIC_SRAM_EN = 1).

Under these conditions, the QSPI controller generates a sequence of control signals in SPI BUS, for each request for write burst access toward the external device. This sequence of control signals is analyzed in the following phases: instruction phase, address phase, extra byte phase, and write data phase. These phases can be programmed via the register QSPIC_AWRITECMD_REG.

Bits QSPIC_WR_INST are used to define the write instruction. This instruction is used for all the cases of bursts: single access, incremental burst, or wrapping burst. The controller handles them accordingly to implement all the lengths of the bursts.

The SPI BUS mode during each phase can be set by the register bits:

- QSPIC_WR_INST_TX_MD for the instruction phase
- QSPIC_WR_ADR_TX_MD for the address phase
- QSPIC_WR_DAT_TX_MD for the read data phase

If the serial RAM must be configured with a special command sequence prior to the write instruction, Manual mode must be used.

20.3.2.2 Manual Mode

For the Manual mode, QSPIC_AUTO_MD must be equal to zero. Manual operation of the bus signal is done via QSPIC_CTRLBUS_REG:

- Start /End of access can be controlled using bits QSPIC_EN_CS and QSPIC_DIS_CS respectively
- SPI mode configured with bits QSPIC_SET_SINGLE, QSPIC_SET_DUAL, and QSPIC_SET_QUAD

Writing to the QSPIC2_WRITEDATA register generates a data transfer from the QSPIC to the SPI bus. Read access at the QSPIC_READDATA register generates a data transfer from the SPI bus. Writing to the QSPIC_DUMMYDATA register generates a number of clock pulses to the SPI bus. During this activity in the SPI bus, the QSPI_IO data pads are in a *hi-z* state.

When access to the SPI bus via QSPIC_WRITEDATA, QSPIC2_READDATA, and QSPIC_DUMMYDATA is very slow, the delay in access to the AHB is very high. In this case, set the

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QSPIC_HRDY_MD register equal to 1. With this feature, the *hready* signal of the SB slave interface is always equal to 1, when accessing the WriteData, ReadData, and DummyData registers. All masters can access the AHB bus without waiting for transmission completion on SPI Bus. A read of the QSPIC_BUSY register must be done to check the end of the activity at the SPI bus before any more access is triggered. In this case, register QSPIC_RECVDATA contains the received data at the end of read access.

20.3.2.3 Clock Selection

The SPI clock mode is set with bit QSPIC_CLK_MD. The supported modes for the generated SPI clock are:

- 0 = Mode 0. The QSPI_SCK is low when the bus is idle (QSPI_CS is high)
- 1 = Mode 3. The QSPI_SCK is high when the bus is idle (QSPI_CS is high)

The QSPI_CLK frequency has a programmable divider CLK_AMBA_REG[QSPIC_DIV/QSPIC2_DIV] which divides the SYS_CLK by 1,2,4,8.

20.3.2.4 Received Data

The standard method to sample the received data is by using the positive edge of the QSPI_SCK. However, when the output delay of the PSRAM device is high, timing issues at the read path are very likely. For this reason, the QSPIC can be programmed to sample the received data with the negative edge of the QSPI_SCK. This is specified with the QSPIC_RXD_NEG register.

Furthermore, the receive data can be pipelined by setting QSPI_RPIPE_EN=1 and the sample clock can be delayed using QSPI_PCLK_MD. Refer to the timing chapter for detailed QSPI Timing information.

20.3.2.5 Delay Line Configuration

When VDD = 0.9 V (POWER_LVL_REG[V12_LEVEL] = 0x1) and QSPI_CLK = 32 MHz, the QSPIC_CTRLMODE_REG[QSPIC_PCLK_MD] bit field should be equal to 2. On the contrary, if VDD = 1.2 V then QSPIC_CTRLMODE_REG[QSPIC_PCLK_MD] bit field should be equal to 7.

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21 eMMC Host Controller

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✗	✗	✓

21.1 Introduction

The eMMC host controller is used to transfer data from/to an external eMMC storage.

Features

- Support for eMMC 4.41
  - Up to SDR-52 mode
  - Maximum clock speed of 48 MHz
  - Support for SDMA and ADMA2 modes
  - No CQE support
- Max supported block-size of 2048 bytes
- 8-bit interface support

21.2 Architecture

The eMMC Host controller block diagram is shown in Figure 49.

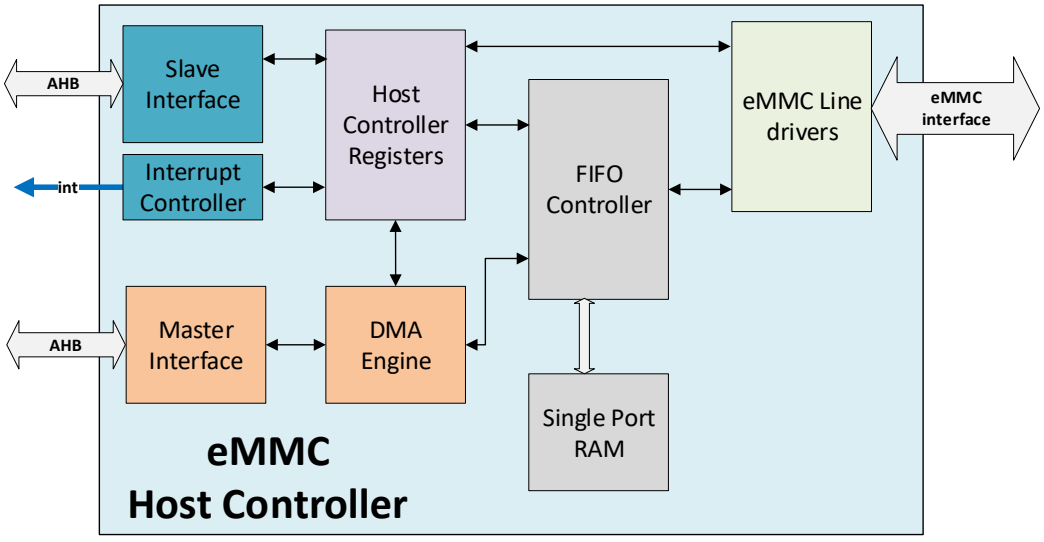

Figure 49: eMMC Host Controller Block Diagram

The controller supports up to 48 MHz clock, which is determined by the system clock and the divider CLK_PDCTRL_REG[EMMC_CLK_DIV]. Valid clock divider values are 1, 2, 4, 8, and 16. For the case that the system is running with RC96M as system clock, the valid clock divider values are 2, 4, 8, and 16 that give 48 MHz, 24 MHz, 12 MHz, and 6 MHz, respectively. If the PLL160MHz is used as system clock, then the valid clock divider values are 4, 8, and 16 that give 40 MHz, 20 MHz, and 10 MHz, respectively.

The eMMC Host controller contains the following subblocks:

- **Slave bus interface module**

  The AHB Slave bus interface module implements the logic to primarily access the controller registers by using the AHB-DMA bus. This module supports only the little-endian scheme for register accesses.

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- **Master bus interface module**

  The Master bus interface module implements the logic to transfer data on the AHB-DMA bus. Through this interface the controller can transfer data from/to internal sysRAM or other slave device in the AHB-DMA bus.

- **DMA engine module**

  The DMA engine module handles the data transfers between the eMMC host controller and the system memory or any other external memory available to the system. It implements the SDMA and ADMA2 modes of operation of the controller.

- **Host Controller Registers module**

  The host controller registers module comprises of the standard eMMC host controller registers as specified by the eMMC protocol.

- **Interrupt Controller module**

  The Interrupt controller module is responsible for the IRQ generation of the host controller.

- **FIFO controller module**

  The FIFO controller module interfaces the host controller with the internal packet buffer memory.

- **eMMC Line drivers module**

  The eMMC line drivers module manages the eMMC interface pins based on the eMMC protocol.

21.2.1 eMMC Bus Protocol

An eMMC bus data transfer contains a command, response, and data block tokens. Each data transfer is considered as a bus operation that always contains a command and a response token. Additionally, certain bus operations also contain a data token. Similar to the SD bus protocol, command and data bit streams are bound by a start bit and a stop bit. Data transfer occurs in the form of blocks that are followed by CRC bits and data is transferred in single or multiple blocks. While a single/multiple read block is terminated by a stop command on the CMD line, a single/multiple write block is terminated by a busy signal on the data (DAT0) line.

The block read and write operations are shown in Figure 50 and Figure 51.

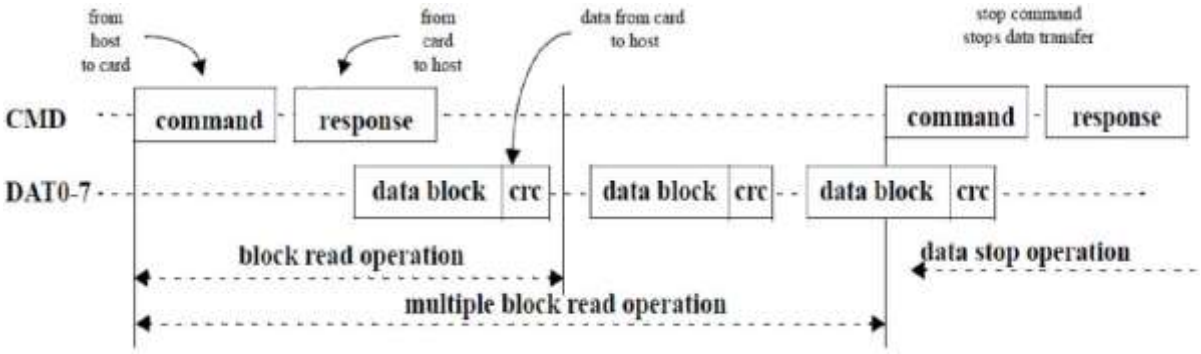

Figure 50: eMMC Block Read Operation

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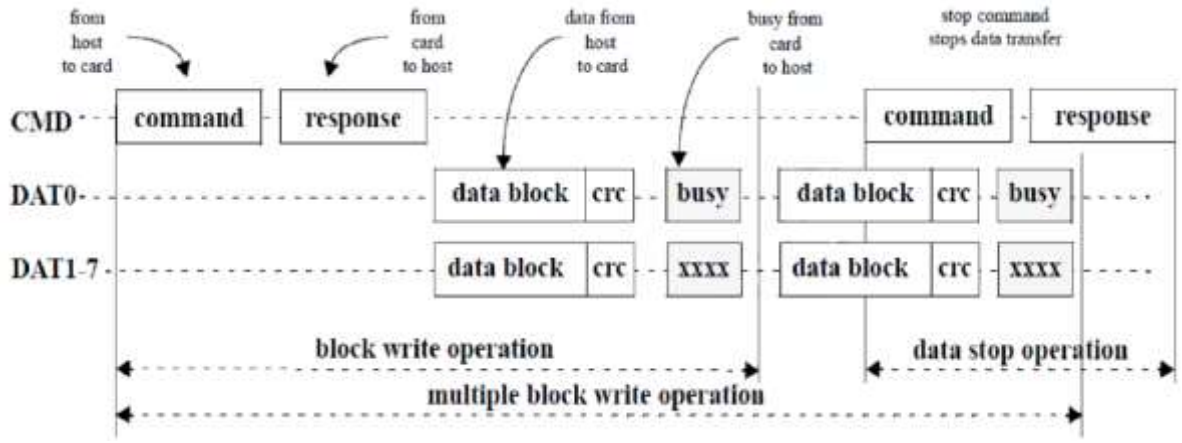

Figure 51: eMMC Block Write Operation

21.3 Programming

There is a sequence of steps that needs to be followed to configure and use the eMMC Host controller.

21.3.1 Write and Read of 512 Bytes (Single Block)

1. Configure all the eMMC GPIOs to pull-up mode by setting the Px_yz_MODE_REG[PUPD]=1
2. Enable PD_CTRL domain (PMU_CTRL_REG[CTRL_SLEEP]=0) and wait for the domain to be up (SYS_STAT_REG[CTRL_IS_UP]=1)
3. Enable the eMMC host controller block (CLK_PDCTRL_REG[EMMC_ENABLE]=1) and select clock divider of the block based on the required speed (CLK_PDCTRL_REG[EMMC_CLK_DIV]).
4. Configure the Tx/Rx clock inversion for proper data sampling (CLK_PDCTRL_REG[EMMC_INV_TX_CLK] = 1 and CLK_PDCTRL_REG[EMMC_INV_RX_CLK] = 1).
5. Configure the eMMC host controller:
   a. Reset the controller by toggling the EMMC_EMMC_CTRL_R_REG[EMMC_RST_N]
   b. Select eMMC card (EMMC_EMMC_CTRL_R_REG[CARD_IS_EMMC]=1)
   c. Enable the card power and select the proper voltage level (EMMC_PWR_CTRL_R_REG[SD_BUS_PWR_VDD1]=0x1 and EMMC_PWR_CTRL_R_REG[SD_BUS_VOL_VDD1])
   d. Configure the clock for the eMMC Host controller:
      i. EMMC_CLK_CTRL_R_REG[CLK_GEN_SELECT] = 0
      ii. EMMC_CLK_CTRL_R_REG[FREQ_SEL] = 0
      iii. EMMC_CLK_CTRL_R_REG[PLL_ENABLE] = 1
      iv. EMMC_CLK_CTRL_R_REG[SD_CLK_EN] = 1
      v. EMMC_CLK_CTRL_R_REG[INTERNAL_CLK_EN] = 1
6. Send CMD0 to the eMMC card (go idle state)
   a. EMMC_NORMAL_INT_STAT_EN_R_REG[CMD_COMPLETE_STAT_EN] = 1
   b. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
   c. EMMC_CMD_R_REG = 0x0C0
   d. EMMC_ARGUMENT_R_REG[ARGUMENT] = 0x0
   e. EMMC_ERROR_INT_STAT_EN_R_REG[CMD_CRC_ERR_STAT_EN] = 0
   f. EMMC_FORCE_ERROR_INT_STAT_R_REG[FORCE_CMD_CRC_ERR] = 0
   g. Do NOT wait until EMMC_NORMAL_INT_STAT_R_REG[CMD_COMPLETE] = 1, return immediately

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7. Send CMD1 to the eMMC card (get operating conditions register contents):
   a. EMMC_NORMAL_INT_STAT_EN_R_REG[CMD_COMPLETE_STAT_EN] = 1
   b. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
   c. EMMC_CMD_R_REG = 0x102
   d. EMMC_ARGUMENT_R_REG[ARGUMENT] = 0x0
   e. EMMC_ERROR_INT_STAT_EN_R_REG[CMD_CRC_ERR_STAT_EN] = 0
   f. EMMC_FORCE_ERROR_INT_STAT_R_REG[FORCE_CMD_CRC_ERR] = 0
   g. Wait until EMMC_NORMAL_INT_STAT_R_REG[CMD_COMPLETE] = 1
8. Send CMD2 to the eMMC card (CID number):
   a. EMMC_NORMAL_INT_STAT_EN_R_REG[CMD_COMPLETE_STAT_EN] = 1
   b. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
   c. EMMC_CMD_R_REG = 0x209
   d. EMMC_ARGUMENT_R_REG[ARGUMENT] = 0x0
   e. EMMC_ERROR_INT_STAT_EN_R_REG[CMD_CRC_ERR_STAT_EN] = 0
   f. EMMC_FORCE_AUTO_CMD_STAT_R_REG[FORCE_AUTO_CMD_CRC_ERR] = 0
   g. Wait until EMMC_NORMAL_INT_STAT_R_REG[CMD_COMPLETE] = 1
9. Send CMD3 (assign relative address to the eMMC card):
   a. EMMC_NORMAL_INT_STAT_EN_R_REG[CMD_COMPLETE_STAT_EN] = 1
   b. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
   c. EMMC_CMD_R_REG = 0x31A
   d. EMMC_ARGUMENT_R_REG[ARGUMENT] = 0x00010000
   e. EMMC_ERROR_INT_STAT_EN_R_REG[CMD_CRC_ERR_STAT_EN] = 0
   f. EMMC_FORCE_AUTO_CMD_STAT_R_REG[FORCE_AUTO_CMD_CRC_ERR] = 0
   g. Wait until EMMC_NORMAL_INT_STAT_R_REG[CMD_COMPLETE] = 1
10. Send CMD13 to assert/verify that the card state is in STANDBY
   a. EMMC_NORMAL_INT_STAT_EN_R_REG[CMD_COMPLETE_STAT_EN] = 1
   b. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
   c. EMMC_CMD_R_REG = 0xD1A
   d. EMMC_ARGUMENT_R_REG[ARGUMENT] = 0x00010000
   e. EMMC_ERROR_INT_STAT_EN_R_REG[CMD_CRC_ERR_STAT_EN] = 0
   f. EMMC_FORCE_AUTO_CMD_STAT_R_REG[FORCE_AUTO_CMD_CRC_ERR] = 0
   g. Wait until EMMC_NORMAL_INT_STAT_R_REG[CMD_COMPLETE] = 1
11. SEND_CSD (CMD9)
   a. EMMC_NORMAL_INT_STAT_EN_R_REG[CMD_COMPLETE_STAT_EN] = 1
   b. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
   c. EMMC_CMD_R_REG = 0x909
   d. EMMC_ARGUMENT_R_REG[ARGUMENT] = 0x00010000
   e. EMMC_ERROR_INT_STAT_EN_R_REG[CMD_CRC_ERR_STAT_EN] = 0
   f. EMMC_FORCE_AUTO_CMD_STAT_R_REG[FORCE_AUTO_CMD_CRC_ERR] = 0
   g. Wait until EMMC_NORMAL_INT_STAT_R_REG[CMD_COMPLETE] = 1
12. Send CMD7 (eMMC card state from Standby to Transfer state):
   a. EMMC_NORMAL_INT_STAT_EN_R_REG[CMD_COMPLETE_STAT_EN] = 1
   b. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
   c. EMMC_CMD_R_REG = 0x712
   d. EMMC_ARGUMENT_R_REG[ARGUMENT] = 0x00010000
   e. EMMC_ERROR_INT_STAT_EN_R_REG[CMD_CRC_ERR_STAT_EN] = 0
   f. EMMC_FORCE_AUTO_CMD_STAT_R_REG[FORCE_AUTO_CMD_CRC_ERR] = 0

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g. Wait until EMMC_NORMAL_INT_STAT_R_REG[CMD_COMPLETE] = 1

13. Send CMD6 to set the bus width to 1-bit:
    a. EMMC_NORMAL_INT_STAT_EN_R_REG[CMD_COMPLETE_STAT_EN] = 1
    b. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
    c. EMMC_CMD_R_REG = 0x61A
    d. EMMC_ARGUMENT_R_REG[ARGUMENT] = 0x03B70000
    e. EMMC_ERROR_INT_STAT_EN_R_REG[CMD_CRC_ERR_STAT_EN] = 0
    f. EMMC_FORCE_AUTO_CMD_STAT_R_REG[FORCE_AUTO_CMD_CRC_ERR] = 0
    g. Wait until EMMC_NORMAL_INT_STAT_R_REG[CMD_COMPLETE] = 1
14. Send CMD6 to set speed mode (HS-SDR)
    a. EMMC_NORMAL_INT_STAT_EN_R_REG[CMD_COMPLETE_STAT_EN] = 1
    b. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
    c. EMMC_CMD_R_REG = 0x61A
    d. EMMC_ARGUMENT_R_REG[ARGUMENT] = 0x03B90100
    e. EMMC_ERROR_INT_STAT_EN_R_REG[CMD_CRC_ERR_STAT_EN] = 0
    f. EMMC_FORCE_AUTO_CMD_STAT_R_REG[FORCE_AUTO_CMD_CRC_ERR] = 0
    g. Wait until EMMC_NORMAL_INT_STAT_R_REG[CMD_COMPLETE] = 1
15. Send CMD13 (read status register from eMMC card to verify card is in TRANSFER state):
    a. EMMC_NORMAL_INT_STAT_EN_R_REG[CMD_COMPLETE_STAT_EN] = 1
    b. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
    c. EMMC_CMD_R_REG = 0xD1A
    d. EMMC_ARGUMENT_R_REG[ARGUMENT] = 0x00010000
    e. Wait until EMMC_NORMAL_INT_STAT_R_REG[CMD_COMPLETE] = 1
16. Send SEND_EXT_CSD (CMD8): read EXT_CSD 512B, high speed, blocking
    a. EMMC_HOST_CTRL1_R_REG[HIGH_SPEED_EN] = 1
    b. EMMC_HOST_CTRL1_R_REG[EXT_DAT_XFER] = 0
    c. EMMC_XFER_MODE_R_REG[DATA_XFER_DIR] = 1
    d. EMMC_BLOCKSIZE_R_REG[XFER_BLOCK_SIZE] = 0x200
    e. EMMC_NORMAL_INT_STAT_EN_R_REG[BUF_WR__READY_STAT_EN] = 1
    f. EMMC_NORMAL_INT_STAT_EN_R_REG[BUF_RD_READY_STAT_EN] = 1
    g. EMMC_NORMAL_INT_STAT_EN_R_REG[XFER_COMPLETE_STAT_EN] = 1
    h. EMMC_NORMAL_INT_SIGNAL_EN_R_REG[XFER_COMPLETE_SIGNAL_EN] = 0
    i. EMMC_ERROR_INT_STAT_EN_R_REG[CMD_CRC_ERR_STAT_EN] = 0
    j. EMMC_FORCE_AUTO_CMD_STAT_R_REG[FORCE_AUTO_CMD_CRC_ERR] = 0
    k. EMMC_ARGUMENT_R_REG[ARGUMENT] = 0x00010000
    l. EMMC_XFER_MODE_R_REG[RESP_ERR_CHK_ENABLE] = 0
    m. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
    n. EMMC_XFER_MODE_R_REG[RESP_TYPE] = 0
    o. EMMC_NORMAL_INT_STAT_EN_R_REG[CMD_COMPLETE_STAT_EN] = 1
    p. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
    q. EMMC_CMD_R_REG = 0x83A
    r. Wait until EMMC_NORMAL_INT_STAT_R_REG[BUF_RD_READY] = 1
    s. Wait until EMMC_NORMAL_INT_STAT_R_REG[CMD_COMPLETE] = 1
    t. Wait until EMMC_PSTATE_REG[BUF_RD_ENABLE] = 1
    u. Read data by reading EMMC_BUF_DATA_R_REG[BUF_DATA] register
    v. Wait until EMMC_NORMAL_INT_STAT_R_REG[XFER_COMPLETE] = 1
17. Send CMD24 to write single block (write 512 bytes at default speed):

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a. EMMC_HOST_CTRL1_R_REG[HIGH_SPEED_EN] = 1
b. EMMC_HOST_CTRL1_R_REG[EXT_DAT_XFER] = 0
c. EMMC_XFER_MODE_R_REG[DATA_XFER_DIR] = 0
d. EMMC_BLOCKSIZE_R_REG[XFER_BLOCK_SIZE] = 0x200 (dependent on the eMMC memory used)
e. EMMC_NORMAL_INT_STAT_EN_R_REG[BUF_WR__READY_STAT_EN] = 1
f. EMMC_NORMAL_INT_STAT_EN_R_REG[BUF_RD_READY_STAT_EN] = 1
g. EMMC_NORMAL_INT_STAT_EN_R_REG[XFER_COMPLETE_STAT_EN] = 1
h. EMMC_NORMAL_INT_SIGNAL_EN_R_REG[XFER_COMPLETE_SIGNAL_EN] = 1
i. EMMC_ERROR_INT_STAT_EN_R_REG[CMD_CRC_ERR_STAT_EN] = 0
j. EMMC_FORCE_AUTO_CMD_STAT_R_REG[FORCE_AUTO_CMD_CRC_ERR] = 0
k. EMMC_ARGUMENT_R_REG[ARGUMENT] = 0x0
l. EMMC_XFER_MODE_R_REG[RESP_ERR_CHK_ENABLE] = 0
m. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
n. EMMC_XFER_MODE_R_REG[RESP_TYPE] = 0
o. EMMC_NORMAL_INT_STAT_EN_R_REG[CMD_COMPLETE_STAT_EN] = 1
p. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
q. EMMC_CMD_R_REG = 0x183A
r. Wait until EMMC_NORMAL_INT_STAT_R_REG[BUF_WR_READY] = 1
s. Wait until EMMC_NORMAL_INT_STAT_R_REG[CMD_COMPLETE] = 1
t. Wait until EMMC_PSTATE_REG[BUF_WR_ENABLE] = 1
u. Send data by writing to EMMC_BUF_DATA_R_REG[BUF_DATA] register
v. Wait until EMMC_NORMAL_INT_STAT_R_REG[XFER_COMPLETE] = 1

18. Send CMD 17 (Read a single block of 512 Bytes):
    a. EMMC_HOST_CTRL1_R_REG[HIGH_SPEED_EN] = 1
    b. EMMC_HOST_CTRL1_R_REG[EXT_DAT_XFER] = 0
    c. EMMC_XFER_MODE_R_REG[DATA_XFER_DIR] = 1
    d. EMMC_BLOCKSIZE_R_REG[XFER_BLOCK_SIZE] = 0x200 (dependent on the eMMC memory used)
    e. EMMC_XFER_MODE_R_REG[BLOCK_COUNT_ENABLE] = 0
    f. EMMC_NORMAL_INT_STAT_EN_R_REG[BUF_RD_READY_STAT_EN] = 1
    g. EMMC_NORMAL_INT_SIGNAL_EN_R_REG[BUF_RD_READY_SIGNAL_EN] = 1
    h. EMMC_NORMAL_INT_STAT_EN_R_REG[XFER_COMPLETE_STAT_EN] = 1
    i. EMMC_NORMAL_INT_SIGNAL_EN_R_REG[XFER_COMPLETE_SIGNAL_EN] = 1
    j. EMMC_ERROR_INT_STAT_EN_R_REG[CMD_CRC_ERR_STAT_EN] = 0
    k. EMMC_FORCE_AUTO_CMD_STAT_R_REG[FORCE_AUTO_CMD_CRC_ERR] = 0
    l. EMMC_ARGUMENT_R_REG[ARGUMENT] = 0x0
    m. EMMC_XFER_MODE_R_REG[RESP_ERR_CHK_ENABLE] = 0
    n. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
    o. EMMC_XFER_MODE_R_REG[RESP_TYPE] = 1
    p. EMMC_NORMAL_INT_STAT_EN_R_REG[CMD_COMPLETE_STAT_EN] = 1
    q. EMMC_XFER_MODE_R_REG[RESP_INT_DISABLE] = 0
    r. EMMC_CMD_R_REG = 0x113A
    s. Wait until EMMC_NORMAL_INT_STAT_R_REG[CMD_COMPLETE] = 1
    t. Wait until EMMC_PSTATE_REG[BUF_RD_ENABLE] = 1
    u. Wait until EMMC_NORMAL_INT_STAT_R_REG[BUF_RD_READY] = 1
    v. Read data from EMMC_BUF_DATA_R_REG[BUF_DATA] register.

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22 Display Controller

Device:	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

22.1 Introduction

The DA1470x is equipped with a Display Controller, capable to support Parallel DPI/DBI Type B/JDI, Serial (SPI3/4 and Dual/Quad SPI) interfaces. The controller can support E-ink and OLED displays.

A global register file controls the parameters of the controller. After applying the timing parameters, data are fetched by a dedicated DMA engine. Depending on the target screen, the output can be formatted to different types as described in the following sections.

Features

- Up to two layers support with blending capabilities
  - Alpha blending
- Global Gamma Correction (LUT-based) support
- Dithering and Gamma Correction support
- AHB 32-bit Master interface with internal DMA engine
- Input color formats:
  - RGBA-8888, ARGB-8888, ABGR-8888, BGRA-8888, RGB-888, RGBA-5551, RGB-565, and RGB-332
- Output interfaces:
  - DPI-2 interface
  - DBI-B interface
  - JDI parallel interfaces
  - 3/4-wire SPI serial interface
  - Dual and Quad SPI serial interface
- Output color formats:
  - 3/4w SPI: RGB-111, RGB-332, RGB-444, RGB-565, RGB-666, RGB-888
  - Dual/Quad SPI: RGB-444, RGB-565, RGB-666, RGB-888
  - DPI-2 6-bit: RGB-222
  - DBI-B 8-bit: RGB-332, RGB-444, RGB-565, RGB-666, RGB-888

22.2 Architecture

Figure 52 shows the integration of the display controller. In the following sections, the parallel and serial display interfaces are addressed.

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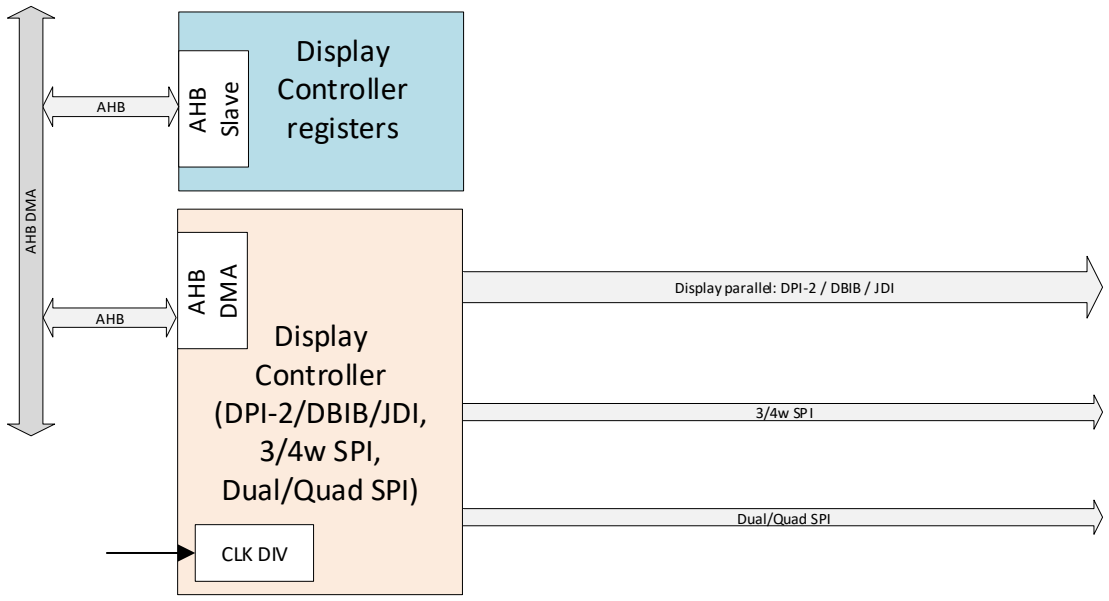

Figure 52: Display Controller Block Diagram

22.2.1 Parallel Display Interfaces

22.2.1.1 HSYNC/VSYNC Parallel Interface (DPI-2)

The signal HSYNC is asserted on every scanline and the signal VSYNC is asserted on every frame. The polarity of the output Clock signal can be defined as positive or negative and the length of each pulse is programmable. Typical waveforms of operation are depicted in Figure 53 and Figure 54.

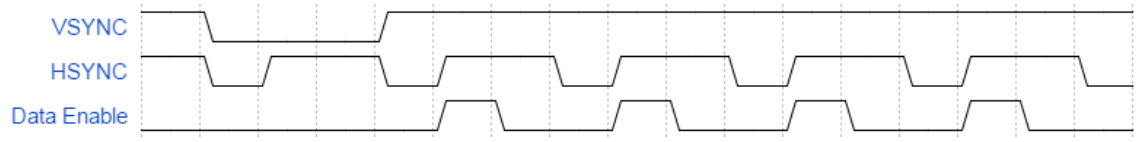

Figure 53: HSYNC/VSYNC Typical Waveform

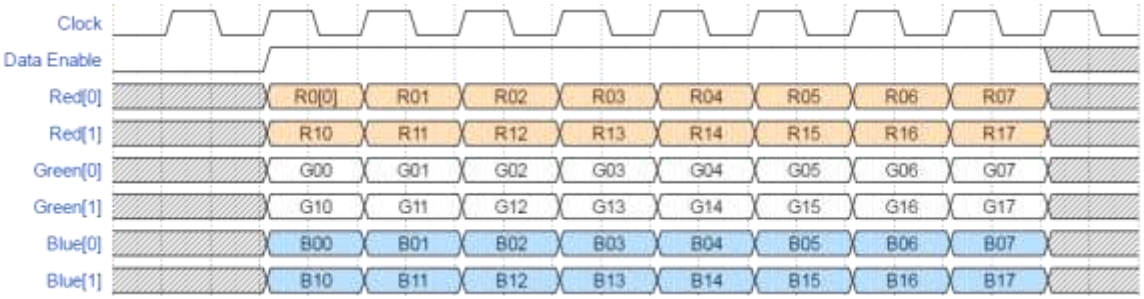

Figure 54: HSYNC/VSYNC Color Bits Waveform

The available signals of the interface are shown in Table 120.

Table 120: HSYNC/VSYNC Parallel I/F Pinout

Pin Name	Type	Description	Source
DPI_CLK	Output	Display Clock	Display Controller
DPI_DE	Output	Indicate valid data on the display data bus	Display Controller

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Pin Name	Type	Description	Source
DPI_HSYNC	Output	Reset the display column pointer to the edge of the display	Display Controller
DPI_VSYNC	Output	Reset the display row pointer to the top of the display	Display Controller
DPI_SD	Output	Control pin to shutdown display	Display Controller
DPI_CM	Output	Control pin for switching between normal color and reduced color mode	Display Controller
DPI_RED0 (DATA[0])	Output	Red image data	Display Controller
DPI_RED1 (DATA[1])	Output	Red image data	Display Controller
DPI_GREEN0 (DATA[2])	Output	Green image data	Display Controller
DPI_GREEN1 (DATA[3])	Output	Green image data	Display Controller
DPI_BLUE0 (DATA[4])	Output	Blue image data	Display Controller
DPI_BLUE1 (DATA[5])	Output	Blue image data	Display Controller
Backlight	Output	LED driver signals	GPIO

22.2.1.2 JDI Parallel Interface

The available signals of the interface are shown in Table 121.

Table 121: JDI Parallel I/F Pinout

Pin Name	Type	Description	Source
HST	Output	Start signal for the horizontal driver	Display Controller
HCK	Output	Shift clock for the horizontal driver	Display Controller
ENB	Output	Write enable signal for the pixel memory	Display Controller
VST	Output	Start signal for the vertical driver	Display Controller
XRST	Output	Reset signal for the horizontal and vertical driver	Display Controller
VCK	Output	Shift clock for the vertical driver	Display Controller
RED0	Output	Red image data	Display Controller
RED1	Output	Red image data	Display Controller
GREEN0	Output	Green image data	Display Controller
GREEN1	Output	Green image data	Display Controller
BLUE0	Output	Blue image data	Display Controller
BLUE1	Output	Blue image data	Display Controller
VCOM (Note 1)	Output	Common electrode driving signal (60 Hz)	GPIO
FRP (Note 1)	Output	Liquid crystal driving signal (60 Hz)	GPIO
XFRP	Output	Liquid crystal driving signal (60 Hz inverted)	GPIO
Backlight	Output	LED driver signals	GPIO

Note 1 The signal can be available during sleep mode.

22.2.1.3 DBI Type-B interface

The available signals of the interface are shown in Table 122.

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Table 122: DBI Type-B I/F Pinout

Pin Name	Type	Description	Source
DBIB_CSX	Output	Display module is selected when low	Display Controller
DBIB_RESX	Output	Display module reset signal (active low)	Display Controller
DBIB_D/CX	Output	Data/Command indication signal. Data transfers when high, command transfers when low	Display Controller
DBIB_WRX	Output	Write indication signal. The host writes data at a rising edge	Display Controller
DBIB_RDX	Output	Read indication signal. The host reads data at rising edge	Display Controller
DBIB_STALL	Input	Display module can receive data when high	Display Controller
DBIB_DB0	Output	Information signal bit 0	Display Controller
DBIB_DB1	Output	Information signal bit 1	Display Controller
DBIB_DB2	Output	Information signal bit 2	Display Controller
DBIB_DB3	Output	Information signal bit 3	Display Controller
DBIB_DB4	Output	Information signal bit 4	Display Controller
DBIB_DB5	Output	Information signal bit 5	Display Controller
DBIB_DB6	Output	Information signal bit 6	Display Controller
DBIB_DB7	Output	Information signal bit 7	Display Controller
DBIB_TE	Input	Tearing Effect	Display Controller
Backlight	Output	LED driver signal	GPIO

22.2.2 Serial Display Interfaces

22.2.2.1 SPI3/4 Serial Interface

The Display controller supports the SPI serial interface with three or four distinct signals. The three-line serial interface uses the CS (chip enable) signal, the SCLK (serial clock) signal, and the SD (MOSI, serial data output) signal. The four-line serial interface use one additional signal, the DC (data/command select). The SD signal is regarded as a command when DC is low and as data when DC is high. The serial clock (SCLK) can be stopped when no communication is necessary.

During the write mode, the Display controller sends the write commands and data to the display. In the four-line serial mode, the data packet (SD) contains only the transmission byte (8 bits) and the control bit is transferred by the DC signal. In the 3-lines serial mode, the data packet (SD) contains a control bit and a transmission byte (9 bits). The MSB is transmitted first in both cases.

The CS signal is configurable. It can be set high or low to indicate the start of the data transmission. Data can be sampled either by the falling or the rising edge of the SCLK depending on the configuration. The clock polarity is also configurable (the clock starts at a high or low edge).

If the CS signal remains active (high or low, depending on the configuration) after the last bit of the transmitted data packet, the Display controller will transmit the MSB of the next byte at the next rising/falling edge of SCLK.

Finally, the SD signal is multiplexed with the SI signal (serial input – MISO) in the same pad, in cases that the DA1470x needs to read data from the display.

22.2.2.2 Dual/Quad SPI Interface

The DualSPI serial interface uses CS (chip enable), SCLK (serial clock), and SD, SD1 (serial data outputs). The command word always is transmitted through the SD line and the data are routed through the SD and SD1 lines. The command word consists of 9-bits, 1-bit data/command indicator, and 8-bits command word. The data word consists of 1-bit data/command indicator and n-bits, according to the chosen format.

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The QuadSPI serial interface uses CS (chip enable), SCLK (serial clock) and SD, SD1, SD2, SD3 (serial data outputs). The header and the command type are always transmitted through the SD line and the data are routed through the SD, SD1, SD2, and SD3 lines. The header consists of 8-bits. The command word consists of 24-bits and the data word consists of n-bits, according to the chosen format.

The available signals of the SPI3/4, DualSPI, and QuadSPI interfaces are shown in Table 123.

Table 123: SPI3/4 – DualSPI – QuadSPI Serial I/F Pinout

Pin Name	Type	Description	Source
LCD_SPI_SCLK	Output	Serial clock signal	Display Controller
LCD_SPI_SD/SI	Output/Input	Serial data (write/read)	Display Controller
LCD_SPI_SD1/DC	Output	Serial data Data/Command select (when SPI4)	Display Controller
LCD_SPI_SD2	Output	Serial data	Display Controller
LCD_SPI_SD3	Output	Serial data or Data/Command select (when SPI4)	Display Controller
LCD_CS	Output	Chip select	Display Controller
EXTCOMIN (Note 1)	Output	COM Inversion Signal Input (1 Hz)	GPIO
RST	Output	Reset display	GPIO
DISP	Output	Display ON/OFF Control	GPIO
LCD_TE	Input	Display Tearing effect signal	GPIO
Backlight	Output	LED driver signals	GPIO

Note 1 The signal can be available during sleep mode.

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22.2.3 Color Input Formats

The following input color formats are supported by the controller:

Table 124: 8-bit RGB332

R2	R1	R0	G2	G1	G0	B1	B0

Table 125: 16-bit RGB565

R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Table 126: 16-bit RGBA5551

R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	A0

Table 127: 24-bit RGB888

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

Table 128: 32-bit RGBA8888

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0

Table 129: 32-bit ARGB8888

A7	A6	A5	A4	A3	A2	A1	A0	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

Table 130: 32-bit ABGR8888

A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0

Table 131: 32-bit BGRA8888

B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0	A7	A6	A5	A4	A3	A2	A1	A0

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22.2.4 Color Output Formats

22.2.4.1 DPI-2 Output Format

The supported DPI-2 output data format is depicted below.

Table 132: DPI-2 6-bit RGB-222

DBIB_DB				
DPI_DATA[1:0]	R_0[1:0]	R_1[1:0]	...	R_n[1:0]
DPI_DATA[3:2]	G_0[1:0]	G_1[1:0]	...	G_n[1:0]
DPI_DATA[5:4]	B_0[1:0]	B_1[1:0]	...	B_n[1:0]

22.2.4.2 DBI Type B Output Formats

The supported DBI Type B output data formats are depicted below.

Table 133: DBI-B 8-bit RGB-332

DBIB_DB					
DBIB_DB[7:5]	R_0[2:0]	R_1[2:0]	R_2[2:0]	...	R_n[2:0]
DBIB_DB[4:2]	G_0[2:0]	G_1[2:0]	G_2[2:0]	...	G_n[2:0]
DBIB_DB[1:0]	B_0[1:0]	B_1[1:0]	B_2[1:0]	...	B_n[1:0]

Table 134: DBI-B 8-bit RGB-444

DBIB_DB					
DBIB_DB[7:4]	R_0[3:0]	B_0[3:0]	G_1[3:0]	...	G_n[3:0]
DBIB_DB[3:0]	G_0[3:0]	R_1[3:0]	B_1[3:0]	...	B_n[3:0]

Table 135: DBI-B 8-bit RGB-565

DBIB_DB							
DBIB_DB[7:5]	R_0[4:2]	G_0[2:0]	R_1[4:2]	G_1[2:0]	...	R_n[4:2]	G_n[2:0]
DBIB_DB[4:2]	R_0[1:0]	B_0[4:3]	R_1[1:0]	B_1[4:3]	...	R_n[1:0]	B_n[4:3]
DBIB_DB[1:0]	G_0[5:3]	B_0[2:0]	G_1[5:3]	B_1[2:0]	...	G_n[5:3]	B_n[2:0]

Table 136: DBI-B 8-bit RGB-666

DBIB_DB							
DBIB_DB[7:2]	R_0[5:0]	G_0[5:0]	B_0[5:0]	...	R_n[5:0]	G_n[3:0]	B_n[5:0]
DBIB_DB[1:0]				...			

Table 137: DBI-B 8-bit RGB-888

DBIB_DB							
DBIB_DB[7:0]	R_0[7:0]	G_0[7:0]	B_0[7:0]	...	R_n[7:0]	G_n[7:0]	B_n[7:0]

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22.2.4.3 SPI3/4 Output Formats

The supported SPI output data formats are depicted below.

Table 138: SPI3/4 – RGB-111 (Option 0)

Byte	Pixel	DCS	D7	D6	D5	D4	D3	D2	D1	D0
Byte1	n pixel	(Note 1)			R0	G0	B0	R0	G0	B0

Table 139: SPI3/4 – RGB-111 (Option 1)

Byte	Pixel	DCS	D7	D6	D5	D4	D3	D2	D1	D0
Byte1	n pixel	(Note 1)		R0	G0	B0		R0	G0	B0

Table 140: SPI3/4 – RGB-111 (Option 2)

Byte	Pixel	DCS	D7	D6	D5	D4	D3	D2	D1	D0
Byte1	n pixel	(Note 1)	R0	G0	B0		R0	G0	B0	

Table 141: SPI3/4 – RGB-111 (Option 3 – B&W)

Byte	Pixel	DCS	D7	D6	D5	D4	D3	D2	D1	D0
Byte1	n pixel	(Note 1)	BW	BW	BW	BW	BW	BW	BW	BW

Table 142: SPI3/4 – RGB-111 (Option 4)

Byte	Pixel	DCS	D7	D6	D5	D4	D3	D2	D1	D0
Byte1	n pixel	(Note 1)	R0	G0	B0	R0	G0	B0	R0	G0

Table 143: SPI3/4 – RGB-332

Byte	Pixel	DCS	D7	D6	D5	D4	D3	D2	D1	D0
Byte1	n pixel	(Note 1)	R2	R1	R0	G2	G1	G0	B1	B0

Table 144: SPI3/4 – RGB-444

Byte	Pixel	DCS	D7	D6	D5	D4	D3	D2	D1	D0
byte0	n pixel	(Note 1)	R3	R2	R1	R0	G3	G2	G1	G0
byte1	n/n+1 pixel	(Note 1)	B3	B2	B1	B0	R3	R2	R1	R0
byte2	n+1 pixel	(Note 1)	G3	G2	G1	G0	B3	B2	B1	B0

Table 145: SPI3/4 – RGB-565

Byte	Pixel	DCS	D7	D6	D5	D4	D3	D2	D1	D0
byte0	n pixel	(Note 1)	R4	R3	R2	R1	R0	G5	G4	G3
byte1	n pixel	(Note 1)	G2	G1	G0	B4	B3	B2	B1	B0

Table 146: SPI3/4 – RGB-666

Byte	Pixel	DCS	D7	D6	D5	D4	D3	D2	D1	D0
byte0	n pixel	(Note 1)	R5	R4	R3	R2	R1	R0		
byte1	n pixel	(Note 1)	G5	G4	G3	G2	G1	G0		
byte2	n pixel	(Note 1)	B5	B4	B3	B2	B1	B0		

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Table 147: SPI3/4 – RGB-888

Byte	Pixel	DCS	D7	D6	D5	D4	D3	D2	D1	D0
byte0	n pixel	(Note 1)	R7	R6	R5	R4	R3	R2	R1	R0
byte1	n pixel	(Note 1)	G7	G6	G5	G4	G3	G2	G1	G0
byte2	n pixel	(Note 1)	B7	B6	B5	B4	B3	B2	B1	B0

Note 1 Available only in SPI3 mode.

22.2.4.4 Dual SPI Output Formats

The supported Dual SPI output data formats are depicted below.

Table 148: Dual SPI – 8 bit RGB-444 (Option 0)

SPI signal		n pixel					n/n+1 pixel					n+1 pixel			
SPI_SD		R3	R2	R1	R0		B3	B2	B1	B0		G3	G2	G1	G0
SPI_SD1/DC		G3	G2	G1	G0		R3	R2	R1	R0		B3	B2	B1	B0

Table 149: Dual SPI – 8 bit RGB-444 (Option 1)

SPI signal		n pixel							n+1 pixel						
SPI_SD		R3	R2	R1	R0	G3	G2		R3	R2	R1	R0	G3	G2	
SPI_SD1/DC		G1	G0	B3	B2	B1	B0		G1	G0	B3	B2	B1	B0	

Table 150: Dual SPI – 8 bit RGB-565

SPI signal		n pixel								n+1 pixel							
SPI_SD		R4	R3	R2	R1	R0	G5	G4	G3	R4	R3	R2	R1	R0	G5	G4	G3
SPI_SD1/DC		G2	G1	G0	B4	B3	B2	B1	B0	G2	G1	G0	B4	B3	B2	B1	B0

Table 151: Dual SPI – 8 bit RGB-666 (Option 0)

SPI signal		n pixel							n/n+1 pixel						
SPI_SD		R5	R4	R3	R2	R1	R0		B5	B4	B3	B2	B1	B0	
SPI_SD1/DC		G5	G4	G3	G2	G1	G0		R5	R4	R3	R2	R1	R0	

Table 152: Dual SPI – 8 bit RGB-666 (Option 1)

SPI signal		n pixel									n+1 pixel								
SPI_SD		R5	R4	R3	R2	R1	R0	G5	G4	G3	R5	R4	R3	R2	R1	R0	G5	G4	G3
SPI_SD1/DC		G2	G1	G0	B5	B4	B3	B2	B1	B0	G2	G1	G0	B5	B4	B3	B2	B1	B0

Table 153: Dual SPI – 8 bit RGB-888 (Option 0)

SPI signal		n pixel								n/n+1 pixel							
SPI_SD		R7	R6	R5	R4	R3	R2	R1	R0	B7	B6	B5	B4	B3	B2	B1	B0
SPI_SD1/DC		G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0

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Table 154: Dual SPI – 8 bit RGB-888 (Option 1)

SPI signal		n pixel												
SPI_SD		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	
SPI_SD1/DC		G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	

22.2.4.5 Quad SPI Output Formats

The supported Quad SPI output data formats are depicted below.

Table 155: Quad SPI – RGB-444

SPI signal	n pixel			n+1 pixel		
SPI_SD	R0	G0	B0	R0	G0	B0
SPI_SD1/DC	R1	G1	B1	R1	G1	B1
SPI_SD2	R2	G2	B2	R2	G2	B2
SPI_SD3	R3	G3	B3	R3	G3	B3

Table 156: Quad SPI – RGB-565

SPI signal	n pixel				n+1 pixel			
SPI_SD	R1	G3	B4	B0	R1	G3	B4	B0
SPI_SD1/DC	R2	G4	G0	B1	R2	G4	G0	B1
SPI_SD2	R3	G5	G1	B2	R3	G5	G1	B2
SPI_SD3	R4	R0	G2	B3	R4	R0	G2	B3

Table 157: Quad SPI – RGB-666

SPI signal	n pixel						n+1 pixel					
SPI_SD	R2		G2		B2		R2		G2		B2	
SPI_SD1/DC	R3		G3		B3		R3		G3		B3	
SPI_SD2	R4	R0	G4	G0	B4	B0	R4	R0	G4	G0	B4	B0
SPI_SD3	R5	R1	G5	G1	B5	B1	R5	R1	G5	G1	B5	B1

Table 158: Quad SPI – RGB-888

SPI signal	n pixel						n+1 pixel					
SPI_SD	R4	R0	G4	G0	B4	B0	R4	R0	G4	G0	B4	B0
SPI_SD1/DC	R5	R1	G5	G1	B5	B1	R5	R1	G5	G1	B5	B1
SPI_SD2	R6	R2	G6	G2	B6	B2	R6	R2	G6	G2	B6	B2
SPI_SD3	R7	R3	G7	G3	B7	B3	R7	R3	G7	G3	B7	B3

22.3 Programming

Refer to the SDK for the full-featured Display Controller Software Library.

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23 GPU

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

23.1 Introduction

The 2D GPU is a powerful hardware rendering engine that operates at the same clock speed as the CPU and the system bus. This block has its own power domain namely the PD_GPU. It has one APB-32 slave interface, connected to the APB32-fast bus, for configuration and status registers, and one AHB-32 Master interface, connected to the AHB DMA bus, for memory accesses. The GPU can use the internal RAM and/or the external PSRAM through the QSPI Flash/PSRAM controllers (QSPIC/QSPIC2) with the use of the data cache (only for the QSPIC2 controller).

The GPU operates in two modes, namely the register based and the display list-based mode. In the register-based mode, the CPU (Cortex M33) is responsible for setting all required registers to initiate a GPU operation. After the GPU is ready, the next render process can start. In the display list-based case, the CPU creates a display list in shared memory. Such a list contains a bundle of render operations which is then executed by the GPU without locking the CPU.

Features

- Support for all graphic primitives (BLIT, Box, Circle, Polygon, Line, Quad, Triangle, Wedge)
- Support several attributes for graphic primitives (Anti-Aliasing, Blend Modes, Color, Edge Blur, Linear Alpha gradient, Pattern, Texture)
- Color formats:
  - Input: ARGB-8888, RGB-565, ARGB-4444, ARGB-1555, ALPHA8, AI44, RGBA-8888, RGBA-4444, RGBA-5551, I8, I4, I2, I1, ALPHA4, ALPHA2, ALPHA1
  - Output: ARGB-8888, RGB-565, ARGB-4444, ALPHA8, RGBA-8888, RGBA-4444

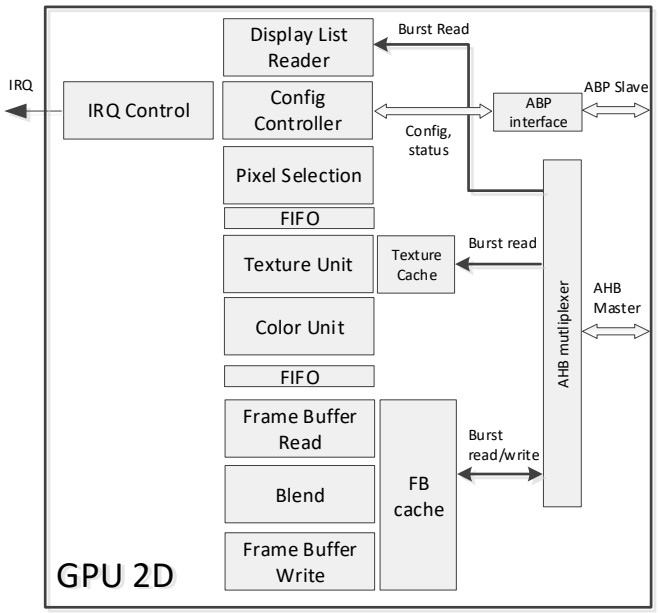

Figure 55: GPU 2D Block Diagram

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23.2 Architecture

23.2.1 Configuration Interface

The configuration interface is used for configuring the 2D GPU and report the current status of the engine. It is also responsible for generating an interrupt request towards the CPU for synchronizing operations. A common interrupt clear mechanism is provided for the CPU acknowledgment.

23.2.2 Display List Interface

The Display list interface reads a memory block containing instructions regarding the operation of the 2D GPU control registers and perform those register updates automatically. This memory block contains a display list and allows for a fully asynchronous operation of the 2D GPU and the CPU providing the best system performance.

23.2.3 Texture Interface

This interface provides the 2D GPU with the needed pixel data for BLIT and texture operations. Pixel formats widths of 8, 16, and 32 bits are supported.

23.2.4 Framebuffer Interface

This interface allows 2D GPU to read and write to/from the frame buffer. Pixel formats widths of 8, 16, and 32 bits are supported.

23.2.5 2D Render Capabilities

The 2D GPU offers a wide range of basic graphic primitives. These are geometries that the GPU can render in one pass. One pass supported primitives are:

- BLIT (Direct and Stretch)
- Box
- Circle (Filled or empty - ring)
- Convex Polygon
- Line
  - Supported Caps: Butt, Round, Square
  - Supported line joins: Bevel, Miter, Round
  - Supporting different start and end widths
- Quad
- Triangle
- Triangle Fan
- Triangle List
- Triangle Stripe
- Triangle Stripe
- Wedge (Filled or empty)

The GPU supports primitive anti-aliasing. In the case of a triangle, the anti-aliasing can be turned on or off for every single edge. This mechanism is useful to render polygons with correct outline anti-aliasing.

The GPU also offers a wide range of color calculation operations (Blending). The color calculation is done in the color and blend units. The following operation can be applied to each color channel (a, r, g, b) individually.

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Table 159: Color Unit Operations

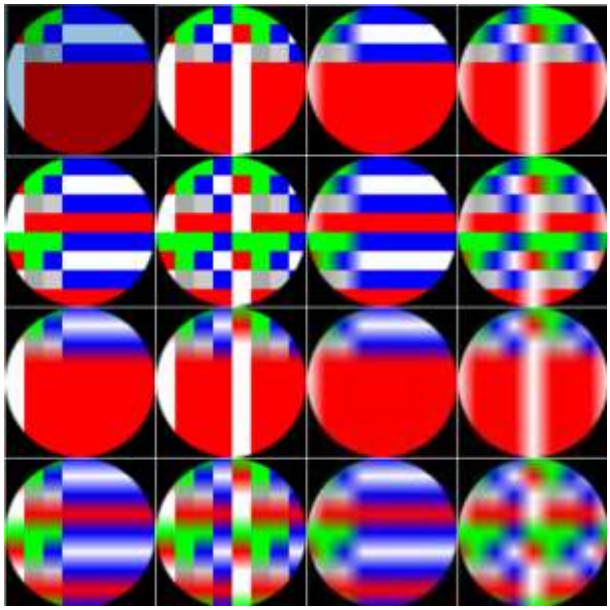
Operation	Operands
Replace	C1
Copy	X
Invert	1-X
Multiply	X*C1
InvMultiply	(1-X)*C1
Blend	X*C1 + (1-X)*C2

Where C1 and C2 (Color1 and Color2) are user-specified constants, and X is the color channel value.

As per blending, the following modes are directly supported as the source and destination factors separately for color and alpha channels: Zero, One, Alpha, One_Minus_Alpha.

Finally, the 2D GPU supports the U/V clamp and U/V repeat. Also, filtering for both clamp and repeat separately is supported. These options are demonstrated in Table 160.

Table 160: Texture Options Example

<table>
<tr><td colspan="3" rowspan="3"></td><td colspan="4">X</td></tr>
<tr><td colspan="2">No filter</td><td colspan="2">Filter</td></tr>
<tr><td>Clamp</td><td>Repeat</td><td>clamp</td><td>Repeat</td></tr>
<tr><td rowspan="4">Y</td><td rowspan="2">No filter</td><td>Clamp</td><td colspan="4" rowspan="4">  </td></tr>
<tr><td>Repeat</td></tr>
<tr><td rowspan="2">Filter</td><td>Clamp</td></tr>
<tr><td>Repeat</td></tr>
</table>

23.3 Programming

Refer to the SDK for the full-featured GPU Software Library.

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24 DMA Controller

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

24.1 Introduction

The DMA controller has eight Direct Memory Access (DMA) channels for fast data transfers to and from SPI, UART, I2C, I3C, SRC/SRC2, PCM, USB, OQSPIC, QSPIC/QSPIC2, GP_ADC, and SD_ADC to and from any on-chip RAM. The DMA controller off-loads the Arm interrupt rate if an interrupt is generated after a programmable number of transfers. A number of peripheral requests is multiplexed on the eight available channels to increase utilization of the DMA. The block diagram of the DMA controller is depicted in Figure 40.

Features

- Eight channels with optional peripheral trigger
- Full 32-bit source and destination pointers
- Flexible interrupt generation
- Programmable transfer length
- Flexible peripheral request per channel
- Option to initialize memory
- Programmable Edge-Sensitive request support
- Programmable support of AHB burst reads/writes, supporting both Memory-to-Memory and Memory-to-Peripheral transfers
- Burst lengths supported are 8-beat (INCR8) and 4-beat (INCR4)
- Programmable bus error detection support and IRQ generation upon detection
- FREEZE support also in on-going Memory-to-Memory transfers
- Support of “secure transfer” mode by a dedicated, conditionally secure DMA channel (DMA7)

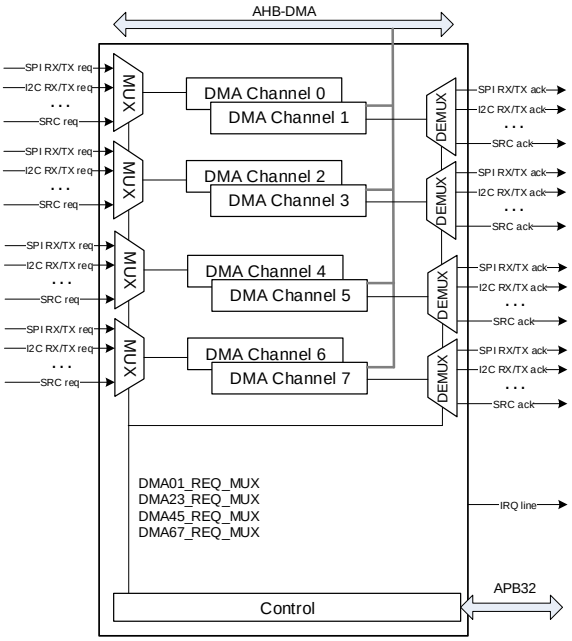

Figure 56: DMA Controller Block Diagram

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24.2 Architecture

24.2.1 DMA Peripherals

The list of peripherals that can request a DMA service is presented in Table 161.

Table 161: DMA Served Peripherals

Block	Direction(s)	Supported Access Rate
SPI	RX & TX	Single
SPI2	RX & TX	Single
SPI3	RX & TX	Single
UART	RX & TX	Single/Burst
UART2	RX & TX	Single/Burst
UART3	RX & TX	Single/Burst
I2C	RX & TX	Single/Burst
I2C2	RX & TX	Single/Burst
I2C3	RX & TX	Single/Burst
I3C	RX & TX	Single/Burst
SRC	Left & Right	Single/Burst (Left or Right)
SRC2	Left & Right	Single/Burst (Left or Right)
PCM	Left & Right	Single
GP_ADC	Read	Single
SD_ADC	Read	Single
O/QSPI FLASH	Read	Burst
QSPIC	Read & Write	Burst
QSPIC2	Read & Write	Burst
USB	RX & TX	Single
RAM	Read & Write	Burst

The Edge-sensitive requests cannot be used when DMA services the USB Rx path (USB-to-Memory). The same applies in the case of the SPI_CTRL_REG[SPI_PRIORITY] = 1 (either Rx or Tx FIFO is enabled). Nevertheless, it is strongly recommended for the case of USB Tx path (Memory-to-USB) and when serving the UART and I2C peripherals (Memory-to-Peripheral).

24.2.2 Input/Output Multiplexer

The multiplexing of peripheral requests is controlled by DMA_REQ_MUX_REG. So, if DMA_REQ_MUX_REG[DMAxy_SEL] is set to a certain (non-reserved) value, the RX/TX request from the corresponding peripheral will be routed to DMA channels x (RX request, even channel) and y (TX request, odd channel) respectively.

Similarly, an acknowledging de-multiplexing mechanism is applied.

However, when two or more bit-fields (peripheral selectors) of DMA_REQ_MUX_REG have the same value, the lesser significant selector will be given priority (see also the register's description).

24.2.3 DMA Channel Operation

A DMA channel is switched on with bit DMA_ON. This bit is automatically reset if the DMA transfer is finished. The DMA channels can either be triggered by software, or by a peripheral DMA request. If

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DREQ_MODE is 0, then a DMA channel is immediately triggered. If DREQ_MODE is 1 the DMA channel can be triggered by a Peripheral request.

If DMA starts, data is transferred from address DMAx_A_START_REG to address DMAx_B_START_REG for a length of DMAx_LEN_REG, which can be 8, 16, or 32 bits wide. The address increment is realized with an internal 16 bits counter DMAx_IDX_REG, which is set to 0 if the DMA transfer starts and is compared with the DMA_LEN_REG after each transfer. The register value is multiplied according to the AINC, BINC, and BW values before it is added to DMA_B_START_REG and DMA_B_START_REG. AINC or BINC must be 0 for register access.

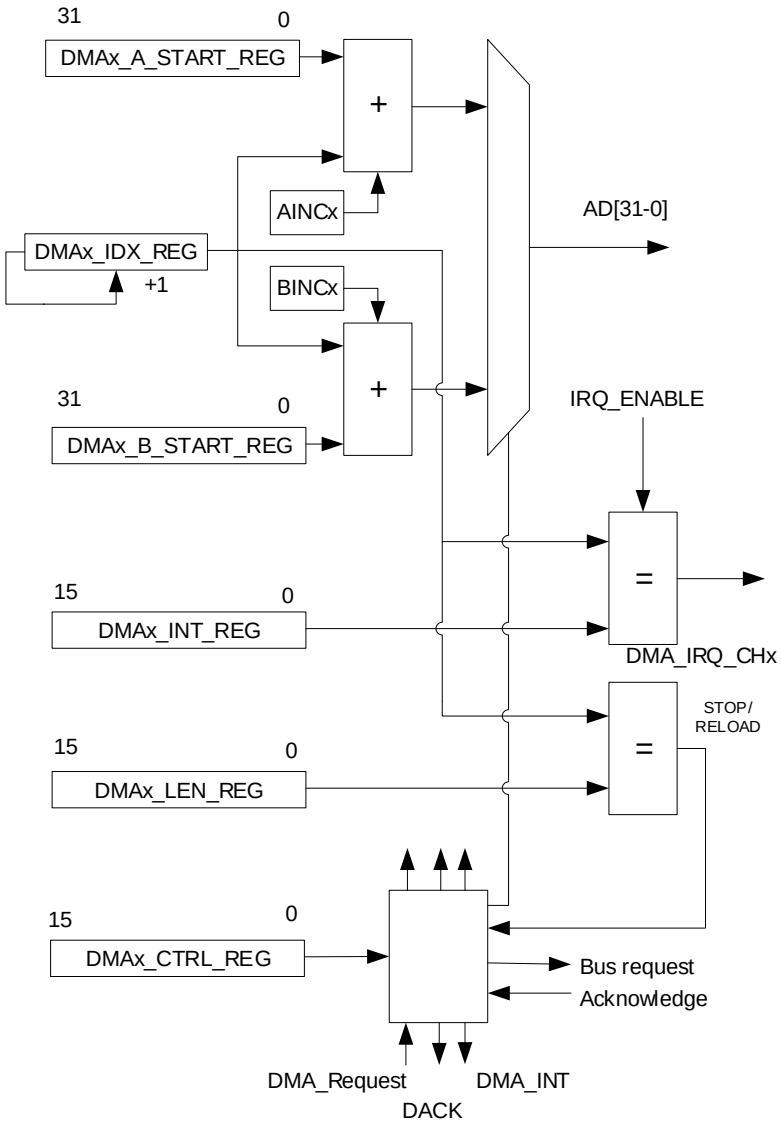

Figure 57: DMA Channel Diagram

If at the end of a DMA cycle the DMA start condition is still true, the DMA continues. The DMA stops when the transfer length is reached and, either DREQ_MODE is low, or DMAx_LEN_REG is equal to the internal index register. This condition also clears the DMA_ON bit.

If bit CIRCULAR is set to 1, the DMA controller automatically resets the internal index registers and continues from its starting address without the intervention of the CPU. If the DMA controller is started with DREQ_MODE = 0, the DMA will always stop, regardless of the state of CIRCULAR.

Each DMA channel can generate an interrupt if DMAx_INT_REG is equal to DMAx_IDX_REG. After the transfer and before DMAx_IDX_REG is incremented, the interrupt is generated.

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For example: if DMA_x_INT_REG=0 and DMA_x_LEN_REG=0, there will be one transfer and an interrupt.

It should be noted that there is no hardware protection from erroneous programming of the DMA registers. However, the software can be notified by an interrupt when a bus error has occurred in either the read or write cycle of the DMA transfer if DMAx_CTRL_REG[BUS_ERROR_DETECT] is set.

24.2.4 DMA Arbitration

The priority level of a DMA channel can be set with bits DMA_PRIO[2:0]. These bits determine which DMA channel will be activated in case there is more than one DMA channel request. If two or more channels have the same priority, an inherent priority applies (see register description).

With DREQ_MODE = 0, a DMA channel can be interrupted by a channel with a higher priority if the DMA_IDLE bit is set.

When DMA_INIT is set, however, the DMA channel currently performing the transfer locks the bus and cannot be interrupted by any other channel, until the transfer is completed, regardless if DMA_IDLE is set. The purpose of DMA_INIT is to initialize a specific memory block with a certain value, fetched also from memory, without any interruption from other active DMA channels that may request the bus at the same time. Consequently, it should be used only for memory initialization, while when the DMA transfers data to/ from peripherals, it should be set to 0. Note that AINC must be set to 0 and BINC to 1 when DMA_INIT is enabled.

It should be noted that memory initialization could also be performed without having the DMA_INIT enabled and by simply setting AINC to 0 and BINC to 1, provided that the source address memory value will not change during the transfer. However, it is not guaranteed that the DMA transfer will not be interrupted by other channels of higher priority when these request access to the bus at the same time.

24.2.5 Freezing DMA Channels

Each channel of the DMA controller can be temporarily disabled by writing a 1 to freeze all channels at SET_FREEZE_REG[FRZ_DMA]. To enable the channels again, a 1 to bits at the RESET_FREEZE_REG must be written. Note that the ongoing Memory-to-Memory transfers (DREQ_MODE=0) can also be interrupted (freeze).

24.2.6 Secure DMA Channel

If the security flag is enabled in the OTP header, then DMA channel #7 becomes a secure channel. This channel is then only used to move keys from the Symmetric Key Area to the AES block for encryption/decryption or the O/QSPI FLASH (XiP) Controller for on-the-fly decryption without the CPU being able to intervene.

24.3 Programming

There is a simple sequence of steps that need to be followed to configure the DMA Controller.

24.3.1 Memory to Memory Transfer

19. Set the length of data to be transferred (DMAx_LEN_REG).
20. Set the source address (DMAx_A_START_REG).
21. Set the destination address (DMAx_B_START_REG).
22. Configure the number of transfers until an interrupt is generated (DMAx_INT_REG).
23. Enable the IRQ of the used DMA channel if needed (DMA_INT_MASK_REG).
24. Configure transfer options:
    a. DMAx_CTRL_REG[AINC]: Automatic increment of source address.
    b. DMAx_CTRL_REG[BINC]: Automatic increment of destination address.

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c. DMAx_CTRL_REG[BW]: Bus transfer width.
d. DMAx_CTRL_REG[BURST_MODE]: Enable DMA read/write bursts if needed.

25. Start the DMA transfer by setting the DMAx_CTRL_REG[DMA_ON] bit.
26. Wait until the transfer is finished (DMAx_CTRL_REG[DMA_ON] = 0) or the corresponding interrupt.
27. Clear the IRQ if it was enabled (DMA_INT_STATUS_REG).

24.3.2 Peripheral to Memory Transfer

1. Set the length of data to be transferred (DMAx_LEN_REG).
2. Set the source address (DMAx_A_START_REG) equal to the peripheral Rx register (for example, I2C_DATA_CMD_REG).
3. Set the destination address (DMAx_B_START_REG).
4. Configure the number of transfers until an interrupt is generated (DMAx_INT_REG).
5. Map the peripheral to the selected channels pair (DMA_REQ_MUX_REG[DMAxy_SEL]).
6. Configure transfer options:
   a. DMAx_CTRL_REG[AINC]: Disable automatic increment of source address.
   b. DMAx_CTRL_REG[BINC]: Automatic increment of destination address.
   c. DMAx_CTRL_REG[BW]: Bus transfer width.
   d. DMAx_CTRL_REG[DREQ_MODE]: Enable triggering by peripheral DMA request.
   e. DMAx_CTRL_REG[DMA_PRIO]: Set channel priority.
   f. DMAx_CTRL_REG[BURST_MODE]: Enable DMA read/write bursts if needed. Note that SPI does not support burst transfers.
7. Enable the IRQ of the used DMA channel (DMA_INT_MASK_REG).
8. Start the DMA transfer by setting the DMAx_CTRL_REG[DMA_ON] bit.
9. Enable peripheral's DMA request (for example, I2C_DMA_CR_REG[TDMAE]).

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25 Crypto Engine

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

25.1 Introduction

The Crypto engine aims to accelerate the algorithm calculations that are needed to implement the RFC4835. It implements AES in ECB, CBC, and CTR modes. It also comprises HASH functions (SHA-1, SHA224/256/384/512, MD5). It supports AES128, AES192, AES 256 as well as the HMAC-SHA-256 authentication protocol.

The Crypto engine uses a DMA engine for transferring encrypted/decrypted data to shared memory in the AHB bus. The control registers of the IP are connected to the AHB bus.

The Crypto engine gives more flexibility to the way input data can be provided to the module. A calculation can be applied on fragmented input data, but not on data residing at a specific memory space, by means of successive register programming in the internal DMA engine.

Features

- AES (Advanced Encryption Standard) with 128, 192, or 256 bits key cryptographic algorithm
- HASH functions: MD5, SHA-1, SHA224/256/384/512 bits
- AES modes of operation
  - ECB (Electronic Code Book)
  - CBC (Cipher Block Chaining)
  - CTR (Counter)
- AHB Master DMA machine for data manipulation
- AHB Slave register file for configuration

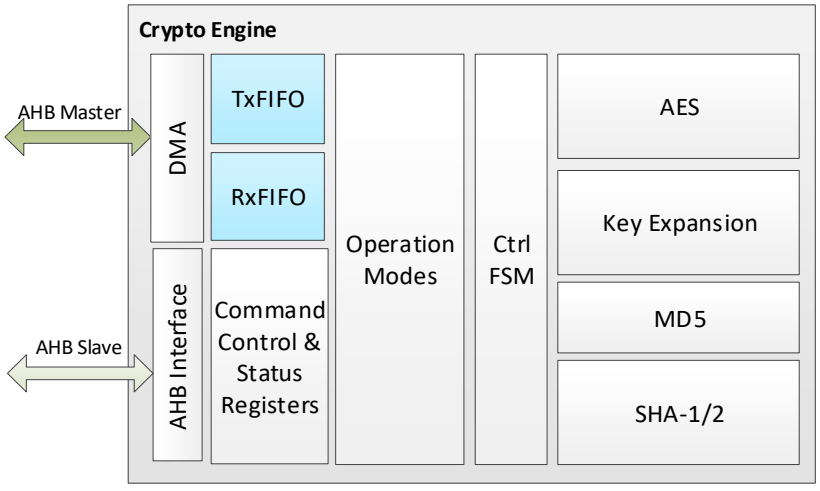

Figure 58: Crypto Engine Architecture

25.2 Architecture

The “Operation Modes” block controls the AES by implementing the respective mode that the selected encryption algorithms will operate each time. Also, this block communicates with DMA via two FIFO’s (RxFIFO and TxFIFO), which isolate the operation of the Crypto IP from the current status of the AHB-AMBA bus and also enable parallel transmission of data in bursts. By using burst transmission, the bus utilization is increased due to reduced bus access requests.

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The “Ctrl FSM” block checks the FIFO’s and DMA status continuously and decides the amount of data traffic, plus which of the FIFO’s will be used. It also decides the “switching off” of the AES/HASH after transferring all results to the memory. The “HASH” block contains all the logic required for the realization of the hash algorithms calculations, as well as circuitry for the padding of data. It also contains glue logic for the transfer of the results to the “Operation Modes” block.

25.2.1 AES

This part of the architecture implements the AES algorithm described in the AES-FIPS PUB 197. The capability it offers is the encryption and decryption of 128 bits data blocks by using 128-, 192-, or 256-bits encryption key.

25.2.2 Operation Modes

The block “Operation Modes” uses the AES to implement the following modes of operations:

- ECB (Electronic Code Book)
- CBC (Cipher Block Chaining
- CTR (Counter)

Padding requirements of the algorithms, to convert all data to multiples of 16 bytes (for AES), must be addressed by software.

By applying successive programming of AES-CBC encryptions using software, the realization of the HMAC-XCBC-AES-96 algorithm is possible.

The implementation of the AES-CCM is feasible, just like the implementation of AES-CTR algorithms for encryption, and AES-CBC for authentication.

25.2.3 HASH

Padding at the input data is automatically applied as required by the hash algorithms. Two types of padding are implemented, due to the different algorithms supported. The purpose is to ensure that the message is a multiple of 512 or 1024 bits, depending on the algorithm. Padding is done similarly in both cases. After the last data byte, one extra byte of value 0x80 is added. Next, a number of bytes (0x00) is added, so that the overall size of the data block (including the extra bytes) mod 512/1024 is 448/896, depending on the algorithm. Following that, a 64/128-bits big-endian number is attached, which represents the size of the data block, in bits (without the padding). While in this process, TX/RX FIFOs are switched into 8-bytes mode.

The block packetizes the algorithm result (128 to 512 bits) into blocks of 64 bytes so that they can be shifted to the TX FIFO. The following hash algorithms are implemented:

- MD5: RFC1321
- SHA-1: FIPS PUB 180-4
- SHA-224/256: FIPS PUB180-4. In this case only initialization changes
- SHA-384/512: FIPS PUB 180-4

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25.3 Programming

25.3.1 AES Engine Programming

There is a simple sequence of steps that needs to be followed to program the AES Engine:

1. Enable the clock by setting the CLK_AMBA_REG[AES_CLK_ENABLE] bit.
2. Select the AES mode (CRYPTO_CTRL_REG[CRYPTO_HASH_SEL] = 0).
3. Define the mode of operation of the AES algorithm (CRYPTO_CTRL_REG[CRYPTO_ALG_MD]). For the CBC/CTR mode of operation, the corresponding IV/CTR block should be defined in the CRYPTO_MREGx_REG registers.
4. Select the AES algorithm (CRYPTO_CTRL_REG[CRYPTO_ALG] = 0).
5. Select the size of AES Key (CRYPTO_CTRL_REG[CRYPTO_AES_KEY_SZ]).
6. Use AES keys expansion if needed (CRYPTO_CTRL_REG[CRYPTO_AES_KEXP]). If the key expansion is enabled, define the (basic) key in the local CRYPTO_KEYS_START memory.
7. Set up data fetching address (CRYPTO_FETCH_ADDR_REG).
8. Set up data destination address (CRYPTO_DEST_ADDR_REG).
9. Set data length (CRYPTO_LEN_REG).
10. Select to Encrypt or Decrypt (CRYPTO_CTRL_REG[CRYPTO_ENCDEC]).
11. Enable the process by setting the CRYPTO_START_REG[CRYPTO_START] bit.
12. Wait the process to finish (CRYPTO_STATUS_REG[CRYPTO_INACTIVE] = 1).

25.3.2 HASH Engine Programming

There is a simple sequence of steps that needs to be followed to program the HASH Engine:

1. Enable the clock by setting the CLK_AMBA_REG[AES_CLK_ENABLE] bit.
2. Select the HASH mode (CRYPTO_CTRL_REG[CRYPTO_HASH_SEL] = 1).
3. Set the number of bytes that will be saved at the memory by the DMA (CRYPTO_CTRL_REG[CRYPTO_HASH_OUT_LEN], see register description).
4. Define the mode of operation of the HASH algorithm (CRYPTO_CTRL_REG[CRYPTO_ALG_MD], see register description).
5. Select the HASH algorithm (CRYPTO_CTRL_REG[CRYPTO_ALG], see register description).
6. Set up data fetching address (CRYPTO_FETCH_ADDR_REG).
7. Set up data destination address (CRYPTO_DEST_ADDR_REG).
8. Set data length (CRYPTO_LEN_REG).
9. Enable the process by setting the CRYPTO_START_REG[CRYPTO_START] bit.
10. Wait the process to finish (CRYPTO_STATUS_REG[CRYPTO_INACTIVE] = 1).

For both cases, an interrupt can be enabled upon the completion of the processing, by setting 1 to the CRYPTO_CTRL_REG[CRYPTO_IRQ_EN] (the interrupt should be enabled also in the CPU).

The clock of the Crypto Block should be disabled after the completion of each operation, by clearing the CLK_AMBA_REG[AES_CLK_ENABLE] bit, if there is no other operation to be performed.

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26 Wake-Up Controller

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

26.1 Introduction

The Wake-Up Controller can be programmed to wake up the DA1470x from the Extended Sleep (clocked) mode. It consists of two parallel circuits that can be programmed regarding the GPIO edge or level monitored one with a debouncing counter usually used for buttons and another that indicates which GPIO has toggled.

The block diagram illustrating the Wake-Up function is depicted in Figure 59.

Features

- Monitors any GPIO state change
- Implements debouncing time from 0 up to 63 ms
- Latches the status of the monitored lines
- Generates three interrupts to PDC, Arm Cortex-M33, and SNC ARM Cortex M0+
- Generates a signal bus towards PDC indicating which GPIO has toggled
- Wakes up the system from Extended Sleep
- Supports level and edge detection for waking up

26.2 Architecture

The Wake-up controller can monitor all GPIO lines for an event. A line of XOR gates defines the polarity of the signal to be monitored. Two parallel structures are implemented explicitly separated in Figure 59 by a dashed line:

- KEY_WAKEUP: It can be programmed to monitor a number of GPIOs regarding their edge or level. After GPIO toggles, a debounce counter can be triggered to debounce the key press before generating an interrupt. The KEY_WKUP_GPIO_IRQ is generated towards the Cortex-M33, SNC, and the PDC (named as Debounced_IO in the PDC). The debouncing time can be programmed up to 63 ms. If debouncing is selected to be 0, the interrupt is issued on edge detection, but the external signal needs to be at least 2xRCLP (32K/512K) clock periods asserted considering the system being active.

  This circuit can wake up the system from Extended (clocked) Sleep. Since the interrupt is kept asserted until acknowledged by SW, the Cortex-M33 can receive it after its power domain has been powered up by PDC. Of course, a respective PDC entry needs to be in place for waking up Cortex-M33.

  When the system is active, the circuit can keep on being used as a button press indicator with debouncing. Note that, if multiple GPIOs have been toggled there is no indication of which one has generated the interrupt.

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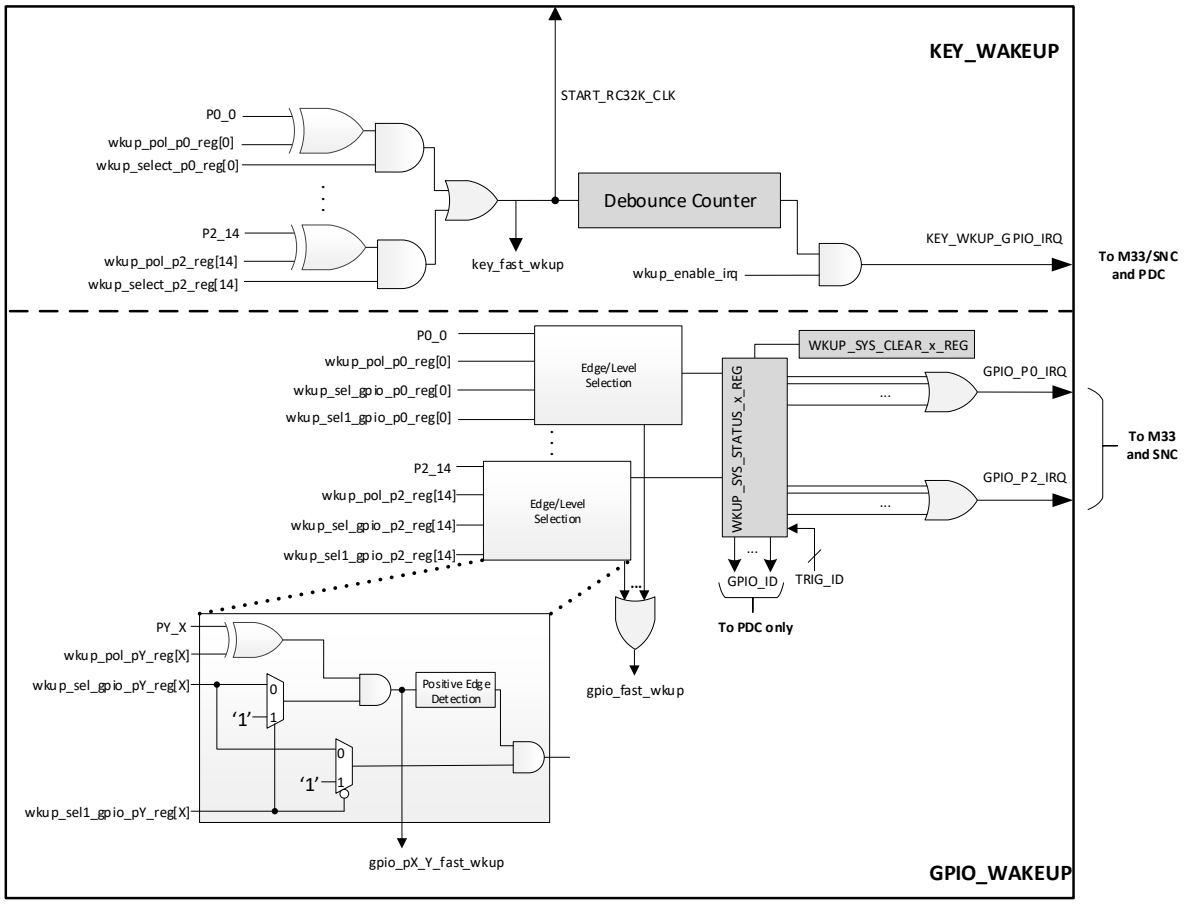

Figure 59: Wake-Up Controller Block Diagram

- GPIO_WAKEUP: This circuit can be programmed to monitor edge (positive or negative) or level sensitive triggers and latch them into a status register, so the source is known by the application. The default behavior is level sensitive. This status register isdelivered to the PDC in form of a signal bus for being used as a trigger for the PDC entries. Moreover, an OR of each GPIO port signal forms a level interrupt towards the Cortex-M33 and SNC, namely GPIO_P0_IRQ, GPIO_P1_IRQ, and GPIO_P2_IRQ.

  Since these three interrupt lines are kept asserted until acknowledged by SW, the M33 or SNC can receive them after its power domain has been powered up by PDC. Of course, a respective PDC entry needs to be in place for waking up Cortex-M33 or SNC.

  The edge or level detection functionality is programmable with the introduction of an extra configuration bit (wkup_sel1_gpio_pY_reg). There is a configuration bit for the selection between the edge-sensitive and level-sensitive operation of the wake-up controller, for a specific GPIO pin, as shown in Table 162.

Table 162: Edge/Level Triggering Configuration for Wake-Up

Configuration	wkup_sel_gpio_pY_reg	wkup_sel1_gpio_pY_reg
Edge sensitive	Enable(1)/Disable(0)	1
Level sensitive	Enable(1)/Disable(0)	0

Figure 60 and Figure 61 shows the IRQ generation based on the configuration of wkup_sel_gpio_pY_reg and wkup_sel1_gpio_pY_reg bits.

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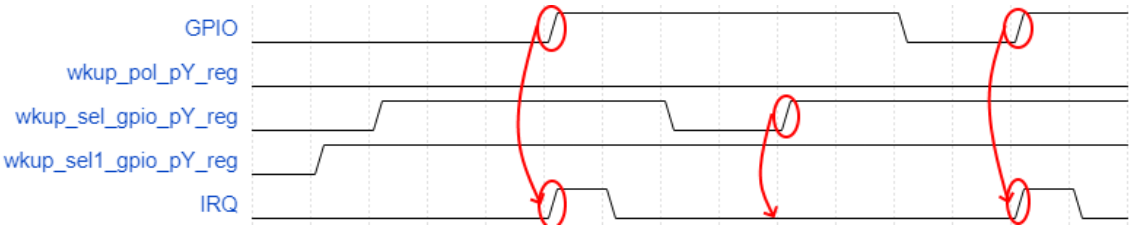

Figure 60: Edge Sensitive GPIO

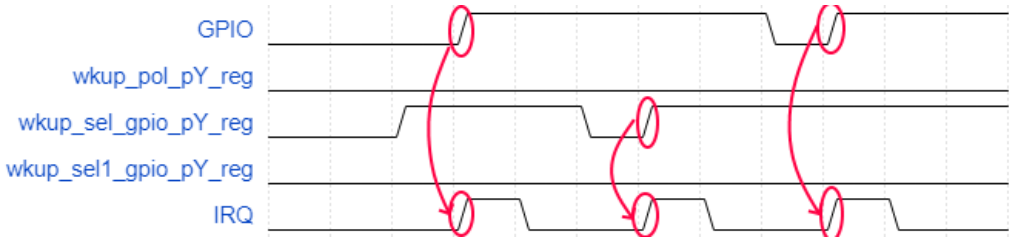

Figure 61: Level Sensitive GPIO

When the system is active, the circuit can keep on being used as an interrupt generator towards Cortex-M33 storing the GPIO state that has caused the interrupt in the first place.

NOTE
The circuits KEY_WAKEUP and GPIO_WAKEUP can wake up the system from any clocked sleep (Deep or Extended) but not from Hibernation.

26.3 Programming

There is a simple sequence of steps that needs to be followed to program the Wake-Up controller:

1. Enable the Wake-Up Controller by setting the CLK_TMR_REG[WAKEUPCT_ENABLE] bit.
2. Set up triggering polarity (WKUP_POL_Px_REG).
3. If debouncing is needed, define debounce time in WKUP_CTRL_REG[WKUP_DEB_VALUE].
4. Register PDC and/or KEY Interrupts:
   a. Add PDC Entries (needed when the device goes to sleep).
   b. Clear any latched values of the GPIOs (WKUP_CLEAR_Px_REG).
   c. Add Wake-Up events (WKUP_SELECT_Px_REG).
   d. Add GPIO interrupts (WKUP_SEL_GPIO_Px_REG and WKUP_SEL1_GPIO_Px_REG).
5. If needed, add the corresponding ISRs and enable the interrupts KEY_WKUP_GPIO_IRQ, GPIO_P0_IRQ, GPIO_P1_IRQ, GPIO_P2_IRQ, PDC_IRQ).

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27 Wake-Up from Hibernation Controller

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

27.1 Introduction

To support extremely low power hibernation, a small wakeup mechanism is implemented. This circuit is in the PD_AON domain. To further reduce the power consumption only a specific number of pins (4) can wake up the device from a hibernation state and only with a rising edge pulse. Finally, the VBUS_AVAILABLE signal can also wake up the device.

27.2 Architecture

The block diagram of the wake-up from (clockless) hibernation controller is shown in Figure 62.

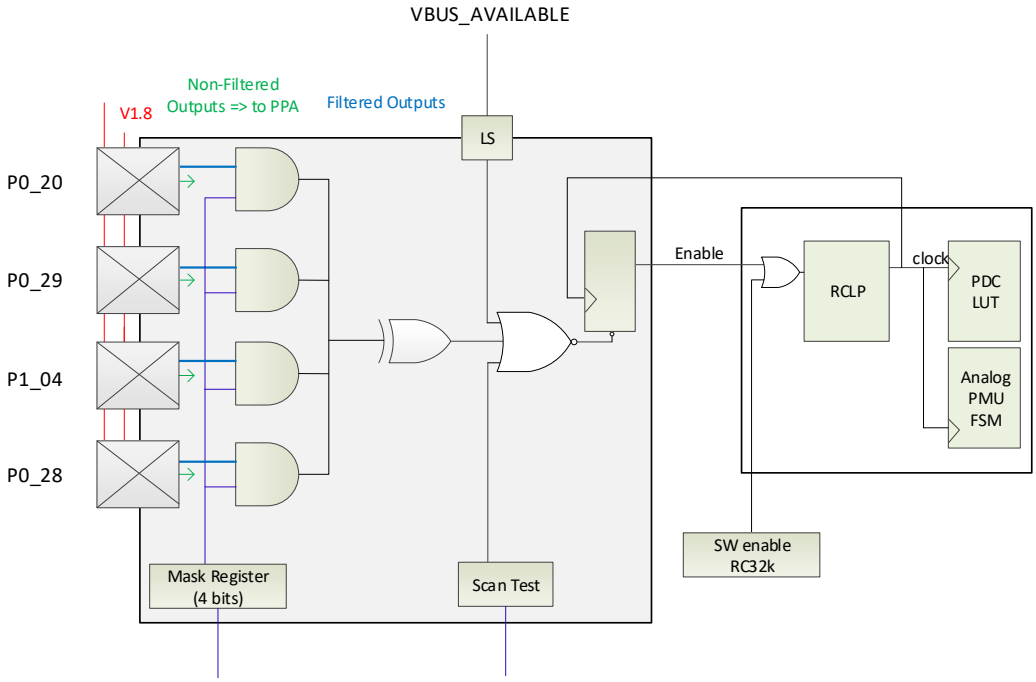

Figure 62: Wake-Up from Hibernation Block Diagram

The grey box is the wake-up from the hibernation circuit. The output enable signal is produced by controlling the async reset of a flip-flop and it is the signal that starts the RCLP module. When RCLP is enabled, the flip-flop is clocked and as a result, it is cleared.

Only four pads and the VBUS_AVAILABLE signal are used as wake-up triggers. The pads feature two outputs:

- A filtered output which is used to enable the RCLP
- Non-filtered output which will be driven to the PPA for general purpose use

A selectable pull-down resistor on the pads can be enabled during hibernation to prevent the wake-up pads from floating. Also, note that floating back-gate diode exists on the pads during hibernation, and lifting them up results in currents. The register file of the hibernation wake-up logic is in the PD_SLP domain and only the flip flops, shown in Figure 62, are reside in the PD_AON domain. An additional level-shifter cell is used for the VBUS_AVAILABLE signal.

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27.3 Programming

There is a simple sequence of steps that needs to be followed to configure the wake-up from hibernation controller block:

1. Enable pull-down on the HiWUx GPIOs if needed by configuring the WAKEUP_HIBERN_REG[WAKEUP_PD_EN] fields.
2. Select which of the HiWU GPIOs will wake up the system from the hibernation in WAKEUP_HIBERN_REG[WAKEUP_EN] fields.
3. Enable the hibernation mode by setting WAKEUP_HIBERN_REG[HIBERATION_ENABLE] bit.

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28 General Purpose ADC

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

28.1 Introduction

The DA1470x is equipped with a high-speed ultra-low-power 10-bit general-purpose Analog-to-Digital Converter (GPADC). It can operate in unipolar (single-ended) mode as well as in bipolar (differential) mode. The ADC has its own voltage regulator (LDO) of 0.9 V, which represents the full-scale reference voltage. Figure 63 shows the block diagram of the GPADC.

Features:

- 10-bit ADC
- Maximum 2.6 MS/s
  - Sampling time programmable between 125 ns and 7.5 µs
- Averaging up to 128 samples to reduce noise and achieve ENOB = 11 bits
- Four single-ended or two differential external input channels (GPIOs)
- Reference voltage = 900 mV
  - Vin = 0 V to +900 mV (single-ended), and -900 mV to +900 mV (differential)
  - Attenuators 2x, 3x, 4x supporting different input ranges up to 3.6 V
- Configurable sample manipulation functionality
- Battery and the internal V_{DD} monitoring channels
- Chopper function
- Offset adjust
- Common-mode input level adjust

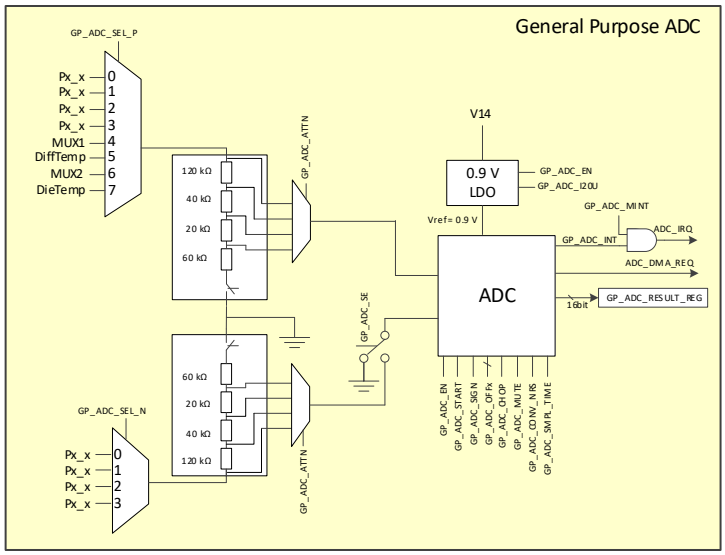

Figure 63: Block Diagram of GPADC

28.2 Architecture

The ADC architecture shown in Figure 63 has the following subblocks:

- Analog to Digital converter (ADC)
  - ADC analog part internally clocked with 100 MHz

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- ADC logic part clocked with the ADC_CLK which is the 16 MHz (DivN_clk/2)
- 0.9 V LDO for the ADC supply with a high PSRR
- Configurable attenuator with 1×, 2×, 3×, and 4× attenuation
- APB Bus interface clocked with the APB clock (APB-32 slow bus). Control and status registers are available through registers GP_ADC_*
- Maskable Interrupt (ADC_IRQ) and DMA request (ADC_DMA_REQ)
- ADC input channel selector. Up to four GPIO pins, the VBAT/VBUS/VSYS rails, the DCDC outputs, the two temperature sensors, and the internal V_{DD}

28.2.1 Input Channels

Table 163 summarizes the ADC input channels. The GPIO signals at the channels [3:0] can be monitored both single-ended and differentially. The signals at the 4-7 inputs can be monitored single-ended or differentially with respect to the GPIOs.

Table 163: ADC Input Channels

Channel	Signal	Description
3:0	GPIO [P0_30, P0_27, P0_06, P0_05]	General Purpose Inputs
4	ADC MUX 1	Table 164
5	Differential Temperature Sensor	Differential Temp Sensor for RF calibration
6	ADC MUX 2	Table 165
7	Temperature Sensor	Temperature Sensor

Table 164: ADC MUX1

Channel	Signal	Description
0	Disabled	No rail selected
1	NC	Not connected
2	Reserved	Reserved
3	I_sense_bus	Enable the current sensing for one of the LDO's (GP_ADC_SEL_REG[GP_ADC_LDO_SENSE_SEL])
4	Reserved	Reserved
5	V30	DCDC Converter V30 rail
6	Reserved	
7	V18F	DCDC Converter V18F rail

Table 165: ADC MUX2

Channel	Signal	Description
0	Disabled	No rail selected
1	V12	DCDC Converter V12 rail
2	V18	DCDC Converter V18 rail
3	V14	DCDC Converter V14 rail
4	V18P	DCDC Converter V18P rail
5	VSYS	DCDC Converter VSYS rail

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Channel	Signal	Description
6	VBUS	DCDC Converter VBUS rail
7	VBAT	DCDC Converter VBAT rail

Table 166 summarizes the voltage ranges which can be handled with the single-ended or differential operation for different attenuation values. The single-ended/differential mode is controlled by the bit GP_ADC_CTRL_REG[GP_ADC_SE] and the attenuation is handled by the bit GP_ADC_CTRL2_REG[GP_ADC_ATTN].

Table 166: GPADC External Input Channels and Voltage Range

GP_ADC_ATTN	GP_ADC_SE	Input Scale	Input Limits
0 (1 ×)	0 1	-0.9 V to +0.9 V 0 V to +0.9 V	-1 V to +1 V -0.1 V to 1V
1 (2 ×)	0 1	-1.8 V to +1.8 V 0 V to +1.8 V	-1.9 V to +1.9 V -0.1 V to 1.9 V
2 (3 ×)	0 1	-2.7 V to +2.7 V 0 V to +2.7 V	-2.8 V to +2.8 V -0.1 V to 2.8 V
3 (4 ×)	0 1	-3.6 V to +3.6 V 0 V to +3.6 V	-3.45 V to +3.45 V -0.1 V to 3.45 V

Table 167 shows the maximum input voltages and the ratio for the VBAT/VSYS/VBUS rails measurements using the GPADC block.

Table 167: GPADC Max Voltage and Rations for VBAT/VSYS/VBUS Rails

Rail	Max GP-ADC in Voltage [V]	Ratio
VBAT	4.762	0.189
VSYS	5.732	0.157
VBUS	5.488	0.164

28.2.2 Operating Modes

The GPADC operation flow diagram is shown in Figure 64.

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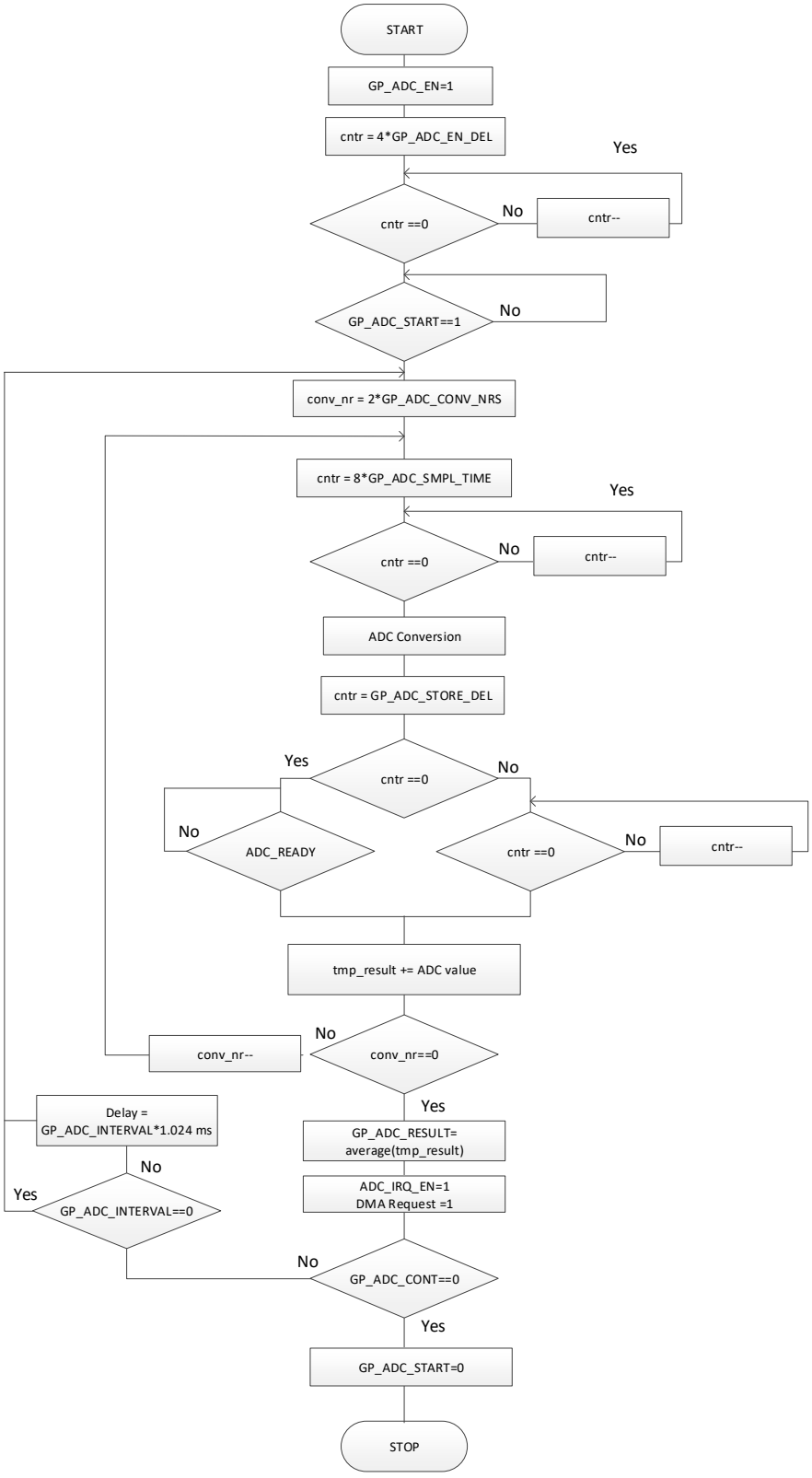

Figure 64: GPADC Operation Flow Diagram

28.2.2.1 Enabling the ADC

Enabling/disabling of the ADC is triggered by configuring bit GP_ADC_CTRL_REG[GP_ADC_EN]. When the bit is set to 1, first the LDO is enabled. Then after the delay value set in

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GP_ADC_CTRL3_REG[GP_ADC_EN_DEL] (typically 16 µs to account for the LDO settling time), the ADC is enabled, and an AD conversion can be started. See Table 168 for recommended values.

Table 168: ADC_LDO Start-Up Delay

f_{ADC_CLK}	GP_ADC_EN_DEL	$T_{ADC\_EN\_DEL}$
16 MHz	0x40	16 µs

Formula:

GP_ADC_EN_DEL = $T_{ADC\_EN\_DEL} \times f_{ADC\_CLK} / 4$

This value must be rounded up to the nearest integer.

The GPADC is a dynamic ADC and consumes no static power, except for the ADC_LDO which consumes approximately 20 µA. Therefore, GP_ADC_EN must be set to 0 if the ADC is not used.

The V14 rail of the DCDC should be enabled before enabling the GP-ADC block.

28.2.2.2 Manual Mode

An AD conversion can be started by setting GP_ADC_START to 1. While the conversion is active, GP_ADC_START remains 1. When a conversion is finished, the hardware sets GP_ADC_START to 0 and GP_ADC_INT to 1 (interrupt), and GP_ADC_RESULT_REG contains the valid ADC value. While the conversion is active, writing 1 to GP_ADC_START does not start a new conversion. SW should always check that bit GP_ADC_START = 0 before starting a new conversion.

28.2.2.3 Continuous Mode

Setting GP_ADC_CTRL_REG[GP_ADC_CONT] to 1 enables the continuous mode, which automatically starts a new AD conversion when the current conversion has been completed. The GP_ADC_START bit is only needed once to trigger the first conversion. If the continuous mode is active, GP_ADC_RESULT_REG always contains the latest ADC value.

To correctly terminate the continuous mode, it is required to disable the GP_ADC_CONT bit first and then wait until the GP_ADC_START bit is cleared to 0, so the ADC is in a defined state.

NOTE
Before making any changes to the ADC settings, users must disable the continuous mode by setting bit GP_ADC_CONT to 0 and waiting until bit GP_ADC_START = 0.

The time interval between two successive AD conversions is programmable with GP_ADC_CTRL3_REG[GP_ADC_INTERVAL] in steps of 1.024 ms. If GP_ADC_INTERVAL = 0, the conversion restarts immediately. If GP_ADC_INTERVAL is not zero, the ADC first synchronizes to the delay clock before starting the conversion. This can take up to 1 ms.

28.2.3 Conversion Modes

28.2.3.1 AD Conversion

Each AD conversion has three phases:

- Sampling
- Conversion
- Storage

The AD conversion starts with the sampling phase. This phase ends after the time set in GP_ADC_CTRL2_REG[GP_ADC_SMPL_TIME] and triggers the conversion phase. If GP_ADC_CTRL2_REG[GP_ADC_STORE_DEL] = 0, handshaking is used, that is, the ADC result is stored when a conversion is finished. Otherwise, a fixed (programmable) delay is used, and the result is stored regardless of whether the conversion is finished or not.

The total conversion time of an AD conversion depends on various settings. In short, it is as follows.

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$$T_{ADC} = \frac{N_{CONV} \cdot \left(N_{CYCL\_SMPL} + N_{CYLC\_STORE}\right)}{f_{ADC\_CLK}} \quad (1)$$

Where

- N_{CONV} = the number of conversions. This is related to the value programmed in GP_ADC_CTRL2_REG[GP_ADC_CONV_NRS], following $2^{GP\_ADC\_CONV\_NRS}$. When GP_ADC_CTRL_REG[GP_ADC_CHOP] is set, the minimum value for N_{CONV} is always 2.
- N_{CYLC_SMPL} = the number of ADC_CLK cycles used for sampling, which is 8 × GP_ADC_CTRL2_REG[GP_ADC_SMPL_TIME].
- N_{CYCL_STORE} = the number of ADC_CLK cycles until the result is stored. When GP_ADC_CTRL2_REG[GP_ADC_STORE_DEL] = 0, handshaking is used. With handshaking, the number of ADC_CLK cycles is typically three. This value may spread from sample to sample and over temperature, otherwise, the number of ADC_CLK cycles is GP_ADC_CTRL2_REG[GP_ADC_STORE_DEL] + 1.

Sampling Phase

The sampling time can be programmed via GP_ADC_CTRL2_REG[GP_ADC_SMPL_TIME] and depends on the sampling time constant in combination with the desired sampling accuracy. This sampling time constant, τ_{ADC_SMPL} (Table 169), then depends on the output impedance of the source, the internal resistive dividers, and the internal sampling capacitor. And the number of required time constants is given by the natural logarithm of the desired accuracy, that is, ln(2^N_{BIT}). For N_{BIT} = 10-bit accuracy, seven-time constants are required.

Table 169: ADC Sampling Time Constant (τ_{ADC_SMPL})

ADC Input	τADC_SMPL
GPADC0, GPADC1 (GP_ADC_ATTN = 0)	ROUT × 0.5 pF (Differential Input) ROUT × 1 pF (Single-Ended Input)
GPADC0, GPADC1 (GP_ADC_ATTN = 1)	(ROUT + 120 kΩ) × 0.5 pF (Differential Input) (ROUT + 120 kΩ) × 1 pF (Single-Ended Input)
GPADC0, GPADC1 (GP_ADC_ATTN = 2)	(ROUT + 160 kΩ) × 0.5 pF (Differential Input) (ROUT + 160 kΩ) × 1 pF (Single-Ended Input)
GPADC0, GPADC1 (GP_ADC_ATTN = 3)	(ROUT + 180 kΩ) × 0.5 pF (Differential Input) (ROUT + 180 kΩ) × 1 pF (Single-Ended Input)

Formula:

GP_ADC_SMPL_TIME = ln(2^N_{BIT}) × τ_{ADC_SMPL} × f_{ADC_CLK} / 8

This value must be rounded up to the nearest integer.

Conversion and Storage Phase

One AD conversion typically takes around 125 ns with a 100 MHz internal ADC clock. The result can be stored either by handshaking or after a fixed number of cycles (programmable).

- Handshake mode (GP_ADC_STORE_DEL = 0)

  In handshake mode, the conversion result is available in GP_ADC_RESULT_REG after two sampling ADC_CLK cycles plus two conversion ADC_CLK cycles plus two ADC_CLK cycles for synchronization.
- Fixed delay mode (GP_ADC_STORE_DEL > 0)

  In fixed delay mode, the conversion result is available in GP_ADC_RESULT_REG after the programmed storage delay, regardless of whether the conversion is ready or not. Note that, when the delay is too short (that is, the conversion is not finished in the allocated time), the old (previous) ADC result is stored.

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28.2.3.2 Averaging

To reduce noise and improve performance, multiple samples can be averaged out (assuming the time average of noise equals zero). This is handled by HW and can be controlled by setting GP_ADC_CTRL2_REG[GP_ADC_CONV_NRS] to a non-zero value. The actual number of the consecutive samples taken is by $2^{GP\_ADC\_CONV\_NRS}$.

Because the internal noise also acts as a form of dither, the actual accuracy can be improved. Therefore, the ADC result is not truncated to 10-bit but stored as 16-bit left-aligned, and truncation is left for the user. The expected Effective Number of Bits (ENOB) is shown in Table 170.

Table 170: ENOB in Oversampling Mode

GP_ADC_CONV_NRS	ENOB (Left Aligned) in GP_ADC_RESULT_REG
0	> 9
1	> 9
2	> 9
3	> 10
4	> 10
5	> 10
6	> 11
7	> 11

28.2.3.3 Chopper Mode

Inherently, the ADC has a DC offset (E_{OFS}). When GP_ADC_CTRL_REG[GP_ADC_CHOP] is set to 1, the hardware triggers two consecutive AD conversions and flips the sign of the offset in-between. Summing the two samples effectively cancels out the inherent ADC offset. This method also smooths other non-ideal effects and is recommended for DC and the slowly changing signals.

When combined with averaging, every other AD conversion is taken with the opposite sign. Without averaging two AD conversions are always triggered.

Note that a DC offset causes saturation effects at zero scale or full scale. When chopping is used without offset calibration, non-linear behavior is introduced towards zero scale and full scale.

28.2.4 Additional Settings

The hardware also supports pre-ADC attenuation via GP_ADC_CTRL2_REG[GP_ADC_ATTN]:

- Setting 0 disables the attenuator
- Setting 1 scales the input range by a factor of two
- Setting 2 scales the input range by a factor of three
- Setting 3 scales the input range by a factor of four

With bit GP_ADC_CTRL_REG[GP_ADC_MUTE] = 1, the input is connected to 0.5 × ADC reference. So, the ideal ADC result should be 511.5. Any deviation from this is the ADC offset.

With bit GP_ADC_CTRL_REG[GP_ADC_SIGN] = 1, the sign of the offset is inverted. When the chopper is used, the hardware alternates GP_ADC_SIGN = 0 and 1. This bit is typically only used for the offset calibration routine described in Section 28.2.6 and has no specific use to the end user.

28.2.5 Non-Ideal Effects

Besides Differential Non-Linearity (DNL) and Integral Non-Linearity (INL), each ADC has a gain error (linear) and an offset error (linear). The gain error (E_G) of the GPADC affects the effective input range. The offset error (E_{OFS}) causes the effective input scale to become non-centered. The offset error can be reduced by chopping and/or by offset calibration.

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The ADC result also includes some noise. If the input signal itself is noise free (inductive effects included), the average noise level is ±1 LSB. Reducing noise effects can be done by taking more samples and calculating the average value. This can be done by programming GP_ADC_CTRL2_REG[GP_ADC_CONV_NRS] to a non-zero value.

With a “perfect” input signal (for example, if a filter capacitor is placed close to the input pin), most of the noise comes from the low-power voltage regulator (LDO) of the ADC. Since the DA1470x is targeted for ultra-compact applications, there is no pin available to add a capacitor at this voltage regulator output.

The dynamic current of the ADC causes extra noise at the regulator output. This noise can be reduced by setting bits GP_ADC_CTRL2_REG[GP_ADC_I20U]. Bit GP_ADC_I20U enables a constant 20 µA load current at the regulator output so that the current does not drop to zero. This increases power consumption by 20 µA.

28.2.6 Offset Calibration

A relative high offset error is caused by a very small dynamic comparator. This offset error can be canceled with the chopping function, but it still causes unwanted saturation effects at zero scale or full scale. With GP_ADC_OFFP_REG and GP_ADC_OFFN_REG, the offset error can be compensated in the ADC network itself. To calibrate the ADC, follow the steps in Table 171. In this routine, 0x200 is the target mid-scale of the ADC.

Table 171: GPADC Calibration Procedure for Single-Ended and Differential Modes

Step	Single-Ended Mode (GP_ADC_SE = 1)	Differential Mode (GP_ADC_SE = 0)
1	Set GP_ADC_OFFP = GP_ADC_OFFN = 0x200; GP_ADC_MUTE = 0x1; GP_ADC_SIGN = 0x0.	Set GP_ADC_OFFP = GP_ADC_OFFN = 0x200; GP_ADC_MUTE = 0x1; GP_ADC_SIGN = 0x0.
2	Start conversion.	Start conversion.
3	adc_off_p = GP_ADC_RESULT - 0x200	adc_off_p = GP_ADC_RESULT - 0x200
4	Set GP_ADC_SIGN = 0x1.	Set GP_ADC_SIGN = 0x1.
5	Start conversion.	Start conversion.
6	adc_off_n = GP_ADC_RESULT - 0x200	adc_off_n = GP_ADC_RESULT - 0x200
7	GP_ADC_OFFP = 0x200 - 2 × adc_off_p GP_ADC_OFFN = 0x200 - 2 × adc_off_n	GP_ADC_OFFP = 0x200 - adc_off_p GP_ADC_OFFN = 0x200 - adc_off_n

To increase the accuracy, it is recommended to set the GP_ADC_CTRL2_REG[GP_ADC_SMPL_TIME] = 2 or 3 and GP_ADC_CTRL2_REG[GP_ADC_CONV_NRS] = 3 or 4 prior to this routine.

It is recommended to implement the above calibration routine during the initialization phase of DA1470x. To verify the calibration results, check whether the GP_ADC_RESULT value is close to 0x200 while bit GP_ADC_CTRL_REG[GP_ADC_MUTE] = 1.

28.2.7 Zero-Scale Adjustment

The GP_ADC_OFFP and GP_ADC_OFFN registers can also be used to set the zero-scale or full-scale input level at a certain target value. For instance, they can be used to calibrate GP_ADC_RESULT to 0x000 at an input voltage of exactly 0.0 V or to calibrate the zero scale of a sensor.

28.2.8 Common Mode Adjustment

The common mode level of the differential signal must be 0.45 V = Full Scale/2 (or 1.35 V with GP_ADC_ATTN = 2, that is, 3× attenuation). If the common mode input level of 0.45 V cannot be achieved, the common mode level of the GPADC can be adjusted via GP_ADC_OFFP_REG and

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GP_ADC_OFFN_REG according to Table 172. The GPADC can tolerate a common mode margin of up to 50 mV.

Table 172: Common Mode Adjustment

CM Voltage (V_{ccm})	GP_ADC_OFFP = GP_ADC_OFFN
0.225 V	0x300
0.450 V	0x200
0.675 V	0x100

Any other common mode levels between 0.0 V and 0.9 V can be calculated from Table 172. Offset calibration can be combined with common mode adjustment by replacing the 0x200 value in the offset calibration routine with the value required to get the appropriate common mode level.

28.2.9 Input Impedance, Inductance, and Input Settling

The GPADC has no input buffer stage. During the sampling phase, a capacitor of 0.5 pF in differential mode or 1 pF in single-ended mode is switched to the input line(s). The pre-charge of this capacitor is at the midscale level, so the input impedance is infinite.

During the sampling phase, a certain settling time is required. A 10-bit accuracy requires at least seven-time constants τ_{ADC_SMPL}, determined by the output impedance of the input signal source, the internal resistive dividers, and the 0.5 pF or 1 pF sampling capacitor. See Table 169.

The inductance from the signal source to the ADC input pin must be very small. Otherwise, filter capacitors are required from the input pins to the ground (single-ended mode) or from pin to pin (differential mode).

28.2.10 Configurable Sample Manipulation

The GPADC supports configurable sample manipulation in the result register based on Table 173.

Table 173: Configurable Sample Manipulation

GP_ADC_CTRL2_REG [GP_ADC_CONV_NRS]	GP_ADC_CTRL_REG [GP_ADC_CHOP]	GP_ADC_RESULT_REG
6,7	-	result[15:0]
5	-	result[15:1], result[1]
4	-	result[15:2], result[2], result[2]
3	-	result[15:3], result[3], result[3, result[3
2	-	result[15:4], result[4], result[4], result[4], result[4]
1	-	result[15:5], result[5], result[5], result[5], result[5], result[5]
0	1	result[15:5], result[5], result[5], result[5], result[5], result[5]
0	0	result[15:6], result[6], result[6], result[6], result[6], result[6], result[6]

28.3 Programming

There is a simple sequence of steps that needs to be followed to program and use the GPADC:

1. Enable the GPADC by setting the GP_ADC_CTRL_REG[GP_ADC_EN] bit.
2. Set up the GPIO input (Px_yy_MODE_REG[PID] = 34).

   Note that there are four dedicated pins that can be used with GP-ADC (P0_05, P0_06, P0_27, and P0_30).

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3. Select the input channel (GP_ADC_SEL_REG).
4. Select the sampling mode (differential or single-ended) by writing the GP_ADC_CTRL_REG[GP_ADC_SE] bit.
5. Select between the manual mode and the continuous mode of sampling (GP_ADC_CTRL_REG[GP_ADC_CONT].
6. Set up extra options (see GP_ADC_CTRLx_REG description).
7. Start the conversion by setting GP_ADC_CTRL_REG[GP_ADC_START] bit.
8. Wait for GP_ADC_CTRL_REG[GP_ADC_START] to become 0 or interrupt being triggered (when used).
9. Clear the ADC interrupt by writing any value to GP_ADC_CLEAR_INT_REG.
10. Get the ADC result from the GP_ADC_RESULT_REG.

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29 Application ADC

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

29.1 Introduction

The DA1470x is equipped with a low-power ADC for voice/audio applications which deliver 11 effective number of bits (ENOB) at a rate of 16 ksamples/s.

In front of the Application ADC, there is a Programmable Gain Amplifier to adjust the input level of an analog microphone to the ADC input range. The microphone is AC coupled to the differential input PGA. In case the analog microphone has a single-ended output, the ground terminal can be connected to one of the inputs.

Features

- 11 bits resolution at 16 ksamples/s
- One differential channel
- Programmable Gain Amplifier in differential mode only

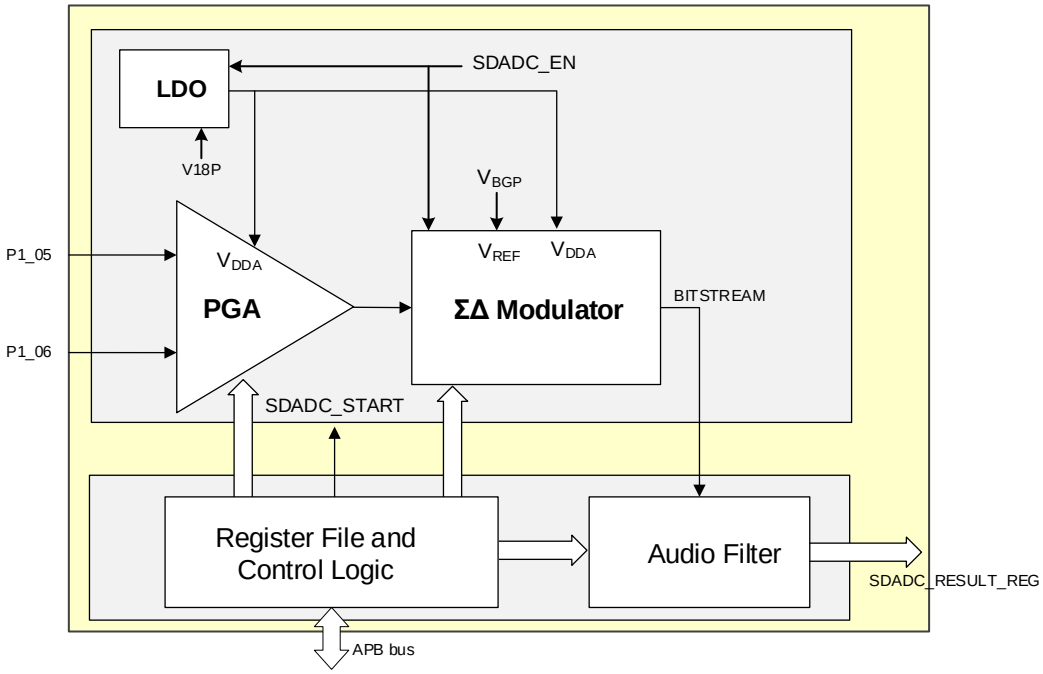

Figure 65: Application ADC Block Diagram

29.2 Architecture

The App ADC comprises an analog part including a ΣΔ-Modulator and auxiliary circuitry, control logic, and a digital part containing a sinc4 digital decimation filter delivering 16 ksps. The audio mode filter and the data path are presented in Figure 66.

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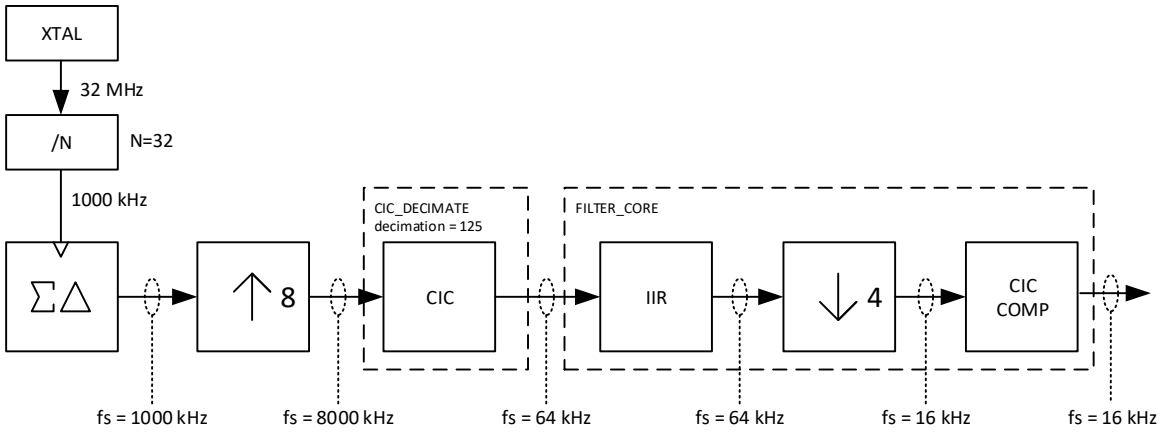

Figure 66: Audio Mode Data Path

This filter delivers a 16-bits word with a 16 kHz rate.

Note
Out of the 16-bits, the ENOB is 11 hence the 5 LSBs are considered to be noise and should be discarded.

The output of the filter is driven to the result register of the App ADC block where it can be read by the CPU or a DMA engine. In parallel, it is connected to the APU block in the SRC input, for sampling conversion directly without the need for a CPU.

29.3 Programming

There is a simple sequence of steps that needs to be followed to program and use the ΣΔ AD Converter:

1. Enable the SDADC block (SDADC_CTRL_REG[SDAC_EN]=1).
2. Enable the interrupts by setting SDADC_CTRL_REG[SDAC_MINT]=1.
3. Configure the PGA block by writing the SDADC_PGA_CTRL_REG.
4. Enable the PGA block by setting SDADC_PGA_CTRL_REG[PGA_EN]=1.
5. Enable the SDADC audio filter (SDADC_CTRL_REG[SDADC_AUDIO_FILTER_EN] =1).
6. Start the conversion by SDADC_CTRL_REG[SDAC_START]=1.
7. Get the ADC result from the SDADC_RESULT_REG when an interrupt is triggered.
8. To stop the conversion:
   a. Stop SDADC sampling by disabling audio filter (SDADC_CTRL_REG[SDADC_AUDIO_FILTER_EN] =0).
   b. Wait until the SDADC_CTRL_REG[SDADC_START] bit becomes a zero.

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30 Audio Unit (AU)

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

30.1 Introduction

The Audio Unit features two digital interfaces, namely a PDM and PCM. It also comprises two Sampling Rate Converter (SRC) units, which are used for adjusting the sampling rate of audio streams between the two interfaces and memory. Two SRC units are used for processing two audio signals simultaneously for parallel listening and playing.

The PDM interface provides a serial connection for one stereo or two mono input devices (for example, MEMS microphones) or digital output devices. The interface has a single clock PDM_CLK and one input/output PDM_DI/PDM_DO that can carry two channels in a time-divided manner.

The PCM controller implements up to 192 kHz synchronous interface to external audio devices, ISDN circuits, and serial data interfaces. It enables master and slave modes and supports I2S and TDM formats.

The Audio Unit is supported by the system DMA controller with configurable channels for the PCM and PDM streams. The PCM data flow utilizes an internal dedicated 8x32-bit FIFO that cannot be used in stereo mode.

Features

- Two Sampling Rate Conversion (SRC) Units for parallel (listening and playing) audio streams
- Supported conversions:
  - SRC_IN (32 bits) to SRC_OUT (32 bits)
  - PDM_IN (1bit) to SRC_OUT (32 bits)
  - SRC_IN (32 bits) to PDM_OUT (1 bit)
- SRC_IN, SRC_OUT Sample rates 8 kHz to 192 kHz
- SNR > 100 dB
- Single Buffer I/O with the use of system DMA controller
- Automatic mode to adjust sample rate to the applied frame sync (for example, PCM_FSC)
- Manual mode to generate interrupts at the programmed sample rate. Adjustment is done by SW based on buffer pointers
- PCM (Master/Slave) interface
  - PCM_FSC
    - Master/slave 4 kHz to 48 kHz
    - Strobe Length 1, 8, 16, 24, 32, 40, 48, and 64 bits
    - PCM_FSC before or on the first bit (In Master mode)
  - 2x32bits channels
  - Programmable slot delay up to 31*8 bits
  - Formats
    - PCM mode
    - I2S mode (Left/Right channel selection) with N*8 for Left and N*8 for Right
  - Programmable clock and frame sync inversion
- PDM interface
  - PDM_CLK frequency 62.5 kHz -- 4 MHz
  - Down-sampling to 32 bits in SRC
  - PDM_CLK on/off to support Sleep mode

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- PDM_DATA
  - Input: 1 Channel in stereo format
  - Output: 2 Channels in mono format, 1 Channel in stereo format
- Programmable Left/Right channel selection

- Direct connection to the ΣΔADC output for down/up conversion without DMA

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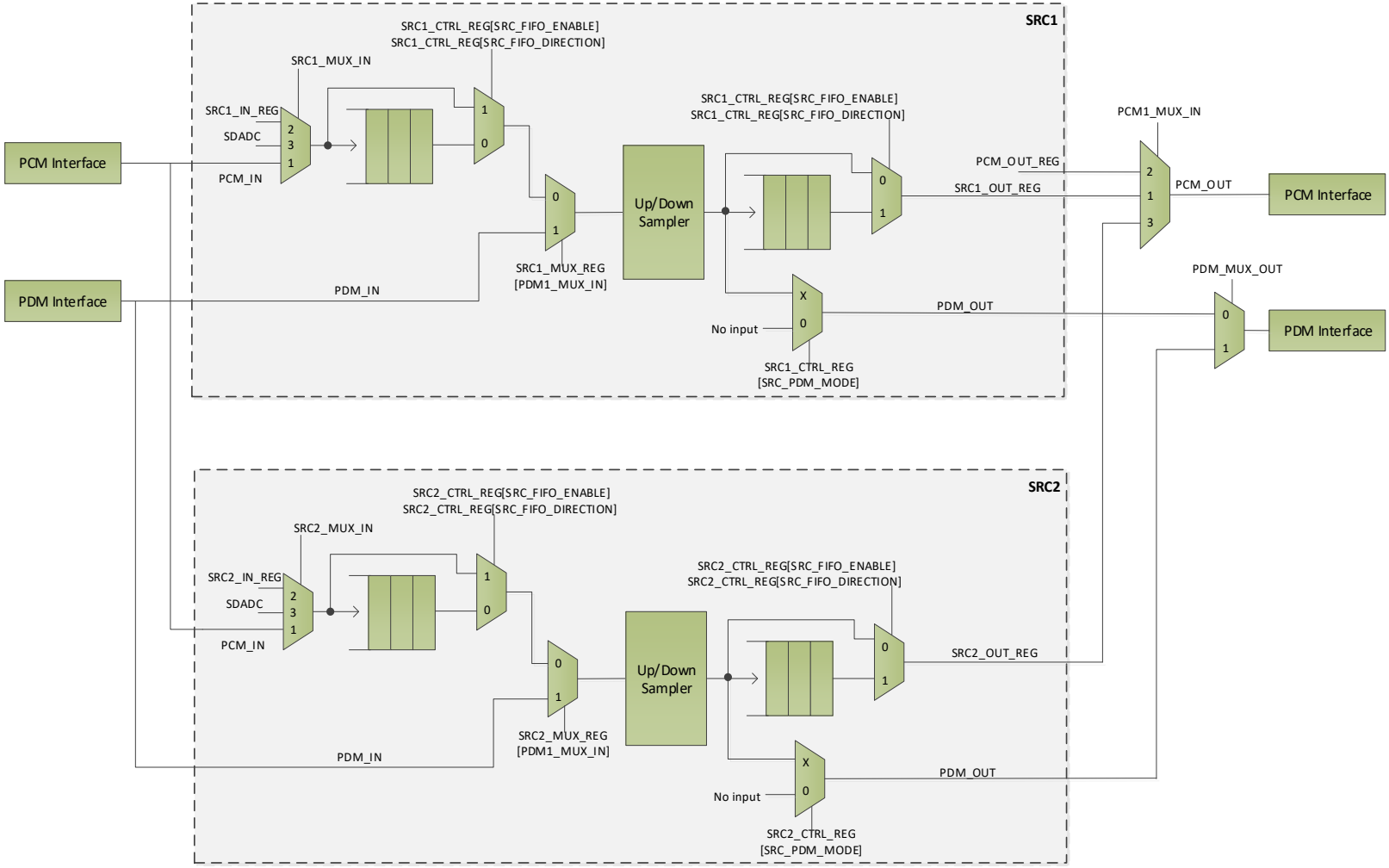

Figure 67: Audio Unit Block Diagram

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30.2 Architecture

30.2.1 Data Paths

The SRC block converts two 32-bit channels into, either a stereo pair or two mono streams. PCM linear data pairs are transferred to SRC1_IN1/2; the output is 2x32-bit left-aligned on SRC1_OUT1/2. The two 1-bit PDM data inputs are received on PDM_IN and are converted to 2x32 bits, left-aligned to SRC_OUT.

The SRCx_IN input multiplexer (Figure 38) is controlled by SRCx_MUX_REG[SRCx_MUX_IN]. The input of these multiplexers comes from the audio interfaces, the SRC1_IN1/2_REG, or the ΣΔ ADC output register. The data to these registers is left-aligned, bits 31-8 are mapped on bits 23-0 of the SRC.

The 32 bits SRC outputs can be read in SRCx_OUT1_REG and SRCx_OUT2_REG and can also be routed to the PCM interface. The input selection of this multiplexer is also controlled by SRC1_MUX_REG[PCM1_MUX_IN].

An 8x32-bit FIFO can be connected to the SRC input or output data path when not in stereo mode. When the FIFO services the SRC input data path, an SRC input event triggers a FIFO write, while a CPU read access triggers a FIFO read. SRC_IN_IRQ / SRC2_IN_IRQ are issued when the FIFO level increments to four samples. When the FIFO services the SRC output data path, an SRC output event triggers a FIFO read, while a CPU write access triggers a FIFO write. SRC_OUT_IRQ/SRC2_OUT_IRQ are issued when the FIFO level drops below five samples. FIFO operation can be completely disabled.

The SRC can be configured to operate in two different modes of operation:

- Manual mode
- Automatic mode

In **manual mode,** the input/output sampling rate is determined by SRCx_IN_FS_REG/SRCx_OUT_FS_REG registers.

In **automatic mode**, the input/output sampling rate is automatically derived from the external synchronization signals and can only be read back at SRCx_IN_FS_REG/SRCx_OUT_FS_REG registers.

When PDM is used (input/output), SRC operates in automatic mode. The sampling rate reported in SRCx_IN_FS_REG registers is PDM_CLK/64, 64 being the default oversampling ratio.
An overview of all possible data paths for both inbound as well as outbound audio streams is illustrated in Figure 68.

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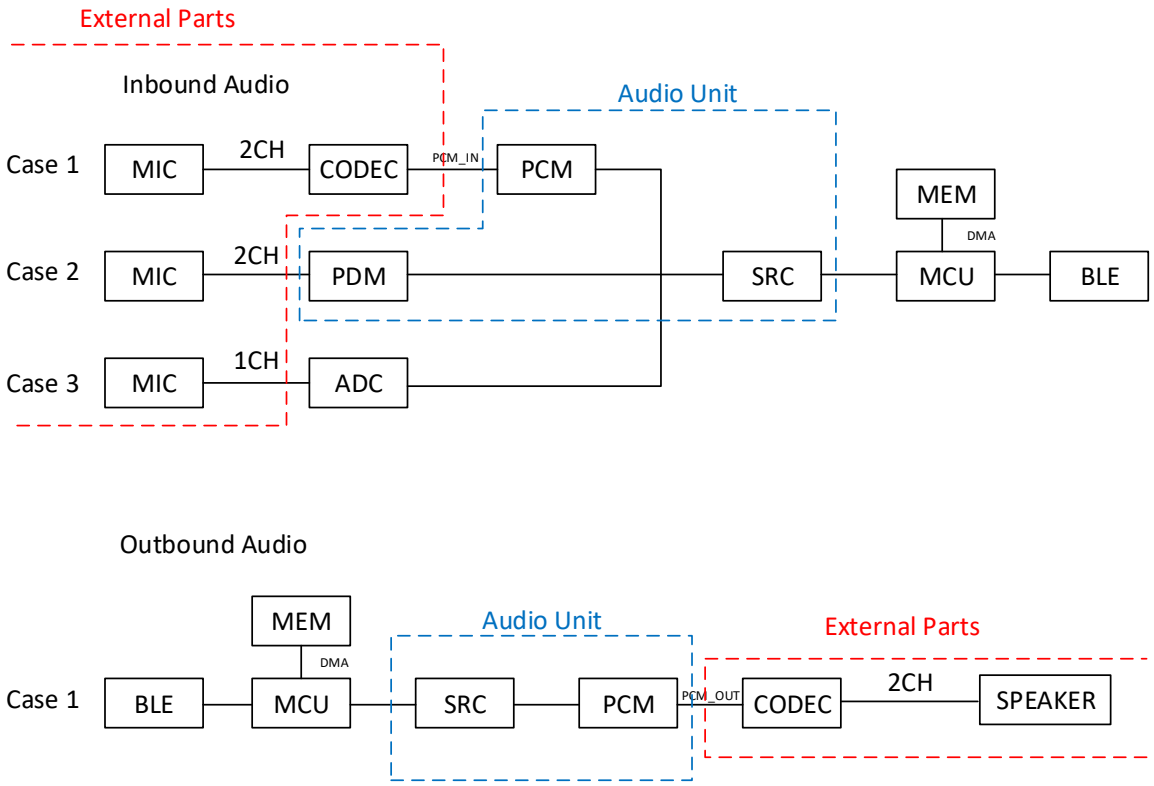

Figure 68: Inbound and Outbound Audio Streams Data Paths

30.2.2 Up/Down Sampler

The Up/Down Sampler (Figure 38) performs the required arbitrary resampling by polynomial interpolation at an 8x oversampled input rate and 16x oversampled output rate.

For maximum flexibility, a generic single-cycle multiplier facilitates variable coefficient multiplications. The multiplier is combined with optional pre- and post-adders into an arithmetic unit.

30.2.3 PCM Interface

30.2.3.1 Channel Access and Delay

The PCM interface has two 32-bit registers for TX and RX, namely PCM1_IN1/OUT1_REG and PCM2_IN1/OUT2_REG for input and output directions respectively. These registers can be arranged as two channels of 32 bits each, four channels of 16 bits each, or eight channels of 8 bits each, named channel 1 to channel 8. By a configurable clock inversion, channel delay, and strobe length adjustment, various formats like PCM, I2S, and TDM can be supported.

The 8 PCM channels can be delayed with a maximum delay of 31x8 bits by configuring PCM1_CTRL_REG[PCM_CH_DEL]. Note that a high delay count in combination with a slow clock can lead to the PCM_FSC sync occurring before all channels are shifted in or out. The received bits of the current channel may not be properly aligned in that case. Furthermore, the SRC blocks only support two channels.

30.2.3.2 Clock Generation

The PCM clock (PCM_CLK) must be generated according to the required sample rate. There are two ways of generating the clock:

- **The Fractional Option**. Dividing the system clock by an integer and a fractional part (inserting jitter in the clock pulse train). This is programmed in the PCM_DIV_REG and PCM_FDIV_REG respectively

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- **The Integer Only option**. Approximate the sample rate by adding more clock pulses than bits required. These extra pulses are ignored. This approach is used when external slave devices cannot tolerate the inserted jitter on the clock line. It is configured in PCM_DIV_REG

The PCM_DIV_REG[PCM_DIV] is a 12-bits field that holds the integer part of the desired clock divider. The fractional part of the divider is stored in the 16 bits PCM_FDIV_REG register. The value of the register is calculated in the following way:

- The position of the leftmost 1 of the value in binary format defines the denominator
- The amount of 1s defines the numerator of the fraction as explained in the example of Table 174.

Table 174: PCM_FDIV_REG Programming Example

PCM_FDIV_REG (Hex)	PCM_FDIV_REG (Binary)	Numerator	Denominator	Fraction
0x0110	0b100010000	2	9	2/9
0x0101	0b100000001	2	9	2/9
0x1ABC	0b1101010111100	8	13	8/13
0xBEEF	0b1011111011101111	13	16	13/16
0xFEEE	0b1111111011101110	13	16	13/16

The FSC pulse is generated from the PCM_CLK by further dividing it by PCM_FSC_DIV.

Both clock generation options are explained in Table 175, with 8 bits, 16 bits, 32 bits, and 48 bits in various sample rates.

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Table 175: Fractional and Integer Only Clock Divisors for Various PCM Frequencies and Sample Rates

				XTAL (kHz) 32000					PLL (kHz) 160000					RCHS (kHz) 96000					RCHS (kHz) 64000				
					Fractional		Integer Only			Fractional		Integer Only			Fractional		Integer Only			Fractional		Integer Only	
Sample Rate (kHz)	Channel	Bits	Desired Bit Clock (KHz)	Desired Divider	PCM_DIV_REG	PCM_FDIV_REG	PCM_DIV_REG	Actual Word size (Bits)	Desired Divider	PCM_DIV_REG	PCM_FDIV_REG	PCM_DIV_REG	Actual Word size (Bits)	Desired Divider	PCM_DIV_REG	PCM_FDIV_REG	PCM_DIV_REG	Actual Word size (Bits)	Desired Divider	PCM_DIV_REG	PCM_FDIV_REG	PCM_DIV_REG	Actual Word size (Bits)
8	1	8	64	500	500		500	8	2500	2500		2500	8	1500	1500		1500	8	1000	1000		1000	8
8	1	16	128	250	250		250	16	1250	1250		1250	16	750	750		750	16	500	500		500	16
8	1	24	192	166,667	166	2/3	160	25	833,333	833	1/3	800	25	500	500		500	24	333.3	333	1/3	320	25
8	1	32	256	125	125		125	32	625	625		625	32	375	375		375	32	250	250		250	32
8	2	8	128	250	250		250	8	1250	1250		1250	8	750	750		750	8	500	500		500	8
8	2	16	256	125	125		125	16	625	625		625	16	375	375		375	16	250	250		250	16
8	2	24	384	83,333	83	1/3	80	25	416,667	416	2/3	400	25	250	250		250	24	166.6	166	2/3	160	25
8	2	32	512	62,5	62	1/2	50	40	312,5	312	1/2	250	40	187,5	187	1/2	150	40	125	125		125	32
16	1	8	128	250	250		250	8	1250	1250		1250	8	750	750		750	8	500	500		500	8
16	1	16	256	125	125		125	16	625	625		625	16	375	375		375	16	250	250		250	16
16	1	24	384	83,333	83	1/3	80	25	416,667	416	2/3	400	25	250	250		250	24	166.6	166	2/3	160	25
16	1	32	512	62,5	62	1/2	50	40	312,5	312	1/2	250	40	187,5	187	1/2	150	40	125	125		125	32
16	2	8	256	125	125		125	8	625	625		625	8	375	375		375	8	250	250		250	8
16	2	16	512	62,5	62	1/2	50	20	312,5	312	1/2	250	20	187,5	187	1/2	150	20	125	125		125	16
16	2	24	768	41,667	41	2/3	40	25	208,333	208	1/3	200	25	125	125		125	24	83.3	83	1/3	80	25
16	2	32	1024	31,25	31	1/4	25	40	156,25	156	1/4	125	40	93,75	93	3/4	75	40	62.5	62	1/2	50	40
32	1	8	256	125	125		125	8	625	625		625	8	375	375		375	8	250	250		250	8
32	1	16	512	62,5	62	1/2	50	20	312,5	312	1/2	250	20	187,5	187	1/2	150	20	125	125		125	16

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				XTAL (kHz) 32000					PLL (kHz) 160000					RCHS (kHz) 96000					RCHS (kHz) 64000				
					Fractional		Integer Only			Fractional		Integer Only			Fractional		Integer Only			Fractional		Integer Only	
32	1	24	768	41,667	41	2/3	40	25	208,333	208	1/3	200	25	125	125		125	24	83.3	83	1/3	80	25
32	1	32	1024	31,25	31	1/4	25	40	156,25	156	1/4	125	40	93,75	93	3/4	75	40	62.5	62	1/2	50	40
32	2	8	512	62,5	62	1/2	50	10	312,5	312	1/2	250	10	187,5	187	1/2	150	10	125	125		125	8
32	2	16	1024	31,25	31	1/4	25	20	156,25	156	1/4	125	20	93,75	93	3/4	75	20	62.5	62	1/2	50	20
32	2	24	1536	20,833	20	5/6	20	25	104,167	104	1/6	100	25	62,5	62	1/2	50	30	41.6	41	2/3	40	25
32	2	32	2048	15,625	15	5/8	10	50	78,125	78	1/8	50	50	46,875	46	7/8	30	50	31.25	31	1/4	25	40
48	1	8	384	83,333	83	1/3	N/A	N/A	416,667	416	2/3	N/A	N/A	250	250		250	8	166.6	166	2/3	N/A	N/A
48	1	16	768	41,667	41	2/3	N/A	N/A	208,333	208	1/3	N/A	N/A	125	125		125	16	83.3	83	1/3	N/A	N/A
48	1	24	1152	27,778	27	7/9	N/A	N/A	138,889	138	8/9	N/A	N/A	83,33333333	83	1/3	80	25	55.5	55	5/9	N/A	N/A
48	1	32	1536	20,833	20	5/6	N/A	N/A	104,167	104	1/6	N/A	N/A	62,5	62	1/2	50	40	41.6	41	2/3	N/A	N/A
48	2	8	768	41,667	41	2/3	N/A	N/A	208,333	208	1/3	N/A	N/A	125	125		125	8	83.3	83	1/3	N/A	N/A
48	2	16	1536	20,833	20	5/6	N/A	N/A	104,167	104	1/6	N/A	N/A	62,5	62	1/2	50	20	41.6	41	2/3	N/A	N/A
48	2	24	2304	13,889	13	8/9	N/A	N/A	69,444	69	4/9	N/A	N/A	41,66666667	41	2/3	40	25	27.7	27	7/9	N/A	N/A
48	2	32	3072	10,417	10	2/5	N/A	N/A	52,083	52	1/12	N/A	N/A	31,25	31	1/4	25	40	20.8	20	5/6	N/A	N/A

The yellow marked fields designate that the actual word size achieved in the Integer Only option is larger than the required bits. The last clock pulses are ignored in this case. For example, to get 24 bits at an 8 kHz sampling rate, a clock of 192 kHz is required. In the Integer Only option, this is not possible. A higher clock will be generated (200 kHz), which results in a word of 25 bits. In this case, the last bit will be ignored. Note that the values in Table 175 are valid for the I2S and TDM without offset modes of operation.

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30.2.3.3 External Synchronization

With the PCM interface in Slave mode, the PCM interface supports direct routing through the sample rate converters (SRCs). Any drift in PCM_FSC or other frame sync frequencies like 44.1 kHz can be directly resampled to, for example, 48 kHz internal sample rate.

30.2.3.4 Data Formats

PCM Master Mode

Master mode is selected if PCM1_CTRL_REG[PCM_MASTER] = 1.

In Master mode, PCM_FSC is output and falls always over Channel 0. The duration of PCM_FSC is programmable with PCM1_CTRL_REG[PCM_FSCLEN] = 1 or 8,16, 24, 32 clock pulses high. The start position is programmable with PCM1_CTRL_REG[PCM_FSCDEL] and can be placed before or on the first bit of channel 0. The repetition frequency of PCM_FSC is programmable in PCM1_CTRL_REG[PCM_FSC_DIV] from 8 to 48 kHz.

If Master mode is selected, PCM_CLK is output and provides one or two clocks per data bit programmable in PCM1_CTRL_REG[PCM_CLK_BIT].

The polarity of the signal can be inverted with bit PCM1_CTRL_REG[PCM_CLKINV].

The PCM_CLK frequency selection is described in Section 30.2.3.2.

PCM Slave Mode

In Slave mode, (bit MASTER = 0) PCM_FSC is input and determines the starting point of channel 0. The repetition rate of PCM_FSC must be equal to PCM_SYNC and must be high for at least one PCM_CLK cycle. Within one frame, PCM_FSC must be low for at least PCM_CLK cycle. Bit PCM_FSCDEL sets the start position of PCM_FSC before or on the first bit (MSB).

In Slave mode, PCM_CLK is input. The minimum received frequency is 256 kHz, the maximum is 3.072 MHz.

In Slave mode, the main counter can be stopped and resumed on a PCM1_FSC or PCM2_FSC rising edge.

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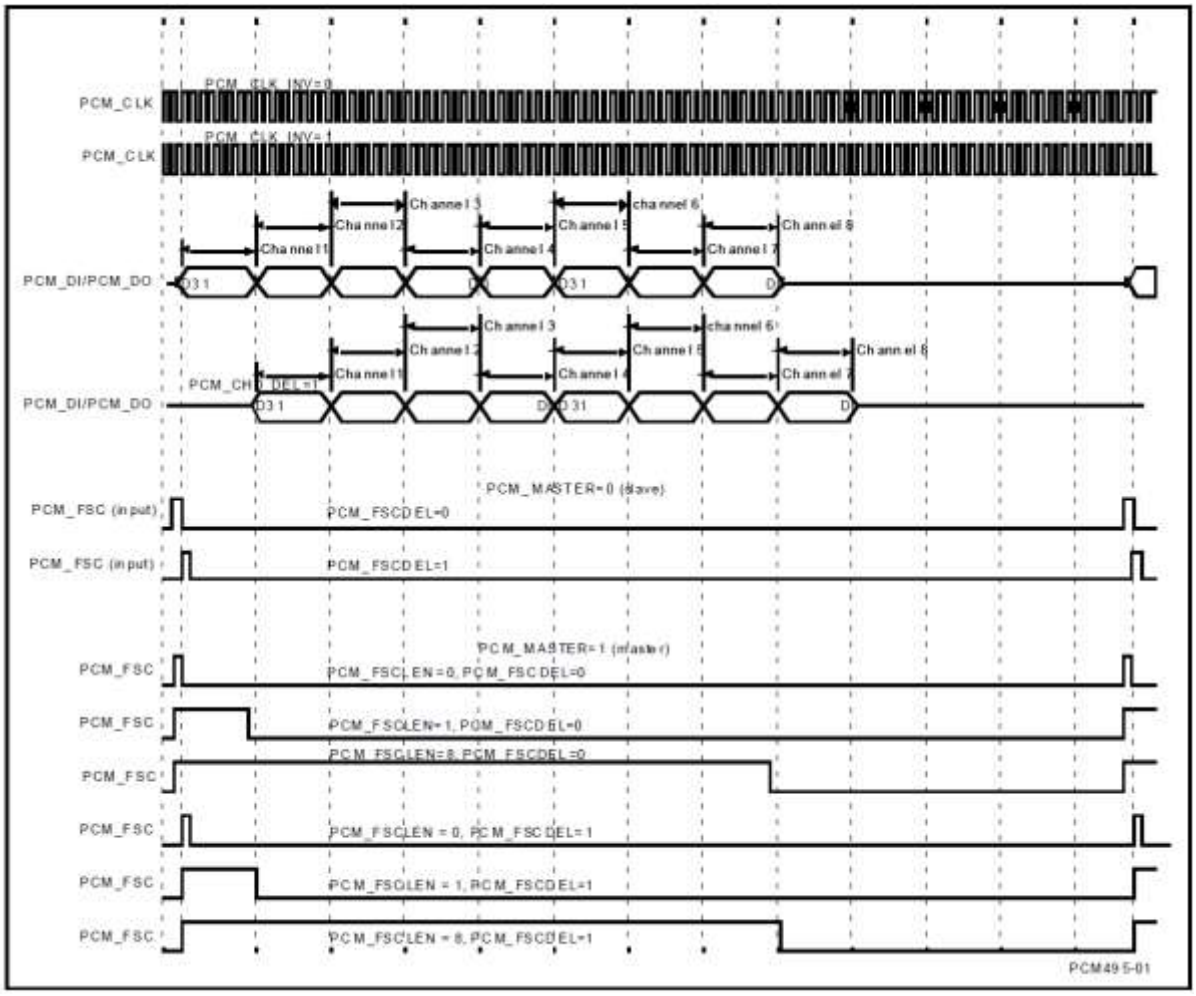

Figure 69: PCM Interface Formats

I2S Formats

The digital audio interface supports I2S mode, Left Justified mode, Right Justified mode, and TDM mode.

I2S mode

To support I2S mode, the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the PCM_FSC, and the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the PCM_FSC, as shown in Figure 70.

Settings for I2S mode:

- PCM_FSC_EDGE: 1 (all after PCM_FSC)
- PCM_FSCLEN: 4 (4x8 High, 4x8 Low)
- PCM_FSC_DEL: 0 (one bit delayed)
- PCM_CLK_INV: 1 (output on falling edge)
- PCM_CH_DEL: 0 (no channel delay)
- PCM_CLK_BIT: 0 (one clock cycle per data bit)

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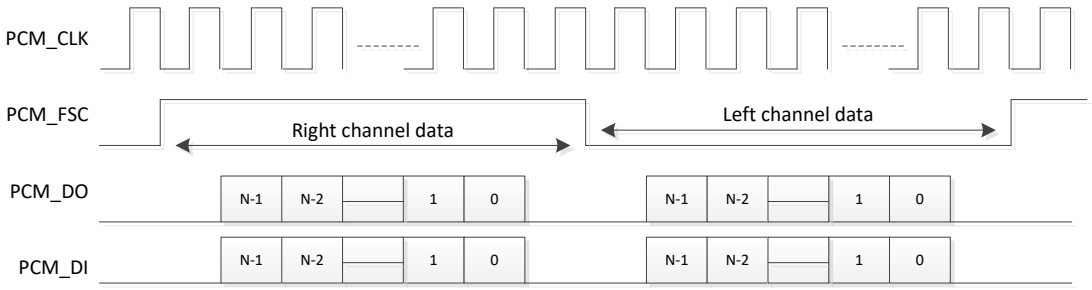

Figure 70: I2S Mode

TDM mode

A time is specified from the normal “start of frame” condition using register bits PCM_CH_DEL. In the left justified TDM example illustrated in Figure 71, the left channel data is valid PCM_CH_DEL clock cycles, after the rising edge of the PCM_FSC, and the right channel data is valid the same PCM_CH_DEL number of clock cycles after the falling edge of the PCM_FSC.

By delaying the channels, left and right alignment can also be achieved.

Settings for TDM mode:

- PCM_FSC_EDGE: 1 (rising and falling PCM_FSC)
- PCM_FSCLEN: Master 1 to 4
  Slave waiting for an edge.
- PCM_FSC_DEL: 1 (no bit delay)
- PCM_CLK_INV: 1 (output on falling edge)
- PCM_CH0_DEL: Slave 1-3 (8/16/24bits offset)
  Master 1-3

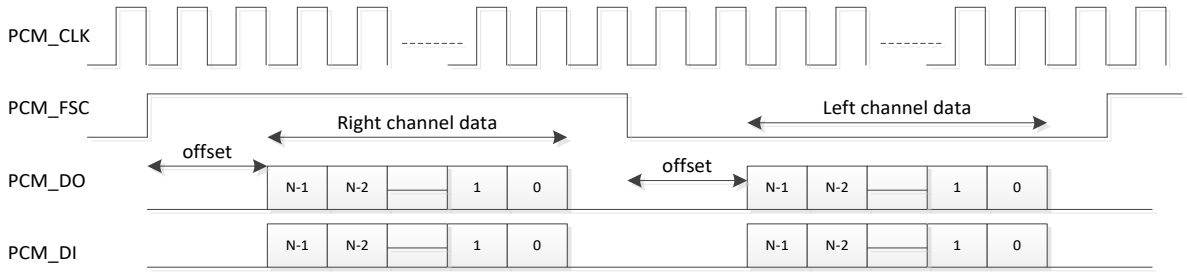

Figure 71: TDM Mode (Left Justified Mode)

Note that offset is always in multiples of eight.

30.2.4 PDM Interface

The PDM comprises two signals, namely the DATA, and the CLK, and supports stereo streams. PDM_DATA is encoded so that the left channel is clocked in on the falling edge of CLK and the right channel is clocked on the rising edge of PDM_CLK as shown in Figure 72.

The interface supports MEMS microphone sleep mode by disabling the PDM_CLK. The PDM interface signals can be mapped on any GPIO by programming PID = 32 and PID = 33 for DATA and CLK respectively in the Px_yz_MODE_REG.

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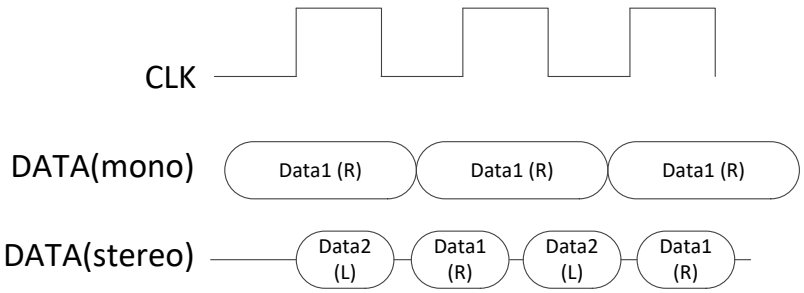

Figure 72: PDM Mono/Stereo Formats

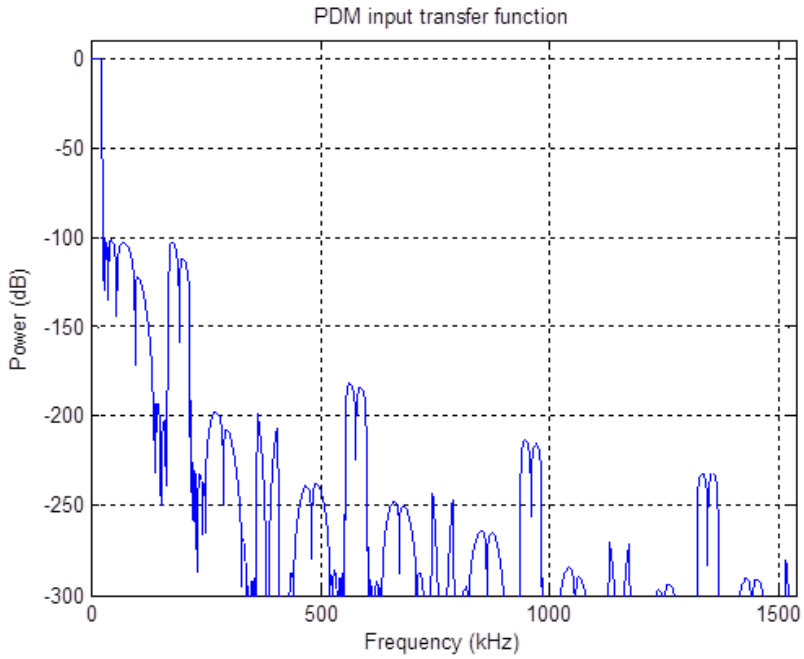

Figure 73: SRC PDM Input Transfer Function

Note that the audio quality degrades when the oversampling ratio is less than 64. For an 8 kHz sample rate, the minimum recommended PDM clock rate is 64 x 8 kHz = 512 kHz.

30.2.5 DMA Support

If more than one sample needs to be transferred to or from the CPU, or the sample rate is so high that it interrupts the CPU too often, the DMA controller must be engaged to perform the transactions. Three channels are reserved in the DMA to support the PCM, the SRC (IN), and the SRC (OUT) directions.

30.2.6 Interrupts

After a Sample Rate Conversion, the input up-sampler and output down-sampler, generate edge triggered interrupts on SRC_IN_SYNC and SRC_OUT_SYNC to the CPU which do not have to be cleared. Note that only one sample shall be read from or written to a single register at a time (there are no FIFOs included).

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30.3 Programming

There is a simple sequence of steps that needs to be followed to configure the Audio Unit:

1. Configure the GPIOs functionality used for the PDM and PCM I/F by writing the appropriate Px_yy_MODE_REG[PID] = 40,41 (PDM) and 36-39 (PCM).
2. Configure the GPIOs direction (Px_yy_MODE_REG[PUPD]).
3. Configure PDM I/F:
   a. Configure as Master by setting the PDM_DIV_REG[PDM_MASTER_MODE] bit.
   b. Set PDM clock divider (PDM_DIV_REG[PDM_DIV]).
   c. Enable PDM (internal) block clock (PDM_DIV_REG[CLK_PDM_EN]).
4. Configure PCM I/F:
   a. Select the clock source (PCM_DIV_REG[PCM_SRC_SEL]).
   b. Setup PCM clock division (PCM_DIV_REG[PCM_DIV], PCM_FDIV_REG).
   c. Enable the clock (master mode) by setting the PCM_DIV_REG[CLK_PCM_EN] bit.
   d. Disable PCM (PCM1_CTRL_REG[PCM_EN] = 0).
   e. Set PCM Framesync divider (PCM1_CTRL_REG[PCM_FSC_DIV]).
   f. (PCM1_CTRL_REG[PCM_FSC_EDGE]).
   g. Set channel delay in multiples of 8 bits (PCM1_CTRL_REG[PCM_CH_DEL]).
   h. Set the number of clock cycles per data bit (PCM1_CTRL_REG[PCM_CLK_BIT]).
   i. Set polarity of PCM FSC (PCM1_CTRL_REG[PCM_FSCINV]).
   j. Set polarity of PCM CLK(PCM1_CTRL_REG[PCM_CLKINV]).
   k. Set PCM DO output mode (PCM1_CTRL_REG[PCM_PPOD]).
   l. Set PCM FSC start time (PCM1_CTRL_REG[PCM_FSCDEL]).
   m. Set PCM FSC data length (PCM1_CTRL_REG[PCM_FSCLEN]).
   n. Set PCM in Master mode (PCM1_CTRL_REG[PCM_MASTER] = 1).
5. Configure the Sample Rate Converter:
   a. Set the SRC clock divider (SRC_DIV_REG[SRC_DIV]).
   b. Enable the SRC block clock by setting the SRC_DIV_REG[CLK_SRC_EN] bit.
   c. Select the SRC input Up Sampling IIR filters setting according to the sample rate (SRC1_CTRL_REG[SRC_IN_DS]).
   d. Configure the SRC input sample rate (SRC1_IN_FS_REG).
   e. Select the SRC output Up Sampling IIR filters setting according to the sample rate (SRC1_CTRL_REG[SRC_OUT_US]).
   f. Configure the SRC output sample rate (SRC1_OUT_FS_REG).
   g. Select the PDM as input to SRC (APU_MUX_REG[PDM1_MUX_IN] = 1).
   h. Enable the SRC FIFO (SRC1_CTRL_REG[SRC_FIFO_ENABLE]) and set direction (SRC1_CTRL_REG[SRC_FIFO_DIRECTION] = 1). Note that in stereo mode, FIFO cannot be used.
   i. Select the output to PCM (APU_MUX_REG[PCM1_MUX_IN] = 1).
   j. Set APU_MUX_REG[SRC1_MUX_IN] = 0.
   k. Set SRC input to Automatic conversion mode (SRC1_CTRL_REG[SRC_IN_AMODE] = 1).
6. Enable SRC (SRC1_CTRL_REG[SRC_EN] = 1).
7. Enable PCM (PCM1_CTRL_REG[PCM_EN] = 1).

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31 VAD

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

31.1 Introduction

The VAD block implements a Voice Activity Detection (VAD) engine for ultra-low power applications. It allows the System on Chip (SoC) stay in sleep mode until enough audible energy has been sensed to trigger an interrupt assertion and consequently wake up the rest of the SoC. It is an adaptative solution that adapts itself to the background noise. The ratio between ambient noise and voice to be detected is adjustable.

It operates on a low-power 32 kHz input clock and will be connected to an analog microphone that resides externally to the SoC.

Features

- Programmable detection parameters enabling to optimize performances for different application requirements
- Low power operation

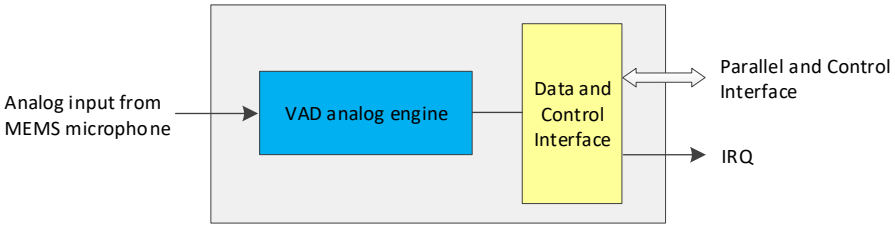

Figure 74: Block Diagram of the VAD and the Digital Control Unit

31.2 Architecture

31.2.1 Voice Detection Concept

The VAD system relies on the principle of energy-based detection. The block computes both the short-term energy (for voice signal) and the long-term energy (for ambient noise) in the voice bandwidth (from 100 Hz to 6 kHz). The detection of a voice event occurs when the relative power between the short-term energy and the long-term energy exceeds a programming threshold (Power Level Sensitivity) as shown in Figure 75.

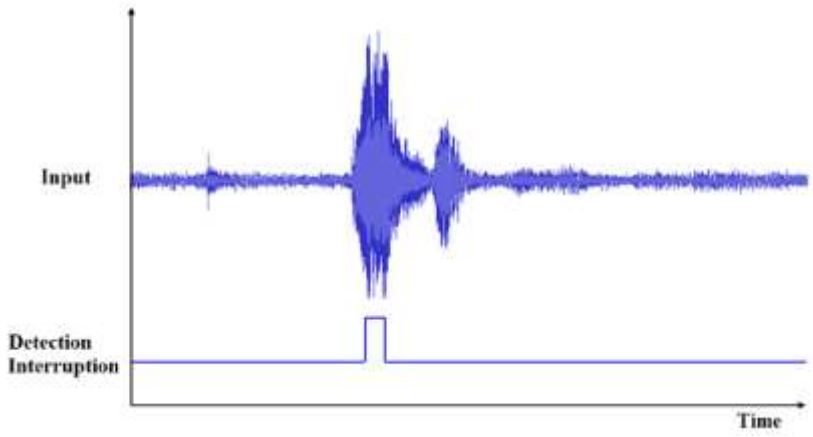

Figure 75: Voice Activity Detection Concept

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The frequency sensitivity of the long-term energy can be adjusted by setting the Background Noise Tracking parameter. The frequency sensitivity of the short-term energy can be adjusted by setting the Voice Tracking parameter.

These parameters allow to speed up or slow down the transient response of the energy computation, and thus increase or lower the frequency sensitivity.

The VAD functionality is dedicated to the power saving purpose for voice detection and voice recognition applications, enabling to wake up the recording path and the application processor.

31.2.2 System Integration

The VAD connects to an external analog microphone which must be constantly operating. The same microphone is also connected to the chip's PGA/AppADC which is powered off. As soon as the VAD senses audible energy that crosses the predefined threshold, it wakes up the CPU which in turn, enables the PGA/AppADC block to start fetching samples into RAM for further processing.

Connections between the VAD, the PGA, and the analog microphone are shown in Figure 76.

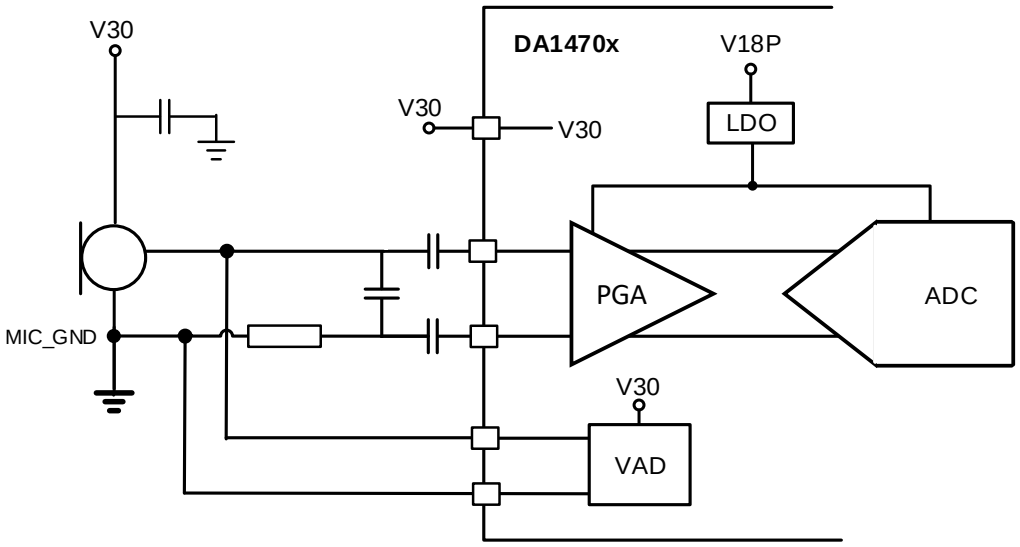

Figure 76: VAD/AMIC/PGA Connection

The VAD and analog microphone (AMIC) are supplied with 3 V by the V30 power rail of the chip. The PGA and the ADC are supplied with 1.8 V by the V18P rail of the chip. The PGA/AppADC supply is DC decoupled from the VAD/AMIC supply.

The VAD circuitry resides in the Sleep power domain (PD_SLP). It also requires VDD = 0.9 V so that the digital part of the VAD is running when the rest of the system is in sleep mode.

31.2.3 Operating Modes

The VAD block comprises three operating modes, as illustrated in Figure 77.

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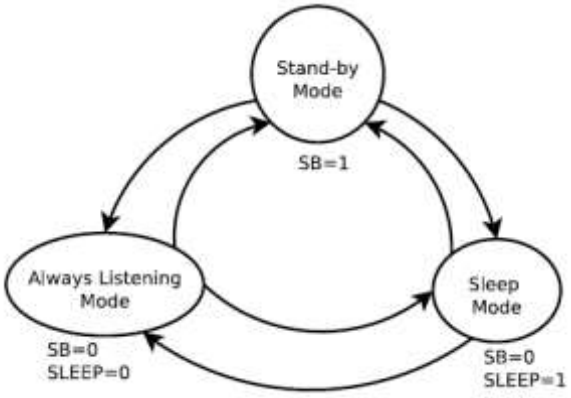

Figure 77: VAD Operating Modes

When in Stand-by-Mode, the VAD is turned off. No voice event can be detected. IRQ line is 0.

In Sleep mode, the analog part of the VAD block is powered on. No voice event can be detected while the IRQ line is still 0. This mode allows a fast transition to Always Listening mode. It is recommended to set the VAD in Sleep mode during the recording of AIP/AIN audio inputs on the PGA/ADC path.

When entering Always Listening mode, IRQ is set to 0. A voice event can be detected. When a voice event is detected, IRQ is set to 1. This interruption can be used to wake up a part of or all the system. IRQ output is synchronized on the internal clock rising edge. The minimum amount of time that this IRQ line is held high is 8 VAD clock cycles.

Note that the delay for the IRQ clearance mechanism depends on the input voice signal. To force the IRQ to 0 for cases of the false trigger, the Sleep mode of the VAD should be used.

31.3 Programming

There is a simple sequence of steps that needs to be followed to configure and enable the VAD block:

1. Deactivate the VAD block by setting VAD_CTRL3_REG[VAD_SB] = 1.
2. Select the clock of the VAD block by configuring CLK_CTRL_REG[VAD_CLK_SEL]. The XTAL32k is the recommended clock for the block.
3. Set the clock division VAD_CTRL3_REG[VAD_MCLK_DIV] = 1.
4. Configure the IRQ mode in VAD_CTRL4_REG[VAD_IRQ_MODE].
5. Optional configuration:
   a. Configure voice tracking, background noise tracking parameters, and power level sensitivity in the VAD_CTRL0_REG register if needed.
   b. Configure minimum delay and minimum event duration in the VAD_CTRL1_REG register if needed.
6. Enable the VAD block by configuring the mode to always listening, by setting VAD_CTRL3_REG[VAD_SB] = 0 and VAD_CTRL3_REG[VAD_SLEEP] = 0
7. After the VAD_IRQ assertion change the mode of the VAD to sleep by setting VAD_CTRL3_REG[VAD_SLEEP] = 1

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32 I2C Interface

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

32.1 Introduction

The I2C Interface is a programmable control bus that provides support for the communication link between Integrated Circuits in a system. It is a simple two-wire bus with a software-defined protocol for system control, which is used in temperature sensors and voltage level translators to EEPROMs, general-purpose I/O, A/D, and D/A converters. It comprises 32 levels deep buffers in both directions.

The DA1470x comprises three instances of the I2C Controller namely I2C, I2C2, and I2C3.

Features

- Two-wire I2C serial interface consists of a serial data line (SDA) and a serial clock (SCL)
- Three speeds are supported:
  - Standard mode (0 to 100 kbit/s)
  - Fast mode (<= 400 kbit/s)
  - High Speed mode (<= 3.4 Mbit/s)
- Clock synchronization
- 32 locations deep transmit/receive FIFOs (32 x 8-bit Rx, 32 x 10-bit Tx)
- Master transmit, Master receive operation
- 7-bit or 10-bit addressing
- 7-bit or 10-bit combined format transfers
- Bulk transmit mode
- Default slave address of 0x055
- Interrupt or polled-mode operation
- Handles Bit and Byte waiting at both bus speeds
- Programmable SDA hold time
- DMA support

32.2 Architecture

The I2C Controller block diagram is shown in Figure 78.

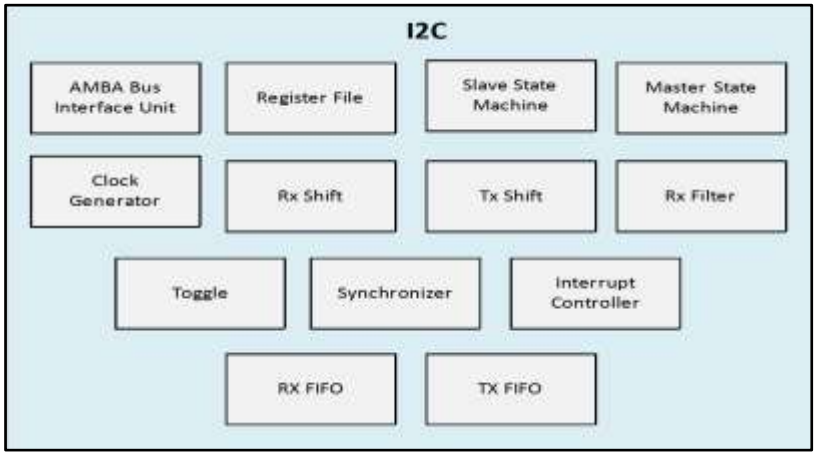

Figure 78: I2C Controller Block Diagram

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It contains the following subblocks:

- AMBA Bus Interface Unit. Interfacing via the APB-32 slow interface to access the register file
- Register File. Contains the configuration registers and is the software interface of the block
- Slave State Machine. Follows the I2C protocol for a slave device
- Master State Machine. Generates the I2C protocol for the master transfers
- Clock Generator. Calculates the required timing to do the following:
  - Generate the SCL clock when configured as a master
  - Check for bus idle
  - Generate a START and a STOP
  - Setup the data and hold the data
- Rx Shift. Takes data into the design and extracts it in byte format
- Tx Shift. Presents data supplied by CPU for transfer on the I2C bus
- Rx Filter. Detects the events in the bus; for example, start, stop and arbitration lost
- Toggle. Generates pulses on both sides and toggles to transfer signals across clock domains
- Synchronizer. Transfers signals from one clock domain to another
- Interrupt Controller. Generates the raw interrupt and interrupt flags, allowing them to be set and cleared
- RX FIFO/TX FIFO. Holds the RX FIFO and TX FIFO register banks and controllers, along with their status levels

32.2.1 I2C Behavior

The I2C can be controlled (through software) to be either an I2C master only, communicating with other I2C slaves, or an I2C slave only, communicating with one or more I2C masters.

The master is responsible for generating the clock and controlling the transfer of data. The slave is responsible for transmitting or receiving data to and from the master. Data acknowledgment is sent by the device that receives data, which can be master or slave. The I2C protocol allows multiple masters to reside on the I2C bus. It uses an arbitration procedure to determine bus ownership.

Each slave has a unique address that is determined by the system designer. When a master wants to communicate with a slave, the master transmits a START/RESTART condition that is then followed by the slave's address and a control bit (R/W) to determine if the master wants to transmit data or receive data from the slave. The slave then sends an acknowledge pulse (ACK) after the address.

If the master (master-transmitter) is writing to the slave (slave-receiver), the receiver gets one byte of data. This transaction continues until the master terminates the transmission with a STOP condition. If the master is reading from a slave (master-receiver), the slave transmits (slave-transmitter) a byte of data to the master, and the master then acknowledges the transaction with the ACK pulse. This transaction continues until the master terminates the transmission by not acknowledging (NACK) the transaction after the last byte is received, and then the master issues a STOP condition or addresses another slave after issuing a RESTART condition. This behavior is illustrated in Figure 79.

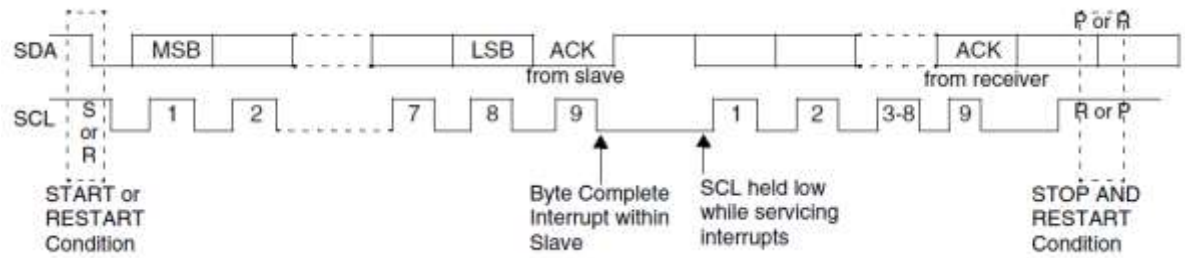

Figure 79: Data Transfer on the I2C Bus

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The I2C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain or open-collector to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400 pF. Data is transmitted in byte packages.

32.2.1.1 START and STOP Generation

When operating as an I2C master, putting data into the transmit FIFO causes the I2C Controller to generate a START condition on the I2C bus. Writing a “1” to I2C_DATA_CMD_REG[9] causes the I2C Controller to generate a STOP condition on the I2C bus; a STOP condition is not issued if this bit is not set, even if the transmit FIFO is empty.

When operating as a slave, the I2C Controller does not generate START and STOP conditions, as per the protocol. However, if a read request is made to the I2C Controller, it holds the SCL line low until read data has been supplied to it. This stalls the I2C bus until read data is provided to the slave I2C Controller, or the I2C Controller slave is disabled by writing a 0 to I2C_ENABLE.

32.2.1.2 Combined Formats

The I2C Controller supports mixed read and write combined format transactions in both 7-bit and 10-bit addressing modes.

The I2C Controller does not support mixed address and mixed address format – that is, a 7-bit address transaction followed by a 10-bit address transaction or vice versa – combined format transactions.

To initiate combined format transfers, I2C_CON.I2C_RESTART_EN should be set to 1. With this value set and operating as a master, when the I2C Controller completes an I2C transfer, it checks the transmit FIFO and executes the next transfer. If the direction of this transfer differs from the previous transfer, the combined format is used to issue the transfer. If the transmit FIFO is empty when the current I2C transfer completes, a STOP is issued, and the next transfer is issued following a START condition.

32.2.2 I2C Protocols

The I2C Controller has the following protocols:

- START and STOP Conditions
- Addressing Slave Protocol
- Transmitting and Receiving Protocol
- START BYTE Transfer Protocol

32.2.2.1 START and STOP Conditions

When the bus is idle, both the SCL and SDA signals are pulled high through external pull-up resistors on the bus. When the master wants to start transmission on the bus, the master issues a START condition. This is defined to be a high-to-low transition of the SDA signal while SCL is 1. When the master wants to terminate the transmission, the master issues a STOP condition. This is defined to be a low-to-high transition of the SDA line while SCL is 1. Figure 80 shows the timing of the START and STOP conditions. When data is being transmitted on the bus, the SDA line must be stable when SCL is 1.

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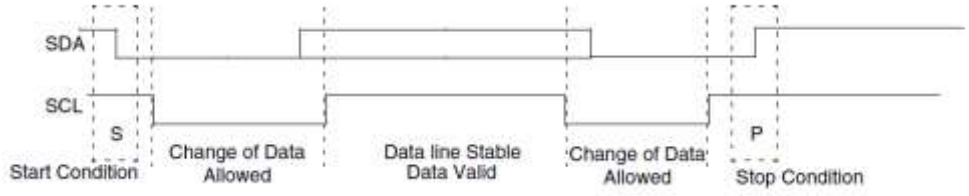

Figure 80: START and STOP Conditions

NOTE
The signal transitions for the START/STOP conditions, as depicted in Figure 80, reflect those observed at the output signals of the Master driving the I2C bus. Care should be taken when observing the SDA/SCL signals at the input signals of the Slave(s), because unequal line delays may result in an incorrect SDA/SCL timing relationship.

32.2.2.2 Addressing Slave Protocol

There are two address formats: 7-bit address format and 10-bit address format.

7-bit Address Format

During the 7-bit address format, the first seven bits (bits 7:1) of the first byte set the slave address and the LSB bit (bit 0) is the R/W bit as shown in Figure 81. When bit 0 (R/W) is set to 0, the master writes to the slave. When bit 0 (R/W) is set to 1, the master reads from the slave.

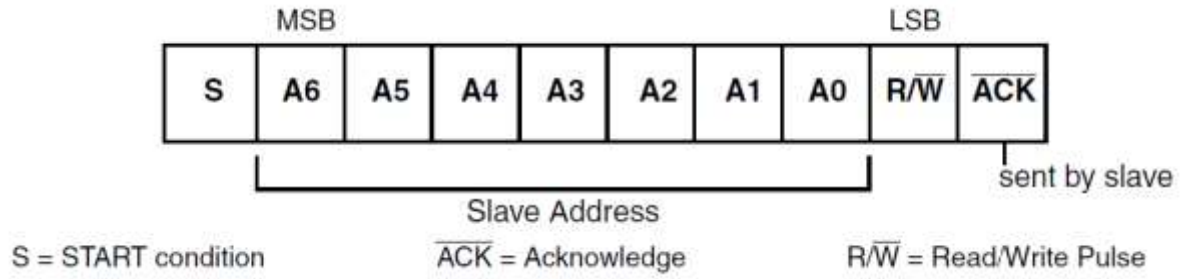

Figure 81: 7-bit Address Format

10-bit Address Format

During 10-bit addressing, two bytes are transferred to set the 10-bit address. The transfer of the first byte contains the following bit definition. The first five bits (bits 7:3) notify the slaves that this is a 10-bit transfer followed by the next two bits (bits 2:1), which set the slaves address bits 9:8, and the LSB bit (bit 0) is the R/W bit. The second byte transferred sets bits 7:0 of the slave address. Figure 82 shows the 10-bit address format, and Table 176 defines the special purpose and reserved first byte addresses.

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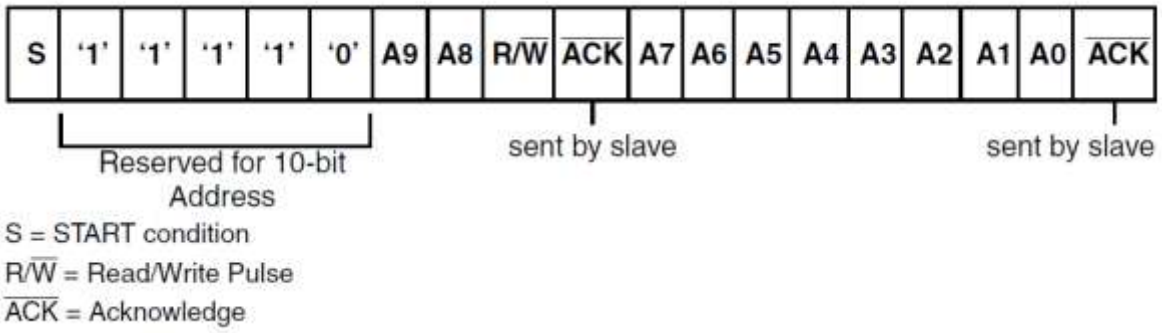

Figure 82: 10-bit Address Format

Table 176: I2C Definition of Bits in First Byte

Slave Address	R/W Bits	Description
0000 000	0	General Call Address. I2C Controller places the data in the receive buffer and issues a General Call interrupt
0000 000	1	START byte. For more details, refer to “START BYTE Transfer Protocol” 0000
0000 001	X	CBUS address. I2C Controller ignores these accesses
0000 010	X	Reserved
0000 011	X	Reserved
0000 1XX	X	High-speed master code (for more information, refer to “Multiple Master Arbitration”
1111 1XX	X	Reserved
1111 0XX	X	10-bit slave addressing

The I2C Controller does not restrict you from using these reserved addresses. However, if you use these reserved addresses, you may run into incompatibilities with other I2C components.

32.2.2.3 Transmitting and Receiving Protocols

The master can initiate data transmission and reception to/from the bus, acting as either a master-transmitter or master-receiver. A slave responds to requests from the master to either transmit data or receive data to/from the bus, acting as either a slave-transmitter or slave-receiver, respectively.

Master-Transmitter and Slave-Receiver

All data is transmitted in byte format, with no limit on the number of bytes transferred per data transfer. After the master sends the address and R/W bit or the master transmits a byte of data to the slave, the slave-receiver must respond with the acknowledge signal (ACK). When a slave-receiver does not respond with an ACK pulse, the master aborts the transfer by issuing a STOP condition. The slave must leave the SDA line high so that the master can abort the transfer.

If the master-transmitter is transmitting data as shown in Figure 83, then the slave-receiver responds to the master-transmitter with an acknowledge pulse after every byte of data is received.

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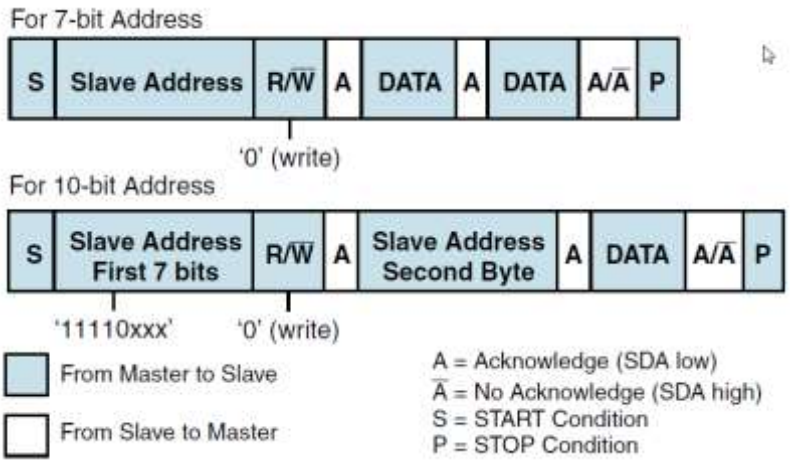

Figure 83: Master-Transmitter Protocol

Master-Receiver and Slave-Transmitter

If the master is receiving data as shown in Figure 84 then the master responds to the slave-transmitter with an acknowledge pulse after a byte of data has been received, except for the last byte. This is the way the master-receiver notifies the slave-transmitter that this is the last byte. The slave-transmitter relinquishes the SDA line after detecting the No Acknowledge (NACK) so that the master can issue a STOP condition.

When a master does not want to relinquish the bus with a STOP condition, the master can issue a RESTART condition. This is identical to a START condition except it occurs after the ACK pulse. The master can then communicate with the same slave or a different slave.

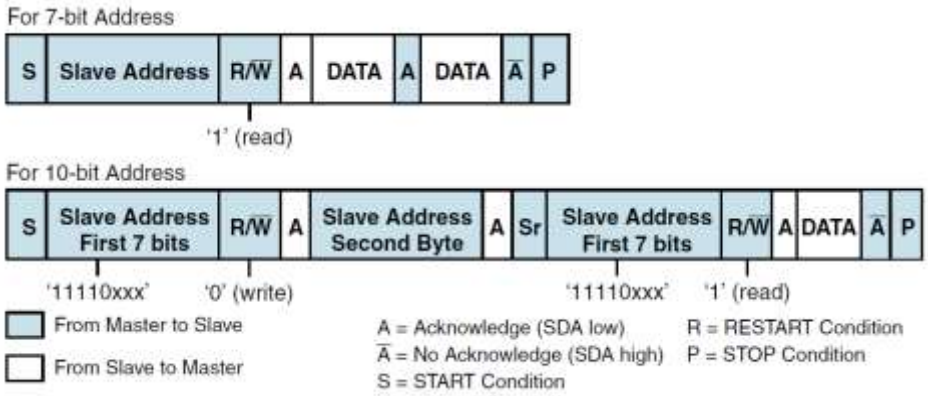

Figure 84: Master-Receiver Protocol

START BYTE Transfer Protocol

The START BYTE transfer protocol is set up for systems that do not have an onboard dedicated I2C hardware module. When the I2C Controller is addressed as a slave, it always samples the I2C bus at the highest speed supported so that it never requires a START BYTE transfer. However, when I2C Controller is a master, it supports the generation of START BYTE transfers at the beginning of every transfer in case a slave device requires it. This protocol consists of seven zeros being transmitted followed by a 1, as illustrated in Figure 85. This allows the processor that is polling the bus to under-sample the address phase until 0 is detected. Once the microcontroller detects a 0, it switches from the under-sampling rate to the correct rate of the master.

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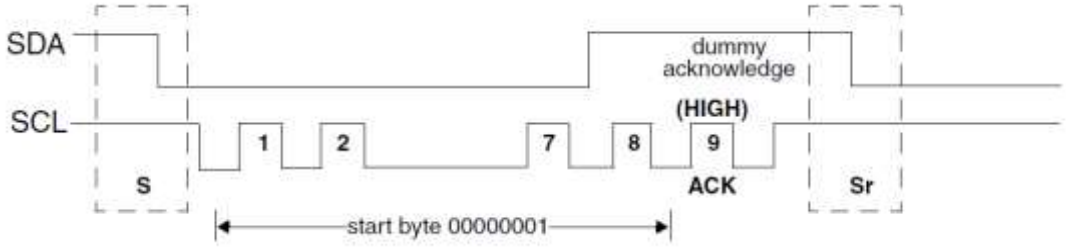

Figure 85: START BYTE Transfer

The START BYTE procedure is as follows:

1. Master generates a START condition.
2. Master transmits the START byte (0000 0001).
3. Master transmits the ACK clock pulse. (Present only to conform with the byte handling format used on the bus)
4. No slave sets the ACK signal to 0.
5. Master generates a RESTART (Sr) condition.

A hardware receiver does not respond to the START BYTE because it is a reserved address and resets after the RESTART condition is generated.

32.2.3 Multiple Master Arbitration

The I2C Controller bus protocol allows multiple masters to reside on the same bus. If there are two masters on the same I2C-bus, there is an arbitration procedure if both try to take control of the bus at the same time by generating a START condition at the same time. Once a master (for example, a microcontroller) has control of the bus, no other master can take control until the first master sends a STOP condition and places the bus in an idle state.

Arbitration takes place on the SDA line, while the SCL line is 1. The master, which transmits a 1 while the other master transmits 0, loses arbitration and turns off its data output stage. The master that lost arbitration can continue to generate clocks until the end of the byte transfer. If both masters are addressing the same slave device, the arbitration could go into the data phase. Figure 86 illustrates the timing of when two masters are arbitrating on the bus.

For high-speed mode, the arbitration cannot go into the data phase because each master is programmed with a unique high-speed master code. This 8-bit code is defined by the system designer and is set by writing to the High-Speed Master Mode Code Address Register, I2C_HS_MADDR. Because the codes are unique, only one master can win the arbitration, which occurs by the end of the transmission of the high-speed master code.

Control of the bus is determined by address or master code and data sent by competing masters, so there is no central master or any order of priority on the bus.

Arbitration is not allowed between the following conditions:

- A RESTART condition and a data bit
- A STOP condition and a data bit
- A RESTART condition and a STOP condition

Slaves are not involved in the arbitration process.

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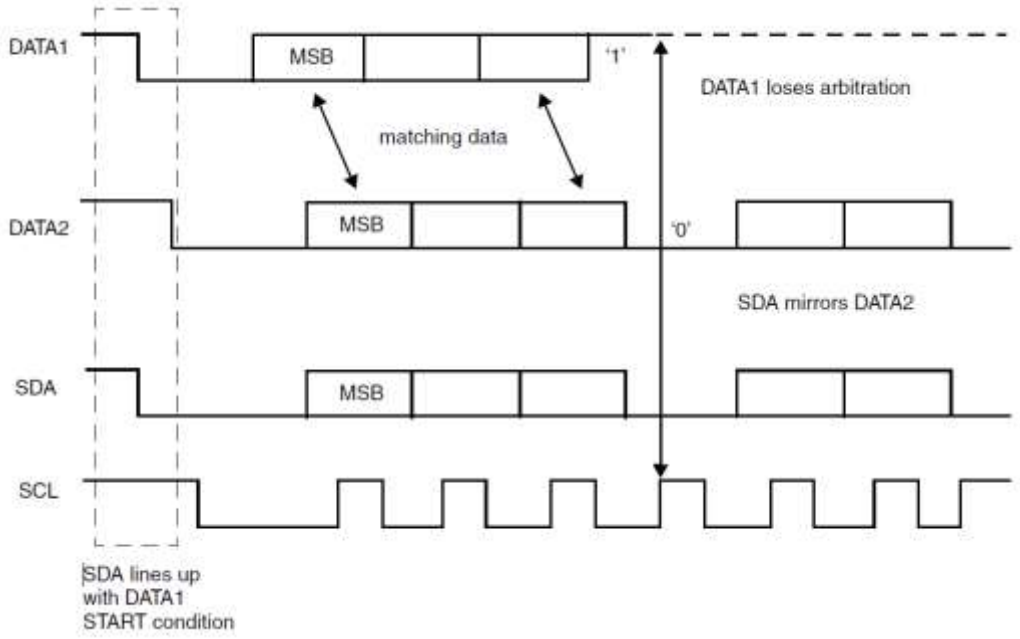

Figure 86: Multiple Master Arbitration

32.2.4 Clock Synchronization

When two or more masters try to transfer information on the bus at the same time, they must arbitrate and synchronize the SCL clock. All masters generate their own clock to transfer messages. Data is valid only during the high period of the SCL clock. Clock synchronization is performed using the wired-AND connection to the SCL signal. When the master transitions the SCL clock to 0, the master starts counting the low time of the SCL clock and transitions the SCL clock signal to 1 at the beginning of the next clock period. However, if another master is holding the SCL line to 0, then the master goes into a HIGH wait state until the SCL clock line transitions to 1.

All masters then count off their high time, and the master with the shortest high time transitions the SCL line to 0. The masters then count out their low time. The one with the longest low time forces the other master into a HIGH wait state. Therefore, a synchronized SCL clock is generated, which is illustrated in Figure 87. Optionally, slaves may hold the SCL line low to slow down the timing on the I2C bus.

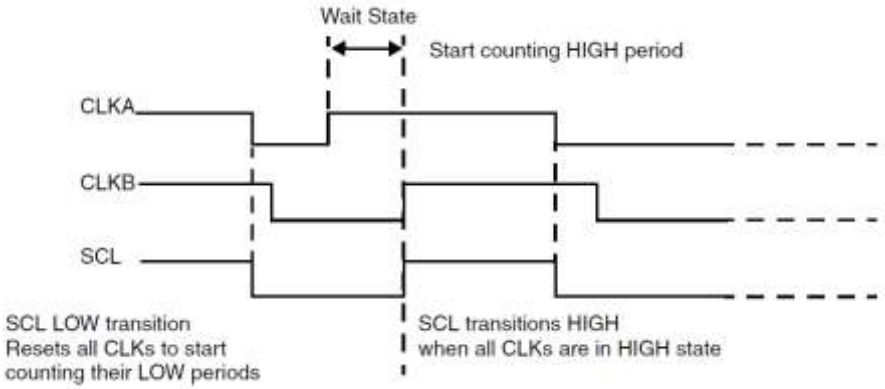

Figure 87: Multiple Master Clock Synchronization

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32.3 Programming

There is a simple sequence of steps that needs to be followed to configure and use the I2C Controllers:

1. Set up the GPIOs to be used for the I2C interface (Px_yy_MODE_REG[PID]).
2. Configure I2C clock frequency.
   For CLK_SNC_REG[I2Cx_CLK_SEL] = 0 (DivN clock):
   a. Standard mode (100 kbit/s): I2Cx_CON_REG[I2C_SPEED] = 1.
   b. Full speed mode (400 kbits/s): I2Cx_CON_REG[I2C_SPEED] = 2.
   c. High speed mode (1 Mbit/s): I2Cx_CON_REG[I2C_SPEED] = 3.
3. Set up the Controller as:
   a. Master: I2Cx_CON_REG[I2C_MASTER_MODE] = 1 and I2Cx_CON_REG[I2C_SLAVE_DISABLE] = 1.
   b. Slave: I2Cx_CON_REG[I2C_MASTER_MODE] = 0 and I2Cx_CON_REG[I2C_SLAVE_DISABLE] = 0.
4. Choose whether the controller starts its transfers in 7 or 10-bit addressing mode when acting as a master (I2Cx_CON_REG[I2C_10BITADDR_MASTER]) or when acting as a slave, whether the controller responds to 7- or 10-bit addresses (I2Cx_CON_REG[I2C_10BITADDR_SLAVE]).
5. Set target slave address in:
   a. Master mode (I2Cx_TAR_REG[IC_TAR] = 0x55 (default)).
   b. Slave mode (I2Cx_SAR_REG[IC_SAR] = 0x55 (default)).
6. Set threshold level on RX and TX FIFO (I2Cx_RX_TL_REG, I2Cx_TX_TL_REG).
7. Enable the required interrupts (I2Cx_INTR_MASK_REG).
8. Enable the I2C Controller by setting the I2Cx_ENABLE_REG[I2C_EN] bit.
9. Read a byte:
   a. Prepare to transmit the read command byte (I2Cx_DATA_CMD_REG[I2C_CMD] = 1).
   b. Wait until TX FIFO is empty (I2Cx_STATUS_REG[TFE] = 1).
   c. Wait until the master has finished reading the byte from the slave device (I2Cx_STATUS_REG[MST_ACTIVITY] = 0).
10. Write a byte:
    a. Prepare to transmit the write command byte (I2Cx_DATA_CMD_REG[I2C_CMD] = 0 and I2Cx_DATA_CMD_REG[I2C_DAT] = command byte).
    b. Wait until TX FIFO is empty (I2Cx_STATUS_REG[TFE] = 1).
    c. Wait until the master has finished reading the response byte from the slave device (I2Cx_STATUS_REG[MST_ACTIVITY] = 0).
11. Stop using and disable the controller:
    a. Define a timer interval (ti2c_poll) equal to the 10 times the signaling period for the highest I2C transfer speed used in the system. For example, if the highest I2C transfer mode is 400 kb/s, then this ti2c_poll is 25 µs.
    b. Define a maximum time-out parameter, MAX_T_POLL_COUNT, such that if any repeated polling operation exceeds this maximum value, an error is reported.
    c. Execute a blocking thread/process/function that prevents any further I2C master transactions to be started by software but allows any pending transfers to be completed (poll I2C_ENABLE_STATUS_REG).
    d. The variable POLL_COUNT is initialized to zero.
    e. Set bit 0 of the I2C_ENABLE_REG register to 0.
    f. Read the IC_ENABLE_STATUS register and test the IC_EN bit (bit 0). Increment POLL_COUNT by one. If POLL_COUNT >= MAX_T_POLL_COUNT, exit with the relevant error code.

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g. If I2C_ENABLE_STATUS_REG[0] is 1, then sleep for ti2c_poll and proceed to the previous step. Otherwise, exit with a relevant success code.

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33 I3C Interface

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

33.1 Introduction

The I3C Interface is a programmable control bus that provides support for the communications link between Integrated Circuits in a system. It is a simple two-wire bus with a software-defined protocol for system control, which is used in temperature sensors and voltage level translators to EEPROMs, general-purpose I/O, A/D, and D/A converters. It comprises 32 levels deep buffers in both directions.

Features

- Two-wire I3C serial interface is backward compatible with I2C
- Maximum Speed 12.5 Mb/s
- Clock synchronization
- 32 locations deep transmit/receive FIFOs (32 x 32-bit Rx, 32 x 32-bit Tx)
- In-band interrupt (IBI) with slave address
- Master mode only
- SDR mode only
- DMA support (by using the general-purpose DMA engine)

33.2 Architecture

The I3C Controller block diagram is shown in Figure 78.

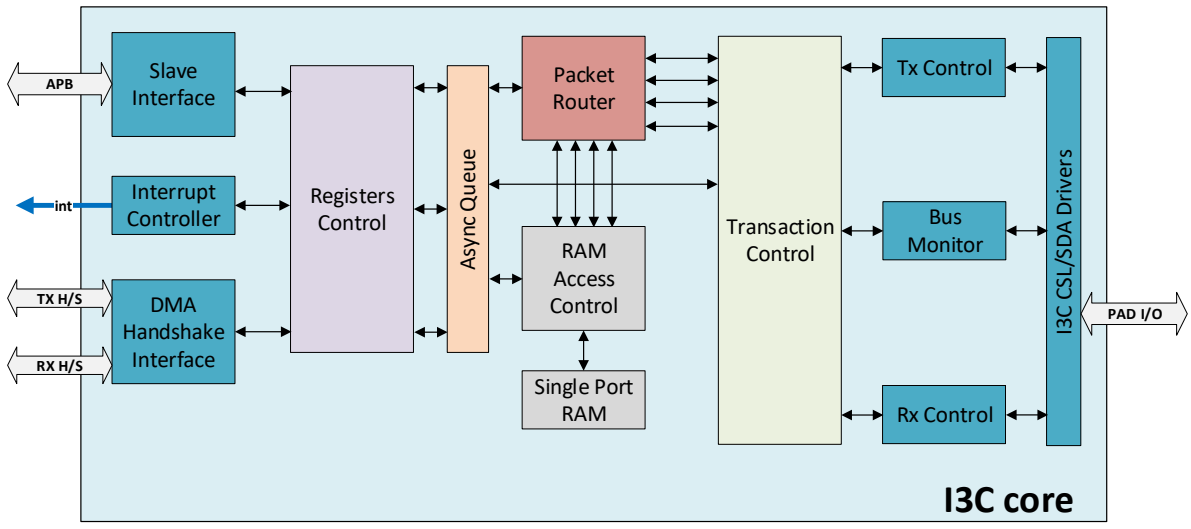

Figure 88: I3C Controller Block Diagram

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It contains the following subblocks:

Slave Interface Module

The Slave interface module converts the APB transactions to the generic register interface to interact with the register block.

Register Control Block Module

The Register Control block contains all the I3C registers. All registers in the block are 32-bit wide. The register interface in I3C is used to program the controller for different bus modes, timing parameters, and enabling/disabling of interrupts.

The register interface is also used for the transmission of command and Tx-data to the controller and reception of Rx-data, IBI-data, and response from the controller.

The Register Control block supports port registers, which are mapped to either FIFO's or Queue's present in the I3C controller.

Interrupt Controller Module

The Interrupt controller module enables the interrupts as a single pin. Interrupts are generated and cleared based on the Interrupt Register settings.

DMA Handshake Interface Module

The DMA handshake interface module is responsible for the assertion and de-assertion of the DMA handshake interface, based on the occupancy levels of Tx-FIFO and Rx-FIFO's. This interface is used for accessing the I3C block through the GP-DMA of the system.

Async Queue Block

The Async queue block consists of each asynchronous queue for the Data Buffers and Queues to maintain coherency between the Slave interface clock and core clock.

RAM Access Control

The RAM access control block performs an arbitration role for the data to be communicated between:

- Data Router and SPRAM
- APB interface and SPRAM

Packet Router Block

Packet router block performs the packing and unpacking of data between the transaction layer and the RAM access control block. Data that comes as separate bytes is packaged and written to the RAM access control that supports four-byte data. Similarly, data transmitted from RAM access control (four-byte data) is unpacked to separate bytes or words, as required by the transaction layer.

Transaction Control Module

The Transaction Control block is a state machine that controls both transmit and receive operations in the current Master mode of I3C. This module instructs the transmit and receive control blocks to operate based on commands from the application interface or in-band interrupt from the slaves.

Transmit Control and Receive Control Blocks

The Transmit Control and Receive Control blocks are used to control protocol-related transmit or receive signals (including timing signals) for Master and Slave, and for arbitration loss checks.

Bus Monitor

The Bus Monitor block is responsible to handle the following:

- IBI Start and HDR-TS Turnaround detection
- Bus-free (in Master mode)

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33.2.1 Bus Configuration

Three different bus configurations are supported by the Master I3C interface:

- Pure I3C bus: Configuration with only I3C devices present on the bus
- Mixed Fast Bus: Configuration with both I3C devices and Legacy I2C Slaves present on the bus. In this case, the legacy I2C Slaves are restricted to the ones that are generally permissible (that is Slave-only, no clock stretching, and that have a true I2C 50 ns glitch filter on SCL)
- Mixed Slow/Limited Bus: Configuration with both I3C devices and legacy I2C Slaves present on the bus. In this case, the legacy I2C Slaves are restricted to the ones that are selectively backward compatible with the I2C standard (that is, Slave-only and no clock stretching); but these do not have a true 50 ns glitch filter on SCL

In a Mixed bus configuration, the maximum possible data rate with I3C devices depends on the compliance of the I2C Slave as defined by the I2C Specification. The maximum data rate as specified in I3C Specification is possible only if all I2C slaves have the 50 ns spike filter on SCL.

In the absence of spike filters or if the presence of filter is unknown, the maximum data rate is limited to only FM or FM+, even for I3C devices (as per the I3C specification). I2C Slaves are not allowed to extend the clock.

33.3 Programming

There is a simple sequence of steps that needs to be followed to configure the I3C controller:

1. Set up the P1_11 and P1_12 GPIOs to be used for the I3C interface (P1_11_MODE_REG[PID] = 32 and P1_12_MODE_REG[PID] = 31).
2. Configure I3C clock frequency:
   a. Select the clock source (Div1 or DivN) for the I3C controller by setting the CLK_SNC_REG[I3C_CLK] register.
   b. Enable the input clock in the I3C controller by setting the CLK_SNC_REG[I3C_ENABLE] register.
3. Disable the I3C controller by setting I3C_DEVICE_CTRL_REG[ENABLE] = 0
4. Initialize the I3C controller in Master mode:
   a. Program the timing register depending on the speed of operation:
      i. For I3C operation the I3C_SCL_I3C_* registers should be configured. For maximum throughput in I3C mode (12.31Mbps) the PLL160M clock should be selected as Div1 (sys_clk) and the following values should be configured:
         - I3C_SCL_I3C_PP_TIMING_REG[I3C_PP_LCNT] = 6
         - I3C_SCL_I3C_PP_TIMING_REG[I3C_PP_HCNT] = 7
      ii. For I2C operation the I3C_SCL_I2C_* registers should be configured
   b. Configure the data buffer threshold controller register (I3C_DATA_BUFFER_THLD_CTRL_REG) and the queue threshold control register (I3C_QUEUE_THLD_CTRL_REG).
   c. Configure the acknowledge support for hot-join devices (I3C_DEVICE_CTRL_REG[HOT_JOIN_CTRL] and broadcast I3C address support (I3C_DEVICE_CTRL_REG[IBA_INCLUDE]) if needed.
   d. Enable the required fields for the interrupts by setting the I3C_INTR_SIGNAL_EN_REG and I3C_INTR_STATUS_EN_REG registers.
   e. Configure the device address table register based on the number of devices connected on the bus and set the slave static address and if it is a legacy I2C device or not in the I3C_DEV_ADDR_TABLE_LOC1_REG register.
5. Enable the I3C controller (I3C_DEVICE_CTRL_REG[ENABLE] = 1) and wait until the controller enters the idle state (I3C_PRESENT_STATE_REG[MASTER_IDLE] = 1).
6. **Read a byte:**

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a. Send the transfer argument (CMD_ATTR = 1) or short data argument (CMD_ATTR = 2) followed by the RnW bit set to zero for writing/addressing the internal slave's memory space (I3C_COMMAND_QUEUE_PORT_REG).
b. Send the transfer argument (CMD_ATTR = 1) by specifying the number of bytes to read from the slave device (I3C_COMMAND_QUEUE_PORT_REG).
c. Send the transfer command (CMD_ATTR = 0) with the RnW bit set to one for reading from the slave device (I3C_COMMAND_QUEUE_PORT_REG).
d. Polling the interrupt receive buffer to see if there is data in the RX FIFO of the I3C controller (I3C_INTR_STATUS_REG[RX_THLD_STS] = 1).
e. Read incoming data from the RX FIFO (I3C_RX_TX_DATA_PORT_REG)

7. **Write a byte:**
   a. For transfers with data payload, send the transfer argument (CMD_ATTR = 1) or short data argument (CMD_ATTR = 2) based on the number of bytes followed by the transfer command (CMD_ATTR = 0) with the RnW bit set to zero (I3C_COMMAND_QUEUE_PORT_REG).
   b. Wait for the transfer to compete by polling the response ready status bit (I3C_INTR_STATUS_REG[RESP_READY_STS] = 1).
   c. Read the response and check that is error-free (I3C_RESPONSE_QUEUE_PORT_REG).
   d. Wait for the controller to be in the IDLE state (I3C_PRESENT_STATE_REG[CM_TFR_ST_STS] = 0).

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34 UART

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

34.1 Introduction

The DA1470x contains three instances of this block: UART, UART2, and UART3.

The UART block is compliant to industry-standard 16550 and is used for serial communication with a peripheral. Data is written from a master (CPU) over the APB bus to the UART. It is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

There is also DMA support on the UART block, so the internal FIFOs can be used. UART2 and UART3 support hardware flow control signals (RTS, CTS).

Features

- Dedicated 16 bytes Transmit and 16 bytes Receive FIFO for each UART
- Hardware flow control and 9-bit mode support (CTS/RTS, UART2, and UART3)
- Shadow registers reduce software overhead and include a software programmable reset
- Transmitter Holding Register Empty (THRE) interrupt mode
- Functionality based on the 16550 industry standard:
  - Programmable character properties, such as the number of data bits per character (5-8)
  - Optional parity bit (with odd or even select) and number of stop bits (1, 1.5, or 2)
  - Line break generation and detection
  - Prioritized interrupt identification
- Programmable serial data baud rate as calculated by the following: baud rate = (serial clock frequency)/(16 x divisor) and the fractional part UART_DLF/16
- ISO7816 support (UART3)

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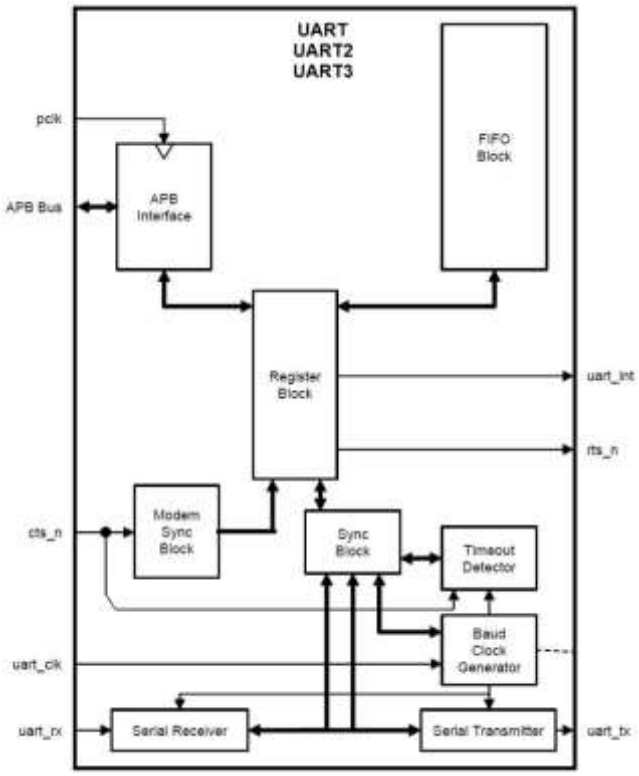

Figure 89: UART Block Diagram

34.2 Architecture

34.2.1 UART (RS232) Serial Protocol

Because the serial communication between the UART and the selected device is asynchronous, additional bits (start and stop) are added to the serial data to indicate the beginning and end. Utilizing these bits allows two devices to be synchronized. This structure of serial data accompanied by start and stop bits is referred to as a character, as shown in Figure 90.

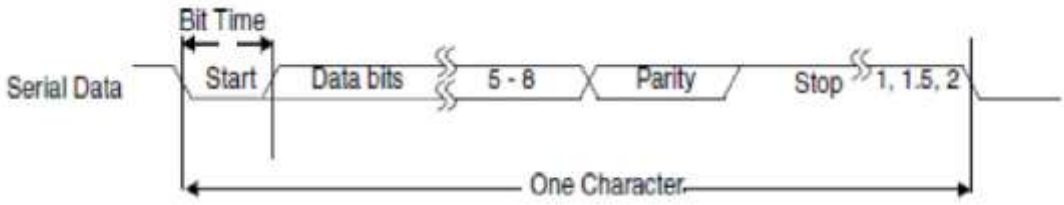

Figure 90: Serial Data Format

An additional parity bit may be added to the serial character. This bit appears after the last data bit, but before the stop bit(s) in the character structure. It provides the UART with the ability to perform simple error checking on the received data.

The UART Line Control Register (UART_LCR_REG) is used to control the serial character characteristics. The individual bits of the data word are sent after the start bit, starting with the least significant bit (LSB). These are followed by the optional parity bit, followed by the stop bit(s), which can be 1, 1.5, or 2.

All the bits in the transmission (with exception of the half-stop bit when 1.5 stop bits are used) are transmitted for the same time duration. This is referred to as a Bit Period or Bit Time. One Bit Time equals 16 baud clocks. To ensure stability on the line, the receiver samples the serial input data at approximately the mid-point of the Bit Time, after the start bit has been detected. As the exact

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number of baud clocks that each bit was transmitted for is known, calculating the mid-point for sampling is not difficult, that is every 16 baud clocks after the mid-point sample of the start bit. Figure 91 shows the sampling points of the first couple of bits in a serial character.

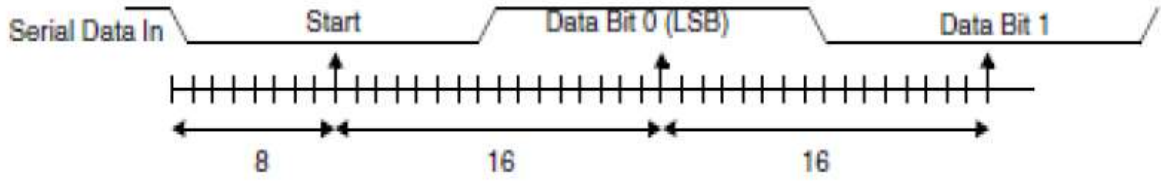

Figure 91: Receiver Serial Data Sampling Points

As part of the 16550 standard, an optional baud clock reference output signal (baudout_n) is supplied to provide timing information to receiving devices that require it. The baud rate of the UART is controlled by the serial clock (*sclk* or *pclk* in a single clock implementation) and the Divisor Latch Register (DLH and DLL). The registers settings for common baud rate values are presented in the following tables.

Table 177: UART/2/3 Baud Rate Generation on DIVN

Baud Rate (Note 1)	Divider	Divisor Latch	DLH Reg	DLL Reg	DLF Reg	Actual BR	Error %
1200	1666.667	1666.6875	6	130	11	1199.99	0.00
2400	833.333	833.3125	3	65	5	2400.06	0.00
4800	416.667	416.6875	1	160	11	4799.76	0.00
9600	208.333	208.3125	0	208	5	9600.96	0.01
14400	138.889	138.875	0	138	14	14401.44	0.01
19200	104.167	104.1875	0	104	3	19196.16	0.02
28800	69.444	69.4375	0	69	7	28802.88	0.01
38400	52.083	52.0625	0	52	1	38415.37	0.04
57600	34.722	34.75	0	34	12	57553.96	0.08
115200	17.361	17.375	0	17	6	115107.91	0.08
230400	8.681	8.6875	0	8	11	230215.83	0.08
460800	4.340	4.3125	0	4	5	463768.12	0.64
921600	2.170	2.1875	0	2	3	914285.71	0.79
1000000	2	2	0	2	0	1000000	0.00

Note 1 Values are valid for UART CLK = 32 MHz (divN_clk).

Table 178: UART/2/3 Baud Rate Generation on RCHS

Baud Rate (Note 1)	Divider	Divisor Latch	DLH Reg	DLL Reg	DLF Reg	Actual BR	Error %
1200	5000.000	5000	19	136	0	1200.00	0.00
2400	2500.000	2500	9	196	0	2400.00	0.00
4800	1250.000	1250	4	226	0	4800.00	0.00
9600	625.000	625	2	113	0	9600.00	0.00
14400	416.667	416.6875	1	160	11	14399.28	0.00
19200	312.500	312.5	1	56	8	19200.00	0.00

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Baud Rate (Note 1)	Divider	Divisor Latch	DLH Reg	DLL Reg	DLF Reg	Actual BR	Error %
28800	208.333	208.3125	0	208	5	28802.88	0.01
38400	156.250	156.25	0	156	4	38400.00	0.00
57600	104.167	104.1875	0	104	3	57588.48	0.02
115200	52.083	52.0625	0	52	1	115246.10	0.04
230400	26.042	26.0625	0	26	1	230215.83	0.08
460800	13.021	13	0	13	0	461538.46	0.16
921600	6.510	6.5	0	6	8	923076.92	0.16
1000000	6	6	0	6	0	1000000	0.00
3000000	2	2	0	2	0	3000000	0.00
6000000	1	1	0	1	0	6000000	0.00

Note 1 Values are valid for CLK_SNC_REG[UARTx_CLK_SEL] = 1 and sys_clk = 96 MHz. For CLK_SNC_REG[UARTx_CLK_SEL] = 0, see Table 177.

Table 179: UART/2/3 Baud Rate Generation on PLL160M

Baud Rate (Note 1)	Divider	Divisor Latch	DLH Reg	DLL Reg	DLF Reg	Actual BR	Error %
1200	8333.333	8333.3125	32	141	5	1200.00	0.00
2400	4166.667	4166.6875	16	70	11	2399.99	0.00
4800	2083.333	2083.3125	8	35	5	4800.05	0.00
9600	1041.667	1041.6875	4	17	11	9599.81	0.00
14400	694.444	694.4375	2	182	7	14400.14	0.00
19200	520.833	520.8125	2	8	13	19200.77	0.00
28800	347.222	347.25	1	91	4	28797.70	0.01
38400	260.417	260.4375	1	4	7	38396.93	0.01
57600	173.611	173.625	0	173	10	57595.39	0.01
115200	86.806	86.8125	0	86	13	115190.78	0.01
230400	43.403	43.375	0	43	6	230547.55	0.06
460800	21.701	21.6875	0	21	11	461095.10	0.06
921600	10.851	10.875	0	10	14	919540.23	0.22
1000000	10	10	0	10	0	1000000	0.00
3000000	3.333	3.3125	0	3	5	3018867.9	0.63
6000000	1.667	1.6875	0	1	11	5925925.9	1.23

Note 1 Values are valid for CLK_SNC_REG[UARTx_CLK_SEL] = 1 and sys_clk = 160 MHz. For CLK_SNC_REG[UARTx_CLK_SEL] = 0, see Table 177.

34.2.2 Clock Support

The UART has two system clocks (*pclk* and *sclk*). Having the second asynchronous serial clock (*sclk*) implemented accommodates accurate serial baud rate settings, as well as APB bus interface requirements.

With the two-clock design, a synchronization module is implemented for synchronization of all control and data across the two system clock boundaries.

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A serial clock faster than four times the *pclk* does not leave enough time for a complete incoming character to be received and pushed into the receiver FIFO. However, in most cases, the *pclk* signal is faster than the serial clock and this should never be an issue.

The serial clock modules must have time to see new register values and reset their respective state machines. This total time is guaranteed to be no more than eight clock cycles of the slower of the two system clocks. Therefore, no data should be transmitted or received before this maximum time expires, after the initial configuration.

34.2.3 Interrupts

The assertion of the UART interrupt (UART_INT) occurs whenever one of the several prioritized interrupt types is enabled and active. The following interrupt types can be enabled with the IER register:

- Receiver Error
- Receiver Data Available
- Character Timeout (in FIFO mode only)
- Transmitter Holding Register Empty at/below threshold (in Programmable THRE interrupt mode)

When an interrupt occurs, the master accesses the UART_IIR_REG to determine the source of the interrupt before dealing with it accordingly. These interrupt types are described in more detail in Table 180.

Table 180: UART Interrupt Priorities

Interrupt ID Bits [3-0]	Interrupt Set and Reset Functions			
	Priority	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0001	-	None		
0110	Highest	Receiver Line status	Overrun/parity/framing errors or break interrupt	Reading the line status register
0100	1	Receiver Data Available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)
1100	2	Character timeout indication	No characters in or out of the RCVR FIFO during the last four-character times and there is at least one character in it during this time	Reading the receiver buffer register
0010	3	Transmitter holding register empty	Transmitter holding register empty (Prog. THRE Mode disabled) or XMIT FIFO at or below threshold (Prog. THRE Mode enabled)	Reading the IIR register (if the source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled)
0000	4	Reserved	-	-
0111	Lowest	Busy detect	Line Control Register was written while the UART is busy (RX or TX line is low)	Reading the UART status register

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34.2.4 Programmable THRE Interrupt

The UART can be configured to have a Programmable THRE Interrupt mode available to increase system performance.

When Programmable THRE Interrupt mode is selected, it can be enabled via the Interrupt Enable Register (IER[7]). When FIFOs and the THRE Mode are implemented and enabled, THRE Interrupts are active at, and below, a programmed transmitter FIFO empty threshold level, as opposed to empty, as shown in the flowchart in Figure 92.

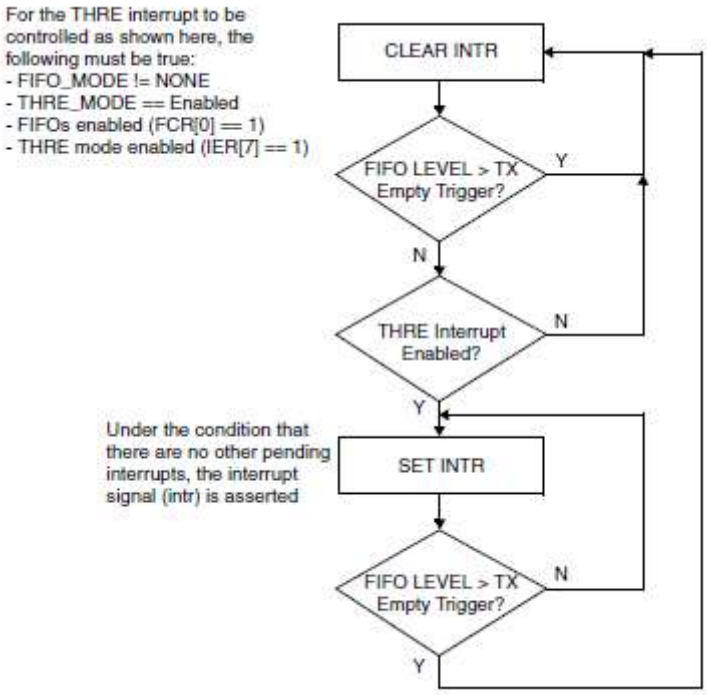

Figure 92: Flowchart of Interrupt Generation for Programmable THRE Interrupt Mode

This threshold level is programmed into FCR[5:4]. The available empty thresholds are: empty, 2, ¼, and ½. See UART_FCR_REG for threshold setting details. The selection of the best threshold value depends on the system's ability to begin a new transmission sequence in a timely manner. However, one of these thresholds should prove optimum in increasing system performance by preventing the transmitter FIFO from running empty.

In addition to the interrupt change, Line Status Register (LSR[5]) also switches function from indicating transmitter FIFO empty to FIFO full. This allows the software to fill the FIFO of each transmit sequence, by polling LSR[5] before writing another character. The flow then becomes “fill transmitter FIFO whenever an interrupt occurs and there is data to transmit” instead of waiting until the FIFO is completely empty. Waiting until the FIFO is empty causes a performance hit whenever the system is too busy to respond immediately.

Even if everything else is selected and enabled, if the FIFOs are disabled via FCR[0], the Programmable THRE Interrupt mode is also disabled. When not selected or disabled, THRE interrupts and LSR[5] function normally (both reflecting an empty THR or FIFO). The flowchart of THRE interrupt generation, when not in programmable THRE interrupt mode, is shown in Figure 93.

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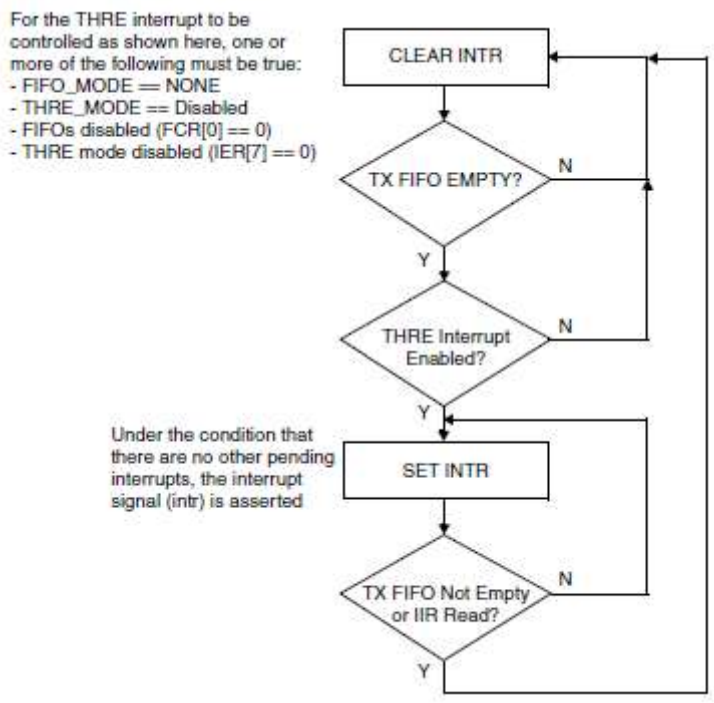

Figure 93: Interrupt Generation not in Programmable THRE Interrupt Mode

34.2.5 Shadow Registers

The shadow registers *shadow* some of the existing register bits that are regularly modified by software. These can be used to reduce the software overhead that is introduced by having to perform read-modify-writes.

- UART_SRBR_REG support a host burst mode where the host increments its address, but still accesses the same Receive buffer register
- UART_STHR support a host burst mode where the host increments its address, but still accesses the same transmit holding register
- UART_SFE_REG accesses the FCR[0] register without accessing the other UART_FCR_REG bits
- UART_SRT_REG accesses the FCR[7-6] register without accessing the other UART_FCR_REG bits
- UART_STER_REG accesses the FCR[5-4] register without accessing the other UART_FCR_REG bits

34.2.6 Direct Test Mode

The on-chip UARTs can be used for the Direct Test Mode required for the final product PHY layer testing. It can be done either over the HCI layer, which engages a full CTS/RTS UART, or using a two-wire UART directly as described in the *Bluetooth® Low Energy Specification (Volume 6, Part F)*.

34.3 Programming

There is a simple sequence of steps that needs to be followed to configure and use the UART controllers:

1. Set up the GPIOs to be used for the UART interface (Px_yy_MODE_REG[PID]).
2. Select the UART clock (CLK_SNC_REG[UARTx_CLK_SEL]).
3. Enable the selected UART by setting the CLK_SNC_REG [UARTx_ENABLE] bit.

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4. Enable access to Divisor Latch Registers (DLL and DLH) by setting the UARTx_LCR_REG[UART_DLAB] bit.
5. Set the desired baud rate. To calculate the registers values for the desired baud rate, use the formula: Divisor = UART CLK / (16 x Baud rate).
   a. UARTx_IER_DLH_REG: High byte of the Divisor integer part.
   b. UARTx_RBR_THR_DLL_REG: Low byte of the Divisor integer part.
   c. UARTx_DLF_REG: The fractional part of the Divisor.
6. Configure the brake control bit, parity, number of stop bits, and data length (UARTx_LCR_REG).
7. Enable and configure the FIFO (UARTx_IIR_FCR_REG).
8. Configure the generated interrupts, if needed (UARTx_IER_DLH_REG).
9. Send a byte:
   a. Check if Transmit Hold Register (THR) is empty (UARTx_LSR_REG[UART_THRE]).
   b. Load the byte to THR (UARTx_RBR_THR_DLL_REG).
   c. Check if the byte was transmitted (UARTx_LSR_REG[UART_TEMT]).
10. Receive a byte:
    a. Wait until serial data is ready (UARTx_LSR_REG[UART_DR]).
    b. Read the incoming byte from the THR (UARTx_RBR_THR_DLL_REG).

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35 UART3 ISO 7816

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

35.1 Introduction

The UART3 block in the DA1470x supports asynchronous protocol smartcards as defined in the ISO 7816-3 (Class B and C) standard.

Features

- ISO/IEC 7816-3 (Class B and C) complaint
- UART Line with Flow Control Signals
- Interrupt line
- DMA support
- An Error signal support with an indication for character repetition
- Inverse and direct convention
- Guard time

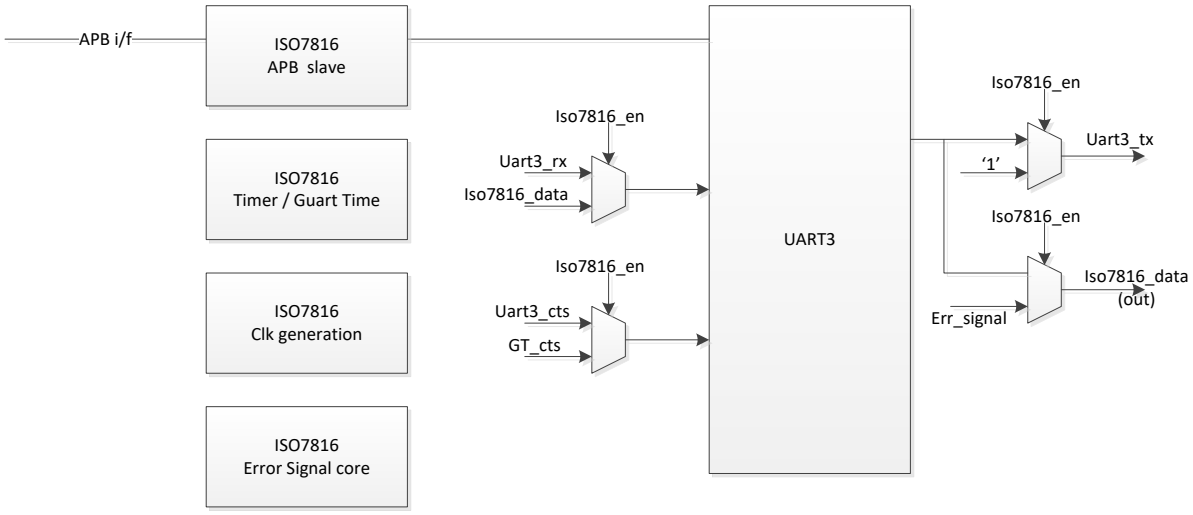

Figure 94: Smart Card (ISO7816-3) Block Diagram

35.2 Architecture

35.2.1 ISO7816-3 Clock Generation

The ISO7816-3 block operates on a system-based clock with a 50 % duty cycle. The clock frequency is calculated using the formula:

F_{SCLK} / [2 * (UART3_CTRL_REG[ISO7816_CLK_DIV] + 1)]

The UART3_CTRL_REG[ISO7816_CLK_DIV] value can be updated at any time, whether the ISO7816-3 clock is enabled or not. The operation of the clock can be checked at any given time by polling the UART3_CTRL_REG[ISO7816_CLK_STATUS] bit and disabled by clearing the ISO7816_CLK_EN[ISO7816_CLK_EN] bit. The UART3_CTRL_REG[ISO7816_CLK_LEVEL] reflects the logical level of the clock while it has been disabled.

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35.2.2 ISO7816-3 Timer – Guard Time

The ISO7816-3 block is equipped with an ISO7816-3 Timer/Guard Timer and can operate in two modes:

- UART3_TIMER_REG[ISO7816_TIM_MODE] = 0
  The timer is clocked with the clock of the ISO7816 module and starts when UART3_TIMER_REG[ISO7816_TIM_EN] = 1. It counts from 0 to UART3_TIMER_REG[ISO7816_TIM_MAX] value. The value of the timer can be read from UART3_TIMER_REG[ISO_TIM_MAX] register field.
  At the point where the top value is reached, the timer stops and the UART3_IRQ_STATUS_REG[ISO7816_TIM_EXPIRED_IRQ] is set. If the UART3_CTRL_REG[ISO7816_TIM_EXPIRED_IRQMASK] is 1, an interrupt is generated. The interrupt is cleared when UART3_TIMER_REG[ISO7816_TIM_EN] is set.
- UART3_TIMER_REG[ISO7816_TIM_MODE] = 1
  The timer is clocked with the 1/16 of the UART bit clock (1/16 etu). If the UART fractional divider has been set, the 1/16 of the UART bit clock does not have a fixed value. If the UART3_TIMER_REG [ISO7816_TIM_EN] bit is set, the timer starts counting from 0 to UART3_TIMER_REG[ISO_TIM_MAX] value, each time a start bit is transmitted by the UART. If the UART3_TIMER_REG[ISO_TIM_MAX] value is set equal to 16*GuartTime-1, the timer counts the minimum delay between the leading edges of two consecutive characters (Guard time). If no FIFO mode and GT>12 etu, the expiration of the timer indicates that the module is allowed to send the next character (Guard Time elapsed). If FIFO mode and GT>12 etu, the UART3_CTRL_REG[ISO7816_AUTO_GT] bit can be set so the module will be able to send the next character automatically each time the Guard Time is reached.

35.2.3 ISO7816-3 Error Detection

The ISO7816-3 block is designed to support the functionality described in section 7.3 of the ISO7816-3 specification document.

Transmit Phase

The transmitter checks the ISO7816 data level for 11 etu sampling time after a character's leading edge is detected. The module samples the data line at 11 etu time and creates two types of interrupts:

- The ISO7816_ERR_TX_TIME_IRQ interrupt is created each time a character is sent
- The ISO7816_ERR_TX_VALUE_IRQ interrupt is created each time the receiver sends an error

The software must check if an ISO7816_ERR_TX_VALUE_IRQ interrupt is generated to retransmit the character. The IRQs are generated at the same time.

Receive Phase

The receiver holds the data line level Low between 1 etu (minimum) and 2 etu (maximum) at 10.5 etu time. The error detection circuit uses the UART parity check and creates an error signal to the transmitter at the proper time. The error signal pulse width and offset can be configured using the UART3_ERR_CTRL_REG register. Furthermore, the ISO7816-3 block can hold the UART_Rx signal High during the error signal transmitting to prevent UART errors from happening.

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35.3 Programming

There is a simple sequence of steps that needs to be followed to configure the Smart Card Controller:

1. Set up the GPIOs to be used for the ISO7816-3 interface (Px_yy_MODE_REG[PID]). Reset (output) and card insert (input) signals shall be configured as GPIOs (Px_yy_MODE_REG[PID] = 0).
2. Enable UART3 by setting the CLK_SNC_REG[UART3_ENABLE] bit.
3. Set up UART3 clock (CLK_SNC_REG[UART3_CLK_SEL]).
4. Enable the ISO7816-3 module by setting the UART3_CONFIG_REG[ISO7816_ENABLE] bit.
5. Set up the ISO7816-3 clock (UART3_CTRL_REG[ISO7816_CLK_DIV]).
6. Initialize UART3 as follows:
    a. Configure FIFO, if needed (UART3_IIR_FCR_REG, UART3_SRT_REG, UART3_STET_REG, UART3_SFE_REG). Note that if Error detection is enabled, the TX FIFO shall remain disabled.
    b. Configure ISO7816 convention.
7. Select data length (UART3_LCR_REG[UART_DLS]):
    a. Select the number of stop bits (UART3_LCR_REG[UART_STOP]).
    b. Enable/disable parity (UART3_LCR_REG[UART_PEN]).
    c. Select even or odd parity (UART3_LCR_REG[UART_EPS]).
    d. If needed, enable Error detection (UART3_CONFIG_REG[ISO7816_ERR_SIG_EN]) and configure the error pulse width and offset (UART3_ERR_CTRL_REG).
    e. Select direct/inverse convention (UART3_CONFIG_REG[ISO7816_CONVENTION]).
8. Configure the baud rate. To calculate the registers values for the desired baud rate, use the formula: Divisor = Fi * (ISO7816_CLK_DIV + 1) / (8 * Di). For Fi and Di values, refer to ISO/IEC 7816-3 Standard Specification, table 7 and table 8:
    a. Enable access to the Divisor Latch register: UART3_LCR_REG[UART_DLAB] = 1.
    b. Set the High byte of the Divisor integer part (UART3_IER_DLH_REG).
    c. Set the Low byte of the Divisor integer part (UART3_RBR_THR_DLL_REG).
    d. Set the fractional part of the Divisor (UART3_DLF_REG).
9. Configure the generated interrupts, if needed (UART3_CTRL_REG).
10. Send a byte:
    a. Set up the Guard Timer (UART3_TIMER_REG).
    b. If TX FIFO is enabled, check if FIFO is full (UART3_USR_REG[UART_TFNF]) or check if Transmit Hold Register (THR) is empty (UART3_LSR_REG[UART_THRE]).
    c. Load the byte to THR (UART3_RBR_THR_DLL_REG).
    d. Check if the byte was transmitted (UART3_LSR_REG[UART_TEMT]).
11. Receive a byte:
    a. Set up the Wait Time (UART3_TIMER_REG).
    b. Wait until serial data is ready (UART3_LSR_REG[UART_DR]) or timer expiration.
    c. Read the received byte from the THR (UART3_RBR_THR_DLL_REG).

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36 SPI Interface

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

36.1 Introduction

This controller implements the Serial Peripheral Interface (SPI™) for master and slave modes.

NOTE
SPI is a trademark of Motorola, Inc.

The serial interface can transmit and receive from 4 to up to 32 bits in master/slave mode. The controller comprises separate TX and RX FIFOs and DMA handshake support. Slave mode clock speed is independent from the system clock speed. The controller can generate an interrupt upon the data threshold reached in the TX or RX FIFOs.

The DA1470x comprises three instances of the SPI Controller, namely SPI, SPI2, and SPI3.

Features

- Slave and master mode for SPI/SPI2 and master mode for SP3
- From 4-bit to up to 32-bit operation
- SPI/SPI2 Master clock line speed up to 24 MHz and SPI3 up to 48 MHz
- SPI mode 0, 1, 2, and 3 support (clock edge and phase)
- Built-in separate 8-bit wide and 32-byte deep RX/TX FIFOs for continuous SPI bursts (SPI, SPI2)
- Built-in separate 8-bit wide and 4-byte deep RX/TX FIFOs for continuous SPI bursts (SPI3)
- Maskable interrupt generation based on TX or RX FIFO thresholds
- DMA support

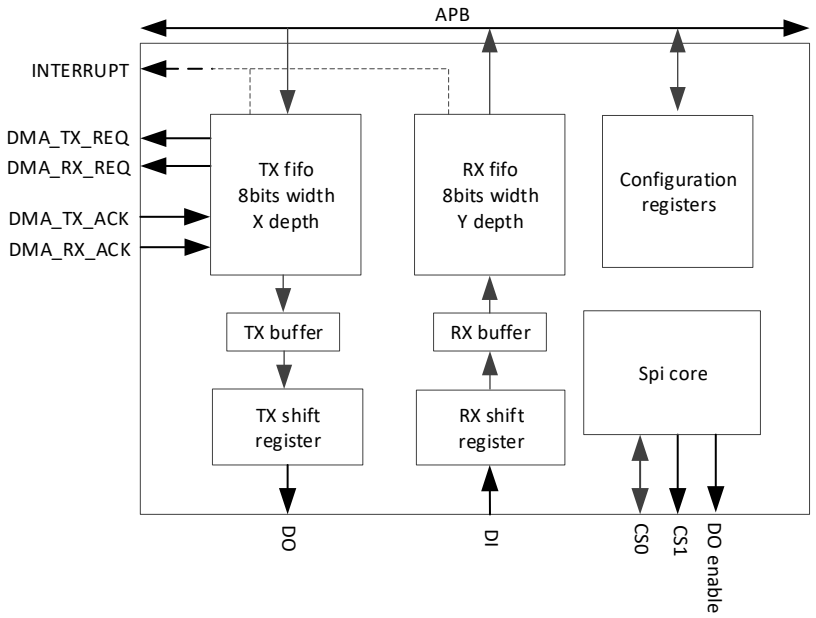

Figure 95: SPI Block Diagram

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36.2 Architecture

The SPI controller is an APB peripheral operating on the apb_clk clock. It contains a front end that is clocked by the spi_clk clock and is responsible for the serialization/deserialization of the data in the RX and TX streams.

Two separate FIFOs are used to store data for RX and TX streams. Since an SPI word can be configured to be from 4 bits to up to 32 bits, one to four FIFO positions can be written/read at the same time. FIFOs contain logic implementing programmable thresholds comparison.

The SPI controller supports DMA requests and interrupt generation based on the FIFO thresholds. If enabled, a DMA request and/or interrupt is asserted with whether TX_FIFO level is low or RX_FIFO level is high.

The SPI interface supports all four modes of operation and the corresponding polarity (CPOL) and phase (CPHA) of the SPI clock (SPI_CLK) are defined in Table 181.

Table 181: SPI Modes Configuration and SCK States

SPI Mode	CPOL	CHPA	TX SPI_CLK	RX SPI_CLK	Idle SPI_CLK
0	0	0	Falling edge	Rising edge	Low
1	0	1	Rising edge	Falling edge	Low
2	1	0	Rising edge	Falling edge	High
3	1	1	Falling edge	Rising edge	High

To read from or to write to an external single-byte FLASH device in the SPI master mode, a byte swap mechanism is implemented to allow for a proper placement of the bytes in a 16-bit word for the DMA to write to/read from the internal RAM. More specifically, when the SPI controller is configured as a master with the DMA support and a 16-bit word width so that the bus utilization is increased compared to reading from an 8-bit device, the byte swap mechanism brings the least significant byte read and place it in the most significant byte in the 16-bit word. The controller automatically swaps the bytes to allow for placing the first byte read in the least significant byte of the 16-bit word. This feature is programmable via SPIx_CTRL_REG[SPI_SWAP_BYTES].

36.2.1 SPI Timing

The timing of the SPI interface when the SPI controller is in slave mode is presented in Figure 96.

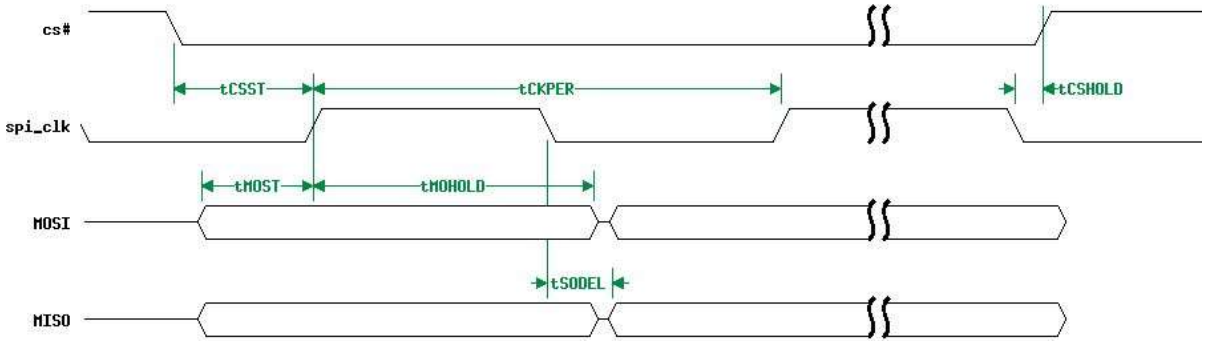

Figure 96: SPI Slave Mode Timing (CPOL = 0, CPHA = 0)

Table 182: SPI Timing Parameters

Parameter	Description	Typ	Unit
t_{CKPER}	spi_clk clock period	No constraints	ns
t_{CSST}	CS active time before the first edge of spi_clk	$t_{CKPER}/2$	ns

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Parameter	Description	Typ	Unit
t_{CSHOLD}	CS non-active time after the last edge of spi_clk	$t_{CKPER}/2$	ns
t_{MOST}	Master input data latching setup time	2	ns
t_{MOHOLD}	Master input data hold time	2	ns
t_{SODEL}	Slave output data delay	14	ns

The aforementioned values are measured in typical conditions, with output pins at 1.8 V and 10 pF load.

36.3 Programming

36.3.1 Master Mode

There is a simple sequence of steps that needs to be followed to configure the SPI controller in master mode:

1. Set the appropriate GPIO ports in SPI clock mode (output), SPI Chip Select mode (output), SPI Data Out mode (output), and SPI Data In mode (input).
2. Enable SPI clock by setting CLK_SNC_REG[SPI/2_ENABLE] = 1 or CLK_SYS_REG[SPI3_ENABLE] = 1.
3. Reset SPI FIFO by setting SPIx_CTRL_REG[SPI_FIFO_RESET] = 1.
4. Set the SPI clock mode (synchronous or asynchronous with APB clock) by programming SPIx_CLOCK_REG[SPI_MASTER_CLK_MODE].
5. Set the SPI clock frequency by programming SPIx_CLOCK_REG[SPI_CLK_DIV]. If SPI_CLK_DIV is not equal to 0x7F, SPI_CLK = module_clk/2 × (SPI_CLK_DIV + 1). If SPI_CLK_DIV = 0x7F, SPI_CLK = module_clk. The module_clk is defined by the CLK_SNC_REG[SPI/2_CLK_SEL] or CLK_SYS_REG[SPI3_CLK_SEL].
6. Set the SPI mode (CPOL or CPHA) by programming SPIx_CONFIG_REG[SPI_MODE].
7. Set the SPI controller in master mode by setting SPIx_CONFIG_REG[SPI_SLAVE_EN] = 0.
8. Define the SPI word length (from 4-bit to 32-bit) by programming SPIx_CONFIG_REG[SPI_WORD_LENGTH]. SPI_WORD_LENGTH = word length - 1.

There is a simple sequence of steps that needs to be followed to execute an SPI Read/Write command:

1. It is possible to configure the SPI module to capture data at the next clock edge when the slave device does not produce the data at the correct clock edge by setting: SPIx_CTRL_REG[SPI_CAPTURE_AT_NEXT_EDGE] = 1. Otherwise, set SPIx_CTRL_REG[SPI_CAPTURE_AT_NEXT_EDGE] = 0.
2. Release FIFO reset by setting SPIx_CTRL_REG[SPI_FIFO_RESET] = 0.
3. Enable SPI TX path by setting SPIx_CTRL_REG[SPI_TX_EN] = 1.
4. Enable SPI RX path by setting SPIx_CTRL_REG[SPI_RX_EN] = 1.
5. Enable the SPI chip select by programming the SPIx_CS_CONFIG_REG[SPI_CS_SELECT] = 1 or 2. This option allows the master to select the slave that is connected to the GPIO that has the function of SPI_EN or SPI_EN2.
6. Enable the SPI controller by setting SPIx_CTRL_REG[SPI_EN] = 1.
7. Write to TX FIFO by programming SPIx_FIFO_WRITE_REG[SPI_FIFO_WRITE]. Write access is permitted only when SPIx_FIFO_STATUS_REG[SPI_STATUS_TX_FULL] = 0.
8. Read from RX FIFO by programming SPIx_FIFO_READ_REG[SPI_FIFO_READ]. Read is permitted only when SPIx_FIFO_STATUS_REG[SPI_STATUS_RX_EMPTY] = 0.
9. To disable the SPI chip select, set SPIx_CS_CONFIG_REG[SPI_CS_SELECT] = 0 to deselect the slave and set SPIx_CTRL_REG[SPI_FIFO_RESET] = 1 to reset the SPI FIFO.

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36.3.2 Slave Mode

There is a simple sequence of steps that needs to be followed to configure the SPI/SPI2 controllers in slave mode:

1. Set the appropriate GPIO ports in SPI clock mode (input), SPI Chip Select mode (input), SPI Data Out mode (output), and SPI Data In mode (input).
2. Enable SPI clock by setting CLK_SNC_REG[SPI/2_ENABLE] = 1.
3. Reset SPI FIFO by setting SPIx_CTRL_REG[SPI_FIFO_RESET] = 1.
4. Set the SPI mode (CPOL or CPHA) by programming SPIx_CONFIG_REG[SPI_MODE].
5. Set the SPI controller in slave mode by setting SPIx_CONFIG_REG[SPI_SLAVE_EN] = 1.
6. Define the SPI word length (from 4-bit to 32-bit) by programming SPIx_CONFIG_REG[SPI_WORD_LENGTH]. SPI_WORD_LENGTH = word length - 1.

There is a simple sequence of steps that needs to be followed to execute an SPI Read/Write command:

1. Set SPI FIFO in normal operation by setting SPIx_CTRL_REG[SPI_FIFO_RESET] = 0.
2. Enable SPI TX path by setting SPIx_CTRL_REG[SPI_TX_EN] = 1.
3. Enable SPI RX path by setting SPIx_CTRL_REG[SPI_RX_EN] = 1.
4. Enable the SPI controller by setting SPIx_CTRL_REG[SPI_EN] = 1.
5. Write the first data byte directly to the TX buffer by programming the SPIx_TXBUFFER_FORCE_REG[SPI_TXBUFFER_FORCE].
6. Write the rest of the data to TX FIFO by programming SPIx_FIFO_WRITE_REG[SPI_FIFO_WRITE]. Write access is permitted only if SPIx_FIFO_STATUS_REG[SPI_STATUS_TX_FULL] = 0.
7. Read from RX FIFO by programming SPIx_FIFO_READ_REG[SPI_FIFO_READ]. Read is permitted only if SPIx_FIFO_STATUS_REG[SPI_STATUS_RX_EMPTY] = 0.

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37 Real-Time Clock

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

37.1 Introduction

The DA1470x is equipped with a Real-Time Clock (RTC) which provides complete clock and calendar information with automatic time units' adjustment and easy configuration.

Features

- Complete time of day clock: 12/24 hour, hours, minutes, seconds, and hundredths
- Calendar function: day of the week, date of the month, month, year, century, leap year compensation, and year 2000 compliant
- Alarm function: month, date, hour, minute, second, and hundredths resolution
- Event interrupt on any calendar or time unit
- Available during sleep
- Granularity of 10 ms

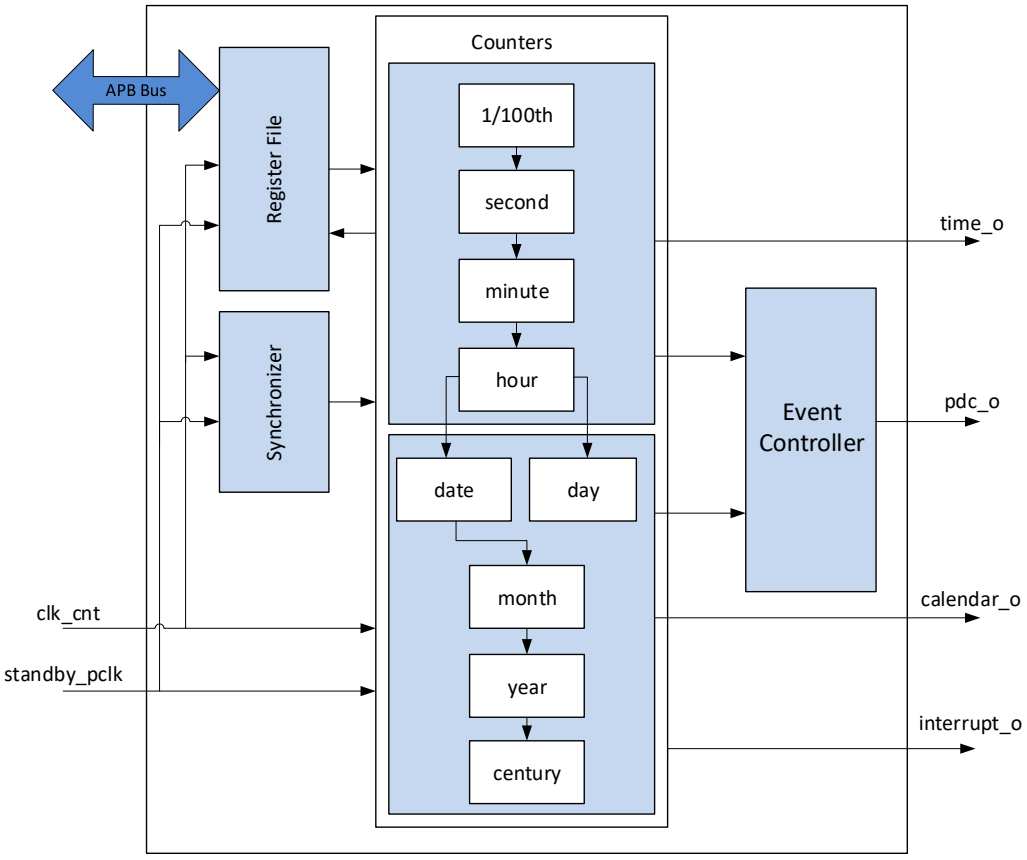

Figure 97: Real-Time Clock Block Diagram

37.2 Architecture

The architecture of the Real-Time Clock is depicted in Figure 97.

The RTC supports a year range from 1900 to 2999 as well as a full month, date, minute, second, and hundredth of second ranges. It also supports hour ranges of 0 to 23 (24-hour format), or 1 to 12 with the a.m./p.m. flag (12-hour format).

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Alarms can be generated in two ways: as a one-time alarm, or as a recurring alarm. In addition to alarms, the RTC can detect when a particular event occurs. Each field of the calendar and time counter can generate an event when it rolls over. For example, an event can be generated every new month, new week, new day, new half-day (12-hour mode), new minute, or new second. Both alarms and events can generate an interrupt. All the interrupts can be set, enabled, disabled, or masked at any time.

The RTC block has been enhanced with the RTC_EVENT_CONTROLLER.

The RTC_EVENT_CONTROLLER comprises a 13-bit counter which counts down starting from a configurable value (programmed in RTC_PDC_EVENT_PERIOD). This operation can be enabled/disabled by RTC_PDC_EVENT_EN.

Every time this counter reaches 0, a signal towards the PDC is asserted. The same signal is also driven to the Cortex-M33 and SNC RTC_EVENT interrupt line. The signal is automatically de-asserted after the RTC_PDC_EVENT_CLEAR_REG is read.

37.3 Programming

There is a simple sequence of steps that needs to be followed to configure the RTC:

1. Configure the 100 Hz RTC granularity if needed:
   a. Based on the selected slp_clk clock (for example, 32768 Hz), set the CLK_RTCDIV_REG[RTC_DIV_INT] = 327 (= 0x147).
   This value should be equal to the integer divisor part of the formula $F_{SLP\_CLK}/100 = \mathbf{327}.680$.
   b. Based on the selected slp_clk clock (for example, 32768 Hz), set the CLK_RTCDIV_REG[RTC_DIV_FRAC] = 680 (= 0x2A8).
   This value should be equal to the fractional divisor part of the formula $F_{SLP\_CLK}/100 = 327.\mathbf{680}$.
   c. To achieve better accuracy of the divisor, configure the denominator for the fractional division accordingly (CLK_RTCDIV_REG[RTC_DIV_DENOM]).
   d. Enable the 100 Hz RTC granularity by setting the CLK_RTCDIV_REG [RTC_DIV_ENABLE] bit.
2. Enable the time functionality by clearing the RTC_CONTROL_REG[RTC_TIME_DISABLE].
3. Enable the calendar functionality by clearing the RTC_CONTROL_REG[RTC_CAL_DISABLE].
4. Choose between 12 or 24 hours based mode (RTC_HOUR_MODE_REG[RTC_HMS]).
5. Configure the time (RTC_TIME_REG).
6. Configure the date (RTC_CALENDAR_REG).
7. Set up a time alarm if needed (RTC_ALARM_ENABLE_REG).
8. Set up a calendar alarm if needed (RTC_CALENDAR_ALARM_REG).
9. Enable the configured alarms (RTC_ALARM_ENABLE_REG[RTC_ALARM_xxxx_EN]).
10. Configure the interrupt generation when an alarm happens (RTC_INTERRUPT_ENABLE_REG). Disable the interrupt generation with RTC_INTERRUPT_DISABLE_REG.
11. Configure the event flag generation when an alarm happens (RTC_EVENT_FLAGS_REG).
12. Choose if SW reset resets the RTC (RTC_KEEP_RTC_REG[RTC_KEEP]).
13. Set up the Event Controller, if needed:
    If trigger to PDC is enabled:
    a. Set up the event period (RTC_PDC_EVENT_PERIOD_REG[RTC_PDC_EVENT_PERIOD]).
    b. Enable the PDC to trigger (RTC_EVENT_CTRL_REG[RTC_PDC_EVENT_EN]).

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38 General-Purpose Timers

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

38.1 Introduction

The Timers block contains six 24-bit wide timers (namely, Timer, Timer2, Timer3, Timer4, Timer5, and Timer6) that are software controlled, programmable, and can be used for various tasks. All Timer blocks are residing in the timer's power domain (PD_TMR) and support the same features with the following exceptions: Timer and Timer4 are of the same type and have an increased amount of triggering GPIO channels (4), with Timer4 only generating a CAPTIMER_IRQ. Timer and Timer4 support an automatic mode switch from one shot to counter, and a single (first) event capture feature. Finally, the PWM signals from all timers except Timer4 and Timer5 can be synchronized.

Features

- Six 24-bit general-purpose timers
- Pulse Width Modulated signal (PWM), one per timer block
- PWM start synchronization (except Timer4 and Timer5)
- Two channels for capture input triggered by GPIOs and generated an interrupt (Timer/Timer4 have four channels)
- Programmable single event capture of the timer’s value after a GPIO toggle (Timer/Timer4 only)
- One-shot pulse with programmable pulse width generated by either a GPIO toggle or a register write
- Automatically switch from one-shot to counter mode capability (Timer/Timer4 only)
- Five-bit clock pre-scaler and selectable clock source of 32 MHz or sleep clock
- Up/down counting capability with free-running mode
- Active while system is in sleep mode
- Dedicated interrupt line per timer, one capture event interrupt (Timer4)
- GPIO edges (positive or negative) counting function

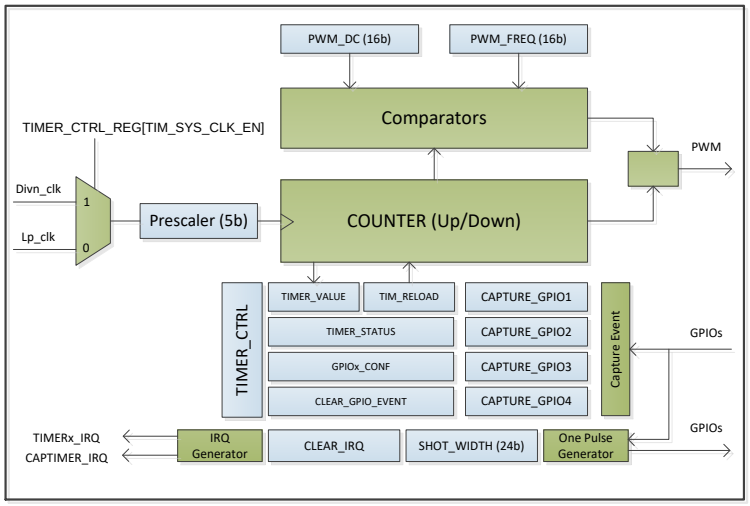

Figure 98: General Purpose Timer’s Block Diagram

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38.2 Architecture

38.2.1 Overview

There are six instances of the same 24-bit timer block (Timer, Timer2, Timer3, Timer4, Timer5, and Timer6) in the system. The general timer's block diagram is shown in Figure 98. All timer blocks are residing in their own power domain (PD_TMR) and support a number of common features that are described in detail in the following section.

The clock input of each timer block can be individually defined to be either an always 32 MHz clock sourced by the sys_clk or the slp_clk. A generic pre-scaler which is common for all timer instances of 5 bits can be used to reduce all-timer clocks further down if needed. This results in a minimum frequency of 0.5 kHz and a maximum of 32 MHz.

The timer instances have a few small differences with respect to the supported features, which are summarized in Table 183.

Table 183: Timers Features Overview

Feature	Timer	Timer2	Timer3	Timer4	Timer5	Timer6
Free-Running Counter, PWM generation, Edge detection counter	✓	✓	✓	✓	✓	✓
PWM start synchronization	✓	✓	✓	✕	✕	✓
PWM when in sleep mode	P0_30	✕	P1_30	P1_31	✕	✕
Event Capturing Channels	4	2	2	4	2	2
Event Capture IRQ	✕	✕	✕	✓	✕	✕
One-Shot	✓	✓	✓	✓	✓	✓
One-Shot with auto switch	✓	✕	✕	✓	✕	✕
First event capture	✓	✕	✕	✓	✕	✕

All GPIO related timer features can be mapped on any of the following GPIOs:

- P0_00 up to P0_13
- P1_00 up to P1_17

38.2.2 Features

38.2.2.1 Free-Running Counter

Each timer block has a configurable free running up/down counter that triggers an interrupt when passing from the pre-configured value and immediately returns to 0 or pre-load depending on whether it is counting up or down. The timer can be instructed to continuously count upwards and wrap around when reaching its boundaries.

38.2.2.2 PWM Generation

Each block outputs a single PWM signal which is not affecting the actual counter running. The PWM generator can define the frequency and the duty cycle of the generated PWM signal by further dividing the clock by a maximum (2^{16}+1). A 16-bit PWM duty cycle register enables 65535 steps for defining the pulse width. Note that for the minimum PWM frequency only 50 % duty cycle is possible.

PWM synchronization is supported for all timers except Timer4 and Timer5. A register defines the selection of which timers' PWM signals should start synchronously. It is assumed that all the timer's blocks are running on the same clock source while PWM frequency and duty cycle might be different.

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38.2.2.3 Event Capturing

Capturing a snapshot of the counter, when a GPIO toggles, is another feature of the Timer block. Any edge on any (pre-configured) GPIO can be sensed to trigger a Timer's snapshot stored into a separate register. Another (or the same) GPIO can be configured for capturing a second edge, hence storing a second snapshot into a second register. The difference of these two registers indicates the time distance of the two triggering events. Hence it can be used for measuring the frequency of a signal or the timing interval between two interrupts coming from external devices.

A single event capturing functionality is also supported by every Timer block. In this mode, the timer stores a snapshot, on the first capture register, only with the first trigger (after programming) of the capture event. Subsequent edges of the triggering GPIO do not change the value of the first capture register and they are neglected by the capturing circuitry.

38.2.2.4 One-Shot

Upon an input trigger from a GPIO toggle or a register write, a separate GPIO serves as an output, delivering a pulse of configurable width. This feature implements a PWM reply in hardware. There are four different options for the input trigger as shown in Table 184.

Table 184: Timer's One-Shot Trigger Options

Option	One-Shot Trigger
1	Select external GPIO as the trigger for one shot
2	Select a register write as the trigger of one shot
3	Either of the two triggers one shot
4	None of the two triggers one shot

A new configuration bit is implemented to allow for automatically switching the Timer block from the one-shot mode into the counter mode. The goal is to automatically switch to counting down right after the completion of the pulse output without the CPU involvement. In case no start value has been programmed, an interrupt then is immediately issued to the CPU.

38.2.2.5 Edge Detection Counter

Every Timer block supports edge detection mode where a specific (programmable) GPIO can be selected for asynchronously counting up edges on this line. This operation is available even when the system is in any of the sleep modes (except for hibernation). The frequency range of the edge train should never exceed 80 MHz so that edges are properly identified, and counter updated. The programmability of the edge (Positive or Negative) is available. Upon a pre-defined counter threshold reach, an interrupt is generated, and the counter is automatically reset to zero.

38.3 Programming

There is a simple sequence of steps that needs to be followed to program the GP Timers:

1. Disable the Timer by clearing the TIMERx_CTRL_REG[TIM_EN] bit and the TIMERx_CTRL_REG[TIM_CLK_EN] bit.
2. Select Timer's clock (TIMER_CTRL_REG[TIM_SYS_CLK_EN]) and pre-scaler (TIMER_PRESCALER_REG).
3. Enable Timer's clock (TIMERx_CTRL_REG[TIM_CLK_EN]).
4. Select Timer's mode (TIMER_CTRL_REG[TIM_ONESHOT_MODE_EN]).
   a. One-shot mode:
      i. Set delay phase (TIMERx_SETTINGS _REG[TIM_RELOAD]).
      ii. Set shot phase duration (TIMERx_SHOTWIDTH_REG).
      iii. Select one shot/primary capture event input (TIMERx_GPIO1 _CONF_REG) and trigger polarity (TIMERx_CTRL_REG[TIM_IN1_EVENT_FALL_EN]).

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iv. Select the secondary capture event input (TIMERx_GPIO2_CONF_REG) and trigger polarity (TIMERx_CTRL_REG[TIM_IN2_EVENT_FALL_EN]).

b. Counter mode:

i. Set timer's up/down direction (TIMER_CTRL_REG[TIM_COUNT_DOWN_EN]).

ii. Set timer's reload or max value (TIMERx_SETTINGS_REG[TIM_RELOAD]).

iii. Enable free run mode if the timer counts upwards by setting the TIMERx_CTRL_REG[TIM_FREE_RUN_MODE_EN] bit.

iv. Set up capture events input (TIMERx_GPIOy_CONF_REG) and trigger polarity (TIMERx_CTRL_REG[TIM_INx_EVENT_FALL_EN]). Note that TIMER supports up to four capture events inputs.

5. Configure PWM:
   a. Set up frequency (TIMERx_PWM_CTRL_REG[TIM_PWM_FREQ]).
   b. Configure duty cycle (TIMERx_PWM_CTRL_REG[TIM_PWM_DC]).
6. Select if needed synchronization between the PWM outputs of different timers by configuring the TIMER_PWM_SYNC_REG
7. Select if the event on the selected input GPIOs creates a CAPTIM interrupt (TIMERx_CTRL_REG[TIM_CAP_GPIOy_IRQ_EN]).
8. Set up GPIO as Timer output (Px_yy_MODE_REG[PID] = 51 to 56, see P0_00_MODE_REG description).
   Note that TIMER, TIMER3, and TIMER4 PWM outputs can be activated at specific pins (P0_30, P1_30, and P1_31) during sleep by setting the SLP_MAP_REG[TMRx_PWM_SLP_MAP] bits.
9. Enable Timer interrupt by setting the TIMERx_CTRL_REG[TIM_IRQ_EN] bit.
10. Enable Timer by setting the TIMERx_CTRL_REG[TIM_EN] bit.

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39 Watchdog Timers

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

39.1 Introduction

The DA1470x contains three watchdog timers:

- The System watchdog that is in the sleep power domain (PD_SLP)
- The CMAC watchdog that is in the radio power domain (PD_RAD)
- The SNC watchdog that is in the SNC power domain (PD_SNC)

They protect the system from getting stuck because of the SW problems in the application processor (Cortex-M33), the SNC processor (Cortex-M0+), and the CMAC area (Cortex-M0+). They are clocked by internally generated clocks, RCLP or RCX, and the CMAC module clock (only for CMAC watchdog). CMAC and SNC watchdogs are accessible by the Cortex-M33 if the radio/SNC power domain is powered up.

Features

- System Watchdog
  - A 13 bits down counter running on either RCLP (fixed division at 32 kHz) or RCX and can operate for 82 seconds or three minutes, depending on the clock
  - Internal programmable clock sources are RCLP or RCX, of which RCLP is the default. If RCX is used as a sleep clock, RCLP might be turned off
  - Generates:
    - NMI to Cortex-M33 if the counter reaches 0
    - HW reset if the counter reaches -16
  - Protected by a lock bit to avoid freeze by mistake
  - Automatically frozen when Cortex-M33 is in debug mode
- CMAC Watchdog
  - A 13 bits down counter running on the CMAC module clock counting 10 ms pulses
  - Generates:
    - Early notification interrupt to Cortex-M0+ if the counter reaches 16
    - CMAC2SYS_IRQ to Cortex-M33 if the counter reaches 0
    - HW reset if the counter reaches -16
  - Protected by a lock bit to avoid freeze by mistake
  - Automatically frozen when CMAC Cortex-M0+ is in debug mode
- SNC Watchdog
  - A 13 bits down counter running on the SNC module clock counting 10ms pulses
  - Generates:
    - Early notification interrupt to SNC Cortex-M0+ if the counter reaches 16
    - HW reset if the counter reaches -16
  - Protected by a lock bit to avoid freeze by mistake
  - Automatically frozen when SNC Cortex-M0+ is in debug mode

Figure 99 shows the block diagram of the system watchdog.

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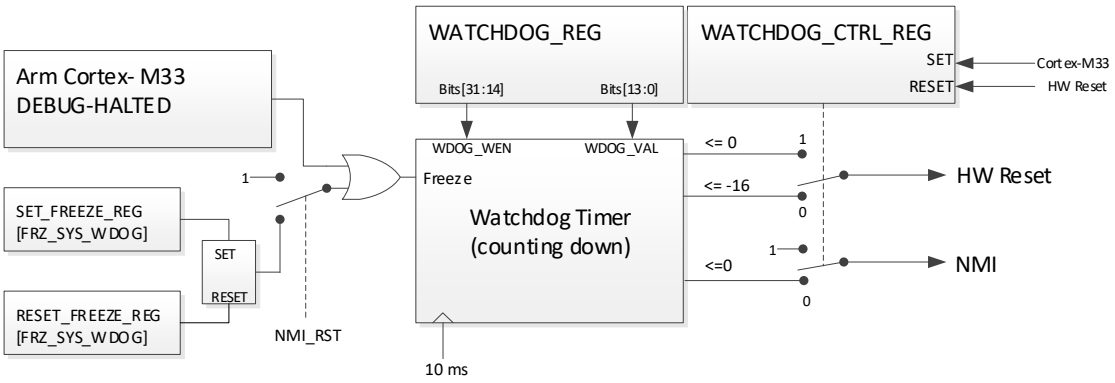

Figure 99: System Watchdog Block Diagram

39.2 Architecture

The System Watchdog is supplied by the sleep domain (PD_SLP) and is automatically enabled as soon as the system powers up. It is decremented by one every 10 ms, assuming the default source clock is the RCLP. The timer value can be accessed through the WATCHDOG_REG which is set to the max value at reset. This results in a maximum watchdog time-out of 82 seconds. If the RCX is used as a source clock, the time-out time is even longer, depending on the RCX frequency.

During write access, WATCHDOG_REG bits [31-14] must be 0. This provides extra filtering for a software run-away writing all ones to the WATCHDOG_REG. If the watchdog reaches 0, the counter value gets a negative value setting bit 8. The counter sequence is 1, 0, 1FFF16 (-1), 1FFE16(-2),...,1FF016 (-16).

If WATCHDOG_CTRL_REG[NMI_RST] = 0, the watchdog timer generates an NMI to the Cortex-M33 when the watchdog timer reaches 0 and an HW reset when the counter becomes less or equal to -16. The NMI handler must write any value > -16 to the WATCHDOG_REG to prevent the generation of a WDOG reset within 16x10ms = 160 ms. If WATCHDOG_CTRL_REG[NMI_RST] = 1, the watchdog timer generates a WDOG reset if the timer becomes less than or equal to 0.

The system watchdog can be frozen by Cortex-M33. It is always frozen automatically when the debugger is attached, and the Cortex-M33 CPU is halted during debugging. However, even if the watchdog is frozen by Cortex-M33, when Cortex-M33 gets into any sleep mode (PD_SYS is turned off), the system watchdog is automatically resumed to operate during sleep.

The CMAC and SNC Watchdogs are the same circuit with the following amendments:

- It resides in the radio or SNC power domain (PD_RAD/PD_SNC). It is active as soon as the power domain is enabled
- Input clock source is the CMAC/SNC module clock, divided to provide a clock period of 10 ms
- It has one extra notification compared to the system watchdog:
  - When 16 is reached, an interrupt is issued to the Cortex-M0+ (CMAC/SNC)
  - When 0 is reached on the CMAC Watchdog, an interrupt is issued to the Cortex-M33
  - When -16 is reached, an HW reset is triggered

These watchdogs are also automatically halted when the debugger is attached and the Cortex-M0+ (CMAC or SNC) is halted during debugging.

39.3 Programming

39.3.1 System Watchdog

There is a simple sequence of steps that needs to be followed to program the System Watchdog:

1. Freeze watchdog by setting the SET_FREEZE_REG[FRZ_SNC_WDOG] bit (optionally).

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2. Select NMI and reset events (WATCHDOG_CTRL_REG[NMI_RST]).
3. Wait until WATCHDOG_CTRL_REG[WRITE_BUSY] = 0.
4. Enable writing of the watchdog timer (WATCHDOG_REG[WDOG_WEN] = 0]).
5. Write watchdog timer reload value (WATCHDOG_REG[WDOG_VAL], see register description).
6. Resume watchdog (RESET_FREEZE_REG[FRZ_SYS_WDOG] = 1) if frozen.

39.3.2 CMAC Watchdog

There is no specific sequence of steps for the CMAC Watchdog since it gets automatically enabled. Some general points are referred below:

- The CMAC watchdog is automatically enabled when the radio power domain is activated
- CMAC takes care of reloading the watchdog timer frequently. M33 intervention is not necessary
- M33 can freeze/unfreeze the CMAC watchdog (SET_FREEZE_REG[FRZ_CMAC_WDOG]) and reload the watchdog timer (CM_WDOG_REG[CM_WDOG_CNT]) if needed
- CMAC watchdog automatically freezes when Cortex-M0+ is halted via the SWD
- When the system power domain is powered down, it’s not possible to freeze CMAC watchdog via SW

39.3.3 SNC Watchdog

There is a simple sequence of steps that needs to be followed to program the SNC Watchdog Timer:

1. Freeze watchdog by setting the SET_FREEZE_REG[FRZ_SYS_WDOG] bit (optionally).
2. Write watchdog timer reload value (SNC_WDOG_REG[SNC_WDOG_CNT], with the value of SNC_WDOG_REG[SNC_WDOG_WRITE_VALID] set to 3 (see register description).
3. Resume watchdog (RESET_FREEZE_REG[FRZ_SYS_WDOG] = 1) if frozen.

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40 USB Controller

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

40.1 Introduction

The USB interface is an integrated USB Node controller compatible with the full speed (FS) and low speed (LS) *USB specification*, *version 1.1* (V1.1).

It integrates a Serial Interface Engine (SIE) and USB endpoint (EP) FIFOs. Seven endpoint pipes are supported: one for the mandatory control endpoint and the other six for interrupt endpoints. Each endpoint pipe has a dedicated FIFO, 64 bytes for the control endpoint and 512 bytes for the other endpoints.

The USB transceiver module is accessed through USB_Dp and USB_Dm pins.

Features

- Full/Low-Speed USB node
- Interfaces to USB V1.1 transceiver with the programmable rise and fall times and integrated D+/D- pull-up resistors
- Serial Interface Engine (SIE) consisting of a Media Access Controller (MAC), *USB Specification 1.0* and *1.1* compliant
- USB Function Controller with seven FIFO-based Endpoints:
  - One bidirectional Control Endpoint 0 (64 bytes)
  - Three Transmit Endpoints (512 bytes each)
  - Three Receive Endpoints (512 bytes each)
- Automatic Data PID toggling/checking and NAK packet recovery (maximum 256x32 bytes of data = 8 kB)

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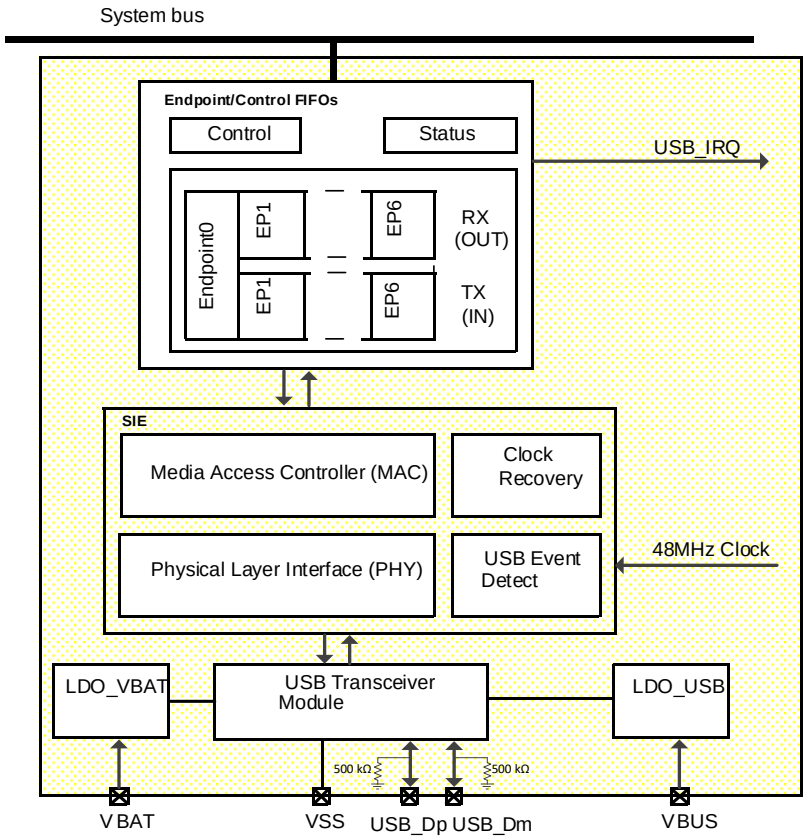

Figure 100: USB Node Block Diagram

40.2 Architecture

40.2.1 Serial Interface Engine

The SIE is comprised of physical (PHY) and Media Access Controller (MAC) modules. The PHY module includes the digital-clock recovery circuit, a digital glitch filter, End of Packet (EOP) detection circuitry, and bit stuffing and unstuffing logic. The MAC module includes packet formatting, CRC generation, and checking, and endpoint address detection. It provides the necessary control to give the NAK, ACK, and STALL responses determined by the Endpoint Pipe Controller (EPC) for the specified endpoint pipe. The SIE is also responsible for detecting and reporting USB-specific events, such as NodeReset, NodeSuspend, and NodeResume. The module output signals to the transceiver are well-matched (under 1 ns) to minimize skew on the USB signals.

The USB specifications use bit stuffing and unstuffing as the method to ensure adequate electrical transitions on the line to enable clock recovery at the receiving end. The bit stuffing block ensures that whenever a string of consecutive 1's is encountered, a 0 is inserted after every sixth 1 in the data stream. The bit unstuffing logic reverses this process.

The clock recovery block uses the incoming NRZI data to extract a data clock (12 MHz for FS, 1.5 MHz for LS) from a 48 MHz (FS)/6 MHz (LS) input clock. The extracted data clock is used in the data recovery circuit. The output of this block is binary data which is decoded from the NRZI stream and can be appropriately sampled using the extracted 12 (1.5) MHz clock. The jitter performance and timing characteristics meet the requirements in *Chapter 7* of the *USB Specification*.

40.2.2 Endpoint Pipe Controller (EPC)

The EPC provides the interface for USB function endpoints. An endpoint is the ultimate source or sink of data. An endpoint pipe facilitates the movement of data between USB and memory and completes the path between the USB host and the function endpoint. According to the *USB*

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specification, up to 31 such endpoints are supported at any given time. USB allows a total of 16 unidirectional endpoints for receive and 16 for transmit. As the control endpoint 0 is always bidirectional, the total number is 31. The FS/LS USB node supports a maximum of seven endpoint pipes with the same function address. See Figure 101 for a schematic diagram of the EPC operation.

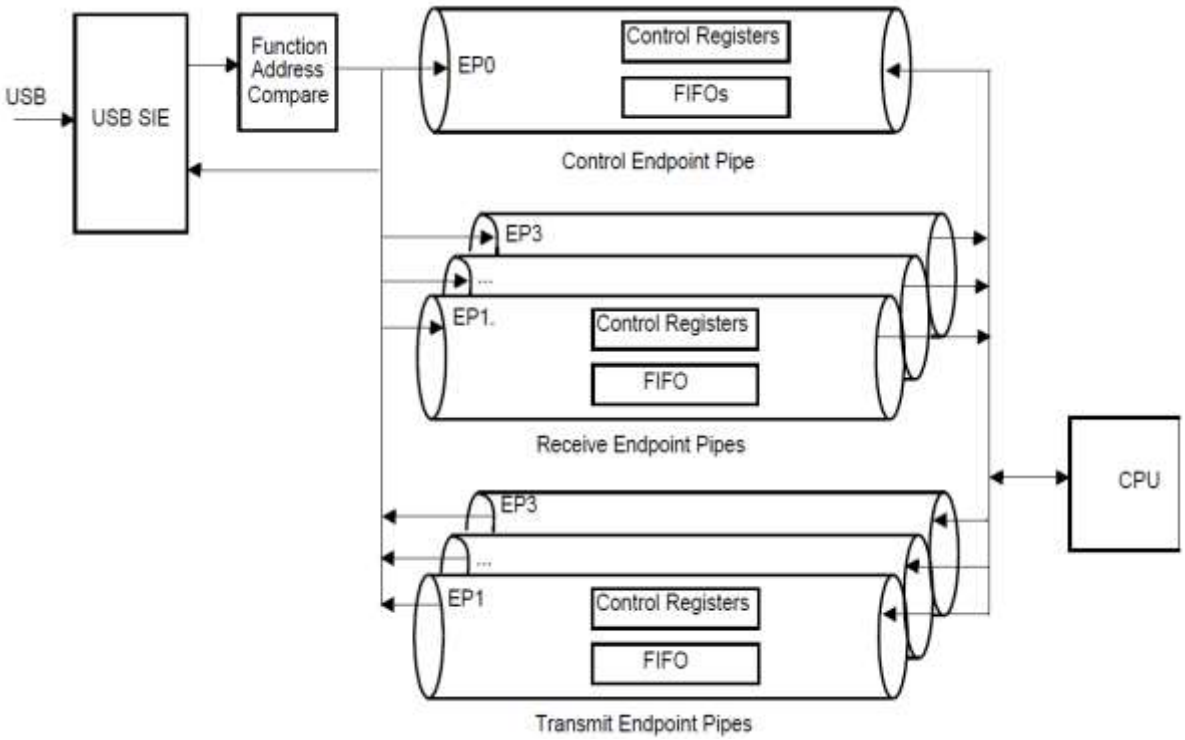

Figure 101: Endpoint Operation

A USB function is a USB device that can transmit and receive information on the bus. A function may have one or more configurations, each of which defines the interfaces that make up the device. Each interface, in turn, is composed of one or more endpoints.

Each endpoint is an addressable entity on USB and is required to respond to IN and OUT tokens from the USB host (typically a PC). IN tokens indicate that the host has requested to receive information from an endpoint, and OUT tokens indicate that it is about to send information to an endpoint.

On detection of an IN token addressed to an endpoint, the endpoint pipe should respond with a data packet. If the endpoint pipe is currently stalled, a STALL handshake packet is sent under software control. If the endpoint pipe is enabled but no data is present, a Negative Acknowledgment (NAK) handshake packet is sent automatically. If the endpoint pipe is isochronous and enabled but no data is present, a bit of stuff error followed by an “end of packet” is sent on the bus.

Similarly, on detection of an OUT token addressed to an endpoint, the endpoint pipe should receive a data packet sent by the host and load it into the appropriate FIFO. If the endpoint pipe is stalled, a STALL handshake packet is sent. If the endpoint pipe is enabled but no buffer is present for data storage, a NAK handshake packet is sent.

A disabled endpoint does not respond to IN, OUT, or SETUP tokens.

The EPC maintains separate status and control information for each endpoint pipe.

For IN tokens, the EPC transfers data from the associated FIFO to the host. For OUT tokens, the EPC transfers data in the opposite direction.

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40.2.3 Functional States

40.2.3.1 Line Condition Detection

At any given time, the USB node is in one of the following states:

- NodeOperational: this is the normal operating state of the node. In this state, the node is configured for operation on the USB
- NodeSuspend: Device operation suspended due to USB inactivity
  - A USB node is expected to enter NodeSuspend state when 3 ms have elapsed and no bus activities have been detected
  - The USB node looks for this event and signals it by setting the USB_SD3 bit in the USB_ALTEV_REG register, which causes a USB_INT, if enabled, to be generated. The firmware should respond by putting the USB node in NodeSuspend state
- NodeResume: Device wake-up from the suspended state
  - In the NodeResume state, a constant “K” is signaled on the USB and should last at least 1 ms and no more than 15 ms. After that, the USB host should continue sending the NodeResume signal for at least another 20 ms, and then completes the NodeResume operation by issuing the End of Packet (EOP) sequence
- NodeReset: Device reset
  - When detecting a NodeResume or NodeReset signal while in NodeSuspend state, the USB node can signal it to the CPU by generating an interrupt

The NodeSuspend, NodeResume, or NodeReset line condition causes a transition from one operating state to another. These conditions are detected by specialized hardware and reported via the Alternate Event (USB_ALTEV_REG) register. If interrupts are enabled, an interrupt is generated upon the occurrence of any of the specified conditions.

Refer to Section 40.2.11 on how to obtain the lowest power consumption in the NodeSuspend state.

The USB node can resume the normal operation in two ways:

- Host initiated. When a resume signal followed by LS EOP on the USB is detected, a USB_ALTEV_REG [USB_RESUME] interrupt is generated. The firmware responds by setting the NodeOperational in the USB_NFSR_REG (see also Section 40.2.11).
- Device initiated. When a local event is detected, for example, a GPIO key is pressed, a KEYB_INT is generated. The firmware releases the USB node from the NodeSuspend state by initiating a NodeResume signal on the USB using the NFSR register. The node firmware must ensure at least 5 ms of Idle on the USB by checking the SD5 in the USB_ALTEV before going to the NodeResume state.

To successfully detect the EOP, the firmware must respond by setting NodeOperational in the USB_NFSR_REG. Once an EOP is detected, the USB_ALTEV_REG[USB_EOP] is set. If no EOP is received from the host within 100 ms, the software must re-initiate NodeResume.

USB specifications require that a device must be ready to respond to USB tokens within 10 ms after wake-up or reset.

40.2.4 Functional State Diagram

Figure 102 shows the device states and transitions as well as the conditions that trigger each transition. All FS/LS USB node state transitions are initiated by the firmware.

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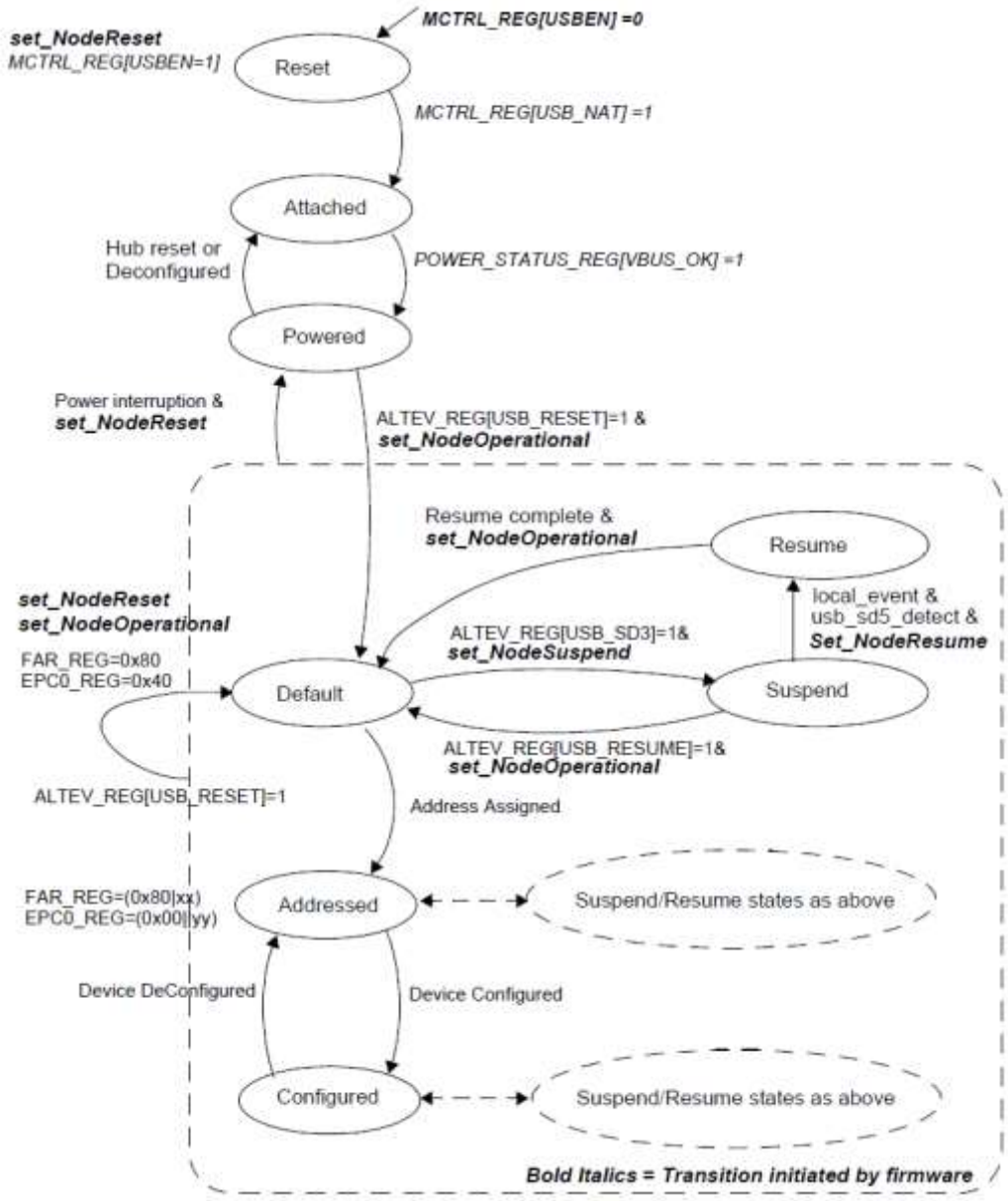

Figure 102: Node Functional State Diagram

Note 1 When the node is not in NodeOperational state, all registers are frozen except for the endpoint controller state machines and the TX_EN, LAST, and RX_EN bits which are reset.

Note 2 In the NodeResume state, resume signaling is propagated upstream.

Note 3 In the NodeSuspend state, the node may enter a low power state and can detect resume signaling.

Table 185: Functional States

State Transition	Condition Asserted
set_NodeReset	Node Functional State register USB_NFS[1:0] bits are written with 00_b The firmware should only initiate set_NodeReset if USB_RESET in the USB_ALTEV_REG register is set.
set_NodeSuspend	Node Functional State register USB_NFS[1:0] bits are written with 11_b The firmware should only initiate set_suspend if USB_SD3 in the USB_ALTEV_REG register is set.
set_NodeOperation	Node Functional State register USB_NFS[1:0] bits are written with 10_b

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State Transition	Condition Asserted
set_NodeResume	Node Functional State register USB_NFS[1:0] bits are written with 01_b The firmware should only initiate clear_suspend if USB_SD5 in the USB_ALTEV_REG register is set.
usb_reset_detect	USB_RESET in the USB_ALTEV_REG register is set to 1.
local_event	A local event that should wake up the USB.
usb_sd5_detect	USB_SD5 in the USB_ALTEV_REG register is set to 1.
usb_suspend_detect	USB_SD3 in the USB_ALTEV_REG register is set to 1.
usb_resume_detect	RESUME in the USB_ALTEV_REG register is set to1.
resume_complete	The node should stay in NodeResume state for at least 10 ms and then must enter NodeOperational state to detect the EOP from the host, which terminates this Remote Resume operation. EOP is signaled when USB_EOP in the USB_ALTEV_REG register is set to 1.

40.2.5 Address Detection

Packets are broadcasted from the host controller to all the nodes on the USB network. Address detection is implemented in hardware to allow selective reception of packets and to permit optimal use of microcontroller bandwidth. One function address with seven different endpoint combinations is decoded in parallel. If a match is found that particular packet is received into the FIFO; otherwise, it is ignored.

Figure 103 shows the block diagram of the function address and endpoint decoding. The incoming USB Token, Packet Address field, and four bits Endpoint field are extracted from the incoming bit stream. The address field is compared to the Function Address register (USB_FAR_REG) and if a match is detected, the USB Endpoint field is compared to all EP bit fields in the Endpoint Control registers (USB_EPCx_REG). The transmit Endpoint Control registers are compared with IN tokens and the receive Endpoint Control registers are compared with OUT tokens. A match then enables the respective endpoint FIFO and transfers the payload data to/from the FIFO. Note that EPC0 is bidirectional and is enabled for IN, OUT, and SETUP tokens.

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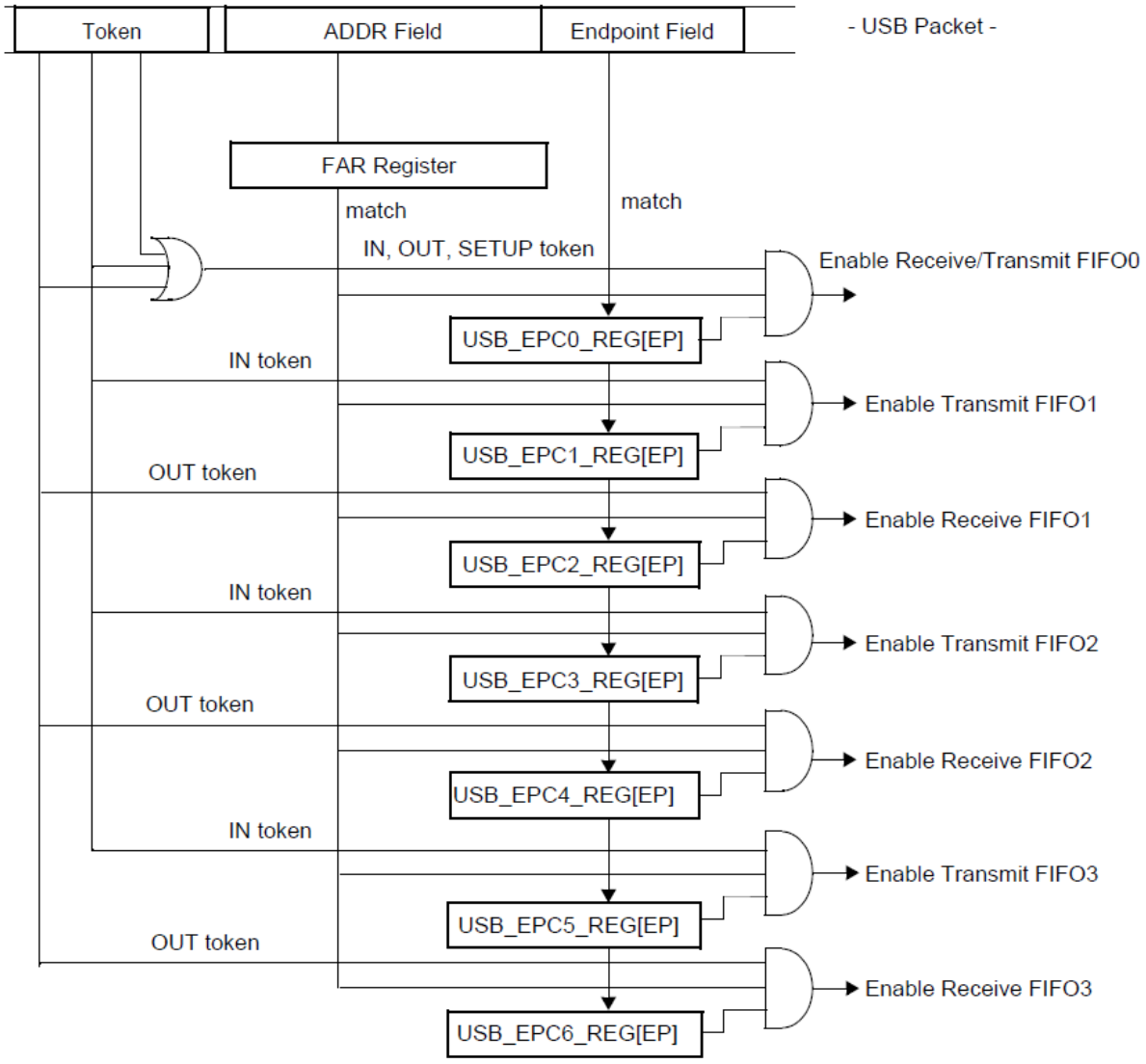

Figure 103: USB Function Address/Endpoint Decoding

40.2.6 Transmit and Receive Endpoint FIFOs

The FS/LS USB node uses a total of seven transmit and receive FIFOs: one bidirectional transmit and receive FIFO for the mandatory control endpoint, three transmit FIFOs, and three receive FIFOs. As shown in Table 186, the bidirectional FIFO for the control endpoint is 64 bytes deep. The additional unidirectional FIFOs are 512 bytes each for both transmit and receive. Each FIFO can be programmed for one exclusive USB endpoint, used together with one globally decoded USB function address. The firmware must not enable both transmit and receive FIFOs for endpoint zero at any given time.

Table 186: USB Node Endpoint Sizes

Endpoint No.	TX FIFO		RX FIFO	
	Size (Bytes)	Name	Size (Bytes)	Name
0	64 FIFO0			
1	512	TXFIFO1 (IN)		
2			512	RXFIFO1 (OUT)

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Endpoint No.	TX FIFO		RX FIFO	
	Size (Bytes)	Name	Size (Bytes)	Name
3	512	TXFIFO2 (IN)		
4			512	RXFIFO2 (OUT)
5	512	TXFIFO3 (IN)		
6			512	RXFIFO3 (OUT)

If two endpoints in the same direction are programmed with the same endpoint number [EP field] and both are enabled, data is received or transmitted to/from the endpoint with the lower number until that endpoint is disabled for bulk or interrupt transfers, or becomes full or empty for ISO transfers. For example, if receive EP1 and receive EP2 both use endpoint 3 and are both isochronous, the first OUT packet is received into EP1 and the second OUT packet into EP2, assuming no firmware interaction in between. For ISO endpoints, this allows implementing a ping-pong buffer scheme together with the frame number match logic. Endpoints in different directions programmed with the same endpoint number operate independently.

40.2.7 Bidirectional Control Endpoint FIFO0

FIFO0 should be used for the bidirectional control endpoint zero. It can be configured to receive data sent to the default address with the USB_DEF bit in the USB_EPC0_REG register.

The Endpoint 0 FIFO can hold a single receive or transmit a packet with up to 64 bytes of data.

NOTE
A packet written to the FIFO is transmitted if an IN token for the respective endpoint is received. If an error condition is detected, the packet data remains in the FIFO and the transmission is retried with the next IN token.

The FIFO contents can be flushed to allow a response to an OUT token or to write new data into the FIFO for the next IN token.

Figure 104 shows the Endpoint 0 state machine. In state TXWAIT, if USB_RXC0_REG[SETUP_FIX] = 0, no state change takes place if a SETUP is received. With SETUP_FIX = 1, the state machine goes to IDLE, flushes to EP0, and receives the token in the RXWAIT state. If a SETUP is received in states TXFILL or RXDRAIN and SETUP_FIX = 1, the SETUP is ignored and no ACK is sent. This allows undisturbed FIFO filling/emptying. This state is usually present for a very short time and forces the host to retransmit the SETUP once. If an OUT token is received for the FIFO, the firmware is informed that the FIFO has received data, only if there was no error condition (CRC or STUFF error). Erroneous receptions are automatically discarded.

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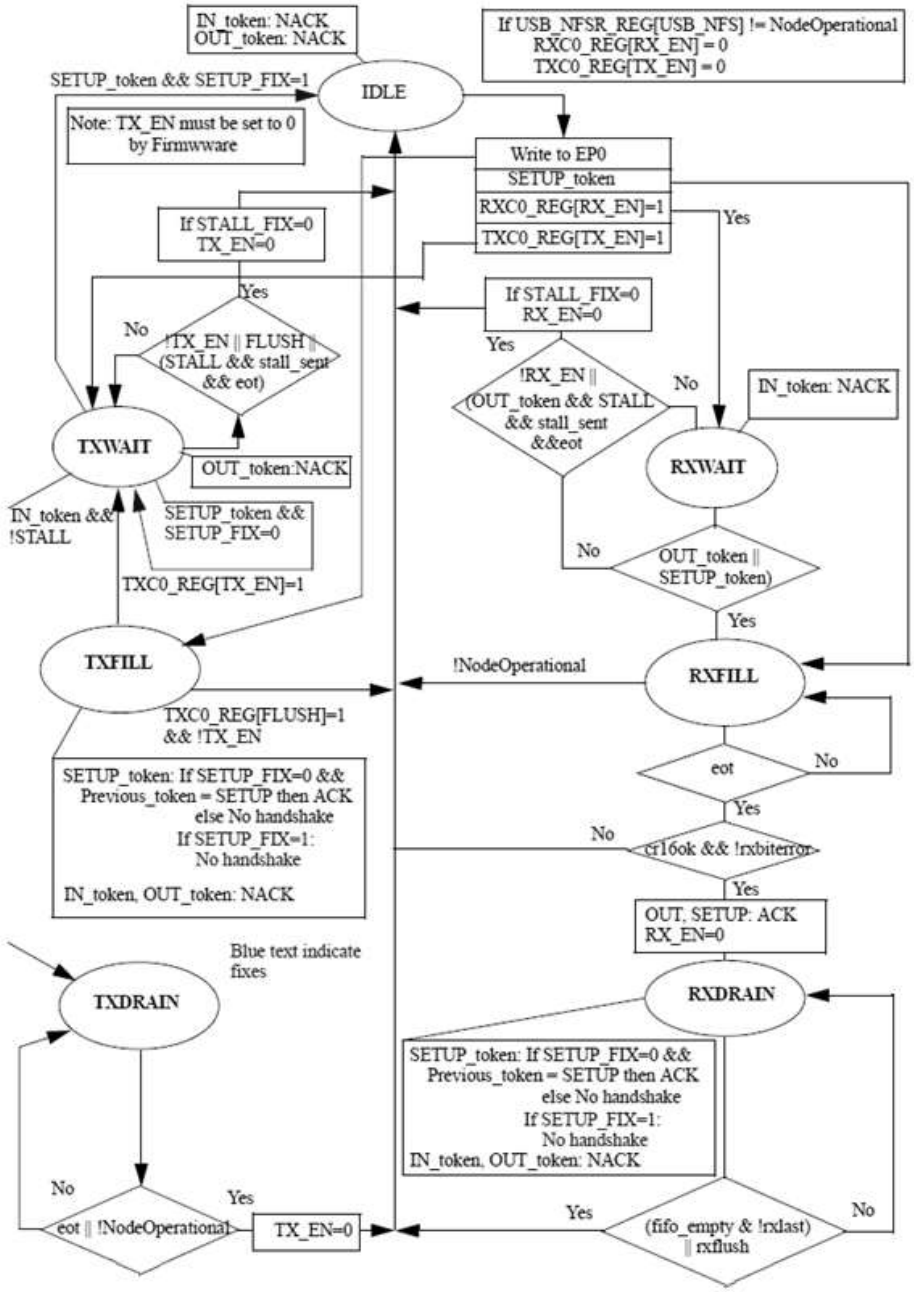

Figure 104: Endpoint 0 Operation

40.2.8 Transmit Endpoint FIFO

The Transmit FIFOs for Endpoints 1, 3, and 5 support bulk and interrupt USB packet transfers larger than the actual FIFO size. Therefore, the firmware must update the FIFO contents while the USB packet is transmitted on the bus.

Figure 105 illustrates the operation of the transmit FIFOs.

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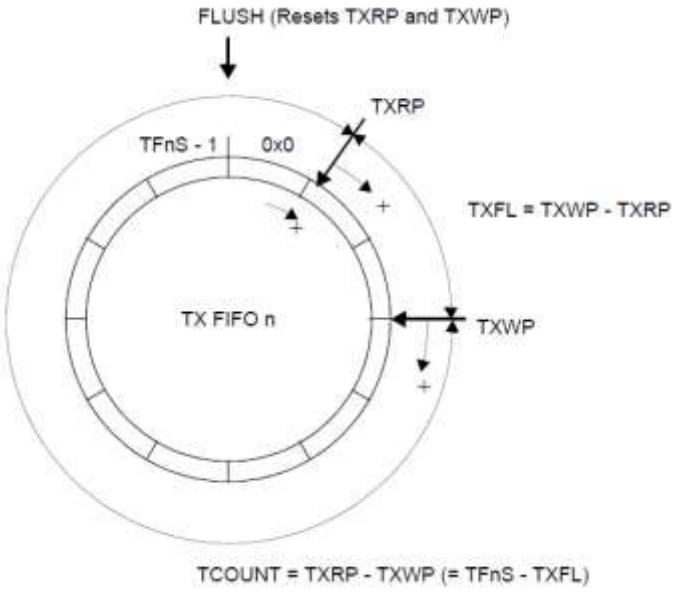

Figure 105: USB Tx FIFO Operation

- **TFnS: Transmit FIFO n Size**

This is the total number of bytes available within the FIFO.

- **TXRP: Transmit Read Pointer**

This pointer is incremented every time the Endpoint Controller reads from the transmit FIFO. This pointer wraps around to zero if TFxS is reached. TXRP is never incremented beyond the value of the write pointer TXWP.

An underrun condition occurs if TXRP equals TXWP and an attempt is made to transmit more bytes when the LAST bit in the USB_TXCx register is not set.

- **TXWP: Transmit Write Pointer**

This pointer is incremented every time the firmware writes to the transmit FIFO. This pointer wraps around to zero if TFnS is reached.

If an attempt is made to write more bytes to the FIFO than the actual space available (FIFO overrun), the write to the FIFO is ignored and TCOUNT is checked for an indication of the number of empty bytes remaining.

- **TXFL: Transmit FIFO Level**

This value indicates how many bytes are currently in the FIFO.

A FIFO warning is issued if TXFL decreases to a specific value. The respective WARNn bit in the FWR register is set if TXFL is equal to or less than the number specified by the TFWL bit in the TXCn register.

- **TCOUNT: Transmit FIFO Count**

This value indicates how many empty bytes can be filled within the transmit FIFO. This value is accessible by firmware via the TXSn register.

40.2.9 Receive Endpoint FIFO

The Receive FIFOs for Endpoints 2, 4, and 6 support bulk and interrupt USB packet transfers larger than the actual FIFO size. If the packet length exceeds the FIFO size, the firmware must read the FIFO contents while the USB packet is being received on the bus.

Figure 106 illustrates the operation of the receive FIFOs.

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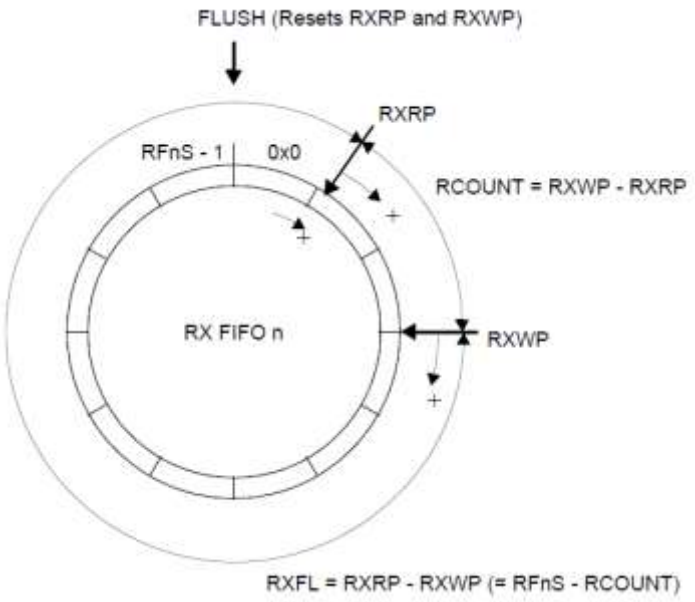

Figure 106: USB Rx FIFO Operation

- **RFnS: Receive FIFO n Size**

This is the total number of bytes available within the FIFO.

- **RXRP: Receive Read Pointer**

This pointer is incremented with every read of the firmware from the receive FIFO. This pointer wraps around to zero if RFnS is reached. RXRP is never incremented beyond the value of RXWP.

If an attempt is made to read more bytes than actually available bytes (FIFO underrun), the last byte is read repeatedly.

- **RXWP: Receive Write Pointer**

This pointer is incremented every time the Endpoint Controller writes to the receive FIFO. This pointer wraps around to zero if RFnS is reached.

An overrun condition occurs if RXRP equals RXWP and an attempt is made to write an additional byte.

- **RXFL: Receive FIFO Level**

This value indicates how many more bytes can be received until an overrun condition occurs with the next write to the FIFO.

A FIFO warning is issued if RXFL decreases to a specific value. The respective WARNn bit in the FWR register is set if RXFL is equal to or less than the number specified by the RFWL bit in the RXCn register.

- **RCOUNT: Receive FIFO Count**

This value indicates how many bytes can be read from the receive FIFO. This value is accessible by firmware via the RXSn register.

40.2.10 Interrupt Hierarchy

Figure 107 shows the register hierarchy for generating USB interrupt events. Each bit in the event register can be masked by setting the corresponding bit in the xxxMSK_REG. A USBFS_IRQ to the CPU is generated if one or more bits in the MAEV_REG are set and the corresponding bits in the MAMSK_REG are set to 1. Bit 7 in the MAMSK_REG is a global interrupt that is enabled for the USBFS_IRQ.

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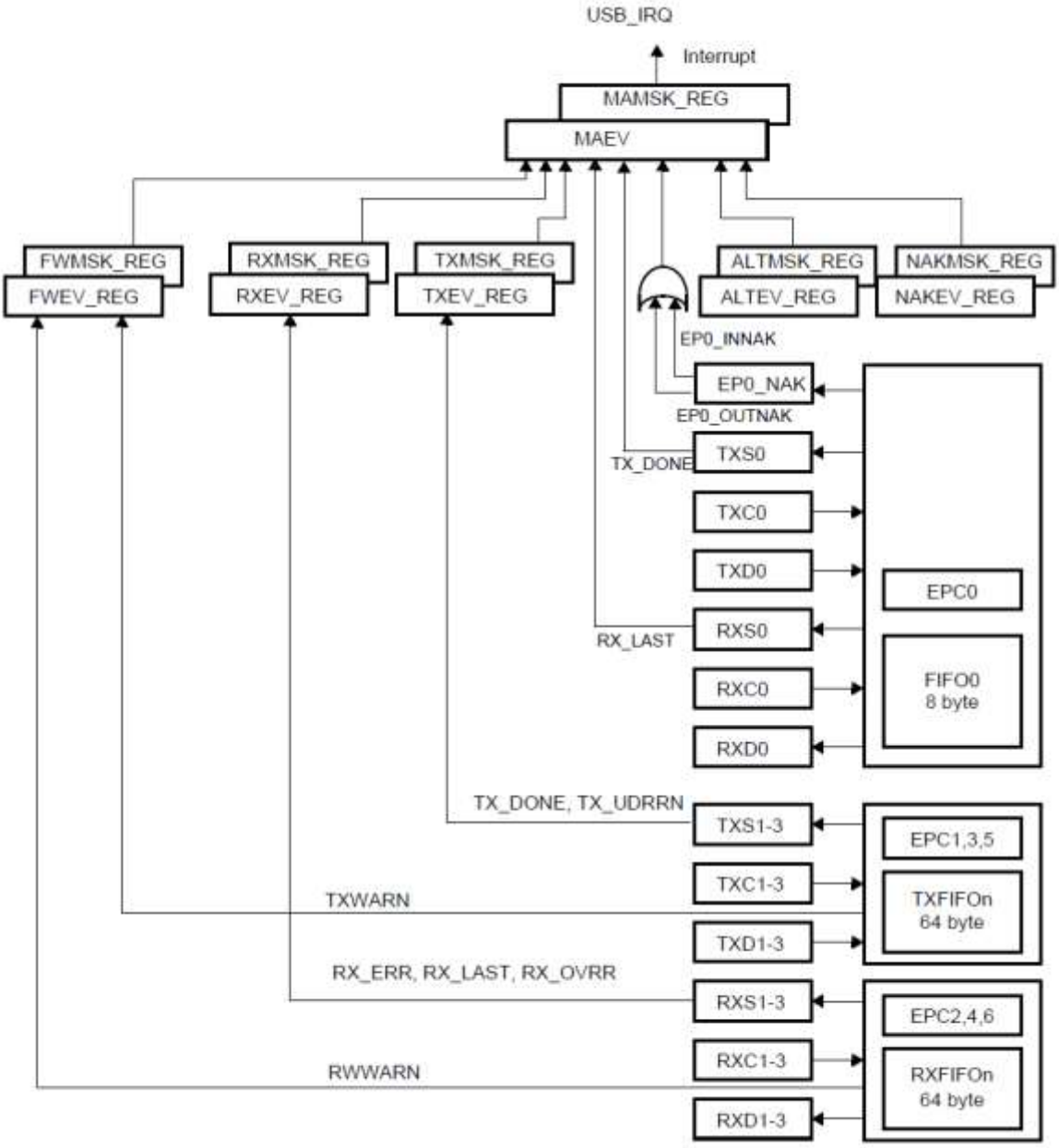

Figure 107: USB Interrupt Register Hierarchy

40.2.11 USB Power Saving Modes

In the NodeSuspend state, the USB transceiver is automatically switched to a low-power mode. Optimal power-saving rest of the chip level can be obtained by:

- Executing from on-chip RAM or ROM. On-chip access is more power-efficient than external memory access. With external FLASH, appropriate gating of the chip selects may be applied
- Switching USB input clock from PLL48M to DivN (CLK_CTRL_REG[USB_CLK_SRC] = 1)
- Switching the PLL48M off (PLL_USB_CTRL1_REG[PLL_EN] = 0)

In suspend mode, any activity on the USB generates the USB_ALTEV_REG[USB_RESUME] interrupt.

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The firmware must respond by:

- Starting the PLL48M and switching the USB input clock from DivN to PLL48M (CLK_CTRL_REG[USB_CLK_SRC] = 0)
- Re-enabling all functions and settings that have been turned off to reduce the currents in suspend mode

Note that the total time needed to bring the USB module back to operational mode is determined by the PLL startup time.

The CPU resumes normal operation after the USB_NFSR_REG register is set in NodeOperational state.

40.2.11.1 Freezing USB Node

The USB module provides support for an In-System-Emulator. If SET_FREEZE_REG[FRZ_USB] is set, the USB module exhibits the following behaviors:

- The automatic Clear-on-Read function of status flags is disabled
- The FIFOs are not updated

To enable the module, the RESET_FREEZE_REG[FRZ_USB] must be set to 1 again.

40.2.11.2 Integrated Resistors

The USB transceiver has integrated resistors as specified in *USB Specification 2.0 ECN "pull-up/pull-down resistors"*.

The resistors switching can be overruled as shown in Figure 108 and Figure 109, if USB_UX20CDR_REG[RPU_TEST_EN] = 1.

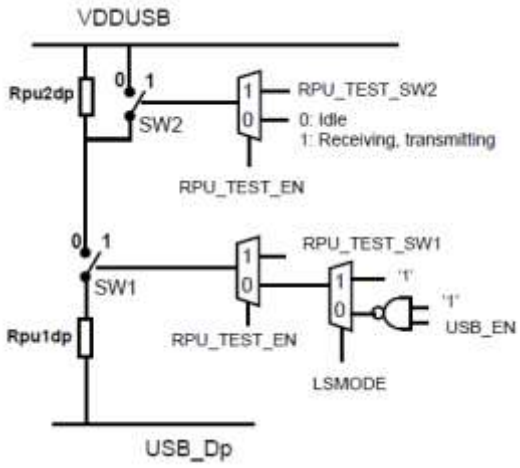

Figure 108: USB_Dp Resistor Switching

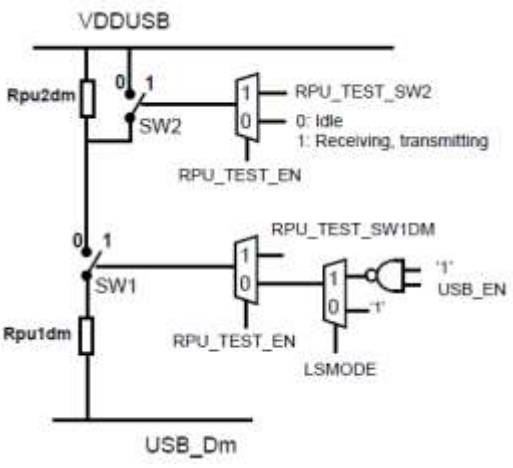

Figure 109: USB_Dm Resistor Switching

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41 LEDs Driver

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

41.1 Introduction

The LED driver features three matched white LED outputs with an absolute accuracy of +/- 5 % (at 25 °C). It supports two solutions for brightness dimming: a selectable output load current and PWM dimming.

The selectable output load is a dimming mode that changes the brightness by changing/reducing the maximum output current. It is controlled by three bits (eight possible settings). The minimum setting is 2.5 mA with an increment of 2.5 mA, so maximal 20 mA. The reduced current settings are especially interesting to be used as a coarse brightness control for short pulses, for example, for a heart rate monitor application.

PWM dimming changes the brightness by modulating the output current from 0 % to 100 % duty-adjustable pulse. The LED brightness is controlled by adjusting the relative ratios of the on and off times. Since the dimming frequency (timer operating on the low power clock) is higher than the human-eye sensitive range (>100 Hz), the effective brightness is perceived by averaging the on and off times. The PWM operation is possible for all eight load settings instead of just the maximum setting.

NOTE
The LED driver cannot operate in any of the sleep modes.

The block diagram of just one driver is presented in Figure 110. Three of these are instantiated in the system.

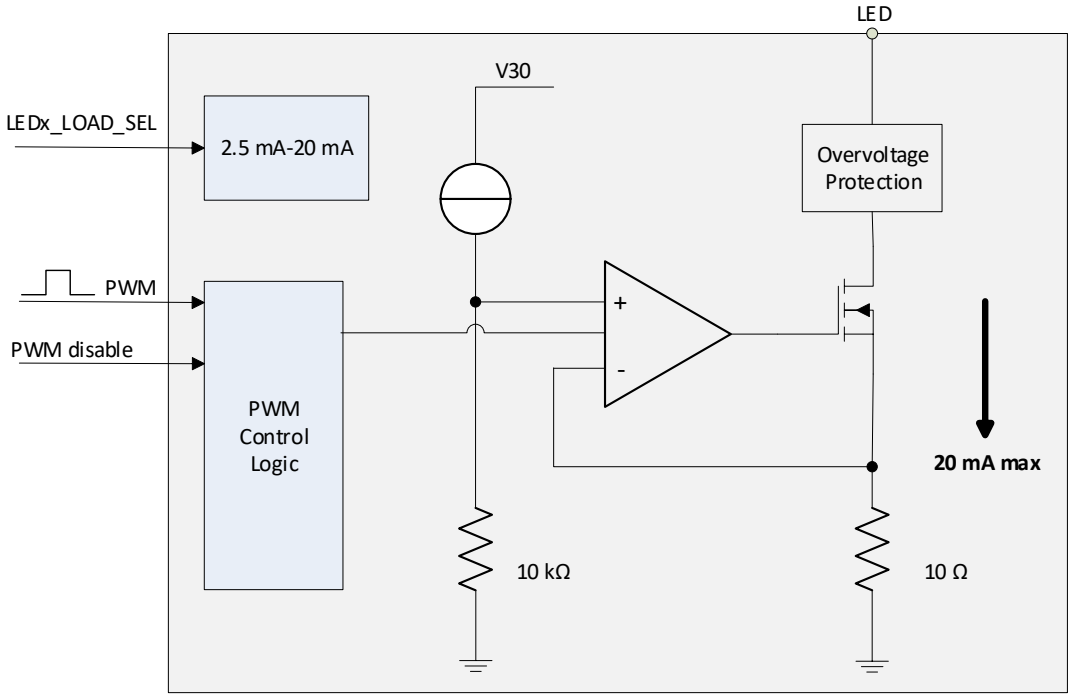

Figure 110: LED Driver Block Diagram

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41.2 Architecture

The LED driver contains the following functional blocks:

- Output load setting. Input is an accurate reference current from a bandgap, and outputs are various (mirrored) currents
- High gain op-amp
- Matched resistor network
- PWM control logic
- Overvoltage protection

A reference current, coming from the bandgap, is mirrored into selectable output current(s). This current is routed through a resistor, resulting in a reference voltage on the positive input of the op-amp. Due to the negative feedback and the high gain, the op-amp in combination with the output transistor forces the same voltage on the negative input and over the output resistor, resulting in the selected output load current. The overvoltage protection shields the LED driver from excessive high voltages, which can be up to VBUS max, on the LED pins.

41.3 Programming

There is a simple sequence of steps that needs to be followed to program the LED drivers:

1. Define the PWM frequency and duty cycle for each LED driver by configuring LED1/2/3_PWM_CONF_REG and LEDS_FREQUENCY_REG. Note that it is possible to use different duty cycles for the two drivers, however, they share the same frequency configuration register.
2. Configure the sinking current by programming LED_LOAD_SEL_REG[LEDx_LOAD_SEL]. This defines the sinking current according to the following formula:

$$I_{LED(sink)} = 2.5\ mA + (LEDx\_LOAD\_SEL \times 2.5\ mA) \quad (2)$$

3. Enable the LED drivers by asserting LEDS_DRV_CTRL_REG[LED1_EN, LED2_EN, LED3_EN].
4. Activate PWM by asserting LEDS_PWM_CTRL_REG[LED1_PWM_ENABLE, LED2_PWM_ENABLE, LED3_PWM_ENABLE].

Note that the PWM can be stopped by writing to either SET_FREEZE_REG[FRZ_PWMLED] or LEDS_PWM_CTRL_REG[PWM_LEDS_SW_PAUSE]. Furthermore, the control logic of the LEDs resides in PD_TMR. PD_SNC can be switched off during sleep with no impact on the LEDs operation.

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42 Input/Output Ports

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

42.1 Introduction

The DA1470x has software-configurable input/output (I/O) pin assignment organized into ports Port 0, Port 1, and Port 2.

Features

- Port 0 and Port 1 have 32 pins each, and Port 2 has 15 pins (including M33_SWCLK, M33_SWDIO, CMAC_SWCLK, CMAC_SWDIO, SNC_SWCLK, and SNC_SWDIO)
- Fully programmable pin assignment (PPA)
- Selectable 25 kΩ pull-up/pull-down resistors per pin
- Programmable open-drain functionality
- Pull-up voltage at V30/V18P voltage configurable per pin
- Fixed assignment for analog, Display Controller, eMMC, I3C, and SPI3 pins
- Pins retainability when system enters the Extended Sleep mode

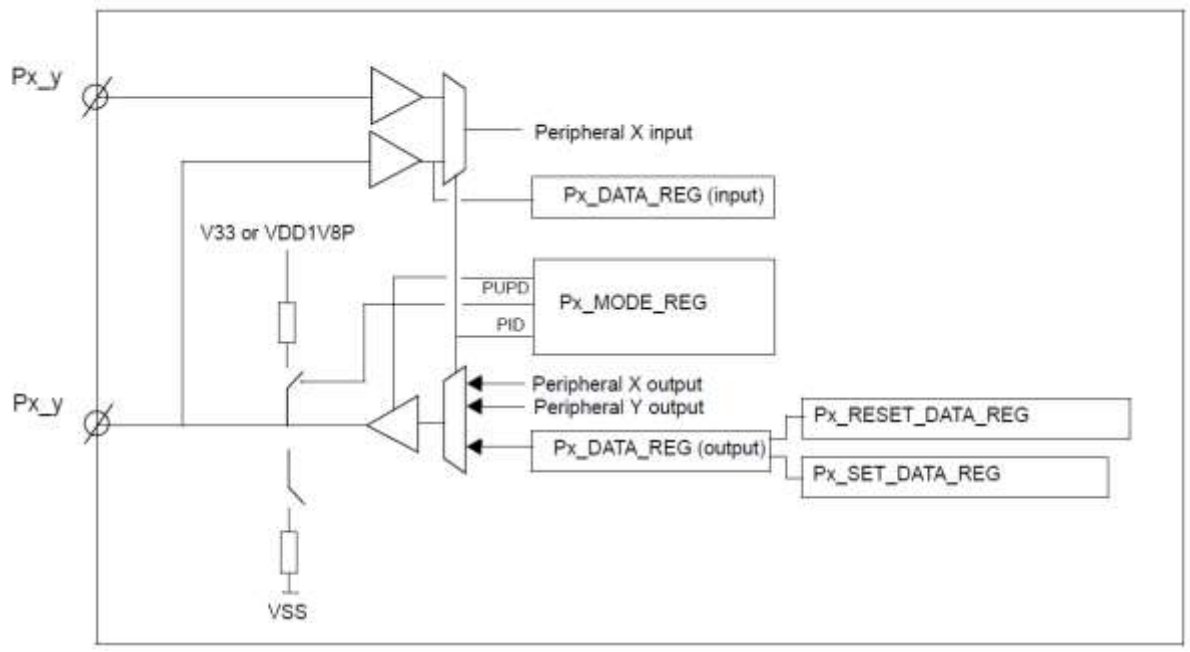

Figure 111: Port P0, P1, and P2 with Programmable Pin Assignment

42.2 Architecture

42.2.1 Programmable Pin Assignment

The Programmable Pin Assignment (PPA) provides a multiplexing function to the I/O pins of on-chip peripherals. Any peripheral input or output signals can be freely mapped to any I/O port bit by setting Px_yy_MODE_REG[5:0]

```
0x00 to 0x3B: Peripheral IO ID (PID)
```

Refer to the Px_yy_MODE_REGs for an overview of the available PIDs. Analog, GPADC, SDADC/PGA signals have fixed pin assignment to limit interference with the digital domain. The

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same applies to Display Controller, eMMC, I3C, and SPI3 controllers' signals. The ARM M33 SWD interface is mapped on P0_00 and P0_01, the CMAC SWD interface on P0_04 and P0_07, and the SNC SWD interface on P0_02 and P0_03.

42.2.1.1 Priority

The firmware can assign the same peripheral output to more than one pin. It is the users' responsibility to make a unique assignment.

If more than one input signal is assigned to a peripheral input, the leftmost pin in the lowest port pin number has priority, for example, P0_00_MODE_REG has priority over P0_01_MODE_REG.

42.2.1.2 Direction Control

The port direction is controlled by setting Pxy_MODE_REG[9:8]. In output mode and analog mode, the pull-up/down resistors are automatically disabled.

42.2.2 General Purpose Port Registers

The general-purpose ports are selected with PID = 0. The port function is accessible through registers:

- Px_DATA_REG: Port data input/output register
- Px_SET_OUTPUT_DATA_REG: Port set output register
- Px_RESET_OUTPUT_DATA_REG: Port reset output register

42.2.2.1 Port Data Register

The registers input Px_DATA_REG and output Px_DATA_REG are mapped on the same address.

The data input register (Px_DATA_REG) is a read-only register that returns the current state on each port pin even if the output direction is selected, regardless of the programmed PID, unless the analog function is selected (in this case it reads 0). The Cortex-M33 CPU can read this register at any time even when the pin is configured as an output.

The data output register (Px_DATA_REG) holds the data to be driven on the output port pins. In this configuration, writing to the register changes the output value.

42.2.2.2 Port Set Data Output Register

Writing a 1 in the set data output register (Px_SET_DATA_REG) sets the corresponding output pin. Writing a 0 is ignored.

42.2.2.3 Port Reset Data Output Register

Writing a 1 in the reset data output register (Px_RESET_DATA_REG) resets the corresponding output pin. Writing a 0 is ignored.

42.2.3 Fixed Assignment Functionality

There are certain signals that have a fixed mapping on specific general-purpose IOs. This assignment is illustrated in the following tables.

Table 187: Debug I/F Signals

GPIO	Debug I/F Signal (Note 1)	GPIO	Debug I/F Signal (Note 1)
P0_00	M33_SWDIO	P0_31	TRACE_CLK
P0_01	M33_SWDCLK	P1_22	TRACE_DATA[1]
P0_02	SNC_SWDIO	P1_23	TRACE_DATA[3]

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GPIO	Debug I/F Signal (Note 1)	GPIO	Debug I/F Signal (Note 1)
P0_03	SNC_SWDCLK	P1_30	TRACE_DATA[0]
P0_04	CMAC_SWDIO	P1_31	TRACE_DATA[2]
P0_07	CMAC_SWDCLK		

Note 1 The SWD signals mapping is defined by SYS_CTRL_REG[DEBUGGER_ENABLE], SYS_CTRL_REG[CMAC_DEBUGGER_ENABLE] and SYS_CTRL_REG[SNC_DEBUGGER_ENABLE]. However, these signals are mapped on the ports by default.

Table 188: Quad SPI Controllers

GPIO	Q-SPI Controllers	GPIO	Q-SPI Controllers
P1_09	QSPIC_D0	P1_24	QSPIC2_CS
P1_13	QSPIC2_D2	P1_25	QSPIC_CS
P1_14	QSPIC2_D1	P1_26	QSPIC_CLK
P1_15	QSPIC2_D0	P1_27	QSPIC_D1
P1_17	QSPIC_D3	P2_04	OQSPIF_D4
P1_18	QSPIC_D2	P2_05	OQSPIF_D5
P1_19	QSPIC2_CLK	P2_06	OQSPIF_D6
P1_20	QSPIC2_D3	P2_07	OQSPIF_D7

Table 189: Analog Functions Signals

GPIO	Analog (Note 1)	GPIO	Analog (Note 1)
P0_05	GPADC1	P0_30	GPADC4
P0_06	GPADC2	P1_05	SDADCp/ PGAp
P0_11	NTC Supply	P1_06	SDADCm/ PGAm
P0_27	GPADC3	P2_08	XTAL32km
P0_29	NTC Sense	P2_09	XTAL32kp

Note 1 The ADC case can be selected by the PID bit field on the respective Px port.

Table 190: Internal Clocks Outputs

GPIO	Clocks Ouputs (Note 1)
P0_09	XTAL32M
P0_20	DIVN
P0_31	XTAL32k
P1_22	RCX
P1_23	RCLP

Note 1 Enable specific clock outputs through GPIO_CLK_SEL_REG register.

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Table 191: External Serial and Parallel I/Fs Signals

GPIO	I3C/SPI3/USB	GPIO	eMMC
P1_11	I3C_SDA	P0_25	eMMC_CLK
P1_12	I3C_SCL	P0_26	eMMC_CMD
P1_28	SPI3_CLK	P1_02	eMMC_D0
P2_00	SPI3_DI	P1_08	eMMC_D3
P2_02	SPI3_DO	P1_09	eMMC_D2
P2_10	USBp	P1_10	eMMC_D1
P2_11	USBm	P1_16	eMMC_D6
		P1_17	eMMC_D5
		P1_18	eMMC_D4
		P1_21	eMMC_RST
		P2_03	eMMC_D7

Table 192: SPI Display I/F Signals

GPIO	JDI Parallel	SPI Display
P0_09	VCK	
P0_10	XFRP	LCD_TE
P0_14	HCK	LCD_SPI_SCLK
P0_15	HST	LCD_SPI_SD/SI
P0_16	VST	LCD_SPI_SD1/DC
P0_17	RED0	LCD_SPI_SD3
P0_18	ENB	LCD_CS
P0_19	VCOM/FRP	EXTCOMIN
P0_21	BLUE1	
P0_22	XRST	LCD_SPI_SD2
P0_23	RED1	
P0_24	GREEN0	
P1_00	GREEN1	
P1_01	BLUE0	

Table 193: Special Functions Signals

GPIO	Special (Note 1)	GPIO	Special (Note 1)
P0_08	UART Boot TX	P0_20	Hibernation WU1
P2_01	UART Boot RX	P0_28	Hibernation WU4
P0_30	Timer.PWM	P0_29	Hibernation WU2
P1_30	Timer3.PWM	P1_04	Hibernation WU3
P1_31	Timer4.PWM		

Note 1 Timer.PWMx signals are available during sleep (See CLK_TMR_REG register).

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Table 194: Diagnostics Signals

GPIO	Diagnostics (Note 1)	GPIO	Diagnostics (Note 1)
P0_14	CMAC_DIAG_0	P1_00	CMAC_DIAG_9
P0_15	CMAC_DIAG_2	P1_01	CMAC_DIAG_10
P0_16	CMAC_DIAG_3	P1_02	CMAC_DIAG_1
P0_20	BANDGAP_ENABLE (Note 2)	P1_04	WOKENUP or CMAC_SLP_TIMER_EXPIRE (Note 2)
P0_21	CMAC_DIAG_11	P1_07	CMAC_DIAG_13
P0_22	CMAC_DIAG_4	P1_08	CMAC_DIAG_14
P0_23	CMAC_DIAG_7	P1_10	CMAC_DIAG_5
P0_24	CMAC_DIAG_8	P1_16	CMAC_DIAG_6
P0_25	CMAC_DIAG_12	P2_03	CMAC_DIAG_15

Note 1 For a complete functionality description of the CMAC diagnostics, see Section 14.

Note 2 SLP_MAP_REG[BANDGAP_SLP_MAP].

42.2.4 GPIO State Retention While Sleeping

Before setting the system to any sleep modes, the state of the pads needs to be retained to avoid external components being affected by the GPIOs changing states when the system goes to sleep and to avoid any floating driving signals from shut-off power domains leading to increasing power dissipation.

The state of the pads is automatically latched by always-on latches by setting the corresponding PAD_LATCH_EN bit in the Px_RESET_PAD_LATCH_REG. These bits latch the digital control signals going into the pad and latch the data output separately for each pin. Hence, if the pad has been set as an output driving high, it retains its precise state. Px_SET_PAD_LATCH_REG is used to unlatch the pins.

The signals in red in Figure 112 and Figure 113 are latched.

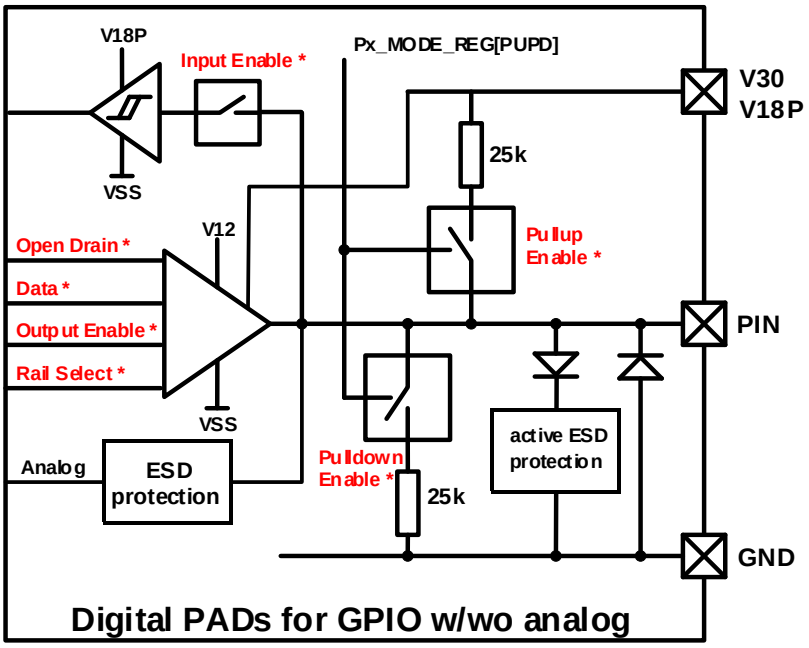

Figure 112: Latching of Digital Pad Signals

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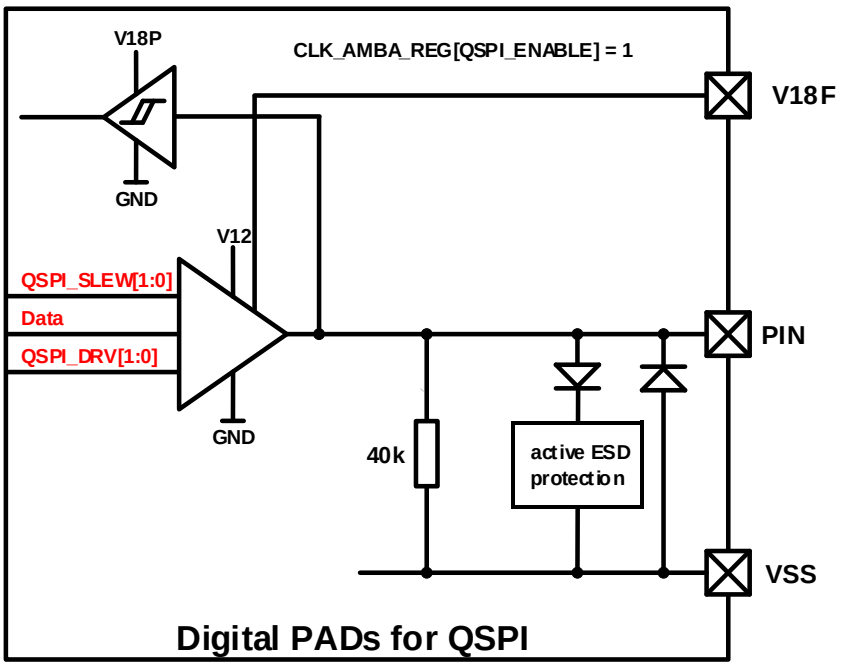

Figure 113: Latching of QSPI Pad Signals

After the system waking up, the software must disable the latching by setting the corresponding PAD_LATCH_EN bits of the Px_PAD_LATCH_REG so that all pads can be accessed and controlled again.

For QSPI pads, the pad latching is overwritten by the QSPI controller as soon as the clock of the controller is enabled.

42.2.5 Special I/O Considerations

There are certain considerations in using the GPIOs:

- To use P2_10 or P2_11 in GPIO mode, USBPAD_REG[USBPAD_EN] must be set. However, the levels allowed on these pins are 0 V and 3 V. The voltage comes from the V30 rail. If 1.8 V is selected as the pin supply, a current of 150 µA is to be expected. Moreover, these pins should not be used in sleep modes, because the USBPAD_REG which belongs to the system power domain is powered off in sleep modes and those pins do not support state retention during power down

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43 Radio

Device	DA14701	DA14705	DA14706	DA14708
Feature Availability	✓	✓	✓	✓

43.1 Introduction

The Radio Transceiver provides a 103 dB RF link budget for reliable wireless communications. All RF blocks are supplied by on-chip low dropout regulators (LDOs). The bias scheme is programmable and optimized for minimum power consumption. The radio block diagram is given in Figure 114. It comprises the Receiver, Transmitter, Synthesizer, Rx/Tx combiner block, and Biasing LDOs.

Features

- Single-ended RFIO interface, 50 Ω matched
- Alignment free operation
- -97 dBm receiver sensitivity
- Configurable transmit output power from -18 dBm up to 6 dBm
- Ultra-low power consumption
- Fast frequency tuning minimizes overhead

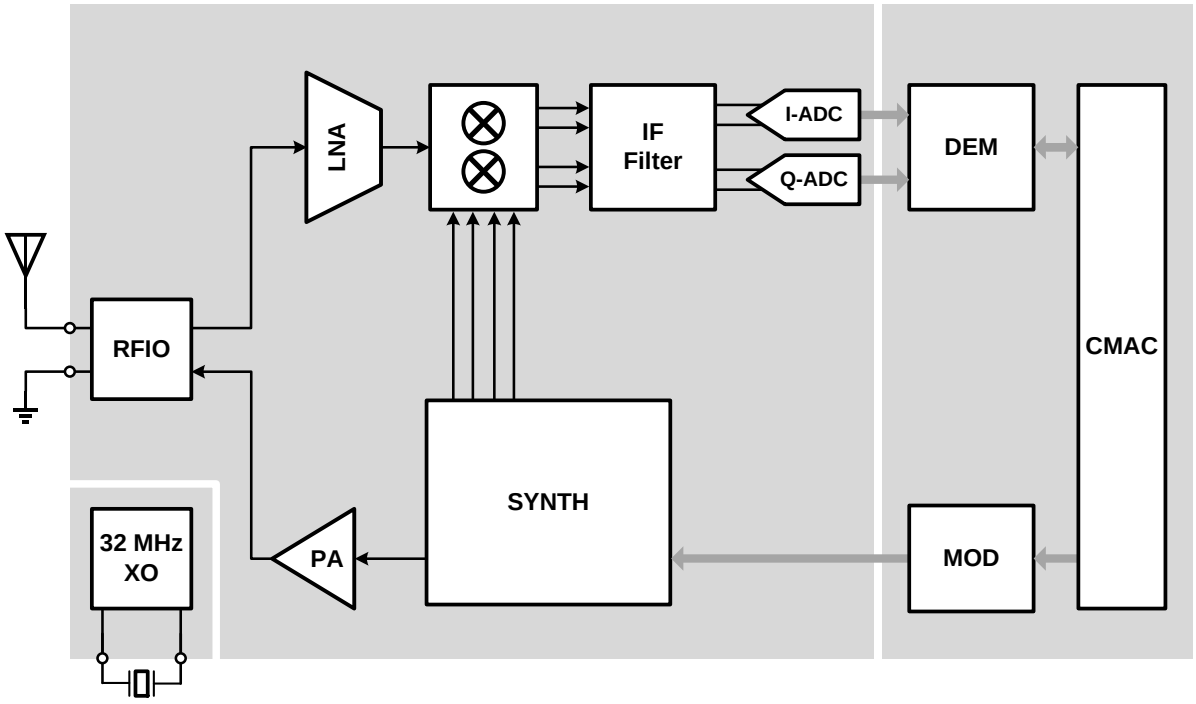

Figure 114: Radio Block Diagram

43.2 Architecture

43.2.1 Receiver

The RX frontend consists of a selective matching network, a low noise amplifier (LNA), and an image rejection down conversion mixer. The intermediate frequency (IF) part of the receiver comprises a filter with programmable gain. The LNA and IF Filter gains are controlled by the AGC. This provides the necessary signal conditioning prior to digitalization. The digital demodulator block (DEM) provides a synchronous bit stream.

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43.2.2 Synthesizer

The RF synthesizer generates the quadrature LO signal for the mixer. It also generates the modulated TX output signal. The DCO runs at twice the required frequency and a dedicated divide-by-two circuit generates the 2.4 GHz signals in the required phase relations. The reference frequency is the 32 MHz crystal clock. The modulation of the TX frequency is performed by two-point modulation.

43.2.3 Transmitter

The RF power amplifier (RFPA) is an extremely efficient Class-D structure, providing typically -18 dBm to +6 dBm to the antenna. It is fed by the VCO's divide-by-two circuit and delivers its TX power to the antenna pin through the combined RX/TX matching circuit.

43.2.4 RFIO

The RX/TX combiner block is a unique feature of the DA1470x. It makes sure that the received power is applied to the LNA with minimum losses towards the RFPA. In TX mode, the LNA poses a minimal load for the RFPA and its input pins are protected from the RFPA. In both modes, the single-ended RFIO port is matched to 50 Ω to provide the simplest possible interfacing to the antenna on the printed circuit board.

43.2.5 Biasing

All RF blocks are supplied by on-chip low dropout regulators (LDOs). The bias scheme is programmable and optimized for minimum power consumption.

43.2.6 RF Monitoring

The radio is equipped with a monitoring block, of which the responsibility is to acquire the data provided by the functional RF Units and other various analog resources and the packing of the data in words of 32 bits (when necessary), and to store them in system's memory, to achieve the production test of the corresponding blocks. The data can be the output of the Demodulator (I and Q) and the data provided by the GPADC.

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44 Registers

This section contains a detailed view of the DA1470x registers. It is organized as follows:

- An overview table is presented initially, which depicts all register names, addresses and descriptions
- A detailed bit level description of each register follows

The register file of the ARM Cortex-M33 and ARM Cortex-M0+ can be found in the following documents, available on the ARM website:

Devices Generic User Guide:
arm_cortex_m33_dgug_100235_0002_00_en.pdf
DUI0662B_cortex_m0p_r0p1_dgug.pdf

Technical Reference Manual:
Cortex_m33_trm_100230_0002_00_en.pdf
DDI0484C_cortex_m0p_r0p1_trm.pdf

These documents contain the register descriptions for the Nested Vectored Interrupt Controller (NVIC), the System Control Block (SCB) and the System Timer (SysTick).

44.1 AMBA Bus Registers

Table 195: Register map AMBA

Address	Register	Description
0x30020000	AHB_DMA_PL1_REG	AHB-DMA layer priority level LCD
0x30020004	AHB_DMA_PL2_REG	AHB-DMA layer priority level GPU
0x30020008	AHB_DMA_PL3_REG	AHB-DMA layer Priority level GEN-DMA
0x3002000C	AHB_DMA_PL4_REG	AHB-DMA layer Priority level CRYPTO-DMA
0x30020010	AHB_DMA_PL5_REG	AHB-DMA layer Priority level MMC
0x30020018	AHB_DMA_PL7_REG	AHB-DMA layer Priority level AHB-S to AHB_DMA arbiter registers
0x30020048	AHB_DMA_DFLT_MASTER_REG	Default master ID number (AHB DMA layer only)
0x3002004C	AHB_DMA_WTEN_REG	Weighted-Token Arbitration Scheme Enable (AHB DMA layer only)
0x30020050	AHB_DMA_TCL_REG	Master clock refresh period (AHB DMA layer only)
0x30020054	AHB_DMA_CCLM1_REG	LCD Master clock tokens
0x30020058	AHB_DMA_CCLM2_REG	GPU Master clock tokens
0x3002005C	AHB_DMA_CCLM3_REG	GEN-DMA Master clock tokens
0x30020060	AHB_DMA_CCLM4_REG	CRYPTO-DMA Master clock tokens
0x30020064	AHB_DMA_CCLM5_REG	MMC Master clock tokens
0x3002006C	AHB_DMA_CCLM7_REG	AHB-S Master clock tokens
0x30020090	AHB_DMA_VERSION_REG	Version ID (AHB DMA layer only)

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Table 196: AHB_DMA_PL1_REG (0x30020000)

Bit	Mode	Symbol	Description	Reset
31:4	R	-	Reserved	0x0
3:0	R/W	AHB_DMA_PL1	Arbitration priority for master LCD. 0 : disables the master 1 : lowest ... 15: highest	0xF

Table 197: AHB_DMA_PL2_REG (0x30020004)

Bit	Mode	Symbol	Description	Reset
31:4	R	-	Reserved	0x0
3:0	R/W	AHB_DMA_PL2	Arbitration priority for master GPU. 0 : disables the master 1 : lowest ... 15: highest	0xE

Table 198: AHB_DMA_PL3_REG (0x30020008)

Bit	Mode	Symbol	Description	Reset
31:4	R	-	Reserved	0x0
3:0	R/W	AHB_DMA_PL3	Arbitration priority for master GEN-DMA. 0 : disables the master 1 : lowest ... 15: highest	0xD

Table 199: AHB_DMA_PL4_REG (0x3002000C)

Bit	Mode	Symbol	Description	Reset
31:4	R	-	Reserved	0x0
3:0	R/W	AHB_DMA_PL4	Arbitration priority for master CRYPTO-DMA. 0 : disables the master 1 : lowest ... 15: highest	0xC

Table 200: AHB_DMA_PL5_REG (0x30020010)

Bit	Mode	Symbol	Description	Reset
31:4	R	-	Reserved	0x0
3:0	R/W	AHB_DMA_PL5	Arbitration priority for master MMC. 0 : disables the master 1 : lowest ...15: highest	0xB

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Table 201: AHB_DMA_PL7_REG (0x30020018)

Bit	Mode	Symbol	Description	Reset
31:4	R	-	Reserved	0x0
3:0	R/W	AHB_DMA_PL7	Arbitration priority for master AHB-S. 1: lowest, 15: highest.	0x9

Table 202: AHB_DMA_DFLT_MASTER_REG (0x30020048)

Bit	Mode	Symbol	Description	Reset
31:4	R	-	Reserved	0x0
3:0	R/W	AHB_DMA_DFLT_MASTER	Default master ID number register. The default master is the master that is granted by the bus when no master has requested ownership. 0: Dummy master 1: LCD 2: GPU 3: GEN-DMA 4: CRYPTO-DMA 5: MMC 6: reserved	0x0

Table 203: AHB_DMA_WTEN_REG (0x3002004C)

Bit	Mode	Symbol	Description	Reset
31:1	R	-	Reserved	0x0
0	R/W	AHB_DMA_WTEN	Weighted-token arbitration scheme enable.	0x0

Table 204: AHB_DMA_TCL_REG (0x30020050)

Bit	Mode	Symbol	Description	Reset
31:16	R	-	Reserved	0x0
15:0	R/W	AHB_DMA_TCL	Master clock refresh period, counting clock cycles. An arbitration period is defined over this number of tokens. When a new arbitration period starts, the master counters are reloaded. Recommended value is the sum of the AHB_DMA_CCLMx_REG valuesplus 2 tokens for each master.	0xFFFF

Table 205: AHB_DMA_CCLM1_REG (0x30020054)

Bit	Mode	Symbol	Description	Reset
31:16	R	-	Reserved	0x0
15:0	R/W	AHB_DMA_CCLM	Number of tokens (counted in AHB clock cycles) that a master can use on the bus before it has to arbitrate on a bus master with low priority and having tokens. Masters with tokens remaining	0xF

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Bit	Mode	Symbol	Description	Reset
			have priority over masters that have used all of their tokens. User should configure all the token values ensuring that the sum does not exceed the total allocated number of tokens. If a value of zero is configured, then the bus is deemed to have infinite tokens and will always operate in the upper-tier of arbitration.	

Table 206: AHB_DMA_CCLM2_REG (0x30020058)

Bit	Mode	Symbol	Description	Reset
31:16	R	-	Reserved	0x0
15:0	R/W	AHB_DMA_CCLM	Refer to AHB_DMA_CCLM1_REG	0xF

Table 207: AHB_DMA_CCLM3_REG (0x3002005C)

Bit	Mode	Symbol	Description	Reset
31:16	R	-	Reserved	0x0
15:0	R/W	AHB_DMA_CCLM	AHB_DMA_CCLM1_REG	0xF

Table 208: AHB_DMA_CCLM4_REG (0x30020060)

Bit	Mode	Symbol	Description	Reset
31:16	R	-	Reserved	0x0
15:0	R/W	AHB_DMA_CCLM	AHB_DMA_CCLM1_REG	0xF

Table 209: AHB_DMA_CCLM5_REG (0x30020064)

Bit	Mode	Symbol	Description	Reset
31:16	R	-	Reserved	0x0
15:0	R/W	AHB_DMA_CCLM	AHB_DMA_CCLM1_REG	0xF

Table 210: AHB_DMA_CCLM7_REG (0x3002006C)

Bit	Mode	Symbol	Description	Reset
31:16	R	-	Reserved	0x0
15:0	R/W	AHB_DMA_CCLM	AHB_DMA_CCLM1_REG	0xF

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Table 211: AHB_DMA_VERSION_REG (0x30020090)

Bit	Mode	Symbol	Description	Reset
31:0	R	AHB_DMA_VERSION		0x3231342A

Table 212: Register map SYSBUS_ICM

Address	Register	Description
0x50040600	QSPIFL2_ARB_REG	
0x50040604	QSPIRAM_ARB_REG	
0x50040608	AHBREG_ARB_REG	
0x5004060C	APBF_ARB_REG	
0x50040610	APB_ARB_REG	

Table 213: QSPIFL2_ARB_REG (0x50040600)

Bit	Mode	Symbol	Description	Reset
1	R/W	QSPIFL2_AHB_CPUS_PRIO	Priority AHB_CPUS layer system bus 0x0 : Highest priority 0x1 : Second prority	0x1
0	R/W	QSPIFL2_AHB_DMA_PRIO	Priority AHB_DMA layer system bus 0x0 : Highest priority 0x1 : Second prority	0x0

Table 214: QSPIRAM_ARB_REG (0x50040604)

Bit	Mode	Symbol	Description	Reset
1	R/W	QSPIRAM_AHB_AHBS_PRIO	Priority AHB AHBS layer system bus 0x0 : Highest priority 0x1 : Second prority	0x1
0	R/W	QSPIRAM_AHB_DMA_PRIO	Priority AHB DMA layer system bus 0x0 : Highest priority 0x1 : Second prority	0x0

Table 215: AHBREG_ARB_REG (0x50040608)

Bit	Mode	Symbol	Description	Reset
1	R/W	AHBREG_AHB_AHBS_PRIO	Priority AHB AHBS layer system bus 0x0 : Highest priority 0x1 : Second prority	0x1
0	R/W	AHBREG_AHB_DMA_PRIO	Priority AHB DMA layer system bus 0x0 : Highest priority 0x1 : Second prority	0x0

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Table 216: APBF_ARB_REG (0x5004060C)

Bit	Mode	Symbol	Description	Reset
5:4	R/W	APBF_AHB_DMA_PRIO	Priority AHB DMA layer system bus 0x0 : Highest priority 0x1 : Second prority 0x2 : Third priority 0x3 : Fourth priority	0x2
3:2	R/W	APBF_SNC_PRIO	Priority SNC interface 0x0 : Highest priority 0x1 : Second prority 0x2 : Third priority 0x3 : Fourth priority	0x1
1:0	R/W	APBF_AHB_AHBS_PRIO	Priority AHB CPUS layer system bus 0x0 : Highest priority 0x1 : Second prority 0x2 : Third priority 0x3 : Fourth priority	0x0

Table 217: APB_ARB_REG (0x50040610)

Bit	Mode	Symbol	Description	Reset
7:6	R/W	APB_AHB_CPUS_PRIO	priority AHB_CPUS layer system bus 0x0 : Highest priority 0x1 : Second prority 0x2 : Third priority 0x3 : Fourth priority	0x3
5:4	R/W	APB_AHB_DMA_PRIO	priority AHB_DMA layer system bus 0x0 : Highest priority 0x1 : Second prority 0x2 : Third priority 0x3 : Fourth priority	0x2
3:2	R/W	APB_SNC_PRIO	priority SNC interface 0x0 : Highest priority 0x1 : Second prority 0x2 : Third priority 0x3 : Fourth priority	0x1
1:0	R/W	APB_CMAC_PRIO	priority CMAC interface 0x0 : Highest priority 0x1 : Second prority 0x2 : Third priority 0x3 : Fourth priority	0x0

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44.2 Crypto-Engine Registers

Table 218: Register map AES_HASH

Address	Register	Description
0x30040000	CRYPTO_CTRL_REG	Crypto Control register
0x30040004	CRYPTO_START_REG	Crypto Start calculation
0x30040008	CRYPTO_FETCH_ADDR_REG	Crypto DMA fetch register
0x3004000C	CRYPTO_LEN_REG	Crypto Length of the input block in bytes
0x30040010	CRYPTO_DEST_ADDR_REG	Crypto DMA destination memory
0x30040014	CRYPTO_STATUS_REG	Crypto Status register
0x30040018	CRYPTO_CLRIRQ_REG	Crypto Clear interrupt request
0x3004001C	CRYPTO_MREG0_REG	Crypto Mode depended register 0
0x30040020	CRYPTO_MREG1_REG	Crypto Mode depended register 1
0x30040024	CRYPTO_MREG2_REG	Crypto Mode depended register 2
0x30040028	CRYPTO_MREG3_REG	Crypto Mode depended register 3
0x30040100	CRYPTO_KEYS_START	Crypto First position of the AES keys storage memory

Table 219: CRYPTO_CTRL_REG (0x30040000)

Bit	Mode	Symbol	Description	Reset
17	R/W	CRYPTO_AES_KEXP	It forces (active high) the execution of the key expansion process with the starting of the AES encryption/decryption process. The bit will be cleared automatically by the hardware, after the completion of the AES key expansion process.	0x0
16	R/W	CRYPTO_MORE_IN	0 : Define that this is the last input block. When the current input is consumed by the crypto engine and the output data is written to the memory, the calculation ends (CRYPTO_INACTIVE goes to one). 1 : The current input data block is not the last. More input data will follow. When the current input is consumed, the engine stops and waits for more data (CRYPTO_WAIT_FOR_IN goes to one).	0x0
15:10	R/W	CRYPTO_HASH_OUT_LEN	The number of bytes minus one of the hash result which will be saved at the memory by the DMA. In relation with the selected hash algorithm the accepted values are: MD5: 0..15 -> 1-16 bytes SHA-1: 0..19 -> 1-20 bytes	0x0

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Bit	Mode	Symbol	Description	Reset
			SHA-256: 0..31 -> 1 - 32 bytes SHA-256/224: 0..27 -> 1- 28 bytes SHA-384: 0..47 -> 1 - 48 bytes SHA-512: 0..63 -> 1 - 64 bytes SHA-512/224: 0..27 -> 1- 28 bytes SHA-512/256: 0..31 -> 1 - 32 bytes	
9	R/W	CRYPTO_HASH_SEL	Selects the type of the algorithm 0 : The encryption algorithm (AES) 1 : A hash algorithm. The exact algorithm is defined by the fileds CRYPTO_ALG and CRYPTO_ALG_MD.	0x0
8	R/W	CRYPTO_IRQ_EN	Interrupt Request Enable 0 : The interrupt generation ability is disabled. 1 : The interrupt generation ability is enabled. Generates an interrupt request at the end of operation.	0x0
7	R/W	CRYPTO_ENCDEC	Encryption/Decryption 0 : Decryption 1 : Encryption	0x0
6:5	R/W	CRYPTO_AES_KEY_SZ	The size of AES Key 0x0 : 128 bits AES Key 0x1 : 192 bits AES Key 0x2 : 256 bits AES Key 0x3 : 256 bits AES Key	0x0
4	R/W	CRYPTO_OUT_MD	Output Mode. This field makes sense only when the AES algorithm is selected (CRYPTO_HASH_SEL =0) 0 : Write back to memory all the resulting data 1 : Write back to memory only the final block of the resulting data	0x0
3:2	R/W	CRYPTO_ALG_MD	It defines the mode of operation of the AES algorithm when the controller is configured for an encryption/decryption processing (CRYPTO_HASH_SEL = 0). 0x0 : ECB 0x1 : ECB 0x2 : CTR 0x3 : CBC When the controller is configured to applies a HASH function, this field selects the desired HASH algorithm with the help of the CRYPTO_ALG. 0x0 : HASH algorithms that are based on 32 bits operations 0x1 : HASH algorithms that are based on 64 bits operations 0x2 : Reserved 0x3 : Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
			See also the CRYPTO_ALG field.	
1:0	R/W	CRYPTO_ALG	Algorithm selection. When CRYPTO_HASH_SEL = 0 the only available choice is the AES algorithm. 0x0 : AES 0x1 : Reserved 0x2 : Reserved 0x3 : Reserved When CRYPTO_HASH_SEL = 1, this field selects the desired hash algorithm, with the help of the CRYPTO_ALG_MD field. If CRYPTO_ALG_MD = 0x0 0x0 : MD5 0x1 : SHA-1 0x2 : SHA-256/224 0x3 : SHA-256 If CRYPTO_ALG_MD = 0x1 0x0 : SHA-384 0x1 : SHA-512 0x2 : SHA-512/224 0x3 : SHA-512/256	0x0

Table 220: CRYPTO_START_REG (0x30040004)

Bit	Mode	Symbol	Description	Reset
0	R0/W	CRYPTO_START	Write 1 to initiate the processing of the input data. This register is auto-cleared.	0x0

Table 221: CRYPTO_FETCH_ADDR_REG (0x30040008)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CRYPTO_FETCH_ADDR	The memory address from where will be retrieved the data that will be processed. The value of this register is updated as the calculation proceeds and the output data are written to the memory.	0x0

Table 222: CRYPTO_LEN_REG (0x3004000C)

Bit	Mode	Symbol	Description	Reset
23:0	R/W	CRYPTO_LEN	It contains the number of bytes of input data. If this number is not a multiple of a block size, the data is automatically extended with zeros. The value of	0x0

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Bit	Mode	Symbol	Description	Reset
			this register is updated as the calculation proceeds and the output data are written to the memory.	

Table 223: CRYPTO_DEST_ADDR_REG (0x30040010)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CRYPTO_DEST_ADDR	Destination address at where the result of the processing is stored. The value of this register is updated as the calculation proceeds and the output data are written to the memory.	0x0

Table 224: CRYPTO_STATUS_REG (0x30040014)

Bit	Mode	Symbol	Description	Reset
2	R	CRYPTO_IRQ_ST	The status of the interrupt request line of the CRYPTO block. 0 : There is no active interrupt request. 1 : An interrupt request is pending.	0x0
1	R	CRYPTO_WAIT_FOR_IN	Indicates the situation where the engine waits for more input data. This is applicable when the CRYPTO_MORE_IN= 1, so the input data are fragmented in the memory. 0 : The crypto is not waiting for more input data. 1 : The crypto waits for more input data. The CRYPTO_INACTIVE flag remains to zero to indicate that the calculation is not finished. The supervisor of the CRYPTO must program to the CRYPTO_FETCH_ADDR and CRYPTO_LEN a new input data fragment. The calculation will be continued as soon as the CRYPTO_START register will be written with 1. This action will clear the CRYPTO_WAIT_FOR_IN flag.	0x0
0	R	CRYPTO_INACTIVE	0 : The CRYPTO is active. The processing is in progress. 1 : The CRYPTO is inactive. The processing has finished.	0x1

Table 225: CRYPTO_CLRIRQ_REG (0x30040018)

Bit	Mode	Symbol	Description	Reset
0	R0/W	CRYPTO_CLRIRQ	Write 1 to clear a pending interrupt request.	0x0

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Table 226: CRYPTO_MREG0_REG (0x3004001C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CRYPTO_MREG0	It contains information that are depended by the mode of operation, when is used the AES algorithm: CBC - IV[31:0] CTR - CTRBLK[31:0]. It is the initial value of the 32 bits counter. At any other mode, the contents of this register has no meaning.	0x0

Table 227: CRYPTO_MREG1_REG (0x30040020)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CRYPTO_MREG1	It contains information that are depended by the mode of operation, when is used the AES algorithm: CBC - IV[63:32] CTR - CTRBLK[63:32] At any other mode, the contents of this register has no meaning.	0x0

Table 228: CRYPTO_MREG2_REG (0x30040024)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CRYPTO_MREG2	It contains information that are depended by the mode of operation, when is used the AES algorithm: CBC - IV[95:64] CTR - CTRBLK[95:64] At any other mode, the contents of this register has no meaning.	0x0

Table 229: CRYPTO_MREG3_REG (0x30040028)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CRYPTO_MREG3	It contains information that are depended by the mode of operation, when is used the AES algorithm: CBC - IV[127:96] CTR - CTRBLK[127:96] At any other mode, the contents of this register has no meaning.	0x0

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Table 230: CRYPTO_KEYS_START (0x30040100)

Bit	Mode	Symbol	Description	Reset
31:0	W	CRYPTO_KEY_X	CRYPTO_KEY_(0-63) This is the AES keys storage memory. This memory is accessible via AHB slave interface, only when the CRYPTO is inactive (CRYPTO_INACTIVE = 1).	N/A

44.3 Analog Miscellaneous Registers

Table 231: Register map ANAMISC

Address	Register	Description
0x50050610	CLK_REF_SEL_REG	Select clock for oscillator calibration
0x50050614	CLK_REF_CNT_REG	Count value for oscillator calibration
0x50050618	CLK_REF_VAL_REG	DIVN reference cycles, lower 16 bits
0x5005061C	CLK_CAL_IRQ_REG	Select clock for oscillator calibration

Table 232: CLK_REF_SEL_REG (0x50050610)

Bit	Mode	Symbol	Description	Reset
7:5	R/W	CAL_CLK_SEL	Select calibration clock input to be used in calibration: 0x0 : DIVN clock 0x1 : RCLP 0x2 : RCHS 0x3 : XTAL32K 0x4 : RCOSC 0x5, 0x6 and 0x7: Reserved	0x0
4	R/W	EXT_CNT_EN_SEL	0 : Enable XTAL_CNT counter by the REF_CLK selected by REF_CLK_SEL. 1 : Enable XTAL_CNT counter from an external input.	0x0
3	R/W	REF_CAL_START	Writing a 1 starts a calibration. This bit is cleared when calibration is finished, and CLK_REF_VAL is ready.	0x0
2:0	R/W	REF_CLK_SEL	Select reference clock input for calibration: 0x0 : RCLP 0x1 : RCHS 0x2 : XTAL32K 0x3 : RCX 0x4 : RCOSC 0x5 : DIVN clock	0x0

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Table 233: CLK_REF_CNT_REG (0x50050614)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	REF_CNT_VAL	Indicates the calibration time, with a decrement counter to 1.	0x0

Table 234: CLK_REF_VAL_REG (0x50050618)

Bit	Mode	Symbol	Description	Reset
31:0	R	XTAL_CNT_VAL	Returns the number of DIVN clock cycles counted during the calibration time, defined with REF_CNT_VAL	0x0

Table 235: CLK_CAL_IRQ_REG (0x5005061C)

Bit	Mode	Symbol	Description	Reset
3	R/W	-	Reserved	0x0
2	R0/WC	CLK_CAL_IRQ_CLR	Clear the IRQ. 1: Clear the IRQ 0: No effect. Read out 0 always.	0x0
1	R	CLK_CAL_IRQ_STATUS	Shows the IRQ bit status.	0x0
0	R/W	CLK_CAL_IRQ_EN	Enable clk calibration IRQ. 0: Disabled. 1*: Enabled. *Note: If IRQ feature is enabled, every calibration should be started by setting CLK_REF_SEL_REG[REF_CAL_START] to 1.	0x0

44.4 Cache Controller Registers

Table 236: Register map CACHE

Address	Register	Description
0x100C0020	CACHE_CTRL2_REG	Cache control register 2 (only Word (32-bits) access supported).
0x100C0028	CACHE_MRM_HITS_REG	Cache MRM (Miss Rate Monitor) HITS register (only Word (32-bits) access supported).
0x100C002C	CACHE_MRM_MISSES_REG	Cache MRM (Miss Rate Monitor) MISSES register (only Word (32-bits) access supported).
0x100C0030	CACHE_MRM_CTRL_REG	Cache MRM (Miss Rate Monitor) CONTROL register (only Word (32-bits) access supported).
0x100C0034	CACHE_MRM_TINT_REG	Cache MRM (Miss Rate Monitor) TIME INTERVAL register (only Word (32-bits) access supported).
0x100C0038	CACHE_MRM_MISSES_THRES_REG	Cache MRM (Miss Rate Monitor) THRESHOLD register (only Word (32-bits) access supported).

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Address	Register	Description
0x100C003C	CACHE_MRM_HITS_THRES_REG	Cache MRM (Miss Rate Monitor) HITS THRESHOLD register (only Word (32-bits) access supported).
0x100C0040	CACHE_FLASH_REG	Cache QSPI Flash program size and base address register (only Word (32-bits) access supported).
0x100C0048	CACHE_MRM_HITS1WS_REG	Cache MRM (Miss Rate Monitor) HITS with 1 Wait State register (only Word (32-bits) access supported).
0x100C0050	SWD_RESET_REG	SWD HW reset control register (only Word (32-bits) access supported).

Table 237: CACHE_CTRL2_REG (0x100C0020)

Bit	Mode	Symbol	Description	Reset
31:22	-	-	Reserved	0
21	R	CACHE_READY	Cache Controller RO status bit. 0: Default. 1: Set 1 when CACHE_CTRL is enabled, initialized and immediately ready for a cacheable access to service.	0
20	R	CACHE_RAM_INIT	Cache Controller RO status bit. 0: Default. 1: Set 1 when SRAM is being initialized (being flushed). Note: The flushing of the cache memory takes 256 HCLK cycles.	0
19	R/W	CACHE_FLUSHED	0: Cache is not flushed yet. 1: Cache is flushed. Note 1: Setting and clearing of this (status) bit field is automatically done by the hardware. It is set on the falling edge and cleared on the rising edge of the (Cache Controller) *CACHE_RAM_INIT* signal. Note 2: When the Cache is flushed by disabling and enabling the Cache Controller with a SYS_CTRL_REG[CACHERAM_MUX] sequence of 1 -> 0 -> 1, the *CACHE_FLUSHED* bit can also be cleared first by the software (if needed) with writing a CACHE_CTRL2_REG(CACHE_FLUSHED) sequence of 1 -> 0. This is needed when the software uses the *CACHE_FLUSHED* bit as a status bit to wait for (for example, in a while-loop).	0
18	R/W	CACHE_FLUSH_DISABLE	0: Default. 1: Flushing of the Cache memory is disabled when SYS_CTRL_REG[CACHERAM_MUX] is switched from 1 to 0. Note: Setting this bit to 1 is only allowed for debugging purposes.	0
17:16	R/W	CACHE_USE_FULL_DB_RANGE	00: CACHERAM (mirrored) read/write and NO use of the full 184 bits databus (for executing program code or extension of the SysRAM with the Cache	0

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Bit	Mode	Symbol	Description	Reset
			RAM). In this mode 8 bits, 16 bits, and 32 bits write access is supported. 01: CACHERAM (mirrored) read and use of the full 184 bits databus of "SRAM_1_0" (for testing and debugging purposes). In this mode only 32 bits write access is supported. 10: CACHERAM (mirrored) read and use of the full 184 bits databus of "SRAM_3_2" (for testing and debugging purposes). In this mode only 32 bits write access is supported. 11: Reserved. Note 1: SYS_CTRL_REG[CACHERAM_MUX] must be set to 0 before accessing the memory mapped (mirrored) Cache Data and TAG memory. Note 2: For all 3 settings, max. 8 kB is available from the memory map.	
15	R/W	CACHE_MHCLKEN_DISABLE	0: Default. 1: The "m_HCLK_EN" input is ignored and the controller avoids inserting m_HTRANS=BUSY because of wait states. Note: This bit is only relevant for executing from QSPI Flash (when set to 1 it will improve performance). This bit should be kept on 0 for executing from eFlash.	0
14	R/W	CACHE_CWF_DISABLE	0: Default. 1: The cache line refill is performed with INCR type burst and "Critical Word First" is disabled. Note: This bit is only relevant for executing from QSPI Flash (when set to 1 it will improve performance).This bit should be kept on 0 for executing from eFlash.	0
13	R/W	CACHE_CGEN	0: Cache controller clock gating is not enabled. 1: Cache controller clock gating is enabled (enabling power saving).	0
12	R/W	CACHE_WEN	0: Cache Data and TAG memory read only. 1: Cache Data and TAG memory read/write. The Data and TAG memory are only updated by the cache controller. There is no HW protection to prevent unauthorized access by the ARM. Note 1: When accessing the memory mapped Cache Data and TAG memory (which is only allowed for debugging purposes) only 32-bits access is supported. Note 2: SYS_CTRL_REG[CACHERAM_MUX] must be set to 0 before accessing the memory mapped Cache Data and TAG memory.	0

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Bit	Mode	Symbol	Description	Reset
			See also the CACHE_CTRL2_REG[CACHE_USE_FULL_DB_RANGE] description.	
11:0	R/W	CACHE_LEN	Length of OQSPI FLASH cacheable memory. N*64 KBytes. N = 0 to 2048, incl. 2048 (max. of 128 MB). Setting CACHE_LEN=0 disables the caching. Note 1: The max. relevant CACHE_LEN setting depends on the chosen Flash region (program) size. Note 2: The first block (CACHE_LEN = 1) includes the memory space specified by CACHE_FLASH_REG[FLASH_REGION_OFFSET].	0

Table 238: CACHE_MRM_HITS_REG (0x100C0028)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	MRM_HITS	Contains the amount of cache hits.	0x0

Table 239: CACHE_MRM_MISSES_REG (0x100C002C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	MRM_MISSES	Contains the amount of cache misses.	0x0

Table 240: CACHE_MRM_CTRL_REG (0x100C0030)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0
4	R/W	MRM_IRQ_HITS_THRES_STATUS	0: No interrupt is generated. 1: Interrupt (pulse-sensitive) is generated because the number of cache hits reached the programmed threshold (threshold != 0).	0
3	R/W	MRM_IRQ_MISSES_THRES_STATUS	0: No interrupt is generated. 1: Interrupt (pulse-sensitive) is generated because the number of cache misses reached the programmed threshold (threshold != 0).	0
2	R/W	MRM_IRQ_TINT_STATUS	0: No interrupt is generated. 1: Interrupt (pulse-sensitive) is generated because the time interval counter reached the end (time interval != 0).	0
1	R/W	MRM_IRQ_MASK	0: Disables interrupt generation. 1: Enables interrupt generation. Note: The Cache MRM generates a pulse-sensitive interrupt towards the ARM processor,	0

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Bit	Mode	Symbol	Description	Reset
0	R/W	MRM_START	0: Freeze the "misses/hits" counters and reset the time interval counter to the programmed value in CACHE_MRM_TINT_REG. 1: Enables the counters. Note: In case CACHE_MRM_CTRL_REG[MRM_START] is set to 1 and CACHE_MRM_TINT_REG (!=0) is used for the MRM interrupt generation, the time interval counter counts down (on a fixed reference clock of 32 MHz) until it's 0. At that time CACHE_MRM_CTRL_REG[MRM_START] will be reset automatically to 0 by the MRM hardware and the MRM interrupt will be generated.	0

Table 241: CACHE_MRM_TINT_REG (0x100C0034)

Bit	Mode	Symbol	Description	Reset
31:19	-	-	Reserved	0x0
18:0	R/W	MRM_TINT	Defines the time interval for the monitoring in 32 MHz clock cycles. See also the description of CACHE_MRM_CTRL_REG[MRM_IRQ_TINT_STATUS]. Note: When MRM_TINT=0 (unrealistic value), no interrupt will be generated.	0x0

Table 242: CACHE_MRM_MISSES_THRES_REG (0x100C0038)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	MRM_MISSES_THRES	Defines the misses threshold to trigger the interrupt generation. See also the description of CACHE_MRM_CTRL_REG[MRM_IRQ_MISSES_THRES_STATUS]. Note: When MRM_MISSES_THRES=0 (unrealistic value), no interrupt will be generated.	0x0

Table 243: CACHE_MRM_HITS_THRES_REG (0x100C003C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	MRM_HITS_THRES	Defines the hits threshold to trigger the interrupt generation. See also the description of CACHE_MRM_CTRL_REG[MRM_IRQ_HITS_THRES_STATUS]. Note: When MRM_HITS_THRES=0 (unrealistic value), no interrupt will be generated.	0x0

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Table 244: CACHE_FLASH_REG (0x100C0040)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	FLASH_REGION_BASE	These bits corresponds with the Flash region base address bits [31:16]. Default value is 0x1800. The Flash region base address bits [31:27] are fixed to 0b00011, supporting the range of 0x1800-0x1FFF. These register bits are retained. Note 1: The updated value takes effect only after a software reset. Note 2 The Flash region base address setting depends on the chosen Flash region size.	0x1800
15:4	R/W	FLASH_REGION_OFFSET	Flash region offset address (in words). This value is added to the Flash (CPU) address bits [13:2]. These register bits are retained. Note 1: The updated value takes effect only after a software reset.	0x0
3:0	R/W	FLASH_REGION_SIZE	Flash region size. Default value is 1 (0.5 MB). 0 = 0.25 MB, 1 = 0.5 MB, 2 = 1 MB, 3 = 2 MB, 4 = 4 MB, 5 = 8 MB, 6 = 16 MB, 7 = 32 MB, 8 = 64 MB, 9 = 128 MB. These register bits are retained. Note 1: The updated value takes effect only after a software reset. Note 2: See for the max. region (program) size the memory map.	0x1

Table 245: CACHE_MRM_HITS1WS_REG (0x100C0048)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	MRM_HITS1WS	Contains the amount of cache hits.	0x0

Table 246: SWD_RESET_REG (0x100C0050)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0
0	R0/W	SWD_HW_RESET_REQ	0: default.	0

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Bit	Mode	Symbol	Description	Reset
			1: HW reset request (from the debugger tool). The register is automatically reset with a HW_RESET. This bit can only be accessed by the debugger software and not by the application.	

44.5 Charger Registers

Table 247: Register map CHARGER

Address	Register	Description
0x50040300	CHG_DET_FSM_CTRL_REG	Charge detection FSM control register
0x50040304	CHG_DET_FSM_STATUS_REG	Charge detection FSM status register
0x50040308	CHG_DET_SW_CTRL_REG	Charge detection manual (SW-based) mode control register
0x5004030C	CHG_DET_STATUS_REG	Charge detection status register holding the comparator outputs
0x50040310	CHG_DET_ADC_CTRL_REG	Charge detection ADC control register
0x50040314	CHG_DET_TIMER_REG	Charge detection timer register (used in the FSM)
0x50040318	CHG_DET_DCD_TIMER_REG	Charge detection DCD time-out timer register (used in the FSM)
0x5004031C	CHG_DET_IRQ_MASK_REG	Charge detection IRQ mask register
0x50040320	CHG_DET_IRQ_STATUS_REG	Charge detection IRQ status register
0x50040324	CHG_DET_IRQ_CLEAR_REG	Charge detection IRQ clear register
0x51000600	CHARGER_CTRL_REG	Charger main control register
0x51000608	CHARGER_STATUS_REG	Charger main status register
0x5100060C	CHARGER_VOLTAGE_PARAM_REG	Charger voltage settings register
0x51000610	CHARGER_CURRENT_PARAM_REG	Charger current settings register
0x51000614	CHARGER_VOLTAGE_STATUS_REG	Charger voltage status register
0x51000618	CHARGER_CURRENT_STATUS_REG	Charger current status register
0x5100061C	CHARGER_TEMPSET_PARAM_REG	Charger battery temperature settings register
0x51000620	CHARGER_TEMPSET2_PARAM_REG	Charger battery temperature settings register (Cooler, Warmer).
0x51000624	CHARGER_PRE_CHARGE_TIMER_REG	Maximum pre-charge time limit register

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Address	Register	Description
0x51000628	CHARGER_CC_CHARGE_TIMER_REG	Maximum CC-charge time limit register
0x5100062C	CHARGER_CV_CHARGE_TIMER_REG	Maximum CV-charge time limit register
0x51000630	CHARGER_TOTAL_CHARGE_TIMER_REG	Maximum total charge time limit register
0x51000634	CHARGER_JEITA_V_CHARGE_REG	JEITA-compliant Charge voltage settings register
0x51000638	CHARGER_JEITA_V_PRECHARGE_REG	JEITA-compliant Pre-Charge voltage settings register
0x5100063C	CHARGER_JEITA_V_REPLENISH_REG	JEITA-compliant Replenish settings register
0x51000640	CHARGER_JEITA_V_OVP_REG	JEITA-compliant OVP settings register
0x51000644	CHARGER_JEITA_CURRENT_REG	JEITA-compliant current settings register
0x51000648	CHARGER_JEITA_CURRENT2_REG	JEITA-compliant current settings register for "Cooler" and "Warmer" zones
0x5100064C	CHARGER_VBAT_COMP_TIMER_REG	Main Vbat comparator timer register
0x51000650	CHARGER_VOVP_COMP_TIMER_REG	Vbat OVP comparator timer register
0x51000654	CHARGER_TDIE_COMP_TIMER_REG	Die temperature comparator timer register
0x51000658	CHARGER_TBAT_MON_TIMER_REG	Battery temperature monitor interval timer register
0x5100065C	CHARGER_TBAT_COMP_TIMER_REG	Battery temperature (main) comparator timer register
0x51000660	CHARGER_THOT_COMP_TIMER_REG	Battery temperature comparator timer register for "Hot" zone
0x51000664	CHARGER_PWR_UP_TIMER_REG	Charger power-up settling timer register
0x51000668	CHARGER_STATE_IRQ_MASK_REG	Mask register of Charger FSM IRQs
0x5100066C	CHARGER_ERROR_IRQ_MASK_REG	Mask register of Charger Error IRQs
0x51000670	CHARGER_STATE_IRQ_STATUS_REG	Status register of Charger FSM IRQs
0x51000674	CHARGER_ERROR_IRQ_STATUS_REG	Status register of Charger Error IRQs
0x51000678	CHARGER_STATE_IRQ_CLR_REG	Interrupt clear register of Charger FSM IRQs
0x5100067C	CHARGER_ERROR_IRQ_CLR_REG	Interrupt clear register of Charger Error IRQs
0x51000680	CHARGER_LOCK_REG	Charger HW lock register
0x51000684	CHARGER_SWLOCK_REG	Charger SW lock register

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Table 248: CHG_DET_FSM_CTRL_REG (0x50040300)

Bit	Mode	Symbol	Description	Reset
0	R/W	CHG_DET_EN	0 = Charge detection FSM is disabled, the analog part is controlled through the CHG_DET_SW_CTRL_REG register's bit-fields. 1 = Charge detection FSM is enabled and controls the analog part, overruling the content of CHG_DET_SW_CTRL_REG	0x0

Table 249: CHG_DET_FSM_STATUS_REG (0x50040304)

Bit	Mode	Symbol	Description	Reset
12:9	R	CHG_DET_STATE	This bit-field returns the current state of the charge detection block's FSM. The supported states are: - 0x0 : WAIT_FOR_ATTACH (starting state) - 0x1 : NODE_ATTACHED (USB_DP_VAL first check) - 0x2 : WAIT_FOR_DCD (Data Contact Detection - first state) - 0x3 : CHECK_FOR_DCD (Data Contact Detection - second state) - 0x4 : WAIT_FOR_PCD (Primary Contact Detection - first state) - 0x5 : CHECK_FOR_PCD (Primary Contact Detection - second state) - 0x6 : WAIT_FOR_SCD (Secondary Contact Detection - first state) - 0x7 : CHECK_FOR_SCD (Secondary Contact Detection - second state) - 0x8 : CHG_PORT_DETECTED (terminal state, indicating the port detection's completion). It is noted that: - The FSM returns to state WAIT_FOR_ATTACH either when VBUS_AVAILABLE goes to 0, or when it is disabled by the SW. - The FSM may return to state WAIT_FOR_ATTACH from any of the other states when VBUS_AVAILABLE goes to 0, implying either a USB detach event or a VBUS voltage drop. - The FSM implements a time-out mechanism during the Data Contact Detection phase (NODE_ATTACHED, WAIT_FOR_DCD and CHECK_FOR_DCD states). A dedicated 10-bit timer counts down in any of these states, until USB_DP_VAL is found to be 0 (so we have a contact detected) or until it expires. - The time-out timer's expiration means that there is no D+/D- pins contact detected within the required time-out period, as defined through CHG_DET_DCD_TIMER_REG and as required by the spec. Even in this case though, the FSM does not abort, but proceeds normally to the next	0x0

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Bit	Mode	Symbol	Description	Reset
			state, which is the first Primary Detection State, to comply with the Battery Charging specification.	
8	R	NO_CONTACT_DETECTED	0 = Contact is sensed on the Dp/Dm (data) pins by the FSM, during the Data Contact Detection (DCD) phase (USB_DP_VAL = 0) 1 = No contact is sensed on the Dp/Dm pins during the DCD phase (USB_DP_VAL = 1) Note: Even in the case of no contact detected on the Dp/Dm pins, the FSM continues with the port detection procedure, moving to the Primary Contact Detection (PCD) states.	0x0
7	R	PORT_2P4AMP_DETECTED	0 = Port detection either not yet finished or finished without detecting a 2.4 Amp charging port 1 = Port detection has finished by detecting a 2.4 Amp charging port	0x0
6	R	PORT_2AMP_DETECTED	0 = Port detection either not yet finished or finished without detecting a 2 Amp charging port 1 = Port detection has finished by detecting a 2 Amp charging port	0x0
5	R	PORT_1AMP_DETECTED	0 = Port detection either not yet finished or finished without detecting a 1 Amp charging port 1 = Port detection has finished by detecting a 1 Amp charging port	0x0
4	R	PS2_PROP_PORT_DETECTED	0 = Port detection either not yet finished or finished without detecting a PS2 or a Proprietary charger port 1 = Port detection has finished by detecting either a PS2 or a Proprietary charger port	0x0
3	R	DCP_PORT_DETECTED	0 = Port detection either not yet finished or finished without detecting a DCP port (Dedicated Charging Port) 1 = Port detection has finished by detecting a DCP port	0x0
2	R	CDP_PORT_DETECTED	0 = Port detection either not yet finished or finished without detecting a CDP port (Charging Downstream Port) 1 = Port detection has finished by detecting a CDP port	0x0
1	R	SDP_PORT_DETECTED	0 = Port detection either not yet finished or finished without detecting an SDP port (Standard Downstream Port) 1 = Port detection has finished by detecting an SDP port	0x0
0	R	DETECTION_COMPLETED	0 = Port detection not yet finished, FSM still active 1 = Port detection completed, FSM has reached its terminal state (CHG_PORT_DETECTED). The port type is accessible through the relevant bit-fields of this register.	0x0

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Table 250: CHG_DET_SW_CTRL_REG (0x50040308)

Bit	Mode	Symbol	Description	Reset
5	R/W	IDM_SINK_ON	0 = Disables the Idm_sink to USBm 1 = Enables the Idm_sink to USBm	0x0
4	R/W	IDP_SINK_ON	0 = Disables the Idp_sink to USBp 1 = Enables the Idp_sink to USBp	0x0
3	R/W	VDM_SRC_ON	0 = Disables the Vdm_src 1 = Enables the Vdm to USBm and also the USB_DCP_DET status bit	0x0
2	R/W	VDP_SRC_ON	0 = Disables the Vdp_src 1 = Enables the Vdp_src and also the USB_CHG_DET status bit	0x0
1	R/W	IDP_SRC_ON	0 = Disables the Idp_src and the Rdm_dwn 1 = Enables the Idp_src and the Rdm_dwn	0x0
0	R/W	USB_CHARGE_ON	0 = Disables the charge detection analog circuit 1 = Enables the charge detection analog circuit	0x0

Table 251: CHG_DET_STATUS_REG (0x5004030C)

Bit	Mode	Symbol	Description	Reset
5	R	USB_DM_VAL2	0: USBp < 2.3 V 1: USBp > 2.5 V	0x0
4	R	USB_DP_VAL2	0: USBp < 2.3 V 1: USBp > 2.5 V	0x0
3	R	USB_DM_VAL	0: USBm < 0.8 V 1: USBm > 1.5 V (PS2 or Proprietary Charger)	0x0
2	R	USB_DP_VAL	0: USBp < 0.8 V 1: USBp > 1.5 V (PS2 or Proprietary Charger)	0x0
1	R	USB_CHG_DET	0: Standard Downstream Port (SDP) or no Dp/Dm contact detected (nothing connected) 1: Charging Downstream Port (CDP) or Dedicated Charging Port (DCP)	0x0
0	R	USB_DCP_DET	0: Charging downstream port is detected 1: Dedicated charger is detected It is noted that the control bit VDM_SRC_ON must be set to validate this status bit. Note: This register shows the actual status.	0x0

Table 252: CHG_DET_ADC_CTRL_REG (0x50040310)

Bit	Mode	Symbol	Description	Reset
2	R/W	-	Reserved	0x0
1	R/W	USB_DM_TO_ADC_EN	0: Disables the connection of USBm to the GP_ADC 1: Enables the connection of USBm to the GP_ADC through a relative test switch	0x0

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Bit	Mode	Symbol	Description	Reset
0	R/W	USB_DP_TO_ADC_EN	0 = Disables the connection of USBp to the GP_ADC 1 = Enables the connection of USBp to the GP_ADC through a relative test switch	0x0

Table 253: CHG_DET_TIMER_REG (0x50040314)

Bit	Mode	Symbol	Description	Reset
23:16	R	CHG_DET_TIMER	This bit-field returns the current value of the charge detection timer, which is used by the FSM and which down-counts with a clock of 1 kHz. The specific clock is enabled by setting the CLK_SYS_REG[CLK_CHG_EN] bit-field to 1 and it is the same clock used by the Charger's digital block. The specific timer is automatically re-loaded with the programmed threshold value (CHG_DET_TIMER_THRES), upon expiring to zero or when the charge detection FSM moves to the state NODE_ATTACHED (0x1).	0x32
15:8	R	-	Reserved	0x0
7:0	R/W	CHG_DET_TIMER_THRES	This bit-field determines the value from which the charge detection timer starts down-counting, until expiring to zero. Non-zero values are recommended.	0x32

Table 254: CHG_DET_DCD_TIMER_REG (0x50040318)

Bit	Mode	Symbol	Description	Reset
25:16	R	DCD_TIMER	This bit-field returns the current value of the DCD time-out timer, also ticking with the 1 KHz clock, same as the shared 8-bit timer. The specific timer counts only in states NODE_ATTACHED, WAIT_FOR_DCD and CHECK_FOR_DCD, since these are the states where Data Contact Detection is evaluated. The timer is automatically reloaded with the programmed threshold value (DCD_TIMEOUT_THRES) as soon as the FSM returns to its starting state (WAIT_FOR_ATTACH, 0x0).	0x258
15:10	R	-	Reserved	0x0
9:0	R/W	DCD_TIMEOUT_THRES	This bit-field determines the value from which the Data Contact Detection (DCD) time-out timer starts down-counting, until expiring to zero. Non-zero values are recommended.	0x258

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Table 255: CHG_DET_IRQ_MASK_REG (0x5004031C)

Bit	Mode	Symbol	Description	Reset
0	R/W	CHG_DET_IRQ_EN	0: Charge detection block's IRQ generation is disabled, interrupts to Cortex-M33 are masked. 1: Charge detection block's IRQ generation is enabled.	0x0

Table 256: CHG_DET_IRQ_STATUS_REG (0x50040320)

Bit	Mode	Symbol	Description	Reset
0	R	CHG_DET_IRQ	0: No new charge detection IRQ has been generated. 1: A new charge detection IRQ is generated and should be cleared by SW, by writing to CHG_DET_IRQ_CLEAR_REG (interrupt is level-sensitive).	0x0

Table 257: CHG_DET_IRQ_CLEAR_REG (0x50040324)

Bit	Mode	Symbol	Description	Reset
0	R0/W	CHG_DET_IRQ_CLR	Writing any value to this register clears the charge detection IRQ, reading always returns zero.	0x0

Table 258: CHARGER_CTRL_REG (0x51000600)

Bit	Mode	Symbol	Description	Reset
28	R/W	EOC_TRIGGER	0: Edge-sensitive End-of-Charge detection support is enabled (default). The Charger's digital block expects a positive edge of the End-of-Charge signal coming from the Charger's analog circuit to let the respective debounce counters start and enable the FSM switch to the END_OF_CHARGE state, if the signal is stable. 1: Level-sensitive End-of-Charge detection is enabled. In this mode, the Charger's digital block only monitors the level of the End-of-Charge signal coming from the analog circuit and if this is seen high in either CC_CHARGE or CV_CHARGE state, the EOC debounce counters start.	0x0
27:22	R	EOC_INTERVAL_CHECK_TIMER	The specific bit-field determines the current state of the timer used to periodically check the End-of-Charge signal, as soon as the Charger's FSM is either in CC_CHARGE or CV_CHARGE state. Thus, as soon as the Charger's FSM enters the CC_CHARGE state: - The timer starts increasing when a positive edge detection on End-of-Charge signal occurs. - It keeps increasing until reaching the programmed EOC_INTERVAL_CHECK_THRES value, if and only if there is no detection of a negative edge on End-of-Charge signal. If this	0x0

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Bit	Mode	Symbol	Description	Reset
			happens, the timer resets and starts over with a new End-of-Charge positive edge. - The timer also resets after having reached its programmed threshold or when the Charger's FSM next state is END_OF_CHARGE. This happens only after having found End-of-Charge signal asserted for 4 consecutive checks and provided that the specific signal has not de-asserted during the timer's interval. Note: It must be noted that out of these two states, the specific timer is kept to zero. It is also noted that this timer runs at the 1 MHz clock of the Charger's block and its value always ranges from 0 to the EOC_INTERVAL_CHECK_THRES value set in the respective bit-field of CHARGER_CTRL_REG.	
21:16	R/W	EOC_INTERVAL_CHECK_THRES	This bit-field determines the periodic interval of checking the End-of-Charge signal, when the Charger's FSM is either in CC_CHARGE or in CV_CHARGE state. To implement this, a dedicated timer has been used, counting from zero up to the value programmed into this bit-field (see also EOC_INTERVAL_CHECK_TIMER field's description). As soon as this timer reaches the programmed value, the End-of-Charge signal is sampled and depending on its status (high or low), another counter, keeping the number of consecutive End-of-Charge events, is increased or not. See also the description of the EOC_DEBOUNCE_CNT bit-field of CHARGER_STATUS_REG, for this counter. Note: The specific bit-field should always be programmed to a non-zero value.	0x3F
15	R/W	REPLENISH_MODE	When this bit-field is set and the Charger's FSM is in the BYPASSED state (thus, in Bypass mode), the internal multiplexer inside the digital part of the charger selects the Replenish, instead of the Pre-charge setting to be driven to the main Vbat comparator of the Charger's analogue circuitry. By this way, SW can read the respective analogue comparator's output in CHARGER_STATUS_REG (bit-field MAIN_VBAT_COMP_OUT), after the battery's volrtage has reached the End-of-Charge level, and determine if the battery voltage has dropped below the Replenish level, re-starting the battery charging accordingly. Note: When the Charger's FSM is active and operational, this bit-field is don't care and the FSM determines which level (Pre-charge or Replenish) will be selected and driven to the analogue, depending on the current state. It is also noted that the supported Pre-charge and Replenish levels can be viewed in the respective bit-fields defined in CHARGER_VOLTAGE_PARAM_REG register.	0x0
14	R/W	PRE_CHARGE_MODE	When set, this bit-field enables a signal of the same name with the bit-field, driven from the Charger's digital part towards the analogue circuitry, in order to determine the current in Pre-	0x1

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Bit	Mode	Symbol	Description	Reset
			Charge mode. If the Charger's FSM is active and operational, the specific bit-field is don't care. Hence, it is considered only when the Charger's FSM has reached the BYPASSED state (thus, in Bypass mode). With the Charger's FSM being bypassed, SW should take over control and set the specific bit-field, in order to deliver the Pre-Charge instead of the normal Charge current to the Charger's analogue circuitry, during the Pre-Charge phase. Note: See also the description of CHARGER_CURRENT_PARAM_REG register for the Pre-Charge and normal Charge current levels supported.	
13	R/W	CHARGE_LOOP_HOLD	When set, this bit-field disables charging, provided that the Charger's FSM has switched to the BYPASSED state. This is possible only by setting the CHARGER_BYPASS bit-field of this register. Thus, as soon as the Charger's FSM is bypassed, the respective signal driven by the FSM is overruled by this bit-field, making the analogue part of the Charger controllable also in this mode. If the Charger's FSM is not bypassed, this bit-field is don't care.	0x1
12	R/W	JEITA_SUPPORT_DISABLED	0: Charger's JEITA FSM monitoring the battery temperature checks also if battery temperature is in the Warm or Cool zones. In that case, it updates accordingly all the Charger's voltage levels (Charge, Pre-Charge, Replenish and OVP) programmed in CHARGER_VOLTAGE_PARAM_REG, as well as the charge and pre-charge current settings of CHARGER_CURRENT_PARAM_REG, depending on the temperature zone determined by the analogue circuitry of the Charger (see also the JEITA registers of the Charger's register file for the Voltage/Current levels in Warm and Cool temperature zones). 1: Charger's JEITA FSM monitoring the battery temperature checks only if battery temperature is either in the Hot or Cold zones. In that case, it notifies the main Charger FSM to stop charging automatically, when in Hot zone. The same will happen also for the case of Cold, unless the NTC_LOW_DISABLE bit-field of CHARGER_CTRL_REG is set. Note : It is not recommended to have the specific bit-field kept to 0 (and thus the JEITA support enabled), if at the same time the bit-field TBAT_PROT_ENABLE of the same register is also 0. Thus, JEITA support should be coupled with the Battery's temperature protection.	0x0
11:10	R/W	TBAT_MONITOR_MODE	Battery temperature pack monitoring modes, according to the following encoding: 00: Battery temperature state checked and updated once, as soon as the charger is powered-up and settled. 01: Battery temperature state checked periodically, depeding on	0x2

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Bit	Mode	Symbol	Description	Reset
			TBAT_MON_TIMER_REG.TBAT_MON_INTERVAL and provided that Charger has been powered-up and charger's FSM is enabled. 10: Battery temperature state checked periodically depending on TBAT_MON_TIMER_REG.TBAT_MON_INTERVAL, provided that Charger is powered-up and regardless if the Charger's FSM is enabled or not. Hence, this mode can be effective regardless of the state of CHARGE_START bit-field of CHARGER_CTRL_REG. 11: When selected, it freezes the Battery temperature monitor FSM, as soon as the latter reaches the CHECK_IDLE state (see also CHARGER_STATUS_REG.CHARGER_JEITA_STATE bit-field's description for the states of this FSM). In this mode, the monitoring of Battery temperature is possible only by checking the status of TBAT_HOT_COMP_OUT and MAIN_TBAT_COMP_OUT bit-fields of CHARGER_STATUS_REG, thus by letting SW take over monitoring. This setting may be used in conjunction with Bypass mode (by setting CHARGER_BYPASS of CHARGER_CTRL_REG), so that both charging and battery temperature status monitoring are controlled by SW.	
9	R/W	CHARGE_TIMERS_HALT_ENABLE	0: Charge timeout timers continue running when charging is disabled because of a Die or of a Battery temperature error, if and only if STOP_CHARGE_TIMERS bit-field is 0 (default). If it is 1, the counters are stopped also in TDIE_PROT and TBAT_PROT states. 1: Charge timeout timers are halted in case of a Die or of a Battery temperature error. In that case, the global charge timer is stopped as soon as the Charger's FSM moves to TDIE_PROT or TBAT_PROT state. Also, either the Pre-Charge, the CC_CHARGE or the CV_CHARGE timer is also stopped, depending on the charging state of the FSM when the Die/Battery temperature error has been detected.	0x1
8	R/W	STOP_CHARGE_TIMERS	0: Charger's Pre-Charge, CC, CV and Total charge timeout timers are ticking properly, running at the 1-Hz clock. 1: All four Charger's timeout timers are halted, counting is disabled. The counters will be reset when the FSM is either in DISABLED or in END_OF_CHARGE state. Note: Value '0' is the recommended, 1 is a test mode, since it will globally halt the four timers and thus will block the generation of the respective timer expiration IRQs.	0x0
7	R/W	NTC_LOW_DISABLE	0: Charging is disabled when the battery temperature is found to have reached the "COLD" region. Therefore, the Charger's FSM moves directly to "TBAT_PROT" error and generates an IRQ to notify the system accordingly, in case the respective IRQ mask bit of CHARGER_ERROR_IRQ_MASK_REG is set.	0x0

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Bit	Mode	Symbol	Description	Reset
			Also, CHARGER_ERROR_IRQ_STATUS_REG. TBAT_ERROR_IRQ field is updated accordingly. 1: Charging is allowed to continue, even when the battery temperature pack reaches the "COLD" region. Consequently, the FSM continues charging and no battery temperature error event is generated.	
6	R/W	TBAT_PROT_ENABLE	0: Battery temperature protection disabled 1: Battery temperature protection enabled. Charging will be stopped in case Battery temperature reaches "Hot" zone. It will also be disabled when reaching "Cold" zone, provided that CHARGER_CTRL_REG.NTC_LOW_DISABLE is not set. This is handled by the Charger's FSM, which moves directly to the respective error state (TBAT_PROT), also generating an Error IRQ if the respective IRQ mask bit is set (see also CHARGER_ERROR_IRQ_MASK_REG).	0x1
5	R/W	TDIE_ERROR_RESUME	0: FSM will not resume from a Die temperature error. Consequently, its state will be staying to "TDIE_PROT", for as long as this bit-field is kept low, regardless of the status of the die tempeture comparator. Also, disabling the specific bit-field will reset the Die temperature error debounce counter, when the Charger's FSM is in TDIE_PROT state (so when a Die temperature error has been already detected) and the specific counter will remain frozen to 0 until the TDIE_ERROR_RESUME bit-field is set (see also the TDIE_ERROR_DEBOUNCE_CNT bit-field of CHARGER_STATUS_REG). 1: FSM will resume from a Die temperature error, as soon as the respective analogue compator confirms that die temperature is again below the maximum allowed level. It is noted that the maximum Die temperature level is programmable via the CHARGER_TEMPSET_PARAM_REG register's respective bit-field (T_DIE_MAX).	0x1
4	R/W	TDIE_PROT_ENABLE	0: Die temperature protection is disabled, thus charging will not be disabled by the Charger's FSM in case of a Die temperature error. 1: Die temperature protection is enabled, thus the Charger's FSM will move to "TDIE_PROT" state, disabling charging at the same time. It is noted that the Die temperature error event will be logged in the respective status bit of CHARGER_IRQ_ERROR_STATUS_REG and an IRQ will be generated, if and only if the corresponding mask bit of CHARGER_IRQ_MASK_REG is set.	0x1
3	R/W	CHARGER_RESUME	0: Charger's FSM is not enable to resume from a charge timeout error or a Vbat OVP (Over-Voltage Protection) error. Consequently, FSM stays in "ERROR" state. 1: Charger's FSM will resume from a charge timeout or from an OVP error, thus its state will	0x1

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Bit	Mode	Symbol	Description	Reset
			move from "ERROR" to "DISABLED" state, so that the charge cycle starts-over. It is noted that in the case of a Vbat OVP error, the FSM will leave "ERROR" state, as soon as the Vbat comparator for the OVP level shows that Vbat is again OK (so lower than the OVP setting).	
2	R/W	CHARGER_BYPASS	0: Charger's FSM is active and running, notifying SW upon switching between its states 1: Charger's FSM is bypassed, so its state stays to "BYPASS", so SW should take over the monitoring of the battery voltage and control of the charger.	0x0
1	R/W	CHARGE_START	0: Charger's FSM is disabled, FSM stays at "DISABLED" state 1: Charger's FSM is enabled, so FSM's state can move from DISABLED to the actual charge states, starting from "PRE_CHARGE".	0x0
0	R/W	CHARGER_ENABLE	0: Charger's analogue circuitry is powered-down 1: Charger's analogue circuitry is being powered-up and will be available after a certain settling time (in ms). As soon as this bit-field is set, the Charger's FSM waits for this settling time, before proceeding into DISABLED state, where it checks the Vbat level, as well as the Die temperature and the Battery temperature states. This is mandatory, before the actual charging begins, so before the FSM moves to PRE_CHARGE state. It is finally noted that the settling time is configurable via CHARGER_PWR_UP_TIMER_REG, counting with the 1-kHz clock. Note: The Charger clocks must have been enabled first, by setting the CLK_SYS_REG[CLK_CHG_EN] bit-field to 1, to let the FSM proceed.	0x0

Table 259: CHARGER_STATUS_REG (0x51000608)

Bit	Mode	Symbol	Description	Reset
28:26	R	OVP_EVENTS_DEBOUNCE_CNT	The specific bit-field returns the consecutive number of times Vbat has exceeded the programmed Over-Voltage Protection (OVP) level. It is used to determine when the Charger's FSM will exit any of the charging states (PRE/CC/CV_CHARGE) and will switch to the ERROR state due to an OVP error. This will happen as soon as the respective counter of OVP events reaches or exceeds a fixed number (4), similar to the approach adopted in the End-of-Charge and Die Temperature debouncing mechanisms. The specific counter increases only while the Charger's FSM is in any of the three charging,states, the Vbat OVP interval check timer	0x0

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Bit	Mode	Symbol	Description	Reset
			has reached the threshold set and when Vbat OVP comparator's output is asserted. Note 1 : By default, as soon as the counter reaches 4, the FSM will switch to the ERROR state and the counter will reset again. Thus, in that case the specific counter ranges from 0 to 4 and vice-versa. However, if the monitoring of Vbat OVP comparator's state is less frequent than 5 (4+1) times the CHARGER_OVP_COMP_TIMER_REG[OVP_INTERVAL_CHECK_THRES] and Vbat has exceeded the OVP voltage level based on the comparator's output signal, then this counter will exceed 4 and may overflow. This will not harm, however, the detection of the OVP event, as it only increases the number of OVP event occurrences by the debounce timer, until the OVP comparator timer's settling time has expired. Thus, the Charger FSM will again switch to ERROR when the counter has reached or exceeded 4 (bit [2] of OVP_EVENTS_DEBOUNCE_CNT is set) and the OVP comparator's timer has expired. Note 2: See also the OVP_INTERVAL_CHECK_TIMER, OVP_INTERVAL_CHECK_THRES of CHARGER_OVP_COMP_TIMER_REG, for the debouncing mechanism of the Vbat OVP comparator's output.	
25:23	R	EOC_EVENTS_DEBOUNCE_CNT	The specific bit-field returns the number of times the End-of-Charge signal has been consecutively found to be high. It is used to determine when the Charger's FSM will switch from CV_CHARGE to END_OF_CHARGE state, implementing a debounce mechanism on End-of-Charge signal, coming from the analogue circuitry of the Charger towards the FSM. The specific counter, running with the Charger's 1Mhz clock: - Increases after detecting that the End-of-Charge signal is high when the respective interval for the End-of-Charge check expires. This actually happens after having detected either a positive edge on the End-of-Charge signal or after having seen the signal's level to be high (see also CHARGER_CTRL_REG[EOC_TRIGGER]) , since only after that is it possible for the interval timer to start ticking. - Resets to zero when End-of-Charge is seen low when the interval timer has expired or when an End-of-Charge negative edge is seen before the timer's expiration, starting-over. - Does not count if End-of-Charge signal is seen high and either the CV_MODE signal (also driven by the analogue circuitry) or the End-of-Charge signal of the previous clock cycle is seen low. - Is reset when the Charger's FSM is not in either the CC_CHARGE or the CV_CHARGE state or after having reached "100"(4). This is the threshold after which the End-of-Charge signal is	0x0

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Bit	Mode	Symbol	Description	Reset
			considered stable by the Charger's FSM, to switch to the END_OF_CHARGE state. Thus, in practice, the specific counter (and bit-field) ranges between 0 and 4. Note: See also the EOC_INTERVAL_CHECK_TIMER/THRES bit-fields of CHARGER_CTRL_REG.	
22:20	R	TDIE_ERROR_DEBOUNCE_CNT	The specific bit-field returns the consecutive number of times the Die temperature is seen either above (for the case of an error) or below (for the case of recovering from an error) the set Die temperature level.This is performed by a counter, which is increased: - Each time the Die temperature comparator shows that Die temperature exceeds the set level, and while charging is active, provided that Die temperature protection is enabled. If, however, the CHARGER_CTRL_REG.TDIE_PROT_ENABLE bit-field is not set, the counter is reset and stays frozen to zero. - Each time the Die temperature comparator shows that Die temperature is again below the set level, and while the FSM is in the Die temperature protection error state (TDIE_PROT) and the TDIE_ERROR_RESUME bit-field of CHARGER_CTRL_REG is set. If the specific bit-field is not set, the debounce counter is reset to 0 and it is kept frozen until the FSM is again enabled to resume from Die temperature errors. If the Die temperature comparator of the Charger's analogue circuitry shows that temperature has exceeded the programmed level for four consecutive times and charging is active, the Charger's FSM considers this as a Die temperature error and moves to the TDIE_PROT state, resetting the timer at the same time and of course halting charging. To recover from this state and resume charging, the FSM needs to see that Die temperature is below the programmed level for four consecutive times, again, provided that the TDIE_ERROR_RESUME bit-field of CHARGER_CTRL_REG is set. As soon as this happens, the error counter is again reset and the Charger's FSM resumes, by moving to PRE_CHARGE state. Consequently, the counter's value always ranges from 0 to 4. Note: When the Charger's FSM is in BYPASSED state, then this bit-field is reset and kept frozen to zero. Consequently, the number of times Die temperature has exceeded the pre-programmed threshold should be determined by SW.	0x0
19:16	R	CHARGER_JEITA_STATE	Returns the state of the Charger's JEITA FSM. This FSM is used to update the state of the battery temperature pack, depending on the value programmed in CHARGER_CTRL_REG.TBAT_MONITOR_MODE bit-field. The encoding of the states is as follows: 0x0 = CHECK_IDLE	0x0

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Bit	Mode	Symbol	Description	Reset
			0x1 = CHECK_THOT 0x2 = CHECK_TCOLD 0x3 = CHECK_TWARMER 0x4 = CHECK_TWARM 0x5 = CHECK_TCOOLER 0x6 = CHECK_TCOOL 0x7 = CHECK_TNORMAL 0x8 = UPDATE_TBAT The FSM initially is in CHECK_IDLE state and starts checking the battery's temperature by visiting the states that check for the respective temperature area (Hot, Cold, Warmer, Warm, Cooler, Cool, Normal), in this order. If the battery temperature is found to be in one of the aforementioned zones, it directly moves to UPDATE_TBAT state, to update the battery temperature's state and notify the main FSM of the Charger about the battery temperature status, before returning to the CHECK_IDLE state. A Charger State IRQ will also be generated upon refreshing the battery temperature status (see also the description of CHARGER_STATE_IRQ_MASK_REG register). Note: It is also noted that if the battery temperature is not found to be in any of the Hot, Cold, Warmer, Warm, Cooler or Cool zones, the FSM concludes that it is in the Normal zone, so between Warm and Cool. Consequently, the state CHECK_TNORMAL lasts only one (1MHz) clock cycle and is used to properly update the Battery temperature status (TBAT_STATUS) accordingly, before the last state (UPDATE_TBAT) is visited.	
15:12	R	CHARGER_STATE	Indicating the state of the Charger's main FSM, based on the following encoding: 0x0 = POWER_UP (Charger's power-up not yet set) 0x1 = INIT (Charger is being power-up, FSM waiting for the analogue to settle) 0x2 = DISABLED (Charger powered-up but charging not yet started) 0x3 = PRE_CHARGE (Pre-Charge state) 0x4 = CC_CHARGE (Constant Current state) 0x5 = CV_CHARGE (Constant Voltage state) 0x6 = END_OF_CHARGE (End-of-Charge state) 0x7 = TDIE_PROT (Die temperature protection state, visited when Die temperature limit is exceeded) 0x8 = TBAT_PROT (Battery temperature protection state, visited when Battery temperature is either COLD or HOT) 0x9 = BYPASSED (Bypassed state, visited only when the FSM is bypassed and SW takes over control) 0xA = ERROR (Error state, visited when a charge time-out occurs or in the case of Vbat exceeding over-voltage level)	0x0

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Bit	Mode	Symbol	Description	Reset
11:9	R	TBAT_STATUS	Battery pack temperature status, according to the following encoding: 0x0 : Battery temperature in COLD zone (default) 0x1 : Battery temperature in COOLER zone (above COLD) 0x2 : Battery temperature in COOL zone (above COOLER) 0x3 : Battery temperature in NORMAL zone (above COOL and below WARM zones) 0x4 : Battery temperature in WARM zone (above NORMAL) 0x5 : Battery temperature in WARMER zone (above WARM and below HOT) 0x6 : Battery temperature in HOT zone It is noted that, according to the JEITA standard (supported if the JEITA_SUPPORT_DISABLED bit-field of CHARGER_CTRL_REG is not set), if the battery pack temperature is in the "HOT" zone, charging will always be stopped. The same will happen also for the case of the COLD zone, unless the "NTC_LOW_DISABLE" bit-field of CHARGER_CTRL_REG is set. In that case, charging will be continued.	0x0
8	R	MAIN_TBAT_COMP_OUT	Returns the status of the main battery temperature comparator. This comparator by default checks if the battery temperature is in the Cold zone. However, if JEITA support is enabled and battery temperature is found to not be in either the Hot or the Cold zone, the same comparator is used to check for the Warm and Cool zones, as JEITA suggests. The specific bit-field is suggested to be used in bypass mode and when the JEITA support is disabled (so when the battery temperature is checked agains the Hot and the Cold zones). In that case, the comparator checks the battery temperature agains the Cold level and its status can be as follows: 0 = Battery temperature pack is found to be below the Cold level, so in the non-allowed Cold temperature zone. Thus, charging will be disabled, provided that the NTC_LOW_DISABLE bit-field of CHARGER_CTRL_REG is not set. 1 = Battery temperature pack is found to be above the non-allowed Cold temperature zone. Thus, charging will be continued, provided that battery temperature will not be in the Hot zone as well. When the Charger's main FSM is active and JEITA is enabled, the Charger's digital block takes over and controls the respective comparator's output.	0x0
7	R	TBAT_HOT_COMP_OUT	Returns the status of the battery temperature comparator dedicated to the Hot temperature zone. 0 = Battery temperature pack is found to be below the Hot zone 1 = Battery temperature pack is found to be in the non-allowed Hot temperature zone. Thus,	0x0

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Bit	Mode	Symbol	Description	Reset
			charging will be disabled, provided that battery temperature protection is enabled.	
6	R	TDIE_COMP_OUT	0 = Die temperature is found to be below the programmed level, set in CHARGER_TEMPSET_PARAM_REG.TDIE_SET level (normal operation) 1 = Die temperature is found to be above the set level. Charging will be disabled if Die temperature protection is enabled and the Die temperature is found to be above the set level four consecutive times (see also TDIE_ERROR_DEBOUNCE_CNT bit-field). In that case, the Charger's FSM will also move the respective error state (TDIE_PROT) and an IRQ may be generated, if the respective mask bit of CHARGER_ERROR_IRQ_MASK_REG is set.	0x0
5	R	VBAT_OVP_COMP_OUT	0 = Vbat has not exceeded the Over-Voltage Protection (OVP) voltage limit, according to the respective analogue comparator's output. 1 = Vbat is found to have exceeded the OVP voltage setting, thus charging should be disabled. The OVP voltage settings are defined in CHARGER_VOLTAGE_PARAM_REG.V_OVP (for the Normal battery temperature zone), as well as in CHARGER_JEITA_V_OVP_REG (for Cool and Warm temperature zones, to comply with JEITA).	0x0
4	R	MAIN_VBAT_COMP_OUT	This bit-field reflects the status of the main Vbat comparator residing in the analogue circuitry of the Charger. This comparator is used to check Vbat against either the Pre-Charge or the Replenish voltage level, depending on what is driven by the Charger's digital block. Thus, when the FSM is active, the comparator gets as reference the Replenish setting as soon as the FSM has reached the END_OF_CHARGE state. Otherwise,the Pre-Charge voltage setting is driven, including the Bypass mode. According to the above, the encoding is as follows for the case the comparator compares Vbat against the Pre-Charge level: 0 = Vbat has not exceeded the set Pre-Charge voltage level. 1 = Vbat has reached or exceeded the set Pre-Charge voltage level. For the case the comparator compares agains the Replenish level (when the FSM has reached the END_OF_CHARGE state, so when the charging has been completed), the encoding is as follows: 0 = Vbat has dropped below the set Replenish level, so charging will re-start and the FSM will move to the PRE_CHARGE state. 1 = Vbat is still greater or equal to the set Replenish level, thus charging remains in hold and the FSM in END_OF_CHARGE state.	0x0

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Bit	Mode	Symbol	Description	Reset
3	R	END_OF_CHARGE	0 = Actual charge current is above the current level programmed in I_END_OF_CHARGE field of CHARGER_CURRENT_PARAM_REG (or charger is off) 1 = Actual charge current is below the current level programmed in I_END_OF_CHARGE bit-field of CHARGER_CURRENT_PARAM_REG.	0x0
2	R	CHARGER_CV_MODE	0 = Charger's voltage loop not in regulation (or Charger is off) 1 = Charger's Constant Voltage (CV) mode active, voltage loop in regulation	0x0
1	R	CHARGER_CC_MODE	0 = Charger's Current loop not in regulation (or Charger is off) 1 = Charger's Constant Current (CC) mode active, current loop in regulation	0x0
0	R	CHARGER_IS_POWERED_UP	0 = Charger is either off or it is being powered-on but the analogue ciruitry is not yet settled. The charger's main FSM is either in POWER_UP or INIT states. 1 = Charger is powered-up, so its analogue ciruitry should now be settled. The Charger's FSM has left both power-up states (POWER_UP, INIT), so charging can start.	0x0

Table 260: CHARGER_VOLTAGE_PARAM_REG (0x5100060C)

Bit	Mode	Symbol	Description	Reset
23:18	R/W	V_OVP	This bit-field determines the VBAT Over-voltage protection limit. This Over-voltage protection level is used by the Charger's analogue circuitry and specifically by a dedicated comparator, the output of which is sampled by the digital block of the Charger. As soon as VBAT is detected to have reached or exceeded this level, the Charger's FSM moves to ERROR state, interrupting charging. If the respective Error IRQ mask bit is set, an Error IRQ pulse will be also generated. Regarding the actual range of supported values for this bit-field, see the the description of V_CHARGE bit-field of this register.	0x32
17:12	R/W	V_REPLENISH	This bit-field determines the absolute value (in V) of the Replenish voltage threshold. As soon as charging has been completed and the Charger's FSM has reached the END_OF_CHARGE state, the respective analogue comparator of the Charger compares VBAT with the Replenish level. If VBAT is found to have dropped below this level, charging should start-over again and in that case, the FSM moves again to the PRE_CHARGE state. Regarding the supported Replenish voltage levels, see the description of V_CHARGE bit-field.	0x21
11:6	R/W	V_PRECHARGE	This bit-field determines the voltage level at which the battery is considered as Pre-charged and therefore the Charger's FSM should move to the	0x8

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Bit	Mode	Symbol	Description	Reset
			CC_CHARGE state, entering the Constant Current charging phase. Regarding the supported Pre-Charge voltage levels, see also the description of V_CHARGE bit-field of this register.	
5:0	R/W	V_CHARGE	This bit-field determines the charge voltage levels supported. The supported levels are determined according to the following encoding: 0 : 2.80 V 1 : 2.85 V 2 : 2.90 V 3 : 2.95 V 4 : 3.00 V 5 : 3.05 V 6 : 3.10 V 7 : 3.15 V 8 : 3.20 V 9 : 3.25 V 10 : 3.30 V 11 : 3.35 V 12 : 3.40 V 13 : 3.45 V 14 : 3.50 V 15 : 3.55 V 16 : 3.60 V 17 : 3.65 V 18 : 3.70 V 19 : 3.75 V 20 : 3.80 V 21 : 3.82 V 22 : 3.84 V 23 : 3.86 V 24 : 3.88 V 25 : 3.90 V 26 : 3.92 V 27 : 3.94 V 28 : 3.96 V 29 : 3.98 V 30 : 4.00 V 31 : 4.02 V 32 : 4.04 V 33 : 4.06 V 34 : 4.08 V 35 : 4.10 V 36 : 4.12 V 37 : 4.14 V 38 : 4.16 V 39 : 4.18 V 40 : 4.20 V 41 : 4.22 V	0x2B

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Bit	Mode	Symbol	Description	Reset
			42 : 4.24 V 43 : 4.26 V 44 : 4.28 V 45 : 4.30 V 46 : 4.32 V 47 : 4.34 V 48 : 4.36 V 49 : 4.38 V 50 : 4.40 V 51 : 4.42 V 52 : 4.44 V 53 : 4.46 V 54 : 4.48 V 55 : 4.50 V 56 : 4.52 V 57 : 4.54 V 58 : 4.56 V 59 : 4.58 V 60 : 4.60 V 61 : 4.70 V 62 : 4.80 V 63 : 4.90 V* It has to be noted that the specific values correspond to the normal battery temperature zone. However, the specific register field may be updated by the JEITA FSM (which checks the battery temperature either once or periodically), in order to adapt the charge voltage to the battery temperature zone (see also CHARGER_CTRL_REG.TBAT_MONITOR_MODE field as well). This is valid also for the other three fields of the current register. Consequently, in that case the register returns the Charge voltage settings that abide to the JEITA requirements for the battery (either COOL, WARM or NORMAL). Note: Option "63" (4.90 V) is not supported for V_CHARGE, V_PRECHARGE and V_REPLENISH bit-fields (and respective levels). It should be used only in the V_OVP bit-field, as the (maximum) Over-voltage protection level.	

Table 261: CHARGER_CURRENT_PARAM_REG (0x51000610)

Bit	Mode	Symbol	Description	Reset
15	R/W	I_EOC_DOUBLE_RANGE	When set, the specific bit-field enables an increase of the (%) range of End-of-Charge current setting. Consequently, the default lower and upper limits of 6 % of I_CHARGE (value 0x0 of I_END_OF_CHARGE bit-field) and 20 % (value 0x7 of the same bit-field) are increased to 12 % and 40 % respectively, as soon as the I_EOC_DOUBLE_RANGE bit-field is set.	0x0

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Bit	Mode	Symbol	Description	Reset
14:12	R/W	I_END_OF_CHARGE	End-of-Charge current setting, ranging from 6 %("000") to 20 % ("111") of the charge current setting, with a step size of 2 %, as follows (when I_EOC_DOUBLE_RANGE = 0): 000 : 6 % 001 : 8 % 010 : 10 % 011 : 12 % 100 : 14 % 101 : 16 % 110 : 18 % 111 : 20 % When I_EOC_DOUBLE_RANGE = 1, the range is: 000 : 12 % 001 : 16 % 010 : 20 % 011 : 24 % 100 : 28 % 101 : 32 % 110 : 36 % 111 : 40 %	0x2
11:6	R/W	I_PRECHARGE	This bit-field determines the Pre-Charge current, in mA, ranging from 0.5 to 72 mA, according to the following encoding: 0 : 0.5 mA 1 : 1 mA 2 : 1.5 mA 3 : 2 mA 4 : 2.5 mA 5 : 3 mA 6 : 3.5 mA 7 : 4 mA 8 : 4.5 mA 9 : 5 mA 10 : 5.5 mA 11 : 6 mA 12 : 6.5 mA 13 : 7 mA 14 : 7.5 mA 15 : 8 mA 16 : 9 mA 17 : 10 mA 18 : 11 mA 19 : 12 mA 20 : 13 mA 21 : 14 mA 22 : 15 mA 23 : 16 mA 24 : 17 mA 25 : 18 mA	0x3

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Bit	Mode	Symbol	Description	Reset
			26 : 19 mA 27 : 20 mA 28 : 21 mA 29 : 22 mA 30 : 23 mA 31 : 24 mA 32 : 27 mA 33 : 30 mA 34 : 33 mA 35 : 36 mA 36 : 39 mA 37 : 42 mA 38 : 45 mA 39 : 48 mA 40 : 51 mA 41 : 54 mA 42 : 57 mA 43 : 60 mA 44 : 63 mA 45 : 66 mA 46 : 69 mA 47 : 72 mA 48 : 72 mA 49 : 72 mA 50 : 72 mA 51 : 72 mA 52 : 72 mA 53 : 72 mA 54 : 72 mA 55 : 72 mA 56 : 72 mA 57 : 72 mA 58 : 72 mA 59 : 72 mA 60 : 72 mA 61 : 72 mA 62 : 72 mA 63 : 72 mA	
5:0	R/W	I_CHARGE	This bit-field determines the charge current range, in mA. The range is from 5 mA to 720 mA, according to the following encoding: 0 : 5 mA 1 : 10 mA 2 : 15 mA 3 : 20 mA 4 : 25 mA 5 : 30 mA 6 : 35 mA 7 : 40 mA	0x6

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Bit	Mode	Symbol	Description	Reset
			8 : 45 mA 9 : 50 mA 10 : 55 mA 11 : 60 mA 12 : 65 mA 13 : 70 mA 14 : 75 mA 15 : 80 mA 16 : 90 mA 17 : 100 mA 18 : 110 mA 19 : 120 mA 20 : 130 mA 21 : 140 mA 22 : 150 mA 23 : 160 mA 24 : 170 mA 25 : 180 mA 26 : 190 mA 27 : 200 mA 28 : 210 mA 29 : 220 mA 30 : 230 mA 31 : 240 mA 32 : 270 mA 33 : 300 mA 34 : 330 mA 35 : 360 mA 36 : 390 mA 37 : 420 mA 38 : 450 mA 39 : 480 mA 40 : 510 mA 41 : 540 mA 42 : 570 mA 43 : 600 mA 44 : 630 mA 45 : 660 mA 46 : 690 mA 47 : 720 mA 48 : 720 mA 49 : 720 mA 50 : 720 mA 51 : 720 mA 52 : 720 mA 53 : 720 mA 54 : 720 mA 55 : 720 mA 56 : 720 mA	

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Bit	Mode	Symbol	Description	Reset
			57 : 720 mA 58 : 720 mA 59 : 720 mA 60 : 720 mA 61 : 720 mA 62 : 720 mA 63 : 720 mA Note: It has to be noted that the specific values correspond to the normal battery temperature zone. However, the specific register field may be updated by the JEITA FSM (which checks the battery temperature either once or periodically), in order to adapt the Charge current to the new battery temperature zone (see also CHARGER_CTRL_REG.TBAT_MONITOR_MODE field as well). This is valid also for the Pre-Charge current field of this register and provided that JEITA support is enabled in CHARGER_CTRL_REG. Consequently, in that case the register return the Charge current settings that abide to the JEITA requirements for the battery (either COOLER, COOL, WARM or NORMAL).	

Table 262: CHARGER_VOLTAGE_STATUS_REG (0x51000614)

Bit	Mode	Symbol	Description	Reset
23:18	R	V_OVP_SET	This bit-field returns the applied V_OVP setting. In JEITA charging, it contains the value corresponding to the present battery temperature zone, according to JEITA_V_OVP_REG. If JEITA charging is disabled, it reflects the V_OVP bit-field of CHARGER_VOLTAGE_PARAM_REG. The specific bit-field is updated by the battery monitoring (JEITA) FSM, as soon as the latter starts running. Until then, it reflects the corresponding bit-field of CHARGER_VOLTAGE_PARAM_REG.	0x36
17:12	R	V_REPLENISH_SET	This bit-field returns the applied V_REPLENISH setting. In JEITA charging, it contains the value corresponding to the present battery temperature zone, according to JEITA_V_REPLENISH_REG. If JEITA charging is disabled, it reflects the V_REPLENISH bit-field of CHARGER_VOLTAGE_PARAM_REG. The specific bit-field is updated by the battery monitoring (JEITA) FSM, as soon as the latter starts running. Until then, it reflects the corresponding bit-field of CHARGER_VOLTAGE_PARAM_REG.	0x1F
11:6	R	V_PRECHARGE_SET	This bit-field returns the applied V_PRECHARGE setting. In JEITA charging, it contains the value corresponding to the present battery temperature zone, according to JEITA_V_PRECHARGE_REG. If JEITA charging is disabled, it reflects the	0x7

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Bit	Mode	Symbol	Description	Reset
			V_PRECHARGE bit-field of CHARGER_VOLTAGE_PARAM_REG. The specific bit-field is updated by the battery monitoring (JEITA) FSM, as soon as the latter starts running. Until then, it reflects the corresponding bit-field of CHARGER_VOLTAGE_PARAM_REG.	
5:0	R	V_CHARGE_SET	This bit-field returns the applied V_CHARGE setting. In JEITA charging, it contains the value corresponding to the present battery temperature zone, according to JEITA_V_CHARGE_REG. If JEITA charging is disabled, it reflects the V_CHARGE bit-field of CHARGER_VOLTAGE_PARAM_REG. The specific bit-field is updated by the battery monitoring (JEITA) FSM, as soon as the latter starts running. Until then, it reflects corresponding the bit-field of CHARGER_VOLTAGE_PARAM_REG.	0x28

Table 263: CHARGER_CURRENT_STATUS_REG (0x51000618)

Bit	Mode	Symbol	Description	Reset
11:6	R	I_PRECHARGE_SET	This bit-field returns the applied Pre-Charge current setting. In JEITA charging, it contains the Pre-Charge value corresponding to the present battery temperature zone, according to JEITA_CURRENT/CURRENT2_SETTINGS_REG. If JEITA charging is disabled, it reflects the value of I_PRECHARGE bit-field CHARGER_CURRENT_PARAM_REG. The specific bit-field is updated by the battery monitoring (JEITA) FSM, as soon as the latter starts running. Until then, it reflects the corresponding bit-field of CHARGER_CURRENT_PARAM_REG.	0x2
5:0	R	I_CHARGE_SET	This bit-field returns the applied CC current setting. In JEITA charging, it contains the value corresponding to the present battery temperature zone, according to CHARGER_JEITA_CURRENT/CURRENT2_REG. If JEITA charging is disabled, it reflects the value of I_CHARGE bit-field CHARGER_CURRENT_PARAM_REG. The specific bit-field is updated by the battery monitoring (JEITA) FSM, as soon as the latter starts running. Until then, it reflects the corresponding bit-field of CHARGER_CURRENT_PARAM_REG.	0x5

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Table 264: CHARGER_TEMPSET_PARAM_REG (0x5100061C)

Bit	Mode	Symbol	Description	Reset
14:12	R/W	TDIE_MAX	This bit-field determines the maximum Die temperature level limit, ranging from 0 °C to 130 °C, according to the following encoding: 000: 0 °C (for test purpose only) 001: 50 °C 010: 80 °C 011: 90 °C 100: 100 °C 101: 110 °C 110: 120 °C (for test purpose only) 111: 130 °C (for test purpose only)	0x3
11:6	R/W	TBAT_HOT	This bit-field determines the battery temperature above which the charge current is zero, defining the "Hot" battery temperature zone. The range is the same with the one defined in the description of TBAT_COLD bit-field.	0x3F
5:0	R/W	TBAT_COLD	This bit-field determines the battery temperature below which the charge current is zero, defining the "Cold" zone. The covered temperatures range is provided in the following list, which also includes the "Comparator Ladder Reference" ratio. Note: the specific range has been computed using an external 12 kΩ resistor. 0: -5C/0.741 1: -4C/0.733 2: -3C/0.724 3: -2C/0.715 4: -1C/0.706 5: 0C/0.695 6: 1C/0.686 7: 2C/0.677 8: 3C/0.668 9 : 4C/0.657 10 : 5C/0.647 11 : 6C/0.638 12 : 7C/0.628 13 : 8C/0.618 14 : 9C/0.608 15 : 10C/0.596 16 : 11C/0.587 17 : 12C/0.578 18 : 13C/0.567 19 : 14C/0.557 20 : 16C/0.546 21 : 17C/0.536 22 : 18C/0.527 23 : 19C/0.517 24 : 20C/0.506 25 : 21C/0.495 26 : 22C/0.486	0xA

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Bit	Mode	Symbol	Description	Reset
			27 : 23C/0.477 28 : 24C/0.467 29 : 25C/0.457 30 : 26C/0.446 31 : 27C/0.438 32 : 28C/0.429 33 : 29C/0.419 34 : 30C/0.410 35 : 31C/0.400 36 : 32C/0.392 37 : 33C/0.383 38 : 34C/0.375 39 : 35C/0.366 40 : 36C/0.356 41 : 37C/0.349 42 : 38C/0.341 43 : 39C/0.333 44 : 40C/0.325 45 : 41C/0.316 46 : 42C/0.309 47 : 43C/0.302 48 : 44C/0.295 49 : 46C/0.287 50 : 47C/0.280 51 : 48C/0.273 52 : 49C/0.267 53 : 50C/0.260 54 : 51C/0.253 55 : 52C/0.247 56 : 53C/0.241 57 : 54C/0.235 58 : 55C/0.229 59 : 56C/0.223 60 : 57C/0.217 61 : 58C/0.212 62 : 59C/0.207 63 : 60C/0.202	

Table 265: CHARGER_TEMPSET2_PARAM_REG (0x51000620)

Bit	Mode	Symbol	Description	Reset
23:18	R/W	TBAT_WARMER	This bit-field determines the battery temperature threshold above which the "WARMER" zone is defined (between WARM and HOT). The temperature range is the same with the one defined in the description of CHARGER_TEMPSET_PARAM_REG[TBAT_COLD] bit-field.	0x37

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Bit	Mode	Symbol	Description	Reset
17:12	R/W	TBAT_WARM	This bit-field determines the battery temperature above which the charge current is reduced, defining the "WARM" temperature zone. The temperature range is the same with the one defined in the description of CHARGER_TEMPSET_PARAM_REG[TBAT_COLD] bit-field.	0x1E
11:6	R/W	TBAT_COOL	This bit-field determines the battery temperature below which the charge current is reduced, defining the "COOL" temperature zone. The temperature range is the same with the one defined in the description of CHARGER_TEMPSET_PARAM_REG[TBAT_COLD] bit-field.	0x19
5:0	R/W	TBAT_COOLER	This bit-field determines the battery temperature below which the charge current is reduced, defining the "COOLER" temperature zone (between COLD and COOL). The temperature range is the same with the one defined in the description of CHARGER_TEMPSET_PARAM_REG[TBAT_COLD] bit-field.	0x14

Table 266: CHARGER_PRE_CHARGE_TIMER_REG (0x51000624)

Bit	Mode	Symbol	Description	Reset
30:16	R	PRE_CHARGE_TIMER	Returns the current value of the Pre-Charge timeout counter, running at a 1-Hz clock. The range of the specific timer is identical to the one of the CC-Charge and the CV-Charge timers, so it may count up to 6 hours, ranging from 0 to MAX_PRE_CHARGE_TIME. It is reset to 0 when the Charger's FSM is either in DISABLED or in END_OF_CHARGE state.	0x0
15	R	-	Reserved	0x0
14:0	R/W	MAX_PRE_CHARGE_TIME	This bit-field determines the maximum time (measured in ticks of the Charger's 1-Hz clock) allowed for the Pre-Charge stage. If this is exceeded, a Pre-Charge time-out error will be captured by the Charger's control unit and its FSM will move to the respective state (ERROR). In order to exit this state and re-start charging, the CHARGER_RESUME bit-field of CHARGER_CTRL_REG must be set. Note: The specific bit-field should be always set to a non-zero value.	0x708

Table 267: CHARGER_CC_CHARGE_TIMER_REG (0x51000628)

Bit	Mode	Symbol	Description	Reset
30:16	R	CC_CHARGE_TIMER	Returns the current value of the CC-Charge timeout counter, running at a 1-Hz clock. The range of the specific timer is identical to the one of	0x0

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Bit	Mode	Symbol	Description	Reset
			the Pre-Charge and the CV-Charge timers, so it may count up to 6 hours, ranging from 0 to MAX_CC_CHARGE_TIME. It is reset to 0 when the Charger's FSM is either in DISABLED or in END_OF_CHARGE state.	
15	R	-	Reserved	0x0
14:0	R/W	MAX_CC_CHARGE_TIME	This bit-field determines the maximum time (measured in ticks of the Charger's 1-Hz clock) allowed for the CC (Constant Current) charging stage. If this is exceeded, a CC charge time-out error will be captured by the Charger's control unit and its FSM will move to the ERROR state. In order to exit this state and re-start charging, the CHARGER_RESUME bit-field of CHARGER_CTRL_REG must be set. Note: The specific bit-field should be always set to a non-zero value.	0x1C20

Table 268: CHARGER_CV_CHARGE_TIMER_REG (0x5100062C)

Bit	Mode	Symbol	Description	Reset
30:16	R	CV_CHARGE_TIMER	Returns the current value of the CV-Charge timeout counter, running at a 1-Hz clock. The range of the specific timer is identical to the one of the Pre-Charge and the CC-Charge timers, so it may count up to 6 hours, ranging from 0 to MAX_CV_CHARGE_TIME. It is reset to 0 when the Charger's FSM is either in DISABLED or in END_OF_CHARGE state.	0x0
15	R	-	Reserved	0x0
14:0	R/W	MAX_CV_CHARGE_TIME	This bit-field determines the maximum time (measured in ticks of the Charger's 1-Hz clock) allowed for the CV (Constant Voltage) charging stage. If this is exceeded, a CV charge time-out error will be captured by the Charger's control unit and its FSM will move to the ERROR state. To exit this state and re-start charging, the CHARGER_RESUME bit-field of CHARGER_CTRL_REG must be set. Note: The specific bit-field should be always set to a non-zero value.	0x1C20

Table 269: CHARGER_TOTAL_CHARGE_TIMER_REG (0x51000630)

Bit	Mode	Symbol	Description	Reset
31:16	R	TOTAL_CHARGE_TIMER	Returns the current value of the overall charge timeout counter, running at a 1-Hz clock. This timer has been set to 16 bits, so that it can count up to 10.5 hours, and ranges from 0 to MAX_TOTAL_CHARGE_TIME. It is reset to 0 when the Charger's FSM is either in DISABLED or in END_OF_CHARGE state.	0x0

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Bit	Mode	Symbol	Description	Reset
15:0	R/W	MAX_TOTAL_CHARGE_TIME	This bit-field determines the maximum overall charging time allowed (measured in ticks of the 1-Hz clock). If this is exceeded, a total charge time-out error will be captured by the Charger's controller and its FSM will move to the ERROR state. An IRQ will be also generated if the respective IRQ mask bit of CHARGER_ERROR_IRQ_MASK_REG is already set. To exit this state, the "CHARGER_RESUME" bit-field of CHARGER_CTRL_REG must be set, to enable the Charger's FSM switch from ERROR to DISABLED state and start-over. Note: The specific bit-field should be always set to a non-zero value.	0x3F48

Table 270: CHARGER_JEITA_V_CHARGE_REG (0x51000634)

Bit	Mode	Symbol	Description	Reset
23:18	R/W	V_CHARGE_TWARMER	Charge voltage setting for the Warmer battery temperature zone. Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG register.	0x29
17:12	R/W	V_CHARGE_TCOOLER	Charge voltage setting for the Cooler battery temperature zone. Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG register.	0x28
11:6	R/W	V_CHARGE_TWARM	Charge voltage setting for the Warm battery temperature zone. Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG register.	0x29
5:0	R/W	V_CHARGE_TCOOL	Charge voltage setting for the Cool battery temperature zone. Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG register.	0x28

Table 271: CHARGER_JEITA_V_PRECHARGE_REG (0x51000638)

Bit	Mode	Symbol	Description	Reset
23:18	R/W	V_PRECHARGE_TWARMER	Pre-Charge voltage setting for the Warmer battery temperature zone. Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG register.	0x6
17:12	R/W	V_PRECHARGE_TCOOLER	Pre-Charge voltage setting for the Cooler battery temperature zone. Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG register.	0x7

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Bit	Mode	Symbol	Description	Reset
11:6	R/W	V_PRECHARGE_TWARM	Pre-Charge voltage setting for the Warm battery temperature zone. Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG register.	0x6
5:0	R/W	V_PRECHARGE_TCOOL	Pre-Charge current setting for the Cool battery temperature zone. Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG register.	0x7

Table 272: CHARGER_JEITA_V_REPLENISH_REG (0x5100063C)

Bit	Mode	Symbol	Description	Reset
23:18	R/W	V_REPLENISH_TWARMER	Replenish voltage setting for the Warmer battery temperature zone. Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG.	0x1E
17:12	R/W	V_REPLENISH_TCOOLER	Replenish voltage setting for the Cooler battery temperature zone. Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG.	0x1F
11:6	R/W	V_REPLENISH_TWARM	Replenish voltage setting for the Warm battery temperature zone. Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG.	0x1E
5:0	R/W	V_REPLENISH_TCOOL	Replenish voltage setting for the Cool battery temperature zone. Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG.	0x1F

Table 273: CHARGER_JEITA_V_OVP_REG (0x51000640)

Bit	Mode	Symbol	Description	Reset
23:18	R/W	V_OVP_TWARMER	VBAT Over-voltage Protection (OVP) setting for the Warmer battery temperature zone.Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG.	0x35
17:12	R/W	V_OVP_TCOOLER	VBAT Over-voltage Protection (OVP) setting for the Cooler battery temperature zone.Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG.	0x36
11:6	R/W	V_OVP_TWARM	VBAT Over-voltage Protection (OVP) setting for the Warm battery temperature zone.Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG.	0x35

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Bit	Mode	Symbol	Description	Reset
5:0	R/W	V_OVP_TCOOL	VBAT Over-voltage Protection (OVP) setting for the Cool battery temperature zone.Regarding the range of values of this bit-field, see also the description of V_CHARGE field of CHARGER_VOLTAGE_PARAM_REG.	0x36

Table 274: CHARGER_JEITA_CURRENT_REG (0x51000644)

Bit	Mode	Symbol	Description	Reset
23:18	R/W	I_PRECHARGE_TWARM	Pre-Charge current setting for the Warm battery temperature zone. Regarding the range of values of this bit-field, see also the description of I_PRECHARGE field of CHARGER_CURRENT_PARAM_REG register.	0x1
17:12	R/W	I_PRECHARGE_TCOOL	Pre-Charge current setting for the Cool battery temperature zone. Regarding the range of values of this bit-field, see also the description of I_PRECHARGE field of CHARGER_CURRENT_PARAM_REG register.	0x2
11:6	R/W	I_CHARGE_TWARM	Charge current setting for the Warm battery temperature pack zone. Regarding the range of values of this bit-field, see also the description of I_CHARGE field of CHARGER_CURRENT_PARAM_REG register.	0x4
5:0	R/W	I_CHARGE_TCOOL	Charge current setting for the "COOL" battery temperature level. Regarding the range of values of this bit-field, see also the description of I_CHARGE field of CHARGER_CURRENT_PARAM_REG register.	0x5

Table 275: CHARGER_JEITA_CURRENT2_REG (0x51000648)

Bit	Mode	Symbol	Description	Reset
23:18	R/W	I_PRECHARGE_TWARMER	Pre-charge current settings bit-field for the "WARMER" battery temperature pack zone. Regarding the range of values of this bit-field, see also the description of I_PRECHARGE field of CHARGER_CURRENT_PARAM_REG register.	0x1
17:12	R/W	I_PRECHARGE_TCOOLER	Pre-charge current settings bit-field for the "COOLER" battery temperature pack zone. Regarding the range of values of this bit-field, see also the description of I_PRECHARGE field of CHARGER_CURRENT_PARAM_REG register.	0x2
11:6	R/W	I_CHARGE_TWARMER	Charge current settings bit-field for the "WARMER" battery temperature pack zone. Regarding the range of values of this bit-field, see also the description of I_CHARGE field of CHARGER_CURRENT_PARAM_REG register.	0x4
5:0	R/W	I_CHARGE_TCOOLER	Charge current settings bit-field for the "COOLER" battery temperature pack zone. Regarding the range of values of this bit-field, see also the description of I_CHARGE field of CHARGER_CURRENT_PARAM_REG register.	0x5

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Table 276: CHARGER_VBAT_COMP_TIMER_REG (0x5100064C)

Bit	Mode	Symbol	Description	Reset
25:16	R	VBAT_COMP_TIMER	Returns the current value of the timer used to determine when the output of the Vbat comparator (checking Vbat vs Pre_Charge and Replenish levels) must be sampled by the digital. As soon as the timer expires (down-counting to 0, starting from the value set in VBAT_COMP_SETTLING), the comparator's output is latched by the Charger's digital block and used by the FSM. Note: When the Charger's FSM is in BYPASSED state, this timer is kept to zero and the SW takes over. In this mode, the specific comparator checks the level of Vbat against the Pre-Charge level. Hence, SW can periodically sample the status of this comparator by reading the MAIN_VBAT_COMP_OUT bit-field of CHARGER_STATUS_REG, to determine if Vbat has exceeded the Pre-Charge level or not.	0x0
15:10	R	-	Reserved	0x0
9:0	R/W	VBAT_COMP_SETTLING	Settling time threshold (in µs) for the Vbat comparator checking Vbat vs the programmed Pre-Charge and Replenish levels. The settings (voltage levels) of the comparator are controlled by the digital block of the Charger and they are driven based on the state of the main FSM (PRE_CHARGE, END_OF_CHARGE).	0x63

Table 277: CHARGER_VOVP_COMP_TIMER_REG (0x51000650)

Bit	Mode	Symbol	Description	Reset
31:26	R	OVP_INTERVAL_CHECK_TIMER	The specific bit-field determines the current state of the timer used to periodically check the output of the Over-Voltage Protection comparator's output signal, as soon as the Charger's FSM reaches any of the charging states (PRE/CC/CV_CHARGE). When this happens, the timer starts ticking with the 1 MHz clock, ranging from 0 up to the programmed interval threshold (see also OVP_INTERVAL_CHECK_THRES field). As soon as this timer reaches the programmed threshold value, the Vbat OVP comparator's output is evaluated, increasing or not the counter keeping the consecutive OVP events. It is noted that out of the charging states, the specific timer is kept frozen to zero, not counting. Note : See also the OVP_OCCURRENCES_CNT bit-field of CHARGER_STATUS_REG for the consecutive OVP events counter.	0x0
25:16	R	VBAT_OVP_COMP_TIMER	Returns the current value of the timer used to determine when the Vbat Over-Voltage protection (OVP) comparator's output must be sampled by the digital. As soon as the timer expires (down-counting to 0, starting from	0x0

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Bit	Mode	Symbol	Description	Reset
			VBAT_OVP_COMP_SETTLING), the comparator's output is latched by the Charger's digital block and used by the main FSM. Note: When the Charger's FSM is in BYPASSED state, this timer is kept to zero and the SW takes over, sampling the status of the VBAT_OVP_COMP_OUT bit-field of CHARGER_STATUS_REG to determine if the Vbat has exceeded the OVP limit.	
15:10	R/W	OVP_INTERVAL_CHECK_THRES	This bit-field determines the periodic interval of checking the dedicated Vbat OVP comparator's output, when the Charger's FSM is in any of the charging states (PRE/CC/CV_CHARGE). The implementation is based on a dedicated timer, counting from zero up to the value programmed into this bit-field (see also OVP_INTERVAL_CHECK_TIMER field's description) and only when the FSM is in any of the three charging states. Out of these states, the timer is kept frozen to zero. As soon as this timer reaches the programmed threshold, the Vbat OVP comparator's output is sampled and depending on its level, (high or low), another counter, keeping the number of consecutive OVP events, is increased or not. The programmed threshold value should always be non-zero. Note: See also the OVP_DEBOUNCE_CNT bit-field of CHARGER_STATUS_REG, for the consecutive OVP events counter.	0x3F
9:0	R/W	VBAT_OVP_COMP_SETTLING	Settling time threshold (in µs) for the Vbat comparator checking Vbat vs the programmed Over-Voltage level.	0x63

Table 278: CHARGER_TDIE_COMP_TIMER_REG (0x51000654)

Bit	Mode	Symbol	Description	Reset
25:16	R	TDIE_COMP_TIMER	Returns the current value of the timer used to determine when the Die temperature comparator's output must be sampled by the digital. As soon as the timer expires (down-counting to 0, starting from TDIE_COMP_SETTLING) the comparator's output is latched by the Charger's digital block and used by the main FSM. After expiring, the timer starts-over again, down-counting, to enable the continuous monitoring of Die temperature by the digital. Note: When the Charger's FSM is in BYPASSED state, this timer is kept to zero and the SW takes over, sampling the status of the TDIE_PROT_COMP_OUT bit-field of CHARGER_STATUS_REG to determine if the Die temperature limit has been exceeded.	0x0
15:10	R	-	Reserved	0x0
9:0	R/W	TDIE_COMP_SETTLING	Settling time threshold (in us) for the Die temperature comparator.	0x63

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Table 279: CHARGER_TBAT_MON_TIMER_REG (0x51000658)

Bit	Mode	Symbol	Description	Reset
25:16	R	TBAT_MON_TIMER	This is the battery temperature monitoring timer, counting with the Charger's 1-kHz clock. If the battery monitor mode is accordingly set in the TBAT_MONITOR_MODE bit-field of CHARGER_CTRL_REG (so either to 0x1 or 0x2), this timer is initially loaded with the value set in TBAT_MON_INTERVAL bit-field in the subsequent 1-kHz cycles starts down-counting to 0. As soon as the specific timer expires,the JEITA FSM starts-over again, to refresh the battery temperature status.	0x0
15:10	R	-	Reserved	0x0
9:0	R/W	TBAT_MON_INTERVAL	Timing interval (in ms) for the Battery temperature monitoring. This interval determines how often the JEITA FSM will be checking and potentially refreshing the Battery temperature status, by selecting accordingly the proper level (Hot, Cold, Warm, Cool or Normal), based on the feedback of the two battery temperature comparators being present in the Charger's analogue circuitry (one for the Hot level and one for Cold, Cool and Warm, to support JEITA). Note: The specific bit-field should be always set to a non-zero value.	0x63

Table 280: CHARGER_TBAT_COMP_TIMER_REG (0x5100065C)

Bit	Mode	Symbol	Description	Reset
25:16	R	TBAT_COMP_TIMER	Returns the main battery temperature comparator's timer, used for the latching of the comparator's output. The output of the comparator is used by the JEITA FSM, to determine the current battery temperature pack's status.	0x0
15:10	R	-	Reserved	0x0
9:0	R/W	TBAT_COMP_SETTLING	Settling time (specified in us) for the main battery temperature comparator, checking for the "COOL", "COLD" and "WARM" levels. The charger's digital block uses a dedicated timer to sample the specific comparator's output. The comparator's output is latched as soon as the timer expires, reaching 0. Then, the timer is reloaded with the settling time value and starts-over, down-counting to 0. Note: The specific bit-field should be always set to a non-zero value.	0x63

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Table 281: CHARGER_THOT_COMP_TIMER_REG (0x51000660)

Bit	Mode	Symbol	Description	Reset
25:16	R	THOT_COMP_TIMER	Returns the battery temperature comparator's timer dedicated for the "Hot" level.	0x0
15:10	R	-	Reserved	0x0
9:0	R/W	THOT_COMP_SETTLING	Charger's battery temperature comparator settling time (specified in us), specifically for the Hot temperature zone. The charger's digital block uses a dedicated timer to sample the specific comparator's output. The comparator's output is latched as soon as the timer expires, reaching 0. Then, the timer is reloaded with the settling time value and starts-over again Note: The specific bit-field should be always set to a non-zero value.	0x63

Table 282: CHARGER_PWR_UP_TIMER_REG (0x51000664)

Bit	Mode	Symbol	Description	Reset
20:16	R	CHARGER_PWR_UP_TIMER	Returns the current value of the charger's power-up timer, running with the 1Khz clock. Note: The specific timer is reset to the value programmed to CHARGER_PWR_UP_SETTLING bit-field, when the Charger's analogue circuitry has been enabled, after being disabled initially. By setting CHARGER_CTRL_REG[CHARGER_ENABLE] to '0', the analogue part is disabled and in order to be properly enable, SW has to wait for 1ms (one 1Khz clock period) time. The latter is is needed to ensure that the power-up timer's control signals in the Charger's digital part will be cleared when the analogue part is again enabled, so that a proper new start-up of the Charger's FSM is possible.	0x0
15:5	R	-	Reserved	0x0
4:0	R/W	CHARGER_PWR_UP_SETTLING	This bit-field determines the charger's power-up (settling) time, required for the analogue circuitry of the charger. As soon as the charger is powered-on by setting the CHARGER_ENABLE bit-field of CHARGER_CTRL_REG, the charger's FSM loads a dedicated timer with this value and waits for this timer to expire, before proceeding to the next states. Note: The specific bit-field should be always set to a non-zero value.	0x2

Table 283: CHARGER_STATE_IRQ_MASK_REG (0x51000668)

Bit	Mode	Symbol	Description	Reset
11	R/W	CV_TO_PRECHARGE_IRQ_EN	When set, this bit-field enables the IRQ generation as soon as the Charger's FSM switches from CV_CHARGE to PRE_CHARGE state.	0x0

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Bit	Mode	Symbol	Description	Reset
10	R/W	CC_TO_PRECHARGE_IRQ_EN	When set, this bit-field enables the IRQ generation as soon as the Charger's FSM switches from CC_CHARGE to PRE_CHARGE state.	0x0
9	R/W	CV_TO_CC_IRQ_EN	When set, this bit-field enables the IRQ generation as soon as the Charger's FSM switches from CV_CHARGE to CC_CHARGE state.	0x0
8	R/W	TBAT_STATUS_UPDATE_IRQ_EN	When set, this bit-field enables the generation of the Charger's state IRQ as soon as the battery temperature status is refreched by the Charger's Battery temperature monitor (JEITA) FSM. As soon as the specific FSM checks the current battery temperature level, it notifies the main Charger FSM that it has run and that the Battery temperature pack state is checked (and potentially refreshed with a new status).	0x0
7	R/W	TBAT_PROT_TO_PRECHARGE_IRQ_EN	When set, this bit-field enables the Charger's state IRQ generation as soon as the Charger's FSM switches from the Battery temperature protection state (TBAT_PROT) to PRE_CHARGE, resuming charging.	0x0
6	R/W	TDIE_PROT_TO_PRECHARGE_IRQ_EN	When set, this bit-field enables the Charger's state IRQ generation as soon as the Charger's FSM switches from the Die temperature protection state (TDIE_PROT) to PRE_CHARGE, resuming charging.	0x0
5	R/W	EOC_TO_PRECHARGE_IRQ_EN	When set, this bit-field enables the Charger's State IRQ generation as soon as the Charger's FSM switches from END_OF_CHARGE again to PRE_CHARGE state. This happens when the Vbat voltage level is detected to be below the Replenish level set.	0x0
4	R/W	CV_TO_EOC_IRQ_EN	When set, this bit-field enables the IRQ generation as soon as the Charger's FSM switches from CV_CHARGE to END_OF_CHARGE state.	0x0
3	R/W	CC_TO_EOC_IRQ_EN	When set, this bit-field enables the IRQ generation as soon as the Charger's FSM switches from CC_CHARGE to END_OF_CHARGE state.	0x0
2	R/W	CC_TO_CV_IRQ_EN	When set, this bit-field enables the IRQ generation as soon as the Charger's FSM switches from CC_CHARGE to CV_CHARGE state.	0x0
1	R/W	PRECHARGE_TO_CC_IRQ_EN	When set, this bit-field enables the IRQ generation as soon as the Charger's FSM switches from PRE_CHARGE to CC_CHARGE state.	0x0
0	R/W	DISABLED_TO_PRECHARGE_IRQ_EN	When set, this bit-field enables the IRQ generation as soon as the Charger's FSM switches from DISABLED to PRE_CHARGE state.	0x0

Table 284: CHARGER_ERROR_IRQ_MASK_REG (0x5100066C)

Bit	Mode	Symbol	Description	Reset
6	R/W	TBAT_ERROR_IRQ_EN	When set, it enables the generation of Battery temperature IRQs.The IRQ is generated as soon as the JEITA FSM detects that the battery temperature is either in the "Hot" or in the "Cold"	0x0

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Bit	Mode	Symbol	Description	Reset
			temperature region, by sampling the respective comparators' output.	
5	R/W	TDIE_ERROR_IRQ_EN	When set, it enables the generation of Die temperature error IRQs. The IRQ is generated as soon as Die temperature error is captured, so as soon as the Charger's FSM moves to the TDIE_PROT state. For this to happen, the Die temperature comparator should indicate that Die temperature has exceeded the limit defined in CHARGER_TEMPSET_PARAM_REG.TDIE_MAX.	0x0
4	R/W	VBAT_OVP_ERROR_IRQ_EN	When set, it enables the generation of VBAT_OVP IRQs. The IRQ is generated as soon as the dedicated Vbat comparator shows that Vbat has exceeded the OVP level and the Charger's FSM has switched to the respective error state ("ERROR").	0x0
3	R/W	TOTAL_CHARGE_TIMEOUT_IRQ_EN	When set, it enables the total charge timeout IRQs. The IRQ is generated as soon as the Charger's global charge timer expires, reaching 0.	0x0
2	R/W	CV_CHARGE_TIMEOUT_IRQ_EN	When set, it enables the CV charge timeout IRQs. The IRQ is generated as soon as the Charger's state timer expires, reaching 0 when the FSM is in the CV_CHARGE state.	0x0
1	R/W	CC_CHARGE_TIMEOUT_IRQ_EN	When set, it enables the CC charge timeout IRQs. The IRQ is generated as soon as the Charger's state timer, expires, reaching 0.	0x0
0	R/W	PRECHARGE_TIMEOUT_IRQ_EN	When set, it enables the Pre-Charge timeout IRQs. The IRQ is generated as soon as the Charger's state timer expires, reaching 0.	0x0

Table 285: CHARGER_STATE_IRQ_STATUS_REG (0x51000670)

Bit	Mode	Symbol	Description	Reset
11	R	CV_TO_PRECHARGE_IRQ	0 = No transition of the Charger's FSM from CV_CHARGE to PRE_CHARGE state has been captured 1 = Charger's FSM has switched from CV_CHARGE to PRE_CHARGE state	0x0
10	R	CC_TO_PRECHARGE_IRQ	0 = No transition of the Charger's FSM from CC_CHARGE to PRE_CHARGE state has been captured 1 = Charger's FSM has switched from CC_CHARGE to PRE_CHARGE state	0x0
9	R	CV_TO_CC_IRQ	0 = No transition of the Charger's FSM from CV_CHARGE to CC_CHARGE state has been captured 1 = Charger's FSM has switched from CV_CHARGE to CC_CHARGE state	0x0
8	R	TBAT_STATUS_UPDATE_IRQ	0 = No battery temperature status update event has been captured 1 = Battery temperature pack's status has been checked and refreshed by the Charger's Battery	0x0

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Bit	Mode	Symbol	Description	Reset
			temperature monitor FSM. Thus, the new status of the battery temperature should be checked by SW.	
7	R	TBAT_PROT_TO_PRECHARGE_IRQ	0 = No transition of the Charger's FSM from TBAT_PROT to PRE_CHARGE state has been captured 1 = Charger's FSM has switched from TBAT_PROT to PRE_CHARGE state, resuming charging after having recovered from a battery temperature error.	0x0
6	R	TDIE_PROT_TO_PRECHARGE_IRQ	0 = No transition of the Charger's FSM from TDIE_PROT to PRE_CHARGE state has been captured 1 = Charger's FSM has switched from TDIE_PROT to PRE_CHARGE state, resuming charging after having recovered from a Die temperature error.	0x0
5	R	EOC_TO_PRECHARGE_IRQ	0 = No transition of the Charger's FSM from END_OF_CHARGE to PRE_CHARGE state has been captured 1 = Charger's FSM has switched from END_OF_CHARGE to PRE_CHARGE state	0x0
4	R	CV_TO_EOC_IRQ	0 = No transition of the Charger's FSM from CV_CHARGE to END_OF_CHARGE state has been captured 1 = Charger's FSM has switched from CV_CHARGE to END_OF_CHARGE state	0x0
3	R	CC_TO_EOC_IRQ	0 = No transition of the Charger's FSM from CC_CHARGE to END_OF_CHARGE state has been captured 1 = Charger's FSM has switched from CC_CHARGE to END_OF_CHARGE state	0x0
2	R	CC_TO_CV_IRQ	0 = No transition of the Charger's FSM from CC_CHARGE to CV_CHARGE state has been captured 1 = Charger's FSM has switched from CC_CHARGE to CV_CHARGE state	0x0
1	R	PRECHARGE_TO_CC_IRQ	0 = No transition of the Charger's FSM from PRE_CHARGE to CC_CHARGE state has been captured 1 = Charger's FSM has switched from PRE_CHARGE to CC_CHARGE state	0x0
0	R	DISABLED_TO_PRECHARGE_IRQ	0 = No transition of the Charger's FSM from DISABLED to PRE_CHARGE state has been captured 1 = Charger's FSM has switched from DISABLED to PRE_CHARGE state	0x0

Table 286: CHARGER_ERROR_IRQ_STATUS_REG (0x51000674)

Bit	Mode	Symbol	Description	Reset
6	R	TBAT_ERROR_IRQ	0 = No Battery temperature error IRQ event is captured, so charging may continue	0x0

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Bit	Mode	Symbol	Description	Reset
			1 = A Battery temperature error IRQ event has been captured, declaring that the Charger's FSM has moved to the respective error state (TBAT_PROT). Note : The status bit is updated automatically when the Battery temperature is detected to be either in the HOT or in the COLD zone, regardless of the state of the respective IRQ mask bit.	
5	R	TDIE_ERROR_IRQ	0 = No Die temperature error IRQ events have been captured, so charging may continue 1 = A Die temperature error IRQ event is captured, declaring that the Charger's FSM has switched to the respective error state (TDIE_PROT) and charging will be automatically stopped. Note : The status bit is updated automatically when a Die temperature error is detected, thus when the die temperature is found to have exceeded the programmed level, regardless of the state of the respective IRQ mask bit. The same applies to all the other status bits of the specific register.	0x0
4	R	VBAT_OVP_ERROR_IRQ	0 = Vbat has not exceeded the Over-Voltage Protection (OVP) level, so charging may continue 1 = Vbat has exceeded the Over-Voltage level, thus an OVP error event has been captured. The Charger's FSM switches to the respective error state (ERROR) as soon as the OVP event is captured by the digital part of the Charger and charging will be automatically stopped.	0x0
3	R	TOTAL_CHARGE_TIMEOUT_IRQ	0 = Total charge time counter has not yet reached the maximum charge time (set in CHARGER_TOTAL_CHARGE_TIME_REG) 1 = Total charge time counter has reached the maximum charge time programmed. The Charger's FSM will move to the respective error state (ERROR) and charging will be automatically stopped, as soon as the specific event is captured.	0x0
2	R	CV_CHARGE_TIMEOUT_IRQ	0 = State charge time counter has not yet reached the maximum CV charge time (set in CHARGER_CV_CHARGE_TIME_REG) 1 = Total charge time counter has reached the maximum CV charge time programmed. The Charger's FSM will move to the respective error state (ERROR) and charging will be automatically stopped, as soon as the specific event is captured.	0x0
1	R	CC_CHARGE_TIMEOUT_IRQ	0 = State charge time counter has not yet reached the maximum CC charge time (set in CHARGER_CC_CHARGE_TIME_REG) 1 = Total charge time counter has reached the maximum CC charge time programmed. The Charger's FSM will move to the respective error state (ERROR) and charging will be automatically stopped, as soon as the specific event is captured.	0x0
0	R	PRECHARGE_TIMEOUT_IRQ	0 = State charge time counter has not yet reached the maximum Pre-charge time (set in CHARGER_PRECHARGE_TIME_REG)	0x0

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Bit	Mode	Symbol	Description	Reset
			1 = Total charge time counter has reached the maximum Pre-charge time programmed. The Charger's FSM will move to the respective error state (ERROR) and charging will be automatically stopped, as soon as the specific event is captured.	

Table 287: CHARGER_STATE_IRQ_CLR_REG (0x51000678)

Bit	Mode	Symbol	Description	Reset
11	R0/W	CV_TO_PRECHARGE_IRQ_CLR	Writing a 1 will reset the respective Charger's State IRQ status bit ; writing a 0 will have no effect	0x0
10	R0/W	CC_TO_PRECHARGE_IRQ_CLR	Writing a 1 will reset the respective Charger's State IRQ status bit ; writing a 0 will have no effect	0x0
9	R0/W	CV_TO_CC_IRQ_CLR	Writing a 1 will reset the respective Charger's State IRQ status bit ; writing a 0 will have no effect	0x0
8	R0/W	TBAT_STATUS_UPDATE_IRQ_CLR	Writing a 1 will reset the Battery temperature status update IRQ status bit ; writing a 0 will have no effect	0x0
7	R0/W	TBAT_PROT_TO_PRECHARGE_IRQ_CLR	Writing a 1 will reset the respective Charger's State IRQ status bit ; writing a 0 will have no effect	0x0
6	R0/W	TDIE_PROT_TO_PRECHARGE_IRQ_CLR	Writing a 1 will reset the respective Charger's State IRQ status bit ; writing a 0 will have no effect	0x0
5	R0/W	EOC_TO_PRECHARGE_IRQ_CLR	Writing a 1 will reset the respective Charger's State IRQ status bit ; writing a 0 will have no effect	0x0
4	R0/W	CV_TO_EOC_IRQ_CLR	Writing a 1 will reset the respective Charger's State IRQ status bit ; writing a 0 will have no effect	0x0
3	R0/W	CC_TO_EOC_IRQ_CLR	Writing a 1 will reset the respective Charger's State IRQ status bit ; writing a 0 will have no effect	0x0
2	R0/W	CC_TO_CV_IRQ_CLR	Writing a 1 will reset the respective Charger's State IRQ status bit ; writing a 0 will have no effect	0x0
1	R0/W	PRECHARGE_TO_CC_IRQ_CLR	Writing a 1 will reset the respective Charger's State IRQ status bit ; writing a 0 will have no effect	0x0
0	R0/W	DISABLED_TO_PRECHARGE_IRQ_CLR	Writing a 1 will reset the respective Charger's State IRQ status bit ; writing a 0 will have no effect	0x0

Table 288: CHARGER_ERROR_IRQ_CLR_REG (0x5100067C)

Bit	Mode	Symbol	Description	Reset
6	R0/W	TBAT_ERROR_IRQ_CLR	Writing a 1 will reset the respective Charger's Error IRQ status bit ; writing a 0 will have no effect	0x0
5	R0/W	TDIE_ERROR_IRQ_CLR	Writing a 1 will reset the respective Charger's Error IRQ status bit ; writing a 0 will have no effect	0x0
4	R0/W	VBAT_OVP_ERROR_IRQ_CLR	Writing a 1 will reset the respective Charger's Error IRQ status bit ; writing a 0 will have no effect	0x0

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Bit	Mode	Symbol	Description	Reset
3	R0/W	TOTAL_CHARGE_TIMEOUT_IRQ_CLR	Writing a 1 will reset the respective Charger's Error IRQ status bit ; writing a 0 will have no effect	0x0
2	R0/W	CV_CHARGE_TIMEOUT_IRQ_CLR	Writing a 1 will reset the respective Charger's Error IRQ status bit ; writing a 0 will have no effect	0x0
1	R0/W	CC_CHARGE_TIMEOUT_IRQ_CLR	Writing a 1 will reset the respective Charger's Error IRQ status bit ; writing a 0 will have no effect	0x0
0	R0/W	PRECHARGE_TIMEOUT_IRQ_CLR	Writing a 1 will reset the respective Charger's Error IRQ status bit ; writing a 0 will have no effect	0x0

Table 289: CHARGER_LOCK_REG (0x51000680)

Bit	Mode	Symbol	Description	Reset
15	RWS	CHARGER_SWLOCK_EN	0 = SW-based protection of Charger registers is disabled, protection is dependent on the value of bits [14:0] 1 = SW-based protection of Charger registers is active. Thus, if any of the 15 lock bits is non-set, the respective Charger register can be locked and back un-locked for writing, if the proper lock/un-lock sequence of writes is issued to CHARGER_SWLOCK_REG.	0x0
14	RWS	JEITA_I_CHARGE2_LOCK	0 = CHARGER_JEITA_CURRENT2_REG is un-locked, register writes are allowed 1 = CHARGER_JEITA_CURRENT2_REG is locked, register writes are not allowed	0x0
13	RWS	JEITA_I_CHARGE_LOCK	0 = CHARGER_JEITA_CURRENT_REG is un-locked, register writes are allowed 1 = CHARGER_JEITA_CURRENT_REG is locked, register writes are not allowed	0x0
12	RWS	JEITA_V_OVP_LOCK	0 = CHARGER_JEITA_V_OVP_REG is un-locked, register writes are allowed 1 = CHARGER_JEITA_V_OVP_REG is locked, register writes are not allowed	0x0
11	RWS	JEITA_V_PRECHARGE_LOCK	0 = CHARGER_JEITA_V_PRECHARGE_REG is un-locked, register writes are allowed 1 = CHARGER_JEITA_V_PRECHARGE_REG is locked, register writes are not allowed	0x0
10	RWS	JEITA_V_CHARGE_LOCK	0 = CHARGER_JEITA_V_CHARGE_REG is un-locked, register writes are allowed 1 = CHARGER_JEITA_V_CHARGE_REG is locked, register writes are not allowed	0x0
9	RWS	TOTAL_CHARGE_TIMEOUT_LOCK	0 = CHARGER_TOTAL_CHARGE_TIMER_REG is un-locked, register writes are allowed 1 = CHARGER_TOTAL_CHARGE_TIMER_REG is locked, register writes are not allowed	0x0
8	RWS	CV_CHARGE_TIMEOUT_LOCK	0 = CHARGER_CV_CHARGE_TIMER_REG is un-locked, register writes are allowed 1 = CHARGER_CV_CHARGE_TIMER_REG is locked, register writes are not allowed	0x0

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Bit	Mode	Symbol	Description	Reset
7	RWS	CC_CHARGE_TIMEOUT_LOCK	0 = CHARGER_CC_CHARGE_TIMER_REG is un-locked, register writes are allowed 1 = CHARGER_CC_CHARGE_TIMER_REG is locked, register writes are not allowed	0x0
6	RWS	PRECHARGE_TIMEOUT_LOCK	0 = CHARGER_PRE_CHARGE_TIMER_REG is un-locked, register writes are allowed 1 = CHARGER_PRE_CHARGE_TIMER_REG is locked, register writes are not allowed	0x0
5	RWS	TEMPSET2_PARAM_LOCK	0 = CHARGER_TEMPSET2_PARAM_REG is un-locked, register writes are allowed 1 = CHARGER_TEMPSET2_PARAM_REG is locked, register writes are not allowed	0x0
4	RWS	TEMPSET_PARAM_LOCK	0 = CHARGER_TEMPSET_PARAM_REG is un-locked, register writes are allowed 1 = CHARGER_TEMPSET_PARAM_REG is locked, register writes are not allowed	0x0
3	RWS	CURRENT_PARAM_LOCK	0 = CHARGER_CURRENT_PARAM_REG is un-locked, writes are allowed 1 = All bit-fields of the register are locked, writes are not allowed	0x0
2	RWS	VOLTAGE_PARAM_LOCK	0 = CHARGER_VOLTAGE_PARAM_REG is un-locked, register writes are allowed 1 = All bit-fields except of V_REPLENISH are locked, register writes to these bit-fields are not allowed	0x0
1	RWS	CHARGER_TEST_CTRL_LOCK	0 = CHARGER_TEST_CTRL_REG is un-locked, register writes are allowed 1 = CHARGER_TEST_CTRL_REG is locked, register writes are not allowed	0x0
0	RWS	CHARGER_CTRL_LOCK	0 = Protected bit-fields of CHARGER_CTRL_REG are un-locked, register writes are allowed 1 = Protected bit-fields are locked, register writes are not allowed The protected bit-fields of CHARGER_CTRL_REG are: CHARGER_BYPASS, TDIE_PROT_ENABLE, TBAT_PROT_ENABLE, NTC_LOW_DISABLE, STOP_CHARGE_TIMERS, TBAT_MONITOR_MODE and JEITA_SUPPORT_DISABLED. Note: All the CHARGER_LOCK_REG bits are set-only bits. So if any of them is set by writing a 1, it cannot be unset by writing a 0.	0x0

Table 290: CHARGER_SWLOCK_REG (0x51000684)

Bit	Mode	Symbol	Description	Reset
2:1	R	SWLOCK_FSM_STATE	Returns the state of the FSM detecting the sequence of writes that either enable (lock) or disable (un-lock) the protection to the Charger registers/register bit-fields, protected also through	0x0

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Bit	Mode	Symbol	Description	Reset
			CHARGER_LOCK_REG (bits [14:0]). The supported states are: - WORD0 : First write expected, either when the SW protection is active (SWLOCK_STATUS = 1) or inactive (0). - WORD1 : Second write expected. If the data written is the proper one, the FSM continues to WORD2 state, otherwise it starts over from state WORD0. - WORD2 : Third and last write expected. In this state, the FSM expects the proper write to toggle the SWLOCK_STATUS bit and switches from lock (default) to un-lock state and vice-versa. From WORD2, the FSM always switches to WORD0. The lock and un-lock data sequences that must be written to this register are provided right below, for the sake of completeness. - LOCK sequence: 0x3768, 0x8673, 0xDEAD - UNLOCK sequence: 0x756E ("un"), 0x6C6F ("lo"), 0x636B ("ck") It is noted that locking is effective only if bit [15] of CHARGER_LOCK_REG is set to 1. Otherwise, even if the sequence of data written by SW is the proper one, the locking through this mechanism will not be achieved and the registers will be protected or not depending on the state of the respective bits ([14:0]) of CHARGER_LOCK_REG.	
0	R	SWLOCK_STATUS	0 = SW locking is not active, writes to the protected Charger registers are allowed depending on CHARGER_LOCK_REG (bits [14:0]) 1 = SW locking will be activated as soon as the (set-only) bit [15] of CHARGER_LOCK_REG is set. In that case, writes are not allowed to all the protected* Charger registers and register bit-fields, regardless of the bits [14:0] of CHARGER_LOCK_REG. The specific bit becomes 1 only if the SW locking sequence of writes to this register is applied (see also SWLOCK_FSM_STATE bit-field for the lock/un-lock sequences). It can be unset only if the SW un-lock write sequence is applied. *Note: The protected Charger registers covered by the SW lock/un-lock mechanism are the ones protected also by the bits [14:0] of CHARGER_LOCK_REG, and which are mentioned in the register descriptions of the respective bit-fields.	0x1

44.6 Clock Generation Controller Registers

Table 291: Register map CRG

Address	Register	Description
0x50020904	CLK_SNC_REG	Peripheral divider register

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Address	Register	Description
0x50020908	SET_CLK_SNC_REG	Peripheral divider register SET register. Reads back 0x0000
0x5002090C	RESET_CLK_SNC_REG	Peripheral divider register RESET register. Reads back 0x0000
0x50040400	CLK_SYS_REG	Peripheral divider register
0x50040408	SET_CLK_SYS_REG	Peripheral divider SET register
0x5004040C	RESET_CLK_SYS_REG	Peripheral divider RESET register
0x50040410	BATCHECK_REG	
0x50050400	XTAL32M_START_REG	Trim values for XTAL32M in START state of startup
0x50050404	XTAL32M_SETTLE_REG	Trim values for XTAL32M in SETTLE state of startup
0x50050408	XTAL32M_TRIM_REG	Trim values for XTAL32M in RUNNING state
0x5005040C	XTAL32M_CAP_MEAS_REG	Capacitance measure circuit control
0x50050410	XTAL32M_FSM_REG	Startup state machine configuration
0x50050414	XTAL32M_CTRL_REG	Xtal32m control register
0x50050418	XTAL32M_IRQ_CTRL_REG	Xtal32m Interrupt control register
0x50050424	XTAL32M_STAT0_REG	XTAL32M status register
0x50050428	XTAL32M_IRQ_STAT_REG	XTAL32M IRQ status register
0x50050460	PLL_SYS_CTRL1_REG	System PLL control register 1.
0x50050464	PLL_SYS_CTRL2_REG	System PLL control register 2.
0x50050468	PLL_SYS_CTRL3_REG	System PLL control register 3.
0x50050470	PLL_SYS_STATUS_REG	System PLL status register.
0x50050474	PLL_USB_CTRL1_REG	USB PLL control register 1.
0x50050478	PLL_USB_CTRL2_REG	USB PLL control register 2.
0x5005047C	PLL_USB_CTRL3_REG	USB PLL control register 3.
0x50050480	PLL_USB_STATUS_REG	USB PLL status register.
0x50050490	SYS_IRQ_CTRL_REG	System IRQ control register
0x50050494	SET_SYS_IRQ_CTRL_REG	System IRQ SET register
0x50050498	RESET_SYS_IRQ_CTRL_REG	System IRQ RESET register
0x50060004	CLK_PDCTRL_REG	Clock control settings for PD_CTRL

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Address	Register	Description
0x51001004	CLK_GPU_REG	Control register for clocks in PD_GPU

Table 292: CLK_SNC_REG (0x50020904)

Bit	Mode	Symbol	Description	Reset
17	R/W	I3C_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
16	R/W	I3C_ENABLE	Enables the clock	0x0
15	R/W	I2C3_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
14	R/W	I2C3_ENABLE	Enables the clock	0x0
13	R/W	I2C2_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
12	R/W	I2C2_ENABLE	Enables the clock	0x0
11	R/W	I2C_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
10	R/W	I2C_ENABLE	Enables the clock	0x0
9	R/W	SPI2_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
8	R/W	SPI2_ENABLE	Enables the clock	0x0
7	R/W	SPI_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
6	R/W	SPI_ENABLE	Enables the clock	0x0
5	R/W	UART3_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
4	R/W	UART3_ENABLE	Enables the clock	0x0
3	R/W	UART2_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
2	R/W	UART2_ENABLE	Enables the clock	0x0
1	R/W	UART_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
0	R/W	UART_ENABLE	Enables the clock	0x0

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Table 293: SET_CLK_SNC_REG (0x50020908)

Bit	Mode	Symbol	Description	Reset
17	RWS	I3C_CLK_SEL	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
16	RWS	I3C_ENABLE	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
15	RWS	I2C3_CLK_SEL	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
14	RWS	I2C3_ENABLE	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
13	RWS	I2C2_CLK_SEL	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
12	RWS	I2C2_ENABLE	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
11	RWS	I2C_CLK_SEL	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
10	RWS	I2C_ENABLE	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
9	RWS	SPI2_CLK_SEL	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
8	RWS	SPI2_ENABLE	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
7	RWS	SPI_CLK_SEL	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
6	RWS	SPI_ENABLE	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
5	RWS	UART3_CLK_SEL	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
4	RWS	UART3_ENABLE	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
3	RWS	UART2_CLK_SEL	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
2	RWS	UART2_ENABLE	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
1	RWS	UART_CLK_SEL	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0
0	RWS	UART_ENABLE	When writing a 1, the respective bit will be set. Writing a 0 is discarded.	0x0

Table 294: RESET_CLK_SNC_REG (0x5002090C)

Bit	Mode	Symbol	Description	Reset
17	RW1C	I3C_CLK_SEL	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
16	RW1C	I3C_ENABLE	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
15	RW1C	I2C3_CLK_SEL	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0

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Bit	Mode	Symbol	Description	Reset
14	RW1C	I2C3_ENABLE	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
13	RW1C	I2C2_CLK_SEL	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
12	RW1C	I2C2_ENABLE	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
11	RW1C	I2C_CLK_SEL	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
10	RW1C	I2C_ENABLE	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
9	RW1C	SPI2_CLK_SEL	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
8	RW1C	SPI2_ENABLE	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
7	RW1C	SPI_CLK_SEL	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
6	RW1C	SPI_ENABLE	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
5	RW1C	UART3_CLK_SEL	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
4	RW1C	UART3_ENABLE	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
3	RW1C	UART2_CLK_SEL	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
2	RW1C	UART2_ENABLE	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
1	RW1C	UART_CLK_SEL	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0
0	RW1C	UART_ENABLE	When writing a 1, the respective bit will be reset. Writing a 0 is discarded.	0x0

Table 295: CLK_SYS_REG (0x50040400)

Bit	Mode	Symbol	Description	Reset
7	R/W	SPI3_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
6	R/W	SPI3_ENABLE	Enables the clock	0x0
5	R/W	CLK_CHG_EN	Enables the clocks for the charger FSM block	0x0
4	R/W	LCD_RESET_REQ	Generates a SW reset towards the LCD controller.	0x0
3	R/W	-	Reserved	0x0
2	R/W	-	Reserved	0x0
1	R/W	LCD_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0

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Bit	Mode	Symbol	Description	Reset
0	R/W	LCD_ENABLE	Enables the clock	0x0

Table 296: SET_CLK_SYS_REG (0x50040408)

Bit	Mode	Symbol	Description	Reset
7	R/W	SPI3_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
6	R/W	SPI3_ENABLE	Enables the clock	0x0
5	R/W	CLK_CHG_EN	Enables the clocks for the charger FSM block	0x0
4	R/W	LCD_RESET_REQ	Generates a SW reset towards the LCD controller.	0x0
3	R/W	-	Reserved	0x0
2	R/W	-	Reserved	0x0
1	R/W	LCD_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
0	R/W	LCD_ENABLE	Enables the clock	0x0

Table 297: RESET_CLK_SYS_REG (0x5004040C)

Bit	Mode	Symbol	Description	Reset
7	R/W	SPI3_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
6	R/W	SPI3_ENABLE	Enables the clock	0x0
5	R/W	CLK_CHG_EN	Enables the clocks for the charger FSM block	0x0
4	R/W	LCD_RESET_REQ	Generates a SW reset towards the LCD controller.	0x0
3	R/W	-	Reserved	0x0
2	R/W	-	Reserved	0x0
1	R/W	LCD_CLK_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
0	R/W	LCD_ENABLE	Enables the clock	0x0

Table 298: BATCHECK_REG (0x50040410)

Bit	Mode	Symbol	Description	Reset
7	R/W	BATCHECK_LOAD_ENABLE	Enable a current load on the battery.	0x0
6:4	R/W	BATCHECK_ILOAD	Set the current load to (ILOAD+1) mA.	0x0

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Bit	Mode	Symbol	Description	Reset
3:0	R/W	BATCHECK_TRIM	Trim the current load with steps of 2.7 % from -19.1 % to +19.1 %. 0: +0.0 % , 8: -0 % 1: +2.7 % , 9: -2.7 % 2: +5.5 % , 10: -5.5 % 3: +8.2 % , 11: -8.2 % 4: +10.9 % , 12: -10.9 % 5: +13.6 % , 13: -13.6 % 6: +16.4 % , 14: -16.4 % 7: +19.1 % , 15: -19.1 %	0x0

Table 299: XTAL32M_START_REG (0x50050400)

Bit	Mode	Symbol	Description	Reset
28:22	R/W	XTAL32M_TIMEOUT	Timeout 0: disabled 1: 4 µs 2: 8 µs 63: 252 µs 64: 268 µs ... 127: 1260 µs	0x0
21:19	R/W	XTAL32M_CMP_BLANK	Blanking time for comparator output 0: disabled 1: 4 µs 2: 8 µs 3: 16 µs 4: 32 µs 5: 64 µs	0x3
18:17	R/W	XTAL32M_CMP_LVL	Comparator triplevel 0: 30 % 1: 35 % 2: 45 % 3: 60 %	0x2
16:14	R/W	XTAL32M_AMPL_SET	Amplitude Regulator input level setting (peak-peak) in START phase of startup 0: 300 mV 1: 350 mV .. 7: 900 mV	0x0
13:10	R/W	XTAL32M_CUR_SET	Current setting (units of 16 µA) in START phase of startup 0: OFF 1: 1x 2: 2x 3: 3x	0xC

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Bit	Mode	Symbol	Description	Reset
			4: 4x 5: 6x 6: 8x 7: 12x 8: 16x 9: 24x 10: 32x 11: 48x 12: 64x 13: 96x 14: 128x 15: 192x	
9:0	R/W	XTAL32M_TRIM	Capacitance bank seting in START phase of startup. 0x2BF: lowest oscillation frequency (highest load capacitance) 0x0: highest oscillation frequency (lowest load capacitance) When XTAL32M_TRIM_REG.XTAL32M_TRIM is smaller than XTAL32M_START_REG.XTAL32M_TRIM, the value from the XTAL32M_TRIM_REG.XTAL32M_TRIM will be used. CL = 3.68pF + 10.8fF/LSB.	0x12C

Table 300: XTAL32M_SETTLE_REG (0x50050404)

Bit	Mode	Symbol	Description	Reset
28:22	R/W	XTAL32M_TIMEOUT	Timeout 0: disabled 1: 4 µs 2: 8 µs 63: 252 µs 64: 268 µs ... 127: 1260 µs	0x0
21:19	R/W	XTAL32M_CMP_BLANK	Blanking time for comparator output 0: disabled 1: 4 µs 2: 8 µs 3: 16 µs 4: 32 µs 5: 64 µs	0x3
18:17	R/W	XTAL32M_CMP_LVL	Comparator triplevel 0: 30 % 1: 35 % 2: 45 %	0x1

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Bit	Mode	Symbol	Description	Reset
			3: 60 %	
16:14	R/W	XTAL32M_AMPL_SET	Amplitude Regulator input level setting (peak-peak) in SETTLE phase of startup 0: 300 mV 1: 350 mV .. 7: 900 mV	0x0
13:10	R/W	XTAL32M_CUR_SET	Current setting (units of 16 µA) in SETTLE phase of startup 0: OFF 1: 1x 2: 2x 3: 3x 4: 4x 5: 6x 6: 8x 7: 12x 8: 16x 9: 24x 10: 32x 11: 48x 12: 64x 13: 96x 14: 128x 15: 192x	0xC
9:0	R/W	XTAL32M_TRIM	Capacitance bank seting in SETLLE phase of startup 0x2BF: lowest oscillation frequency (highest load capacitance) 0x0: highest oscillation frequency (lowest load capacitance) CL = 3.68pF + 10.8fF/LSB	0x12C

Table 301: XTAL32M_TRIM_REG (0x50050408)

Bit	Mode	Symbol	Description	Reset
24:19	R/W	XTAL32M_BOOST_TRIM	Boost trimming, set accordingly to shunt capacitance. Sensitivity: 125 fF/LSB 0x0: Boost Disabled 1: 250 fF 2: 375 fF 3: 500 fF; 4: 625 fF; 62: 7.875 pF 63: 8 pF	0x0
18:17	R/W	XTAL32M_CMP_LVL	Comparator triplevel 0: 30 %	0x1

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Bit	Mode	Symbol	Description	Reset
			1: 35 % 2: 45 % 3: 60 %	
16:14	R/W	XTAL32M_AMPL_SET	Amplitude Regulator input level setting (peak-peak) in running phase 0: 300 mV 1: 350 mV .. 7: 900 mV	0x0
13:10	R/W	XTAL32M_CUR_SET	Current setting (units of 16 µA) in running phase 0: OFF 1: 1x 2: 2x 3: 3x 4: 4x 5: 6x 6: 8x 7: 12x 8: 16x 9: 24x 10: 32x 11: 48x 12: 64x 13: 96x 14: 128x 15: 192x	0x7
9:0	R/W	XTAL32M_TRIM	Capacitance bank seting in running phase, use to trim the xtal32m output frequency 0x2BF: lowest oscillation frequency (highest load capacitance) 0x0: highest oscillation frequency (lowest load capacitance) CL = 3.68 pF + 10.8 fF/LSB	0x12C

Table 302: XTAL32M_CAP_MEAS_REG (0x5005040C)

Bit	Mode	Symbol	Description	Reset
8:6	R/W	XTAL32M_MEAS_TIME	Select measurement time (in DIVN clock-cycles) 0: 32 1: 64 6: 2048 7: 4096	0x2
5	R/W	XTAL32M_MEAS_START	Starts capacitance measurement	0x0
4:3	R/W	XTAL32M_MEAS_CUR	Select measurement current (minimum required capacitance) 0: 100 nA (0.44 pF)	0x2

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Bit	Mode	Symbol	Description	Reset
			1: 500 nA (2.22 pF) 2: 1 µA (4.44 pF) 3: 5 µA (22.2 pF)	
2:0	R/W	XTAL32M_CAP_SELECT	Select measured capacitance 0: disabled 1: hold capacitance 2: xtal_p 3: xtal_n 4: xtal_p + xtal_n 5: low reference on xtal_p 6: low reference on xtal_p	0x0

Table 303: XTAL32M_FSM_REG (0x50050410)

Bit	Mode	Symbol	Description	Reset
5	R/W	XTAL32M_BOOST_MODE	Boost mode configuration 0: Only allow BOOST mode in START state 1: Allow BOOST mode in SETTLE and START state	0x0
4	R/W	XTAL32M_FSM_APPLY_CONFIG	CUR_SET, AMPL_SET, CMP_LVL and TRIM from XTAL32M_TRIM_REG are 0: applied at next startup 1: immediately applied	0x0
3	R/W	XTAL32M_FSM_FORCE_IDLE	Forces FSM in IDLE state, allows for software control	0x0
2	R/W	XTAL32M_CMP_MODE	Use the following comparator trim settings in SETTLE state: 0: XTAL32M_TRIM_REG.CMP_LVL 1: XTAL32M_SETTLE_REG.CMP_LVL	0x0
1	R/W	XTAL32M_TRIM_MODE	Use the following trim settings in the SETTLE state: 0: XTAL32M_TRIM_REG.TRIM 1: XTAL32M_SETTLE_REG.TRIM	0x0
0	R/W	XTAL32M_CUR_MODE	Use the following current setting in the SETTLE state: 0: XTAL32M_START_REG.CUR_SET 1: XTAL32M_SETTLE_REG.CUR_SET	0x0

Table 304: XTAL32M_CTRL_REG (0x50050414)

Bit	Mode	Symbol	Description	Reset
11:9	R/W	XTAL32M_DRIVE_CYCLES	Number of drive clock-cycles 0x0: Drive disabled 0x1: 4 0x2: 8 0x3: 16	0x2

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Bit	Mode	Symbol	Description	Reset
			0x4: 32 0x5: 64 0x6:128 0x7:256	
8	R/W	XTAL32M_ENABLE	Enables xtal32m (testing purposes)	0x0
7:6	R/W	XTAL32M_BIASPROT	Bias startup circuit 0: enable during startup 1: always enabled 2: always disabled	0x0
5:4	R/W	XTAL32M_LDO_SAH	Controls amplitude regulator sample-and-hold 2'b00: set to HOLD when IRQ fires 2'b01: always TRACK 2'b1x: always HOLD	0x1
3:2	R/W	XTAL32M_AMPREG_SAH	Controls amplitude regulator sample-and-hold 2'b00: set to HOLD when IRQ fires 2'b01: always TRACK 2'b1x: always HOLD	0x1
1:0	R/W	XTAL32M_BIAS_SAH	Controls bias sample-and-hold 2'b00: set to HOLD when IRQ fires 2'b01: always TRACK 2'b1x: always HOLD	0x1

Table 305: XTAL32M_IRQ_CTRL_REG (0x50050418)

Bit	Mode	Symbol	Description	Reset
11:10	R/W	XTAL32M_IRQ_CAP_CTRL	The IRQ counter is captured in the XTAL32M_IRQ_STATUS_REG.IRQ_COUNT_CAP when reaching the following state 0: START 1: SETTLE 2: RUN	0x2
9	R/W	XTAL32M_IRQ_ENABLE	Enable xtal interrupt generation.	0x0
8	R/W	XTAL32M_IRQ_CLK	Clock divider for IRQ counter 0: 4 µs 1: 32 µs	0x0
7:0	R/W	XTAL32M_IRQ_CNT	IRQ counter start value.	0xFF

Table 306: XTAL32M_STAT0_REG (0x50050424)

Bit	Mode	Symbol	Description	Reset
29	R	XTAL32M_OVERLOAD	Indicates xtal is overloaded	0x0

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Bit	Mode	Symbol	Description	Reset
28:27	R	XTAL32M_CMP_LVL_STAT	Current value for amplitude regulator comparator setting	0x0
26:24	R	XTAL32M_AMPL_TRIM	Current value for amplitude trim	0x0
23:14	R	XTAL32M_TRIM_VAL	Current value for oscillator trimming	0x3FF
13:10	R	XTAL32M_CUR_SET_STAT	Current value for cur_set	0x0
9	R	XTAL32M_LDO_OK	Indicates LDO voltage level is ok	0x0
8:7	R	XTAL32M_CMP_OUT	Amplitude regulator comparator output state	0x0
6:3	R	XTAL32M_STATE	State of xtal startup FSM 0x0: IDLE 0x1: WAIT_LDO 0x2: WAIT_BIAS 0x3: XTAL_DRIVE 0x4: START_BLANK 0x5: START 0x6: SETTLE_BLANK 0x7: SETTLE 0x8: RUN 0x9: CAP_TEST_IDLE 0xA: CAP_TEST_MEAS 0xB: CAP_TEST_END	0x0
2:1	R	XTAL32M_CMP_OUT_HOLD	Captured state of amplitude regulator comparators at IRQ fire.	0x0
0	R	XTAL32M_READY	Indicates xtal startup FSM has reached the RUNNIG state and is ready for use (sysclk)	0x0

Table 307: XTAL32M_IRQ_STAT_REG (0x50050428)

Bit	Mode	Symbol	Description	Reset
15:8	R	XTAL32M_IRQ_COUNT_CAP	Captured IRQ counter	0x0
7:0	R	XTAL32M_IRQ_COUNT_STAT	Current IRQ counter value	0x0

Table 308: PLL_SYS_CTRL1_REG (0x50050460)

Bit	Mode	Symbol	Description	Reset
15	R/W	PLL_OUT_DIV	0: Output divider ON 1: Output divider OFF	0x1
14	R/W	PLL_SEL_MIN_CUR_INT	0: VCO current read from min_current <5:0>, 1: VCO current is internally determined with a calibration algoritm.	0x1
13:12	R/W	-	Reserved	0x2

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Bit	Mode	Symbol	Description	Reset
11	R/W	PLL_PRE_DIV	PLL input divider (1: Indicates divide by 2).	0x1
10:4	R/W	PLL_N_DIV	PLL loop divider N (x means divide by x, 0 means divide by 1)	0xA
3	R/W	LDO_PLL_VREF_HOLD	0: Indicates that the reference input is tracked, 1: Indicates that the reference input is sampled.	0x0
2	R/W	LDO_PLL_ENABLE	0: LDO PLL off, 1: LDO PLL on.	0x0
1	R/W	PLL_RST_N	0: PLL in Reset 1L PLL out of Reset	0x0
0	R/W	PLL_EN	0: Power down 1: PLL on	0x0

Table 309: PLL_SYS_CTRL2_REG (0x50050464)

Bit	Mode	Symbol	Description	Reset
15	R/W	PLL_RECALIB	Recalibrate	0x0
14:10	R/W	-	Reserved	0x9
9:8	R/W	-	Reserved	0x0
7	R/W	-	Reserved	0x1
6	R/W	-	Reserved	0x0
5	R/W	-	Reserved	0x0
4:0	R/W	-	Reserved	0x0

Table 310: PLL_SYS_CTRL3_REG (0x50050468)

Bit	Mode	Symbol	Description	Reset
15:13	R/W	-	Reserved	0x4
12:11	R/W	-	Reserved	0x2
10	R/W	-	Reserved	0x0
9	R/W	-	Reserved	0x0
8	R/W	-	Reserved	0x0
7	R/W	-	Reserved	0x0
6:1	R/W	PLL_MIN_CURRENT	VCO current trimming.	0x38
0	R/W	-	Reserved	0x0

Table 311: PLL_SYS_STATUS_REG (0x50050470)

Bit	Mode	Symbol	Description	Reset
15	R	LDO_PLL_OK	1: Indicates that LDO PLL is in regulation.	0x0
14:12	R	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
11	R	PLL_CALIBRATION_END	Indicates that calibration has finished.	0x0
10:5	R	PLL_BEST_MIN_CUR	Calibrated VCO current.	0x0
4:1	R	-	Reserved	0x0
0	R	PLL_LOCK_FINE	1: PLL locked	0x0

Table 312: PLL_USB_CTRL1_REG (0x50050474)

Bit	Mode	Symbol	Description	Reset
15	R/W	PLL_OUT_DIV	0: Output divider ON 1: Output divider OFF	0x0
14	R/W	PLL_SEL_MIN_CUR_INT	0: VCO current read from min_current <5:0>, 1: VCO current is internally determined with a calibration algoritm.	0x1
13:12	R/W	-	Reserved	0x2
11	R/W	PLL_PRE_DIV	PLL input divider (1: Indicates divide by 2).	0x1
10:4	R/W	PLL_N_DIV	PLL loop divider N (x means divide by x, 0 means divide by 1)	0x9
3	R/W	LDO_PLL_VREF_HOLD	0: Indicates that the reference input is tracked, 1: Indicates that the reference input is sampled.	0x0
2	R/W	LDO_PLL_ENABLE	0: LDO PLL off, 1: LDO PLL on.	0x0
1	R/W	PLL_RST_N	0: PLL in Reset 1L PLL out of Reset	0x0
0	R/W	PLL_EN	0: Power down 1: PLL on	0x0

Table 313: PLL_USB_CTRL2_REG (0x50050478)

Bit	Mode	Symbol	Description	Reset
31:16	R	-	Reserved	0x0
15	R/W	PLL_RECALIB	Recalibrate	0x0
14:10	R/W	-	Reserved	0x9
9:8	R/W	-	Reserved	0x0
7	R/W	-	Reserved	0x1
6	R/W	-	Reserved	0x0
5	R/W	-	Reserved	0x0
4:0	R/W	-	Reserved	0x0

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Table 314: PLL_USB_CTRL3_REG (0x5005047C)

Bit	Mode	Symbol	Description	Reset
15:13	R/W	-	Reserved	0x4
12:11	R/W	-	Reserved	0x2
10	R/W	-	Reserved	0x0
9	R/W	-	Reserved	0x0
8	R/W	-	Reserved	0x0
7	R/W	-	Reserved	0x0
6:1	R/W	PLL_MIN_CURRENT	VCO current trimming.	0x38
0	R/W	-	Reserved	0x0

Table 315: PLL_USB_STATUS_REG (0x50050480)

Bit	Mode	Symbol	Description	Reset
15	R	LDO_PLL_OK	1: Indicates that LDO PLL is in regulation.	0x0
14:12	R	-	Reserved	0x0
11	R	PLL_CALIBRATION_END	Indicates that calibration has finished.	0x0
10:5	R	PLL_BEST_MIN_CUR	Calibrated VCO current.	0x0
4:1	R	-	Reserved	0x0
0	R	PLL_LOCK_FINE	1: PLL locked	0x0

Table 316: SYS_IRQ_CTRL_REG (0x50050490)

Bit	Mode	Symbol	Description	Reset
5	R/W	CMAC2SNC_IRQ_BIT	Direct read/write to the specific IRQ bit	0x0
4	R/W	CMAC2SYS_IRQ_BIT	Direct read/write to the specific IRQ bit	0x0
3	R/W	SNC2SYS_IRQ_BIT	Direct read/write to the specific IRQ bit	0x0
2	R/W	SNC2CMAC_IRQ_BIT	Direct read/write to the specific IRQ bit	0x0
1	R/W	SYS2SNC_IRQ_BIT	Direct read/write to the specific IRQ bit	0x0
0	R/W	SYS2CMAC_IRQ_BIT	Direct read/write to the specific IRQ bit	0x0

Table 317: SET_SYS_IRQ_CTRL_REG (0x50050494)

Bit	Mode	Symbol	Description	Reset
5	R/W	CMAC2SNC_IRQ_BIT	When writing a 1, the respective IRQ line will be set. Writing a 0 is discarded.	0x0

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Bit	Mode	Symbol	Description	Reset
4	R/W	CMAC2SYS_IRQ_BIT	When writing a 1, the respective IRQ line will be set. Writing a 0 is discarded.	0x0
3	R/W	SNC2SYS_IRQ_BIT	When writing a 1, the respective IRQ line will be set. Writing a 0 is discarded.	0x0
2	R/W	SNC2CMAC_IRQ_BIT	When writing a 1, the respective IRQ line will be set. Writing a 0 is discarded.	0x0
1	R/W	SYS2SNC_IRQ_BIT	When writing a 1, the respective IRQ line will be set. Writing a 0 is discarded.	0x0
0	R/W	SYS2CMAC_IRQ_BIT	When writing a 1, the respective IRQ line will be set. Writing a 0 is discarded.	0x0

Table 318: RESET_SYS_IRQ_CTRL_REG (0x50050498)

Bit	Mode	Symbol	Description	Reset
5	R/W	CMAC2SNC_IRQ_BIT	When writing a 1, the respective IRQ line will be reset. Writing a 0 is discarded.	0x0
4	R/W	CMAC2SYS_IRQ_BIT	When writing a 1, the respective IRQ line will be reset. Writing a 0 is discarded.	0x0
3	R/W	SNC2SYS_IRQ_BIT	When writing a 1, the respective IRQ line will be reset. Writing a 0 is discarded.	0x0
2	R/W	SNC2CMAC_IRQ_BIT	When writing a 1, the respective IRQ line will be reset. Writing a 0 is discarded.	0x0
1	R/W	SYS2SNC_IRQ_BIT	When writing a 1, the respective IRQ line will be reset. Writing a 0 is discarded.	0x0
0	R/W	SYS2CMAC_IRQ_BIT	When writing a 1, the respective IRQ line will be reset. Writing a 0 is discarded.	0x0

Table 319: CLK_PDCTRL_REG (0x50060004)

Bit	Mode	Symbol	Description	Reset
13	R/W	EMMC_INV_TX_CLK	Inverts the clock in the TX path	0x0
12	R/W	EMMC_INV_RX_CLK	Invert the clock in the RX path, cascaded with INV_TX_CLK	0x0
11	R/W	EMMC_ENABLE	Enables the clock.	0x0
10:7	R/W	EMMC_CLK_DIV	clock divider setting 0x0 : divide by 16 0x1 : divide by 1 0x2 : divide by 2 0x4 : divide by 4 0x8 : divide by 8	0x0
6	R/W	-	Reserved	0x0
5	R/W	-	Reserved	0x0
4	R/W	-	Reserved	0x0
3:0	R/W	-	Reserved	0x0

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Table 320: CLK_GPU_REG (0x51001004)

Bit	Mode	Symbol	Description	Reset
3	R/W	-	Reserved	0x0
2	R/W	-	Reserved	0x0
1	R/W	-	Reserved	0x0
0	R/W	GPU_ENABLE		0x0

Table 321: Register map CRG_AUD

Address	Register	Description
0x50030040	PCM_DIV_REG	PCM divider and enables
0x50030044	PCM_FDIV_REG	PCM fractional division register
0x50030048	PDM_DIV_REG	PDM divider and enables
0x5003004C	SRC_DIV_REG	SRC divider and enables

Table 322: PCM_DIV_REG (0x50030040)

Bit	Mode	Symbol	Description	Reset
13	R/W	PCM_SRC_SEL	Selects the clock source 1 = DIV1 clock 0 = DIVN clock	0x0
12	R/W	CLK_PCM_EN	Enable for the internally generated PCM clock The PCM_DIV must be set before or together with CLK_PCM_EN.	0x0
11:0	R/W	PCM_DIV	PCM clock divider. Minimum value is 0x2.	0x0

Table 323: PCM_FDIV_REG (0x50030044)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	PCM_FDIV	These bits define the fractional division part of the PCM clock. The left most 1 defines the denominator, the number of 1 bits define the numerator. For example, 0x0110 means 2/9, with a distribution of 1.0001.0000 0xfeee means 13/16, with a distribution of 1111.1110.1110.1110	0x0

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Table 324: PDM_DIV_REG (0x50030048)

Bit	Mode	Symbol	Description	Reset
9	R/W	PDM_MASTER_MODE	Master mode selection 0: slave mode 1: master mode	0x0
8	R/W	CLK_PDM_EN	Enable for the internally generated PDM clock The PDM_DIV must be set before or together with CLK_PDM_EN.	0x0
7:0	R/W	PDM_DIV	PDM clock divider	0x0

Table 325: SRC_DIV_REG (0x5003004C)

Bit	Mode	Symbol	Description	Reset
17	R/W	CLK_SRC2_EN	Enable for the internally generated SRC2 clock The SRC2_DIV must be set before or together with CLK_SRC2_EN.	0x0
16	R/W	CLK_SRC_EN	Enable for the internally generated SRC clock The SRC_DIV must be set before or together with CLK_SRC_EN.	0x0
15:8	R/W	SRC2_DIV	SRC2 clock divider	0x0
7:0	R/W	SRC_DIV	SRC clock divider	0x0

Table 326: Register map CRG_TOP

Address	Register	Description
0x50000000	CLK_AMBA_REG	HCLK, PCLK, divider and clock gates
0x50000004	CLK_CMAC_SWITCH_REG	Clock switching register for CMAC clock domain
0x5000000C	RST_CTRL_REG	Reset control register
0x50000010	CLK_RADIO_REG	Radio PLL control register
0x50000014	CLK_CTRL_REG	Clock control register
0x50000018	CLK_TMR_REG	Clock control for the timers
0x5000001C	CLK_SWITCH2XTAL_REG	Switches clock from RC32M to XTAL32M
0x50000020	PMU_CTRL_REG	Power Management Unit control register
0x50000024	SYS_CTRL_REG	System Control register
0x50000028	SYS_STAT_REG	System status register
0x5000002C	CLK_SNC_CTRL_REG	
0x50000030	SLP_MAP_REG	Map signals on GPIOs during sleep
0x50000034	LCD_EXT_CTRL_REG	
0x5000003C	CLK_RCLP_REG	32/512 kHz RC oscillator register
0x50000040	CLK_XTAL32K_REG	32 kHz XTAL oscillator register

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Address	Register	Description
0x50000044	CLK_RCHS_REG	Fast RC control register
0x50000048	CLK_RCX_REG	RCX-oscillator control register
0x5000004C	CLK_RTCDIV_REG	Divisor for RTC 100Hz clock
0x50000050	BANDGAP_REG	bandgap trimming
0x50000054	VBUS_IRQ_MASK_REG	IRQ masking
0x50000058	VBUS_IRQ_CLEAR_REG	Clear pending IRQ register
0x50000060	BOD_CTRL_REG	Brown Out Detection control register
0x50000064	BOD_STATUS_REG	
0x50000070	P0_PAD_LATCH_REG	Control the state retention of the GPIO ports
0x50000074	P0_SET_PAD_LATCH_REG	Control the state retention of the GPIO ports
0x50000078	P0_RESET_PAD_LATCH_REG	Control the state retention of the GPIO ports
0x5000007C	P1_PAD_LATCH_REG	Control the state retention of the GPIO ports
0x50000080	P1_SET_PAD_LATCH_REG	Control the state retention of the GPIO ports
0x50000084	P1_RESET_PAD_LATCH_REG	Control the state retention of the GPIO ports
0x50000088	P2_PAD_LATCH_REG	Control the state retention of the GPIO ports
0x5000008C	P2_SET_PAD_LATCH_REG	Control the state retention of the GPIO ports
0x50000090	P2_RESET_PAD_LATCH_REG	Control the state retention of the GPIO ports
0x50000094	POR_CTRL_REG	Controls the POR on VBAT
0x50000098	POR_PIN_REG	Selects a GPIO pin for POR generation
0x5000009C	POR_TIMER_REG	Time for POR to happen
0x500000BC	RESET_STAT_REG	Reset status register
0x500000C0	RAM_PWR_CTRL_REG	Control power state of System RAMS
0x500000CC	SECURE_BOOT_REG	Controls secure booting
0x500000D4	DISCHARGE_RAIL_REG	Immediate rail resetting. There is no LDO/DCDC gating
0x500000E0	WAKEUP_HIBERN_REG	
0x500000E4	SW_V18F_REG	
0x500000E8	BIAS_VREF_SEL_REG	
0x500000EC	ANA_STATUS_REG	Analog Signals Status Register
0x500000F0	POWER_CTRL_REG	Power control register
0x500000F4	PMU_SLEEP_REG	Configures the sleep/wakeup strategy

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Address	Register	Description
0x500000F8	POWER_LVL_REG	

Table 327: CLK_AMBA_REG (0x50000000)

Bit	Mode	Symbol	Description	Reset
20	R/W	OQSPI_PULLUP_ENABLE	Selects pull value when OQSPIF_D* pads are not output. 0: The pads are pull-down 1: The pads are pull-up (to V18F)	0x0
19	R/W	OQSPI_GPIO_MODE	If this bit is set, the upper 4 pins of the OQSPIF controller can be used as GPIO, P2_07 to P2_04. In this mode, the OQSPIF controller should be restricted to QUAD mode or less. Note: the supply remains V18F, so if the supply is off, the pads become floating.	0x0
18	R/W	QSPIC2_ENABLE	Clock enable for QSPI RAM controller	0x0
17:16	R/W	QSPIC2_DIV	Clock divider setting. 0b00: divide by 1 0b01: divide by 2 0b10: divide by 4 0b11: divide by 8	0x0
15	R/W	QSPIC_ENABLE	Clock enable for QSPI FLASH2 controller	0x0
14:13	R/W	QSPIC_DIV	Clock divider setting. 0b00: divide by 1 0b01: divide by 2 0b10: divide by 4 0b11: divide by 8	0x0
12	R/W	OQSPIF_ENABLE	Clock enable for Octal SPI controller	0x0
11:10	R/W	OQSPIF_DIV	Clock divider setting. 0b00: divide by 1 0b01: divide by 2 0b10: divide by 4 0b11: divide by 8	0x0
9	R/W	OTP_ENABLE	Clock enable for OTP controller	0x0
8	R/W	AES_CLK_ENABLE	Clock enable for AES crypto block	0x0
7:5	R/W	SLOW_PCLK_DIV	Slow-APB interface clock, derived from DIVN_CLK: 0b000: divide divn_clk by 1 0b001: divide divn_clk by 2 0b010: divide divn_clk by 4 0b011: divide divn_clk by 8 0b1xx: divide divn_clk by 16	0x2
4:3	R/W	PCLK_DIV	Fast-APB interface clock, Cascaded with HCLK: 0b00: divide hclk by 1 0b01: divide hclk by 2 0b10: divide hclk by 4	0x2

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Bit	Mode	Symbol	Description	Reset
			0b11: divide hclk by 8	
2:0	R/W	HCLK_DIV	AHB interface and microprocessor clock. Source clock divided by: 0b000: divide clk by 1 0b001: divide clk by 2 0b010: divide clk by 4 0b011: divide clk by 8 0b1xx: divide clk by 16	0x2

Table 328: CLK_CMAC_SWITCH_REG (0x50000004)

Bit	Mode	Symbol	Description	Reset
2	R	CMAC_RUNNING_ON_XTAL	This bit is 1 when the CMAC_CLK is enabled, and the switch is set in the XTAL32M position.	0x0
1	R	CMAC_RUNNING_ON_DIVN	This bit is 1 when the CMAC_CLK is enabled, and the switch is set in the DIVN_CLK position.	0x0
0	R/W	CMAC_CLK_SEL	Selects the clock source of the CMAC_CLK. 0: DIVN_CLK is selected 1: XTAL32M is selected. Note: this bitfield can only be set to 1 when the PD_RAD domain is on (RAD_IS_UP), and will be automatically reset to 0 when the PD_RAD power domain turns off.	0x0

Table 329: RST_CTRL_REG (0x5000000C)

Bit	Mode	Symbol	Description	Reset
0	R/W	SYS_CACHE_FLUSH_WITH_SW_RESET	0: Flush the System Cache memory only at HW reset. 1: Flush the System Cache memory also at SW reset.	0x0

Table 330: CLK_RADIO_REG (0x50000010)

Bit	Mode	Symbol	Description	Reset
6	R/W	RAD_REG_RESET_REQ	Reset request for registers of the radio PHY.	0x0
5	R/W	RFCU_ENABLE	Enable the RF control Unit clock	0x0
4	R/W	CMAC_SYNCH_RESET	Force synchronous reset to CMAC core and Sleep Timer. Its effective only when both Radio and Timer Power Domains are powered and the clocks are enabled. CMAC CPU and CMAC registers, including the retained ones, will be reset. It should be kept in reset for enough time to make sure that it will be captured by CMAC, Low Power and APB clocks.	0x1

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Bit	Mode	Symbol	Description	Reset
3	R/W	-	Reserved	0x0
2	R/W	CMAC_CLK_ENABLE	Enables the clock	0x0
1:0	R/W	-	Reserved	0x0

Table 331: CLK_CTRL_REG (0x50000014)

Bit	Mode	Symbol	Description	Reset
15	R	RUNNING_AT_PLL	Indicates that the PLL clock is used as clock, and may not be switched off	0x0
14	R	RUNNING_AT_XTAL32M	Indicates that the XTAL32M clock is used as clock, and may not be switched off	0x0
13	R	RUNNING_AT_RCHS	Indicates that the RCHS clock is used as clock	0x1
12	R	RUNNING_AT_RCLP	Indicates that the RCLP_CLK is being used as clock	0x0
11:7	R	-	Reserved	0x0
6	R/W	VAD_CLK_SEL	Selects the clock for the VAD. 0: Select RCLP clock (normalized for ~32 kHz) 1: Select XTAL32K	0x0
5	R/W	-	Reserved	0x0
4	R/W	USB_CLK_SRC	Selects the USB source clock 0 : USB PLL 48 MHz clk 1 : DIVN clk, to be used in suspend mode	0x0
3:2	R/W	LP_CLK_SEL	Sets the clock source of the LowerPower clock 0x0: RCLP 0x1: RCX 0x2: XTAL32K through the oscillator with an external Crystal. 0x3: XTAL32K through an external square wave generator (set PID of GPIO to FUNC_GPIO)	0x0
1:0	R/W	SYS_CLK_SEL	Selects the clock source. 0x0 : XTAL32M 0x1 : RCHS 0x2 : RCLP 0x3 : The PLL 160 MHz is used Note: switching to/from PLL may only be done from/to XTAL32M.	0x1

Table 332: CLK_TMR_REG (0x50000018)

Bit	Mode	Symbol	Description	Reset
2	R/W	-	Reserved	0x0
1	R/W	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
0	R/W	WAKEUPCT_ENABLE	Enables the clock	0x0

Table 333: CLK_SWITCH2XTAL_REG (0x5000001C)

Bit	Mode	Symbol	Description	Reset
0	W	SWITCH2XTAL	When writing to this register, the clock switch will happen from RC32M to XTAL32M. If any other clock is selected than RC32M, the selection is discarded.	0x0

Table 334: PMU_CTRL_REG (0x50000020)

Bit	Mode	Symbol	Description	Reset
13	R/W	RETAIN_RGP_RAM	Retain the R-G-B RAMs inside the LCD display controller	0x0
12	R/W	RETAIN_GPU_CLUT	Retain the GPU CLUT memory	0x0
11	R/W	RETAIN_DCACHE	Selects the retainability of the dcache block while PD_CTRL is off. 1 is retainable, 0 is power gated	0x0
10	R/W	GPU_SLEEP	Put the GPU power domain (PD_GPU) in powerdown	0x1
9	R/W	CTRL_SLEEP	Put the Controller power domain (PD_CTRL) in powerdown	0x1
8	R/W	-	Reserved	0x0
7	R/W	RETAIN_CACHE	Selects the retainability of the cache block during deep sleep. 1 is retainable, 0 is power gated	0x0
6	R/W	SYS_SLEEP	Put the System powerdomain (PD_SYS) in powerdown. If this bit is 1, and there is no pending IRQ in the PDC for the M33, the PD_SYS will be switched off. Wakeup should be handled by the PDC.	0x0
5	R/W	RESET_ON_WAKE UP	Perform a Hardware Reset after waking up. Booter will be started.	0x0
4	R/W	-	Reserved	0x0
3	R/W	SNC_SLEEP	Put the Communications powerdomain (PD_SNC) in powerdown	0x1
2	R/W	TIM_SLEEP	Put the Timers Powerdomain (PD_TIM) in powerdown.	0x1
1	R/W	RADIO_SLEEP	Put the digital part of the radio, including CMAC (PD_RAD) in powerdown	0x1
0	R/W	AUD_SLEEP	Put the audio power domain (PD_AUD) in powerdown	0x1

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Table 335: SYS_CTRL_REG (0x50000024)

Bit	Mode	Symbol	Description	Reset
15	W	SW_RESET	Writing a 1 to this bit will generate a SW_RESET.	0x0
14:11	R	-	Reserved	0x0
10	R/W	CACHERAM_MUX	Controls accessiblity of Cache RAM (incl. enabling/disabling of the Cache Controller): 0: the cache controller is disabled/bypassed, the cacheRAM is visible in the memory space, 1: the cache controller is enabled, the cacheRAM is not visible anymore in the memory space. Note: When the cache controller is enabled after or at reset, the Cache is first initialized (cleared/flushed) by writing all 0s to each line, one line per clock cycle to all SRAM modules. When the cache controller is disabled/bypassed the cache memory is cleared/flushed in the same way as during the first after reset initialization.	0x0
9	R/W	TIMEOUT_DISABLE	Disables timeout in Power statemachine. By default, the statemachine continues if after 2 ms the blocks are not started up. This can be read back from ANA_STATUS_REG	0x0
8	R/W	-	Reserved	0x0
7	R/W	DEBUGGER_ENABLE	Enable the debugger. This bit is set by the booter according to the OTP header. If not set, the SWDIO and SW_CLK can be used as GPIO ports.	0x0
6	R/W	-	Reserved	0x0
5	R/W	SNC_DEBUGGER_ENABLE	Enable the SNC debugger. If not set, the SWDIO and SW_CLK can be used as gpio ports.	0x0
4	R/W	-	Reserved	0x0
3	R/W	REMAP_INTVECT	0: normal operation 1: If ARM is in address range 0 - 0x1FF then the address is remapped to SYS-RAM 0x0F00.0000 - 0x0F00.01FF (and only when remapped to OQSPI FLASH (REMAP_ADR0 is 2 or 4). This allows to put the interrupt vector table to be placed in RAM while executing from OQSPI (to improve ISR performance).	0x0
2:0	R/W	REMAP_ADR0	Controls which memory is located at address 0x0000 for execution. 0x0: ROM 0x1: OTP un-cached 0x2: OQSPI FLASH cached (see also the CACHE_FLASH_REG.FLASH_REGION.* descriptions) Note 1: When REMAP_ADR0=0x2, address 0x0 is mapped to FLASH_REGION_BASE + FLASH_REGION_OFFSET<<2.	0x0

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Bit	Mode	Symbol	Description	Reset
			Note 2: When REMAP_ADR0=0x2, the CPU can only access the Flash region [FLASH_REGION_BASE + FLASH_REGION_OFFSET<<2, FLASH_REGION_SIZE] from the 0x18000000 address range. The complete Flash can be accessed via the 0x38000000 address range but only uncached. 0x3: RAMS un-cached 0x4: OQSPI FLASH un-cached (for verification only) 0x5: SYSRAM3 (for SNC-based applications, where SNC uses SYSRAM 1&2) 0x6: Cache Data RAM un-cached (CACHERAM_MUX=0, for testing purposes only) Note 3: DWord (64 bits) access is not supported by the Cache Data RAM interface in mirrored mode (only 32, 16 and 8 bits). Note 4: DMA access is not supported by the Cache Data RAM interface when REMAP_ADR0=0x6.	

Table 336: SYS_STAT_REG (0x50000028)

Bit	Mode	Symbol	Description	Reset
17	R	GPU_IS_UP	Indicates that PD_GPU is functional	0x0
16	R	GPU_IS_DOWN	Indicates that PD_GPU is in power down	0x1
15	R	CTRL_IS_UP	Indicates that PD_CTRL is functional	0x0
14	R	CTRL_IS_DOWN	Indicates that PD_CTRL is in power down	0x1
13	R	POWER_IS_UP	Indicates that the Startup statemachine is finished, and all power regulation is in order. In UltraFastWakeup mode, the SW needs to wait for this signal before starting any heavy traffic.	0x1
12	R	DBG_IS_ACTIVE	Indicates that a debugger is attached.	0x0
11	R	SNC_IS_UP	Indicates that PD_SNC is functional	0x0
10	R	SNC_IS_DOWN	Indicates that PD_SNC is in power down	0x1
9	R	TIM_IS_UP	Indicates that PD_TIM is functional	0x0
8	R	TIM_IS_DOWN	Indicates that PD_TIM is in power down	0x1
7	R	MEM_IS_UP	Indicates that PD_MEM is functional	0x1
6	R	MEM_IS_DOWN	Indicates that PD_MEM is in power down	0x0
5	R	SYS_IS_UP	Indicates that PD_SYS is functional	0x1
4	R	SYS_IS_DOWN	Indicates that PD_SYS is in power down	0x0
3	R	AUD_IS_UP	Indicates that PD_AUD is functional	0x0
2	R	AUD_IS_DOWN	Indicates that PD_AUD is in power down	0x1
1	R	RAD_IS_UP	Indicates that PD_RAD is functional	0x0
0	R	RAD_IS_DOWN	Indicates that PD_RAD is in power down	0x1

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Table 337: CLK_SNC_CTRL_REG (0x5000002C)

Bit	Mode	Symbol	Description	Reset
2	R/W	SNC_STATE_RETAINED	A flag which can be used from FW to indicate that the CPU state has been retained and should be restored during the wakeup sequence (at the beginning of Reset Handler). This flag is retained during the power-down periods.	0x0
1	R/W	SNC_CLK_ENABLE	Clock-enable for the CM0plus in the SNC.	0x0
0	R/W	SNC_RESET_REQ	Force the SNC microprocessor in reset.	0x1

Table 338: SLP_MAP_REG (0x50000030)

Bit	Mode	Symbol	Description	Reset
8	R/W	LCD_INV_EXT_CLK_SLP_MAP	Maps inverted LCD_EXT_CLK on P0_10, for LCD XFRP function This state is preserved during deep sleep, to allow pin output toggle on the pad during deep sleep.	0x0
7	R/W	LCD_EXT_CLK_SLP_MAP	Maps LCD_EXT_CLK on P0_19, for LCD VCOM/FRP/EXTCOMIN function This state is preserved during deep sleep, to allow pin output toggle on the pad during deep sleep.	0x0
6	R/W	BANDGAP_SLP_MAP	Setting this bit will: - map bandgap_enable to P0_20 - map (wokenup OR cmac_slp_timer_expire) to P1_04	0x0
5	R/W	RCLP_SLP_MAP	Maps RCLP onto P1_23. This state is preserved during deep sleep, to allow pin output toggle on the pad during deep sleep.	0x0
4	R/W	XTAL32K_SLP_MAP	Maps XTA32k onto P0_31. This state is preserved during deep sleep, to allow pin output toggle on the pad during deep sleep.	0x0
3	R/W	RCX_SLP_MAP	Maps RCX onto P1_22. This state is preserved during deep sleep, to allow pin output toggle on the pad during deep sleep.	0x0
2	R/W	TMR4_PWM_SLP_MAP	Maps Timer4_pwm onto P1_31 This state is preserved during deep sleep, to allow pin output toggle on the pad during deep sleep.	0x0
1	R/W	TMR3_PWM_SLP_MAP	Maps Timer3_pwm onto P1_30 This state is preserved during deep sleep, to allow pin output toggle on the pad during deep sleep.	0x0
0	R/W	TMR_PWM_SLP_MAP	Maps Timer1_pwm onto P0_30 This state is preserved during deep sleep, to allow pin output toggle on the pad during deep sleep.	0x0

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Table 339: LCD_EXT_CTRL_REG (0x50000034)

Bit	Mode	Symbol	Description	Reset
10	R/W	LCD_EXT_CLK_EN		0x0
9:0	R/W	LCD_EXT_CNT_RELOAD	Reload value for LCD_EXT_CLK generation. When the counter hits 0x0, it is reloaded with LCD_EXT_CNT_RELOAD<<5. So the clock period is F(slp_clk) * 32 * (LCD_EXT_CNT_RELOAD+1) Value 0x0 is not allowed. The LCD_EXT_CLK is generated from the SLP_CLK.	0x8

Table 340: CLK_RCLP_REG (0x5000003C)

Bit	Mode	Symbol	Description	Reset
5	R/W	RCLP_LOW_SPEED_FORCE	Forces RCLP in 32-kHz mode. If this bit is 0 then RCLP frequency is 512 kHz	0x0
4:1	R/W	RCLP_TRIM	0000 = lowest frequency 0111 = default 1111 = highest frequency	0x7
0	R/W	RCLP_ENABLE	Enables the 32-kHz RC oscillator. Do not disable this bit, as deep/extended sleep state is not correctly entered.	0x1

Table 341: CLK_XTAL32K_REG (0x50000040)

Bit	Mode	Symbol	Description	Reset
9	R/W	XTAL32K_DISABLE_OUTPUT	Disables output buffer, test only	0x0
8	R/W	-	Reserved	0x0
7	R/W	XTAL32K_DISABLE_AMPREG	Setting this bit disables the amplitude regulation of the XTAL32kHz oscillator. Set this bit to 1 for an external clock to XTAL32Kp Keep this bit 0 with a crystal between XTAL32Kp and XTAL32Km	0x0
6:3	R/W	XTAL32K_CUR	Bias current for the 32-kHz XTAL oscillator. 0000 is minimum, 1111 is maximum, 0011 is default. For each application there is an optimal setting for which the start-up behavior is optimal	0x5
2:1	R/W	XTAL32K_RBIAS	Setting for the bias resistor. 00 is maximum, 11 is minimum. Prefered setting will be provided by Renesas Electronics	0x3
0	R/W	XTAL32K_ENABLE	Enables the 32-kHz XTAL oscillator	0x0

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Table 342: CLK_RCHS_REG (0x50000044)

Bit	Mode	Symbol	Description	Reset
25	R/W	-	Reserved	0x0
24	R/W	-	Reserved	0x0
23:22	R/W	RCHS_SPEED	Selects speed of RCHS output 0b00: 32 MHz, by dividing 96 / 3. 0b01: 96 MHz, by dividing 96 /1. 0b1x: 64 MHz. Note: switching to/from 64 MHz requires the RCHS to settle, which can be > 100 µs. Switching 32 to/from 96 MHz does not require settling.	0x0
21:20	R/W	RCHS_INIT_RANGE	Course frequency adjustment	0x1
19:12	R/W	RCHS_INIT_DEL	Fine frequency adjustment	0x80
11:9	R/W	RCHS_INIT_DTCF	Fine duty-cycle adjustment. 0x0: minimum 0x2: default 0x4: maximum 0x5 until 0x7: oscillator does not work	0x2
8:5	R/W	RCHS_INIT_DTC	Course duty-cycle adjustment. 0x0: minimum 0x5: default 0xA: maximum 0xB until 0xF: oscillator does not work	0x5
4:1	R/W	RCHS_BIAS	Bias adjustment. Avoid higher bias trim settings (for example, 0xF), the resulting LDO output voltage might be too high. The voltage can be measured with the GP-ADC.	0x7
0	R/W	RCHS_ENABLE	Enables the HighSpeed RC oscillator. Setting this bit will always-enable the oscillator, overruling the Hardware control	0x0

Table 343: CLK_RCX_REG (0x50000048)

Bit	Mode	Symbol	Description	Reset
11:8	R/W	RCX_BIAS	LDO bias current. 0x0: minimum 0xF: maximum	0xA
7	R/W	RCX_C0	Add unit capacitance to RC-time delay.	0x1
6:2	R/W	RCX_CADJUST	Adjust capacitance part of RC-time delay. 0x00: minimum capacitance 0x1F: maximum capacitance	0x1F
1	R/W	-	Reserved	0x0
0	R/W	RCX_ENABLE	0: Disable the RCX oscillator (watchdog runs at RCLP)	0x0

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Bit	Mode	Symbol	Description	Reset
			1: Enable the RCX oscillator (watchdog runs at RCX)	

Table 344: CLK_RTCDIV_REG (0x5000004C)

Bit	Mode	Symbol	Description	Reset
21	R/W	RTC_RESET_REQ	Reset request for the RTC module	0x0
20	R/W	RTC_DIV_ENABLE	Enable for the 100 Hz generation for the RTC block	0x0
19	R/W	RTC_DIV_DENOM	Selects the denominator for the fractional division: 0b0: 1000 0b1: 1024	0x0
18:10	R/W	RTC_DIV_INT	Integer divisor part for RTC 100 Hz generation	0x147
9:0	R/W	RTC_DIV_FRAC	Fractional divisor part for RTC 100 Hz generation. if RTC_DIV_DENOM=1, <RTC_DIV_FRAC> out of 1024 cycles will divide by <RTC_DIV_INT+1>, the rest is <RTC_DIV_INT> If RTC_DIV_DENOM=0, <RTC_DIV_FRAC> out of 1000 cycles will divide by <RTC_DIV_INT+1>, the rest is <RTC_DIV_INT>	0x2A8

Table 345: BANDGAP_REG (0x50000050)

Bit	Mode	Symbol	Description	Reset
15	R/W	EN_BGR_TCCOMP	Enable Temperature compensation in the reference current for Charger and LED module. 1 = enabled (= default setting) 0 = disabled original currents from BGR are used instead of the Temp-compensated currents	0x1
14:13	R/W	-	Reserved	0x0
12	R/W	BANDGAP_ENABLE_CLAMP	Enables a supply clamp inside the bandgap that improves PSRR. Should be enabled by software after cold boot.	0x0
11:6	R/W	BGR_TRIM	Trim register for bandgap	0x0
5	R/W	SYSRAM_LPMX	RAM Transparent Light Sleep (TLS) Core Enable for System RAMs and Cache RAM. Assert low to enable the TLS core feature, which will result in lower leakage current. In case VDD is below 0.81 V, it is necessary to hold this pin high to maintain data retention.	0x1
4:0	R/W	BGR_ITRIM	Current trimming for bias	0x0

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Table 346: VBUS_IRQ_MASK_REG (0x50000054)

Bit	Mode	Symbol	Description	Reset
2	R/W	-	Reserved	0x0
1	R/W	VBUS_IRQ_EN_RISE	Setting this bit to 1 enables VBUS_IRQ generation when the VBUS starts to ramp above threshold	0x0
0	R/W	VBUS_IRQ_EN_FALL	Setting this bit to 1 enables VBUS_IRQ generation when the VBUS starts to fall below threshold	0x0

Table 347: VBUS_IRQ_CLEAR_REG (0x50000058)

Bit	Mode	Symbol	Description	Reset
15:0	W	VBUS_IRQ_CLEAR	Writing any value to this register will reset the VBUS_IRQ line	0x0

Table 348: BOD_CTRL_REG (0x50000060)

Bit	Mode	Symbol	Description	Reset
18	R/W	BOD_VBUS_RST_EN	If set, generate power-on reset on channel VBUS	0x1
17	R/W	BOD_VBAT_RST_EN	If set, generate power-on reset on channel VBAT.	0x1
16	R/W	-	Reserved	0x1
15	R/W	BOD_VSYS_RST_EN	If set, generate power-on reset on channel VSYS. Bear in mind that there is an additional configurable POR on VSYS rail, check POR_CTRL_REG.	0x1
14	R/W	BOD_V18F_RST_EN	If set, generate power-on reset on channel V18F	0x1
13	R/W	BOD_V18P_RST_EN	If set, generate power-on reset on channel V18P	0x1
12	R/W	BOD_V18_RST_EN	If set, generate power-on reset on channel V18	0x1
11	R/W	BOD_V14_RST_EN	If set, generate power-on reset on channel V14	0x1
10	R/W	BOD_V12_RST_EN	If set, generate power-on reset on channel V12	0x1
9	R/W	BOD_VBUS_EN	Enable brown-out detection for channel VBUS	0x0
8	R/W	BOD_VBAT_EN	Enable brown-out detection for channel VBAT.	0x0
7	R/W	-	Reserved	0x0
6	R/W	BOD_VSYS_EN	Enable brown-out detection for channel VSYS. Bear in mind that there is an additional configurable POR on VSYS rail, check POR_CTRL_REG.	0x0
5	R/W	BOD_V18F_EN	Enable brown-out detection for channel V18F	0x0
4	R/W	BOD_V18P_EN	Enable brown-out detection for channel V18P	0x0
3	R/W	BOD_V18_EN	Enable brown-out detection for channel V18	0x0
2	R/W	BOD_V14_EN	Enable brown-out detection for channel V14	0x0

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Bit	Mode	Symbol	Description	Reset
1	R/W	BOD_V12_EN	Enable brown-out detection for channel VDD (V12)	0x1
0	R/W	BOD_STATUS_CLEAR	Clears BOD_STATUS_REG when this bit is 1 for more than 2 µs. It must be 0 to register BOD events in BOD_STATUS_REG.	0x0

Table 349: BOD_STATUS_REG (0x50000064)

Bit	Mode	Symbol	Description	Reset
8	R	BOD_VBUS	1: below trigger level (BOD event) 0: above trigger level	0x0
7	R	BOD_VBAT	1: below trigger level (BOD event) 0: above trigger level	0x0
6	R	-	Reserved	0x0
5	R	BOD_VSYS	1: below trigger level (BOD event) 0: above trigger level	0x0
4	R	BOD_V18F	1: below trigger level (BOD event) 0: above trigger level	0x0
3	R	BOD_V18P	1: below trigger level (BOD event) 0: above trigger level	0x0
2	R	BOD_V18	1: below trigger level (BOD event) 0: above trigger level	0x0
1	R	BOD_V14	1: below trigger level (BOD event) 0: above trigger level	0x0
0	R	BOD_V12	1: below trigger level (BOD event) 0: above trigger level	0x0

Table 350: P0_PAD_LATCH_REG (0x50000070)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	P0_LATCH_EN	Direct write to the individual pad latching signals. Latches the control signals of the pads for state retention in powerdown mode. 0 = Control signals are retained 1 = Latch is transparant, pad can be recontrolled	0xFFFFFFFF

Table 351: P0_SET_PAD_LATCH_REG (0x50000074)

Bit	Mode	Symbol	Description	Reset
31:0	RWS	P0_SET_LATCH_EN	Direct Set of the marked bits. Reading returns 0x0.	0x0

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Table 352: P0_RESET_PAD_LATCH_REG (0x50000078)

Bit	Mode	Symbol	Description	Reset
31:0	RW1C	P0_RESET_LATCH_EN	Direct Reset of the marked bits. Reading returns 0x0.	0x0

Table 353: P1_PAD_LATCH_REG (0x5000007C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	P1_LATCH_EN	Direct write to the individual pad latching signals. Latches the control signals of the pads for state retention in powerdown mode. 0 = Control signals are retained 1 = Latch is transparant, pad can be recontrolled	0xFFFFFFFF

Table 354: P1_SET_PAD_LATCH_REG (0x50000080)

Bit	Mode	Symbol	Description	Reset
31:0	RWS	P1_SET_LATCH_EN	Direct Set of the marked bits. Reading returns 0x0.	0x0

Table 355: P1_RESET_PAD_LATCH_REG (0x50000084)

Bit	Mode	Symbol	Description	Reset
31:0	RW1C	P1_RESET_LATCH_EN	Direct Reset of the marked bits. Reading returns 0x0.	0x0

Table 356: P2_PAD_LATCH_REG (0x50000088)

Bit	Mode	Symbol	Description	Reset
14:0	R/W	P2_LATCH_EN	Direct write to the individual pad latching signals. Latches the control signals of the pads for state retention in powerdown mode. 0 = Control signals are retained 1 = Latch is transparant, pad can be recontrolled	0x7FFF

Table 357: P2_SET_PAD_LATCH_REG (0x5000008C)

Bit	Mode	Symbol	Description	Reset
14:0	RWS	P2_SET_LATCH_EN	Direct Set of the marked bits. Reading returns 0x0.	0x0

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Table 358: P2_RESET_PAD_LATCH_REG (0x50000090)

Bit	Mode	Symbol	Description	Reset
14:0	RW1C	P2_RESET_LATCH_EN	Direct Reset of the marked bits. Reading returns 0x0.	0x0

Table 359: POR_CTRL_REG (0x50000094)

Bit	Mode	Symbol	Description	Reset
11	R/W	POR_VSYS_SLEEP_CYCLE_EN	Enables POR_VSYS during BOD check cycles in sleep (If POR_VSYS_DISABLE = 0)	0x1
10	R/W	POR_VSYS_HYST_SEL	Selects POR_VSYS threshold level, when hysteresis is disabled (see POR_VSYS_DISABLE) 0: Vthres = VTH_L (low level) 1: Vthres = VTH_H (high level)	0x0
9	R/W	POR_VSYS_HYST_DISABLE	Disable POR_VSYS hysteresis.	0x0
8	R/W	POR_VSYS_FORCE_ON	FORCE POR_VSYS to be ON (also in SLEEP)	0x0
7	R/W	POR_VSYS_MASK	Mask POR on VSYS	0x0
6	R/W	POR_VSYS_DISABLE	Disable POR_VSYS	0x0
5	R/W	POR_V30_SLEEP_CYCLE_EN	Enables POR_V30 during BOD check cycles in sleep (If POR_V30_DISABLE = 0)	0x1
4	R/W	POR_V30_HYST_SEL	Selects POR_VDDA_3V0 threshold level, when hysteresis is disabled (see POR_VDDA_3V0_HYST_DISABLE) 0: Vthres = VTH_L (low level) 1: Vthres = VTH_H (high level)	0x0
3	R/W	POR_V30_HYST_DISABLE	Disable POR_VDDA_3V0 hysteresis; select level with POR_VDDA_3V0_HYST_SEL	0x0
2	R/W	POR_V30_FORCE_ON	Force POR_VDDA_3V0 always ON, (also in SLEEP)	0x0
1	R/W	POR_V30_MASK	Mask POR_VDDA_3V0	0x0
0	R/W	POR_V30_DISABLE	Disable POR_VDDA_3V0	0x0

Table 360: POR_PIN_REG (0x50000098)

Bit	Mode	Symbol	Description	Reset
7	R/W	POR_PIN_POLARITY	0: Active Low 1: Active High Note: This applies only for the GPIO pin. Reset pad is always active High	0x0
6:0	R/W	POR_PIN_SELECT	0x00: P0_00 ... 0x1f: P0_31	0x7F

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Bit	Mode	Symbol	Description	Reset
			0x20: P1_00 ... 0x3F: P1_31 0x40: P2_00 ... 0x4E: P2_14 0x4F to 0x7F: reserved	

Table 361: POR_TIMER_REG (0x5000009C)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	POR_TIME	Time for the POReset to happen. Formula: Time = POR_TIME x 4096 x RC32 clock period Default value: ~3 seconds	0x18

Table 362: RESET_STAT_REG (0x500000BC)

Bit	Mode	Symbol	Description	Reset
6	R/W	SNC_WDOGRESET_STAT	Indicates that a SNC-Watchdog timeout has happened. Note that it is also set when a POReset has happened.	0x1
5	R/W	CMAC_WDOGRESET_STAT	Indicates that a CMAC-Watchdog timeout has happened. Note that it is also set when a POReset has happened.	0x1
4	R/W	SWD_HWRESET_STAT	Indicates that a write to SWD_RESET_REG has happened. Note that it is also set when a POReset has happened.	0x1
3	R/W	WDOGRESET_STAT	Indicates that a Watchdog timeout has happened. Note that it is also set when a POReset has happened.	0x1
2	R/W	SWRESET_STAT	Indicates that a SW Reset has happened	0x1
1	R/W	HWRESET_STAT	Indicates that a HW Reset has happened	0x1
0	R/W	PORESET_STAT	Indicates that a PowerOn Reset has happened. All bitfields of RESET_STAT_REG should be read (to check the source of reset) and then cleared to 0, allowing thus the HW to automatically set to 1 the proper bitfields during the next reset event.	0x1

Table 363: RAM_PWR_CTRL_REG (0x500000C0)

Bit	Mode	Symbol	Description	Reset
27:26	R/W	RAM13_PWR_CTRL	See description of RAM0_PWR_CTRL.	0x0
25:24	R/W	RAM12_PWR_CTRL	See description of RAM0_PWR_CTRL.	0x0

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Bit	Mode	Symbol	Description	Reset
23:22	R/W	RAM11_PWR_CTRL	See description of RAM0_PWR_CTRL.	0x0
21:20	R/W	RAM10_PWR_CTRL	See description of RAM0_PWR_CTRL.	0x0
19:18	R/W	RAM9_PWR_CTRL	See description of RAM0_PWR_CTRL.	0x0
17:16	R/W	RAM8_PWR_CTRL	See description of RAM0_PWR_CTRL.	0x0
15:14	R/W	RAM7_PWR_CTRL	See description of RAM0_PWR_CTRL.	0x0
13:12	R/W	RAM6_PWR_CTRL	See description of RAM0_PWR_CTRL.	0x0
11:10	R/W	RAM5_PWR_CTRL	See description of RAM0_PWR_CTRL.	0x0
9:8	R/W	RAM4_PWR_CTRL	See description of RAM0_PWR_CTRL.	0x0
7:6	R/W	RAM3_PWR_CTRL	See description of RAM0_PWR_CTRL.	0x0
5:4	R/W	RAM2_PWR_CTRL	See description of RAM0_PWR_CTRL.	0x0
3:2	R/W	RAM1_PWR_CTRL	See description of RAM0_PWR_CTRL.	0x0
1:0	R/W	RAM0_PWR_CTRL	Power state control of the individual RAMs. May only change when the memory isn't accessed. When PD_MEM_IS_UP: 0x0: Normal operation 0x1: Normal operation 0x2: Retained (no access possible) 0x3: Off (memory content corrupted) When PD_MEM_IS_DOWN: 0x0: Retained 0x1: Off (memory content corrupted) 0x2: Retained 0x3: Off (memory content corrupted)	0x0

Table 364: SECURE_BOOT_REG (0x500000CC)

Bit	Mode	Symbol	Description	Reset
9	R/W	PROT_OTP_CS_WRITE	This bit will permanentlly disable any write action to the CS inside the OTP	0x0
8	R/W	FORCE_SNC_DEBUGGER_OFF	This bit will permanently disable the SNC debugger	0x0
7	R/W	PROT_OQSPIF_KEY_READ	This bit will permanently disable CPU read capability at OTP offset 0x00000B00 and for the complete segment	0x0
6	R/W	PROT_OQSPIF_KEY_WRITE	This bit will permanently disable ANY write capability at OTP offset 0x00000B00 and for the complete segment	0x0
5	R/W	PROT_AES_KEY_READ	This bit will permanently disable CPU read capability at OTP offset 0x00000A00 and for the complete segment	0x0
4	R/W	PROT_AES_KEY_WRITE	This bit will permanently disable ANY write capability at OTP offset 0x00000A00 and for the complete segment	0x0

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Bit	Mode	Symbol	Description	Reset
3	R/W	PROT_SIG_KEY_WRITE	This bit will permanently disable ANY write capability at OTP offset 0x000008C0 and for the complete segment	0x0
2	R/W	FORCE_CMAC_DEBUGGER_OFF	This bit will permanently disable the CMAC debugger	0x0
1	R/W	FORCE_DEBUGGER_OFF	Follows the respective OTP flag value. Its value is updated by the BootROM code. 1: The system debugger SWD is totally disabled. 0: The system debugger is enabled with DEBUGGER_ENABLE	0x0
0	R/W	SECURE_BOOT	Follows the respective OTP flag value. Its value is updated by the BootROM code. 1: system is a secure system supporting secure boot 0: system is not supporting secure boot	0x0

Table 365: DISCHARGE_RAIL_REG (0x500000D4)

Bit	Mode	Symbol	Description	Reset
5	R/W	RESET_V18F	1: enables immediate discharging of the V18F rail. Note that the source is not disabled. 0: disable immediate discharging of the V18F rail.	0x0
4	R/W	-	Reserved	0x0
3	R/W	RESET_V30	1: enables immediate discharging of the V30 rail. Note that the source is not disabled. 0: disable immediate discharging of the V30 rail.	0x0
2	R/W	RESET_V18P	1: enables immediate discharging of the V18P rail. Note that the source is not disabled. 0: disable immediate discharging of the V18P rail.	0x0
1	R/W	RESET_V18	1: enables immediate discharging of the V18 rail. Note that the source is not disabled. 0: disable immediate discharging of the V18 rail.	0x0
0	R/W	RESET_V14	1: enables immediate discharging of the V14 rail. Note that the source is not disabled. 0: disable immediate discharging of the V14 rail.	0x0

Table 366: WAKEUP_HIBERN_REG (0x500000E0)

Bit	Mode	Symbol	Description	Reset
12	R/W	HIBERNATION_ENABLE	Enable hibernation mode	0x0
11:10	R/W	-	Reserved	0x3
9:6	R/W	WAKEUP_PD_EN	Enables pull-down for GPIO[n] during hibernation Bit 0: P0_20 Bit 1: P0_29 Bit 2: P1_04 Bit 3: P0_28	0xF

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Bit	Mode	Symbol	Description	Reset
5:4	R/W	-	Reserved	0x3
3:0	R/W	WAKEUP_EN	Enables GPIO[n] to wake up from hibernation Bit 0: P0_20 Bit 1: P0_29 Bit 2: P1_04 Bit 3: P0_28	0xF

Table 367: SW_V18F_REG (0x500000E4)

Bit	Mode	Symbol	Description	Reset
3:2	R/W	DELAY_TRIM	Soft start delay trim	0x1
1	R/W	SKIP_SOFT_START	Skip soft start routine	0x0
0	R/W	FORCE_SW_ON	Forces closing sw_V18f, independent of v18p state	0x0

Table 368: BIAS_VREF_SEL_REG (0x500000E8)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	BIAS_VREF_RF2_SEL	Same coding as BIAS_VREF_RF1_SEL.	0xB
3:0	R/W	BIAS_VREF_RF1_SEL	Vref_code | Vref_Voltage (mV) 0:900 1:930 2:960 3:990 4:1020 5:1050 6:1080 7:1110 8:1140 9:1170 10:1200 11:1230 12:1260 13:1290 14:1320 15:1350	0xB

Table 369: ANA_STATUS_REG (0x500000EC)

Bit	Mode	Symbol	Description	Reset
29	R	FLAG_LDO_V30_COMBINED_OK	When high, ldo_v30 OR ldo_v30_ret is active (for VAD system)	0x0

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Bit	Mode	Symbol	Description	Reset
28	R	XOR_DOUT_WAKE UP_PADS	Will be the result of XOR operation of the hibernation wake-up pads outputs combined. DFT_EN_INPUT_PD_AON_PADS in TEST_CTRL5_REG must be 1.	0x0
27	R	VBUS_AVAILABLE	High when VBUS > (VBAT + 150 mV). Hysteresis is approx. 40 mV	0x0
26	R	FLAG_ADC_LDO_ OK	When high, ldo_adc is active	0x0
25	R	FLAG_IBIAS_TRIM	10 nA Iref trimming, high when on-chip current is larger than reference current	0x0
24	R	BOD_VIN_NOK	General output of the BOD to indicate that one of the monitored inputs is below the trigger-level.	0x0
23	R	BG_OK	When high bandgap is active	0x0
22	R	BOOST_DCDC_VL ED_OK	When high, boost dcdc vled is active	0x0
21	R	LDO_VSYS_HIGH_ TEMP	If 1 indicates that temperature of LDO_VSYS is above operating conditions	0x0
20:19	R	VBAT_VSYS_STAT E	0x0 : Hibernation mode or VBUS-only (sysbat switch opened). 0x1 : Test mode (sysbat switch closed). 0x2 : Ideal diode enabled (with VBAT-only or VBUS and VBAT) . 0x3 : Sleep mode (with VBAT-only, sysbat switch closed).	0x0
18	R	LDO_VSYS_HEAD_ LIM	When high, the headroom loop is controlling VSYS	0x0
17	R	LDO_VSYS_CURR _LIM	When high, the current limiter is controlling VSYS	0x0
16	R	LDO_VSYS_LIM	When high, the voltage loop is controlling VSYS	0x0
15	R	LDO_VSYS_OK	When high, LDO_VSYS is in regulating mode	0x0
14	R	-	Reserved	0x0
13	R	LDO_V30_OK	When high, ldo_v30 is active	0x0
12	R	SWITCH_V18F_OK	V18F switch completely closed	0x0
11	R	BUCK_DCDC_V18 P_OK	V18P Rail ok based on DCDC V18P programmed level	0x0
10	R	BUCK_DCDC_V18_ OK	V18 Rail ok based on DCDC V18 programmed level	0x0
9	R	BUCK_DCDC_V14_ OK	V14 Rail ok based on DCDC V14 programmed level	0x0
8	R	BUCK_DCDC_V12_ OK	V12 Rail ok based on DCDC V12 programmed level	0x0
7	R	COMP_VBUS_PLU GIN	VBUS is connected (VBUS > 2.5 V)	0x0
6	R	COMP_VSYS_NEA R_VLED	BOOST_VLED_SEL=0x0 : VSYS>4.3 BOOST_VLED_SEL=0x1 : VSYS>4.55 BOOST_VLED_SEL=0x2 : VSYS>4.8 BOOST_VLED_SEL=0x3 : VSYS>4.8	0x0

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Bit	Mode	Symbol	Description	Reset
5	R	COMP_VBUS_ABOVE_VSYS	VBUS>VSYS+0.05 V	0x0
4	R	COMP_VSYS_OK	VSYS> 2.45 V	0x0
3	R	COMP_VBAT_OK	VBAT> 2.7 V	0x0
2	R	COMP_VBUS_OK	1: VBUS> 4.1 V 0: VBUS<3.4 V	0x0
1	R	POR_VSYS_OK	When high, VSYS is higher then POR threshold	0x0
0	R	POR_V30_OK	When high, V30 is higher then POR threshold	0x0

Table 370: POWER_CTRL_REG (0x500000F0)

Bit	Mode	Symbol	Description	Reset
31:28	R/W	-	Reserved	0x0
27	R/W	EN_RCX_SUPPLY_BIAS	RCX supply bias switch for calibration. This bit needs to be 0 before entering hibernation, otherwise a POR will occur.	0x0
26:25	R/W	-	Reserved	0x0
24	R/W	DCDC_BOOST_CLAMP_EN	Enables clamp circuit between V_LED and ground in the boost converter to bleed of spikes caused by switching currents in bondwires.	0x1
23	R/W	-	Reserved	0x0
22	R/W	-	Reserved	0x0
21:20	R/W	-	Reserved	0x0
19	R/W	SW_V18F_SLEEP_ON	Closes the V18F switch in sleep when DCDC_V18P_SLEEP_EN is 1. See SW_V18F register for more settings.	0x1
18	R/W	SW_V18F_ON	Closes the V18F switch when DCDC_V18P_EN is 1. See SW_V18F register for more settings.	0x1
17	R/W	DCDC_VLED_SLEEP_EN	Enables boost dcdc led rail in sleep mode	0x0
16	R/W	DCDC_VLED_EN	Enables boost dcdc led rail in active mode	0x0
15	R/W	DCDC_V18P_SLEEP_EN	Enables buck dcdc V18p rail in sleep mode	0x1
14	R/W	DCDC_V18P_EN	Enables buck dcdc V18p rail in active mode	0x1
13	R/W	DCDC_V18_SLEEP_EN	Enables buck dcdc V18 rail in sleep mode	0x0
12	R/W	DCDC_V18_EN	Enables buck dcdc V18 rail in active mode	0x0
11	R/W	DCDC_V14_SLEEP_EN	Enables buck dcdc V14 rail in sleep mode	0x0
10	R/W	DCDC_V14_EN	Enables buck dcdc V14 rail in active mode	0x0
9	R/W	DCDC_V12_SLEEP_EN	Enables buck dcdc V12 rail in sleep mode	0x1
8	R/W	DCDC_V12_EN	Enables buck dcdc V12 rail in active mode	0x1

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Bit	Mode	Symbol	Description	Reset
7	R/W	CLAMP_V12_DIS	Disables V12 clamp. During Hibernation, V12 clamp will be enabled regardless of this bit.	0x1
6	R/W	CLAMP_V30_EN	Enables V30 clamp.	0x0
5	R/W	-	Reserved	0x0
4	R/W	LDO_RET_V30_SLEEP_EN	Enables ldo V30 ret in sleep mode	0x1
3	R/W	LDO_RET_V30_EN	Enables ldo V30 ret in active mode	0x0
2	R/W	LDO_V30_SLEEP_EN	Enables ldo V30 in sleep mode	0x0
1	R/W	LDO_V30_EN	Enables ldo V30 in active mode	0x1
0	R/W	LDO_START_DISABLE	Disables ldo start.	0x1

Table 371: PMU_SLEEP_REG (0x500000F4)

Bit	Mode	Symbol	Description	Reset
31	R/W	ULTRA_FAST_WAKEUP	Allows the core to start running on the RC32M while the PMU is still waiting for supplies to settle to the final value. Only use in combination with FAST_WAKEUP and 0.9 V on VDD during sleep.	0x0
30	R/W	ENABLE_FAST_SWITCH	Enables early clock switching upon event detection to speed up the wake-up time	0x0
29:23	R/W	VLED_BYPASS_REFRESH_TIME	Determines how long the VLED bypass switch is closed when VSYS near VLED flag and VLED VNOK flag are asserted in sleep. Each 1 LSB represents 31.25 µs. If VLED_BYPASS_REFRESH_TIME(sec) >= BASE_REFRESH_INTERVAL(sec), then VLED bypass switch will remain closed while VSYS near VLED flag is high during sleep. If VLED_BYPASS_REFRESH_TIME = 0, then VLED bypass switch will remain opened in sleep independently on the state of VSYS near VLED comparator, and will only be closed if needed during the boost refresh cycles.	0x1
22:19	R/W	BOD_SLEEP_INTERVAL	This is the interval at which the BOD comparators/POR will be checked during sleep. Value represents RAILS_REFRESH_INTERVAL times-> BOD and POR are checked every(sec)=BASE_REFRESH_INTERVAL(sec)*RAILS_REFRESH_INTERVAL*BOD_SLEEP_INTERVAL If 0, BOD/POR will not be checked in sleep.	0x1
18:5	R/W	RAILS_REFRESH_INTERVAL	This is the interval at which the power rails reference voltage will be refreshed during sleep. Value represents BASE_REFRESH_INTERVAL times-> Rails refresh every(sec)=BASE_REFRESH_INTERVAL(sec)*RAILS_REFRESH_INTERVAL. If 0, then voltage reference will not be refreshed in sleep, and BOD/POR will not be checked in sleep.	0xF0

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Bit	Mode	Symbol	Description	Reset
4:0	R/W	BASE_REFRESH_INTERVAL	This sets the base time for calculating the intervals at which PMU refreshes during sleep. In addition, if DCDC_VLED_SLEEP_EN=1, this will be the VLED refresh interval. Each 1 LSB represents 0.125 ms. Thus, max base time = 3.875 ms. If 0, then there will not be any refresh cycle in SLEEP.	0x8

Table 372: POWER_LVL_REG (0x500000F8)

Bit	Mode	Symbol	Description	Reset
19	R/W	-	Reserved	0x0
18:17	R/W	VSYS_LEVEL	Level setting for VSYS rail when ldo_vsys is enabled (COMP_VBUS_OK & COMP_VBUS_ABOVE_VSYS): 0: 4.8 V 1: 4.6 V 2: 4.4 V 3: 4.2 V	0x0
16	R/W	V18_LEVEL	Level setting for V18 rail: 0: 1.2 V 1: 1.8 V	0x1
15:14	R/W	V14_LEVEL	Level setting for V14 rail: 0: 1.2 V 1: 1.3 V 2: 1.4 V 3: 1.5 V	0x2
13:12	R/W	V12_SLEEP_LEVEL	Level setting for V12 rail in sleep: 0: 0.75 V 1: 0.9 V 2: 1.2 V 3: reserved	0x1
11:10	R/W	V12_LEVEL	Level setting for V12 rail: 0: 0.75 V 1: 0.9 V 2: 1.2 V 3: reserved	0x2
9:8	R/W	V30_SLEEP_LEVEL	Level setting for V30 in sleep: 0x0: 3.0 V 0x1: reserved 0x2: 3.3 V 0x3: 3.3 V	0x0
7:6	R/W	V30_LEVEL	Level setting for V30: 0x0: 3.0 V 0x1: reserved 0x2: 3.3 V	0x0

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Bit	Mode	Symbol	Description	Reset
			0x3: 3.3 V	
5:3	R/W	-	Reserved	0x6
2:0	R/W	-	Reserved	0x0

Table 373: Register map CRG_VSYS

Address	Register	Description
0x50000B00	VSYS_GEN_CTRL_REG	
0x50000B04	VSYS_GEN_IRQ_STATUS_REG	
0x50000B08	VSYS_GEN_IRQ_CLEAR_REG	
0x50000B0C	VSYS_GEN_IRQ_MASK_REG	

Table 374: VSYS_GEN_CTRL_REG (0x50000B00)

Bit	Mode	Symbol	Description	Reset
24:23	R/W	FORCE_VBAT_VSYS_SW	0x0,0x1: VBAT_VSYS set to ideal diode 0x2: Forces VBAT_VSYS switch to be opened 0x3: Forces VBAT_VSYS switch to be closed	0x0
22:21	R/W	FORCE_LDO_ENABLE	0x0,0x1: LDO VSYS will be enabled when COMP_VBUS_OK & COMP_VBUS_ABOVE_VSYS. 0x2: LDO_VSYS will be disabled regardless of VBUS state 0x3: LDO_VSYS will be enabled regardless of VBUS state	0x0
20:19	R/W	LDO_TEMP_PROTECT_MODE	0x0: LDO_VSYS is muted (disabled) when temperature is too high, when temperature is back to operating conditions ldo is unmuted 0x1: LDO_VSYS is muted (disabled) when temperature is too high, LDO_VSYS_HIGH_TEMP_IRQ must be cleared to allow ldo to be unmuted. See VSYS_GEN_IRQ_CLEAR_REG. 0x2: LDO_VSYS is not muted (disabled) when temperature is too high 0x3: Force LDO_VSYS mute	0x0
18	R/W	EN_HEADROOM	Enables the voltage headroom loop in the LDO_VSYS.	0x1
17:13	R/W	CURLIM_OFFSET_TRIM	For adjusting the offset of the curlim range (+/- 78 mA) 0x0 = maximum positive offset. 0x10 = minimal offset (reset value). 0x1F = maximum negative offset.	0x10

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Bit	Mode	Symbol	Description	Reset
12:8	R/W	CURLIM_GAIN_TRIM	For adjusting the gain of the curlim range (+/- 20%) 0x0 = maximum gain. 0x10 = nominal gain (reset value). 0x1F = minimum gain.	0x10
7:1	R/W	CURLIM_SET	Sets the level of the LDO_VSYS current limiter in 10 mA steps. It is reset when vbus is not plugged (COMP_VBUS_PLUGIN == 0). 0x0 = 1270 mA 0x1 = 1260 mA ... 0x76 = 90 mA (reset value)	0x76
0	R/W	EN_CURLIM	Enables the current limiter in the LDO_VSYS	0x1

Table 375: VSYS_GEN_IRQ_STATUS_REG (0x50000B04)

Bit	Mode	Symbol	Description	Reset
1	R	VBUS_LOW_DRIVE_IRQ_STATUS	Indicates vbus drive strength is not enough to keep vbus up with the set limit of ldo_vbus. Consider lowering CURLIM_SET in VSYS_GEN_CTRL_REG.	0x0
0	R	LDO_VSYS_HIGH_TEMP_IRQ_STATUS	Indicates that a high temperature has been detected at ldo_vsys	0x0

Table 376: VSYS_GEN_IRQ_CLEAR_REG (0x50000B08)

Bit	Mode	Symbol	Description	Reset
1	R0/W	VBUS_LOW_DRIVE_IRQ_CLEAR	Clears VBUS_LOW_DRIVE_IRQ	0x0
0	R0/W	LDO_VSYS_HIGH_TEMP_IRQ_CLEAR	Clears LDO_VSYS_HIGH_TEMP_IRQ	0x0

Table 377: VSYS_GEN_IRQ_MASK_REG (0x50000B0C)

Bit	Mode	Symbol	Description	Reset
1	R/W	VBUS_LOW_DRIVE_IRQ_MASK	Masks VBUS_LOW_DRIVE_IRQ interrupt. It is reset when vbus is not plugged in (COMP_VBUS_PLUGIN == 0). This is because when vbus is just plugged in, it is likely to bounce; therefore IRQ is masked to avoid false triggering. Some time after vbus plugin, software might increase ldo_vsys current limit and should set this mask to 0 (after clearing IRQ).	0x1
0	R/W	LDO_VSYS_HIGH_TEMP_IRQ_MASK	Masks LDO_VSYS_HIGH_TEMP_IRQ interrupt	0x0

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44.7 Data Cache Controller Registers

Table 378: Register map DCACHE

Address	Register	Description
0x30100000	DCACHE_CTRL_REG	Dcache Control register
0x30100004	DCACHE_BASE_ADDR_REG	Dcache base address for cacheable region
0x30100008	DCACHE_MRM_HITS_REG	Dcache MRM (Miss Rate Monitor) HITS register
0x3010000C	DCACHE_MRM_MISSES_REG	Dcache MRM (Miss Rate Monitor) MISSES register
0x30100010	DCACHE_MRM_EVICTS_REG	Dcache MRM (Miss Rate Monitor) EVICTS register
0x30100014	DCACHE_MRM_CTRL_REG	Dcache MRM (Miss Rate Monitor) CONTROL register
0x30100018	DCACHE_MRM_TINT_REG	Dcache MRM (Miss Rate Monitor) TIME INTERVAL register
0x3010001C	DCACHE_MRM_MISSES_THRES_REG	Dcache MRM (Miss Rate Monitor) THRESHOLD register
0x30100020	DCACHE_MRM_HITS_THRES_REG	Dcache MRM (Miss Rate Monitor) HITS THRESHOLD register
0x30100024	DCACHE_MRM_EVICTS_THRES_REG	Dcache MRM (Miss Rate Monitor) EVICTS THRESHOLD register

Table 379: DCACHE_CTRL_REG (0x30100000)

Bit	Mode	Symbol	Description	Reset
31:27	R	-	Reserved	0x0
26	R/W	DCACHE_BYPASS	0: All AHB transfers are going via the DCACHE, depending on the DCACHE_ENABLE, DCACHE_LEN and DCACHE_BASE_ADDR data is cached or not. 1: Bypass the DCACHE completly, all accesses towards the QSPIC2 controller are routed arround the DCACHE	0x0
25	R/W	-	Reserved	0x0
24	R/W	DCACHE_WBUFFER_FLUSH	Write buffer flush 0: Write buffer isn't flushed (default) 1: Write buffer is flushed	0x0
23	R	DCACHE_WBUFFER_EMPTY	Status of the write buffer 0: Write buffer isn't empty 1: Write buffer is empty	0x1
22	R/W	DCACHE_WFLUSHED	0: DCACHE is not write flushed yet. 1: DCACHE is write flushed.	0x0

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Bit	Mode	Symbol	Description	Reset
			Note 1: Setting and clearing of this (status) bit field is automatically done by the hardware. Note 2: The *CACHE_WFLUSHED* bit can also be cleared first by the software by writing a 0	
21	R	DCACHE_READY	0: DCACHE isn't initialized yet 1: DCACHE initialization has been completed	0x0
20	R0/W	DCACHE_WFLUSH	Write a 1 to this field will trigger a write flush of the "dirty" lines. All modified data in "dirty" line will be written back to the PSRAM. The corresponding "dirty" bits will be cleared. Reading this bit will return 0.	0x0
19	R0/W	DCACHE_INIT	Write a 1 to this field will trigger an initialization of the cache (0s are written in the TAG area). Reading from this field will always return 0.	0x0
18	R/W	DCACHE_ENABLE	Enable the dcache controller HW block: 0: Disabled, all AHB accesses towards the QSPI are bypassing the HW block straight into the PSRAM 1: Enabled, all AHB access towards the QSPI within the cacheable region are cached.	0x0
17:0	R/W	DCACHE_LEN	Length of PSRAM cacheable memory N*1 kB. N = 0 to 131072 (max. of 128 MB). Setting DCACHE_LEN = 0 disables the caching.	0x0

Table 380: DCACHE_BASE_ADDR_REG (0x30100004)

Bit	Mode	Symbol	Description	Reset
16:0	R/W	DCACHE_BASE_ADDR	Base of PSRAM cacheable memory N*1 kB. N = 0 to 131072 (max. of 128 MB).	0x0

Table 381: DCACHE_MRM_HITS_REG (0x30100008)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	MRM_HITS	Contains the amount of cache hits.	0x0

Table 382: DCACHE_MRM_MISSES_REG (0x3010000C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	MRM_MISSES	Contains the amount of cache misses.	0x0

Table 383: DCACHE_MRM_EVICTS_REG (0x30100010)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	MRM_EVICTS	Contains the amount of cache evicts	0x0

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Table 384: DCACHE_MRM_CTRL_REG (0x30100014)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0
5	R/W	MRM_IRQ_EVICTS_THRES_STATUS	0: No interrupt is generated. 1: Interrupt (pulse-sensitive) is generated because the number of cache evicts reached the programmed threshold (threshold != 0).	0
4	R/W	MRM_IRQ_HITS_THRES_STATUS	0: No interrupt is generated. 1: Interrupt (pulse-sensitive) is generated because the number of cache hits reached the programmed threshold (threshold != 0).	0
3	R/W	MRM_IRQ_MISSES_THRES_STATUS	0: No interrupt is generated. 1: Interrupt (pulse-sensitive) is generated because the number of cache misses reached the programmed threshold (threshold != 0).	0
2	R/W	MRM_IRQ_TINT_STATUS	0: No interrupt is generated. 1: Interrupt (pulse-sensitive) is generated because the time interval counter reached the end (time interval != 0).	0
1	R/W	MRM_IRQ_MASK	0: Disables interrupt generation. 1: Enables interrupt generation. Note: The Cache MRM generates a pulse-sensitive interrupt towards the ARM processor	0
0	R/W	MRM_START	0: Freeze the "misses/hits" counters and reset the time interval counter to the programmed value in CACHE_MRM_TINT_REG. 1: Enables the counters. Note: In case CACHE_MRM_CTRL_REG[MRM_START] is set to 1 and CACHE_MRM_TINT_REG (!=0) is used for the MRM interrupt generation, the time interval counter counts down (on a fixed reference clock of 16 MHz) until it is 0. At that time CACHE_MRM_CTRL_REG[MRM_START] will be reset automatically to 0 by the MRM hardware and the MRM interrupt will be generated.	0

Table 385: DCACHE_MRM_TINT_REG (0x30100018)

Bit	Mode	Symbol	Description	Reset
31:19	-	-	Reserved	0x0
18:0	R/W	MRM_TINT	Defines the time interval for the monitoring in 32 MHz clock cycles. See also the description of CACHE_MRM_CTRL_REG[MRM_IRQ_TINT_STATUS]. Note: When MRM_TINT=0 (unrealistic value), no interrupt will be generated.	0x0

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Table 386: DCACHE_MRM_MISSES_THRES_REG (0x3010001C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	MRM_MISSES_THRES	Defines the misses threshold to trigger the interrupt generation. See also the description of CACHE_MRM_CTRL_REG[MRM_IRQ_MISSES_THRES_STATUS]. Note: When MRM_MISSES_THRES=0 (unrealistic value), no interrupt will be generated.	0x0

Table 387: DCACHE_MRM_HITS_THRES_REG (0x30100020)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	MRM_HITS_THRES	Defines the hits threshold to trigger the interrupt generation. See also the description of CACHE_MRM_CTRL_REG[MRM_IRQ_HITS_THRES_STATUS]. Note: When MRM_HITS_THRES=0 (unrealistic value), no interrupt will be generated.	0x0

Table 388: DCACHE_MRM_EVICTS_THRES_REG (0x30100024)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	MRM_EVICTS_THRES	Defines the hits threshold to trigger the interrupt generation. See also the description of CACHE_MRM_CTRL_REG[MRM_IRQ_EVICTS_THRES_STATUS]. Note: When MRM_EVICTS_THRES=0 (unrealistic value), no interrupt will be generated.	0x0

44.8 SIMO DCDC Converter Registers

Table 389: Register map DCDC

Address	Register	Description
0x50000300	BUCK_CTRL_REG	DCDC Buck Control Register

Table 390: BUCK_CTRL_REG (0x50000300)

Bit	Mode	Symbol	Description	Reset
15:14	R/W	CFG_TIMEOUT	Sets maximum switch on-time. 0x0: Disabled 0x1: 0.5 µs 0x2: 1.0 µs (Default) 0x3: 1.5 µs	0x2
13	R/W	EN_FREEWHEEL	Enables freewheel switch when converter is idle.	0x0
12:10	R/W	TRIM_BIAS	Bias current trim.	0x3

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Bit	Mode	Symbol	Description	Reset
			0x0: +21 % 0x1: +14 % 0x2: +7 % 0x3: +0 % (Default) 0x4: -7 % 0x5: -14 % 0x6: -21 % 0x7: -28 %	
9:8	R/W	-	Reserved	0x0
7:5	R/W	CFG_IMAX_UPPER	Sets upper value of inductor peak current limit control. 0x0: 260 mA 0x1: 400 mA 0x2: 530 mA 0x3: 660 mA 0x4: 790 mA 0x5: 920 mA 0x6: 1060 mA (Default) 0x7: 1190 mA	0x6
4:2	R/W	CFG_IMAX_LOWER	Sets lower value of inductor peak current limit control. 0x0: 260 mA (Default) 0x1: 400 mA 0x2: 530 mA 0x3: 660 mA 0x4: 790 mA 0x5: 920 mA 0x6: 1060 mA 0x7: 1190 mA	0x0
1:0	R/W	CFG_HYST	Controls hysteresis on output comparator. Values listed are typical. 0x0: 6 mV (Default) 0x1: 9 mV 0x2: 12 mV 0x3: 15 mV	0x0

44.9 DCDC Boost Converter Registers

Table 391: Register map DCDC_BOOST

Address	Register	Description
0x50000500	VLED_PWR_CTRL_REG	VLED Power Control Register
0x50000504	VLED_PWR_STATUS_REG	VLED Power Status Register
0x50000508	BOOST_CTRL_REG0	DCDC Boost Control Register
0x5000050C	BOOST_CTRL_REG1	DCDC Boost Second Control Register

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Address	Register	Description
0x50000514	BOOST_STATUS_REG	DCDC Boost Status Register

Table 392: VLED_PWR_CTRL_REG (0x50000500)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	VLED_PWR_FORCE	Manual selection of VLED supply source, requires that VLED_PWR_MANUAL = 0x1 0x0: VLED not powered 0x1: VLED powered by VSYS 0x2: VLED powered by boost converter 0x3: N.A.	0x0
10	R/W	VLED_PWR_MANUAL	0x0: VLED supply source automatically selected 0x1: VLED supply source manually selected	0x0
9	R/W	VLED_PWR_USE_VSYS_LVL	Sets the condition for powering VLED from VSYS 0x0: VLED always powered from VSYS 0x1: VLED powered form VSYS if VSYS is near VLED, depending on vsys-comparator (Default)	0x1
8	R/W	VLED_PWR_ENABLE	0x0: VLED power controller disabled 0x1: VLED power controller enabled	0x0
7:0	R/W	VSYS_OK_DEBOUNCE	Sets debounce time on VSYS comparator in steps of 1.024 ms Note: actual delay can be up to one period of 1.024 ms clock shorter than programmed depending on alignment of comparator trip event and clock edge	0x0

Table 393: VLED_PWR_STATUS_REG (0x50000504)

Bit	Mode	Symbol	Description	Reset
5	R	VLED_PWR_ALLOW_BOOST	Indicates whether boost converter is blocked or not	0x0
4	R	VLED_PWR_VSYS_CONNECTED	Indicates that VSYS switch is closed	0x0
3:2	R	VLED_PWR_SWITCH_CTRL_STATE	State of the VLED power control FSM 0x0: Disabled 0x1: VSYS 0x2: Boost 0x3: N.A.	0x0
1	R	VSYS_OK_DEBOUNCED	Output of VSYS OK debounce logic	0x0
0	R	VSYS_OK	Output of VSYS OK logic	0x0

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Table 394: BOOST_CTRL_REG0 (0x50000508)

Bit	Mode	Symbol	Description	Reset
20:17	R/W	BOOST_TIMEOUT_TRIG_DELAY	Delay before generating next comparator clock after a timeout event on the P switch, allows inductor current to drop to zero 0x0: Disabled 0x1: 250 ns 0x2: 500 ns 0x3: 750 ns 0x4: 1000 ns (default) 0x5: 1250 ns 0x6: 1500 ns 0x7: 1750 ns 0x8: 2000 ns 0x9: 2250 ns 0xA: 2500 ns 0xB: 2750 ns 0xC: 3000 ns 0xD: 3250 ns 0xE: 3500 ns 0xF: 3750 ns	0x4
16:13	R/W	BOOST_PSW_TIMEOUT	P switch timeout, if switch is closed longer than this a timeout is generated and the FSM is forced to the next state 0x0: Disabled 0x1: 250 ns 0x2: 500 ns 0x3: 750 ns 0x4: 1000 ns 0x5: 1250 ns 0x6: 1500 ns 0x7: 1750 ns 0x8: 2000 ns (default) 0x9: 2250 ns 0xA: 2500 ns 0xB: 2750 ns 0xC: 3000 ns 0xD: 3250 ns 0xE: 3500 ns 0xF: 3750 ns	0x8
12:9	R/W	BOOST_NSW_TIMEOUT	N switch timeout, if switch is closed longer than this a timeout is generated and the FSM is forced to the next state 0x0: Disabled 0x1: 125 ns 0x2: 250 ns 0x3: 375 ns 0x4: 500 ns 0x5: 625 ns 0x6: 750 ns (default)	0x6

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Bit	Mode	Symbol	Description	Reset
			0x7: 875 ns 0x8: 1000 ns 0x9: 1125 ns 0xA: 1250 ns 0xB: 1375 ns 0xC: 1500 ns 0xD: 1625 ns 0xE: 1750 ns 0xF: 1875 ns	
8:7	R/W	BOOST_OK_CLR_COUNT	Number of subsequent V_NOK events before BOOST_VLED_OK is reset 0x0: 2 0x1: 4 0x2: 8 (default) 0x3: 15	0x2
6:5	R/W	BOOST_IDLE_CLK_DIV	Determines times between comparator samples when converter is idle 0x0 = 250 ns 0x1 = 500 ns (default) 0x2 = 1000 ns 0x3 = 2000 ns	0x1
4:2	R/W	BOOST_VLED_TRIM	Trim setting for boost converter, sets deviation from nominal output voltage (4 V) 0x0: -75 mV 0x1: -50 mV 0x2: -25 mV 0x3: 0 mV (default) 0x4: 25 mV 0x5: 50 mV 0x6: 75 mV 0x7: 100 mV	0x3
1:0	R/W	BOOST_VLED_SEL	Voltage selection for boost converter, sets nominal output voltage 0x0: 4.50V (default) 0x1: 4.75V 0x2: 5.00V 0x3: 5.00V	0x0

Table 395: BOOST_CTRL_REG1 (0x5000050C)

Bit	Mode	Symbol	Description	Reset
17	R/W	BOOST_CUR_LIM_SLEEP_FIXED	Enable fixed current iso dynamic current in sleep mode 0x0: Use dynamic current control 0x1: Use fixed current as defined in BOOST_CUR_LIM_SLEEP (default)	0x1
16:12	R/W	BOOST_CUR_LIM_SLEEP	Fixed inductor peak current limit in sleep mode I = 30 mA * (1 + N), default 960 mA	0x1F

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Bit	Mode	Symbol	Description	Reset
11:10	R/W	BOOST_CUR_LIM_STEP	Step size taken by automatic inductor peak current limit control 0x0: 0 (disabled) 0x1: 1 0x2: 2 (default) 0x3: 3	0x2
9:5	R/W	BOOST_CUR_LIM_MAX	Maximum inductor peak current limit I = 30 mA * (1 + N), default 960 mA	0x1F
4:0	R/W	BOOST_CUR_LIM_MIN	Minimum inductor peak current limit I = 30 mA * (1 + N), default 150 mA	0x4

Table 396: BOOST_STATUS_REG (0x50000514)

Bit	Mode	Symbol	Description	Reset
23:18	R	BOOST_COMP_TRIM	Actual P side comparator trim value	0x0
17	R	BOOST_IDLE	Converter idle	0x1
16:12	R	BOOST_CUR_LIM	Actual inductor peak current limit	0x4
11	R	BOOST_COMP_P_DYN_P	P output of P side dynamic comparator	0x0
10	R	BOOST_COMP_P_DYN_N	N output of P side dynamic comparator	0x0
9	R	BOOST_COMP_P_CONT	Output of P side continuous time comparator	0x0
8	R	BOOST_COMP_N_CONT	Output of N side continuous time comparator	0x0
7	R	BOOST_TIMEOUT_PSW	Timeout on P switch occurred	0x0
6	R	BOOST_TIMEOUT_NSW	Timeout on N switch occurred	0x0
5	R	BOOST_VOUT_NOK	NOK output of output voltage comparator	0x0
4	R	BOOST_VOUT_OK	OK output of output voltage comparator	0x0
3:2	R	BOOST_SW_STATE	State of boost converter switches 0x0: Both off 0x1: P switch on 0x2: N switch on 0x3: Undefined	0x0
1	R	BOOST_STARTUP_COMPLETE	Indicates if the converter is enabled and the startup counter has expired (internal biasing settled)	0x0
0	R	BOOST_VLED_OK	Indicates that V_LED is above its threshold, reset after too many subsequent V_NOK events	0x0

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44.10 DMA Controller Registers

Table 397: Register map DMA

Address	Register	Description
0x51000400	DMA0_A_START_REG	Source address register of DMA channel 0
0x51000404	DMA0_B_START_REG	Destination address register of DMA channel 0
0x51000408	DMA0_INT_REG	Interrupt length register of DMA channel 0
0x5100040C	DMA0_LEN_REG	Transfer length register of DMA channel 0
0x51000410	DMA0_CTRL_REG	Control register of DMA channel 0
0x51000414	DMA0_IDX_REG	Index pointer register of DMA channel 0
0x51000420	DMA1_A_START_REG	Source address register of DMA channel 1
0x51000424	DMA1_B_START_REG	Destination address register of DMA channel 1
0x51000428	DMA1_INT_REG	Interrupt length register of DMA channel 1
0x5100042C	DMA1_LEN_REG	Transfer length register of DMA channel 1
0x51000430	DMA1_CTRL_REG	Control register of DMA channel 1
0x51000434	DMA1_IDX_REG	Index pointer register of DMA channel 1
0x51000440	DMA2_A_START_REG	Source address register of DMA channel 2
0x51000444	DMA2_B_START_REG	Destination address register of DMA channel 2
0x51000448	DMA2_INT_REG	Interrupt length register of DMA channel 2
0x5100044C	DMA2_LEN_REG	Transfer length register of DMA channel 2
0x51000450	DMA2_CTRL_REG	Control register of DMA channel 2
0x51000454	DMA2_IDX_REG	Index pointer register of DMA channel 2
0x51000460	DMA3_A_START_REG	Source address register of DMA channel 3
0x51000464	DMA3_B_START_REG	Destination address register of DMA channel 3
0x51000468	DMA3_INT_REG	Interrupt length register of DMA channel 3
0x5100046C	DMA3_LEN_REG	Transfer length register of DMA channel 3
0x51000470	DMA3_CTRL_REG	Control register of DMA channel 3
0x51000474	DMA3_IDX_REG	Index pointer register of DMA channel 3
0x51000480	DMA4_A_START_REG	Source address register of DMA channel 4
0x51000484	DMA4_B_START_REG	Destination address register of DMA channel 4
0x51000488	DMA4_INT_REG	Interrupt length register of DMA channel 4
0x5100048C	DMA4_LEN_REG	Transfer length register of DMA channel 4
0x51000490	DMA4_CTRL_REG	Control register of DMA channel 4
0x51000494	DMA4_IDX_REG	Index pointer register of DMA channel 4

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Address	Register	Description
0x510004A0	DMA5_A_START_REG	Source address register of DMA channel 5
0x510004A4	DMA5_B_START_REG	Destination address register of DMA channel 5
0x510004A8	DMA5_INT_REG	Interrupt length register of DMA channel 5
0x510004AC	DMA5_LEN_REG	Transfer length register of DMA channel 5
0x510004B0	DMA5_CTRL_REG	Control register of DMA channel 5
0x510004B4	DMA5_IDX_REG	Index pointer register of DMA channel 5
0x510004C0	DMA6_A_START_REG	Source address register of DMA channel 6
0x510004C4	DMA6_B_START_REG	Destination address register of DMA channel 6
0x510004C8	DMA6_INT_REG	Interrupt length register of DMA channel 6
0x510004CC	DMA6_LEN_REG	Transfer length register of DMA channel 6
0x510004D0	DMA6_CTRL_REG	Control register of DMA channel 6
0x510004D4	DMA6_IDX_REG	Index pointer register of DMA channel 6
0x510004E0	DMA7_A_START_REG	Source address register of DMA channel 7
0x510004E4	DMA7_B_START_REG	Destination address register of DMA channel 7
0x510004E8	DMA7_INT_REG	Interrupt length register of DMA channel 7
0x510004EC	DMA7_LEN_REG	Transfer length register of DMA channel 7
0x510004F0	DMA7_CTRL_REG	Control register of DMA channel 7
0x510004F4	DMA7_IDX_REG	Index pointer register of DMA channel 7
0x51000500	DMA_REQ_MUX_REG	DMA channels peripherals mapping register
0x51000504	DMA_INT_STATUS_REG	DMA Interrupt status register
0x51000508	DMA_CLEAR_INT_REG	DMA Interrupt clear register
0x5100050C	DMA_INT_MASK_REG	DMA Interrupt mask register
0x51000510	DMA_SET_INT_MASK_REG	DMA Set Interrupt mask register
0x51000514	DMA_RESET_INT_MASK_REG	DMA Reset Interrupt mask register

Table 398: DMA0_A_START_REG (0x51000400)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA0_A_START	Source start address of channel 0	0x0

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Table 399: DMA0_B_START_REG (0x51000404)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA0_B_START	Destination start address of channel 0	0x0

Table 400: DMA0_INT_REG (0x51000408)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA0_INT	Number of transfers until an interrupt is generated. The interrupt is generated after a transfer, if and only if DMA0_INT_REG has reached DMA0_IDX_REG and before DMA0_IDX_REG is incremented. The interrupt enable bit of this this channel must be already enabled, to let the channel's controller generate the interrupt (see also DMA_INT_MASK_REG and the SET/RESET interrupt registers).	0x0

Table 401: DMA0_LEN_REG (0x5100040C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA0_LEN	DMA channel's transfer length. DMA0_LEN of value 0, 1, 2, ... results into an actual transfer length of 1, 2, 3, ...	0x0

Table 402: DMA0_CTRL_REG (0x51000410)

Bit	Mode	Symbol	Description	Reset
16	R/W	DMA_EXCLUSIVE_ACCESS	0: DMA channel de-asserts the bus request upon completion of the write transfer (burst or single-shot) 1: DMA channel keeps on requesting the bus upon completion of the write. This is effective only in Memory-to-Memory transfers (DREQ_MODE = 0) and results into requesting the bus continuously during the whole transfer, to speed-up its completion (default).	0x1
15	R/W	BUS_ERROR_DETECT	0: Ignores bus error response from the AHB bus, so DMA continues normally. 1: Detects the bus response and tracks any bus error may occur during the transfer. If a bus error is detected, the channel completes the current read-write DMA cycle (either in burst or single transfers mode) and then closes the transfer, de-asserting DMA_ON bit automatically. It is noted that the respective bus error detection status bit of DMA_INT_STATUS_REG is automatically cleared as soon as the channel is switched-on again, to perform a new transfer.	0x1
14:13	R/W	BURST_MODE	Enables the DMA read/write bursts, according to the following configuration: 00 = Bursts are disabled	0x0

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Bit	Mode	Symbol	Description	Reset
			01 = Bursts of 4 are enabled 10 = Bursts of 8 are enabled 11 = Reserved	
12	R/W	REQ_SENSE	0: DMA operates with level-sensitive peripheral requests (default) 1: DMA operates with (positive) edge-sensitive peripheral requests	0x0
11	R/W	DMA_INIT	0: DMA performs copy A1 to B1, A2 to B2, and so on ... 1: DMA performs copy of A1 to B1, B2, and so on ... This feature is useful for memory initialization to any value. Thus, BINC must be set to 1, while AINC is don't care, as only one fetch from A is done. This process cannot be interrupted by other DMA channels. It is also noted that DMA_INIT should not be used when DREQ_MODE=1.	0x0
10	R/W	DMA_IDLE	0: Blocking mode, the DMA performs a fast back-to-back copy, disabling bus access for any bus master with lower priority. 1: Interrupting mode, the DMA inserts a wait cycle after each store allowing the CPU to steal cycles or cache to perform a burst read. If DREQ_MODE=1 or DMA_EXCLUSIVE_ACCESS=1, DMA_IDLE is don't care.	0x0
9:7	R/W	DMA_PRIO	The priority level determines which DMA channel will be granted access for transferring data, in case more than one channels are active and request the bus at the same time. The greater the value, the higher the priority. In specific: 000: lowest priority 111: highest priority If different channels with equal priority level values request the bus at the same time, an inherent priority mechanism is applied. According to this mechanism, if, for example, both the DMA0 and DMA1 channels have the same priority level, then DMA0 will first be granted access to the bus.	0x0
6	R/W	CIRCULAR	0: Normal mode. The DMA channel stops after having completed the transfer of length determined by DMAx_LEN_REG. DMA_ON automatically deasserts when the transfer is completed. 1: Circular mode (applicable only if DREQ_MODE = 1). In this mode, DMA_ON never deasserts, as the DMA channel automatically resets DMAx_IDX_REG and starts a new transfer.	0x0
5	R/W	AINC	Enable increment of source address. 0 = do not increment (source address stays the same during the transfer) 1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	0x0
4	R/W	BINC	Enable increment of destination address.	0x0

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Bit	Mode	Symbol	Description	Reset
			0 = do not increment (destination address stays the same during the transfer) 1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	
3	R/W	DREQ_MODE	0: DMA channel starts immediately 1: DMA channel must be triggered by peripheral DMA request (see also the description of DMA_REQ_MUX_REG)	0x0
2:1	R/W	BW	Bus transfer width: 00 = 1 B (suggested for peripherals like UART and 8-bit SPI) 01 = 2 B (suggested for peripherals like I2C and 16-bit SPI) 10 = 4 B (suggested for Memory-to-Memory transfers) 11 = Reserved	0x0
0	R/W	DMA_ON	0: DMA channel is off, clocks are disabled 1: DMA channel is enabled. This bit will be automatically cleared after the completion of a transfer, if Circular mode is not enabled. In Circular mode, this bit stays set. NOTE: If DMA_ON is disabled by SW while the DMA channel is active, it cannot be enabled again until the channel has completed the last on-going read-write cycle and has stopped. Thus, the SW has to check that the reading of DMA0_CTRL_REG.DMA_ON returns 0, before setting again the specific bit-field.	0x0

Table 403: DMA0_IDX_REG (0x51000414)

Bit	Mode	Symbol	Description	Reset
15:0	R	DMA0_IDX	This (read-only) register determines the data items already transferred by the DMA channel. Hence, if its value is 1, then the DMA channel has already copied one data item and it is currently performing the next copy. If its value is 2, then two items have already been copied, and so on. When the transfer is completed (so when DMA0_CTRL_REG[DMA_ON] has been cleared) and DMA0_CTRL_REG[CIRCULAR] is not set, the register keeps its (last) value (which should be equal to DMA0_LEN_REG) and it is automatically reset to 0 upon starting a new transfer. In Circular mode, the register is automatically initialized to 0 as soon as the DMA channel starts-over again.	0x0

Table 404: DMA1_A_START_REG (0x51000420)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA1_A_START	Source start address of channel 1	0x0

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Table 405: DMA1_B_START_REG (0x51000424)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA1_B_START	Destination start address of channel 1	0x0

Table 406: DMA1_INT_REG (0x51000428)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA1_INT	Number of transfers until an interrupt is generated. The interrupt is generated after a transfer, if and only if DMA1_INT_REG has reached DMA1_IDX_REG and before DMA1_IDX_REG is incremented. The interrupt enable bit of this this channel must be already enabled, to let the channel's controller generate the interrupt (see also DMA_INT_MASK_REG and the SET/RESET interrupt registers).	0x0

Table 407: DMA1_LEN_REG (0x5100042C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA1_LEN	DMA channel's transfer length. DMA1_LEN of value 0, 1, 2, ... results into an actual transfer length of 1, 2, 3, ...	0x0

Table 408: DMA1_CTRL_REG (0x51000430)

Bit	Mode	Symbol	Description	Reset
16	R/W	DMA_EXCLUSIVE_ACCESS	0: DMA channel de-asserts the bus request upon completion of the write transfer (burst or single-shot) 1: DMA channel keeps on requesting the bus upon completion of the write. This is effective only in Memory-to-Memory transfers (DREQ_MODE = 0) and results into requesting the bus continuously during the whole transfer, to speed-up its completion (default).	0x1
15	R/W	BUS_ERROR_DETECT	0: Ignores bus error response from the AHB bus, so DMA continues normally. 1: Detects the bus response and tracks any bus error may occur during the transfer. If a bus error is detected, the channel completes the current read-write DMA cycle (either in burst or single transfers mode) and then closes the transfer, de-asserting DMA_ON bit automatically. It is noted that the respective bus error detection status bit of DMA_INT_STATUS_REG is automatically cleared as soon as the channel is switched-on again, to perform a new transfer.	0x1

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Bit	Mode	Symbol	Description	Reset
14:13	R/W	BURST_MODE	Enables the DMA read/write bursts, according to the following configuration: 00 = Bursts are disabled 01 = Bursts of 4 are enabled 10 = Bursts of 8 are enabled 11 = Reserved	0x0
12	R/W	REQ_SENSE	0: DMA operates with level-sensitive peripheral requests (default) 1: DMA operates with (positive) edge-sensitive peripheral requests	0x0
11	R/W	DMA_INIT	0: DMA performs copy A1 to B1, A2 to B2, and so on ... 1: DMA performs copy of A1 to B1, B2, and so on ... This feature is useful for memory initialization to any value. Thus, BINC must be set to 1, while AINC is don't care, as only one fetch from A is done. This process cannot be interrupted by other DMA channels. It is also noted that DMA_INIT should not be used when DREQ_MODE=1.	0x0
10	R/W	DMA_IDLE	0: Blocking mode, the DMA performs a fast back-to-back copy, disabling bus access for any bus master with lower priority. 1: Interrupting mode, the DMA inserts a wait cycle after each store allowing the CPU to steal cycles or cache to perform a burst read. If DREQ_MODE=1 or DMA_EXCLUSIVE_ACCESS=1, DMA_IDLE is don't care.	0x0
9:7	R/W	DMA_PRIO	The priority level determines which DMA channel will be granted access for transferring data, in case more than one channels are active and request the bus at the same time. The greater the value, the higher the priority. In specific: 000 = lowest priority 111 = highest priority If different channels with equal priority level values request the bus at the same time, an inherent priority mechanism is applied. According to this mechanism, if, for example, both the DMA0 and DMA1 channels have the same priority level, then DMA0 will first be granted access to the bus.	0x0
6	R/W	CIRCULAR	0: Normal mode. The DMA channel stops after having completed the transfer of length determined by DMAx_LEN_REG. DMA_ON automatically deasserts when the transfer is completed. 1: Circular mode (applicable only if DREQ_MODE = 1). In this mode, DMA_ON never deasserts, as the DMA channel automatically resets DMAx_IDX_REG and starts a new transfer.	0x0
5	R/W	AINC	Enable increment of source address. 0 = do not increment (source address stays the same during the transfer)	0x0

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Bit	Mode	Symbol	Description	Reset
			1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	
4	R/W	BINC	Enable increment of destination address. 0 = do not increment (destination address stays the same during the transfer) 1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	0x0
3	R/W	DREQ_MODE	0: DMA channel starts immediately 1: DMA channel must be triggered by peripheral DMA request (see also the description of DMA_REQ_MUX_REG)	0x0
2:1	R/W	BW	Bus transfer width: 00 = 1 B (suggested for peripherals like UART and 8-bit SPI) 01 = 2 B (suggested for peripherals like I2C and 16-bit SPI) 10 = 4 B (suggested for Memory-to-Memory transfers) 11 = Reserved	0x0
0	R/W	DMA_ON	0: DMA channel is off, clocks are disabled 1: DMA channel is enabled. This bit will be automatically cleared after the completion of a transfer, if Circular mode is not enabled. In Circular mode, this bit stays set. NOTE: If DMA_ON is disabled by SW while the DMA channel is active, it cannot be enabled again until the channel has completed the last on-going read-write cycle and has stopped. Thus, the SW has to check that the reading of DMA1_CTRL_REG.DMA_ON returns 0, before setting again the specific bit-field.	0x0

Table 409: DMA1_IDX_REG (0x51000434)

Bit	Mode	Symbol	Description	Reset
15:0	R	DMA1_IDX	This (read-only) register determines the data items already transferred by the DMA channel. Hence, if its value is 1, then the DMA channel has already copied one data item and it is currently performing the next copy. If its value is 2, then two items have already been copied, and so on. When the transfer is completed (so when DMA1_CTRL_REG[DMA_ON] has been cleared) and DMA1_CTRL_REG[CIRCULAR] is not set, the register keeps its (last) value (which should be equal to DMA1_LEN_REG) and it is automatically reset to 0 upon starting a new transfer. In Circular mode, the register is automatically initialized to 0 as soon as the DMA channel starts-over again.	0x0

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Table 410: DMA2_A_START_REG (0x51000440)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA2_A_START	Source start address of channel 2	0x0

Table 411: DMA2_B_START_REG (0x51000444)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA2_B_START	Destination start address of channel 2	0x0

Table 412: DMA2_INT_REG (0x51000448)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA2_INT	Number of transfers until an interrupt is generated. The interrupt is generated after a transfer, if and only if DMA2_INT_REG has reached DMA2_IDX_REG and before DMA2_IDX_REG is incremented. The interrupt enable bit of this this channel must be already enabled, to let the channel's controller generate the interrupt (see also DMA_INT_MASK_REG and the SET/RESET interrupt registers).	0x0

Table 413: DMA2_LEN_REG (0x5100044C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA2_LEN	DMA channel's transfer length. DMA2_LEN of value 0, 1, 2, ... results into an actual transfer length of 1, 2, 3, ...	0x0

Table 414: DMA2_CTRL_REG (0x51000450)

Bit	Mode	Symbol	Description	Reset
16	R/W	DMA_EXCLUSIVE_ACCESS	0: DMA channel de-asserts the bus request upon completion of the write transfer (burst or single-shot) 1: DMA channel keeps on requesting the bus upon completion of the write. This is effective only in Memory-to-Memory transfers (DREQ_MODE = 0) and results into requesting the bus continuously during the whole transfer, to speed-up its completion (default).	0x1
15	R/W	BUS_ERROR_DETECT	0: Ignores bus error response from the AHB bus, so DMA continues normally. 1: Detects the bus response and tracks any bus error may occur during the transfer. If a bus error is detected, the channel completes the current read-write DMA cycle (either in burst or single transfers mode) and then closes the transfer, de-asserting DMA_ON bit automatically.	0x1

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Bit	Mode	Symbol	Description	Reset
			It is noted that the respective bus error detection status bit of DMA_INT_STATUS_REG is automatically cleared as soon as the channel is switched-on again, to perform a new transfer.	
14:13	R/W	BURST_MODE	Enables the DMA read/write bursts, according to the following configuration: 00 = Bursts are disabled 01 = Bursts of 4 are enabled 10 = Bursts of 8 are enabled 11 = Reserved	0x0
12	R/W	REQ_SENSE	0: DMA operates with level-sensitive peripheral requests (default) 1: DMA operates with (positive) edge-sensitive peripheral requests	0x0
11	R/W	DMA_INIT	0: DMA performs copy A1 to B1, A2 to B2, and so on ... 1: DMA performs copy of A1 to B1, B2, and so on ... This feature is useful for memory initialization to any value. Thus, BINC must be set to 1, while AINC is don't care, as only one fetch from A is done. This process cannot be interrupted by other DMA channels. It is also noted that DMA_INIT should not be used when DREQ_MODE=1.	0x0
10	R/W	DMA_IDLE	0: Blocking mode, the DMA performs a fast back-to-back copy, disabling bus access for any bus master with lower priority. 1: Interrupting mode, the DMA inserts a wait cycle after each store allowing the CPU to steal cycles or cache to perform a burst read. If DREQ_MODE=1 or DMA_EXCLUSIVE_ACCESS=1, DMA_IDLE is don't care.	0x0
9:7	R/W	DMA_PRIO	The priority level determines which DMA channel will be granted access for transferring data, in case more than one channels are active and request the bus at the same time. The greater the value, the higher the priority. In specific: 000 = lowest priority 111 = highest priority If different channels with equal priority level values request the bus at the same time, an inherent priority mechanism is applied. According to this mechanism, if, for example, both the DMA0 and DMA1 channels have the same priority level, then DMA0 will first be granted access to the bus.	0x0
6	R/W	CIRCULAR	0: Normal mode. The DMA channel stops after having completed the transfer of length determined by DMAx_LEN_REG. DMA_ON automatically deasserts when the transfer is completed. 1: Circular mode (applicable only if DREQ_MODE = '1'). In this mode, DMA_ON never deasserts, as the DMA channel automatically resets DMAx_IDX_REG and starts a new transfer.	0x0

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Bit	Mode	Symbol	Description	Reset
5	R/W	AINC	Enable increment of destination address. 0 = do not increment (destination address stays the same during the transfer) 1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	0x0
4	R/W	BINC	Enable increment of destination address 0 = do not increment 1 = increment according value of BW	0x0
3	R/W	DREQ_MODE	0: DMA channel starts immediately 1: DMA channel must be triggered by peripheral DMA request (see also the description of DMA_REQ_MUX_REG)	0x0
2:1	R/W	BW	Bus transfer width: 00 = 1 B (suggested for peripherals like UART and 8-bit SPI) 01 = 2 B (suggested for peripherals like I2C and 16-bit SPI) 10 = 4 B (suggested for Memory-to-Memory transfers) 11 = Reserved	0x0
0	R/W	DMA_ON	0: DMA channel is off, clocks are disabled 1: DMA channel is enabled. This bit will be automatically cleared after the completion of a transfer, if Circular mode is not enabled. In Circular mode, this bit stays set. NOTE: If DMA_ON is disabled by SW while the DMA channel is active, it cannot be enabled again until the channel has completed the last on-going read-write cycle and has stopped. Thus, the SW has to check that the reading of DMA2_CTRL_REG.DMA_ON returns 0, before setting again the specific bit-field.	0x0

Table 415: DMA2_IDX_REG (0x51000454)

Bit	Mode	Symbol	Description	Reset
15:0	R	DMA2_IDX	This (read-only) register determines the data items already transferred by the DMA channel. Hence, if its value is 1, then the DMA channel has already copied one data item and it is currently performing the next copy. If its value is 2, then two items have already been copied, and so on. When the transfer is completed (so when DMA2_CTRL_REG[DMA_ON] has been cleared) and DMA2_CTRL_REG[CIRCULAR] is not set, the register keeps its (last) value (which should be equal to DMA2_LEN_REG) and it is automatically reset to 0 upon starting a new transfer. In Circular mode, the register is automatically initialized to 0 as soon as the DMA channel starts-over again.	0x0

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Table 416: DMA3_A_START_REG (0x51000460)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA3_A_START	Source start address of channel 3	0x0

Table 417: DMA3_B_START_REG (0x51000464)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA3_B_START	Destination start address of channel 3	0x0

Table 418: DMA3_INT_REG (0x51000468)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA3_INT	Number of transfers until an interrupt is generated. The interrupt is generated after a transfer, if and only if DMA3_INT_REG has reached DMA3_IDX_REG and before DMA3_IDX_REG is incremented. The interrupt enable bit of this this channel must be already enabled, to let the channel's controller generate the interrupt (see also DMA_INT_MASK_REG and the SET/RESET interrupt registers).	0x0

Table 419: DMA3_LEN_REG (0x5100046C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA3_LEN	DMA channel's transfer length. DMA3_LEN of value 0, 1, 2, ... results into an actual transfer length of 1, 2, 3, ...	0x0

Table 420: DMA3_CTRL_REG (0x51000470)

Bit	Mode	Symbol	Description	Reset
16	R/W	DMA_EXCLUSIVE_ACCESS	0: DMA channel de-asserts the bus request upon completion of the write transfer (burst or single-shot) 1: DMA channel keeps on requesting the bus upon completion of the write. This is effective only in Memory-to-Memory transfers (DREQ_MODE = 0) and results into requesting the bus continuously during the whole transfer, to speed-up its completion (default).	0x1
15	R/W	BUS_ERROR_DETECT	0: Ignores bus error response from the AHB bus, so DMA continues normally. 1: Detects the bus response and tracks any bus error may occur during the transfer. If a bus error is detected, the channel completes the current read-write DMA cycle (either in burst or single transfers mode) and then closes the transfer, de-asserting DMA_ON bit automatically.	0x1

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Bit	Mode	Symbol	Description	Reset
			It is noted that the respective bus error detection status bit of DMA_INT_STATUS_REG is automatically cleared as soon as the channel is switched-on again, to perform a new transfer.	
14:13	R/W	BURST_MODE	Enables the DMA read/write bursts, according to the following configuration: 00 = Bursts are disabled 01 = Bursts of 4 are enabled 10 = Bursts of 8 are enabled 11 = Reserved	0x0
12	R/W	REQ_SENSE	0: DMA operates with level-sensitive peripheral requests (default) 1: DMA operates with (positive) edge-sensitive peripheral requests	0x0
11	R/W	DMA_INIT	0: DMA performs copy A1 to B1, A2 to B2, and so on ... 1: DMA performs copy of A1 to B1, B2, and so on ... This feature is useful for memory initialization to any value. Thus, BINC must be set to 1, while AINC is don't care, as only one fetch from A is done. This process cannot be interrupted by other DMA channels. It is also noted that DMA_INIT should not be used when DREQ_MODE=1.	0x0
10	R/W	DMA_IDLE	0: Blocking mode, the DMA performs a fast back-to-back copy, disabling bus access for any bus master with lower priority. 1: Interrupting mode, the DMA inserts a wait cycle after each store allowing the CPU to steal cycles or cache to perform a burst read. If DREQ_MODE=1 or DMA_EXCLUSIVE_ACCESS=1', DMA_IDLE is don't care.	0x0
9:7	R/W	DMA_PRIO	The priority level determines which DMA channel will be granted access for transferring data, in case more than one channels are active and request the bus at the same time. The greater the value, the higher the priority. In specific: 000 = lowest priority 111 = highest priority If different channels with equal priority level values request the bus at the same time, an inherent priority mechanism is applied. According to this mechanism, if, for example, both the DMA0 and DMA1 channels have the same priority level, then DMA0 will first be granted access to the bus.	0x0
6	R/W	CIRCULAR	0: Normal mode. The DMA channel stops after having completed the transfer of length determined by DMAx_LEN_REG. DMA_ON automatically deasserts when the transfer is completed. 1: Circular mode (applicable only if DREQ_MODE = 1). In this mode, DMA_ON never deasserts, as the DMA channel automatically resets DMAx_IDX_REG and starts a new transfer.	0x0

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Bit	Mode	Symbol	Description	Reset
5	R/W	AINC	Enable increment of source address. 0 = do not increment (source address stays the same during the transfer) 1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	0x0
4	R/W	BINC	Enable increment of destination address. 0 = do not increment (destination address stays the same during the transfer) 1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	0x0
3	R/W	DREQ_MODE	0: DMA channel starts immediately 1: DMA channel must be triggered by peripheral DMA request (see also the description of DMA_REQ_MUX_REG)	0x0
2:1	R/W	BW	Bus transfer width: 00 = 1 Byte (suggested for peripherals like UART and 8-bit SPI) 01 = 2 Bytes (suggested for peripherals like I2C and 16-bit SPI) 10 = 4 Bytes (suggested for Memory-to-Memory transfers) 11 = Reserved	0x0
0	R/W	DMA_ON	0: DMA channel is off, clocks are disabled 1: DMA channel is enabled. This bit will be automatically cleared after the completion of a transfer, if Circular mode is not enabled. In Circular mode, this bit stays set. NOTE: If DMA_ON is disabled by SW while the DMA channel is active, it cannot be enabled again until the channel has completed the last on-going read-write cycle and has stopped. Thus, the SW has to check that the reading of DMA3_CTRL_REG.DMA_ON returns 0, before setting again the specific bit-field.	0x0

Table 421: DMA3_IDX_REG (0x51000474)

Bit	Mode	Symbol	Description	Reset
15:0	R	DMA3_IDX	This (read-only) register determines the data items already transferred by the DMA channel. Hence, if its value is 1, then the DMA channel has already copied one data item and it is currently performing the next copy. If its value is 2, then two items have already been copied, and so on. When the transfer is completed (so when DMA3_CTRL_REG[DMA_ON] has been cleared) and DMA3_CTRL_REG[CIRCULAR] is not set, the register keeps its (last) value (which should be equal to DMA3_LEN_REG) and it is automatically reset to 0 upon starting a new transfer. In Circular mode, the register is automatically initialized to 0 as soon as the DMA channel starts-over again.	0x0

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Table 422: DMA4_A_START_REG (0x51000480)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA4_A_START	Source start address of channel 4	0x0

Table 423: DMA4_B_START_REG (0x51000484)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA4_B_START	Destination start address of channel 4	0x0

Table 424: DMA4_INT_REG (0x51000488)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA4_INT	Number of transfers until an interrupt is generated. The interrupt is generated after a transfer, if and only if DMA4_INT_REG has reached DMA4_IDX_REG and before DMA4_IDX_REG is incremented. The interrupt enable bit of this this channel must be already enabled, to let the channel's controller generate the interrupt (see also DMA_INT_MASK_REG and the SET/RESET interrupt registers).	0x0

Table 425: DMA4_LEN_REG (0x5100048C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA4_LEN	DMA channel's transfer length. DMA4_LEN of value 0, 1, 2, ... results into an actual transfer length of 1, 2, 3, ...	0x0

Table 426: DMA4_CTRL_REG (0x51000490)

Bit	Mode	Symbol	Description	Reset
16	R/W	DMA_EXCLUSIVE_ACCESS	0: DMA channel de-asserts the bus request upon completion of the write transfer (burst or single-shot) 1: DMA channel keeps on requesting the bus upon completion of the write. This is effective only in Memory-to-Memory transfers (DREQ_MODE = 0) and results into requesting the bus continuously during the whole transfer, to speed-up its completion (default).	0x1
15	R/W	BUS_ERROR_DETECT	0: Ignores bus error response from the AHB bus, so DMA continues normally. 1: Detects the bus response and tracks any bus error may occur during the transfer. If a bus error is detected, the channel completes the current read-write DMA cycle (either in burst or single	0x1

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Bit	Mode	Symbol	Description	Reset
			transfers mode) and then closes the transfer, de-asserting DMA_ON bit automatically. It is noted that the respective bus error detection status bit of DMA_INT_STATUS_REG is automatically cleared as soon as the channel is switched-on again, to perform a new transfer.	
14:13	R/W	BURST_MODE	Enables the DMA read/write bursts, according to the following configuration: 00 = Bursts are disabled 01 = Bursts of 4 are enabled 10 = Bursts of 8 are enabled 11 = Reserved	0x0
12	R/W	REQ_SENSE	0: DMA operates with level-sensitive peripheral requests (default) 1: DMA operates with (positive) edge-sensitive peripheral requests	0x0
11	R/W	DMA_INIT	0: DMA performs copy A1 to B1, A2 to B2, and so on ... 1: DMA performs copy of A1 to B1, B2, and so on ... This feature is useful for memory initialization to any value. Thus, BINC must be set to 1, while AINC is don't care, as only one fetch from A is done. This process cannot be interrupted by other DMA channels. It is also noted that DMA_INIT should not be used when DREQ_MODE=1.	0x0
10	R/W	DMA_IDLE	0: Blocking mode, the DMA performs a fast back-to-back copy, disabling bus access for any bus master with lower priority. 1: Interrupting mode, the DMA inserts a wait cycle after each store allowing the CPU to steal cycles or cache to perform a burst read. If DREQ_MODE=1 or DMA_EXCLUSIVE_ACCESS=1, DMA_IDLE is don't care.	0x0
9:7	R/W	DMA_PRIO	The priority level determines which DMA channel will be granted access for transferring data, in case more than one channels are active and request the bus at the same time. The greater the value, the higher the priority. In specific: 000 = lowest priority 111 = highest priority If different channels with equal priority level values request the bus at the same time, an inherent priority mechanism is applied. According to this mechanism, if, for example, both the DMA0 and DMA1 channels have the same priority level, then DMA0 will first be granted access to the bus.	0x0
6	R/W	CIRCULAR	0: Normal mode. The DMA channel stops after having completed the transfer of length determined by DMAx_LEN_REG. DMA_ON automatically deasserts when the transfer is completed. 1: Circular mode (applicable only if DREQ_MODE = 1). In this mode, DMA_ON never deasserts, as	0x0

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Bit	Mode	Symbol	Description	Reset
			the DMA channel automatically resets DMAx_IDX_REG and starts a new transfer.	
5	R/W	AINC	Enable increment of source address. 0 = do not increment (source address stays the same during the transfer) 1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	0x0
4	R/W	BINC	Enable increment of destination address. 0 = do not increment (destination address stays the same during the transfer) 1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	0x0
3	R/W	DREQ_MODE	0: DMA channel starts immediately 1: DMA channel must be triggered by peripheral DMA request (see also the description of DMA_REQ_MUX_REG)	0x0
2:1	R/W	BW	Bus transfer width: 00 = 1 B (suggested for peripherals like UART and 8-bit SPI) 01 = 2 B (suggested for peripherals like I2C and 16-bit SPI) 10 = 4 B (suggested for Memory-to-Memory transfers) 11 = Reserved	0x0
0	R/W	DMA_ON	0: DMA channel is off, clocks are disabled 1: DMA channel is enabled. This bit will be automatically cleared after the completion of a transfer, if Circular mode is not enabled. In Circular mode, this bit stays set. NOTE: If DMA_ON is disabled by SW while the DMA channel is active, it cannot be enabled again until the channel has completed the last on-going read-write cycle and has stopped. Thus, the SW has to check that the reading of DMA4_CTRL_REG.DMA_ON returns 0, before setting again the specific bit-field.	0x0

Table 427: DMA4_IDX_REG (0x51000494)

Bit	Mode	Symbol	Description	Reset
15:0	R	DMA4_IDX	This (read-only) register determines the data items already transferred by the DMA channel. Hence, if its value is 1, then the DMA channel has already copied one data item and it is currently performing the next copy. If its value is 2, then two items have already been copied, and so on. When the transfer is completed (so when DMA4_CTRL_REG[DMA_ON] has been cleared) and DMA4_CTRL_REG[CIRCULAR] is not set, the register keeps its (last) value (which should be equal to DMA4_LEN_REG) and it is automatically reset to 0 upon starting a new transfer. In Circular	0x0

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Bit	Mode	Symbol	Description	Reset
			mode, the register is automatically initialized to 0 as soon as the DMA channel starts-over again.	

Table 428: DMA5_A_START_REG (0x510004A0)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA5_A_START	Source start address of channel 5	0x0

Table 429: DMA5_B_START_REG (0x510004A4)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA5_B_START	Destination start address of channel 5	0x0

Table 430: DMA5_INT_REG (0x510004A8)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA5_INT	Number of transfers until an interrupt is generated. The interrupt is generated after a transfer, if and only if DMA5_INT_REG has reached DMA5_IDX_REG and before DMA5_IDX_REG is incremented. The interrupt enable bit of this this channel must be already enabled, to let the channel's controller generate the interrupt (see also DMA_INT_MASK_REG and the SET/RESET interrupt registers).	0x0

Table 431: DMA5_LEN_REG (0x510004AC)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA5_LEN	DMA channel's transfer length. DMA5_LEN of value 0, 1, 2, ... results into an actual transfer length of 1, 2, 3, ...	0x0

Table 432: DMA5_CTRL_REG (0x510004B0)

Bit	Mode	Symbol	Description	Reset
16	R/W	DMA_EXCLUSIVE_ACCESS	0: DMA channel de-asserts the bus request upon completion of the write transfer (burst or single-shot) 1: DMA channel keeps on requesting the bus upon completion of the write. This is effective only in Memory-to-Memory transfers (DREQ_MODE = 0) and results into requesting the bus continuously during the whole transfer, to speed-up its completion (default).	0x1
15	R/W	BUS_ERROR_DETECT	0: Ignores bus error response from the AHB bus, so DMA continues normally.	0x1

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Bit	Mode	Symbol	Description	Reset
			1: Detects the bus response and tracks any bus error may occur during the transfer. If a bus error is detected, the channel completes the current read-write DMA cycle (either in burst or single transfers mode) and then closes the transfer, de-asserting DMA_ON bit automatically. It is noted that the respective bus error detection status bit of DMA_INT_STATUS_REG is automatically cleared as soon as the channel is switched-on again, to perform a new transfer.	
14:13	R/W	BURST_MODE	Enables the DMA read/write bursts, according to the following configuration: 00 = Bursts are disabled 01 = Bursts of 4 are enabled 10 = Bursts of 8 are enabled 11 = Reserved	0x0
12	R/W	REQ_SENSE	0: DMA operates with level-sensitive peripheral requests (default) 1: DMA operates with (positive) edge-sensitive peripheral requests	0x0
11	R/W	DMA_INIT	0: DMA performs copy A1 to B1, A2 to B2, and so on ... 1: DMA performs copy of A1 to B1, B2, and so on ... This feature is useful for memory initialization to any value. Thus, BINC must be set to 1, while AINC is don't care, as only one fetch from A is done. This process cannot be interrupted by other DMA channels. It is also noted that DMA_INIT should not be used when DREQ_MODE=1.	0x0
10	R/W	DMA_IDLE	0: Blocking mode, the DMA performs a fast back-to-back copy, disabling bus access for any bus master with lower priority. 1: Interrupting mode, the DMA inserts a wait cycle after each store allowing the CPU to steal cycles or cache to perform a burst read. If DREQ_MODE=1 or DMA_EXCLUSIVE_ACCESS=1, DMA_IDLE is don't care.	0x0
9:7	R/W	DMA_PRIO	The priority level determines which DMA channel will be granted access for transferring data, in case more than one channels are active and request the bus at the same time. The greater the value, the higher the priority. In specific: 000 = lowest priority 111 = highest priority If different channels with equal priority level values request the bus at the same time, an inherent priority mechanism is applied. According to this mechanism, if, for example, both the DMA0 and DMA1 channels have the same priority level, then DMA0 will first be granted access to the bus.	0x0
6	R/W	CIRCULAR	0: Normal mode. The DMA channel stops after having completed the transfer of length determined by DMAx_LEN_REG. DMA_ON	0x0

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Bit	Mode	Symbol	Description	Reset
			automatically deasserts when the transfer is completed. 1: Circular mode (applicable only if DREQ_MODE = 1). In this mode, DMA_ON never deasserts, as the DMA channel automatically resets DMAx_IDX_REG and starts a new transfer.	
5	R/W	AINC	Enable increment of source address. 0 = do not increment (source address stays the same during the transfer) 1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	0x0
4	R/W	BINC	Enable increment of destination address. 0 = do not increment (destination address stays the same during the transfer) 1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	0x0
3	R/W	DREQ_MODE	0: DMA channel starts immediately 1: DMA channel must be triggered by peripheral DMA request (see also the description of DMA_REQ_MUX_REG)	0x0
2:1	R/W	BW	Bus transfer width: 00 = 1 B (suggested for peripherals like UART and 8-bit SPI) 01 = 2 B (suggested for peripherals like I2C and 16-bit SPI) 10 = 4 B (suggested for Memory-to-Memory transfers) 11 = Reserved	0x0
0	R/W	DMA_ON	0: DMA channel is off, clocks are disabled 1: DMA channel is enabled. This bit will be automatically cleared after the completion of a transfer, if Circular mode is not enabled. In Circular mode, this bit stays set. NOTE: If DMA_ON is disabled by SW while the DMA channel is active, it cannot be enabled again until the channel has completed the last on-going read-write cycle and has stopped. Thus, the SW has to check that the reading of DMA5_CTRL_REG.DMA_ON returns 0, before setting again the specific bit-field.	0x0

Table 433: DMA5_IDX_REG (0x510004B4)

Bit	Mode	Symbol	Description	Reset
15:0	R	DMA5_IDX	This (read-only) register determines the data items already transferred by the DMA channel. Hence, if its value is 1, then the DMA channel has already copied one data item and it is currently performing the next copy. If its value is 2, then two items have already been copied, and so on.	0x0

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Bit	Mode	Symbol	Description	Reset
			When the transfer is completed (so when DMA5_CTRL_REG[DMA_ON] has been cleared) and DMA5_CTRL_REG[CIRCULAR] is not set, the register keeps its (last) value (which should be equal to DMA5_LEN_REG) and it is automatically reset to 0 upon starting a new transfer. In Circular mode, the register is automatically initialized to 0 as soon as the DMA channel starts-over again.	

Table 434: DMA6_A_START_REG (0x510004C0)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA6_A_START	Source start address of channel 6	0x0

Table 435: DMA6_B_START_REG (0x510004C4)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA6_B_START	Destination start address of channel 6	0x0

Table 436: DMA6_INT_REG (0x510004C8)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA6_INT	Number of transfers until an interrupt is generated. The interrupt is generated after a transfer, if and only if DMA6_INT_REG has reached DMA6_IDX_REG and before DMA6_IDX_REG is incremented. The interrupt enable bit of this this channel must be already enabled, to let the channel's controller generate the interrupt (see also DMA_INT_MASK_REG and the SET/RESET interrupt registers).	0x0

Table 437: DMA6_LEN_REG (0x510004CC)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA6_LEN	DMA channel's transfer length. DMA6_LEN of value 0, 1, 2, ... results into an actual transfer length of 1, 2, 3, ...	0x0

Table 438: DMA6_CTRL_REG (0x510004D0)

Bit	Mode	Symbol	Description	Reset
16	R/W	DMA_EXCLUSIVE_ACCESS	0: DMA channel de-asserts the bus request upon completion of the write transfer (burst or single-shot) 1: DMA channel keeps on requesting the bus upon completion of the write. This is effective only in Memory-to-Memory transfers (DREQ_MODE =	0x1

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Bit	Mode	Symbol	Description	Reset
			0) and results into requesting the bus continuously during the whole transfer, to speed-up its completion (default).	
15	R/W	BUS_ERROR_DETECT	0: Ignores bus error response from the AHB bus, so DMA continues normally. 1: Detects the bus response and tracks any bus error may occur during the transfer. If a bus error is detected, the channel completes the current read-write DMA cycle (either in burst or single transfers mode) and then closes the transfer, de-asserting DMA_ON bit automatically. It is noted that the respective bus error detection status bit of DMA_INT_STATUS_REG is automatically cleared as soon as the channel is switched-on again, to perform a new transfer.	0x1
14:13	R/W	BURST_MODE	Enables the DMA read/write bursts, according to the following configuration: 00 = Bursts are disabled 01 = Bursts of 4 are enabled 10 = Bursts of 8 are enabled 11 = Reserved	0x0
12	R/W	REQ_SENSE	0: DMA operates with level-sensitive peripheral requests (default) 1: DMA operates with (positive) edge-sensitive peripheral requests	0x0
11	R/W	DMA_INIT	0: DMA performs copy A1 to B1, A2 to B2, and so on ... 1: DMA performs copy of A1 to B1, B2, and so on ... This feature is useful for memory initialization to any value. Thus, BINC must be set to 1, while AINC is don't care, as only one fetch from A is done. This process cannot be interrupted by other DMA channels. It is also noted that DMA_INIT should not be used when DREQ_MODE=1.	0x0
10	R/W	DMA_IDLE	0: Blocking mode, the DMA performs a fast back-to-back copy, disabling bus access for any bus master with lower priority. 1: Interrupting mode, the DMA inserts a wait cycle after each store allowing the CPU to steal cycles or cache to perform a burst read. If DREQ_MODE=1 or DMA_EXCLUSIVE_ACCESS=1, DMA_IDLE is don't care.	0x0
9:7	R/W	DMA_PRIO	The priority level determines which DMA channel will be granted access for transferring data, in case more than one channels are active and request the bus at the same time. The greater the value, the higher the priority. In specific: 000 = lowest priority 111 = highest priority If different channels with equal priority level values request the bus at the same time, an inherent priority mechanism is applied. According to this mechanism, if, for example, both the DMA0 and	0x0

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Bit	Mode	Symbol	Description	Reset
			DMA1 channels have the same priority level, then DMA0 will first be granted access to the bus.	
6	R/W	CIRCULAR	0: Normal mode. The DMA channel stops after having completed the transfer of length determined by DMAx_LEN_REG. DMA_ON automatically deasserts when the transfer is completed. 1: Circular mode (applicable only if DREQ_MODE = 1). In this mode, DMA_ON never deasserts, as the DMA channel automatically resets DMAx_IDX_REG and starts a new transfer.	0x0
5	R/W	AINC	Enable increment of source address. 0 = do not increment (source address stays the same during the transfer) 1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	0x0
4	R/W	BINC	Enable increment of destination address. 0 = do not increment (destination address stays the same during the transfer) 1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	0x0
3	R/W	DREQ_MODE	0: DMA channel starts immediately 1: DMA channel must be triggered by peripheral DMA request (see also the description of DMA_REQ_MUX_REG)	0x0
2:1	R/W	BW	Bus transfer width: 00 = 1 B (suggested for peripherals like UART and 8-bit SPI) 01 = 2 B (suggested for peripherals like I2C and 16-bit SPI) 10 = 4 B (suggested for Memory-to-Memory transfers) 11 = Reserved	0x0
0	R/W	DMA_ON	0: DMA channel is off, clocks are disabled 1: DMA channel is enabled. This bit will be automatically cleared after the completion of a transfer, if Circular mode is not enabled. In Circular mode, this bit stays set. NOTE: If DMA_ON is disabled by SW while the DMA channel is active, it cannot be enabled again until the channel has completed the last on-going read-write cycle and has stopped. Thus, the SW has to check that the reading of DMA6_CTRL_REG.DMA_ON returns 0, before setting again the specific bit-field.	0x0

Table 439: DMA6_IDX_REG (0x510004D4)

Bit	Mode	Symbol	Description	Reset
15:0	R	DMA6_IDX	This (read-only) register determines the data items already transferred by the DMA channel. Hence, if	0x0

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Bit	Mode	Symbol	Description	Reset
			its value is 1, then the DMA channel has already copied one data item and it is currently performing the next copy. If its value is 2, then two items have already been copied, and so on. When the transfer is completed (so when DMA6_CTRL_REG[DMA_ON] has been cleared) and DMA6_CTRL_REG[CIRCULAR] is not set, the register keeps its (last) value (which should be equal to DMA6_LEN_REG) and it is automatically reset to 0 upon starting a new transfer. In Circular mode, the register is automatically initialized to 0 as soon as the DMA channel starts-over again.	

Table 440: DMA7_A_START_REG (0x510004E0)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA7_A_START	Source start address of channel 7	0x0

Table 441: DMA7_B_START_REG (0x510004E4)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DMA7_B_START	Destination start address of channel 7	0x0

Table 442: DMA7_INT_REG (0x510004E8)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA7_INT	Number of transfers until an interrupt is generated. The interrupt is generated after a transfer, if and only if DMA7_INT_REG has reached DMA7_IDX_REG and before DMA7_IDX_REG is incremented. The interrupt enable bit of this this channel must be already enabled, to let the channel's controller generate the interrupt (see also DMA_INT_MASK_REG and the SET/RESET interrupt registers).	0x0

Table 443: DMA7_LEN_REG (0x510004EC)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DMA7_LEN	DMA channel's transfer length. DMA7_LEN of value 0, 1, 2, ... results into an actual transfer length of 1, 2, 3, ...	0x0

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Table 444: DMA7_CTRL_REG (0x510004F0)

Bit	Mode	Symbol	Description	Reset
16	R/W	DMA_EXCLUSIVE_ACCESS	0: DMA channel de-asserts the bus request upon completion of the write transfer (burst or single-shot) 1: DMA channel keeps on requesting the bus upon completion of the write. This is effective only in Memory-to-Memory transfers (DREQ_MODE = 0) and results into requesting the bus continuously during the whole transfer, to speed-up its completion (default).	0x1
15	R/W	BUS_ERROR_DETECT	0: Ignores bus error response from the AHB bus, so DMA continues normally. 1: Detects the bus response and tracks any bus error may occur during the transfer. If a bus error is detected, the channel completes the current read-write DMA cycle (either in burst or single transfers mode) and then closes the transfer, de-asserting DMA_ON bit automatically. It is noted that the respective bus error detection status bit of DMA_INT_STATUS_REG is automatically cleared as soon as the channel is switched-on again, to perform a new transfer. NOTE: This bit-field is overruled to 1 when channel 5 is configured as trusted channel (in Secure Boot mode).	0x1
14:13	R/W	BURST_MODE	Enables the DMA read/write bursts, according to the following configuration: 00 = Bursts are disabled 01 = Bursts of 4 are enabled 10 = Bursts of 8 are enabled 11 = Reserved	0x0
12	R/W	REQ_SENSE	0: DMA operates with level-sensitive peripheral requests (default) 1: DMA operates with (positive) edge-sensitive peripheral requests	0x0
11	R/W	DMA_INIT	0: DMA performs copy A1 to B1, A2 to B2, and so on ... 1: DMA performs copy of A1 to B1, B2, and so on ... This feature is useful for memory initialization to any value. Thus, BINC must be set to 1, while AINC is don't care, as only one fetch from A is done. This process cannot be interrupted by other DMA channels. It is also noted that DMA_INIT should not be used when DREQ_MODE=1. NOTE: This bit-field is overruled to 0 when channel 5 is configured as trusted channel (in Secure Boot mode).	0x0
10	R/W	DMA_IDLE	0: Blocking mode, the DMA performs a fast back-to-back copy, disabling bus access for any bus master with lower priority. 1: Interrupting mode, the DMA inserts a wait cycle after each store allowing the CPU to steal cycles or cache to perform a burst read.	0x0

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Bit	Mode	Symbol	Description	Reset
			If DREQ_MODE=1 or DMA_EXCLUSIVE_ACCESS=1, DMA_IDLE is don't care. NOTE: This bit-field is overruled to 0 when the DMA channel 7 is configured as trusted channel (in Secure Boot mode).	
9:7	R/W	DMA_PRIO	The priority level determines which DMA channel will be granted access for transferring data, in case more than one channels are active and request the bus at the same time. The greater the value, the higher the priority. In specific: 000 = lowest priority 111 = highest priority If different channels with equal priority level values request the bus at the same time, an inherent priority mechanism is applied. According to this mechanism, if, for example, both the DMA0 and DMA1 channels have the same priority level, then DMA0 will first be granted access to the bus.	0x0
6	R/W	CIRCULAR	0: Normal mode. The DMA channel stops after having completed the transfer of length determined by DMAx_LEN_REG. DMA_ON automatically deasserts when the transfer is completed. 1: Circular mode (applicable only if DREQ_MODE = 1). In this mode, DMA_ON never deasserts, as the DMA channel automatically resets DMAx_IDX_REG and starts a new transfer.	0x0
5	R/W	AINC	Enable increment of source address. 0 = do not increment (source address stays the same during the transfer) 1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	0x0
4	R/W	BINC	Enable increment of destination address. 0 = do not increment (destination address stays the same during the transfer) 1 = increment according to the value of BW bit-field (by 1, when BW="00" ; by 2, when BW="01" ; by 4, when BW="10")	0x0
3	R/W	DREQ_MODE	0: DMA channel starts immediately 1: DMA channel must be triggered by peripheral DMA request (see also the description of DMA_REQ_MUX_REG) NOTE: This bit-field is overruled to 0 when channel 5 is configured as trusted channel (in Secure Boot mode).	0x0
2:1	R/W	BW	Bus transfer width: 00 = 1 Byte (suggested for peripherals like UART and 8-bit SPI) 01 = 2 Bytes (suggested for peripherals like I2C and 16-bit SPI) 10 = 4 Bytes (suggested for Memory-to-Memory transfers) 11 = Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
0	R/W	DMA_ON	0: DMA channel is off, clocks are disabled 1: DMA channel is enabled. This bit will be automatically cleared after the completion of a transfer, if Circular mode is not enabled. In Circular mode, this bit stays set. NOTE: If DMA_ON is disabled by SW while the DMA channel is active, it cannot be enabled again until the channel has completed the last on-going read-write cycle and has stopped. Thus, the SW has to check that the reading of DMA7_CTRL_REG.DMA_ON returns 0, before setting again the specific bit-field.	0x0

Table 445: DMA7_IDX_REG (0x510004F4)

Bit	Mode	Symbol	Description	Reset
15:0	R	DMA7_IDX	This (read-only) register determines the data items already transferred by the DMA channel. Hence, if its value is 1, then the DMA channel has already copied one data item and it is currently performing the next copy. If its value is 2, then two items have already been copied, and so on. When the transfer is completed (so when DMA7_CTRL_REG[DMA_ON] has been cleared) and DMA7_CTRL_REG[CIRCULAR] is not set, the register keeps its (last) value (which should be equal to DMA7_LEN_REG) and it is automatically reset to 0 upon starting a new transfer. In Circular mode, the register is automatically initialized to 0 as soon as the DMA channel starts-over again.	0x0

Table 446: DMA_REQ_MUX_REG (0x51000500)

Bit	Mode	Symbol	Description	Reset
15:12	R/W	DMA67_SEL	Select which combination of peripherals are mapped on the DMA channels. The peripherals are mapped as pairs on two channels. The first DMA request is mapped on channel 6 and the second on channel 7. See the description of DMA01_SEL bit-field for the exact peripherals' mapping. NOTE: When channel DMA7 is configured as secure channel, it cannot support any peripheral requests, since DREQ_MODE is disabled automatically, overruling the corresponding bit-field of DMA7_CTRL_REG.	0xF
11:8	R/W	DMA45_SEL	Select which combination of peripherals are mapped on the DMA channels. The peripherals are mapped as pairs on two channels. The first DMA request is mapped on channel 4 and the second on channel 5. See the description of DMA01_SEL bit-field for the exact peripherals' mapping.	0xF

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Bit	Mode	Symbol	Description	Reset
7:4	R/W	DMA23_SEL	Select which combination of peripherals are mapped on the DMA channels. The peripherals are mapped as pairs on two channels. The first DMA request is mapped on channel 2 and the second on channel 3. See the description of DMA01_SEL bit-field for the exact peripherals' mapping.	0xF
3:0	R/W	DMA01_SEL	Select which combination of peripherals are mapped on the DMA channels. The peripherals are mapped as pairs on two channels. The first DMA request is mapped on channel 0 and the second on channel 1 and the peripherals supported are listed below. Note that in the following list, the "rx" implies a Peripheral-to-Memory transfer and the "tx" a Memory-to-Peripheral transfer. 0x0: SPI_rx / SPI_tx 0x1: SP2_rx / SPI2_tx 0x2: UART_rx / UART_tx 0x3: UART2_rx / UART2_tx 0x4: I2C_rx / I2C_tx 0x5: I2C2_rx / I2C2_tx 0x6: USB_rx / USB_tx 0x7: UART3_rx / UART3_tx 0x8: PCM / PCM 0x9: SRC_rx / SRC_tx 0xA: SPI3_rx / SPI3_tx 0xB: I2C3_rx / I2C3_tx 0xC: GP_ADC / APP_ADC 0xD: SRC2_rx / SRC2_tx 0xE: I3C_rx / I3C_tx 0xF: None NOTE: If any of the two available peripheral selector fields (DMA01_SEL, DMA23_SEL) have the same value, the lesser significant selector has higher priority and will control the DMA acknowledge signal driven to the selected peripheral. Hence, if DMA01_SEL = DMA23_SEL, the channels 0 and 1 will provide the Rx and Tx DMA acknowledge signals for the selected peripheral. Consequently, it is suggested to assign the intended peripheral value to a unique selector field. Exception is the SRC, for which the mapping of the same peripheral option to more than one channel pairs may be intended (for example, for stereo mode).	0xF

Table 447: DMA_INT_STATUS_REG (0x51000504)

Bit	Mode	Symbol	Description	Reset
15	R	DMA_BUS_ERR7	0: No bus error response is detected for channel 7	0x0

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Bit	Mode	Symbol	Description	Reset
			1: Bus error response detected for channel 7 NOTE: This bit-field is auto-clear and it is initialized to 0 as soon as a new transfer is started. It is also noted that when channel 7 is configured as "trusted" (in Secure Boot mode), this bit-field is overruled to 0, masking the bus error status reported to the user.	
14	R	DMA_BUS_ERR6	0: No bus error response is detected for channel 6 1: Bus error response detected for channel 6	0x0
13	R	DMA_BUS_ERR5	0: No bus error response is detected for channel 5 1: Bus error response detected for channel 5	0x0
12	R	DMA_BUS_ERR4	0: No bus error response is detected for channel 4 1: Bus error response detected for channel 4 NOTE: This bit-field is auto-clear and it is initialized to 0 as soon as a new transfer is started.	0x0
11	R	DMA_BUS_ERR3	0: No bus error response is detected for channel 3 1: Bus error response detected for channel 3 NOTE: This bit-field is auto-clear and it is initialized to 0 as soon as a new transfer is started.	0x0
10	R	DMA_BUS_ERR2	0: No bus error response is detected for channel 2 1: Bus error response detected for channel 2 NOTE: This bit-field is auto-clear and it is initialized to 0 as soon as a new transfer is started.	0x0
9	R	DMA_BUS_ERR1	0: No bus error response is detected for channel 1 1: Bus error response detected for channel 1 NOTE: This bit-field is auto-clear and it is initialized to 0 as soon as a new transfer is started.	0x0
8	R	DMA_BUS_ERR0	0: No bus error response is detected for channel 0 1: Bus error response detected for channel 0 NOTE: This bit-field is auto-clear and it is initialized to 0 as soon as a new transfer is started.	0x0
7	R	DMA_IRQ_CH7	0: IRQ on channel 7 is not set 1: IRQ on channel 7 is set	0x0
6	R	DMA_IRQ_CH6	0: IRQ on channel 6 is not set 1: IRQ on channel 6 is set	0x0
5	R	DMA_IRQ_CH5	0: IRQ on channel 5 is not set 1: IRQ on channel 5 is set	0x0
4	R	DMA_IRQ_CH4	0: IRQ on channel 4 is not set 1: IRQ on channel 4 is set	0x0
3	R	DMA_IRQ_CH3	0: IRQ on channel 3 is not set 1: IRQ on channel 3 is set	0x0
2	R	DMA_IRQ_CH2	0: IRQ on channel 2 is not set 1: IRQ on channel 2 is set	0x0
1	R	DMA_IRQ_CH1	0: IRQ on channel 1 is not set 1: IRQ on channel 1 is set	0x0
0	R	DMA_IRQ_CH0	0: IRQ on channel 0 is not set 1: IRQ on channel 0 is set	0x0

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Table 448: DMA_CLEAR_INT_REG (0x51000508)

Bit	Mode	Symbol	Description	Reset
7	R0/W	DMA_RST_IRQ_CH 7	Writing a 1 will reset the status bit of DMA_INT_STATUS_REG for channel 7 ; writing a 0 will have no effect	0x0
6	R0/W	DMA_RST_IRQ_CH 6	Writing a 1 will reset the status bit of DMA_INT_STATUS_REG for channel 6 ; writing a 0 will have no effect	0x0
5	R0/W	DMA_RST_IRQ_CH 5	Writing a 1 will reset the status bit of DMA_INT_STATUS_REG for channel 5 ; writing a 0 will have no effect	0x0
4	R0/W	DMA_RST_IRQ_CH 4	Writing a 1 will reset the status bit of DMA_INT_STATUS_REG for channel 4 ; writing a 0 will have no effect	0x0
3	R0/W	DMA_RST_IRQ_CH 3	Writing a 1 will reset the status bit of DMA_INT_STATUS_REG for channel 3 ; writing a 0 will have no effect	0x0
2	R0/W	DMA_RST_IRQ_CH 2	Writing a 1 will reset the status bit of DMA_INT_STATUS_REG for channel 2 ; writing a 0 will have no effect	0x0
1	R0/W	DMA_RST_IRQ_CH 1	Writing a 1 will reset the status bit of DMA_INT_STATUS_REG for channel 1 ; writing a 0 will have no effect	0x0
0	R0/W	DMA_RST_IRQ_CH 0	Writing a 1 will reset the status bit of DMA_INT_STATUS_REG for channel 0 ; writing a 0 will have no effect	0x0

Table 449: DMA_INT_MASK_REG (0x5100050C)

Bit	Mode	Symbol	Description	Reset
7	R/W	DMA_IRQ_ENABLE 7	0: disable interrupts on channel 7 1: enable interrupts on channel 7	0x0
6	R/W	DMA_IRQ_ENABLE 6	0: disable interrupts on channel 6 1: enable interrupts on channel 6	0x0
5	R/W	DMA_IRQ_ENABLE 5	0: disable interrupts on channel 5 1: enable interrupts on channel 5	0x0
4	R/W	DMA_IRQ_ENABLE 4	0: disable interrupts on channel 4 1: enable interrupts on channel 4	0x0
3	R/W	DMA_IRQ_ENABLE 3	0: disable interrupts on channel 3 1: enable interrupts on channel 3	0x0
2	R/W	DMA_IRQ_ENABLE 2	0: disable interrupts on channel 2 1: enable interrupts on channel 2	0x0
1	R/W	DMA_IRQ_ENABLE 1	0: disable interrupts on channel 1 1: enable interrupts on channel 1	0x0
0	R/W	DMA_IRQ_ENABLE 0	0: disable interrupts on channel 0 1: enable interrupts on channel 0	0x0

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Table 450: DMA_SET_INT_MASK_REG (0x51000510)

Bit	Mode	Symbol	Description	Reset
7	RWS	DMA_SET_IRQ_ENABLE7	Writing a 1 will enable the IRQs in the DMA channel 7, writing a 0 has no effect. Reading returns always 0.	0x0
6	RWS	DMA_SET_IRQ_ENABLE6	Writing a 1 will enable the IRQs in the DMA channel 6, writing a 0 has no effect. Reading returns always 0.	0x0
5	RWS	DMA_SET_IRQ_ENABLE5	Writing a 1 will enable the IRQs in the DMA channel 5, writing a 0 has no effect. Reading returns always 0.	0x0
4	RWS	DMA_SET_IRQ_ENABLE4	Writing a 1 will enable the IRQs in the DMA channel 4, writing a 0 has no effect. Reading returns always 0.	0x0
3	RWS	DMA_SET_IRQ_ENABLE3	Writing a 1 will enable the IRQs in the DMA channel 3, writing a 0 has no effect. Reading returns always 0.	0x0
2	RWS	DMA_SET_IRQ_ENABLE2	Writing a 1 will enable the IRQs in the DMA channel 2, writing a 0 has no effect. Reading returns always 0.	0x0
1	RWS	DMA_SET_IRQ_ENABLE1	Writing a 1 will enable the IRQs in the DMA channel 1, writing a 0 has no effect. Reading returns always 0.	0x0
0	RWS	DMA_SET_IRQ_ENABLE0	Writing a 1 will enable the IRQs in the DMA channel 0, writing a 0 has no effect. Reading returns always 0.	0x0

Table 451: DMA_RESET_INT_MASK_REG (0x51000514)

Bit	Mode	Symbol	Description	Reset
7	RWS	DMA_RESET_IRQ_ENABLE7	Writing a 1 will disable the IRQs in the DMA channel 7, writing a 0 has no effect. Reading returns always 0.	0x0
6	RWS	DMA_RESET_IRQ_ENABLE6	Writing a 1 will disable the IRQs in the DMA channel 6, writing a 0 has no effect. Reading returns always 0.	0x0
5	RWS	DMA_RESET_IRQ_ENABLE5	Writing a 1 will disable the IRQs in the DMA channel 5, writing a 0 has no effect. Reading returns always 0.	0x0
4	RWS	DMA_RESET_IRQ_ENABLE4	Writing a 1 will disable the IRQs in the DMA channel 4, writing a 0 has no effect. Reading returns always 0.	0x0
3	RWS	DMA_RESET_IRQ_ENABLE3	Writing a 1 will disable the IRQs in the DMA channel 3, writing a 0 has no effect. Reading returns always 0.	0x0
2	RWS	DMA_RESET_IRQ_ENABLE2	Writing a 1 will disable the IRQs in the DMA channel 2, writing a 0 has no effect. Reading returns always 0.	0x0

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Bit	Mode	Symbol	Description	Reset
1	RWS	DMA_RESET_IRQ_ENABLE1	Writing a 1 will disable the IRQs in the DMA channel 1, writing a 0 has no effect. Reading returns always 0.	0x0
0	RWS	DMA_RESET_IRQ_ENABLE0	Writing a 1 will disable the IRQs in the DMA channel 0, writing a 0 has no effect. Reading returns always 0.	0x0

44.11 General Purpose ADC and Application ADC Registers

Table 452: Register map GPADC

Address	Register	Description
0x50020800	GP_ADC_CTRL_REG	General Purpose ADC Control Register
0x50020804	GP_ADC_CTRL2_REG	General Purpose ADC Second Control Register
0x50020808	GP_ADC_CTRL3_REG	General Purpose ADC Third Control Register
0x5002080C	GP_ADC_SEL_REG	General Purpose ADC Input Selection Register
0x50020810	GP_ADC_OFFP_REG	General Purpose ADC Positive Offset Register
0x50020814	GP_ADC_OFFN_REG	General Purpose ADC Negative Offset Register
0x50020818	GP_ADC_TRIM_REG	General Purpose ADC Trim Register
0x5002081C	GP_ADC_CLEAR_INT_REG	General Purpose ADC Clear Interrupt Register
0x50020820	GP_ADC_RESULT_REG	General Purpose ADC Result Register
0x50040500	SDADC_CTRL_REG	Sigma Delta ADC Control Register
0x50040504	SDADC_PGA_CTRL_REG	Sigma Delta ADC PGA Control Registers
0x5004050C	SDADC_CLEAR_INT_REG	Sigma Delta ADC Clear Interrupt Register
0x50040510	SDADC_RESULT_REG	Sigma Delta ADC Result Register
0x50040514	SDADC_AUDIO_FILT_REG	Sigma Delta ADC Audio Filter Register

Table 453: GP_ADC_CTRL_REG (0x50020800)

Bit	Mode	Symbol	Description	Reset
16:15	R/W	GP_ADC_RESULT_MODE	Sample mode 0: Sample extention, the result is aligned on the MSBs. The lowest calculated LSB is extended over the unused bits. 1: Sample truncation, the result is aligned on the 8 LSBs. Any additional accurancy isn't available. 2: Normal mode, the result is aligned on the MSBs. Any unused LSBs are kept zero.	0x2

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Bit	Mode	Symbol	Description	Reset
			3: N.A.	
14	R/W	GP_ADC_DIE_TEMP_EN	Enables the die-temperature sensor. Output can be measured on GPADC input 4.	0x0
13:12	R/W	GP_ADC_DIFF_TEMP_SEL	0= Gnd, 1 =sensor near radio, 2 =sensor near charger, 3 =sensor near bandgap with sensors disabled (GP_ADC_DIFF_TEMP_EN = 0) :0 = GND 1 = Z, 2= V(ntc) from charger, 3 = V(temp) from charger	0x0
11	R/W	GP_ADC_DIFF_TEMP_EN	1: Enable the on-chip temperature sensors	0x0
10	R/W	GP_ADC_LDO_HOLD	0: GPADC LDO tracking bandgap reference 1: GPADC LDO hold sampled bandgap reference	0x0
9	R/W	GP_ADC_CHOP	0: Chopper mode off 1: Chopper mode enabled. Takes two samples with opposite GP_ADC_SIGN to cancel the internal offset voltage of the ADC; Highly recommended for DC-measurements.	0x0
8	R/W	GP_ADC_SIGN	0: Default 1: Conversion with opposite sign at input and output to cancel out the internal offset of the ADC and low-frequency	0x0
7	R/W	GP_ADC_MUTE	0: Normal operation 1: Mute ADC input. Takes sample at mid-scale (to dertermine the internal offset and/or noise of the ADC with regards to VDD_REF which is also sampled by the ADC).	0x0
6	R/W	GP_ADC_SE	0: Differential mode 1: Single ended mode	0x0
5	R/W	GP_ADC_MINT	0: Disable (mask) GP_ADC_INT. 1: Enable GP_ADC_INT to ICU.	0x0
4	R	GP_ADC_INT	1: AD conversion ready and has generated an interrupt. Must be cleared by writing any value to GP_ADC_CLEAR_INT_REG.	0x0
3	R/W	GP_ADC_DMA_EN	0: DMA functionality disabled 1: DMA functionality enabled	0x0
2	R/W	GP_ADC_CONT	0: Manual ADC mode, a single result will be generated after setting the GP_ADC_START bit. 1: Continuous ADC mode, new ADC results will be constantly stored in GP_ADC_RESULT_REG. Still GP_ADC_START has to be set to start the execution. The time between conversions is configurable with GP_ADC_INTERVAL.	0x0
1	R/W	GP_ADC_START	0: ADC conversion ready. 1: If a 1 is written, the ADC starts a conversion. After the conversion this bit will be set to 0 and the GP_ADC_INT bit will be set. It is not allowed to write this bit while it is not (yet) zero.	0x0
0	R/W	GP_ADC_EN	0: LDO is off and ADC is disabled.. 1: LDO is turned on and afterwards the ADC is enabled.	0x0

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Table 454: GP_ADC_CTRL2_REG (0x50020804)

Bit	Mode	Symbol	Description	Reset
15:13	R/W	GP_ADC_STORE_DEL	0: Data is stored after handshake synchronisation 1-3: Reserved 4: Data is stored 5 ADC_CLK cycles after internal start trigger 7: Data is stored 8 ADC_CLK cycles after internal start trigger	0x0
12:9	R/W	GP_ADC_SMPL_TIME	0: The sample time (switch is closed) is two ADC_CLK cycles 1: The sample time is 1*8 ADC_CLK cycles 2: The sample time is 2*8 ADC_CLK cycles 15: The sample time is 15*8 ADC_CLK cycles	0x1
8:6	R/W	GP_ADC_CONV_NRS	0: 1 sample is taken or 2 in case ADC_CHOP is active. 1: 2 samples are taken. 2: 4 samples are taken. 7: 128 samples are taken.	0x0
5:3	R/W	-	Reserved	0x0
2	R/W	GP_ADC_I20U	1: Adds 20 µA constant load current at the ADC LDO to minimize ripple on the reference voltage of the ADC.	0x0
1:0	R/W	GP_ADC_ATTN	0: No attenuator (input voltages up to 0.9 V allowed) 1: Enabling 2x attenuator (input voltages up to 1.8 V allowed) 2: Enabling 3x attenuator (input voltages up to 2.7 V allowed) 3: Enabling 4x attenuator (input voltages up to 3.6 V allowed) Enabling the attenuator requires a longer sampling time.	0x0

Table 455: GP_ADC_CTRL3_REG (0x50020808)

Bit	Mode	Symbol	Description	Reset
15:8	R/W	GP_ADC_INTERVAL	Defines the interval between two ADC conversions in case GP_ADC_CONT is set. 0: No extra delay between two conversions. 1: 1.024 ms interval between two conversions. 2: 2.048 ms interval between two conversions. 255: 261.12 ms interval between two conversions.	0x0
7:0	R/W	GP_ADC_EN_DEL	Defines the delay for enabling the ADC after enabling the LDO. 0: Not allowed 1: 4x ADC_CLK period. n: n*4x ADC_CLK period.	0x40

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Table 456: GP_ADC_SEL_REG (0x5002080C)

Bit	Mode	Symbol	Description	Reset
16:14	R/W	-	Reserved	0x0
13:11	R/W	GP_ADC_SEL_MUX2	0: No rail selected 1: V12 2: V18 3: V14 4: V18P 5: VSYS monitor 6: VBUS monitor 7: VBAT monitor	0x0
10:8	R/W	GP_ADC_SEL_MUX1	0: No rail selected 1: NC 2: Reserved 3: I_sense_bus 4: Reserved 5: V30 6: Reserved 7: V18F	0x0
7	R/W	-	Reserved	0x0
6:4	R/W	GP_ADC_SEL_P	ADC positive input selection. 0: ADC0 (P0[5]) 1: ADC1 (P0[6]) 2: ADC2 (P0[27]) 3: ADC3 (P0[30]) 4: MUX1 5: Diff temp 6: MUX2 7: Die temp	0x0
3	R/W	-	Reserved	0x0
2:0	R/W	GP_ADC_SEL_N	ADC negative input selection. Differential only (GP_ADC_SE=0). 0: ADC0 (P0[5]) 1: ADC1 (P0[6]) 2: ADC2 (P0[27]) 3: ADC3 (P0[30]) All other combinations are reserved.	0x0

Table 457: GP_ADC_OFFP_REG (0x50020810)

Bit	Mode	Symbol	Description	Reset
9:0	R/W	GP_ADC_OFFP	Offset adjust of "positive" array of ADC-network (effective if "GP_ADC_SE=0", or "GP_ADC_SE=1 AND GP_ADC_SIGN=0 OR GP_ADC_CHOP=1")	0x200

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Table 458: GP_ADC_OFFN_REG (0x50020814)

Bit	Mode	Symbol	Description	Reset
9:0	R/W	GP_ADC_OFFN	Offset adjust of "negative" array of ADC-network (effective if "GP_ADC_SE=0", or "GP_ADC_SE=1 AND GP_ADC_SIGN=1 OR GP_ADC_CHOP=1")	0x200

Table 459: GP_ADC_TRIM_REG (0x50020818)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	GP_ADC_LDO_LEVEL	GPADC LDO level -4: -24 mV -3: -18 mV -2: -12 mV -1: -6 mV 0: 0 (default) 1: +6 mV 2: +12 mV 3: +18 mV	0x0

Table 460: GP_ADC_CLEAR_INT_REG (0x5002081C)

Bit	Mode	Symbol	Description	Reset
15:0	R0/W	GP_ADC_CLR_INT	Writing any value to this register will clear the ADC_INT interrupt. Reading returns 0.	0x0

Table 461: GP_ADC_RESULT_REG (0x50020820)

Bit	Mode	Symbol	Description	Reset
15:0	R	GP_ADC_VAL	Returns the 10 up to 16 bits linear value of the last AD conversion. The upper 10 bits are always valid, the lower 6 bits are only valid in case oversampling has been applied. Two samples results in one extra bit and 64 samples results in six extra bits.	0x0

Table 462: SDADC_CTRL_REG (0x50040500)

Bit	Mode	Symbol	Description	Reset
20	R/W	-	Reserved	0x0
19	R/W	-	Reserved	0x0
18	R/W	SDADC_DMA_EN	0: DMA functionality disabled 1: DMA functionality enabled	0x0
17	R/W	SDADC_MINT	0: Disable (mask) SDADC_ADC_INT. 1: Enable SDADC_ADC_INT to ICU.	0x0

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Bit	Mode	Symbol	Description	Reset
16	R	SDADC_INT	1: AD conversion ready and has generated an interrupt. Must be cleared by writing any value to SDADC_CLEAR_INT_REG.	0x0
15	R	SDADC_LDO_OK	1: Internal LDO is ready for use	0x0
14:13	R/W	-	Reserved	0x0
12	R/W	SDADC_AUDIO_FILTER_EN	0: Disable audio filter, ADC is forced into reset. When setting to 0 while SDADC_START = 1, the last sample is completed first before disabling. 1: Enable the audio filter, this bit needs to be set before the SDADC_START bit is set to 1.	0x0
11:10	R/W	SDADC_RESULT_MODE	Sample mode 0: Sample extention, SDADC_RESULT_REG = {sample[15:2], sample[2], sample[2]} 1: Sample truncation, SDADC_RESULT_REG = {0x00, sample[15:8]} 2: Normal mode, SDADC_RESULT_REG = sample[15:0] 3: N.A.	0x2
9	R/W	-	Reserved	0x0
8:6	R/W	-	Reserved	0x0
5:2	R/W	-	Reserved	0x0
1	R/W	SDADC_START	0: ADC idle 1: Start ADC	0x0
0	R/W	SDADC_EN	0: LDO is off and ADC is disabled. 1: LDO, bias currents and modulator are enabled.	0x0

Table 463: SDADC_PGA_CTRL_REG (0x50040504)

Bit	Mode	Symbol	Description	Reset
11:9	R/W	PGA_GAIN	select the PGA gain select: 0 : -12 dB 1 : -6 dB 2 : 0 dB 3 : 6 dB 4 : 12 dB 5 : 18 dB 6 : 24 dB 7 : 30 dB	0x0
8:7	R/W	PGA_MODE	Use PGA in single ended mode 0 : Differential mode (default) 1 : Use N-branch as single ended mode 2 : Differential mode 3 : Use P-branch as single ended mode	0x0
6	R/W	PGA_MUTE	Mute the PGA output 0 : Unmuted (default) 1 : Mute	0x0

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Bit	Mode	Symbol	Description	Reset
5:3	R/W	PGA_BIAS	Configure the PGA bias control: 0: 0.40 x Ibias 1: 0.44 x Ibias 2: 0.50 x Ibias 3: 0.57 x Ibias 4: 0.66 x Ibias 5: 0.80 x Ibias 6: 1.00 x Ibias 7: 1.33 x Ibias	0x4
2	R/W	PGA_SHORTIN	PGA input short 0 : Normal mode (default) 1 : Short PGA inputs	0x0
1:0	R/W	PGA_EN	PGA enable: 00: both branches of PGA disabled 01: Positive branch of PGA enabled, Negative branch disabled 10: Positive branch of PGA disabled, Negative branch enabled 11: Both branches of PGA enabled	0x0

Table 464: SDADC_CLEAR_INT_REG (0x5004050C)

Bit	Mode	Symbol	Description	Reset
31:0	R0/W	SDADC_CLR_INT	Writing any value to this register will clear the ADC_INT interrupt. Reading returns 0.	0x0

Table 465: SDADC_RESULT_REG (0x50040510)

Bit	Mode	Symbol	Description	Reset
15:0	R	SDADC_VAL	Returns 16 bits linear value of the last AD conversion.	0x0

Table 466: SDADC_AUDIO_FILT_REG (0x50040514)

Bit	Mode	Symbol	Description	Reset
20:0	R/W	SDADC_CIC_OFFSET	Constant CIC offset	0x0

44.12 General Purpose I/O Registers

Table 467: Register map GPIO

Address	Register	Description
0x50050100	P0_DATA_REG	P0 Data input / output Register

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Address	Register	Description
0x50050104	P1_DATA_REG	P1 Data input / output Register
0x50050108	P2_DATA_REG	P2 Data input / output Register
0x5005010C	P0_SET_DATA_REG	P0 Set port pins Register
0x50050110	P1_SET_DATA_REG	P1 Set port pins Register
0x50050114	P2_SET_DATA_REG	P1 Set port pins Register
0x50050118	P0_RESET_DATA_REG	P0 Reset port pins Register
0x5005011C	P1_RESET_DATA_REG	P1 Reset port pins Register
0x50050120	P2_RESET_DATA_REG	P0 Reset port pins Register
0x50050124	P0_00_MODE_REG	P0_00 Mode Register
0x50050128	P0_01_MODE_REG	P0_01 Mode Register
0x5005012C	P0_02_MODE_REG	P0_02 Mode Register
0x50050130	P0_03_MODE_REG	P0_03 Mode Register
0x50050134	P0_04_MODE_REG	P0_04 Mode Register
0x50050138	P0_05_MODE_REG	P0_05 Mode Register
0x5005013C	P0_06_MODE_REG	P0_06 Mode Register
0x50050140	P0_07_MODE_REG	P0_07 Mode Register
0x50050144	P0_08_MODE_REG	P0_08 Mode Register
0x50050148	P0_09_MODE_REG	P0_09 Mode Register
0x5005014C	P0_10_MODE_REG	P0_10 Mode Register
0x50050150	P0_11_MODE_REG	P0_11 Mode Register
0x50050154	P0_12_MODE_REG	P0_12 Mode Register
0x50050158	P0_13_MODE_REG	P0_13 Mode Register
0x5005015C	P0_14_MODE_REG	P0_14 Mode Register
0x50050160	P0_15_MODE_REG	P0_15 Mode Register
0x50050164	P0_16_MODE_REG	P0_16 Mode Register
0x50050168	P0_17_MODE_REG	P0_17 Mode Register
0x5005016C	P0_18_MODE_REG	P0_18 Mode Register
0x50050170	P0_19_MODE_REG	P0_19 Mode Register
0x50050174	P0_20_MODE_REG	P0_20 Mode Register
0x50050178	P0_21_MODE_REG	P0_21 Mode Register
0x5005017C	P0_22_MODE_REG	P0_22 Mode Register
0x50050180	P0_23_MODE_REG	P0_23 Mode Register
0x50050184	P0_24_MODE_REG	P0_24 Mode Register
0x50050188	P0_25_MODE_REG	P0_25 Mode Register
0x5005018C	P0_26_MODE_REG	P0_26 Mode Register
0x50050190	P0_27_MODE_REG	P0_27 Mode Register
0x50050194	P0_28_MODE_REG	P0_28 Mode Register

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Address	Register	Description
0x50050198	P0_29_MODE_REG	P0_29 Mode Register
0x5005019C	P0_30_MODE_REG	P0_30 Mode Register
0x500501A0	P0_31_MODE_REG	P0_31 Mode Register
0x500501A4	P1_00_MODE_REG	P1_00 Mode Register
0x500501A8	P1_01_MODE_REG	P1_01 Mode Register
0x500501AC	P1_02_MODE_REG	P1_02 Mode Register
0x500501B0	P1_03_MODE_REG	P1_03 Mode Register
0x500501B4	P1_04_MODE_REG	P1_04 Mode Register
0x500501B8	P1_05_MODE_REG	P1_05 Mode Register
0x500501BC	P1_06_MODE_REG	P1_06 Mode Register
0x500501C0	P1_07_MODE_REG	P1_07 Mode Register
0x500501C4	P1_08_MODE_REG	P1_08 Mode Register
0x500501C8	P1_09_MODE_REG	P1_09 Mode Register
0x500501CC	P1_10_MODE_REG	P1_10 Mode Register
0x500501D0	P1_11_MODE_REG	P1_11 Mode Register
0x500501D4	P1_12_MODE_REG	P1_12 Mode Register
0x500501D8	P1_13_MODE_REG	P1_13 Mode Register
0x500501DC	P1_14_MODE_REG	P1_14 Mode Register
0x500501E0	P1_15_MODE_REG	P1_15 Mode Register
0x500501E4	P1_16_MODE_REG	P1_16 Mode Register
0x500501E8	P1_17_MODE_REG	P1_17 Mode Register
0x500501EC	P1_18_MODE_REG	P1_18 Mode Register
0x500501F0	P1_19_MODE_REG	P1_19 Mode Register
0x500501F4	P1_20_MODE_REG	P1_20 Mode Register
0x500501F8	P1_21_MODE_REG	P1_21 Mode Register
0x500501FC	P1_22_MODE_REG	P1_22 Mode Register
0x50050200	P1_23_MODE_REG	P1_23 Mode Register
0x50050204	P1_24_MODE_REG	P1_24 Mode Register
0x50050208	P1_25_MODE_REG	P1_25 Mode Register
0x5005020C	P1_26_MODE_REG	P1_26 Mode Register
0x50050210	P1_27_MODE_REG	P1_27 Mode Register
0x50050214	P1_28_MODE_REG	P1_28 Mode Register
0x50050218	P1_29_MODE_REG	P1_29 Mode Register
0x5005021C	P1_30_MODE_REG	P1_30 Mode Register
0x50050220	P1_31_MODE_REG	P1_31 Mode Register
0x50050224	P2_00_MODE_REG	P2_00 Mode Register
0x50050228	P2_01_MODE_REG	P2_01 Mode Register
0x5005022C	P2_02_MODE_REG	P2_02 Mode Register
0x50050230	P2_03_MODE_REG	P2_03 Mode Register

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Address	Register	Description
0x50050234	P2_04_MODE_REG	P2_04 Mode Register
0x50050238	P2_05_MODE_REG	P2_05 Mode Register
0x5005023C	P2_06_MODE_REG	P2_06 Mode Register
0x50050240	P2_07_MODE_REG	P2_07 Mode Register
0x50050244	P2_08_MODE_REG	P2_08 Mode Register
0x50050248	P2_09_MODE_REG	P2_09 Mode Register
0x5005024C	P2_10_MODE_REG	P2_10 Mode Register
0x50050250	P2_11_MODE_REG	P2_11 Mode Register
0x50050254	P2_12_MODE_REG	P2_12 Mode Register
0x50050258	P2_13_MODE_REG	P2_13 Mode Register
0x5005025C	P2_14_MODE_REG	P2_14 Mode Register
0x50050260	P0_PADPWR_CTRL_REG	P0 Output Power Control Register
0x50050264	P1_PADPWR_CTRL_REG	P1 Output Power Control Register
0x50050268	P2_PADPWR_CTRL_REG	P2 Output Power Control Register
0x5005026C	GPIO_CLK_SEL_REG	Select which clock to map on ports P0/P1
0x50050270	P0_WEAK_CTRL_REG	P0 Weak Pads Control Register
0x50050274	P1_WEAK_CTRL_REG	P1 Weak Pads Control Register
0x50050278	P2_WEAK_CTRL_REG	P2 Weak Pads Control Register
0x5005027C	LCDC_MAP_CTRL_REG	LCDC mapping control Register
0x50050280	PAD_DRIVE_CTRL_REG	Pad drive control for SPI3/eMMC

Table 468: P0_DATA_REG (0x50050100)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	P0_DATA	Set P0 output register when written; Returns the value of P0 port when read	0x3015

Table 469: P1_DATA_REG (0x50050104)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	P1_DATA	Set P1 output register when written; Returns the value of P1 port when read	0x23000000

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Table 470: P2_DATA_REG (0x50050108)

Bit	Mode	Symbol	Description	Reset
14:0	R/W	P2_DATA	Set P2 output register when written; Returns the value of P2 port when read	0x6000

Table 471: P0_SET_DATA_REG (0x5005010C)

Bit	Mode	Symbol	Description	Reset
31:0	R0/W	P0_SET	Writing a 1 to P0[y] sets P0[y] to 1. Writing 0 is discarded; Reading returns 0	0x0

Table 472: P1_SET_DATA_REG (0x50050110)

Bit	Mode	Symbol	Description	Reset
31:0	R0/W	P1_SET	Writing a 1 to P1[y] sets P1[y] to 1. Writing 0 is discarded; Reading returns 0	0x0

Table 473: P2_SET_DATA_REG (0x50050114)

Bit	Mode	Symbol	Description	Reset
14:0	R0/W	P2_SET	Writing a 1 to P2[y] sets P2[y] to 1. Writing 0 is discarded; Reading returns 0	0x0

Table 474: P0_RESET_DATA_REG (0x50050118)

Bit	Mode	Symbol	Description	Reset
31:0	R0/W	P0_RESET	Writing a 1 to P0[y] sets P0[y] to 0. Writing 0 is discarded; Reading returns 0	0x0

Table 475: P1_RESET_DATA_REG (0x5005011C)

Bit	Mode	Symbol	Description	Reset
31:0	R0/W	P1_RESET	Writing a 1 to P1[y] sets P1[y] to 0. Writing 0 is discarded; Reading returns 0	0x0

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Table 476: P2_RESET_DATA_REG (0x50050120)

Bit	Mode	Symbol	Description	Reset
14:0	R0/W	P2_RESET	Writing a 1 to P2[y] sets P2[y] to 0. Writing 0 is discarded; Reading returns 0	0x0

Table 477: P0_00_MODE_REG (0x50050124)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x1
7:6	R	-	Reserved	0x0
5:0	R/W	PID	Function of port: 0: GPIO 1: UART_RX 2: UART_TX 3: UART2_RX 4: UART2_TX 5: UART2_CTSN 6: UART2_RTSN 7: UART3_RX 8: UART3_TX 9: UART3_CTSN / ISO_RST 10: UART3_RTSN / ISO_CARDINSERT 11: ISO_CLK 12: ISO_DATA 13: SPI_DI 14: SPI_DO 15: SPI_CLK 16: SPI_EN 17: SPI_EN2 18: SPI2_DI 19: SPI2_DO 20: SPI2_CLK 21: SPI2_EN 22: SPI2_EN2 23: SPI3_EN 24: SPI3_EN2 25: I2C_SCL 26: I2C_SDA 27: I2C2_SCL 28: I2C2_SDA 29: I2C3_SCL 30: I2C3_SDA	0x0

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Bit	Mode	Symbol	Description	Reset
			31: I3C_SCL 32: I3C_SDA 33: USB_SOF 34: ADC (Analog) 35: USB (P2_10 and P2_11) 36: PCM_DI 37: PCM_DO 38: PCM_FSC 39: PCM_CLK 40: PDM_DATA 41: PDM_CLK 42: COEX_EXT_ACT 43: COEX_SMART_ACT 44: COEX_SMART_PRI 45: PORT0_DCF 46: PORT1_DCF 47: PORT2_DCF 48: PORT3_DCF 49: PORT4_DCF 50: CLOCK (see also GPIO_CLK_SEL_REG for the dedicated pins mapping of supported clocks) 51: TIM_PWM 52: TIM2_PWM 53: TIM3_PWM 54: TIM4_PWM 55: TIM5_PWM 56: TIM6_PWM 57: TIM_1SHOT 58: TIM2_1SHOT 59: TIM3_1SHOT 60: TIM4_1SHOT 61: TIM5_1SHOT 62: TIM6_1SHOT 63: CMAC_DIAG (Dedicated Pins)	

Table 478: P0_01_MODE_REG (0x50050128)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

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Table 479: P0_02_MODE_REG (0x5005012C)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x1
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 480: P0_03_MODE_REG (0x50050130)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 481: P0_04_MODE_REG (0x50050134)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x1
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 482: P0_05_MODE_REG (0x50050138)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected	0x2

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Bit	Mode	Symbol	Description	Reset
			11 = Output, no resistors selected In ADC mode, these bits are don't care	
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 483: P0_06_MODE_REG (0x5005013C)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 484: P0_07_MODE_REG (0x50050140)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 485: P0_08_MODE_REG (0x50050144)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

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Table 486: P0_09_MODE_REG (0x50050148)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 487: P0_10_MODE_REG (0x5005014C)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 488: P0_11_MODE_REG (0x50050150)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 489: P0_12_MODE_REG (0x50050154)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0

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Bit	Mode	Symbol	Description	Reset
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x1
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 490: P0_13_MODE_REG (0x50050158)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x1
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 491: P0_14_MODE_REG (0x5005015C)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 492: P0_15_MODE_REG (0x50050160)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected	0x2

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Bit	Mode	Symbol	Description	Reset
			In ADC mode, these bits are don't care.	
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 493: P0_16_MODE_REG (0x50050164)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 494: P0_17_MODE_REG (0x50050168)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 495: P0_18_MODE_REG (0x5005016C)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

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Table 496: P0_19_MODE_REG (0x50050170)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 497: P0_20_MODE_REG (0x50050174)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 498: P0_21_MODE_REG (0x50050178)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 499: P0_22_MODE_REG (0x5005017C)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull	0x0

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Bit	Mode	Symbol	Description	Reset
			1: Open drain	
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 500: P0_23_MODE_REG (0x50050180)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 501: P0_24_MODE_REG (0x50050184)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 502: P0_25_MODE_REG (0x50050188)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected	0x2

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Bit	Mode	Symbol	Description	Reset
			11 = Output, no resistors selected In ADC mode, these bits are don't care.	
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 503: P0_26_MODE_REG (0x5005018C)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 504: P0_27_MODE_REG (0x50050190)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 505: P0_28_MODE_REG (0x50050194)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 506: P0_29_MODE_REG (0x50050198)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 507: P0_30_MODE_REG (0x5005019C)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 508: P0_31_MODE_REG (0x500501A0)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

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Table 509: P1_00_MODE_REG (0x500501A4)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 510: P1_01_MODE_REG (0x500501A8)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 511: P1_02_MODE_REG (0x500501AC)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 512: P1_03_MODE_REG (0x500501B0)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected	0x2

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Bit	Mode	Symbol	Description	Reset
			11 = Output, no resistors selected In ADC mode, these bits are don't care	
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 513: P1_04_MODE_REG (0x500501B4)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 514: P1_05_MODE_REG (0x500501B8)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 515: P1_06_MODE_REG (0x500501BC)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

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Table 516: P1_07_MODE_REG (0x500501C0)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 517: P1_08_MODE_REG (0x500501C4)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 518: P1_09_MODE_REG (0x500501C8)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 519: P1_10_MODE_REG (0x500501CC)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected	0x2

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Bit	Mode	Symbol	Description	Reset
			01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 520: P1_11_MODE_REG (0x500501D0)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 521: P1_12_MODE_REG (0x500501D4)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 522: P1_13_MODE_REG (0x500501D8)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2

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Bit	Mode	Symbol	Description	Reset
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 523: P1_14_MODE_REG (0x500501DC)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 524: P1_15_MODE_REG (0x500501E0)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 525: P1_16_MODE_REG (0x500501E4)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

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Table 526: P1_17_MODE_REG (0x500501E8)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 527: P1_18_MODE_REG (0x500501EC)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 528: P1_19_MODE_REG (0x500501F0)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 529: P1_20_MODE_REG (0x500501F4)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0

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Bit	Mode	Symbol	Description	Reset
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 530: P1_21_MODE_REG (0x500501F8)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 531: P1_22_MODE_REG (0x500501FC)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 532: P1_23_MODE_REG (0x50050200)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected	0x2

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Bit	Mode	Symbol	Description	Reset
			In ADC mode, these bits are don't care.	
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 533: P1_24_MODE_REG (0x50050204)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x1
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 534: P1_25_MODE_REG (0x50050208)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x1
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 535: P1_26_MODE_REG (0x5005020C)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

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Table 536: P1_27_MODE_REG (0x50050210)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 537: P1_28_MODE_REG (0x50050214)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 538: P1_29_MODE_REG (0x50050218)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x1
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 539: P1_30_MODE_REG (0x5005021C)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull	0x0

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Bit	Mode	Symbol	Description	Reset
			1: Open drain	
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 540: P1_31_MODE_REG (0x50050220)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 541: P2_00_MODE_REG (0x50050224)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 542: P2_01_MODE_REG (0x50050228)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected	0x2

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Bit	Mode	Symbol	Description	Reset
			11 = Output, no resistors selected In ADC mode, these bits are don't care.	
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 543: P2_02_MODE_REG (0x5005022C)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 544: P2_03_MODE_REG (0x50050230)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 545: P2_04_MODE_REG (0x50050234)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 546: P2_05_MODE_REG (0x50050238)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 547: P2_06_MODE_REG (0x5005023C)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 548: P2_07_MODE_REG (0x50050240)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

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Table 549: P2_08_MODE_REG (0x50050244)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 550: P2_09_MODE_REG (0x50050248)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 551: P2_10_MODE_REG (0x5005024C)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 552: P2_11_MODE_REG (0x50050250)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0

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Bit	Mode	Symbol	Description	Reset
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 553: P2_12_MODE_REG (0x50050254)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x2
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 554: P2_13_MODE_REG (0x50050258)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care.	0x1
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 555: P2_14_MODE_REG (0x5005025C)

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected	0x1

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Bit	Mode	Symbol	Description	Reset
			In ADC mode, these bits are don't care.	
7:6	R	-	Reserved	0x0
5:0	R/W	PID	See P0_00_MODE_REG[PID]	0x0

Table 556: P0_PADPWR_CTRL_REG (0x50050260)

Bit	Mode	Symbol	Description	Reset
31	R/W	P0_31_OUT_CTRL	0 = P0_31 port output is powered by the V30 rail (default) 1 = P0_31 port output is powered by the 1V8P rail Bit 31 controls the power supply of P0_31.	0x0
30	R/W	P0_30_OUT_CTRL	0 = P0_30 port output is powered by the V30 rail (default) 1 = P0_30 port output is powered by the 1V8P rail Bit 30 controls the power supply of P0_30.	0x0
29	R/W	P0_29_OUT_CTRL	0 = P0_29 port output is powered by the V30 rail (default) 1 = P0_29 port output is powered by the 1V8P rail Bit 29 controls the power supply of P0_29.	0x0
28	R/W	P0_28_OUT_CTRL	0 = P0_28 port output is powered by the V30 rail (default) 1 = P0_28 port output is powered by the 1V8P rail Bit 28 controls the power supply of P0_28.	0x0
27	R/W	P0_27_OUT_CTRL	0 = P0_27 port output is powered by the V30 rail (default) 1 = P0_27 port output is powered by the 1V8P rail Bit 27 controls the power supply of P0_27.	0x0
26	R/W	-	Reserved	0x0
25	R/W	-	Reserved	0x0
24	R/W	P0_24_OUT_CTRL	0 = P0_24 port output is powered by the V30 rail (default) 1 = P0_24 port output is powered by the 1V8P rail Bit 24 controls the power supply of P0_24.	0x0
23	R/W	P0_23_OUT_CTRL	0 = P0_23 port output is powered by the V30 rail (default) 1 = P0_23 port output is powered by the 1V8P rail Bit 23 controls the power supply of P0_23.	0x0
22	R/W	P0_22_OUT_CTRL	0 = P0_22 port output is powered by the V30 rail (default) 1 = P0_22 port output is powered by the 1V8P rail Bit 22 controls the power supply of P0_22.	0x0
21	R/W	P0_21_OUT_CTRL	0 = P0_21 port output is powered by the V30 rail (default) 1 = P0_21 port output is powered by the 1V8P rail Bit 21 controls the power supply of P0_21.	0x0
20	R/W	P0_20_OUT_CTRL	0 = P0_20 port output is powered by the V30 rail (default)	0x0

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Bit	Mode	Symbol	Description	Reset
			1 = P0_20 port output is powered by the 1V8P rail Bit 20 controls the power supply of P0_20.	
19	R/W	P0_19_OUT_CTRL	0 = P0_19 port output is powered by the V30 rail (default) 1 = P0_19 port output is powered by the 1V8P rail Bit 19 controls the power supply of P0_19.	0x0
18	R/W	P0_18_OUT_CTRL	0 = P0_18 port output is powered by the V30 rail (default) 1 = P0_18 port output is powered by the 1V8P rail Bit 18 controls the power supply of P0_18.	0x0
17	R/W	P0_17_OUT_CTRL	0 = P0_17 port output is powered by the V30 rail (default) 1 = P0_17 port output is powered by the 1V8P rail Bit 17 controls the power supply of P0_17.	0x0
16	R/W	P0_16_OUT_CTRL	0 = P0_16 port output is powered by the V30 rail (default) 1 = P0_16 port output is powered by the 1V8P rail Bit 16 controls the power supply of P0_16.	0x0
15	R/W	P0_15_OUT_CTRL	0 = P0_15 port output is powered by the V30 rail (default) 1 = P0_15 port output is powered by the 1V8P rail Bit 15 controls the power supply of P0_15.	0x0
14	R/W	P0_14_OUT_CTRL	0 = P0_14 port output is powered by the V30 rail (default) 1 = P0_14 port output is powered by the 1V8P rail Bit 14 controls the power supply of P0_14.	0x0
13	R/W	-	Reserved	0x0
12	R/W	-	Reserved	0x0
11	R/W	P0_11_OUT_CTRL	0 = P0_11 port output is powered by the V30 rail (default) 1 = P0_11 port output is powered by the 1V8P rail Bit 11 controls the power supply of P0_11.	0x0
10	R/W	P0_10_OUT_CTRL	0 = P0_10 port output is powered by the V30 rail (default) 1 = P0_10 port output is powered by the 1V8P rail Bit 10 controls the power supply of P0_10.	0x0
9	R/W	P0_09_OUT_CTRL	0 = P0_09 port output is powered by the V30 rail (default) 1 = P0_09 port output is powered by the 1V8P rail Bit 9 controls the power supply of P0_09.	0x0
8	R/W	P0_08_OUT_CTRL	0 = P0_08 port output is powered by the V30 rail (default) 1 = P0_08 port output is powered by the 1V8P rail Bit 8 controls the power supply of P0_08.	0x0
7	R/W	P0_07_OUT_CTRL	0 = P0_07 port output is powered by the V30 rail (default) 1 = P0_07 port output is powered by the 1V8P rail Bit 7 controls the power supply of P0_07.	0x0

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Bit	Mode	Symbol	Description	Reset
6	R/W	P0_06_OUT_CTRL	0 = P0_06 port output is powered by the V30 rail (default) 1 = P0_06 port output is powered by the 1V8P rail Bit 6 controls the power supply of P0_06.	0x0
5	R/W	P0_05_OUT_CTRL	0 = P0_05 port output is powered by the V30 rail (default) 1 = P0_05 port output is powered by the 1V8P rail Bit 5 controls the power supply of P0_05.	0x0
4	R/W	P0_04_OUT_CTRL	0 = P0_04 port output is powered by the V30 rail (default) 1 = P0_04 port output is powered by the 1V8P rail Bit 4 controls the power supply of P0_04.	0x0
3	R/W	P0_03_OUT_CTRL	0 = P0_03 port output is powered by the V30 rail (default) 1 = P0_03 port output is powered by the 1V8P rail Bit 3 controls the power supply of P0_03.	0x0
2	R/W	P0_02_OUT_CTRL	0 = P0_02 port output is powered by the V30 rail (default) 1 = P0_02 port output is powered by the 1V8P rail Bit 2 controls the power supply of P0_02.	0x0
1	R/W	P0_01_OUT_CTRL	0 = P0_01 port output is powered by the V30 rail (default) 1 = P0_01 port output is powered by the 1V8P rail Bit 1 controls the power supply of P0_01.	0x0
0	R/W	P0_00_OUT_CTRL	0 = P0_00 port output is powered by the V30 rail (default) 1 = P0_00 port output is powered by the 1V8P rail Bit 0 controls the power supply of P0_00.	0x0

Table 557: P1_PADPWR_CTRL_REG (0x50050264)

Bit	Mode	Symbol	Description	Reset
31	R/W	P1_31_OUT_CTRL	0 = P1_31 port output is powered by the V30 rail (default) 1 = P1_31 port output is powered by the 1V8P rail Bit 31 controls the power supply of P1_31.	0x0
30	R/W	P1_30_OUT_CTRL	0 = P1_30 port output is powered by the V30 rail (default) 1 = P1_30 port output is powered by the 1V8P rail Bit 30 controls the power supply of P1_30.	0x0
29	R/W	-	Reserved	0x0
28	R/W	-	Reserved	0x0
27	R/W	-	Reserved	0x0
26	R/W	-	Reserved	0x0
25	R/W	-	Reserved	0x0
24	R/W	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
23	R/W	P1_23_OUT_CTRL	0 = P1_23 port output is powered by the V30 rail (default) 1 = P1_23 port output is powered by the 1V8P rail Bit 23 controls the power supply of P1_23.	0x0
22	R/W	P1_22_OUT_CTRL	0 = P1_22 port output is powered by the V30 rail (default) 1 = P1_22 port output is powered by the 1V8P rail Bit 30 controls the power supply of P1_22.	0x0
21	R/W	-	Reserved	0x0
20	R/W	-	Reserved	0x0
19	R/W	-	Reserved	0x0
18	R/W	-	Reserved	0x0
17	R/W	-	Reserved	0x0
16	R/W	-	Reserved	0x0
15	R/W	-	Reserved	0x0
14	R/W	-	Reserved	0x0
13	R/W	-	Reserved	0x0
12	R/W	P1_12_OUT_CTRL	0 = P1_12 port output is powered by the V30 rail (default) 1 = P1_12 port output is powered by the 1V8P rail Bit 12 controls the power supply of P1_12.	0x0
11	R/W	P1_11_OUT_CTRL	0 = P1_11 port output is powered by the V30 rail (default) 1 = P1_11 port output is powered by the 1V8P rail Bit 11 controls the power supply of P1_11.	0x0
10	R/W	-	Reserved	0x0
9	R/W	-	Reserved	0x0
8	R/W	-	Reserved	0x0
7	R/W	P1_07_OUT_CTRL	0 = P1_07 port output is powered by the V30 rail (default) 1 = P1_07 port output is powered by the 1V8P rail Bit 7 controls the power supply of P1_07.	0x0
6	R/W	P1_06_OUT_CTRL	0 = P1_06 port output is powered by the V30 rail (default) 1 = P1_06 port output is powered by the 1V8P rail Bit 6 controls the power supply of P1_06.	0x0
5	R/W	P1_05_OUT_CTRL	0 = P1_05 port output is powered by the V30 rail (default) 1 = P1_05 port output is powered by the 1V8P rail Bit 5 controls the power supply of P1_05.	0x0
4	R/W	P1_04_OUT_CTRL	0 = P1_04 port output is powered by the V30 rail (default) 1 = P1_04 port output is powered by the 1V8P rail Bit 4 controls the power supply of P1_04.	0x0
3	R/W	P1_03_OUT_CTRL	0 = P1_03 port output is powered by the V30 rail (default)	0x0

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Bit	Mode	Symbol	Description	Reset
			1 = P1_03 port output is powered by the 1V8P rail Bit 3 controls the power supply of P1_03.	
2	R/W	-	Reserved	0x0
1	R/W	P1_01_OUT_CTRL	0 = P1_01 port output is powered by the V30 rail (default) 1 = P1_01 port output is powered by the 1V8P rail Bit 1 controls the power supply of P1_01.	0x0
0	R/W	P1_00_OUT_CTRL	0 = P1_00 port output is powered by the V30 rail (default) 1 = P1_00 port output is powered by the 1V8P rail Bit 0 controls the power supply of P1_00.	0x0

Table 558: P2_PADPWR_CTRL_REG (0x50050268)

Bit	Mode	Symbol	Description	Reset
14	R/W	-	Reserved	0x0
13	R/W	-	Reserved	0x0
12	R/W	-	Reserved	0x0
11	R/W	P2_11_OUT_CTRL	0 = P2_11 port output is powered by the V30 rail (default) 1 = P2_11 port output is powered by the 1V8P rail Bit 11 controls the power supply of P2_11.	0x0
10	R/W	P2_10_OUT_CTRL	0 = P2_10 port output is powered by the V30 rail (default) 1 = P2_10 port output is powered by the 1V8P rail Bit 10 controls the power supply of P2_10.	0x0
9	R/W	P2_09_OUT_CTRL	0 = P2_09 port output is powered by the V30 rail (default) 1 = P2_09 port output is powered by the 1V8P rail Bit 9 controls the power supply of P2_09.	0x0
8	R/W	P2_08_OUT_CTRL	0 = P2_08 port output is powered by the V30 rail (default) 1 = P2_08 port output is powered by the 1V8P rail Bit 8 controls the power supply of P2_08.	0x0
7	R/W	-	Reserved	0x0
6	R/W	-	Reserved	0x0
5	R/W	-	Reserved	0x0
4	R/W	-	Reserved	0x0
3	R/W	-	Reserved	0x0
2	R/W	-	Reserved	0x0
1	R/W	P2_01_OUT_CTRL	0 = P2_01 port output is powered by the V30 rail (default) 1 = P2_01 port output is powered by the 1V8P rail Bit 1 controls the power supply of P2_01.	0x0
0	R/W	-	Reserved	0x0

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Table 559: GPIO_CLK_SEL_REG (0x5005026C)

Bit	Mode	Symbol	Description	Reset
9	R/W	DIVN_OUTPUT_EN	DIVN output enable bit-field. When set, it enables the mapping of DIVN clock on dedicated GPIO (P0_20). The specific GPIO must be configured as GPIO output.	0x0
8	R/W	-	Reserved	0x0
7	R/W	XTAL32M_OUTPUT_EN	XTAL32M output enable bit-field. When set, it enables the mapping of XTAL32M clock on dedicated GPIO (P0_09). The specific GPIO must be configured as GPIO output.	0x0
6	R/W	RCX_OUTPUT_EN	RCX output enable bit-field. When set, it enables the mapping of RCX clock on dedicated GPIO (P1_22). The specific GPIO must be configured as GPIO output.	0x0
5	R/W	RCLP_OUTPUT_EN	RCLP output enable bit-field. When set, it enables the mapping of RCLP clock on dedicated GPIO (P1_23). The specific GPIO must be configured as GPIO output.	0x0
4	R/W	XTAL32K_OUTPUT_EN	XTAL32K output enable bit-field. When set, it enables the mapping of XTAL32K clock on dedicated GPIO (P0_31).The specific GPIO must be configured as GPIO output.	0x0
3	R/W	FUNC_CLOCK_EN	If set, it enables the mapping of the selected clock signal, according to FUNC_CLOCK_SEL bit-field. The clock can be mapped to any GPIO (PX_YY), as long as PX_YY_MODE_REG[PID]= (FUNC_CLOCK) and PX_YY_MODE_REG[PUPD]=3 (Output). Bits 4-9 are ignored in this case. If not set, then each clock is mapped to a dedicated GPIO, according to bits 4-9."	0x0
2:0	R/W	FUNC_CLOCK_SEL	Select which clock to map when PID = FUNC_CLOCK. 0x0: XTAL32K 0x1: RCLP 0x2: RCX 0x3: XTAL32M 0x4: DIVN 0x5: Reserved 0x6: Reserved 0x7: Reserved FUNC_CLOCK_EN = 1 else masked	0x0

Table 560: P0_WEAK_CTRL_REG (0x50050270)

Bit	Mode	Symbol	Description	Reset
31	R/W	P0_31_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_31 pad	0x0

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Bit	Mode	Symbol	Description	Reset
			Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	
30	R/W	P0_30_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_30 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
29	R/W	P0_29_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_29 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
28	R/W	P0_28_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_28 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
27	R/W	P0_27_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_27 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
26	R/W	-	Reserved	0x0
25	R/W	-	Reserved	0x0
24	R/W	P0_24_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_24 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
23	R/W	P0_23_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_23 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
22	R/W	P0_22_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_22 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
21	R/W	P0_21_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_21 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific	0x0

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Bit	Mode	Symbol	Description	Reset
			pad (see also the description of P0_PADPWDR_CTRL_REG).	
20	R/W	P0_20_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_20 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
19	R/W	P0_19_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_19 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
18	R/W	P0_18_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_18 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
17	R/W	P0_17_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_17 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
16	R/W	P0_16_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_16 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
15	R/W	P0_15_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_15 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
14	R/W	P0_14_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_14 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
13	R/W	-	Reserved	0x0
12	R/W	-	Reserved	0x0
11	R/W	P0_11_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_11 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0

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Bit	Mode	Symbol	Description	Reset
10	R/W	P0_10_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_10 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
9	R/W	P0_09_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_09 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
8	R/W	P0_08_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_08 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
7	R/W	P0_07_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_07 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
6	R/W	P0_06_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_06 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
5	R/W	P0_05_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_05 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
4	R/W	P0_04_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_04 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
3	R/W	P0_03_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_03 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
2	R/W	P0_02_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_02 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific	0x0

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Bit	Mode	Symbol	Description	Reset
			pad (see also the description of P0_PADPWDR_CTRL_REG).	
1	R/W	P0_01_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_01 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0
0	R/W	P0_00_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P0_00 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P0_PADPWDR_CTRL_REG).	0x0

Table 561: P1_WEAK_CTRL_REG (0x50050274)

Bit	Mode	Symbol	Description	Reset
31	R/W	P1_31_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_30 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
30	R/W	P1_30_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_30 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
29	R/W	-	Reserved	0x0
28	R/W	-	Reserved	0x0
27	R/W	P1_27_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_27 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
26	R/W	P1_26_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_26 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
25	R/W	P1_25_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_25 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0

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Bit	Mode	Symbol	Description	Reset
24	R/W	P1_24_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_24 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
23	R/W	P1_23_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_23 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
22	R/W	P1_22_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_22 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
21	R/W	-	Reserved	0x0
20	R/W	P1_20_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_20 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
19	R/W	P1_19_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_19 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
18	R/W	-	Reserved	0x0
17	R/W	-	Reserved	0x0
16	R/W	-	Reserved	0x0
15	R/W	P1_15_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_15 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
14	R/W	P1_14_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_14 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
13	R/W	P1_13_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_13 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific	0x0

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Bit	Mode	Symbol	Description	Reset
			pad (see also the description of P1_PADPWDR_CTRL_REG).	
12	R/W	P1_12_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_12 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
11	R/W	P1_11_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_11 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
10	R/W	-	Reserved	0x0
9	R/W	-	Reserved	0x0
8	R/W	-	Reserved	0x0
7	R/W	P1_07_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_07 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
6	R/W	P1_06_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_06 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
5	R/W	P1_05_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_05 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
4	R/W	P1_04_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_04 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
3	R/W	P1_03_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_03 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0
2	R/W	-	Reserved	0x0
1	R/W	P1_01_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_01 pad	0x0

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Bit	Mode	Symbol	Description	Reset
			Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	
0	R/W	P1_00_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P1_00 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P1_PADPWDR_CTRL_REG).	0x0

Table 562: P2_WEAK_CTRL_REG (0x50050278)

Bit	Mode	Symbol	Description	Reset
14	R/W	-	Reserved	0x0
13	R/W	-	Reserved	0x0
12	R/W	-	Reserved	0x0
11	R/W	-	Reserved	0x0
10	R/W	-	Reserved	0x0
9	R/W	P2_09_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P2_09 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P2_PADPWDR_CTRL_REG).	0x0
8	R/W	P2_08_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P2_08 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P2_PADPWDR_CTRL_REG).	0x0
7	R/W	P2_07_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P2_07 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P2_PADPWDR_CTRL_REG).	0x0
6	R/W	P2_06_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P2_06 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P2_PADPWDR_CTRL_REG).	0x0
5	R/W	P2_05_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P2_05 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P2_PADPWDR_CTRL_REG).	0x0
4	R/W	P2_04_LOWDRV	0 = Normal operation	0x0

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Bit	Mode	Symbol	Description	Reset
			1 = Reduces the driving strength of P2_04 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P2_PADPWDR_CTRL_REG).	
3	R/W	-	Reserved	0x0
2	R/W	-	Reserved	0x0
1	R/W	P2_01_LOWDRV	0 = Normal operation 1 = Reduces the driving strength of P2_01 pad Note: This mode should be coupled with the selection of VDD1V8P supply rail for the specific pad (see also the description of P2_PADPWDR_CTRL_REG).	0x0
0	R/W	-	Reserved	0x0

Table 563: LCDC_MAP_CTRL_REG (0x5005027C)

Bit	Mode	Symbol	Description	Reset
14	R/W	MAP_ON_P1_07_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P1_07, overruling P1_07_MODE_REG. The signals mapped, depending on the mode, are the following: - JDI LCD I/F : Not applicable - LCD SPI I/F : Not applicable	0x0
13	R/W	MAP_ON_P1_01_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P1_01, overruling P1_01_MODE_REG. The signals mapped, depending on the mode, are the following: - JDI LCD I/F : BLUE0 (Output) - LCD SPI I/F : Not applicable	0x0
12	R/W	MAP_ON_P1_00_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P1_00, overruling P1_00_MODE_REG. The signals mapped, depending on the mode, are the following: - JDI LCD I/F : GREEN1 (Output) - LCD SPI I/F : Not applicable	0x0
11	R/W	MAP_ON_P0_24_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P0_24, overruling P0_24_MODE_REG. The signals mapped, depending on the mode, are the following: - JDI LCD I/F : GREEN0 (Output) - LCD SPI I/F : Not applicable	0x0
10	R/W	MAP_ON_P0_23_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P0_23, overruling P0_23_MODE_REG. The	0x0

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Bit	Mode	Symbol	Description	Reset
			signals mapped, depending on the mode, are the following: - JDI LCD I/F : RED1 (Output) - LCD SPI I/F : Not applicable	
9	R/W	MAP_ON_P0_22_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P0_22, overruling P0_22_MODE_REG. The signals mapped, depending on the mode, are the following: - JDI LCD I/F : XRST (Output) - LCD SPI I/F : LCD_SPI_SD2 (Output)	0x0
8	R/W	MAP_ON_P0_21_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P0_21, overruling P0_21_MODE_REG. The signals mapped, depending on the mode, are the following: - JDI LCD I/F : BLUE1 (Output) - LCD SPI I/F : Not applicable	0x0
7	R/W	MAP_ON_P0_19_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P0_19, overruling P0_19_MODE_REG. The signals mapped, depending on the mode, are the following: - JDI LCD I/F : VCOM/FRP (Input) - LCD SPI I/F : EXTCOMIN (Input)	0x0
6	R/W	MAP_ON_P0_18_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P0_18, overruling P0_18_MODE_REG. The signals mapped, depending on the mode, are the following: - JDI LCD I/F : ENB (Output) - MIPI DPI-2 : DPI_DE (Output) - MIPI DBI-B : DBIB_RESX (Output) - LCD SPI I/F : LCD_SPI_CS (Output)	0x0
5	R/W	MAP_ON_P0_17_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P0_17, overruling P0_17_MODE_REG. The signals mapped, depending on the mode, are the following: - JDI LCD I/F : RED0 (Output) - LCD SPI I/F : LCD_SPI_SD3 (Output)	0x0
4	R/W	MAP_ON_P0_16_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P0_16, overruling P0_16_MODE_REG. The signals mapped, depending on the mode, are the following: - JDI LCD I/F : VST (Output) - LCD SPI I/F : LCD_SPI_SD1 (Output)	0x0
3	R/W	MAP_ON_P0_15_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P0_15, overruling P0_15_MODE_REG. The	0x0

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Bit	Mode	Symbol	Description	Reset
			signals mapped, depending on the mode, are the following: - JDI LCD I/F : HST (Output) - LCD SPI I/F : LCD_SPI_SD (direction controlled by the LCDC SPI I/F)	
2	R/W	MAP_ON_P0_14_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P0_14, overruling P0_14_MODE_REG. The signals mapped, depending on the mode, are the following: - JDI LCD I/F : HCK (Output) - LCD SPI I/F : LCD_SPI_SCLK (Output)	0x0
1	R/W	MAP_ON_P0_10_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P0_10, overruling P0_10_MODE_REG. The signals mapped, depending on the mode, are the following: - JDI LCD I/F : XFRP (Input) - LCD SPI I/F : LCD_TE (Input)	0x0
0	R/W	MAP_ON_P0_09_EN	0 = Normal operation 1 = Enables the mapping of LCDC signals on P0_09, overruling P0_09_MODE_REG. The signals mapped, depending on the mode, are the following: - JDI LCD I/F : VCK (Output) - LCD SPI I/F : LCD_SPI_SI (Input)	0x0

Table 564: PAD_DRIVE_CTRL_REG (0x50050280)

Bit	Mode	Symbol	Description	Reset
11:10	R/W	EMMC_DRIVE	Pads drive current 0: 4 mA 1: 8 mA 2: 12 mA 3: 16 mA	0x3
9:8	R/W	EMMC_SLEW	Pads slew rate control. Indicative values under certain conditions: 0: Rise=1.7 V/ns, Fall=1.9 V/ns (weak) 1: Rise=2.0 V/ns, Fall=2.3 V/ns 2: Rise=2.3 V/ns, Fall=2.6 V/ns 3: Rise=2.4 V/ns, Fall=2.7 V/ns (strong) Conditions: external pin capacitance 6 pF, Vcc = 1.8 V, T = 25 °C and Idrive = 16 mA.	0x3
7:6	R/W	-	Reserved	0x3
5:4	R/W	-	Reserved	0x3
3:2	R/W	SPI3_DRIVE	Pads drive current 0: 4 mA 1: 8 mA 2: 12 mA	0x3

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Bit	Mode	Symbol	Description	Reset
			3: 16 mA	
1:0	R/W	SPI3_SLEW	QSPI pads slew rate control. Indicative values under certain conditions: 0: Rise=1.7 V/ns, Fall=1.9 V/ns (weak) 1: Rise=2.0 V/ns, Fall=2.3 V/ns 2: Rise=2.3 V/ns, Fall=2.6 V/ns 3: Rise=2.4 V/ns, Fall=2.7 V/ns (strong) Conditions: FLASH pin capacitance 6 pF, Vcc = 1.8 V, T = 25 °C and Idrive = 16 mA.	0x3

44.13 General Purpose Registers

Table 565: Register map GPREG

Address	Register	Description
0x50040100	SET_FREEZE_REG	Controls freezing of various timers/counters (incl. DMA and USB).
0x50040104	RESET_FREEZE_REG	Controls unfreezing of various timers/counters (incl. DMA and USB).
0x50040108	DEBUG_REG	Various debug information register.
0x5004010C	GP_STATUS_REG	General purpose system status register.
0x50040118	USBPAD_REG	USB pads control register

Table 566: SET_FREEZE_REG (0x50040100)

Bit	Mode	Symbol	Description	Reset
31:14	R	-	Reserved	0x0
13	R/W	FRZ_SWTIM6	If 1, the SW Timer6 is frozen, 0 is discarded.	0x0
12	R/W	FRZ_SWTIM5	If 1, the SW Timer5 is frozen, 0 is discarded.	0x0
11	R/W	FRZ_SNC_WDOG	If 1, the SNC SW Watchdog Timer is frozen, 0 is discarded.	0x0
10	R/W	FRZ_CMAC_WDOG	If 1, the CMAC SW Watchdog Timer is frozen, 0 is discarded.	0x0
9	R/W	FRZ_SWTIM4	If 1, the SW Timer4 is frozen, 0 is discarded.	0x0
8	R/W	FRZ_SWTIM3	If 1, the SW Timer3 is frozen, 0 is discarded.	0x0
7	R/W	FRZ_PWMLED	If 1, the PWM LED is frozen, 0 is discarded.	0x0
6	R/W	FRZ_SWTIM2	If 1, the SW Timer2 is frozen, 0 is discarded.	0x0
5	R/W	FRZ_DMA	If 1, the DMA is frozen, 0 is discarded.	0x0
4	R/W	FRZ_USB	If 1, the USB is frozen, 0 is discarded.	0x0
3	R/W	FRZ_SYS_WDOG	If 1, the SYS SW Watchdog Timer is frozen, 0 is discarded. WATCHDOG_CTRL_REG[NMI_RST] must be 0 to allow the freeze function.	0x0
2	R/W	FRZ_RESERVED		0x0

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Bit	Mode	Symbol	Description	Reset
1	R/W	FRZ_SWTIM	If 1, the SW Timer is frozen, 0 is discarded.	0x0
0	R/W	FRZ_WKUPTIM	If 1, the Wake Up Timer is frozen, 0 is discarded.	0x0

Table 567: RESET_FREEZE_REG (0x50040104)

Bit	Mode	Symbol	Description	Reset
31:14	R	-	Reserved	0x0
13	R/W	FRZ_SWTIM6	If 1, the SW Timer6 continues, 0 is discarded.	0x0
12	R/W	FRZ_SWTIM5	If 1, the SW Timer5 continues, 0 is discarded.	0x0
11	R/W	FRZ_SNC_WDOG	If 1, the SNC SW Watchdog Timer continues, 0 is discarded.	0x0
10	R/W	FRZ_CMAC_WDOG	If 1, the CMAC SW Watchdog Timer continues, 0 is discarded.	0x0
9	R/W	FRZ_SWTIM4	If 1, the SW Timer4 continues, 0 is discarded.	0x0
8	R/W	FRZ_SWTIM3	If 1, the SW Timer3 continues, 0 is discarded.	0x0
7	R/W	FRZ_PWMLED	If 1, the PWM LED continues, 0 is discarded.	0x0
6	R/W	FRZ_SWTIM2	If 1, the SW Timer2 continues, 0 is discarded.	0x0
5	R/W	FRZ_DMA	If 1, the DMA continues, 0 is discarded.	0x0
4	R/W	FRZ_USB	If 1, the USB continues, 0 is discarded.	0x0
3	R/W	FRZ_SYS_WDOG	If 1, the SYS SW Watchdog Timer continues, 0 is discarded.	0x0
2	R/W	FRZ_RESERVED		0x0
1	R/W	FRZ_SWTIM	If 1, the SW Timer continues, 0 is discarded.	0x0
0	R/W	FRZ_WKUPTIM	If 1, the Wake Up Timer continues, 0 is discarded.	0x0

Table 568: DEBUG_REG (0x50040108)

Bit	Mode	Symbol	Description	Reset
31:16	R	-	Reserved	0x0
15:13	R	-	Reserved	0x0
12	R/W	ETM_TRACE_MAP_ON_PINS_EN	1: ETM/TPIU Trace signals mapped on GPIO pins is enabled.	0x0
11	R	SNC_CPU_IS_HALTED	1: SNC CPU is halted.	0x0
10	R/W	HALT_SNC_CPU_EN	1: Enable halting the SNC CPU when the SYS CPU (ARM CM33) or CMAC CPU is halted. Note 1: This bit is retained. Note 2: Set this bit to 0 before going into deep sleep to prevent unpredictable halting behavior after waking up. Note 3: To be able to use this functionality, the **SNC CPU** debug module (DAP) must be enabled by connecting the debugger tool to it.	0x0

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Bit	Mode	Symbol	Description	Reset
9	R/W	SNC_CPU_FREEZE_EN	1: Enable Freezing on-chip peripherals (see Note 2) by the SNC CPU. Note 1: This bit is retained. Note 2: See [RE]SET_FREEZE_REG for the specific on-chip peripherals.	0x0
8	R/W	CROSS_CPU_HALT_SENSITIVITY	Select the cross CPU halt sensitivity. 0: Level triggered, 1: Pulse triggered. Note: This bit is retained.	0x1
7	R/W	SYS_CPUWAIT_ON_JTAG	1: Stall the processor core out of reset (**only after a wake-up from JTAG**). Debugger access continue when the core is stalled. When set to '0' again the core resumes instruction execution. This feature is independent of the PDC (Power Domain Controller) settings. If this bit is set and there is SW/JTAG activity during deep sleep, the SYS CPU is stalled after the wake-up. Note: This bit is retained.	0x0
6	R/W	SYS_CPUWAIT	1: Stall the processor core out of reset (**always after a wake-up**). Debugger access continue when the core is stalled. When set to 0 again the core resumes instruction execution. Note: This bit is retained.	0x0
5	R	CMAC_CPU_IS_HALTED	1: CMAC CPU is halted.	0x0
4	R	SYS_CPU_IS_HALTED	1: SYS CPU (ARM CM33) is halted.	0x0
3	R/W	HALT_SYS_CPU_EN	1: Enable halting the SYS CPU (ARM CM33) when the CMAC CPU or SNC CPU is halted. Note 1: This bit is retained. Note 2: Set this bit to 0 before going into deep sleep to prevent unpredictable halting behavior after waking up. Note 3: To be able to use this functionality, the **SYS CPU** debug module (DAP) must be enabled by connecting the debugger tool to it.	0x0
2	R/W	HALT_CMAC_CPU_EN	1: Enable halting the CMAC CPU when the SYS CPU (ARM CM33) or SNC CPU is halted. Note 1: This bit is retained. Note 2: Set this bit to 0 before going into deep sleep to prevent unpredictable halting behavior after waking up. Note 3: To be able to use this functionality, the **CMAC CPU** debug module (DAP) must be enabled by connecting the debugger tool to it.	0x0
1	R/W	CMAC_CPU_FREEZE_EN	1: Enable Freezing on-chip peripherals (see Note 2) by the CMAC CPU. Note 1: This bit is retained. Note 2: See [RE]SET_FREEZE_REG for the specific on-chip peripherals.	0x0
0	R/W	SYS_CPU_FREEZE_EN	1: Enable Freezing on-chip peripherals (see Note 2) by the SYS CPU (ARM CM33).	0x1

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Bit	Mode	Symbol	Description	Reset
			Default 1, freezing of the on-chip peripherals is enabled when the Cortex-M33 is halted in DEBUG State. If 0, freezing of the on-chip peripherals is only depending on [RE]SET_FREEZE_REG except the system watchdog timer. The system watchdog timer is always frozen when the Cortex-M33 is halted in DEBUG State. Note 1: This bit is retained. Note 2: See [RE]SET_FREEZE_REG for the specific on-chip peripherals.	

Table 569: GP_STATUS_REG (0x5004010C)

Bit	Mode	Symbol	Description	Reset
31:2	R	-	Reserved	0x0
1	R/W	-	Reserved	0x0
0	R/W	CAL_PHASE	If 1, it designates that the chip is in Calibration Phase, that is the OTP has been initially programmed but no Calibration has occured.	0x0

Table 570: USBPAD_REG (0x50040118)

Bit	Mode	Symbol	Description	Reset
2	R/W	USBPHY_FORCE_SW2_ON	0: Pull-up resistor SW2 is controlled by the USB controller. It is off when the USB is not enabled. 1: Force the pull-up resistor on USBP to be 2.3 kΩ	0x0
1	R/W	USBPHY_FORCE_SW1_OFF	0: Pull-up resistor SW1 is controlled by the USB controller. It is off when the USB is not enabled. 1: Force the pull-up resistor on USBP to be switched off.	0x0
0	R/W	USBPAD_EN	0: The power for the USB PHY and USB pads is switched on when the USB is enabled. 1: The power for the USB PHY and USB pads is forced on.	0x0

44.14 GPU Registers

Table 571: Register map GPU_CORE

Address	Register	Description
0x51001200	D2_CONTROL	#0: Geometry control register. This register controls the pixel enumeration and selection units, deciding which pixels are part of the geometry. Each geometry limiter can be enabled (default is disabled) by setting one of the enable bits. Note that disabled limiters are always read as 1.0. Limiters are grouped into three pairs of quadratic limiters, each of which can be coupled to track a quadractic instead of a linear equation. Note that in case of a coupled limiter only the first should have its enable Bit set. First

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Address	Register	Description
		two limiter outputs can be routed through an additional unit before clamping to mirror their gradient and form a "band" instead of the usual "halfplane". By default, each limiter output is clamped to fit into a range of [0..1] but by setting a limiter into threshold mode you can force its output to become binary (exactly 1.0 or exactly 0.0 at all times). All limiter outputs are combined into a single value by an array of combiner units. Each unit does a logical AND (intersection) by default, but can be switched into union mode to perform a logical OR instead. To improve enumeration efficiency on convex shapes, specify the hints for span store and span delay (see also D2_PITCH). To increase the precision of all limiters, the limiter-precision bit can be set (see also feature bits of D2_HWREVISION). Some bits are reserved
0x51001204	D2_CONTROL2	#1: Surface control register. This register controls the colorization, texturing and blending units, deciding what color a pixel should have. By default, the pixel color source is D2_COLOR1 but setting pattern or texture enable changes this. When using texturemapping filtering and clamping, control bits are used to specify details for the fetching of texels. Texture formats are defined by the read format. Writeback frame buffer formats are defined by the write format. The standard GPU uses as framebuffer formats. After a pixelcolor has been constructed the new pixel (src) is blended with the current framebuffer content (dst) as defined by the color channel blend flags. There are two modes for alpha channel blending: If USE_ACB = 0 then the former write-alpha mode is used (see also feature bits of D2_HWREVISION): An "alpha source" is relevant only if the framebuffer format includes an alpha channel. If USE_ACB = 1, then the full alpha channel blending is used as defined by the alpha channel blend flags. bit[xx] D2C_BC2A - blending for alpha channel is done with the alpha channel of D2_COLOR2 instead of the real dst value. This is an internal bit that is set if "alpha source" is set to 00. The entries of the CLUT are 32 bit words (see D2_TEXCLUT_DATA). The RLE format bits define the RLE format.
0x51001208	D2_CONTROL3	#2: Burst length limit control register. This register controls the burst length limit for the master bus interfaces. Log2 of the burst length limit: 0 - 2^0 = single transfer; 2 - 2^2 = max burst length 4; 3 - 2^3 = max burst length 8; 4 - 2^4 = max burst length 16. Valid values depend on the protocol of the used bus interface.
0x51001210	D2_L1START	#4: Limiter1 start value. All limiter registers are *write only*, reading will return undefined results. Limiters must be enabled (see D2_CONTROL) to produce an output value. In addition to the 6 geometry limiters there are two special UV-Limiters (see Texture registers). The start value is a 16:16 fixedpoint number valid at the first pixel of the bounding box.
0x51001214	D2_L2START	#5: Limiter2 start value. See D2_L1START
0x51001218	D2_L3START	#6: Limiter3 start value. See D2_L1START
0x5100121C	D2_L4START	#7: Limiter4 start value. See D2_L1START
0x51001220	D2_L5START	#8: Limiter5 start value. See D2_L1START
0x51001224	D2_L6START	#9: Limiter6 start value. See D2_L1START
0x51001228	D2_L1XADD	#10: Limiter1 X-Axis increment. The xadd value is the 16:16 fixedpoint difference between two samples with a distance of 1 pix along the x axis.
0x5100122C	D2_L2XADD	#11: Limiter2 X-Axis increment. See D2_L1XADD

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Address	Register	Description
0x51001230	D2_L3XADD	#12: Limiter3 X-Axis increment
0x51001234	D2_L4XADD	#13: Limiter4 X-Axis increment. See D2_L1XADD
0x51001238	D2_L5XADD	#14: Limiter5 X-Axis increment. See D2_L1XADD
0x5100123C	D2_L6XADD	#15: Limiter6 X-Axis increment. See D2_L1XADD
0x51001240	D2_L1YADD	#16: Limiter1 Y-Axis increment. The yadd value is the 16:16 fixedpoint difference between two samples with a distance of 1 pixel along the y axis.
0x51001244	D2_L2YADD	#17: Limiter2 Y-Axis increment. See D2_L1YADD
0x51001248	D2_L3YADD	#18: Limiter3 Y-Axis increment. See D2_L1YADD
0x5100124C	D2_L4YADD	#19: Limiter4 Y-Axis increment. See D2_L1YADD
0x51001250	D2_L5YADD	#20: Limiter5 Y-Axis increment. See D2_L1YADD
0x51001254	D2_L6YADD	#21: Limiter6 Y-Axis increment. See D2_L1YADD
0x51001258	D2_L1BAND	#22: Limiter1 band width parameter. Postfilter - first two limiter outputs can be routed through an additional unit before clamping to mirror their gradient and form a "band" instead of the usual "halfplane". When band output filtering is enabled for limiter1 (D2C_BAND1ENABLE see D2_CONTROL), this register stores the 16:16 fixedpoint inner width of band region.
0x5100125C	D2_L2BAND	#23: Limiter2 band width parameter. See D2_L1BAND
0x51001264	D2_COLOR1	#25: Base color register. All color registers are *write only*, reading will return undefined results. When using textures the two color registers (D2_COLOR1 and D2_COLOR2) are still used to modify the color value read from texture memory. The equation applied to each of the four color channels (when texture mapping) is: (c2-c1)*tex+c1. To keep the unmodified texture data c1 has to be 0 and c2 has to be 1, meaning 0x00000000 and 0xffffffff for D2_COLOR1 and D2_COLOR2 respectively. Color is always stored as 32-bit ARGB value. With 0xff000000 being opaque black.
0x51001268	D2_COLOR2	#26: Secondary color register. Secondary color is relevant only when rendering patterns, textures or using a D2C_BC2 blendmode (see D2_CONTROL2).
0x51001274	D2_PATTERN	#29: Pattern register. Each bit in the pattern register is interpreted as a reference to one of two color registers (0bit = D2_COLOR1, 1bit = D2_COLOR2).
0x51001278	D2_SIZE	#30: Bounding box dimension
0x5100127C	D2_PITCH	#31: Framebuffer pitch and spanstore delay
0x51001280	D2_ORIGIN	#32: Address of the first pixel in framebuffer. Writing to D2_ORIGIN will trigger GPU to start rendering.
0x51001290	D2_LUSTART	#36: U Limiter start value. The start value is a 16:16 fixedpoint number valid at the first pixel of the bounding box.
0x51001294	D2_LUXADD	#37: U Limiter X-Axis increment. The add value for U is the 16:16 fixedpoint difference between two samples with a distance of 1 pixel along the x axis.
0x51001298	D2_LUYADD	#38: U Limiter Y-Axis increment. The add value for U is the 16:16 fixedpoint difference between two samples with a distance of 1 pixel along the y axis.
0x5100129C	D2_LVSTARTI	#39: V Limiter start value integer part

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Address	Register	Description
0x510012A0	D2_LVSTARTF	#40: V Limiter start value fractional part. The start value is a 32:16 fixedpoint number valid at the first pixel of the bounding box.
0x510012A4	D2_LVXADDI	#41: V Limiter X-Axis increment integer part. The add value for V is the 32:16 fixedpoint difference between two samples with a distance of 1 pixel along the x axis.
0x510012A8	D2_LVYADDI	#42: V Limiter Y-Axis increment integer part. The add value for V is the 32:16 fixedpoint difference between two samples with a distance of 1 pixel along the y axis.
0x510012AC	D2_LVYXADDF	#43: V Limiter X and Y increment fractional parts
0x510012B4	D2_TEXPITCH	#45: Texels per texture line Pitch is equal or bigger than texture width.
0x510012B8	D2_TEXMASK	#46: Texture size or texture address mask. Depending on the clamping mode this register encodes the clamp limit or wrap mask.
0x510012BC	D2_TEXORIGIN	#47: Texture base address. All texture registers are *write only*, reading will return undefined results. Patterns and textures require a 1D or 2D index (UV Coordinate) at every pixel. Specialized UV-Limiters are available to generate these. Address of the upper left corner texel. Addresses inside the framebuffer can be used as valid texture origin as well.
0x510012C0	D2_IRQCTL	#48: Interrupt control register. The GPU features three sources for interrupts. They can be enabled and cleared individually. Enumeration finished - this interrupt is issued after every enumeration has finished. An enumeration is triggered by writing to D2_ORIGIN. This interrupt can be used if the CPU sets up all registers and waits for the enumeration to finish. It should not be used if the display list reader is active. Dlist finished - this interrupt is issued if the display list reader is used and it reads a display list end command (see special cases of Display list format). The display list reader starts to execute a display list if the start address of the display list is written to D2_DLISTSTART. Bus error - this interrupt is issued if any of the three bus adapters signals an error (see D2_STATUS). Read D2_STATUS to determine the current IRQ state (inside the IRQ handler, for example).
0x510012C4	D2_CACHECTL	#49: Cache control register. Internal caches can be enabled/disabled and flushed using this register. Note that caches will be disabled if a value without its enable bits set is written to D2_CACHECTL.
0x510012C8	D2_DLISTSTART	#50: Displaylist start address. Setting a new displaylist base address (writing to D2_DLISTSTART) *triggers* execution of the new dlist. Execution will stop only when a new list is set or the list terminates. Note that once the display list is started, the display list reader is the master for all register writes to the core: No register write must be done via the slave bus as long as the display list execution is ongoing. Otherwise, commands from the display list may be lost and rendering artifacts as well as core hangups can occur.
0x510012CC	D2_PERFCOUNT1	#51: Performance counter. Writing to the D2_PERFCOUNT1 register resets the first internal performance counter to the specified value. Reading returns the actual performance count. GPU will increment the count every time the event selected by D2_PERFTRIGGER lower 16 bits triggers.
0x510012D0	D2_PERFCOUNT2	#52: Performance counter. Writing to the D2_PERFCOUNT2 register resets the second internal performance counter to the

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Address	Register	Description
		specified value. GPU will increment the count every time the event selected by D2_PERFTRIGGER upper 16 bits triggers.
0x510012D4	D2_PERFTRIGGER	#53: Performance counters control register. Select the internal event that will increment D2_PERFCOUNT1 respectively D2_PERFCOUNT2 register. Possible event values: D2PC_NONE - disable performance counter (0), D2PC_GPUCYCLES - GPU active cycles (1), D2PC_FBREADS - framebuffer read access (2), D2PC_FBWRITES - framebuffer write access (3), D2PC_TXREADS - texture read access (4), D2PC_INVPIXELS - invisible pixels (enumerated but selected with alpha 0%) (5), D2PC_INVPIXELS_MISS - invisible pixels while internal fifo is empty (lost cycles) (6), D2PC_DLRCYCLES - displaylist reader active cycles (7), D2PC_FBREADHITS - framebuffer read hits (8), D2PC_FBREADMISSES - framebuffer read misses (9), D2PC_FBWRITEHITS - framebuffer write hits (10), D2PC_FBWRITEMISSES - framebuffer write misses (11), D2PC_TEXREADHITS - texture read hits (12), D2PC_TEXREADMISSES - texture read misses (13), D2_PC_DLRBURSTREADS - display list reader burst reads (17), D2_PC_DLRWORDSREAD - display list reader words read (18), D2PC_RLEREWINDS - RLE unit rewinds (20), D2_PC_TEXBURSTREADS - texture cache burst reads (21), D2_PC_TEXWORDSREAD - texture cache words read (22), D2_PC_FBBURSTREADS - framebuffer cache burst reads (23), D2_PC_FBWORDSREAD - framebuffer cache words read (24), D2_PC_FBBURSTWRITES - framebuffer cache burst writes (25), D2_PC_FBWORDSWRITTEN - framebuffer cache words written (26), D2PC_CLKCYCLES - every clock cycle (for use as timer) (31)
0x510012D8	D2_TEXCLUT	#54: Color Lookup Table for the indexed texture format 16x24bit Triggers a write into the CLUT if CLUT size is 16 x 24bit.
0x510012DC	D2_TEXCLUT_ADDR	#55: Color Lookup Table write address for the indexed texture format 256x32 bit. Start address for consecutive writes to D2_TEXCLUT_DATA if CLUT size is 256x32 bit.
0x510012E0	D2_TEXCLUT_DATA	#56: Color Lookup Table write data for the indexed texture format 256x32 bit. Writes one 32 bit color value into the CLUT if CLUT size is 256x32 bit. The write address is given by D2_TEXCLUT_ADDR and increments by 1 after each data write. bits[15..0] - first color value RGB565 if CLUTFORMAT = rgb565 for index*2. bits[31..16] - second color value RGB565 if CLUTFORMAT = rgb565 for index*2+1. See also D2_CONTROL2
0x510012E4	D2_TEXCLUT_OFFSET	#57: Offset to the texture index for the indexed texture formats i8, i4, i2 and i1. The index offset is combined with the texture index by a bitwise OR operation. For subbyte texture formats the CLUT can be divided into parts with different color sets.
0x510012E8	D2_COLKEY	#58: Color key value. The R, G, and B components of the internal color representation of a texel is compared with the color key. If the values are equal then A, R, G, and B are set to 0 (transparent), else A is set to 1. Color keying can be enabled by setting bit D2C_COLKEY_ENABLE in D2_CONTROL2
0x510012F0	D2_HWREVISION	#1: Hardware version and feature set ID. Read this (constant) register to identify the present hardware revision and feature set. HW Revision ID structure: Bits[28..16] HWFEATURES - Features. D/AVE Type: 0 - D/AVE2DT-S, 1 - D/AVE2DT-L. Feature Bits: the feature set is defined by the feature bits. The reset value depends on the hardware configuration.

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Address	Register	Description
0x510012F4	D2_STATUS	#0: Status control register. The current GPU status can be polled by reading this register. It contains a combination of the following bits. Source interface bus error: 001 - MFB interface, 010 - MTX interface, 100 - MDL interface. Depending on the hardware featureset (see D2_HWREVISION) some bits might be irrelevant on a specific HW platform.

Table 572: D2_CONTROL (0x51001200)

Bit	Mode	Symbol	Description	Reset
31:27	W	RESERVED	Reserved for GPU internal use	0x0
26:25	-	-	Reserved	0x0
24	W	D2C_LIMITERPRECISION	Increase precision of limiters from 16.16 to 10.22	0x0
23	W	D2C_SPANSTORE	Nextline span start is always equal or left to current-line span start	0x0
22	W	D2C_SPANABORT	Shape is horizontally convex. only a single span per scanline	0x0
21	W	D2C_UNIONCD	Combine outputs C and D as union (output is final)	0x0
20	W	D2C_UNIONAB	Combine outputs A and B as union (output is called C)	0x0
19	W	D2C_UNION56	Combine limiter 5 and 6 as union (output is called D)	0x0
18	W	D2C_UNION34	Combine limiter 3 and 4 as union (output is called B)	0x0
17	W	D2C_UNION12	Combine limiter 1 and 2 as union (output is called A)	0x0
16	W	D2C_BAND2ENABLE	Enable band postprocess for limiter 2 (see <D2_L2BAND>)	0x0
15	W	D2C_BAND1ENABLE	Enable band postprocess for limiter 1 (see <D2_L1BAND>)	0x0
14	W	D2C_LIM6THRESHOLD	Enable limiter 6 threshold mode	0x0
13	W	D2C_LIM5THRESHOLD	Enable limiter 5 threshold mode	0x0
12	W	D2C_LIM4THRESHOLD	Enable limiter 4 threshold mode	0x0
11	W	D2C_LIM3THRESHOLD	Enable limiter 3 threshold mode	0x0
10	W	D2C_LIM2THRESHOLD	Enable limiter 2 threshold mode	0x0
9	W	D2C_LIM1THRESHOLD	Enable limiter 1 threshold mode	0x0
8	W	D2C_QUAD3ENABLE	Enable quadratic coupling of limiters 5 and 6	0x0
7	W	D2C_QUAD2ENABLE	Enable quadratic coupling of limiters 3 and 4	0x0

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Bit	Mode	Symbol	Description	Reset
6	W	D2C_QUAD1ENABLE	Enable quadratic coupling of limiters 1 and 2	0x0
5	W	D2C_LIM6ENABLE	Enable limiter 6	0x0
4	W	D2C_LIM5ENABLE	Enable limiter 5	0x0
3	W	D2C_LIM4ENABLE	Enable limiter 4	0x0
2	W	D2C_LIM3ENABLE	Enable limiter 3	0x0
1	W	D2C_LIM2ENABLE	Enable limiter 2	0x0
0	W	D2C_LIM1ENABLE	Enable limiter 1	0x0

Table 573: D2_CONTROL2 (0x51001204)

Bit	Mode	Symbol	Description	Reset
31	W	D2C_RLEFORMAT2	Bit1 of RLE texel format	0x0
30	W	D2C_RLEFORMAT1	Bit0 of RLE texel format 00 - 1 byte per pixel 01 - 2 byte per pixel 10 - 3 byte per pixel 11 - 4 byte per pixel	0x0
29	W	D2C_BDIA	Dst factor for alpha channel will be inverted (meaning 1-a or 1-1 depending on BDFA)	0x0
28	W	D2C_BSIA	Src factor for alpha channel will be inverted (meaning 1-a or 1-1 depending on BSFA)	0x0
27	W	D2C_CLUTFORMAT1	Bit0 of the CLUT entry format 0 - argb8888 (4 bpp) 1 - rgb565 (2 bpp x 2) two entries per 32 bit word	0x0
26	W	D2C_COLKEY_ENABLE	Enable color keying (see also <D2_COLKEY> and feature bits of <D2_HWREVISION>)	0x0
25	W	D2C_CLUT_ENABLE	Enable the use of the CLUT (see also feature bits of <D2_HWREVISION>); if disabled the texture indices are written to FB	0x0
24	W	D2C_RLE_ENABLE	Enable RLE decoder (see also feature bits of <D2_HWREVISION>)	0x0
23	W	D2C_WRITEALPHA2	Bit1 of the "alpha source" (depends on USE_ACB)	0x0
22	W	D2C_WRITEALPHA1	Bit0 of the "alpha source" (depends on USE_ACB) 00 - alpha from D2_COLOR2 01 - src alpha (pixel coverage) 10 - reserved (alpha is set to zero) 11 - existing framebuffer alpha (alpha channel is kept unchanged)	0x0
21	W	D2C_WRITEFORMAT2	Bit1 of the framebuffer format descriptor	0x0

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Bit	Mode	Symbol	Description	Reset
20	W	D2C_WRITEFORMAT1	Bit0 of the framebuffer format descriptor 000 - alpha8 (1 bpp) 001 - rgb565 (2 bpp) 010 - argb8888 (4 bpp) 011 - argb4444 (2 bpp) 110 - rgba8888 (4 bpp) 111 - rgba4444 (2 bpp)	0x0
19	W	D2C_READFORMAT2	Bit1 of the texture format descriptor	0x0
18	W	D2C_READFORMAT1	Bit0 of the texture format descriptor 0000 - alpha8 (1 bpp) 0001 - rgb565 (2 bpp) 0010 - argb8888 (4 bpp) 0011 - argb4444 (2 bpp) 0100 - argb1555 (2 bpp) 0101 - ai44 (1 bpp) 0110 - rgba8888 (4 bpp) 0111 - rgba4444 (2 bpp) 1000 - rgba5551 (2 bpp) 1001 - i8 (1 bpp, 1pbb) 1010 - i4 (2 ppb) 1011 - i2 (4 ppb) 1100 - i1 (8 ppb) 1101 - alpha4 (2 ppb) 1110 - alpha2 (4 ppb) 1111 - alpha1 (8 ppb)	0x0
17	W	D2C_TEXTUREFILTERY	Linear filtering on texture v axis	0x0
16	W	D2C_TEXTUREFILTERX	Linear filtering on texture u axis	0x0
15	W	D2C_TEXTURECLAMPY	Clamp instead of mask v coordinate	0x0
14	W	D2C_TEXTURECLAMPX	Clamp instead of mask u coordinate	0x0
13	W	D2C_BC2	Blending for color channels is done with <D2_COLOR2> instead of the real dst value	0x0
12	W	D2C_BDI	Dst factor for color channels will be inverted (meaning 1-a or 1-1 depending on BDF)	0x0
11	W	D2C_BSI	Src factor for color channels will be inverted (meaning 1-a or 1-1 depending on BSF)	0x0
10	W	D2C_BDF	Dst factor for color channels is alpha (factor is 1 per default)	0x0
9	W	D2C_BSF	Src factor for color channels is alpha (factor is 1 per default)	0x0
8	W	D2C_WRITEFORMAT3	Bit2 of the framebuffer format descriptor	0x0

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Bit	Mode	Symbol	Description	Reset
7	W	D2C_BDFA	Dst factor for alpha channel is alpha (factor is 1 per default)	0x0
6	W	D2C_BSFA	Src factor for alpha channel is alpha (factor is 1 per default)	0x0
5	W	D2C_READFORMAT4	Bit3 of the texture format descriptor	0x0
4	W	D2C_READFORMAT3	Bit2 of the texture format descriptor	0x0
3	W	USE_ACB	Use full alpha channel blending, else use write-alpha mode	0x0
2	W	D2C_PATTERNSOURCEL5	Limiter 5 is used as pattern index instead of the default U-Limiter	0x0
1	W	D2C_TEXTUREENABLE	Pixel source is read from texture and used as an alpha to blend between <D2_COLOR1> and <D2_COLOR2>	0x0
0	W	D2C_PATTERNENABLE	Pixel source is a pattern color (blend of <D2_COLOR1> and <D2_COLOR2> depending on <D2_PATTERN> and pattern index)	0x0

Table 574: D2_CONTROL3 (0x51001208)

Bit	Mode	Symbol	Description	Reset
26:24	W	BURSTLENGTH_MDL	Burst length limit for MDL read (other values are not allowed) 0: single word transfer 2: 4 words 3: 8 words 4: 16 words	0x4
23:19	-	-	Reserved	0x0
18:16	W	BURSTLENGTH_MTX	Burst length limit for MTX read (other values are not allowed) 0: single word transfer 2: 4 words 3: 8 words 4: 16 words	0x4
15:11	-	-	Reserved	0x0
10:8	W	BURSTLENGTH_MFBW	Burst length limit for MFB write (other values are not allowed) 0: single word transfer 2: 4 words 3: 8 words 4: 16 words	0x4
7:3	-	-	Reserved	0x0
2:0	W	BURSTLENGTH_MFBR	Burst length limit for MFB read (other values are not allowed) 0: single word transfer 2: 4 words	0x4

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Bit	Mode	Symbol	Description	Reset
			3: 8 words 4: 16 words	

Table 575: D2_L1START (0x51001210)

Bit	Mode	Symbol	Description	Reset
31:0	W	L1START		0x0

Table 576: D2_L2START (0x51001214)

Bit	Mode	Symbol	Description	Reset
31:0	W	L2START		0x0

Table 577: D2_L3START (0x51001218)

Bit	Mode	Symbol	Description	Reset
31:0	W	L3START		0x0

Table 578: D2_L4START (0x5100121C)

Bit	Mode	Symbol	Description	Reset
31:0	W	L4START		0x0

Table 579: D2_L5START (0x51001220)

Bit	Mode	Symbol	Description	Reset
31:0	W	L5START		0x0

Table 580: D2_L6START (0x51001224)

Bit	Mode	Symbol	Description	Reset
31:0	W	L6START		0x0

Table 581: D2_L1XADD (0x51001228)

Bit	Mode	Symbol	Description	Reset
31:0	W	L1XADD		0x0

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Table 582: D2_L2XADD (0x5100122C)

Bit	Mode	Symbol	Description	Reset
31:0	W	L2XADD		0x0

Table 583: D2_L3XADD (0x51001230)

Bit	Mode	Symbol	Description	Reset
31:0	W	L3XADD		0x0

Table 584: D2_L4XADD (0x51001234)

Bit	Mode	Symbol	Description	Reset
31:0	W	L4XADD		0x0

Table 585: D2_L5XADD (0x51001238)

Bit	Mode	Symbol	Description	Reset
31:0	W	L5XADD		0x0

Table 586: D2_L6XADD (0x5100123C)

Bit	Mode	Symbol	Description	Reset
31:0	W	L6XADD		0x0

Table 587: D2_L1YADD (0x51001240)

Bit	Mode	Symbol	Description	Reset
31:0	W	L1YADD		0x0

Table 588: D2_L2YADD (0x51001244)

Bit	Mode	Symbol	Description	Reset
31:0	W	L2YADD		0x0

Table 589: D2_L3YADD (0x51001248)

Bit	Mode	Symbol	Description	Reset
31:0	W	L3YADD		0x0

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Table 590: D2_L4YADD (0x5100124C)

Bit	Mode	Symbol	Description	Reset
31:0	W	L4YADD		0x0

Table 591: D2_L5YADD (0x51001250)

Bit	Mode	Symbol	Description	Reset
31:0	W	L5YADD		0x0

Table 592: D2_L6YADD (0x51001254)

Bit	Mode	Symbol	Description	Reset
31:0	W	L6YADD		0x0

Table 593: D2_L1BAND (0x51001258)

Bit	Mode	Symbol	Description	Reset
31:0	W	L1BAND		0x0

Table 594: D2_L2BAND (0x5100125C)

Bit	Mode	Symbol	Description	Reset
31:0	W	L2BAND		0x0

Table 595: D2_COLOR1 (0x51001264)

Bit	Mode	Symbol	Description	Reset
31:0	W	COLOR1		0x0

Table 596: D2_COLOR2 (0x51001268)

Bit	Mode	Symbol	Description	Reset
31:0	W	COLOR2		0x0

Table 597: D2_PATTERN (0x51001274)

Bit	Mode	Symbol	Description	Reset
31:0	W	PATTERN		0x0

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Table 598: D2_SIZE (0x51001278)

Bit	Mode	Symbol	Description	Reset
31:16	W	SIZEY	The height (in pixels) of the primitives bounding box.	0x0
15:0	W	SIZEX	The width (in pixels) of the primitives bounding box.	0x0

Table 599: D2_PITCH (0x5100127C)

Bit	Mode	Symbol	Description	Reset
31:16	W	SSD	Spanstore delay, the number of scanlines to delay spanstore operations.	0x0
15:0	W	PITCH	The width (in pixels) of one framebuffer scanline. A negative width can be used to render bottom-up instead of top-down.	0x0

Table 600: D2_ORIGIN (0x51001280)

Bit	Mode	Symbol	Description	Reset
31:0	W	ORIGIN		0x0

Table 601: D2_LUSTART (0x51001290)

Bit	Mode	Symbol	Description	Reset
31:0	W	LUSTART		0x0

Table 602: D2_LUXADD (0x51001294)

Bit	Mode	Symbol	Description	Reset
31:0	W	LUXADD		0x0

Table 603: D2_LUYADD (0x51001298)

Bit	Mode	Symbol	Description	Reset
31:0	W	LUYADD		0x0

Table 604: D2_LVSTARTI (0x5100129C)

Bit	Mode	Symbol	Description	Reset
31:0	W	LVSTARTI		0x0

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Table 605: D2_LVSTARTF (0x510012A0)

Bit	Mode	Symbol	Description	Reset
15:0	W	LVSTARTF	Fractional part.	0x0

Table 606: D2_LVXADDI (0x510012A4)

Bit	Mode	Symbol	Description	Reset
31:0	W	LVXADDI		0x0

Table 607: D2_LVYADDI (0x510012A8)

Bit	Mode	Symbol	Description	Reset
31:0	W	LVYADDI		0x0

Table 608: D2_LVYXADDF (0x510012AC)

Bit	Mode	Symbol	Description	Reset
31:16	W	D2_LVYADDI_FRAC	Y increment fractional part for <D2_LVYADDI>.	0x0
15:0	W	D2_LVXADDI_FRAC	X increment fractional part for <D2_LVXADDI>.	0x0

Table 609: D2_TEXPITCH (0x510012B4)

Bit	Mode	Symbol	Description	Reset
31:0	W	TEXPITCH		0x0

Table 610: D2_TEXMASK (0x510012B8)

Bit	Mode	Symbol	Description	Reset
31:11	W	TEXVMASK	V mask.	0x0
10:0	W	TEXUMASK	U mask.	0x0

Table 611: D2_TEXORIGIN (0x510012BC)

Bit	Mode	Symbol	Description	Reset
31:0	W	TEXORIGIN		0x0

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Table 612: D2_IRQCTL (0x510012C0)

Bit	Mode	Symbol	Description	Reset
5	W	D2IRQCTL_CLR_BUS_ERROR	Clear Interrupt "Bus error"	0x0
4	W	D2IRQCTL_ENABLE_BUS_ERROR	Interruptmask enable "Bus error"	0x0
3	W	D2IRQCTL_CLR_FINISH_DLIST	Clear Interrupt "Displaylist is finished". Make sure to clear the IRQ before starting the DLR again. No register writes must be done by the CPU while the DLR is active.	0x0
2	W	D2IRQCTL_CLR_FINISH_ENUM	Clear Interrupt "Enumeration is finished"	0x0
1	W	D2IRQCTL_ENABLE_FINISH_DLIST	Interruptmask enable "Displaylist is finished"	0x0
0	W	D2IRQCTL_ENABLE_FINISH_ENUM	Interruptmask enable "Enumeration is finished"	0x0

Table 613: D2_CACHECTL (0x510012C4)

Bit	Mode	Symbol	Description	Reset
3	W	D2C_CACHECTL_FLUSH_TX	Flush texture cache	0x0
2	W	D2C_CACHECTL_ENABLE_TX	Texture cache enable	0x0
1	W	D2C_CACHECTL_FLUSH_FB	Flush framebuffer cache	0x0
0	W	D2C_CACHECTL_ENABLE_FB	Framebuffer cache enable	0x0

Table 614: D2_DLISTSTART (0x510012C8)

Bit	Mode	Symbol	Description	Reset
31:0	W	DLISTSTART		0x0

Table 615: D2_PERFCOUNT1 (0x510012CC)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PERFCOUNT1		0x0

Table 616: D2_PERFCOUNT2 (0x510012D0)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PERFCOUNT2		0x0

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Table 617: D2_PERFTRIGGER (0x510012D4)

Bit	Mode	Symbol	Description	Reset
31:16	W	PERFTRIGGER2	Select the internal event that will increment D2_PERFCOUNT2 register.	0x0
15:0	W	PERFTRIGGER1	Select the internal event that will increment D2_PERFCOUNT1 register.	0x0

Table 618: D2_TEXCLUT (0x510012D8)

Bit	Mode	Symbol	Description	Reset
31:24	W	TEXCLUT_INDEX	Index of the CLUT entry, that shall be written	0x0
23:0	W	TEXCLUT_RGB	Color Value RGB888	0x0

Table 619: D2_TEXCLUT_ADDR (0x510012DC)

Bit	Mode	Symbol	Description	Reset
7:0	W	TEXCLUT_ADDR	Write address	0x0

Table 620: D2_TEXCLUT_DATA (0x510012E0)

Bit	Mode	Symbol	Description	Reset
31:0	W	TEXCLUT_ARGB	Color value ARGB8888 if CLUTFORMAT = argb8888	0x0

Table 621: D2_TEXCLUT_OFFSET (0x510012E4)

Bit	Mode	Symbol	Description	Reset
7:0	W	TEXCLUT_OFFSET	Index offset	0x0

Table 622: D2_COLKEY (0x510012E8)

Bit	Mode	Symbol	Description	Reset
23:0	W	COLKEY_RGB	Color Key Value RGB888	0x0

Table 623: D2_HWREVISION (0x510012F0)

Bit	Mode	Symbol	Description	Reset
28	R	FB_BURSTSPLITTING	Bursts can be split with respect to burst length limit	0x1
27	R	FB_ALPHACHANNELBLENDING	Full alpha channel blending available	0x1

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Bit	Mode	Symbol	Description	Reset
26	R	FB_HILIMITERPRECISION	Increasable precision of limiters available	0x1
25	R	FB_COLORKEY	Color keying available	0x1
24	R	FB_TEXCLUT256	Extend CLUT to 256x32bit ARGB8888	0x1
23	R	FB_RLEUNIT	RLE texture decoder available	0x1
22	R	FB_FBPREFETCH	Framebuffer prefetch available	0x0
21	R	FB_TEXCLUT	Color Lookup Table 16x24bit for indexed textureformat available	0x1
20	R	FB_PERFCOUNT	Two performance counters available	0x1
19	R	FB_TXCACHE	Texture Cache available	0x1
18	R	FB_FBCACHE	Framebuffer Cache available	0x1
17	R	FB_DLR	DisplayListReader available	0x1
16	R	FB_SWGPU	Software GPU	0x0
15:12	R	HWTYPE	GPU Type	0x0
11:8	R	HWBRANCH	Branch number	0x0
7:0	R	HWREVISION	Revision number	0xD

Table 624: D2_STATUS (0x510012F4)

Bit	Mode	Symbol	Description	Reset
10:8	R	D2C_IRQ_BUS_ERROR_SRC	Source interface of bus error	0x0
7	-	-	Reserved	0x0
6	R	D2C_IRQ_BUS_ERROR	IRQ on bus error	0x0
5	R	D2C_IRQ_DLIST	IRQ on display list finish	0x0
4	R	D2C_IRQ_ENUM	IRQ on enumeration finish	0x0
3	R	D2C_DLISTACTIVE	Display list active, cant direct access hwregs	0x0
2	R	D2C_CACHE_DIRTY	Framebuffer cache dirty, cant flip frame	0x0
1	R	D2C_BUSY_WRITE	Framebuffer writeback busy, cant change framebuffer type	0x0
0	R	D2C_BUSY_ENUM	Enumeration unit busy, cant start new primitive	0x0

Table 625: Register map GPU_REG

Address	Register	Description
0x51001100	GPU_CTRL_REG	

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Table 626: GPU_CTRL_REG (0x51001100)

Bit	Mode	Symbol	Description	Reset
6	R/W	PWRS_B	Power save mode read port memories 0: Disabled 1: Enabled	0x0
0	R/W	GPU_EN	GPU enable 0:Enable 1:Disable	0x0

44.15 I2C Controller Registers

Table 627: Register map I2C

Address	Register	Description
0x50020500	I2C3_CON_REG	I2C Control Register
0x50020504	I2C3_TAR_REG	I2C Target Address Register
0x50020508	I2C3_SAR_REG	I2C Slave Address Register
0x5002050C	I2C3_HS_MADDR_REG	I2C High Speed Master Mode Code Address Register
0x50020510	I2C3_DATA_CMD_REG	I2C Rx/Tx Data Buffer and Command Register
0x50020514	I2C3_SS_SCL_HCNT_REG	Standard Speed I2C Clock SCL High Count Register
0x50020518	I2C3_SS_SCL_LCNT_REG	Standard Speed I2C Clock SCL Low Count Register
0x5002051C	I2C3_FS_SCL_HCNT_REG	Fast Speed I2C Clock SCL High Count Register
0x50020520	I2C3_FS_SCL_LCNT_REG	Fast Speed I2C Clock SCL Low Count Register
0x50020524	I2C3_HS_SCL_HCNT_REG	High Speed I2C Clock SCL High Count Register
0x50020528	I2C3_HS_SCL_LCNT_REG	High Speed I2C Clock SCL Low Count Register
0x5002052C	I2C3_INTR_STAT_REG	I2C Interrupt Status Register
0x50020530	I2C3_INTR_MASK_REG	I2C Interrupt Mask Register
0x50020534	I2C3_RAW_INTR_STAT_REG	I2C Raw Interrupt Status Register
0x50020538	I2C3_RX_TL_REG	I2C Receive FIFO Threshold Register
0x5002053C	I2C3_TX_TL_REG	I2C Transmit FIFO Threshold Register
0x50020540	I2C3_CLR_INTR_REG	Clear Combined and Individual Interrupt Register
0x50020544	I2C3_CLR_RX_UNDER_REG	Clear RX_UNDER Interrupt Register
0x50020548	I2C3_CLR_RX_OVER_REG	Clear RX_OVER Interrupt Register

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Address	Register	Description
0x5002054C	I2C3_CLR_TX_OVER_REG	Clear TX_OVER Interrupt Register
0x50020550	I2C3_CLR_RD_REQ_REG	Clear RD_REQ Interrupt Register
0x50020554	I2C3_CLR_TX_ABRT_REG	Clear TX_ABRT Interrupt Register
0x50020558	I2C3_CLR_RX_DONE_REG	Clear RX_DONE Interrupt Register
0x5002055C	I2C3_CLR_ACTIVITY_REG	Clear ACTIVITY Interrupt Register
0x50020560	I2C3_CLR_STOP_DET_REG	Clear STOP_DET Interrupt Register
0x50020564	I2C3_CLR_START_DET_REG	Clear START_DET Interrupt Register
0x50020568	I2C3_CLR_GEN_CALL_REG	Clear GEN_CALL Interrupt Register
0x5002056C	I2C3_ENABLE_REG	I2C Enable Register
0x50020570	I2C3_STATUS_REG	I2C Status Register
0x50020574	I2C3_TXFLR_REG	I2C Transmit FIFO Level Register
0x50020578	I2C3_RXFLR_REG	I2C Receive FIFO Level Register
0x5002057C	I2C3_SDA_HOLD_REG	I2C SDA Hold Time Length Register
0x50020580	I2C3_TX_ABRT_SOURCE_REG	I2C Transmit Abort Source Register
0x50020588	I2C3_DMA_CR_REG	DMA Control Register
0x5002058C	I2C3_DMA_TDLR_REG	DMA Transmit Data Level Register
0x50020590	I2C3_DMA_RDLR_REG	I2C Receive Data Level Register
0x50020594	I2C3_SDA_SETUP_REG	I2C SDA Setup Register
0x50020598	I2C3_ACK_GENERAL_CALL_REG	I2C ACK General Call Register
0x5002059C	I2C3_ENABLE_STATUS_REG	I2C Enable Status Register
0x500205A0	I2C3_IC_FS_SPKLEN_REG	I2C SS and FS spike suppression limit Size
0x500205A4	I2C3_IC_HS_SPKLEN_REG	I2C HS spike suppression limit Size
0x50020600	I2C_CON_REG	I2C Control Register
0x50020604	I2C_TAR_REG	I2C Target Address Register
0x50020608	I2C_SAR_REG	I2C Slave Address Register
0x5002060C	I2C_HS_MADDR_REG	I2C High Speed Master Mode Code Address Register
0x50020610	I2C_DATA_CMD_REG	I2C Rx/Tx Data Buffer and Command Register

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Address	Register	Description
0x50020614	I2C_SS_SCL_HCNT_REG	Standard Speed I2C Clock SCL High Count Register
0x50020618	I2C_SS_SCL_LCNT_REG	Standard Speed I2C Clock SCL Low Count Register
0x5002061C	I2C_FS_SCL_HCNT_REG	Fast Speed I2C Clock SCL High Count Register
0x50020620	I2C_FS_SCL_LCNT_REG	Fast Speed I2C Clock SCL Low Count Register
0x50020624	I2C_HS_SCL_HCNT_REG	High Speed I2C Clock SCL High Count Register
0x50020628	I2C_HS_SCL_LCNT_REG	High Speed I2C Clock SCL Low Count Register
0x5002062C	I2C_INTR_STAT_REG	I2C Interrupt Status Register
0x50020630	I2C_INTR_MASK_REG	I2C Interrupt Mask Register
0x50020634	I2C_RAW_INTR_STAT_REG	I2C Raw Interrupt Status Register
0x50020638	I2C_RX_TL_REG	I2C Receive FIFO Threshold Register
0x5002063C	I2C_TX_TL_REG	I2C Transmit FIFO Threshold Register
0x50020640	I2C_CLR_INTR_REG	Clear Combined and Individual Interrupt Register
0x50020644	I2C_CLR_RX_UNDER_REG	Clear RX_UNDER Interrupt Register
0x50020648	I2C_CLR_RX_OVER_REG	Clear RX_OVER Interrupt Register
0x5002064C	I2C_CLR_TX_OVER_REG	Clear TX_OVER Interrupt Register
0x50020650	I2C_CLR_RD_REQ_REG	Clear RD_REQ Interrupt Register
0x50020654	I2C_CLR_TX_ABRT_REG	Clear TX_ABRT Interrupt Register
0x50020658	I2C_CLR_RX_DONE_REG	Clear RX_DONE Interrupt Register
0x5002065C	I2C_CLR_ACTIVITY_REG	Clear ACTIVITY Interrupt Register
0x50020660	I2C_CLR_STOP_DET_REG	Clear STOP_DET Interrupt Register
0x50020664	I2C_CLR_START_DET_REG	Clear START_DET Interrupt Register
0x50020668	I2C_CLR_GEN_CALL_REG	Clear GEN_CALL Interrupt Register
0x5002066C	I2C_ENABLE_REG	I2C Enable Register
0x50020670	I2C_STATUS_REG	I2C Status Register
0x50020674	I2C_TXFLR_REG	I2C Transmit FIFO Level Register
0x50020678	I2C_RXFLR_REG	I2C Receive FIFO Level Register
0x5002067C	I2C_SDA_HOLD_REG	I2C SDA Hold Time Length Register

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Address	Register	Description
0x50020680	I2C_TX_ABRT_SOURCE_REG	I2C Transmit Abort Source Register
0x50020688	I2C_DMA_CR_REG	DMA Control Register
0x5002068C	I2C_DMA_TDLR_REG	DMA Transmit Data Level Register
0x50020690	I2C_DMA_RDLR_REG	I2C Receive Data Level Register
0x50020694	I2C_SDA_SETUP_REG	I2C SDA Setup Register
0x50020698	I2C_ACK_GENERAL_CALL_REG	I2C ACK General Call Register
0x5002069C	I2C_ENABLE_STATUS_REG	I2C Enable Status Register
0x500206A0	I2C_IC_FS_SPKLEN_REG	I2C SS and FS spike suppression limit Size
0x500206A4	I2C_IC_HS_SPKLEN_REG	I2C HS spike suppression limit Size
0x50020700	I2C2_CON_REG	I2C Control Register
0x50020704	I2C2_TAR_REG	I2C Target Address Register
0x50020708	I2C2_SAR_REG	I2C Slave Address Register
0x5002070C	I2C2_HS_MADDR_REG	I2C High Speed Master Mode Code Address Register
0x50020710	I2C2_DATA_CMD_REG	I2C Rx/Tx Data Buffer and Command Register
0x50020714	I2C2_SS_SCL_HCNT_REG	Standard Speed I2C Clock SCL High Count Register
0x50020718	I2C2_SS_SCL_LCNT_REG	Standard Speed I2C Clock SCL Low Count Register
0x5002071C	I2C2_FS_SCL_HCNT_REG	Fast Speed I2C Clock SCL High Count Register
0x50020720	I2C2_FS_SCL_LCNT_REG	Fast Speed I2C Clock SCL Low Count Register
0x50020724	I2C2_HS_SCL_HCNT_REG	High Speed I2C Clock SCL High Count Register
0x50020728	I2C2_HS_SCL_LCNT_REG	High Speed I2C Clock SCL Low Count Register
0x5002072C	I2C2_INTR_STAT_REG	I2C Interrupt Status Register
0x50020730	I2C2_INTR_MASK_REG	I2C Interrupt Mask Register
0x50020734	I2C2_RAW_INTR_STAT_REG	I2C Raw Interrupt Status Register
0x50020738	I2C2_RX_TL_REG	I2C Receive FIFO Threshold Register
0x5002073C	I2C2_TX_TL_REG	I2C Transmit FIFO Threshold Register
0x50020740	I2C2_CLR_INTR_REG	Clear Combined and Individual Interrupt Register
0x50020744	I2C2_CLR_RX_UNDER_REG	Clear RX_UNDER Interrupt Register

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Address	Register	Description
0x50020748	I2C2_CLR_RX_OVER_REG	Clear RX_OVER Interrupt Register
0x5002074C	I2C2_CLR_TX_OVER_REG	Clear TX_OVER Interrupt Register
0x50020750	I2C2_CLR_RD_REQ_REG	Clear RD_REQ Interrupt Register
0x50020754	I2C2_CLR_TX_ABRT_REG	Clear TX_ABRT Interrupt Register
0x50020758	I2C2_CLR_RX_DONE_REG	Clear RX_DONE Interrupt Register
0x5002075C	I2C2_CLR_ACTIVITY_REG	Clear ACTIVITY Interrupt Register
0x50020760	I2C2_CLR_STOP_DET_REG	Clear STOP_DET Interrupt Register
0x50020764	I2C2_CLR_START_DET_REG	Clear START_DET Interrupt Register
0x50020768	I2C2_CLR_GEN_CALL_REG	Clear GEN_CALL Interrupt Register
0x5002076C	I2C2_ENABLE_REG	I2C Enable Register
0x50020770	I2C2_STATUS_REG	I2C Status Register
0x50020774	I2C2_TXFLR_REG	I2C Transmit FIFO Level Register
0x50020778	I2C2_RXFLR_REG	I2C Receive FIFO Level Register
0x5002077C	I2C2_SDA_HOLD_REG	I2C SDA Hold Time Length Register
0x50020780	I2C2_TX_ABRT_SOURCE_REG	I2C Transmit Abort Source Register
0x50020788	I2C2_DMA_CR_REG	DMA Control Register
0x5002078C	I2C2_DMA_TDLR_REG	DMA Transmit Data Level Register
0x50020790	I2C2_DMA_RDLR_REG	I2C Receive Data Level Register
0x50020794	I2C2_SDA_SETUP_REG	I2C SDA Setup Register
0x50020798	I2C2_ACK_GENERAL_CALL_REG	I2C ACK General Call Register
0x5002079C	I2C2_ENABLE_STATUS_REG	I2C Enable Status Register
0x500207A0	I2C2_IC_FS_SPKLEN_REG	I2C SS and FS spike suppression limit Size
0x500207A4	I2C2_IC_HS_SPKLEN_REG	I2C HS spike suppression limit Size

Table 628: I2C3_CON_REG (0x50020500)

Bit	Mode	Symbol	Description	Reset
31:11	-	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
10	R	I2C_STOP_DET_IF_MASTER_ACTIVE	In Master mode: 1 = issues the STOP_DET interrupt only when master is active. 0 = issues the STOP_DET irrespective of whether master is active or not.	0x0
9	R/W	I2C_RX_FIFO_FULL_HLD_CTRL	This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH 1 = Hold bus when RX_FIFO is full 0 = Overflow when RX_FIFO is full	0x0
8	R/W	I2C_TX_EMPTY_CTRL	This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register. 1 = Controlled generation of TX_EMPTY interrupt 0 = Default behaviour of TX_EMPTY interrupt	0x0
7	R/W	I2C_STOP_DET_IF ADDRESSED	1 = slave issues STOP_DET intr only if addressed 0 = slave issues STOP_DET intr always During a general call address, this slave does not issue the STOP_DET interrupt if STOP_DET_IF_ADDRESSED = 1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).	0x0
6	R/W	I2C_SLAVE_DISABLE	Slave enabled or disabled after reset is applied, which means software does not have to configure the slave. 0=slave is enabled 1=slave is disabled Software should ensure that if this bit is written with '0', then bit 0 should also be written with a '0'.	0x1
5	R/W	I2C_RESTART_EN	Determines whether RESTART conditions may be sent when acting as a master 0= disable 1=enable	0x1
4	R/W	I2C_10BITADDR_MASTER	Controls whether the controller starts its transfers in 7- or 10-bit addressing mode when acting as a master. 0= 7-bit addressing 1= 10-bit addressing	0x1
3	R/W	I2C_10BITADDR_SLAVE	When acting as a slave, this bit controls whether the controller responds to 7- or 10-bit addresses. 0= 7-bit addressing 1= 10-bit addressing	0x1
2:1	R/W	I2C_SPEED	These bits control at which speed the controller operates. 1= standard mode (100 kbit/s) 2= fast mode (400 kbit/s) 3= high speed mode	0x3
0	R/W	I2C_MASTER_MODE	This bit controls whether the controller master is enabled.	0x1

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Bit	Mode	Symbol	Description	Reset
			0= master disabled 1= master enabled Software should ensure that if this bit is written with '1' then bit 6 should also be written with a '1'.	

Table 629: I2C3_TAR_REG (0x50020504)

Bit	Mode	Symbol	Description	Reset
31:12	-	-	Reserved	0x0
11	R/W	SPECIAL	On read This bit indicates whether software performs a General Call or START BYTE command. 0 = ignore bit 10 GC_OR_START and use IC_TAR normally 1 = perform special I2C command as specified in GC_OR_START bit On write 1 = Enables programming of GENERAL_CALL or START_BYTE transmission 0 = Disables programming of GENERAL_CALL or START_BYTE transmission Writes to this register succeed only when IC_ENABLE[0] is set to 0.	0x0
10	R/W	GC_OR_START	On read If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the controller. 0 = General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The controller remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. 1 = START BYTE On write 1 = START byte transmission 0 = GENERAL_CALL byte transmission Writes to this register succeed only when IC_ENABLE[0] is set to 0.	0x0
9:0	R/W	IC_TAR	This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. Note: If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave Writes to this register succeed only when IC_ENABLE[0] is set to 0.	0x55

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Table 630: I2C3_SAR_REG (0x50020508)

Bit	Mode	Symbol	Description	Reset
31:10	-	-	Reserved	0x0
9:0	R/W	IC_SAR	The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. Writes to this register succeed only when IC_ENABLE[0] is set to 0.	0x55

Table 631: I2C3_HS_MADDR_REG (0x5002050C)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	I2C_IC_HS_MAR	This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect.	0x1

Table 632: I2C3_DATA_CMD_REG (0x50020510)

Bit	Mode	Symbol	Description	Reset
30:11	-	-	Reserved	0x0
10	W	I2C_RESTART	This bit controls whether a RESTART is issued before the byte is sent or received. 1 = If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 = If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.	0x0
9	W	I2C_STOP	This bit controls whether a STOP is issued after the byte is sent or received. 1 = STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to	0x0

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Bit	Mode	Symbol	Description	Reset
			start a new transfer by issuing a START and arbitrating for the bus. 0 = STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.	
8	W	I2C_CMD	This bit controls whether a read or a write is performed. This bit does not control the direction when the I2C Ctrl acts as a slave. It controls only the direction when it acts as a master. 1 = Read 0 = Write When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that CPU data is to be transmitted and as DAT or IC_DATA_CMD[7:0]. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the I2C_RAW_INTR_STAT_REG), unless bit 11 (SPECIAL) in the I2C_TAR register has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs. NOTE: It is possible that while attempting a master I2C read transfer on the controller, a RD_REQ interrupt may have occurred simultaneously due to a remote I2C master addressing the controller. In this type of scenario, it ignores the I2C_DATA_CMD write, generates a TX_ABRT interrupt, and waits to service the RD_REQ interrupt	0x0
7:0	R/W	I2C_DAT	This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the controller. However, when you read this register, these bits return the value of data received on the controller's interface.	0x0

Table 633: I2C3_SS_SCL_HCNT_REG (0x50020514)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_SS_SCL_HCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled	0x91

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Bit	Mode	Symbol	Description	Reset
			which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. NOTE: This register must not be programmed to a value higher than 65525, because the controller uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.	

Table 634: I2C3_SS_SCL_LCNT_REG (0x50020518)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_SS_SCL_LCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the I2C_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set.	0xAB

Table 635: I2C3_FS_SCL_HCNT_REG (0x5002051C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_FS_SCL_HCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register can be written only when the I2C interface is disabled, which corresponds to the I2C_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set.	0x1A

Table 636: I2C3_FS_SCL_LCNT_REG (0x50020520)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_FS_SCL_LCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or	0x32

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Bit	Mode	Symbol	Description	Reset
			General CALL. This register can be written only when the I2C interface is disabled, which corresponds to the I2C_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the controller. The lower byte must be programmed first. Then the upper byte is programmed.	

Table 637: I2C3_HS_SCL_HCNT_REG (0x50020524)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_HS_SCL_HCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed.refer to "IC_CLK Frequency Configuration". The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.	0x6

Table 638: I2C3_HS_SCL_LCNT_REG (0x50020528)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_HS_SCL_LCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. For more information, refer to "IC_CLK Frequency Configuration". The SCL low time depends on the loading of the bus. For 100pF loading, the SCL low time is 160ns; for 400pF loading, the SCL low time is 320ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the	0x10

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Bit	Mode	Symbol	Description	Reset
			IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8.	

Table 639: I2C3_INTR_STAT_REG (0x5002052C)

Bit	Mode	Symbol	Description	Reset
31:15	-	-	Reserved	0x0
14	R	R_SCL_STUCK_AT_LOW	1 = R_SCL_STUCK_AT_LOW interrupt is active 0 = R_SCL_STUCK_AT_LOW interrupt is inactive	0x0
13	R	R_MASTER_ON_HOLD	Indicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.	0x0
12	R	R_RESTART_DET	Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. Note: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.	0x0
11	R	R_GEN_CALL	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling controller or when the CPU reads bit 0 of the I2C_CLR_GEN_CALL register. The controller stores the received data in the Rx buffer.	0x0
10	R	R_START_DET	Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether controller is operating in slave or master mode.	0x0
9	R	R_STOP_DET	Indicates whether a STOP condition has occurred on the I2C interface regardless of whether controller is operating in slave or master mode.	0x0
8	R	R_ACTIVITY	This bit captures I2C Ctrl activity and stays set until it is cleared. There are four ways to clear it: => Disabling the I2C Ctrl => Reading the IC_CLR_ACTIVITY register => Reading the IC_CLR_INTR register	0x0

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Bit	Mode	Symbol	Description	Reset
			=> System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the controller module is idle, this bit remains set until cleared, indicating that there was activity on the bus.	
7	R	R_RX_DONE	When the controller is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.	0x0
6	R	R_TX_ABRT	This bit indicates if the controller, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a "transmit abort". When this bit is set to 1, the I2C_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. NOTE: The controller flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register I2C_CLR_TX_ABRT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes from the APB interface.	0x0
5	R	R_RD_REQ	This bit is set to 1 when the controller is acting as a slave and another I2C master is attempting to read data from the controller. The controller holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the I2C_DATA_CMD register. This bit is set to 0 just after the processor reads the I2C_CLR_RD_REQ register	0x0
4	R	R_TX_EMPTY	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the I2C_TX_TL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When the IC_ENABLE bit 0 is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with ic_en=0, this bit is set to 0.	0x0
3	R	R_TX_OVER	Set during transmit if the transmit buffer is filled to 32 and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared	0x0
2	R	R_RX_FULL	Set when the receive buffer reaches or goes above the RX_TL threshold in the I2C_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (I2C_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX	0x0

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Bit	Mode	Symbol	Description	Reset
			FIFO is not full. So this bit is cleared once the I2C_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.	
1	R	R_RX_OVER	Set if the receive buffer is completely filled to 32 and an additional byte is received from an external I2C device. The controller acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.	0x0
0	R	R_RX_UNDER	Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.	0x0

Table 640: I2C3_INTR_MASK_REG (0x50020530)

Bit	Mode	Symbol	Description	Reset
31:15	-	-	Reserved	0x0
14	R	M_SCL_STUCK_AT_LOW	M_SCL_STUCK_AT_LOW Register field Reserved bits	0x0
13	R/W	M_MASTER_ON_HOLD	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
12	R/W	M_RESTART_DET	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
11	R/W	M_GEN_CALL	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
10	R/W	M_START_DET	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
9	R/W	M_STOP_DET	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
8	R/W	M_ACTIVITY	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
7	R/W	M_RX_DONE	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
6	R/W	M_TX_ABRT	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
5	R/W	M_RD_REQ	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
4	R/W	M_TX_EMPTY	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
3	R/W	M_TX_OVER	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
2	R/W	M_RX_FULL	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
1	R/W	M_RX_OVER	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1

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Bit	Mode	Symbol	Description	Reset
0	R/W	M_RX_UNDER	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1

Table 641: I2C3_RAW_INTR_STAT_REG (0x50020534)

Bit	Mode	Symbol	Description	Reset
31:15	-	-	Reserved	0x0
14	R	SCL_STUCK_AT_LOW	CL_STUCK_AT_LOW Register field Reserved bits	0x0
13	R	MASTER_ON_HOLD	ndicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.	0x0
12	R	RESTART_DET	Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. Note: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.	0x0
11	R	GEN_CALL	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling controller or when the CPU reads bit 0 of the I2C_CLR_GEN_CALL register. I2C Ctrl stores the received data in the Rx buffer.	0x0
10	R	START_DET	Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether controller is operating in slave or master mode.	0x0
9	R	STOP_DET	Indicates whether a STOP condition has occurred on the I2C interface regardless of whether controller is operating in slave or master mode.	0x0
8	R	ACTIVITY	This bit captures I2C Ctrl activity and stays set until it is cleared. There are four ways to clear it: => Disabling the I2C Ctrl => Reading the IC_CLR_ACTIVITY register => Reading the IC_CLR_INTR register => System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the controller module is idle, this bit remains set until cleared, indicating that there was activity on the bus.	0x0
7	R	RX_DONE	When the controller is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs	0x0

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Bit	Mode	Symbol	Description	Reset
			on the last byte of the transmission, indicating that the transmission is done.	
6	R	TX_ABRT	This bit indicates if the controller, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a "transmit abort". When this bit is set to 1, the I2C_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. NOTE: The controller flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register I2C_CLR_TX_ABRT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes from the APB interface.	0x0
5	R	RD_REQ	This bit is set to 1 when I2C Ctrl is acting as a slave and another I2C master is attempting to read data from the controller. The controller holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the I2C_DATA_CMD register. This bit is set to 0 just after the processor reads the I2C_CLR_RD_REQ register	0x0
4	R	TX_EMPTY	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the I2C_TX_TL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When the IC_ENABLE bit 0 is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with ic_en=0, this bit is set to 0.	0x0
3	R	TX_OVER	Set during transmit if the transmit buffer is filled to 32 and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared	0x0
2	R	RX_FULL	Set when the receive buffer reaches or goes above the RX_TL threshold in the I2C_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (I2C_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the I2C_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.	0x0
1	R	RX_OVER	Set if the receive buffer is completely filled to 32 and an additional byte is received from an external I2C device. The controller acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (I2C_ENABLE[0]=0), this bit keeps its level until the master or slave	0x0

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Bit	Mode	Symbol	Description	Reset
			state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.	
0	R	RX_UNDER	Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.	0x0

Table 642: I2C3_RX_TL_REG (0x50020538)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4:0	R/W	RX_TL	Receive FIFO Threshold Level Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in I2C_RAW_INTR_STAT register). The valid range is 0-31, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 31 sets the threshold for 32 entries.	0x0

Table 643: I2C3_TX_TL_REG (0x5002053C)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4:0	R/W	TX_TL	Transmit FIFO Threshold Level Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in I2C_RAW_INTR_STAT register). The valid range is 0-31, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 31 sets the threshold for 32 entries..	0x0

Table 644: I2C3_CLR_INTR_REG (0x50020540)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_INTR	Read this register to clear the combined interrupt, all individual interrupts, and the I2C_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the I2C_TX_ABRT_SOURCE register for an exception to clearing I2C_TX_ABRT_SOURCE	0x0

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Table 645: I2C3_CLR_RX_UNDER_REG (0x50020544)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_RX_UNDER	Read this register to clear the RX_UNDER interrupt (bit 0) of the I2C_RAW_INTR_STAT register.	0x0

Table 646: I2C3_CLR_RX_OVER_REG (0x50020548)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_RX_OVER	Read this register to clear the RX_OVER interrupt (bit 1) of the I2C_RAW_INTR_STAT register.	0x0

Table 647: I2C3_CLR_TX_OVER_REG (0x5002054C)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_TX_OVER	Read this register to clear the TX_OVER interrupt (bit 3) of the I2C_RAW_INTR_STAT register.	0x0

Table 648: I2C3_CLR_RD_REQ_REG (0x50020550)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_RD_REQ	Read this register to clear the RD_REQ interrupt (bit 5) of the I2C_RAW_INTR_STAT register.	0x0

Table 649: I2C3_CLR_TX_ABRT_REG (0x50020554)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_TX_ABRT	Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the I2C_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the I2C_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.	0x0

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Table 650: I2C3_CLR_RX_DONE_REG (0x50020558)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_RX_DONE	Read this register to clear the RX_DONE interrupt (bit 7) of the I2C_RAW_INTR_STAT register.	0x0

Table 651: I2C3_CLR_ACTIVITY_REG (0x5002055C)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_ACTIVITY	Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register	0x0

Table 652: I2C3_CLR_STOP_DET_REG (0x50020560)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_STOP_DET	Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.	0x0

Table 653: I2C3_CLR_START_DET_REG (0x50020564)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_START_DET	Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.	0x0

Table 654: I2C3_CLR_GEN_CALL_REG (0x50020568)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_GEN_CALL	Read this register to clear the GEN_CALL interrupt (bit 11) of I2C_RAW_INTR_STAT register.	0x0

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Table 655: I2C3_ENABLE_REG (0x5002056C)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	0x0
2	R/W	I2C_TX_CMD_BLOCK	In Master mode: 1 = Blocks the transmission of data on I2C bus even if Tx FIFO has data to transmit. 0.= The transmission of data starts on I2C bus automatically, as soon as the first data is available in the Tx FIFO.	0x0
1	R/W	I2C_ABORT	The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.	0x0
0	R/W	I2C_EN	Controls whether the controller is enabled. 0 = Disables the controller (TX and RX FIFOs are held in an erased state) 1 = Enables the controller Software can disable the controller while it is active. However, it is important that care be taken to ensure that the controller is disabled properly. When the controller is disabled, the following occurs: * The TX FIFO and RX FIFO get flushed. * Status bits in the IC_INTR_STAT register are still active until the controller goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the controller stops the current transfer at the end of the current byte and does not acknowledge the transfer. There is a two ic_clk delay when enabling or disabling the controller	0x0

Table 656: I2C3_STATUS_REG (0x50020570)

Bit	Mode	Symbol	Description	Reset
31:11	-	-	Reserved	0x0
10	R	LV_HOLD_RX_FIFO_FULL	This bit indicates the BUS Hold in Slave mode due to Rx FIFO is Full and an additional byte has been received 1 = Slave holds the bus due to Rx FIFO is full 0 = Slave is not holding the bus or Bus hold is not due to Rx FIFO is full	0x0
9	R	SLV_HOLD_TX_FIFO_EMPTY	This bit indicates the BUS Hold in Slave mode for the Read request when the Tx FIFO is empty. The Bus is in hold until the Tx FIFO has data to Transmit for the read request.	0x0

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Bit	Mode	Symbol	Description	Reset
			1 = Slave holds the bus due to Tx FIFO is empty 0 = Slave is not holding the bus or Bus hold is not due to Tx FIFO is empty	
8	R	MST_HOLD_RX_FIFO_FULL	This bit indicates the BUS Hold in Master mode due to Rx FIFO is Full and additional byte has been received 1 = Master holds the bus due to Rx FIFO is full 0 = Master is not holding the bus or Bus hold is not due to Rx FIFO is full	0x0
7	R	MST_HOLD_TX_FIFO_EMPTY	the DW_apb_i2c master stalls the write transfer when Tx FIFO is empty, and the the last byte does not have the Stop bit set. This bit indicates the BUS hold when the master holds the bus because of the Tx FIFO being empty, and the the previous transferred command does not have the Stop bit set. 1 =Master holds the bus due to Tx FIFO is empty 0 =Master is not holding the bus or Bus hold is not due to Tx FIFO is empty	0x0
6	R	SLV_ACTIVITY	Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. 0 = Slave FSM is in IDLE state so the Slave part of the controller is not Active 1 = Slave FSM is not in IDLE state so the Slave part of the controller is Active	0x0
5	R	MST_ACTIVITY	Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. 0 = Master FSM is in IDLE state so the Master part of the controller is not Active 1 = Master FSM is not in IDLE state so the Master part of the controller is Active	0x0
4	R	RFF	Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0 = Receive FIFO is not full 1 = Receive FIFO is full	0x0
3	R	RFNE	Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty	0x0
2	R	TFE	Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty	0x1
1	R	TFNF	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.	0x1

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Bit	Mode	Symbol	Description	Reset
			0 = Transmit FIFO is full 1 = Transmit FIFO is not full	
0	R	I2C_ACTIVITY	I2C Activity Status.	0x0

Table 657: I2C3_TXFLR_REG (0x50020574)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R	TXFLR	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO. Size is constrained by the TXFLR value	0x0

Table 658: I2C3_RXFLR_REG (0x50020578)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R	RXFLR	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO. Size is constrained by the RXFLR value	0x0

Table 659: I2C3_SDA_HOLD_REG (0x5002057C)

Bit	Mode	Symbol	Description	Reset
23:16	R/W	I2C_SDA_RX_HOLD	Sets the required SDA hold time in units of ic_clk period, when receiver.	0x0
15:0	R/W	I2C_SDA_TX_HOLD	Sets the required SDA hold time in units of ic_clk period, when transmitter.	0x1

Table 660: I2C3_TX_ABRT_SOURCE_REG (0x50020580)

Bit	Mode	Symbol	Description	Reset
16	R	ABRT_USER_ABRT	Master-Transmitter : This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1])	0x0
15	R	ABRT_SLVRD_INTX	Slave-Transmitter : When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of 2IC_DATA_CMD register 1 = Slave trying to transmit to remote master in read mode 0 = Slave trying to transmit to remote master in read mode- scenario not present	0x0
14	R	ABRT_SLV_ARBLOST	Slave-Transmitter : Slave lost the bus while transmitting data to a remote master. I2C_TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never "owns"	0x0

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Bit	Mode	Symbol	Description	Reset
			the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then the controller no longer own the bus. 1 = Slave lost arbitration to remote master 0 = Slave lost arbitration to remote master-scenario not present	
13	R	ABRT_SLVFLUSH_TXFIFO	Slave-Transmitter : Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. 1 = Slave flushes existing data in TX-FIFO upon getting read command 0 = Slave flushes existing data in TX-FIFO upon getting read command- scenario not present	0x0
12	R	ARB_LOST	Master-Transmitter or Slave-Transmitter : Master has lost arbitration, or if I2C_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Note: I2C can be both master and slave at the same time. 1 = Master or Slave-Transmitter lost arbitration 0 = Master or Slave-Transmitter lost arbitration-scenario not present	0x0
11	R	ABRT_MASTER_DIS	Master-Transmitter or Master-Receiver : User tries to initiate a Master operation with the Master mode disabled. 1 = User intitating master operation when MASTER disable 0 = User initiating master operation when MASTER disabled- scenario not present	0x0
10	R	ABRT_10B_RD_NORSTRT	Master-Receiver : The restart is disabled (IC_RESTART_EN bit (I2C_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode. 1 =Master trying to read in 10Bit addressing mode when RESTART disabled 0 =Master not trying to read in 10Bit addressing mode when RESTART disabled	0x0
9	R	ABRT_SBYTE_NORSTRT	Master : To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (I2C_CON[5]=1), the SPECIAL bit must be cleared (I2C_TAR[11]), or the GC_OR_START bit must be cleared (I2C_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted. 1: The restart is disabled (IC_RESTART_EN bit (I2C_CON[5]) = 0) and the user is trying to send a START Byte. 1 = User trying to send START byte when RESTART disabled	0x0

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Bit	Mode	Symbol	Description	Reset
			0 = User trying to send START byte when RESTART disabled- scenario not present	
8	R	ABRT_HS_NORSTRT	Master-Transmitter or Master-Receiver : The restart is disabled (IC_RESTART_EN bit (I2C_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode 1 = User trying to switch Master to HS mode when RESTART disabled 0 = User trying to switch Master to HS mode when RESTART disabled- scenario not present	0x0
7	R	ABRT_SBYTE_ACKDET	Master : Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). 1 = ACK detected for START byte 0 = ACK detected for START byte- scenario not present	0x0
6	R	ABRT_HS_ACKDET	Master : Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). 1 = HS Master code ACKed in HS Mode 0 = HS Master code ACKed in HS Mode- scenario not present	0x0
5	R	ABRT_GCALL_READ	Master-Transmitter : The controller in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1). 1 = GCALL is followed by read from bus 0 = GCALL is followed by read from bus-scenario not present	0x0
4	R	ABRT_GCALL_NOACK	Master-Transmitter : the controller in master mode sent a General Call and no slave on the bus acknowledged the General Call. 1 = GCALL not ACKed by any slave 0 = GCALL not ACKed by any slave-scenario not present	0x0
3	R	ABRT_TXDATA_NOACK	Master-Transmitter : This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). 1 = Transmitted data not ACKed by addressed slave 0 = Transmitted data non-ACKed by addressed slave-scenario not present	0x0
2	R	ABRT_10ADDR2_NOACK	Master-Transmitter or Master-Receiver : Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave. 1= Byte 2 of 10Bit Address not ACKed by any slave 0 = This abort is not generated	0x0
1	R	ABRT_10ADDR1_NOACK	Master-Transmitter or Master-Receiver : Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.	0x0

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Bit	Mode	Symbol	Description	Reset
			1 =Byte 1 of 10Bit Address not ACKed by any slave 0 =This abort is not generated	
0	R	ABRT_7B_ADDR_NOACK	Master-Transmitter or Master-Receiver : Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. 1 =This abort is generated because of NOACK for 7-bit address 0 =This abort is not generated	0x0

Table 661: I2C3_DMA_CR_REG (0x50020588)

Bit	Mode	Symbol	Description	Reset

1	R/W	TDMAE	Transmit DMA Enable. //This bit enables/disables the transmit FIFO DMA channel.
			0 = Transmit DMA disabled
			1 = Transmit DMA enabled
				0x0

0	R/W	RDMAE	Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled	0x0

Table 662: I2C3_DMA_TDLR_REG (0x5002058C)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	DMATDL	Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.	0x0

Table 663: I2C3_DMA_RDLR_REG (0x50020590)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	DMARDL	Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.	0x0

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Table 664: I2C3_SDA_SETUP_REG (0x50020594)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x0
7:0	R/W	SDA_SETUP	SDA Setup. This register controls the amount of time delay (number of I2C clock periods) between the rising edge of SCL and SDA changing by holding SCL low when I2C block services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. It is recommended that if the required delay is 1000ns, then for an I2C frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.Writes to this register succeed only when IC_ENABLE[0] = 0.	0x64

Table 665: I2C3_ACK_GENERAL_CALL_REG (0x50020598)

Bit	Mode	Symbol	Description	Reset
15:1	-	-	Reserved	0x0
0	R/W	ACK_GEN_CALL	ACK General Call. When set to 1, I2C Ctrl responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the controller does not generate General Call interrupts. 1 = Generate ACK for a General Call 0 = Generate NACK for General Call	0x0

Table 666: I2C3_ENABLE_STATUS_REG (0x5002059C)

Bit	Mode	Symbol	Description	Reset
15:3	-	-	Reserved	0x0
2	R	SLV_RX_DATA_LOST	Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0. When read as 1, the controller is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. NOTE: If the remote I2C master terminates the transfer with a STOP condition before the controller has a chance to NACK a transfer, and IC_ENABLE has been set to 0, then this bit is also set to 1. When read as 0, the controller is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. NOTE: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.	0x0

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Bit	Mode	Symbol	Description	Reset
			1 = Slave RX Data is lost 0 = Slave RX Data is not lost	
1	R	SLV_DISABLED_WHILE_BUSY	Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: (a) I2C Ctrl is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, the controller is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in I2C Ctrl (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. NOTE: If the remote I2C master terminates the transfer with a STOP condition before the the controller has a chance to NACK a transfer, and IC_ENABLE has been set to 0, then this bit will also be set to 1. When read as 0, the controller is deemed to have been disabled when there is master activity, or when the I2C bus is idle. NOTE: The CPU can safely read this bit when IC_EN (bit 0) is read as 0. 1 =Slave is disabled when it is active 0 =Slave is disabled when it is idle	0x0
0	R	IC_EN	ic_en Status. This bit always reflects the value driven on the output port ic_en. When read as 1, the controller is deemed to be in an enabled state. When read as 0, the controller is deemed completely inactive. NOTE: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLV_RX_DATA_LOST (bit 2) and SLV_DISABLED_WHILE_BUSY (bit 1). 1 = I2C enabled 0 =I2C disabled	0x0

Table 667: I2C3_IC_FS_SPKLEN_REG (0x500205A0)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x0
7:0	R/W	I2C_FS_SPKLEN	This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register	0x1

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Bit	Mode	Symbol	Description	Reset
			being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.	

Table 668: I2C3_IC_HS_SPKLEN_REG (0x500205A4)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	I2C_HS_SPKLEN	This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.	0x1

Table 669: I2C_CON_REG (0x50020600)

Bit	Mode	Symbol	Description	Reset
31:11	-	-	Reserved	0x0
10	R	I2C_STOP_DET_IF_MASTER_ACTIVE	In Master mode: 1 = issues the STOP_DET interrupt only when master is active. 0 = issues the STOP_DET irrespective of whether master is active or not.	0x0
9	R/W	I2C_RX_FIFO_FULL_HLD_CTRL	This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH 1 = Hold bus when RX_FIFO is full 0 = Overflow when RX_FIFO is full	0x0
8	R/W	I2C_TX_EMPTY_CTRL	This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register. 1 = Controlled generation of TX_EMPTY interrupt 0 = Default behaviour of TX_EMPTY interrupt	0x0
7	R/W	I2C_STOP_DET_IF_ADDRESSED	1 = slave issues STOP_DET intr only if addressed 0 = slave issues STOP_DET intr always During a general call address, this slave does not issue the STOP_DET interrupt if STOP_DET_IF_ADDRESSED = 1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).	0x0

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Bit	Mode	Symbol	Description	Reset
6	R/W	I2C_SLAVE_DISABLE	Slave enabled or disabled after reset is applied, which means software does not have to configure the slave. 0=slave is enabled 1=slave is disabled Software should ensure that if this bit is written with '0', then bit 0 should also be written with a '0'.	0x1
5	R/W	I2C_RESTART_EN	Determines whether RESTART conditions may be sent when acting as a master 0= disable 1=enable	0x1
4	R/W	I2C_10BITADDR_MASTER	Controls whether the controller starts its transfers in 7- or 10-bit addressing mode when acting as a master. 0= 7-bit addressing 1= 10-bit addressing	0x1
3	R/W	I2C_10BITADDR_SLAVE	When acting as a slave, this bit controls whether the controller responds to 7- or 10-bit addresses. 0= 7-bit addressing 1= 10-bit addressing	0x1
2:1	R/W	I2C_SPEED	These bits control at which speed the controller operates. 1= standard mode (100 kbit/s) 2= fast mode (400 kbit/s) 3= high speed mode	0x3
0	R/W	I2C_MASTER_MODE	This bit controls whether the controller master is enabled. 0= master disabled 1= master enabled Software should ensure that if this bit is written with '1' then bit 6 should also be written with a '1'.	0x1

Table 670: I2C_TAR_REG (0x50020604)

Bit	Mode	Symbol	Description	Reset
31:12	-	-	Reserved	0x0
11	R/W	SPECIAL	On read This bit indicates whether software performs a General Call or START BYTE command. 0 = ignore bit 10 GC_OR_START and use IC_TAR normally 1 = perform special I2C command as specified in GC_OR_START bit On write 1 = Enables programming of GENERAL_CALL or START_BYTE transmission 0 = Disables programming of GENERAL_CALL or START_BYTE transmission	0x0

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Bit	Mode	Symbol	Description	Reset
			Writes to this register succeed only when IC_ENABLE[0] is set to 0.	
10	R/W	GC_OR_START	On read If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the controller. 0 = General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The controller remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. 1 = START BYTE On write 1 = START byte transmission 0 = GENERAL_CALL byte transmission Writes to this register succeed only when IC_ENABLE[0] is set to 0.	0x0
9:0	R/W	IC_TAR	This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. Note: If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave Writes to this register succeed only when IC_ENABLE[0] is set to 0.	0x55

Table 671: I2C_SAR_REG (0x50020608)

Bit	Mode	Symbol	Description	Reset
31:10	-	-	Reserved	0x0
9:0	R/W	IC_SAR	The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. Writes to this register succeed only when IC_ENABLE[0] is set to 0.	0x55

Table 672: I2C_HS_MADDR_REG (0x5002060C)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	I2C_IC_HS_MAR	This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used	0x1

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Bit	Mode	Symbol	Description	Reset
			for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect.	

Table 673: I2C_DATA_CMD_REG (0x50020610)

Bit	Mode	Symbol	Description	Reset
30:11	-	-	Reserved	0x0
10	W	I2C_RESTART	This bit controls whether a RESTART is issued before the byte is sent or received. 1 = If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 = If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.	0x0
9	W	I2C_STOP	This bit controls whether a STOP is issued after the byte is sent or received. 1 = STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. 0 = STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.	0x0
8	W	I2C_CMD	This bit controls whether a read or a write is performed. This bit does not control the direction when the I2C Ctrl acts as a slave. It controls only the direction when it acts as a master. 1 = Read 0 = Write When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that CPU data is to be transmitted and as DAT or IC_DATA_CMD[7:0]. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call	0x0

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Bit	Mode	Symbol	Description	Reset
			command has been sent results in a TX_ABRT interrupt (bit 6 of the I2C_RAW_INTR_STAT_REG), unless bit 11 (SPECIAL) in the I2C_TAR register has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs. NOTE: It is possible that while attempting a master I2C read transfer on the controller, a RD_REQ interrupt may have occurred simultaneously due to a remote I2C master addressing the controller. In this type of scenario, it ignores the I2C_DATA_CMD write, generates a TX_ABRT interrupt, and waits to service the RD_REQ interrupt	
7:0	R/W	I2C_DAT	This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the controller. However, when you read this register, these bits return the value of data received on the controller's interface.	0x0

Table 674: I2C_SS_SCL_HCNT_REG (0x50020614)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_SS_SCL_HCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. NOTE: This register must not be programmed to a value higher than 65525, because the controller uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.	0x91

Table 675: I2C_SS_SCL_LCNT_REG (0x50020618)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_SS_SCL_LCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the I2C_ENABLE register being set to 0. Writes at other times have no effect.	0xAB

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Bit	Mode	Symbol	Description	Reset
			The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set.	

Table 676: I2C_FS_SCL_HCNT_REG (0x5002061C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_FS_SCL_HCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register can be written only when the I2C interface is disabled, which corresponds to the I2C_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set.	0x1A

Table 677: I2C_FS_SCL_LCNT_REG (0x50020620)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_FS_SCL_LCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register can be written only when the I2C interface is disabled, which corresponds to the I2C_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the controller. The lower byte must be programmed first. Then the upper byte is programmed.	0x32

Table 678: I2C_HS_SCL_HCNT_REG (0x50020624)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_HS_SCL_HCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed.refer to "IC_CLK Frequency Configuration". The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes	0x6

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Bit	Mode	Symbol	Description	Reset
			read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.	

Table 679: I2C_HS_SCL_LCNT_REG (0x50020628)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_HS_SCL_LCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. For more information, refer to "IC_CLK Frequency Configuration". The SCL low time depends on the loading of the bus. For 100pF loading, the SCL low time is 160ns; for 400pF loading, the SCL low time is 320ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8.	0x10

Table 680: I2C_INTR_STAT_REG (0x5002062C)

Bit	Mode	Symbol	Description	Reset
31:15	-	-	Reserved	0x0
14	R	R_SCL_STUCK_AT_LOW	1 = R_SCL_STUCK_AT_LOW interrupt is active 0 = R_SCL_STUCK_AT_LOW interrupt is inactive	0x0
13	R	R_MASTER_ON_HOLD	Indicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.	0x0

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Bit	Mode	Symbol	Description	Reset
12	R	R_RESTART_DET	Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. Note: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.	0x0
11	R	R_GEN_CALL	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling controller or when the CPU reads bit 0 of the I2C_CLR_GEN_CALL register. The controller stores the received data in the Rx buffer.	0x0
10	R	R_START_DET	Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether controller is operating in slave or master mode.	0x0
9	R	R_STOP_DET	Indicates whether a STOP condition has occurred on the I2C interface regardless of whether controller is operating in slave or master mode.	0x0
8	R	R_ACTIVITY	This bit captures I2C Ctrl activity and stays set until it is cleared. There are four ways to clear it: => Disabling the I2C Ctrl => Reading the IC_CLR_ACTIVITY register => Reading the IC_CLR_INTR register => System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the controller module is idle, this bit remains set until cleared, indicating that there was activity on the bus.	0x0
7	R	R_RX_DONE	When the controller is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.	0x0
6	R	R_TX_ABRT	This bit indicates if the controller, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a "transmit abort". When this bit is set to 1, the I2C_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. NOTE: The controller flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register I2C_CLR_TX_ABRT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes from the APB interface.	0x0

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Bit	Mode	Symbol	Description	Reset
5	R	R_RD_REQ	This bit is set to 1 when the controller is acting as a slave and another I2C master is attempting to read data from the controller. The controller holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the I2C_DATA_CMD register. This bit is set to 0 just after the processor reads the I2C_CLR_RD_REQ register	0x0
4	R	R_TX_EMPTY	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the I2C_TX_TL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When the IC_ENABLE bit 0 is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with ic_en=0, this bit is set to 0.	0x0
3	R	R_TX_OVER	Set during transmit if the transmit buffer is filled to 32 and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared	0x0
2	R	R_RX_FULL	Set when the receive buffer reaches or goes above the RX_TL threshold in the I2C_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (I2C_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the I2C_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.	0x0
1	R	R_RX_OVER	Set if the receive buffer is completely filled to 32 and an additional byte is received from an external I2C device. The controller acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.	0x0
0	R	R_RX_UNDER	Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.	0x0

Table 681: I2C_INTR_MASK_REG (0x50020630)

Bit	Mode	Symbol	Description	Reset
31:15	-	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
14	R	M_SCL_STUCK_AT_LOW	M_SCL_STUCK_AT_LOW Register field Reserved bits	0x0
13	R/W	M_MASTER_ON_HOLD	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
12	R/W	M_RESTART_DET	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
11	R/W	M_GEN_CALL	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
10	R/W	M_START_DET	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
9	R/W	M_STOP_DET	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
8	R/W	M_ACTIVITY	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
7	R/W	M_RX_DONE	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
6	R/W	M_TX_ABRT	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
5	R/W	M_RD_REQ	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
4	R/W	M_TX_EMPTY	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
3	R/W	M_TX_OVER	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
2	R/W	M_RX_FULL	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
1	R/W	M_RX_OVER	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
0	R/W	M_RX_UNDER	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1

Table 682: I2C_RAW_INTR_STAT_REG (0x50020634)

Bit	Mode	Symbol	Description	Reset
31:15	-	-	Reserved	0x0
14	R	SCL_STUCK_AT_LOW	CL_STUCK_AT_LOW Register field Reserved bits	0x0
13	R	MASTER_ON_HOLD	ndicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.	0x0
12	R	RESTART_DET	Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. Note: However, in high-speed mode or during a START BYTE transfer, the RESTART comes	0x0

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Bit	Mode	Symbol	Description	Reset
			before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.	
11	R	GEN_CALL	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling controller or when the CPU reads bit 0 of the I2C_CLR_GEN_CALL register. I2C Ctrl stores the received data in the Rx buffer.	0x0
10	R	START_DET	Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether controller is operating in slave or master mode.	0x0
9	R	STOP_DET	Indicates whether a STOP condition has occurred on the I2C interface regardless of whether controller is operating in slave or master mode.	0x0
8	R	ACTIVITY	This bit captures I2C Ctrl activity and stays set until it is cleared. There are four ways to clear it: => Disabling the I2C Ctrl => Reading the IC_CLR_ACTIVITY register => Reading the IC_CLR_INTR register => System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the controller module is idle, this bit remains set until cleared, indicating that there was activity on the bus.	0x0
7	R	RX_DONE	When the controller is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.	0x0
6	R	TX_ABRT	This bit indicates if the controller, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a "transmit abort". When this bit is set to 1, the I2C_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. NOTE: The controller flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register I2C_CLR_TX_ABRT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes from the APB interface.	0x0
5	R	RD_REQ	This bit is set to 1 when I2C Ctrl is acting as a slave and another I2C master is attempting to read data from the controller. The controller holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the I2C_DATA_CMD register.	0x0

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Bit	Mode	Symbol	Description	Reset
			This bit is set to 0 just after the processor reads the I2C_CLR_RD_REQ register	
4	R	TX_EMPTY	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the I2C_TX_TL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When the IC_ENABLE bit 0 is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with ic_en=0, this bit is set to 0.	0x0
3	R	TX_OVER	Set during transmit if the transmit buffer is filled to 32 and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared	0x0
2	R	RX_FULL	Set when the receive buffer reaches or goes above the RX_TL threshold in the I2C_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (I2C_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the I2C_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.	0x0
1	R	RX_OVER	Set if the receive buffer is completely filled to 32 and an additional byte is received from an external I2C device. The controller acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.	0x0
0	R	RX_UNDER	Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.	0x0

Table 683: I2C_RX_TL_REG (0x50020638)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4:0	R/W	RX_TL	Receive FIFO Threshold Level Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in I2C_RAW_INTR_STAT register). The valid range is 0-31, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.	0x0

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Bit	Mode	Symbol	Description	Reset
			A value of 0 sets the threshold for 1 entry, and a value of 31 sets the threshold for 32 entries.	

Table 684: I2C_TX_TL_REG (0x5002063C)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4:0	R/W	TX_TL	Transmit FIFO Threshold Level Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in I2C_RAW_INTR_STAT register). The valid range is 0-31, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 31 sets the threshold for 32 entries..	0x0

Table 685: I2C_CLR_INTR_REG (0x50020640)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_INTR	Read this register to clear the combined interrupt, all individual interrupts, and the I2C_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the I2C_TX_ABRT_SOURCE register for an exception to clearing I2C_TX_ABRT_SOURCE	0x0

Table 686: I2C_CLR_RX_UNDER_REG (0x50020644)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_RX_UNDER	Read this register to clear the RX_UNDER interrupt (bit 0) of the I2C_RAW_INTR_STAT register.	0x0

Table 687: I2C_CLR_RX_OVER_REG (0x50020648)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_RX_OVER	Read this register to clear the RX_OVER interrupt (bit 1) of the I2C_RAW_INTR_STAT register.	0x0

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Table 688: I2C_CLR_TX_OVER_REG (0x5002064C)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_TX_OVER	Read this register to clear the TX_OVER interrupt (bit 3) of the I2C_RAW_INTR_STAT register.	0x0

Table 689: I2C_CLR_RD_REQ_REG (0x50020650)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_RD_REQ	Read this register to clear the RD_REQ interrupt (bit 5) of the I2C_RAW_INTR_STAT register.	0x0

Table 690: I2C_CLR_TX_ABRT_REG (0x50020654)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_TX_ABRT	Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the I2C_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the I2C_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.	0x0

Table 691: I2C_CLR_RX_DONE_REG (0x50020658)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_RX_DONE	Read this register to clear the RX_DONE interrupt (bit 7) of the I2C_RAW_INTR_STAT register.	0x0

Table 692: I2C_CLR_ACTIVITY_REG (0x5002065C)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_ACTIVITY	Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register	0x0

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Table 693: I2C_CLR_STOP_DET_REG (0x50020660)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_STOP_DET	Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.	0x0

Table 694: I2C_CLR_START_DET_REG (0x50020664)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_START_DET	Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.	0x0

Table 695: I2C_CLR_GEN_CALL_REG (0x50020668)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_GEN_CALL	Read this register to clear the GEN_CALL interrupt (bit 11) of I2C_RAW_INTR_STAT register.	0x0

Table 696: I2C_ENABLE_REG (0x5002066C)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	0x0
2	R/W	I2C_TX_CMD_BLOCK	In Master mode: 1 = Blocks the transmission of data on I2C bus even if Tx FIFO has data to transmit. 0.= The transmission of data starts on I2C bus automatically, as soon as the first data is available in the Tx FIFO.	0x0
1	R/W	I2C_ABORT	The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.	0x0
0	R/W	I2C_EN	Controls whether the controller is enabled. 0 = Disables the controller (TX and RX FIFOs are held in an erased state)	0x0

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Bit	Mode	Symbol	Description	Reset
			1 = Enables the controller Software can disable the controller while it is active. However, it is important that care be taken to ensure that the controller is disabled properly. When the controller is disabled, the following occurs: * The TX FIFO and RX FIFO get flushed. * Status bits in the IC_INTR_STAT register are still active until the controller goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the controller stops the current transfer at the end of the current byte and does not acknowledge the transfer. There is a two ic_clk delay when enabling or disabling the controller	

Table 697: I2C_STATUS_REG (0x50020670)

Bit	Mode	Symbol	Description	Reset
31:11	-	-	Reserved	0x0
10	R	LV_HOLD_RX_FIFO_FULL	This bit indicates the BUS Hold in Slave mode due to Rx FIFO is Full and an additional byte has been received 1 = Slave holds the bus due to Rx FIFO is full 0 = Slave is not holding the bus or Bus hold is not due to Rx FIFO is full	0x0
9	R	SLV_HOLD_TX_FIFO_EMPTY	This bit indicates the BUS Hold in Slave mode for the Read request when the Tx FIFO is empty. The Bus is in hold until the Tx FIFO has data to Transmit for the read request. 1 = Slave holds the bus due to Tx FIFO is empty 0 = Slave is not holding the bus or Bus hold is not due to Tx FIFO is empty	0x0
8	R	MST_HOLD_RX_FIFO_FULL	This bit indicates the BUS Hold in Master mode due to Rx FIFO is Full and additional byte has been received 1 = Master holds the bus due to Rx FIFO is full 0 = Master is not holding the bus or Bus hold is not due to Rx FIFO is full	0x0
7	R	MST_HOLD_TX_FIFO_EMPTY	the DW_apb_i2c master stalls the write transfer when Tx FIFO is empty, and the the last byte does not have the Stop bit set. This bit indicates the BUS hold when the master holds the bus because of the Tx FIFO being empty, and the the previous transferred command does not have the Stop bit set. 1 =Master holds the bus due to Tx FIFO is empty 0 =Master is not holding the bus or Bus hold is not due to Tx FIFO is empty	0x0

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Bit	Mode	Symbol	Description	Reset
6	R	SLV_ACTIVITY	Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. 0 = Slave FSM is in IDLE state so the Slave part of the controller is not Active 1 = Slave FSM is not in IDLE state so the Slave part of the controller is Active	0x0
5	R	MST_ACTIVITY	Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. 0 = Master FSM is in IDLE state so the Master part of the controller is not Active 1 = Master FSM is not in IDLE state so the Master part of the controller is Active	0x0
4	R	RFF	Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0 = Receive FIFO is not full 1 = Receive FIFO is full	0x0
3	R	RFNE	Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty	0x0
2	R	TFE	Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty	0x1
1	R	TFNF	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full	0x1
0	R	I2C_ACTIVITY	I2C Activity Status.	0x0

Table 698: I2C_TXFLR_REG (0x50020674)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R	TXFLR	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO. Size is constrained by the TXFLR value	0x0

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Table 699: I2C_RXFLR_REG (0x50020678)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R	RXFLR	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO. Size is constrained by the RXFLR value	0x0

Table 700: I2C_SDA_HOLD_REG (0x5002067C)

Bit	Mode	Symbol	Description	Reset
23:16	R/W	I2C_SDA_RX_HOLD	Sets the required SDA hold time in units of ic_clk period, when receiver.	0x0
15:0	R/W	I2C_SDA_TX_HOLD	Sets the required SDA hold time in units of ic_clk period, when transmitter.	0x1

Table 701: I2C_TX_ABRT_SOURCE_REG (0x50020680)

Bit	Mode	Symbol	Description	Reset
16	R	ABRT_USER_ABRT	Master-Transmitter : This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1])	0x0
15	R	ABRT_SLVRD_INTX	Slave-Transmitter : When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of 2IC_DATA_CMD register 1 = Slave trying to transmit to remote master in read mode 0 = Slave trying to transmit to remote master in read mode- scenario not present	0x0
14	R	ABRT_SLV_ARBLOST	Slave-Transmitter : Slave lost the bus while transmitting data to a remote master. I2C_TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never "owns" the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then the controller no longer own the bus. 1 = Slave lost arbitration to remote master 0 = Slave lost arbitration to remote master- scenario not present	0x0
13	R	ABRT_SLVFLUSH_TXFIFO	Slave-Transmitter : Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. 1 = Slave flushes existing data in TX-FIFO upon getting read command 0 = Slave flushes existing data in TX-FIFO upon getting read command- scenario not present	0x0
12	R	ARB_LOST	Master-Transmitter or Slave-Transmitter : Master has lost arbitration, or if	0x0

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Bit	Mode	Symbol	Description	Reset
			I2C_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Note: I2C can be both master and slave at the same time. 1 = Master or Slave-Transmitter lost arbitration 0 = Master or Slave-Transmitter lost arbitration- scenario not present	
11	R	ABRT_MASTER_DIS	Master-Transmitter or Master-Receiver : User tries to initiate a Master operation with the Master mode disabled. 1 = User intitating master operation when MASTER disable 0 = User initiating master operation when MASTER disabled- scenario not present	0x0
10	R	ABRT_10B_RD_NORSTRT	Master-Receiver : The restart is disabled (IC_RESTART_EN bit (I2C_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode. 1 =Master trying to read in 10Bit addressing mode when RESTART disabled 0 =Master not trying to read in 10Bit addressing mode when RESTART disabled	0x0
9	R	ABRT_SBYTE_NORSTRT	Master : To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (I2C_CON[5]=1), the SPECIAL bit must be cleared (I2C_TAR[11]), or the GC_OR_START bit must be cleared (I2C_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted. 1: The restart is disabled (IC_RESTART_EN bit (I2C_CON[5]) = 0) and the user is trying to send a START Byte. 1 = User trying to send START byte when RESTART disabled 0 = User trying to send START byte when RESTART disabled- scenario not present	0x0
8	R	ABRT_HS_NORSTRT	Master-Transmitter or Master-Receiver : The restart is disabled (IC_RESTART_EN bit (I2C_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode 1 = User trying to switch Master to HS mode when RESTART disabled 0 = User trying to switch Master to HS mode when RESTART disabled- scenario not present	0x0
7	R	ABRT_SBYTE_ACKDET	Master : Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). 1 = ACK detected for START byte 0 = ACK detected for START byte- scenario not present	0x0
6	R	ABRT_HS_ACKDET	Master : Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). 1 = HS Master code ACKed in HS Mode	0x0

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Bit	Mode	Symbol	Description	Reset
			0 = HS Master code ACKed in HS Mode- scenario not present	
5	R	ABRT_GCALL_READ	Master-Transmitter : The controller in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1). 1 = GCALL is followed by read from bus 0 = GCALL is followed by read from bus-scenario not present	0x0
4	R	ABRT_GCALL_NOACK	Master-Transmitter : the controller in master mode sent a General Call and no slave on the bus acknowledged the General Call. 1 = GCALL not ACKed by any slave 0 = GCALL not ACKed by any slave-scenario not present	0x0
3	R	ABRT_TXDATA_NOACK	Master-Transmitter : This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). 1 = Transmitted data not ACKed by addressed slave 0 = Transmitted data non-ACKed by addressed slave-scenario not present	0x0
2	R	ABRT_10ADDR2_NOACK	Master-Transmitter or Master-Receiver : Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave. 1= Byte 2 of 10Bit Address not ACKed by any slave 0 = This abort is not generated	0x0
1	R	ABRT_10ADDR1_NOACK	Master-Transmitter or Master-Receiver : Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. 1 =Byte 1 of 10Bit Address not ACKed by any slave 0 =This abort is not generated	0x0
0	R	ABRT_7B_ADDR_NOACK	Master-Transmitter or Master-Receiver : Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. 1 =This abort is generated because of NOACK for 7-bit address 0 =This abort is not generated	0x0

Table 702: I2C_DMA_CR_REG (0x50020688)

Bit	Mode	Symbol	Description	Reset

1	R/W	TDMAE	Transmit DMA Enable. //This bit enables/disables the transmit FIFO DMA channel.
			0 = Transmit DMA disabled
			1 = Transmit DMA enabled
				0x0

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Bit	Mode	Symbol	Description	Reset
0	R/W	RDMAE	Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled	0x0

Table 703: I2C_DMA_TDLR_REG (0x5002068C)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	DMATDL	Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.	0x0

Table 704: I2C_DMA_RDLR_REG (0x50020690)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	DMARDL	Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.	0x0

Table 705: I2C_SDA_SETUP_REG (0x50020694)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x0
7:0	R/W	SDA_SETUP	SDA Setup. This register controls the amount of time delay (number of I2C clock periods) between the rising edge of SCL and SDA changing by holding SCL low when I2C block services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. It is recommended that if the required delay is 1000ns, then for an I2C frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.Writes to this register succeed only when IC_ENABLE[0] = 0.	0x64

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Table 706: I2C_ACK_GENERAL_CALL_REG (0x50020698)

Bit	Mode	Symbol	Description	Reset
15:1	-	-	Reserved	0x0
0	R/W	ACK_GEN_CALL	ACK General Call. When set to 1, I2C Ctrl responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the controller does not generate General Call interrupts. 1 = Generate ACK for a General Call 0 = Generate NACK for General Call	0x0

Table 707: I2C_ENABLE_STATUS_REG (0x5002069C)

Bit	Mode	Symbol	Description	Reset
15:3	-	-	Reserved	0x0
2	R	SLV_RX_DATA_LOST	Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0. When read as 1, the controller is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. NOTE: If the remote I2C master terminates the transfer with a STOP condition before the controller has a chance to NACK a transfer, and IC_ENABLE has been set to 0, then this bit is also set to 1. When read as 0, the controller is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. NOTE: The CPU can safely read this bit when IC_EN (bit 0) is read as 0. 1 = Slave RX Data is lost 0 = Slave RX Data is not lost	0x0
1	R	SLV_DISABLED_WHILE_BUSY	Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: (a) I2C Ctrl is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, the controller is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in I2C Ctrl (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. NOTE: If the remote I2C master terminates the transfer with a STOP condition before the the controller has a chance to NACK a transfer, and	0x0

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Bit	Mode	Symbol	Description	Reset
			IC_ENABLE has been set to 0, then this bit will also be set to 1. When read as 0, the controller is deemed to have been disabled when there is master activity, or when the I2C bus is idle. NOTE: The CPU can safely read this bit when IC_EN (bit 0) is read as 0. 1 =Slave is disabled when it is active 0 =Slave is disabled when it is idle	
0	R	IC_EN	ic_en Status. This bit always reflects the value driven on the output port ic_en. When read as 1, the controller is deemed to be in an enabled state. When read as 0, the controller is deemed completely inactive. NOTE: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLV_RX_DATA_LOST (bit 2) and SLV_DISABLED_WHILE_BUSY (bit 1). 1 = I2C enabled 0 =I2C disabled	0x0

Table 708: I2C_IC_FS_SPKLEN_REG (0x500206A0)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x0
7:0	R/W	I2C_FS_SPKLEN	This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.	0x1

Table 709: I2C_IC_HS_SPKLEN_REG (0x500206A4)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	I2C_HS_SPKLEN	This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect.	0x1

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Bit	Mode	Symbol	Description	Reset
			The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.	

Table 710: I2C2_CON_REG (0x50020700)

Bit	Mode	Symbol	Description	Reset
31:11	-	-	Reserved	0x0
10	R	I2C_STOP_DET_IF_MASTER_ACTIVE	In Master mode: 1 = issues the STOP_DET interrupt only when master is active. 0 = issues the STOP_DET irrespective of whether master is active or not.	0x0
9	R/W	I2C_RX_FIFO_FULL_HLD_CTRL	This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH 1 = Hold bus when RX_FIFO is full 0 = Overflow when RX_FIFO is full	0x0
8	R/W	I2C_TX_EMPTY_CTRL	This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register. 1 = Controlled generation of TX_EMPTY interrupt 0 = Default behaviour of TX_EMPTY interrupt	0x0
7	R/W	I2C_STOP_DET_IF ADDRESSED	1 = slave issues STOP_DET intr only if addressed 0 = slave issues STOP_DET intr always During a general call address, this slave does not issue the STOP_DET interrupt if STOP_DET_IF_ADDRESSED = 1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).	0x0
6	R/W	I2C_SLAVE_DISABLE	Slave enabled or disabled after reset is applied, which means software does not have to configure the slave. 0=slave is enabled 1=slave is disabled Software should ensure that if this bit is written with '0', then bit 0 should also be written with a '0'.	0x1
5	R/W	I2C_RESTART_EN	Determines whether RESTART conditions may be sent when acting as a master 0= disable 1=enable	0x1
4	R/W	I2C_10BITADDR_MASTER	Controls whether the controller starts its transfers in 7- or 10-bit addressing mode when acting as a master. 0= 7-bit addressing 1= 10-bit addressing	0x1
3	R/W	I2C_10BITADDR_SLAVE	When acting as a slave, this bit controls whether the controller responds to 7- or 10-bit addresses.	0x1

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Bit	Mode	Symbol	Description	Reset
			0= 7-bit addressing 1= 10-bit addressing	
2:1	R/W	I2C_SPEED	These bits control at which speed the controller operates. 1= standard mode (100 kbit/s) 2= fast mode (400 kbit/s) 3= high speed mode	0x3
0	R/W	I2C_MASTER_MODE	This bit controls whether the controller master is enabled. 0= master disabled 1= master enabled Software should ensure that if this bit is written with '1' then bit 6 should also be written with a '1'.	0x1

Table 711: I2C2_TAR_REG (0x50020704)

Bit	Mode	Symbol	Description	Reset
31:12	-	-	Reserved	0x0
11	R/W	SPECIAL	On read This bit indicates whether software performs a General Call or START BYTE command. 0 = ignore bit 10 GC_OR_START and use IC_TAR normally 1 = perform special I2C command as specified in GC_OR_START bit On write 1 = Enables programming of GENERAL_CALL or START_BYTE transmission 0 = Disables programming of GENERAL_CALL or START_BYTE transmission Writes to this register succeed only when IC_ENABLE[0] is set to 0.	0x0
10	R/W	GC_OR_START	On read If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the controller. 0 = General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The controller remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. 1 = START BYTE On write 1 = START byte transmission 0 = GENERAL_CALL byte transmission Writes to this register succeed only when IC_ENABLE[0] is set to 0.	0x0
9:0	R/W	IC_TAR	This is the target address for any master transaction. When transmitting a General Call,	0x55

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Bit	Mode	Symbol	Description	Reset
			these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. Note: If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave Writes to this register succeed only when IC_ENABLE[0] is set to 0.	

Table 712: I2C2_SAR_REG (0x50020708)

Bit	Mode	Symbol	Description	Reset
31:10	-	-	Reserved	0x0
9:0	R/W	IC_SAR	The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. Writes to this register succeed only when IC_ENABLE[0] is set to 0.	0x55

Table 713: I2C2_HS_MADDR_REG (0x5002070C)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	I2C_IC_HS_MAR	This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect.	0x1

Table 714: I2C2_DATA_CMD_REG (0x50020710)

Bit	Mode	Symbol	Description	Reset
30:11	-	-	Reserved	0x0
10	W	I2C_RESTART	This bit controls whether a RESTART is issued before the byte is sent or received. 1 = If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the	0x0

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Bit	Mode	Symbol	Description	Reset
			previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 = If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.	
9	W	I2C_STOP	This bit controls whether a STOP is issued after the byte is sent or received. 1 = STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. 0 = STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.	0x0
8	W	I2C_CMD	This bit controls whether a read or a write is performed. This bit does not control the direction when the I2C Ctrl acts as a slave. It controls only the direction when it acts as a master. 1 = Read 0 = Write When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that CPU data is to be transmitted and as DAT or IC_DATA_CMD[7:0]. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the I2C_RAW_INTR_STAT_REG), unless bit 11 (SPECIAL) in the I2C_TAR register has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs. NOTE: It is possible that while attempting a master I2C read transfer on the controller, a RD_REQ interrupt may have occurred simultaneously due to a remote I2C master addressing the controller. In this type of scenario, it ignores the I2C_DATA_CMD write, generates a TX_ABRT interrupt, and waits to service the RD_REQ interrupt	0x0
7:0	R/W	I2C_DAT	This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the controller. However, when you read this register, these bits return the value of data received on the controller's interface.	0x0

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Table 715: I2C2_SS_SCL_HCNT_REG (0x50020714)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_SS_SCL_HCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. NOTE: This register must not be programmed to a value higher than 65525, because the controller uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.	0x91

Table 716: I2C2_SS_SCL_LCNT_REG (0x50020718)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_SS_SCL_LCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the I2C_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set.	0xAB

Table 717: I2C2_FS_SCL_HCNT_REG (0x5002071C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_FS_SCL_HCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register can be written only when the I2C interface is disabled, which corresponds to the I2C_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set.	0x1A

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Table 718: I2C2_FS_SCL_LCNT_REG (0x50020720)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_FS_SCL_LCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register can be written only when the I2C interface is disabled, which corresponds to the I2C_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the controller. The lower byte must be programmed first. Then the upper byte is programmed.	0x32

Table 719: I2C2_HS_SCL_HCNT_REG (0x50020724)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_HS_SCL_HCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed.refer to "IC_CLK Frequency Configuration". The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.	0x6

Table 720: I2C2_HS_SCL_LCNT_REG (0x50020728)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IC_HS_SCL_LCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. For more information, refer to "IC_CLK Frequency Configuration". The SCL low time depends on the loading of the bus. For 100pF loading, the SCL low time is	0x10

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Bit	Mode	Symbol	Description	Reset
			160ns; for 400pF loading, the SCL low time is 320ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8.	

Table 721: I2C2_INTR_STAT_REG (0x5002072C)

Bit	Mode	Symbol	Description	Reset
31:15	-	-	Reserved	0x0
14	R	R_SCL_STUCK_AT_LOW	1 = R_SCL_STUCK_AT_LOW interrupt is active 0 = R_SCL_STUCK_AT_LOW interrupt is inactive	0x0
13	R	R_MASTER_ON_HOLD	Indicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.	0x0
12	R	R_RESTART_DET	Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. Note: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.	0x0
11	R	R_GEN_CALL	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling controller or when the CPU reads bit 0 of the I2C_CLR_GEN_CALL register. The controller stores the received data in the Rx buffer.	0x0
10	R	R_START_DET	Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether controller is operating in slave or master mode.	0x0
9	R	R_STOP_DET	Indicates whether a STOP condition has occurred on the I2C interface regardless of whether controller is operating in slave or master mode.	0x0

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Bit	Mode	Symbol	Description	Reset
8	R	R_ACTIVITY	This bit captures I2C Ctrl activity and stays set until it is cleared. There are four ways to clear it: => Disabling the I2C Ctrl => Reading the IC_CLR_ACTIVITY register => Reading the IC_CLR_INTR register => System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the controller module is idle, this bit remains set until cleared, indicating that there was activity on the bus.	0x0
7	R	R_RX_DONE	When the controller is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.	0x0
6	R	R_TX_ABRT	This bit indicates if the controller, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a "transmit abort". When this bit is set to 1, the I2C_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. NOTE: The controller flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register I2C_CLR_TX_ABRT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes from the APB interface.	0x0
5	R	R_RD_REQ	This bit is set to 1 when the controller is acting as a slave and another I2C master is attempting to read data from the controller. The controller holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the I2C_DATA_CMD register. This bit is set to 0 just after the processor reads the I2C_CLR_RD_REQ register	0x0
4	R	R_TX_EMPTY	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the I2C_TX_TL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When the IC_ENABLE bit 0 is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with ic_en=0, this bit is set to 0.	0x0
3	R	R_TX_OVER	Set during transmit if the transmit buffer is filled to 32 and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared	0x0

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Bit	Mode	Symbol	Description	Reset
2	R	R_RX_FULL	Set when the receive buffer reaches or goes above the RX_TL threshold in the I2C_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (I2C_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the I2C_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.	0x0
1	R	R_RX_OVER	Set if the receive buffer is completely filled to 32 and an additional byte is received from an external I2C device. The controller acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.	0x0
0	R	R_RX_UNDER	Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.	0x0

Table 722: I2C2_INTR_MASK_REG (0x50020730)

Bit	Mode	Symbol	Description	Reset
31:15	-	-	Reserved	0x0
14	R	M_SCL_STUCK_AT_LOW	M_SCL_STUCK_AT_LOW Register field Reserved bits	0x0
13	R/W	M_MASTER_ON_HOLD	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
12	R/W	M_RESTART_DET	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
11	R/W	M_GEN_CALL	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
10	R/W	M_START_DET	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
9	R/W	M_STOP_DET	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
8	R/W	M_ACTIVITY	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x0
7	R/W	M_RX_DONE	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
6	R/W	M_TX_ABRT	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
5	R/W	M_RD_REQ	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
4	R/W	M_TX_EMPTY	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1

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Bit	Mode	Symbol	Description	Reset
3	R/W	M_TX_OVER	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
2	R/W	M_RX_FULL	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
1	R/W	M_RX_OVER	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1
0	R/W	M_RX_UNDER	These bits mask their corresponding interrupt status bits in the I2C_INTR_STAT register.	0x1

Table 723: I2C2_RAW_INTR_STAT_REG (0x50020734)

Bit	Mode	Symbol	Description	Reset
31:15	-	-	Reserved	0x0
14	R	SCL_STUCK_AT_LOW	CL_STUCK_AT_LOW Register field Reserved bits	0x0
13	R	MASTER_ON_HOLD	ndicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.	0x0
12	R	RESTART_DET	Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. Note: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.	0x0
11	R	GEN_CALL	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling controller or when the CPU reads bit 0 of the I2C_CLR_GEN_CALL register. I2C Ctrl stores the received data in the Rx buffer.	0x0
10	R	START_DET	Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether controller is operating in slave or master mode.	0x0
9	R	STOP_DET	Indicates whether a STOP condition has occurred on the I2C interface regardless of whether controller is operating in slave or master mode.	0x0
8	R	ACTIVITY	This bit captures I2C Ctrl activity and stays set until it is cleared. There are four ways to clear it: => Disabling the I2C Ctrl => Reading the IC_CLR_ACTIVITY register => Reading the IC_CLR_INTR register => System reset	0x0

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Bit	Mode	Symbol	Description	Reset
			Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the controller module is idle, this bit remains set until cleared, indicating that there was activity on the bus.	
7	R	RX_DONE	When the controller is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.	0x0
6	R	TX_ABRT	This bit indicates if the controller, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a "transmit abort". When this bit is set to 1, the I2C_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. NOTE: The controller flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register I2C_CLR_TX_ABRT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes from the APB interface.	0x0
5	R	RD_REQ	This bit is set to 1 when I2C Ctrl is acting as a slave and another I2C master is attempting to read data from the controller. The controller holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the I2C_DATA_CMD register. This bit is set to 0 just after the processor reads the I2C_CLR_RD_REQ register	0x0
4	R	TX_EMPTY	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the I2C_TX_TL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When the IC_ENABLE bit 0 is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with ic_en=0, this bit is set to 0.	0x0
3	R	TX_OVER	Set during transmit if the transmit buffer is filled to 32 and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared	0x0
2	R	RX_FULL	Set when the receive buffer reaches or goes above the RX_TL threshold in the I2C_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (I2C_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the	0x0

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Bit	Mode	Symbol	Description	Reset
			I2C_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.	
1	R	RX_OVER	Set if the receive buffer is completely filled to 32 and an additional byte is received from an external I2C device. The controller acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.	0x0
0	R	RX_UNDER	Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.	0x0

Table 724: I2C2_RX_TL_REG (0x50020738)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4:0	R/W	RX_TL	Receive FIFO Threshold Level Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in I2C_RAW_INTR_STAT register). The valid range is 0-31, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 31 sets the threshold for 32 entries.	0x0

Table 725: I2C2_TX_TL_REG (0x5002073C)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4:0	R/W	TX_TL	Transmit FIFO Threshold Level Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in I2C_RAW_INTR_STAT register). The valid range is 0-31, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 31 sets the threshold for 32 entries..	0x0

Table 726: I2C2_CLR_INTR_REG (0x50020740)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
0	R	CLR_INTR	Read this register to clear the combined interrupt, all individual interrupts, and the I2C_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the I2C_TX_ABRT_SOURCE register for an exception to clearing I2C_TX_ABRT_SOURCE	0x0

Table 727: I2C2_CLR_RX_UNDER_REG (0x50020744)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_RX_UNDER	Read this register to clear the RX_UNDER interrupt (bit 0) of the I2C_RAW_INTR_STAT register.	0x0

Table 728: I2C2_CLR_RX_OVER_REG (0x50020748)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_RX_OVER	Read this register to clear the RX_OVER interrupt (bit 1) of the I2C_RAW_INTR_STAT register.	0x0

Table 729: I2C2_CLR_TX_OVER_REG (0x5002074C)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_TX_OVER	Read this register to clear the TX_OVER interrupt (bit 3) of the I2C_RAW_INTR_STAT register.	0x0

Table 730: I2C2_CLR_RD_REQ_REG (0x50020750)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_RD_REQ	Read this register to clear the RD_REQ interrupt (bit 5) of the I2C_RAW_INTR_STAT register.	0x0

Table 731: I2C2_CLR_TX_ABRT_REG (0x50020754)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_TX_ABRT	Read this register to clear the TX_ABRT interrupt (bit 6) of the	0x0

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Bit	Mode	Symbol	Description	Reset
			IC_RAW_INTR_STAT register, and the I2C_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the I2C_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.	

Table 732: I2C2_CLR_RX_DONE_REG (0x50020758)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_RX_DONE	Read this register to clear the RX_DONE interrupt (bit 7) of the I2C_RAW_INTR_STAT register.	0x0

Table 733: I2C2_CLR_ACTIVITY_REG (0x5002075C)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_ACTIVITY	Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register	0x0

Table 734: I2C2_CLR_STOP_DET_REG (0x50020760)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_STOP_DET	Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.	0x0

Table 735: I2C2_CLR_START_DET_REG (0x50020764)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_START_DET	Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.	0x0

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Table 736: I2C2_CLR_GEN_CALL_REG (0x50020768)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	CLR_GEN_CALL	Read this register to clear the GEN_CALL interrupt (bit 11) of I2C_RAW_INTR_STAT register.	0x0

Table 737: I2C2_ENABLE_REG (0x5002076C)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	0x0
2	R/W	I2C_TX_CMD_BLOCK	In Master mode: 1 = Blocks the transmission of data on I2C bus even if Tx FIFO has data to transmit. 0.= The transmission of data starts on I2C bus automatically, as soon as the first data is available in the Tx FIFO.	0x0
1	R/W	I2C_ABORT	The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.	0x0
0	R/W	I2C_EN	Controls whether the controller is enabled. 0 = Disables the controller (TX and RX FIFOs are held in an erased state) 1 = Enables the controller Software can disable the controller while it is active. However, it is important that care be taken to ensure that the controller is disabled properly. When the controller is disabled, the following occurs: * The TX FIFO and RX FIFO get flushed. * Status bits in the IC_INTR_STAT register are still active until the controller goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the controller stops the current transfer at the end of the current byte and does not acknowledge the transfer. There is a two ic_clk delay when enabling or disabling the controller	0x0

Table 738: I2C2_STATUS_REG (0x50020770)

Bit	Mode	Symbol	Description	Reset
31:11	-	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
10	R	LV_HOLD_RX_FIFO_FULL	This bit indicates the BUS Hold in Slave mode due to Rx FIFO is Full and an additional byte has been received 1 = Slave holds the bus due to Rx FIFO is full 0 = Slave is not holding the bus or Bus hold is not due to Rx FIFO is full	0x0
9	R	SLV_HOLD_TX_FIFO_EMPTY	This bit indicates the BUS Hold in Slave mode for the Read request when the Tx FIFO is empty. The Bus is in hold until the Tx FIFO has data to Transmit for the read request. 1 = Slave holds the bus due to Tx FIFO is empty 0 = Slave is not holding the bus or Bus hold is not due to Tx FIFO is empty	0x0
8	R	MST_HOLD_RX_FIFO_FULL	This bit indicates the BUS Hold in Master mode due to Rx FIFO is Full and additional byte has been received 1 = Master holds the bus due to Rx FIFO is full 0 = Master is not holding the bus or Bus hold is not due to Rx FIFO is full	0x0
7	R	MST_HOLD_TX_FIFO_EMPTY	the DW_apb_i2c master stalls the write transfer when Tx FIFO is empty, and the the last byte does not have the Stop bit set. This bit indicates the BUS hold when the master holds the bus because of the Tx FIFO being empty, and the the previous transferred command does not have the Stop bit set. 1 =Master holds the bus due to Tx FIFO is empty 0 =Master is not holding the bus or Bus hold is not due to Tx FIFO is empty	0x0
6	R	SLV_ACTIVITY	Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. 0 = Slave FSM is in IDLE state so the Slave part of the controller is not Active 1 = Slave FSM is not in IDLE state so the Slave part of the controller is Active	0x0
5	R	MST_ACTIVITY	Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. 0 = Master FSM is in IDLE state so the Master part of the controller is not Active 1 = Master FSM is not in IDLE state so the Master part of the controller is Active	0x0
4	R	RFF	Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0 = Receive FIFO is not full 1 = Receive FIFO is full	0x0
3	R	RFNE	Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty	0x0

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Bit	Mode	Symbol	Description	Reset
2	R	TFE	Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty	0x1
1	R	TFNF	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full	0x1
0	R	I2C_ACTIVITY	I2C Activity Status.	0x0

Table 739: I2C2_TXFLR_REG (0x50020774)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R	TXFLR	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO. Size is constrained by the TXFLR value	0x0

Table 740: I2C2_RXFLR_REG (0x50020778)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R	RXFLR	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO. Size is constrained by the RXFLR value	0x0

Table 741: I2C2_SDA_HOLD_REG (0x5002077C)

Bit	Mode	Symbol	Description	Reset
23:16	R/W	I2C_SDA_RX_HOLD	Sets the required SDA hold time in units of ic_clk period, when receiver.	0x0
15:0	R/W	I2C_SDA_TX_HOLD	Sets the required SDA hold time in units of ic_clk period, when transmitter.	0x1

Table 742: I2C2_TX_ABRT_SOURCE_REG (0x50020780)

Bit	Mode	Symbol	Description	Reset
16	R	ABRT_USER_ABRT	Master-Transmitter : This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1])	0x0
15	R	ABRT_SLVRD_INTX	Slave-Transmitter : When the processor side responds to a slave mode request for data to be	0x0

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Bit	Mode	Symbol	Description	Reset
			transmitted to a remote master and user writes a 1 in CMD (bit 8) of 2IC_DATA_CMD register 1 = Slave trying to transmit to remote master in read mode 0 = Slave trying to transmit to remote master in read mode- scenario not present	
14	R	ABRT_SLV_ARBLOST	Slave-Transmitter : Slave lost the bus while transmitting data to a remote master. I2C_TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never "owns" the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then the controller no longer own the bus. 1 = Slave lost arbitration to remote master 0 = Slave lost arbitration to remote master- scenario not present	0x0
13	R	ABRT_SLVFLUSH_TXFIFO	Slave-Transmitter : Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. 1 = Slave flushes existing data in TX-FIFO upon getting read command 0 = Slave flushes existing data in TX-FIFO upon getting read command- scenario not present	0x0
12	R	ARB_LOST	Master-Transmitter or Slave-Transmitter : Master has lost arbitration, or if I2C_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Note: I2C can be both master and slave at the same time. 1 = Master or Slave-Transmitter lost arbitration 0 = Master or Slave-Transmitter lost arbitration- scenario not present	0x0
11	R	ABRT_MASTER_DIS	Master-Transmitter or Master-Receiver : User tries to initiate a Master operation with the Master mode disabled. 1 = User intitating master operation when MASTER disable 0 = User initiating master operation when MASTER disabled- scenario not present	0x0
10	R	ABRT_10B_RD_NORSTRT	Master-Receiver : The restart is disabled (IC_RESTART_EN bit (I2C_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode. 1 =Master trying to read in 10Bit addressing mode when RESTART disabled 0 =Master not trying to read in 10Bit addressing mode when RESTART disabled	0x0
9	R	ABRT_SBYTE_NORSTRT	Master : To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (I2C_CON[5]=1), the SPECIAL bit must be cleared (I2C_TAR[11]), or the GC_OR_START bit must be cleared (I2C_TAR[10]). Once the source of the	0x0

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Bit	Mode	Symbol	Description	Reset
			ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted. 1: The restart is disabled (IC_RESTART_EN bit (I2C_CON[5]) = 0) and the user is trying to send a START Byte. 1 = User trying to send START byte when RESTART disabled 0 = User trying to send START byte when RESTART disabled- scenario not present	
8	R	ABRT_HS_NORSTRT	Master-Transmitter or Master-Receiver : The restart is disabled (IC_RESTART_EN bit (I2C_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode 1 = User trying to switch Master to HS mode when RESTART disabled 0 = User trying to switch Master to HS mode when RESTART disabled- scenario not present	0x0
7	R	ABRT_SBYTE_ACKDET	Master : Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). 1 = ACK detected for START byte 0 = ACK detected for START byte- scenario not present	0x0
6	R	ABRT_HS_ACKDET	Master : Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). 1 = HS Master code ACKed in HS Mode 0 = HS Master code ACKed in HS Mode- scenario not present	0x0
5	R	ABRT_GCALL_READ	Master-Transmitter : The controller in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1). 1 = GCALL is followed by read from bus 0 = GCALL is followed by read from bus-scenario not present	0x0
4	R	ABRT_GCALL_NOACK	Master-Transmitter : the controller in master mode sent a General Call and no slave on the bus acknowledged the General Call. 1 = GCALL not ACKed by any slave 0 = GCALL not ACKed by any slave-scenario not present	0x0
3	R	ABRT_TXDATA_NOACK	Master-Transmitter : This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). 1 = Transmitted data not ACKed by addressed slave 0 = Transmitted data non-ACKed by addressed slave-scenario not present	0x0

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Bit	Mode	Symbol	Description	Reset
2	R	ABRT_10ADDR2_NOACK	Master-Transmitter or Master-Receiver : Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave. 1= Byte 2 of 10Bit Address not ACKed by any slave 0 = This abort is not generated	0x0
1	R	ABRT_10ADDR1_NOACK	Master-Transmitter or Master-Receiver : Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. 1 =Byte 1 of 10Bit Address not ACKed by any slave 0 =This abort is not generated	0x0
0	R	ABRT_7B_ADDR_NOACK	Master-Transmitter or Master-Receiver : Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. 1 =This abort is generated because of NOACK for 7-bit address 0 =This abort is not generated	0x0

Table 743: I2C2_DMA_CR_REG (0x50020788)

Bit	Mode	Symbol	Description	Reset

1	R/W	TDMAE	Transmit DMA Enable. //This bit enables/disables the transmit FIFO DMA channel.
			0 = Transmit DMA disabled
			1 = Transmit DMA enabled
				0x0

0	R/W	RDMAE	Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled	0x0

Table 744: I2C2_DMA_TDLR_REG (0x5002078C)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	DMATDL	Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.	0x0

Table 745: I2C2_DMA_RDLR_REG (0x50020790)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	DMARDL	Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is,	0x0

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Bit	Mode	Symbol	Description	Reset
			dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.	

Table 746: I2C2_SDA_SETUP_REG (0x50020794)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x0
7:0	R/W	SDA_SETUP	SDA Setup. This register controls the amount of time delay (number of I2C clock periods) between the rising edge of SCL and SDA changing by holding SCL low when I2C block services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. It is recommended that if the required delay is 1000ns, then for an I2C frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.Writes to this register succeed only when IC_ENABLE[0] = 0.	0x64

Table 747: I2C2_ACK_GENERAL_CALL_REG (0x50020798)

Bit	Mode	Symbol	Description	Reset
15:1	-	-	Reserved	0x0
0	R/W	ACK_GEN_CALL	ACK General Call. When set to 1, I2C Ctrl responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the controller does not generate General Call interrupts. 1 = Generate ACK for a General Call 0 = Generate NACK for General Call	0x0

Table 748: I2C2_ENABLE_STATUS_REG (0x5002079C)

Bit	Mode	Symbol	Description	Reset
15:3	-	-	Reserved	0x0
2	R	SLV_RX_DATA_LOST	Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0. When read as 1, the controller is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even	0x0

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Bit	Mode	Symbol	Description	Reset
			though a data byte has been responded with a NACK. NOTE: If the remote I2C master terminates the transfer with a STOP condition before the controller has a chance to NACK a transfer, and IC_ENABLE has been set to 0, then this bit is also set to 1. When read as 0, the controller is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. NOTE: The CPU can safely read this bit when IC_EN (bit 0) is read as 0. 1 = Slave RX Data is lost 0 = Slave RX Data is not lost	
1	R	SLV_DISABLED_WHILE_BUSY	Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: (a) I2C Ctrl is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, the controller is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in I2C Ctrl (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. NOTE: If the remote I2C master terminates the transfer with a STOP condition before the the controller has a chance to NACK a transfer, and IC_ENABLE has been set to 0, then this bit will also be set to 1. When read as 0, the controller is deemed to have been disabled when there is master activity, or when the I2C bus is idle. NOTE: The CPU can safely read this bit when IC_EN (bit 0) is read as 0. 1 =Slave is disabled when it is active 0 =Slave is disabled when it is idle	0x0
0	R	IC_EN	ic_en Status. This bit always reflects the value driven on the output port ic_en. When read as 1, the controller is deemed to be in an enabled state. When read as 0, the controller is deemed completely inactive. NOTE: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLV_RX_DATA_LOST (bit 2) and SLV_DISABLED_WHILE_BUSY (bit 1). 1 = I2C enabled 0 =I2C disabled	0x0

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Table 749: I2C2_IC_FS_SPKLEN_REG (0x500207A0)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x0
7:0	R/W	I2C_FS_SPKLEN	This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.	0x1

Table 750: I2C2_IC_HS_SPKLEN_REG (0x500207A4)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	I2C_HS_SPKLEN	This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.	0x1

44.16 I3C Controller Registers

Table 751: Register map I3C

Address	Register	Description
0x50020C00	I3C_DEVICE_CTRL_REG	Device Control Register
0x50020C04	I3C_DEVICE_ADDR_REG	Device Address Register
0x50020C08	I3C_HW_CAPABILITY_REG	Hardware Capability register
0x50020C0C	I3C_COMMAND_QUEUE_PORT_REG	COMMAND_QUEUE_PORT
0x50020C10	I3C_RESPONSE_QUEUE_PORT_REG	RESPONSE_QUEUE_PORT
0x50020C14	I3C_RX_TX_DATA_PORT_REG	Receive and Transmit Data Port Register

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Address	Register	Description
0x50020C18	I3C_IBI_QUEUE_STATUS_DATA_REG	In-Band Interrupt Queue Status and Data Register
0x50020C1C	I3C_QUEUE_THLD_CTRL_REG	Queue Threshold Control Register
0x50020C20	I3C_DATA_BUFFER_THLD_CTRL_REG	Data Buffer Threshold Control Register
0x50020C24	I3C_IBI_QUEUE_CTRL_REG	IBI Queue Control Register
0x50020C30	I3C_IBI_SIR_REQ_REJECT_REG	IBI SIR Request Rejection Control Register
0x50020C34	I3C_RESET_CTRL_REG	Reset Control Register
0x50020C38	I3C_SLV_EVENT_STATUS_REG	Slave Event Status Register
0x50020C3C	I3C_INTR_STATUS_REG	Interrupt Status Register
0x50020C40	I3C_INTR_STATUS_EN_REG	Interrupt Status Enable Register
0x50020C44	I3C_INTR_SIGNAL_EN_REG	Interrupt Signal Enable Register
0x50020C48	I3C_INTR_FORCE_REG	Interrupt Force Enable Register
0x50020C4C	I3C_QUEUE_STATUS_LEVEL_REG	Queue Status Level Register
0x50020C50	I3C_DATA_BUFFER_STAT_LEVEL_REG	Data Buffer Status Level Register
0x50020C54	I3C_PRESENT_STATE_REG	Present State Register
0x50020C5C	I3C_DEVICE_ADDR_TABLE_PTR_REG	Pointer for Device Address Table Registers
0x50020C60	I3C_DEV_CHAR_TABLE_POINTER_REG	Pointer for Device Characteristics Table
0x50020C6C	I3C_VENDOR_SPECIFIC_REG_PTR_REG	Pointer for Vendor specific Registers
0x50020CB0	I3C_DEVICE_CTRL_EXTENDED_REG	Device Control Extended Register
0x50020CB4	I3C_SCL_I3C_OD_TIMING_REG	SCL I3C Open Drain Timing Register
0x50020CB8	I3C_SCL_I3C_PP_TIMING_REG	SCL I3C Push Pull Timing Register
0x50020CBC	I3C_SCL_I2C_FM_TIMING_REG	SCL I2C Fast Mode Timing Register
0x50020CC0	I3C_SCL_I2C_FMP_TIMING_REG	SCL I2C Fast Mode Plus Timing Register
0x50020CC8	I3C_SCL_EXT_LCNT_TIMING_REG	SCL Extended Low Count Timing Register
0x50020CCC	I3C_SCL_EXT_TERMN_LCNT_TIME_REG	SCL Termination Bit Low count Timing Register

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Address	Register	Description
0x50020CD0	I3C_SDA_HOLD_DLY_TIMING_REG	SDA Hold Delay Timing Register
0x50020CD4	I3C_BUS_FREE_AVAIL_TIMING_REG	Bus Free Timing Register
0x50020CE0	I3C_VER_ID_REG	I3C Version ID Register
0x50020CE4	I3C_VER_TYPE_REG	I3C Version Type Register
0x50020CE8	I3C_QUEUE_SIZE_CAPABILITY_REG	I3C Queue Size Capability Register
0x50020E00	I3C_DEV_CHAR_TABLE1_LOC1_REG	Device Characteristic Table Location-1 of Device1
0x50020E04	I3C_DEV_CHAR_TABLE1_LOC2_REG	Device Characteristic Table Location-2 of Device1
0x50020E08	I3C_DEV_CHAR_TABLE1_LOC3_REG	Device Characteristic Table Location-3 of Device1
0x50020E0C	I3C_DEV_CHAR_TABLE1_LOC4_REG	Device Characteristic Table Location-4 of Device1
0x50020E10	I3C_DEV_CHAR_TABLE2_LOC1_REG	Device Characteristic Table Location-1 of Device2
0x50020E14	I3C_DEV_CHAR_TABLE2_LOC2_REG	Device Characteristic Table Location-2 of Device2
0x50020E18	I3C_DEV_CHAR_TABLE2_LOC3_REG	Device Characteristic Table Location-3 of Device2
0x50020E1C	I3C_DEV_CHAR_TABLE2_LOC4_REG	Device Characteristic Table Location-4 of Device2
0x50020E20	I3C_DEV_CHAR_TABLE3_LOC1_REG	Device Characteristic Table Location-1 of Device3
0x50020E24	I3C_DEV_CHAR_TABLE3_LOC2_REG	Device Characteristic Table Location-2 of Device3
0x50020E28	I3C_DEV_CHAR_TABLE3_LOC3_REG	Device Characteristic Table Location-3 of Device3
0x50020E2C	I3C_DEV_CHAR_TABLE3_LOC4_REG	Device Characteristic Table Location-4 of Device3
0x50020E30	I3C_DEV_CHAR_TABLE4_LOC1_REG	Device Characteristic Table Location-1 of Device4
0x50020E34	I3C_DEV_CHAR_TABLE4_LOC2_REG	Device Characteristic Table Location-2 of Device4
0x50020E38	I3C_DEV_CHAR_TABLE4_LOC3_REG	Device Characteristic Table Location-3 of Device4
0x50020E3C	I3C_DEV_CHAR_TABLE4_LOC4_REG	Device Characteristic Table Location-4 of Device4
0x50020E40	I3C_DEV_CHAR_TABLE5_LOC1_REG	Device Characteristic Table Location-1 of Device5
0x50020E44	I3C_DEV_CHAR_TABLE5_LOC2_REG	Device Characteristic Table Location-2 of Device5
0x50020E48	I3C_DEV_CHAR_TABLE5_LOC3_REG	Device Characteristic Table Location-3 of Device5
0x50020E4C	I3C_DEV_CHAR_TABLE5_LOC4_REG	Device Characteristic Table Location-4 of Device5

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Address	Register	Description
0x50020E50	I3C_DEV_CHAR_TABLE6_LOC1_REG	Device Characteristic Table Location-1 of Device6
0x50020E54	I3C_DEV_CHAR_TABLE6_LOC2_REG	Device Characteristic Table Location-2 of Device6
0x50020E58	I3C_DEV_CHAR_TABLE6_LOC3_REG	Device Characteristic Table Location-3 of Device6
0x50020E5C	I3C_DEV_CHAR_TABLE6_LOC4_REG	Device Characteristic Table Location-4 of Device6
0x50020E60	I3C_DEV_CHAR_TABLE7_LOC1_REG	Device Characteristic Table Location-1 of Device7
0x50020E64	I3C_DEV_CHAR_TABLE7_LOC2_REG	Device Characteristic Table Location-2 of Device7
0x50020E68	I3C_DEV_CHAR_TABLE7_LOC3_REG	Device Characteristic Table Location-3 of Device7
0x50020E6C	I3C_DEV_CHAR_TABLE7_LOC4_REG	Device Characteristic Table Location-4 of Device7
0x50020E70	I3C_DEV_CHAR_TABLE8_LOC1_REG	Device Characteristic Table Location-1 of Device8
0x50020E74	I3C_DEV_CHAR_TABLE8_LOC2_REG	Device Characteristic Table Location-2 of Device8
0x50020E78	I3C_DEV_CHAR_TABLE8_LOC3_REG	Device Characteristic Table Location-3 of Device8
0x50020E7C	I3C_DEV_CHAR_TABLE8_LOC4_REG	Device Characteristic Table Location-4 of Device8
0x50020E80	I3C_DEV_ADDR_TABLE_LOC1_REG	Device Address Table of Device1
0x50020E84	I3C_DEV_ADDR_TABLE_LOC2_REG	Device Address Table of Device2
0x50020E88	I3C_DEV_ADDR_TABLE_LOC3_REG	Device Address Table of Device3
0x50020E8C	I3C_DEV_ADDR_TABLE_LOC4_REG	Device Address Table of Device4
0x50020E90	I3C_DEV_ADDR_TABLE_LOC5_REG	Device Address Table of Device5
0x50020E94	I3C_DEV_ADDR_TABLE_LOC6_REG	Device Address Table of Device6
0x50020E98	I3C_DEV_ADDR_TABLE_LOC7_REG	Device Address Table of Device7
0x50020E9C	I3C_DEV_ADDR_TABLE_LOC8_REG	Device Address Table of Device8

Table 752: I3C_DEVICE_CTRL_REG (0x50020C00)

Bit	Mode	Symbol	Description	Reset
31	R/W	ENABLE	Controls whether or not i3c is enabled. 1: Enables the i3c controller.	0x0

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Bit	Mode	Symbol	Description	Reset
			0: Disables the i3c controller. In Master mode of operation, software can Disable i3c while it is active. However, the controller may not get Disabled immediately and will be 'Disabled' after commands in the Command queue (if any) are executed leading to a STOP condition on the bus and Master FSM is in IDLE state (as indicated by PRESENT_STATE Register).	
30	R/W	RESUME	i3c Resume. This bit is used to resume the Controller after it goes to Halt state. In the master mode of operation the controller goes to the halt state (as indicated in PRESENT_STATE Register) due to any type of error in the transfer (the type of error is indicated by ERR_STATUS field in the RESPONSE_QUEUE_PORT register). After the controller has gone to halt state, the application has to write 1'b1 to this bit to resume the controller. This bit is auto-cleared once the controller resumes the transfers by initiating the next command.	0x0
29	R/W	ABORT	i3c Abort. This bit is used in master mode of operation. This bit allows the controller to relinquish the I3C Bus before completing the issued transfer. In response to an ABORT request, the controller issues the STOP condition after the complete data byte is transferred or received. This bit is auto-cleared once the transfer is aborted and controller issues a "Transfer Abort" interrupt.	0x0
28	R/W	DMA_ENABLE_I3C	DMA Handshake Interface Enable. This bit is used to enable or disable the DMA Handshaking interface and is applicable to both Master and Slave mode of operation. 1: Enables the DMA handshake control to interact with external DMA. 0: The DMA handshake control has no significance.	0x0

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Bit	Mode	Symbol	Description	Reset
27:9	R	-	Reserved	0x0
8	R/W	HOT_JOIN_CTRL	Hot-Join Ack/Nack Control This bit is used in master mode of operation. This bit acts as global control to ACK/NACK the Hot-Join Request from the devices. The i3c Master will ACK/NACK the Hot-Join request from other devices connected on the I3C Bus, based on programming of this bit. 0: ACK the Hot-join request. 1: NACK and send broadcast CCC to disable Hot-join. Values: 0x0 (DISABLED): Ack Hot-Join requests 0x1 (ENABLED): Nack and auto-disable Hot-Join request	0x1
7	R/W	I2C_SLAVE_PRESENT	I2C Slave Present This bit is used in master mode of operation. This Bit indicates whether any Legacy I2C Devices are present in the system. In HDR mode, this field is used to select TSL over TSP in mixed bus configuration. Values: 0x0 (DISABLED): I2C Slave not present 0x1 (ENABLED): I2C Slave present	0x1
6:1	R	-	Reserved	0x0
0	R/W	IBA_INCLUDE	I3C Broadcast Address include. This bit is used in master mode of operation. This bit is used to include I3C broadcast address (0x7E) for private transfer. Note: If I3C broadcast address is not included for the private transfers, In-band Interrupts (IBI) driven from Slaves may not win address arbitration. Hence, the IBIs will get delayed. Values:	0x1

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Bit	Mode	Symbol	Description	Reset
			0x0 (NOT_INCLUDED): I3C Broadcast Address is not included for Private Transfers 0x1 (INCLUDED): I3C Broadcast Address is included for Private Transfers	

Table 753: I3C_DEVICE_ADDR_REG (0x50020C04)

Bit	Mode	Symbol	Description	Reset
31	R/W	DYNAMIC_ADDR_VALID	Dynamic Address Valid This bit is used to control whether the DYNAMIC_ADDR is valid or not. In I3C Main Master mode, the user sets this bit to 1 as it self-assigns its dynamic address. In all other operation modes, the Controller sets this bit to 1 when Main Master assigns the Dynamic address during ENTDAA or SETDASA mechanism. Values: 0x0 (INVALID): Dynamic Address is invalid 0x1 (VALID): Dynamic Address is valid	0x1
30:23	R	-	Reserved	0x0
22:16	R/W	DYNAMIC_ADDR	Device Dynamic Address. This field is used to program the Device Dynamic Address. The Controller uses this address for I3C transfers. In Main Master mode, the user/application has to program the Dynamic Address through the Slave interface as it self-assigns its Dynamic Address. In all other modes, the Main Master assigns this address during ENTDAA or SETDASA mechanism.	0x0
15:0	R	-	Reserved	0x0

Table 754: I3C_HW_CAPABILITY_REG (0x50020C08)

Bit	Mode	Symbol	Description	Reset
31:20	R	-	Reserved	0x0
19	R	SLV_IBI_CAP	Reflects the IC_SLV_IBI Configurable Parameter.	0x0

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Bit	Mode	Symbol	Description	Reset
			Specifies slave's capability to initiate slave interrupt requests.	
18	R	SLV_HJ_CAP	Reflects the IC_SLV_HJ Configurable Parameter. Specifies slave's capability to initiate Hot-join request.	0x0
17	R	DMA_EN	Reflects the IC_HAS_DMA Configurable Parameter. Specifies whether controller is configured to have DMA handshaking interface.	0x1
16:11	R	HDR_TX_CLOCK_PERIOD	Reflects the IC_HDR_TX_CLK_PERIOD Configurable Parameter.	0x28
10:5	R	CLOCK_PERIOD	Reflects the IC_CLK_PERIOD Configurable Parameter	0x8
4	R	HDR_TS_EN	Reflects the IC_SPEED_HDR_TS Configurable Parameter. Specifies the Controllers capability to perform HDR-TS transfers. 0 : HDR-TS not supported 1 : HDR-TS supported	0x0
3	R	HDR_DDR_EN	Reflects the IC_SPEED_HDR_DDR Configurable Parameter. Specifies the Controllers capability to perform HDR-DDR transfers. 0 : HDR-DDR not supported 1 : HDR-DDR supported	0x0
2:0	R	DEVICE_ROLE_CONFIG	Reflects the IC_DEVICE_ROLE Configurable Parameter. Specifies the configured role of i3c controller 1 : Master Only 2 : Programmable Master-Slave 3 : Secondary Master 4 : Slave Only	0x1

Table 755: I3C_COMMAND_QUEUE_PORT_REG (0x50020C0C)

Bit	Mode	Symbol	Description	Reset
31:0	W	COMMAND	32 bit command	0x0

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Table 756: I3C_RESPONSE_QUEUE_PORT_REG (0x50020C10)

Bit	Mode	Symbol	Description	Reset
31:0	R	RESPONSE	32 bit Response	0x0

Table 757: I3C_RX_TX_DATA_PORT_REG (0x50020C14)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	RX_TX_DATA_PORT	Receive and Transmit Data Port. (Merged in Doxbox) The Receive data port is mapped to the Rx-Data Buffer. The Receive data is always packed in 4-byte aligned data words and stored in the Rx-Data Buffer. If the command length is not aligned to the 4-bytes, then the additional data bytes have to be ignored.	0x0

Table 758: I3C_IBI_QUEUE_STATUS_DATA_REG (0x50020C18)

Bit	Mode	Symbol	Description	Reset
31:28	R	IBI_STS	IBI Received Status. Defines the master response for IBI received. 4'b0xxx: Responded with ACK 4'b1xxx: Responded with NACK Others : RESERVED	0x0
27:16	R	-	Reserved	0x0
15:8	R	IBI_ID	IBI Identifier. The byte received after START which includes the address and the R/W bit. Device address and R/W bit in case of Slave Interrupt or Master Request. Hot-Join ID and R/W bit in case of Hot-Join IBI.	0x0
7:0	R	DATA_LENGTH	In-Band Interrupt data length. This field represents the length of data received along with the IBI, in bytes.	0x0

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Table 759: I3C_QUEUE_THLD_CTRL_REG (0x50020C1C)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	IBI_STATUS_THLD	In-Band Interrupt Status Threshold Value. Every In Band Interrupt received (with or without data) by I3C controller generates an IBI status. This field controls the number of IBI status entries (or greater) in the IBI queue that trigger the IBI_THLD_STAT interrupt. The valid range is 0 to 7. The software shall program only valid values. A value of 0 sets the threshold for 1 entry, and a value of N sets the threshold for N+1 entries.	0x1
23:16	R	-	Reserved	0x0
15:8	R/W	RESP_BUF_THLD	Response Buffer Threshold Value. Controls the number of entries (or greater) in the Response Queue that trigger the RESP_READY_STAT_INTR interrupt. The valid range is 0 to 3. The software shall program only valid values. A value of 0 sets the threshold for 1 entry, and a value of N sets the threshold for N+1 entries.	0x1
7:0	R/W	CMD_EMPTY_BUF_THLD	Command Buffer Empty Threshold Value. Controls the number of empty locations (or greater) in the Command Queue that trigger CMD_QUEUE_READY_STAT interrupt. The valid range is 0 to 7. The software shall program only valid values. Value of N ranging from 1 to 7 sets the threshold to N empty locations and a value of 0 sets the threshold to indicate that the queue is completely empty.	0x1

Table 760: I3C_DATA_BUFFER_THLD_CTRL_REG (0x50020C20)

Bit	Mode	Symbol	Description	Reset
31:27	R	-	Reserved	0x0
26:24	R/W	RX_START_THLD	Receive Start Threshold Value. In master mode of operation when the controller is set up to initiate a read transfer, it waits until either one of the conditions are met before it initiates the read transfer on the I3C Interface. Data length (as specified in the command) number of locations are empty in the Receive FIFO.	0x3

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Bit	Mode	Symbol	Description	Reset
			Threshold number of locations (or more) are empty in the Receive FIFO. The supported values for RX_START_THLD are: 000 - 1 001 - 4 010 - 8 011 - 16 100 - 32 101 - 64	
23:19	R	-	Reserved	0x0
18:16	R/W	TX_START_THLD	Transfer Start Threshold Value. In master mode of operation when the controller is set up to initiate a write transfer, it waits until either one of the following conditions are met before it initiates the write transfer on the I3C Interface. Data length (as specified in the command) number of locations are filled in the Transmit FIFO Threshold number of entries (or more) are available in the Transmit FIFO The supported values for TX_START_THLD are: 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64	0x3
15:11	R	-	Reserved	0x0
10:8	R/W	RX_BUF_THLD	Receive Buffer Threshold Value. This field controls the number of entries (or above) in the Receive FIFO that trigger the RX_THLD_STAT interrupt. If the programmed value is greater than the buffer depth, then threshold will be set to 32. The supported values for RX_BUF_THLD are 000: 1 001: 4 010: 8 011: 16 100: 32	0x3

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Bit	Mode	Symbol	Description	Reset
			101: 64	
7:3	R	-	Reserved	0x0
2:0	R/W	TX_EMPTY_BUF_THLD	Transmit Buffer Threshold Value. This field controls the number of empty locations (or above) in the Transmit FIFO that trigger the TX_THLD_STAT interrupt. If the programmed value is greater than the buffer depth, then threshold will be set to 32. The supported values for TX_BUF_THLD are 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64	0x3

Table 761: I3C_IBI_QUEUE_CTRL_REG (0x50020C24)

Bit	Mode	Symbol	Description	Reset
31:4	R	-	Reserved	0x0
3	R/W	NOTIFY_SIR_REJECTED	Notify Rejected Slave Interrupt Request Control. This bit is used to suppress reporting to the application about SIR request rejected. 0: Suppress passing the IBI Status to the IBI FIFO (hence not notifying the application) when a Slave Interrupt Request is NACKed and auto-disabled based on the IBI_SIR_REQ_REJECT Register. 1: Writes IBI Status to the IBI FIFO (hence notifying the application) when a Slave Interrupt Request is NACKed and auto-disabled based on the IBI_SIR_REQ_REJECT Register. Values: 0x0 (DISABLED): Notify SIR Rejected Disable 0x1 (ENABLED): Notify SIR Rejected Enable	0x0
2:1	R	-	Reserved	0x0
0	R/W	NOTIFY_HJ_REJECTED	Notify Rejected Hot-Join Control. This bit is used to suppress reporting to the application about Hot-Join request rejected (NACK and Auto Disable).	0x0

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Bit	Mode	Symbol	Description	Reset
			0: Suppress passing the IBI Status to the IBI FIFO (hence not notifying the application) when a HJ Request is NACKed and auto-disabled based on the DEVICE_CTRL.HOT_JOIN_CTRL. 1: Writes IBI Status to the IBI FIFO (hence notifying the application) when a HJ Request is NACKed and auto-disabled based on the DEVICE_CTRL.HOT_JOIN_CTRL. Values: 0x0 (DISABLED): Notify Hot-Join Rejected Disable 0x1 (ENABLED): Notify Hot-Join Rejected Enable	

Table 762: I3C_IBI_SIR_REQ_REJECT_REG (0x50020C30)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	SIR_REQ_REJECT	In-band Slave Interrupt Request Reject. The application of the i3c can decide whether to send ACK or NACK for a Slave request received from any I3C device. A device specific response control bit is provided to select the response option. Master will ACK/NACK the Master Request based on programming of control bit, corresponding to the interrupting device. 0 - ACK the SIR Request 1 - NACK and send directed auto disable CCC	0x0

Table 763: I3C_RESET_CTRL_REG (0x50020C34)

Bit	Mode	Symbol	Description	Reset
31:6	R	-	Reserved	0x0
5	R/W	IBI_QUEUE_RST	IBI Queue Software Reset. This bit is only used in master mode of operation. Write 1'b1 to this bit to exercise IBI Queue reset This bit will be cleared automatically once the IBI Queue reset is completed.	0x0
4	R/W	RX_FIFO_RST	Receive Buffer Software Reset.	0x0

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Bit	Mode	Symbol	Description	Reset
			Write 1'b1 to this bit to exercise Receive Buffer reset. This bit will be cleared automatically once the Receive buffer reset is completed.	
3	R/W	TX_FIFO_RST	Transmit Buffer Software Reset. Write 1'b1 to this bit to exercise Transmit Buffer reset. This bit will be cleared automatically once the Transmit Buffer reset is completed.	0x0
2	R/W	RESP_QUEUE_RST	Response Queue Software Reset. Write 1'b1 to this bit to exercise Response Queue reset. This bit will be cleared automatically once the Response Queue reset is completed.	0x0
1	R/W	CMD_QUEUE_RST	Command Queue Software Reset. Write 1'b1 to this bit to exercise Command Queue reset. This bit will the cleared automatically once the Command Queue reset is completed.	0x0
0	R/W	SOFT_RST	Core Software Reset. Write 1'b1 to this bit to exercise software reset. This will reset all Buffers - Receive, Transmit, Command and Response This bit will be cleared automatically once the core reset is completed.	0x0

Table 764: I3C_SLV_EVENT_STATUS_REG (0x50020C38)

Bit	Mode	Symbol	Description	Reset
31:8	R	-	Reserved	0x0
7	RW1C	MWL_UPDATED	MWL Updated Status. This bit indicates a SETMWL CCC is received by the slave. The updated MWL value can be read from SLV_MAX_LEN register. This status can be cleared by writing 1'b1 to this field after reading the updated MWL.	0x0
6	RW1C	MRL_UPDATED	MRL Updated Status. This bit indicates a SETMRL CCC is received by the slave. The updated MRL value can be read from SLV_MAX_LEN register. This status can be cleared by writing 1'b1 to this field after reading the updated MRL.	0x0
5:4	R	ACTIVITY_STATE	Activity State Status. ENTAS0 - 00	0x0

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Bit	Mode	Symbol	Description	Reset
			ENTAS1 - 01 ENTAS2 - 10 ENTAS3 - 11 This bit reflects the Activity State of slave set by the Master.	
3:0	R	-	Reserved	0x0

Table 765: I3C_INTR_STATUS_REG (0x50020C3C)

Bit	Mode	Symbol	Description	Reset
31:10	R	-	Reserved	0x0
9	RW1C	TRANSFER_ERR_STS	Transfer Error Status. This interrupt is generated if any error occurs during transfer. The error type will be specified in the response packet associated with the command (in ERR_STATUS field of RESPONSE_QUEUE_PORT register). This bit can be cleared by writing 1'b1.	0x0
8:6	R	-	Reserved	0x0
5	RW1C	TRANSFER_ABORT_STS	Transfer Abort Status. This field is used only in master mode of operation. This interrupt is generated if transfer is aborted. This interrupt can be cleared by writing 1'b1.	0x0
4	R	RESP_READY_STS	Response Queue Ready Status. This interrupt is generated when number of entries in response queue is greater than or equal to threshold value specified by RESP_BUF_THLD field in QUEUE_THLD_CTRL register. This interrupt will be cleared automatically when number of entries in response buffer is less than threshold value specified.	0x0
3	R	CMD_QUEUE_READY_STS	Command Queue Ready. This interrupt is generated when number of empty locations in command queue is greater than or equal to threshold value specified by CMD_EMPTY_BUF_THLD field in QUEUE_THLD_CTRL register. This interrupt will be cleared automatically when number of empty	0x0

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Bit	Mode	Symbol	Description	Reset
			locations in command buffer is less than threshold value specified.	
2	R	IBI_THLD_STS	IBI Buffer Threshold Status. This field is only used in master mode of operation This interrupt is generated when number of entries in IBI buffer is greater than or equal to threshold value specified by IBI_BUF_THLD field in QUEUE_THLD_CTRL register. This interrupt will be cleared automatically when number of entries in IBI buffer is less than threshold value specified.	0x0
1	R	RX_THLD_STS	Receive Buffer Threshold Status. This interrupt is generated when number of entries in receive buffer is greater than or equal to threshold value specified by RX_BUF_THLD field in DATA_BUFFER_THLD_CTRL register. This interrupt will be cleared automatically when number of entries in receive buffer is less than threshold value specified.	0x0
0	R	TX_THLD_STS	Transmit Buffer Threshold Status. This interrupt is generated when number of empty locations in transmit buffer is greater than or equal to threshold value specified by TX_EMPTY_BUF_THLD field in DATA_BUFFER_THLD_CTRL register. This interrupt will be cleared automatically when number of empty locations in transmit buffer is less than threshold value specified.	0x0

Table 766: I3C_INTR_STATUS_EN_REG (0x50020C40)

Bit	Mode	Symbol	Description	Reset
31:10	R	-	Reserved	0x0
9	R/W	TRANSFER_ERR_STS_EN	Transfer Error Status Enable	0x0
8:6	R	-	Reserved	0x0
5	R/W	TRANSFER_ABORT_STS_EN	Transfer Abort Status Enable. This field is used only in master mode of operation.	0x0
4	R/W	RESP_READY_STS_EN	Response Queue Ready Status Enable	0x0
3	R/W	CMD_QUEUE_READY_STS_EN	Command Queue Ready Status Enable	0x0
2	R/W	IBI_THLD_STS_EN	IBI Buffer Threshold Status Enable.	0x0

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Bit	Mode	Symbol	Description	Reset
			This field is used only in master mode of operation.	
1	R/W	RX_THLD_STS_EN	Receive Buffer Threshold Status Enable	0x0
0	R/W	TX_THLD_STS_EN	Transmit Buffer Threshold Status Enable	0x0

Table 767: I3C_INTR_SIGNAL_EN_REG (0x50020C44)

Bit	Mode	Symbol	Description	Reset
31:10	R	-	Reserved	0x0
9	R/W	TRANSFER_ERR_SIGNAL_EN	Transfer Error Signal Enable	0x0
8:6	R	-	Reserved	0x0
5	R/W	TRANSFER_ABORT_SIGNAL_EN	Transfer Abort Signal Enable. This field is used only in master mode of operation.	0x0
4	R/W	RESP_READY_SIGNAL_EN	Response Queue Ready Signal Enable	0x0
3	R/W	CMD_QUEUE_READY_SIGNAL_EN	Command Queue Ready Signal Enable	0x0
2	R/W	IBI_THLD_SIGNAL_EN	IBI Buffer Threshold Signal Enable. This field is used only in master mode of operation.	0x0
1	R/W	RX_THLD_SIGNAL_EN	Receive Buffer Threshold Signal Enable	0x0
0	R/W	TX_THLD_SIGNAL_EN	Transmit Buffer Threshold Signal Enable. *Note: For the deassertion of the interrupt, first the *SIGNAL_EN bitfield should be cleared and then the *STATUS_EN one, otherwise is not working. This comment applies for the rest bitfields of this register	0x0

Table 768: I3C_INTR_FORCE_REG (0x50020C48)

Bit	Mode	Symbol	Description	Reset
31:10	R	-	Reserved	0x0
9	W	TRANSFER_ERR_FORCE_EN	Transfer Error Force Enable	0x0
8:6	R	-	Reserved	0x0
5	W	TRANSFER_ABORT_FORCE_EN	Transfer Abort Force Enable. This field is used only in master mode of operation.	0x0

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Bit	Mode	Symbol	Description	Reset
4	W	RESP_READY_FORCE_EN	Response Queue Ready Force Enable	0x0
3	W	CMD_QUEUE_READY_FORCE_EN	Command Queue Ready Force Enable	0x0
2	W	IBI_THLD_FORCE_EN	IBI Buffer Threshold Force Enable. This field is used only in master mode of operation.	0x0
1	W	RX_THLD_FORCE_EN	Receive Buffer Threshold Force Enable	0x0
0	W	TX_THLD_FORCE_EN	Transmit Buffer Threshold Force Enable.	0x0

Table 769: I3C_QUEUE_STATUS_LEVEL_REG (0x50020C4C)

Bit	Mode	Symbol	Description	Reset
31:29	R	-	Reserved	0x0
28:24	R	IBI_STS_CNT	IBI Buffer Status Count. Contains the number of IBI status entries in the IBI Buffer. This field is used in master mode of operation.	0x0
23:16	R	IBI_BUF_BLR	IBI Buffer Level Value. Contains the number of valid entries in the IBI Buffer. This field is used in master mode of operation.	0x0
15:8	R	RESP_BUF_BLR	Response Buffer Level Value. Contains the number of valid data entries in the response Buffer.	0x0
7:0	R	CMD_QUEUE_EMPTY_LOC	Command Queue Empty Locations. Contains the number of empty locations in the command Buffer.	0x8

Table 770: I3C_DATA_BUFFER_STAT_LEVEL_REG (0x50020C50)

Bit	Mode	Symbol	Description	Reset
31:24	R	-	Reserved	0x0
23:16	R	RX_BUF_BLR	Receive Buffer Level Value.	0x0

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Bit	Mode	Symbol	Description	Reset
			Contains the number of valid data entries in the receive Buffer.	
15:8	R	-	Reserved	0x0
7:0	R	TX_BUF_EMPTY_LOC	Transmit Buffer Empty Level Value. Contains the number of empty locations in the transmit Buffer.	0x20

Table 771: I3C_PRESENT_STATE_REG (0x50020C54)

Bit	Mode	Symbol	Description	Reset
31:29	R	-	Reserved	0x0
28	R	MASTER_IDLE	This field reflects whether the Master Controller is in Idle state or not. This bit will set when all the Queues(Command , Response, IBI) and Buffers(Transmit and Receive) are empty along with the Master State machine is in Idle state. Values: 0x0 (MST_NOT_IDLE): Master Controller is not in IDLE State 0x1 (MST_IDLE): Master Controller is in IDLE State.	0x1
27:24	R	CMD_TID	This field reflects the Transaction-ID of the current executing command.	0x0
23:22	R	-	Reserved	0x0
21:16	R	CM_TFR_ST_STS	Current Master Transfer State Status. Indicates the state of current transfer currently executing by the i3c controller. This is valid in Master mode only. 6'h0: IDLE (Controller is Idle state, waiting for commands from application or Slave initated In-band Interrupt) 6'h1: START Generation State. 6'h2: RESTART Generation State. 6'h3: STOP Generation State. 6'h4: START Hold Generation for the Slave Initiated START State. 6'h5: Broadcast Write Address Header(7'h7E,W) Generation State. 6'h6: Broadcast Read Address Header(7'h7E,R) Generation State. 6'h7: Dynamic Address Assignment State. 6'h8: Slave Address Generation State. 6'hB: CCC Byte Generation State. 6'hC: HDR Command Generation State.	0x0

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Bit	Mode	Symbol	Description	Reset
			6'hD: Write Data Transfer State. 6'hE: Read Data Transfer State. 6'hF: In-Band Interrupt(SIR) Read Data State. 6'h10: In-Band Interrupt Auto-Disable State 6'h11: HDR-DDR CRC Data Generation/Receive State. 6'h12: Clock Extension State. 6'h13: Halt State.	
15:14	R	-	Reserved	0x0
13:8	R	CM_TFR_STS	Transfer Type Status. Indicates the type of transfer currently executing by the i3c controller. In Master mode of operation : 6'h0: IDLE (Controller is in Idle state, waiting for commands from application or Slave initated In-band Interrupt) 6'h1: Broadcast CCC Write Transfer. 6'h2: Directed CCC Write Transfer. 6'h3: Directed CCC Read Transfer. 6'h4: ENTDAA Address Assignment Transfer. 6'h5: SETDASA Address Assignment Transfer. 6'h6: Private I3C SDR Write Transfer. 6'h7: Private I3C SDR Read Transfer. 6'h8: Private I2C SDR Write Transfer. 6'h9: Private I2C SDR Read Transfer. 6'hA: Private HDR Ternary Symbol(TS) Write Transfer. 6'hB: Private HDR Ternary Symbol(TS) Read Transfer. 6'hC: Private HDR Double-Data Rate(DDR) Write Transfer. 6'hD: Private HDR Double-Data Rate(DDR) Read Transfer. 6'hE: Servicing In-Band Interrupt Transfer. 6'hF: Halt state (Controller is in Halt State, waiting for the application to resume through DEVICE_CTRL Register)	0x0
7:3	R	-	Reserved	0x0
2	R	CURRENT_MASTER	This Bit is used to check whether the Master is Current Master or not. The Current Master is the Master that owns the SCL line. If this bit is set to 0, the Master is not Current Master and requires to request and the ownership before initiating any transfer on the line.	0x0

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Bit	Mode	Symbol	Description	Reset
			If this bit is set to 1, the Master is the Current Master and can initate the transfers on the line. 0: Master is not Current Master 1: Master is Current Master	
1	R	SDA_LINE_SIGNAL_LEVEL	This bit is used to check the SDA line level to recover from errors and for debugging. This bit reflects the value of synchronized sda_in_a signal. This is valid in Master mode only.	0x1
0	R	SCL_LINE_SIGNAL_LEVEL	This bit is used to check the SCL line level to recover from errors and for debugging. This bit reflects the value of synchronized scl_in_a signal. This is valid in Master mode only	0x1

Table 772: I3C_DEVICE_ADDR_TABLE_PTR_REG (0x50020C5C)

Bit	Mode	Symbol	Description	Reset
31:16	R	DEV_ADDR_TABLE_DEPTH	Depth of Device Address Table	0x8
15:0	R	P_DEV_ADDR_TABLE_START_ADDR	Start Address of Device Address Table.	0x280

Table 773: I3C_DEV_CHAR_TABLE_POINTER_REG (0x50020C60)

Bit	Mode	Symbol	Description	Reset
31:22	R	-	Reserved	0x0
21:19	R/W	PRESENT_DEV_CHAR_TABLE_INDX	Current index of Device Characteristics Table. This field returns the current location of Device Characteristics Table index. Initially, this index points to 0. Once the complete characteristics information of a Slave device is written into Device Characteristics Table during ENTDAA, this index increments by 1. The first winning device information is stored in Device Characteristics Table index 0, the second winning device information in index 1, and so on. If required, this index can be used to override the location, where characteristic information of Slave devices on the I3C bus are written during ENTDAA. Hence, this field is useful only if the device is Current Master. During DEFSLV CCC, the index always starts from 0. In Non-current Master, this field is always read-only.	0x0

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Bit	Mode	Symbol	Description	Reset
18:12	R	DEV_CHAR_TABLE_DEPTH	Depth of Device Characteristics Table	0x20
11:0	R	P_DEV_CHAR_TABLE_START_ADDR	Start Address of Device Characteristics Table.	0x200

Table 774: I3C_VENDOR_SPECIFIC_REG_PTR_REG (0x50020C6C)

Bit	Mode	Symbol	Description	Reset
31:16	R	-	Reserved	0x0
15:0	R	P_VENDOR_REG_START_ADDR	Start Address of Vendor specific registers.	0xB0

Table 775: I3C_DEVICE_CTRL_EXTENDED_REG (0x50020CB0)

Bit	Mode	Symbol	Description	Reset
31:2	R	-	Reserved	0x0
1:0	R/W	DEV_OPERATION_MODE	This bit is used to select the Device Operation Mode before the controller is enabled. This field shall be written only when the i3c is disabled. 0: Master 1: Slave 2: Reserved 3: Reserved This field will be automatically updated by the controller once the role change happens in secondary master mode..	0x0

Table 776: I3C_SCL_I3C_OD_TIMING_REG (0x50020CB4)

Bit	Mode	Symbol	Description	Reset
31:24	R	-	Reserved	0x0
23:16	R/W	I3C_OD_HCNT	I3C Open Drain High Count. SCL open-drain High count (I3C) for I3C transfers targeted to I3C devices.	0xA
15:8	R	-	Reserved	0x0
7:0	R/W	I3C_OD_LCNT	I3C Open Drain Low Count. SCL Open-drain low count for I3C transfers targeted to I3C devices.	0x10

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Table 777: I3C_SCL_I3C_PP_TIMING_REG (0x50020CB8)

Bit	Mode	Symbol	Description	Reset
31:24	R	-	Reserved	0x0
23:16	R/W	I3C_PP_HCNT	I3C Push Pull High Count. SCL push-pull High count for I3C transfers targeted to I3C devices.	0xA
15:8	R	-	Reserved	0x0
7:0	R/W	I3C_PP_LCNT	I3C Push Pull Low Count. SCL Push-pull low count for I3C transfers targeted to I3C devices.	0xA

Table 778: I3C_SCL_I2C_FM_TIMING_REG (0x50020CBC)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	I2C_FM_HCNT	I2C Fast Mode High Count The SCL open-drain high count timing for I2C fast mode transfers.	0x10
15:0	R/W	I2C_FM_LCNT	I2C Fast Mode Low Count The SCL open-drain low count timing for I2C fast mode transfers.	0x10

Table 779: I3C_SCL_I2C_FMP_TIMING_REG (0x50020CC0)

Bit	Mode	Symbol	Description	Reset
31:24	R	-	Reserved	0x0
23:16	R/W	I2C_FMP_HCNT	I2C Fast Mode Plus High Count The SCL open-drain high count timing for I2C fast mode transfers.	0x10
15:0	R/W	I2C_FMP_LCNT	I2C Fast Mode Plus Low Count The SCL open-drain low count timing for I2C fast mode transfers.	0x10

Table 780: I3C_SCL_EXT_LCNT_TIMING_REG (0x50020CC8)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	I3C_EXT_LCNT_4	I3C Extended Low Count Register 4	0x20

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Bit	Mode	Symbol	Description	Reset
			SDR4 uses this register field for data transfer.	
23:16	R/W	I3C_EXT_LCNT_3	I3C Extended Low Count Register 3 SDR3 uses this register field for data transfer.	0x20
15:8	R/W	I3C_EXT_LCNT_2	I3C Extended Low Count Register 2 SDR2 uses this register field for data transfer.	0x20
7:0	R/W	I3C_EXT_LCNT_1	I3C Extended Low Count Register 1 SDR1 uses this register field for data transfer.	0x20

Table 781: I3C_SCL_EXT_TERMN_LCNT_TIME_REG (0x50020CCC)

Bit	Mode	Symbol	Description	Reset
31:4	R	-	Reserved	0x0
3:0	R/W	I3C_EXT_TERMN_LCNT	I3C Read Termination Bit Low count. Extended I3C Read Termination Bit low count for I3C Read transfers. Effective Termination-Bit Low Period is derived based on the SDR speed as shown below SDR0 speed: I3C_PP_LCNT + I3C_EXT_TERMN_LCNT SDR1 speed: I3C_EXT_LCNT_1 + I3C_EXT_TERMN_LCNT SDR2 speed: I3C_EXT_LCNT_2 + I3C_EXT_TERMN_LCNT SDR3 speed: I3C_EXT_LCNT_3 + I3C_EXT_TERMN_LCNT SDR4 speed: I3C_EXT_LCNT_4 + I3C_EXT_TERMN_LCNT	0x0

Table 782: I3C_SDA_HOLD_DLY_TIMING_REG (0x50020CD0)

Bit	Mode	Symbol	Description	Reset
31:19	R	-	Reserved	0x0
18:16	R/W	SDA_TX_HOLD	This field controls the hold time (in term of the core clock period) of the transmit data (SDA) with respect to the SCL edge in FM FM+ SDR and DDR speed mode of operations. This field is not applicable for the ternary speed modes. The valid values are 1 to 7. Others are Reserved.	0x1
15:0	R	-	Reserved	0x0

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Table 783: I3C_BUS_FREE_AVAIL_TIMING_REG (0x50020CD4)

Bit	Mode	Symbol	Description	Reset
31:16	R	-	Reserved	0x0
15:0	R/W	BUS_FREE_TIME	This register field is used only in Master mode of operation I3C Bus Free Count Value. In Pure Bus System, this field represents tCAS parameter. In Mixed Bus system, this field is expected to be programmed to tLOW of I2C Timing.	0x20

Table 784: I3C_VER_ID_REG (0x50020CE0)

Bit	Mode	Symbol	Description	Reset
31:0	R	I3C_VER_ID	Current release type This field indicates the mipi_i3c current release type that is read by an application. For example, release type "ga" is represented in ASCII as 0x6761 and "ea" is represented as 0x6561. Lower 16 bits read from this register can be ignored by the application if release type is "ga". If release type is "ea" the lower 16 bits represents the "ea" release version. An application reading this register along with the I3C_VER_ID register, gathers details of the current release.	0x3130302A

Table 785: I3C_VER_TYPE_REG (0x50020CE4)

Bit	Mode	Symbol	Description	Reset
31:0	R	I3C_VER_TYPE	Current release type This field indicates the i3c current release type that is read by an application. For example, release type "ga" is represented in ASCII as 0x6761 and "ea" is represented as 0x6561. Lower 16 bits read from this register can be ignored by the application if release type is "ga". If release type is "ea" the lower 16 bits represents the "ea" release version. An application reading this register along with the I3C_VER_ID register, gathers details of the current release.	0x6C633033

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Bit	Mode	Symbol	Description	Reset

Table 786: I3C_QUEUE_SIZE_CAPABILITY_REG (0x50020CE8)

Bit	Mode	Symbol	Description	Reset
31:20	R	-	Reserved	0x0
19:16	R	IBI_BUF_SIZE	IBI Queue Size This field reflects the configured IBI Queue size (in DWORDS) in Encoded Values. Values: - 0x0 : 2 DWORDS - 0x1 : 4 DWORDS - 0x2 : 8 DWORDS - 0x3 : 16 DWORDS	0x2
15:12	R	RESP_BUF_SIZE	Response Queue Size This field reflects the configured Response Queue size (in DWORDS) in Encoded Values. Values: - 0x0 : 2 DWORDS - 0x1 : 4 DWORDS - 0x2 : 8 DWORDS - 0x3 : 16 DWORDS	0x1
11:8	R	CMD_BUF_SIZE	Command Queue Size This field reflects the configured Command Queue size (in DWORDS) in Encoded Values. Values: - 0x0 : 2 DWORDS - 0x1 : 4 DWORDS - 0x2 : 8 DWORDS - 0x3 : 16 DWORDS	0x2
7:4	R	RX_BUF_SIZE	Receive Data Buffer Size This field reflects the configured Receive Buffer size (in DWORDS) in Encoded Values. Values: - 0x0 : 2 DWORDS - 0x1 : 4 DWORDS - 0x2 : 8 DWORDS - 0x3 : 16 DWORDS - 0x4 : 32 DWORDS - 0x5 : 64 DWORDS	0x4
3:0	R	TX_BUF_SIZE	Transmit Data Buffer Size This field reflects the configured Transmit Buffer size (in DWORDS) in Encoded Values.	0x4

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Bit	Mode	Symbol	Description	Reset
			Values: - 0x0 : 2 DWORDS - 0x1 : 4 DWORDS - 0x2 : 8 DWORDS - 0x3 : 16 DWORDS - 0x4 : 32 DWORDS - 0x5 : 64 DWORDS	

Table 787: I3C_DEV_CHAR_TABLE1_LOC1_REG (0x50020E00)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	LSB_PROVISIONAL_ID	The LSB 32-bit value of Provisional-ID	0x0

Table 788: I3C_DEV_CHAR_TABLE1_LOC2_REG (0x50020E04)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:0	R/W	MSB_PROVISIONAL_ID	The MSB 16-bit value of Provisional-ID	0x0

Table 789: I3C_DEV_CHAR_TABLE1_LOC3_REG (0x50020E08)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:8	R/W	BCR	Bus Characteristic Value	0x0
7:0	R/W	DCR	Device Characteristic Value	0x0

Table 790: I3C_DEV_CHAR_TABLE1_LOC4_REG (0x50020E0C)

Bit	Mode	Symbol	Description	Reset
31:8	R/W	-	Reserved	0x0
7:0	R/W	DEV_DYNAMIC_ADDR_LOC4	Device Dynamic Address assigned.	0x0

Table 791: I3C_DEV_CHAR_TABLE2_LOC1_REG (0x50020E10)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	LSB_PROVISIONAL_ID	The LSB 32-bit value of Provisional-ID	0x0

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Table 792: I3C_DEV_CHAR_TABLE2_LOC2_REG (0x50020E14)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:0	R/W	MSB_PROVISIONAL_ID	The MSB 16-bit value of Provisional-ID	0x0

Table 793: I3C_DEV_CHAR_TABLE2_LOC3_REG (0x50020E18)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:8	R/W	BCR	Bus Characteristic Value	0x0
7:0	R/W	DCR	Device Characteristic Value	0x0

Table 794: I3C_DEV_CHAR_TABLE2_LOC4_REG (0x50020E1C)

Bit	Mode	Symbol	Description	Reset
31:8	R/W	-	Reserved	0x0
7:0	R/W	DEV_DYNAMIC_ADDR_LOC4	Device Dynamic Address assigned.	0x0

Table 795: I3C_DEV_CHAR_TABLE3_LOC1_REG (0x50020E20)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	LSB_PROVISIONAL_ID	The LSB 32-bit value of Provisional-ID	0x0

Table 796: I3C_DEV_CHAR_TABLE3_LOC2_REG (0x50020E24)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:0	R/W	MSB_PROVISIONAL_ID	The MSB 16-bit value of Provisional-ID	0x0

Table 797: I3C_DEV_CHAR_TABLE3_LOC3_REG (0x50020E28)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:8	R/W	BCR	Bus Characteristic Value	0x0
7:0	R/W	DCR	Device Characteristic Value	0x0

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Table 798: I3C_DEV_CHAR_TABLE3_LOC4_REG (0x50020E2C)

Bit	Mode	Symbol	Description	Reset
31:8	R/W	-	Reserved	0x0
7:0	R/W	DEV_DYNAMIC_ADDR_LOC4	Device Dynamic Address assigned.	0x0

Table 799: I3C_DEV_CHAR_TABLE4_LOC1_REG (0x50020E30)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	LSB_PROVISIONAL_ID	The LSB 32-bit value of Provisional-ID	0x0

Table 800: I3C_DEV_CHAR_TABLE4_LOC2_REG (0x50020E34)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:0	R/W	MSB_PROVISIONAL_ID	The MSB 16-bit value of Provisional-ID	0x0

Table 801: I3C_DEV_CHAR_TABLE4_LOC3_REG (0x50020E38)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:8	R/W	BCR	Bus Characteristic Value	0x0
7:0	R/W	DCR	Device Characteristic Value	0x0

Table 802: I3C_DEV_CHAR_TABLE4_LOC4_REG (0x50020E3C)

Bit	Mode	Symbol	Description	Reset
31:8	R/W	-	Reserved	0x0
7:0	R/W	DEV_DYNAMIC_ADDR_LOC4	Device Dynamic Address assigned.	0x0

Table 803: I3C_DEV_CHAR_TABLE5_LOC1_REG (0x50020E40)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	LSB_PROVISIONAL_ID	The LSB 32-bit value of Provisional-ID	0x0

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Table 804: I3C_DEV_CHAR_TABLE5_LOC2_REG (0x50020E44)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:0	R/W	MSB_PROVISIONAL_ID	The MSB 16-bit value of Provisional-ID	0x0

Table 805: I3C_DEV_CHAR_TABLE5_LOC3_REG (0x50020E48)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:8	R/W	BCR	Bus Characteristic Value	0x0
7:0	R/W	DCR	Device Characteristic Value	0x0

Table 806: I3C_DEV_CHAR_TABLE5_LOC4_REG (0x50020E4C)

Bit	Mode	Symbol	Description	Reset
31:8	R/W	-	Reserved	0x0
7:0	R/W	DEV_DYNAMIC_ADDR_LOC4	Device Dynamic Address assigned.	0x0

Table 807: I3C_DEV_CHAR_TABLE6_LOC1_REG (0x50020E50)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	LSB_PROVISIONAL_ID	The LSB 32-bit value of Provisional-ID	0x0

Table 808: I3C_DEV_CHAR_TABLE6_LOC2_REG (0x50020E54)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:0	R/W	MSB_PROVISIONAL_ID	The MSB 16-bit value of Provisional-ID	0x0

Table 809: I3C_DEV_CHAR_TABLE6_LOC3_REG (0x50020E58)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:8	R/W	BCR	Bus Characteristic Value	0x0
7:0	R/W	DCR	Device Characteristic Value	0x0

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Table 810: I3C_DEV_CHAR_TABLE6_LOC4_REG (0x50020E5C)

Bit	Mode	Symbol	Description	Reset
31:8	R/W	-	Reserved	0x0
7:0	R/W	DEV_DYNAMIC_ADDR_LOC4	Device Dynamic Address assigned.	0x0

Table 811: I3C_DEV_CHAR_TABLE7_LOC1_REG (0x50020E60)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	LSB_PROVISIONAL_ID	The LSB 32-bit value of Provisional-ID	0x0

Table 812: I3C_DEV_CHAR_TABLE7_LOC2_REG (0x50020E64)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:0	R/W	MSB_PROVISIONAL_ID	The MSB 16-bit value of Provisional-ID	0x0

Table 813: I3C_DEV_CHAR_TABLE7_LOC3_REG (0x50020E68)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:8	R/W	BCR	Bus Characteristic Value	0x0
7:0	R/W	DCR	Device Characteristic Value	0x0

Table 814: I3C_DEV_CHAR_TABLE7_LOC4_REG (0x50020E6C)

Bit	Mode	Symbol	Description	Reset
31:8	R/W	-	Reserved	0x0
7:0	R/W	DEV_DYNAMIC_ADDR_LOC4	Device Dynamic Address assigned.	0x0

Table 815: I3C_DEV_CHAR_TABLE8_LOC1_REG (0x50020E70)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	LSB_PROVISIONAL_ID	The LSB 32-bit value of Provisional-ID	0x0

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Table 816: I3C_DEV_CHAR_TABLE8_LOC2_REG (0x50020E74)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:0	R/W	MSB_PROVISIONAL_ID	The MSB 16-bit value of Provisional-ID	0x0

Table 817: I3C_DEV_CHAR_TABLE8_LOC3_REG (0x50020E78)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Reserved	0x0
15:8	R/W	BCR	Bus Characteristic Value	0x0
7:0	R/W	DCR	Device Characteristic Value	0x0

Table 818: I3C_DEV_CHAR_TABLE8_LOC4_REG (0x50020E7C)

Bit	Mode	Symbol	Description	Reset
31:8	R/W	-	Reserved	0x0
7:0	R/W	DEV_DYNAMIC_ADDR_LOC4	Device Dynamic Address assigned.	0x0

Table 819: I3C_DEV_ADDR_TABLE_LOC1_REG (0x50020E80)

Bit	Mode	Symbol	Description	Reset
31	R/W	LEGACY_I2C_DEVICE	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device.	0x0
30:29	R/W	DEV_NACK_RETRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initated by the Master.	0x0
28:24	R/W	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
23:16	R/W	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. The MSB, bit[23], should be programmed with parity of dynamic address.	0x0
15:7	R/W	-	Reserved	0x0
6:0	R/W	DEV_STATIC_ADDR	Device Static Address.	0x0

Table 820: I3C_DEV_ADDR_TABLE_LOC2_REG (0x50020E84)

Bit	Mode	Symbol	Description	Reset
31	R/W	LEGACY_I2C_DEVICE	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device.	0x0
30:29	R/W	DEV_NACK_RETRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initated by the Master.	0x0
28:24	R/W	-	Reserved	0x0
23:16	R/W	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. The MSB, bit[23], should be programmed with parity of dynamic address.	0x0
15:7	R/W	-	Reserved	0x0
6:0	R/W	DEV_STATIC_ADDR	Device Static Address.	0x0

Table 821: I3C_DEV_ADDR_TABLE_LOC3_REG (0x50020E88)

Bit	Mode	Symbol	Description	Reset
31	R/W	LEGACY_I2C_DEVICE	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device.	0x0
30:29	R/W	DEV_NACK_RETRY_CNT	This field is used to set the Device NACK Retry count for the particular device.	0x0

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Bit	Mode	Symbol	Description	Reset
			If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initated by the Master.	
28:24	R/W	-	Reserved	0x0
23:16	R/W	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. The MSB, bit[23], should be programmed with parity of dynamic address.	0x0
15:7	R/W	-	Reserved	0x0
6:0	R/W	DEV_STATIC_ADDR	Device Static Address.	0x0

Table 822: I3C_DEV_ADDR_TABLE_LOC4_REG (0x50020E8C)

Bit	Mode	Symbol	Description	Reset
31	R/W	LEGACY_I2C_DEVICE	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device.	0x0
30:29	R/W	DEV_NACK_RETRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initated by the Master.	0x0
28:24	R/W	-	Reserved	0x0
23:16	R/W	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. The MSB, bit[23], should be programmed with parity of dynamic address.	0x0

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Bit	Mode	Symbol	Description	Reset
15:7	R/W	-	Reserved	0x0
6:0	R/W	DEV_STATIC_ADDR	Device Static Address.	0x0

Table 823: I3C_DEV_ADDR_TABLE_LOC5_REG (0x50020E90)

Bit	Mode	Symbol	Description	Reset
31	R/W	LEGACY_I2C_DEVICE	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device.	0x0
30:29	R/W	DEV_NACK_RETRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initated by the Master.	0x0
28:24	R/W	-	Reserved	0x0
23:16	R/W	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. The MSB, bit[23], should be programmed with parity of dynamic address.	0x0
15:7	R/W	-	Reserved	0x0
6:0	R/W	DEV_STATIC_ADDR	Device Static Address.	0x0

Table 824: I3C_DEV_ADDR_TABLE_LOC6_REG (0x50020E94)

Bit	Mode	Symbol	Description	Reset
31	R/W	LEGACY_I2C_DEVICE	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device.	0x0
30:29	R/W	DEV_NACK_RETRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK	0x0

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Bit	Mode	Symbol	Description	Reset
			for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initated by the Master.	
28:24	R/W	-	Reserved	0x0
23:16	R/W	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. The MSB, bit[23], should be programmed with parity of dynamic address.	0x0
15:7	R/W	-	Reserved	0x0
6:0	R/W	DEV_STATIC_ADDR	Device Static Address.	0x0

Table 825: I3C_DEV_ADDR_TABLE_LOC7_REG (0x50020E98)

Bit	Mode	Symbol	Description	Reset
31	R/W	LEGACY_I2C_DEVICE	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device.	0x0
30:29	R/W	DEV_NACK_RETRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initated by the Master.	0x0
28:24	R/W	-	Reserved	0x0
23:16	R/W	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. The MSB, bit[23], should be programmed with parity of dynamic address.	0x0
15:7	R/W	-	Reserved	0x0
6:0	R/W	DEV_STATIC_ADDR	Device Static Address.	0x0

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Table 826: I3C_DEV_ADDR_TABLE_LOC8_REG (0x50020E9C)

Bit	Mode	Symbol	Description	Reset
31	R/W	LEGACY_I2C_DEVICE	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device.	0x0
30:29	R/W	DEV_NACK_RETRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initated by the Master.	0x0
28:24	R/W	-	Reserved	0x0
23:16	R/W	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. The MSB, bit[23], should be programmed with parity of dynamic address.	0x0
15:7	R/W	-	Reserved	0x0
6:0	R/W	DEV_STATIC_ADDR	Device Static Address.	0x0

44.17 Display Controller Registers

Table 827: Register map LCDC

Address	Register	Description
0x30030000	LCDC_MODE_REG	Display Mode
0x30030004	LCDC_CLKCTRL_REG	Clock Divider
0x30030008	LCDC_BGCOLOR_REG	Background Color
0x3003000C	LCDC_RESXY_REG	Resolution X,Y
0x30030014	LCDC_FRONTPORCHXY_REG	Front Porch X and Y
0x30030018	LCDC_BLANKINGXY_REG	Blanking X and Y

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Address	Register	Description
0x3003001C	LCDC_BACKPORCHXY_REG	Back Porch X and Y
0x30030024	LCDC_STARTXY_REG	Specifies the start position of the very first frame
0x30030028	LCDC_DBIB_CFG_REG	MIPI DBIB Config Register
0x3003002C	LCDC_GPIO_REG	General Purpose IO (8-bits)
0x30030030	LCDC_LAYER0_MODE_REG	Layer0 Mode
0x30030034	LCDC_LAYER0_STARTXY_REG	Layer0 Start XY
0x30030038	LCDC_LAYER0_SIZEXY_REG	Layer0 Size XY
0x3003003C	LCDC_LAYER0_BASEADDR_REG	Layer0 Base Addr
0x30030040	LCDC_LAYER0_STRIDE_REG	Layer0 Stride
0x30030044	LCDC_LAYER0_RESXY_REG	Layer0 Res XY
0x30030050	LCDC_LAYER1_MODE_REG	Layer1 Mode
0x30030054	LCDC_LAYER1_STARTXY_REG	Layer0 Start XY
0x30030058	LCDC_LAYER1_SIZEXY_REG	Layer1 Size XY
0x3003005C	LCDC_LAYER1_BASEADDR_REG	Layer1 Base Addr
0x30030060	LCDC_LAYER1_STRIDE_REG	Layer1 Stride
0x30030064	LCDC_LAYER1_RESXY_REG	Layer1 Res XY
0x300300E8	LCDC_DBIB_CMD_REG	MIPI DBIB Command Register
0x300300EC	LCDC_DBIB_RDAT_REG	Data read by DBI Type-B/SPI interface
0x300300F0	LCDC_CONF_REG	Supported config
0x300300F4	LCDC_IDREG_REG	Identification Register
0x300300F8	LCDC_INTERRUPT_REG	Interrupt Register
0x300300FC	LCDC_STATUS_REG	Status Register
0x30030100	LCDC_COLMOD_REG	Color mode status register
0x30030184	LCDC_CRC_REG	CRC check
0x300301A0	LCDC_FMTCTRL_REG	DBI and JDI format control
0x300301A4	LCDC_FMTCTRL_2_REG	DBI and JDI format control

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Address	Register	Description
0x300301A8	LCDC_CLKCTRL_CG_REG	Controls the CLock Gaters and the routing of format and pixel clock
0x300301AC	LCDC_FMTCTRL_3_REG	JDI format control
0x30030400	LCDC_PALETTE_BASE	Global palette/gamma correction
0x300307FC	LCDC_PALETTE_255	Global palette/gamma correction

Table 828: LCDC_MODE_REG (0x30030000)

Bit	Mode	Symbol	Description	Reset
31	R/W	MODE_EN	Mode register. 0 : disable 1 : enable	0x0
30:29	R/W	-	Reserved	0x0
28	R/W	VSYNC_POL	VSYNC polarity. 0: positive 1: negative	0x0
27	R/W	HSYNC_POL	HSYNC polarity. 0: positive 1: negative	0x0
26	R/W	DE_POL	DE polarity. 0: positive 1: negative	0x0
25:24	R/W	DITH_MODE	0x00: Dithering is disabled 0x01: Dithering 18-bits mode 0x02: Dithering 16-bits mode 0x03: Dithering 15-bits mode	0x0
23	R/W	VSYNC_SCPL	Set VSYNC for a single cycle per line. 0: disable 1: enable	0x0
22	R/W	PIXCLKOUT_POL	Pixel clock out polarity. 0: positive 1: negative	0x0
21	R/W	-	Reserved	0x0
20	R/W	GLOBAL_GAMMA_EN	When set to 1, global gamma correction is enabled	0x0
19	R/W	FORCE_BLANK	Forces output to blank. 0: disable 1: enable	0x0
18	R/W	UNDERRUN_PREVENTION_EN	When set to 1, underrun prevention is enabled for interfaces that support this	0x0
17	R/W	SFRAME_UPD	Single frame update. 0: disable 1: enable	0x0

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Bit	Mode	Symbol	Description	Reset
16:15	R/W	-	Reserved	0x0
14:12	R/W	DPI2_CONFIG	Defines MIPI DPI-2 Configuration 0x00: RGB888 24-bits 0x01: RGB666 18-bits Configuration 1 0x02: RGB666 18-bits Configuration 2 0x03: RGB565 16-bits Configuration 1 0x04: RGB565 16-bits Configuration 2 0x05: RGB565 16-bits Configuration 3 0x06: Reserved 0x07: Reserved	0x0
11	R/W	PIXCLKOUT_SEL	Selects the pixel out clock for the display. 0: based on the pixel pipeline clock 1: based on the format pipeline clock See also the LCDC_CLKCTRL_REG.	0x0
10:9	R/W	-	Reserved	0x0
8:5	R/W	OUT_MODE	Selection of the output mode 0000: Parallel RGB 1000: JDI MIP All the other values are reserved.	0x0
4	R/W	DBIB_OFF	When set to 0, DBI Type-B interface is enabled	0x0
3	R/W	FORM_OFF	Formating off 0: disabled 1: enabled	0x0
2	R/W	-	Reserved	0x0
1	R/W	DSCAN	Double horizontal scan 0: disabled 1: enabled	0x0
0	R/W	TMODE	Test mode 0: disabled 1: enabled	0x0

Table 829: LCDC_CLKCTRL_REG (0x30030004)

Bit	Mode	Symbol	Description	Reset
31:27	R/W	SEC_CLK_DIV	Secondary clock divider that generates the format pipeline clock. Source clock of this divider is the main clock of LCD controller. The period of the generated clock is defined as : LCDC_SEC_CLK_DIV x period_of_main_clock.	0x0
26:14	R/W	-	Reserved	0x0
13:8	R/W	DMA_HOLD	Hold time before DMA activated.	0x4
7:6	R/W	-	Reserved	0x0
5:0	R/W	CLK_DIV	Clock divider that generates the pixel pipeline clock. Source clock of this divider is the format pipeline clock (see also LCDC_SEC_CLK_DIV). The period of the generated clock is defines as :	0x1

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Bit	Mode	Symbol	Description	Reset
			LCDC_CLK_DIV x period_of_format_clk. A zero value gives division by one.	

Table 830: LCDC_BGCOLOR_REG (0x30030008)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	BG_RED	Red color used as background.	0x0
23:16	R/W	BG_GREEN	Green color used as background.	0x0
15:8	R/W	BG_BLUE	Blue color used as background.	0x0
7:0	R/W	BG_ALPHA	Alpha color used as background.	0x0

Table 831: LCDC_RESXY_REG (0x3003000C)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	RES_X	Resolution X in pixels.	0x0
15:0	R/W	RES_Y	Resolution Y in pixels.	0x0

Table 832: LCDC_FRONTPORCHXY_REG (0x30030014)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	FPORCH_X	Front porch X (pixel clocks)	0x0
15:0	R/W	FPORCH_Y	Front porch Y (lines)	0x0

Table 833: LCDC_BLANKINGXY_REG (0x30030018)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	BLANKING_X	Blanking period X (HSYNC pulse length)	0x0
15:0	R/W	BLANKING_Y	Blanking period Y (VSYNC lines)	0x0

Table 834: LCDC_BACKPORCHXY_REG (0x3003001C)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	BPORCH_X	Back porch X (pixel clocks)	0x0
15:0	R/W	BPORCH_Y	Back porch Y (lines)	0x0

Table 835: LCDC_STARTXY_REG (0x30030024)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	START_X	Specify framess X dimension	0x0
15:0	R/W	START_Y	Specify framess Y dimension	0x0

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Table 836: LCDC_DBIB_CFG_REG (0x30030028)

Bit	Mode	Symbol	Description	Reset
31	R/W	DBIB_INTERFACE_EN	When set to 1, the DBI Type-B interface is activated	0x0
30	R/W	DBIB_CSX_CFG_EN	When set to 1, the value of the CSX signal of the DBI Type-B interface can be configured from the DBIB_CFG[29] register bit	0x0
29	R/W	DBIB_CSX_CFG	Sets the value of DBIB_CSX signal: CSX is set to one if DBIB_CFG[29] has the value of one CSX is set to zero if DBIB_CFG[29] has the value of zero	0x0
28	R/W	DBIB_TE_DISABLE	When set to 1, the DBIB_TE signal is disabled	0x0
27	R/W	SPI_DC_AS_SPI_SD1	When set to 1, enables the usage of SPI_DC wire as SPI_SD1	0x0
26	R/W	DBIB_FORCE_IDLE	When set to 1, force DBI Type-B interface to idle state. Swap on the fly data for the interface	0x0
25	R/W	DBIB_RESX_OUT_EN	Drives DBIB_RESX output signal of DBI Type-B interface	0x0
24	R/W	SUB_PIXEL_REVERSE	Reverse sub pixel order	0x0
23	R/W	SPI3_EN	When set to 1, SPI 3-wire interface is enabled	0x0
22	R/W	SPI4_EN	When set to 1, SPI 4-wire interface is enabled	0x0
21	R/W	DBIB_BACK_PRESSURE_EN	When set to 1, Enables back-pressure for DBI Type-B interface	0x0
20	R/W	SPI_CLK_PHASE	Sets SPI Clock Phase	0x0
19	R/W	SPI_CLK_POLARITY	Sets SPI Clock Polarity	0x0
18	R/W	SPID_JDI	Enable JDI over SPI	0x0
17	R/W	CMD_DATA_AS_HEADER	When set to 1, command data are used as header of each line	0x0
16	R/W	BIT_ORDER_ADDR_INVERT	When set to 1, inverts the bit-order of the horizontal line address (used along with DBIB_CFG[17] register bit)	0x0
15	R/W	SPI_2BYTE_ADDR	When set to 1, two-byte address is sent with each horizontal line (SPI)	0x0
14	R/W	PIX_CLK_AT_DBIB_CLK	When set to 1, expose pixel generation clock on the DBIB_CLK	0x0
13	R/W	EXT_CTRL_EN	When set to 1, enables the external control	0x0
12	R/W	HORIZONTAL_BLANK_EN	When set to 1, enables the horizontal blanking	0x0
11	R/W	DUAL_SPI_SUBPIXEL_EXTRACT_EN	When set to 1, Enables DualSPI sub-pixel transaction	0x0
10	R/W	QUAD_SPI_EN	When set to 1, Enables QuadSPI	0x0

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Bit	Mode	Symbol	Description	Reset
9	R/W	DUAL_SPI_EN	When set to 1, Enables DualSPI	0x0
8:6	R/W	DBIB_INTERFACE_WIDTH	Set DBI Type-B interface width (8, 9 or 16 bits) and the serial interface: 0x0: 8-bit interface 0x1: 9-bit interface (reserved, not supported) 0x2: 16-bit interface (reserved, not supported) 0x3: SPI 0x4: Dual SPI 0x5: Quad SPI	0x0
5:3	R/W	DBIB_DATA_ORDER	Set the data order of the 8-bit data word: 0x0: option 0 0x1: option 1 0x2: option 2 0x3: option 3 0x4: option 4 0x5: Reserved 0x6: Reserved 0x7: Reserved	0x0
2:0	R/W	DBIB_COLOR_FMT	Defines the output format and depends of the type of the output interface. For the SPI3/SPI4 are supported the following formats: 0x0 : Reserved 0x1 : RGB111 0x2 : RGB332 0x3 : RGB444 0x4 : Reserved 0x5 : RGB565 0x6 : RGB666 0x7 : RGB888	0x0

Table 837: LCDC_GPIO_REG (0x3003002C)

Bit	Mode	Symbol	Description	Reset
31:17	-	-	Reserved	0x0
16	W	DPI_CM_ASSERT	Assert DPI-2 Color Mode signal	0x0
15	W	DPI_SD_ASSERT	Assert DPI-2 Shutdown signal	0x0
14:13	R/W	-	Reserved	0x2
12:6	R/W	-	Reserved	0x0
5	R/W	GPIO_SPI_SI_ON_SD_PAD	Enable to have the SPI SI on the SPI SD pad	0x0
4:3	R/W	GPIO_OUTPUT_MODE	Select the mode that should be mapped on the GPIO pins 0x0 = JDI 0x1 = DPI 0x2 = DBI 0x3 = SPI	0x0

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Bit	Mode	Symbol	Description	Reset
2	R/W	GPIO_OUTPUT_EN	Enable the GPIO pins for LCDC control. The GPIO_OUTPUT_MODE is used to define what LCDC pins will be mapped towards the GPIO pins.	0x0
1	R/W	TE_INV	Applies an inversion on the TE (tearing effect) signal. 0 : the inversion is not applied on the TE signal 1 : the inversion is applied on TE signal	0x0
0	R/W	-	Reserved	0x0

Table 838: LCDC_LAYER0_MODE_REG (0x30030030)

Bit	Mode	Symbol	Description	Reset
31	R/W	L0_EN	Enable layer. 0 : disable 1 : enable	0x0
30	R/W	L0_FORCE_ALPHA	When set to 1, force alpha with global alpha	0x0
29	R/W	-	Reserved	0x0
28	R/W	L0_PREMUL_IMG_ALPHA	When set to 1, premultiply image alpha is enabled	0x0
27	R/W	L0_ASSERT_HLOCK_DMA	When set to 1, HLOCK signal on AHB DMAs is asserted	0x0
26	R/W	-	Reserved	0x0
25:24	R/W	-	Reserved	0x0
23:16	R/W	L0_ALPHA	Alpha layer global value (0x00-0xFF range)	0x0
15:12	R/W	L0_DST_BLEND	Destinary Blending Function 0000: BLEND ZERO 0001: BLEND ONE 0010: BLEND ALPHA SRC 0011: BLEND ALPHA GBL 0100: BLEND ALPHA SRCGBL 0101: BLEND INV SRC 0110: BLEND INV GBL 0111: BLEND INV SRCGBL 1010: BLEND ALPHA DST 1101: BLEND INV DST	0x0
11:8	R/W	L0_SRC_BLEND	Source Blending Function 0000: BLEND ZERO 0001: BLEND ONE 0010: BLEND ALPHA SRC 0011: BLEND ALPHA GBL 0100: BLEND ALPHA SRCGBL 0101: BLEND INV SRC 0110: BLEND INV GBL 0111: BLEND INV SRCGBL 1010: BLEND ALPHA DST 1101: BLEND INV DST	0x0

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Bit	Mode	Symbol	Description	Reset
7:5	R/W	-	Reserved	0x0
4:0	R/W	L0_COLOR_MODE	Color Mode: 00001: 16-bit RGBX5551 color format, 00010: 32-bit RGBX8888 color format, 00100: 8-bit RGB332 color format, 00101: 16-bit RGB565 color format, 00110: 32-bit XRGB8888, 01101: ABGR8888, 01110: BGRA8888 others: reserved / not supported	0x0

Table 839: LCDC_LAYER0_STARTXY_REG (0x30030034)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	L0_START_X	Start X (offset pixels)	0x0
15:0	R/W	L0_START_Y	Start Y (offset pixels)	0x0

Table 840: LCDC_LAYER0_SIZEXY_REG (0x30030038)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	L0_SIZE_X	Size X (Size of layer in pixels)	0x0
15:0	R/W	L0_SIZE_Y	Size Y (Size of layer in pixels)	0x0

Table 841: LCDC_LAYER0_BASEADDR_REG (0x3003003C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	L0_BASE_ADDR	Base Address of the frame buffer	0x0

Table 842: LCDC_LAYER0_STRIDE_REG (0x30030040)

Bit	Mode	Symbol	Description	Reset
31:28	R/W	-	Reserved	0x0
27:25	R/W	L0_DMA_PREFETCH	Specify the DMA prefetch Level in layer 0 * 0x000 : 0 DMA rows (default) * 0x001 : 1 DMA row * 0x010 : 2 DMA rows * 0x011 : 3 DMA rows * 0x100 : 4 DMA rows	0x0
24:21	R/W	-	Reserved	0x0
20:19	R/W	L0_FIFO_THR	Layer dma fifo threshold burst start 00: half fifo (default) 01: 2 burst size	0x0

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Bit	Mode	Symbol	Description	Reset
			10: 4 burst size 11: 8 burst size	
18:17	R/W	-	Reserved	0x0
16	R/W	L0_NO_16BEAT_BURST	When set to 1 forbids INCR16 bursts in layer 0	0x0
15:0	R/W	L0_STRIDE	Layer Stride (distance from line to line in bytes)	0x0

Table 843: LCDC_LAYER0_RESXY_REG (0x30030044)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	L0_RES_X	Resolution X (Resolution of layer in pixels)	0x0
15:0	R/W	L0_RES_Y	Resolution Y (Resolution of layer in pixels)	0x0

Table 844: LCDC_LAYER1_MODE_REG (0x30030050)

Bit	Mode	Symbol	Description	Reset
31	R/W	L1_EN	Enable layer. 0 : disable 1 : enable	0x0
30	R/W	L1_FORCE_ALPHA	When set to 1, force alpha with global alpha	0x0
29	R/W	-	Reserved	0x0
28	R/W	L1_PREMUL_IMG_ALPHA	When set to 1, premultiply image alpha is enabled	0x0
27	R/W	L1_ASSERT_HLOCK_DMA	When set to 1, HLOCK signal on AHB DMAs is asserted	0x0
26	R/W	-	Reserved	0x0
25:24	R/W	-	Reserved	0x0
23:16	R/W	L1_ALPHA	Alpha layer global value (0x00-0xFF range)	0x0
15:12	R/W	L1_DST_BLEND	Destinary Blending Function 0000: BLEND ZERO 0001: BLEND ONE 0010: BLEND ALPHA SRC 0011: BLEND ALPHA GBL 0100: BLEND ALPHA SRCGBL 0101: BLEND INV SRC 0110: BLEND INV GBL 0111: BLEND INV SRCGBL 1010: BLEND ALPHA DST 1101: BLEND INV DST	0x0
11:8	R/W	L1_SRC_BLEND	Source Blending Function 0000: BLEND ZERO 0001: BLEND ONE 0010: BLEND ALPHA SRC	0x0

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Bit	Mode	Symbol	Description	Reset
			0011: BLEND ALPHA GBL 0100: BLEND ALPHA SRCGBL 0101: BLEND INV SRC 0110: BLEND INV GBL 0111: BLEND INV SRCGBL 1010: BLEND ALPHA DST 1101: BLEND INV DST	
7:5	R/W	-	Reserved	0x0
4:0	R/W	L1_COLOR_MODE	Color Mode: 00001: 16-bit RGBX5551 color format, 00010: 32-bit RGBX8888 color format, 00100: 8-bit RGB332 color format, 00101: 16-bit RGB565 color format, 00110: 32-bit XRGB8888, 01101: ABGR8888, 01110: BGRA8888 others: reserved / not supported	0x0

Table 845: LCDC_LAYER1_STARTXY_REG (0x30030054)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	L1_START_X	Start X (offset pixels)	0x0
15:0	R/W	L1_START_Y	Start Y (offset pixels)	0x0

Table 846: LCDC_LAYER1_SIZEXY_REG (0x30030058)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	L1_SIZE_X	Size X (Size of layer in pixels)	0x0
15:0	R/W	L1_SIZE_Y	Size Y (Size of layer in pixels)	0x0

Table 847: LCDC_LAYER1_BASEADDR_REG (0x3003005C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	L1_BASE_ADDR	Base Address of the frame buffer	0x0

Table 848: LCDC_LAYER1_STRIDE_REG (0x30030060)

Bit	Mode	Symbol	Description	Reset
31:28	R/W	-	Reserved	0x0
27:25	R/W	L1_DMA_PREFETCH	Specify the DMA prefetch Level in layer 1 * 0x000 : 0 DMA rows (default) * 0x001 : 1 DMA row	0x0

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Bit	Mode	Symbol	Description	Reset
			* 0x010 : 2 DMA rows * 0x011 : 3 DMA rows * 0x100 : 4 DMA rows	
24:21	R/W	-	Reserved	0x0
20:19	R/W	L1_FIFO_THR	Layer dma fifo threshold burst start 00: half fifo (default) 01: 2 burst size 10: 4 burst size 11: 8 burst size	0x0
18:17	R/W	-	Reserved	0x0
16	R/W	L1_NO_16BEAT_BURST	When set to 1 forbids INCR16 bursts in layer 1	0x0
15:0	R/W	L1_STRIDE	Layer Stride (distance from line to line in bytes)	0x0

Table 849: LCDC_LAYER1_RESXY_REG (0x30030064)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	L1_RES_X	Resolution X (Resolution of layer in pixels)	0x0
15:0	R/W	L1_RES_Y	Resolution Y (Resolution of layer in pixels)	0x0

Table 850: LCDC_DBIB_CMD_REG (0x300300E8)

Bit	Mode	Symbol	Description	Reset
31	R/W	PART_UPDATE	When set to 0, indicates that the command data are the Base address for partial update. Applied on SPI/JDI-SPI type	0x0
30	R/W	DBIB_CMD_SEND	Send command to the DBI interface	0x0
29:28	R/W	CMD_WIDTH	Determine the command width. Applicable only on the QuadSPI 0x00: 1 Byte 0x01: 2 Bytes 0x02: 3 Bytes 0x03: Reserved	0x0
27	R/W	QSPI_SERIAL_CMD_TRANS	When sets to 1, switch to serial transmission of the command. Applicable only for QuadSPI.	0x0
26	R/W	RD_MODE_EN	When sets to 1, read mode is enabled	0x0
25	R/W	FMTCTRL_EXPOSE_SETTING	When sets to 1, FMTCTRL[15:8] is exposed on DBIB_CT pins and FMTCTRL[31] on DBIB_GE else FMTCTRL[15:8] is exposed on DBIB_CT pins and FMTCTRL[30] on DBIB_GE	0x0
24	R/W	ST_INT_CMD_TYPE	When sets to 1, store internally a command type which is transmitted at the beggining of each scanline	0x0
23:16	R/W	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
15:0	R/W	DBIB_CMD_VAL	Data to send to the DBI interface	0x0

Table 851: LCDC_DBIB_RDAT_REG (0x300300EC)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	DBIB_RDAT	On Write: 31-30 bits: Specify the number of read cycles 0x0: 8 cycles 0x1: 16 cycles 0x2: 24 cycles Used along with FMTCTRL[20:16] register bits 29-0 bits: Reserved On Read: 31-0 bits: Read data from DBI Type-B/SPI interfaces	0x0

Table 852: LCDC_CONF_REG (0x300300F0)

Bit	Mode	Symbol	Description	Reset
31:0	R	CONF	0 bit : Indicates that Global Gamma/Palette is enabled 1 bit : Indicates that fixed cursor is enabled 2 bit : Indicates that programmable cursor is enabled 3 bit : Indicates that dithering is enabled 4 bit : Indicates that formatting is enabled 5 bit : Indicates that high quality YUV/YCbCr converter is enabled 6 bit : Indicates that DBI Type-B interface is enabled 7 bit : Indicates that RGB to YUV/YCbCr converter is enabled 8 bit : Indicates that layer 0 is enabled 9 bit : Indicates that layer 0 has blender 10 bit : Indicates that layer 0 has scaler 11 bit : Indicates that layer 0 has gamma LUT 12 bit : Indicates that layer 1 is enabled 13 bit : Indicates that layer 1 has blender 14 bit : Indicates that layer 1 has scaler 15 bit : Indicates that layer 1 has gamma LUT 16 bit : Indicates that layer 2 is enabled 17 bit : Indicates that layer 2 has blender 18 bit : Indicates that layer 2 has scaler 19 bit : Indicates that layer 2 has gamma LUT 20 bit : Indicates that layer 3 is enabled 21 bit : Indicates that layer 3 has blender 22 bit : Indicates that layer 3 has scaler	0x3359

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Bit	Mode	Symbol	Description	Reset
			23 bit : Indicates that layer 3 has gamma LUT 27-24 bits : Reserved 28 bit : Indicates that layer 0 has YUV Memory 29 bit : Indicates that layer 1 has YUV Memory 30 bit : Indicates that layer 2 has YUV Memory 31 bit : Indicates that layer 3 has YUV Memory	

Table 853: LCDC_IDREG_REG (0x300300F4)

Bit	Mode	Symbol	Description	Reset
31:0	R	LCDC_ID	Identification register	0x87452365

Table 854: LCDC_INTERRUPT_REG (0x300300F8)

Bit	Mode	Symbol	Description	Reset
31	R/W	IRQ_TRIGGER_SEL	IRQ trigger control 0: Level triggering 1: Edge triggering In the case of the level triggering, the request remains active in the LCDC until to be cleared. The request can be cleared by performing a write access in the LCDC_INTERRUPT_REG. This is not required in the case of the edge triggering.	0x0
30	R/W	-	Reserved	0x0
29:5	-	-	Reserved	0x0
4	R/W	FE_IRQ_EN	Frame end interrupt enabled	0x0
3	R/W	TE_IRQ_EN	Tearing enable interrupt enabled	0x0
2	R/W	-	Reserved	0x0
1	R/W	HSYNC_IRQ_EN	HSYNC interrupt enabled	0x0
0	R/W	VSYNC_IRQ_EN	VSYNC or TE interrupt enabled. See also the configuration bit LCDC_DBIB_CFG_REG[LCDC_DBIB_TE_DIS] for the TE signal.	0x1

Table 855: LCDC_STATUS_REG (0x300300FC)

Bit	Mode	Symbol	Description	Reset
31:17	-	-	Reserved	0x0
16	R	SPI_RD_WR_OP	Indicates read/write operation on SPI	0x0
15	R	DBIB_CMD_FIFO_FULL	Indicates if the command FIFO is full	0x0
14	R	DBI_SPI_CS	Indicates DBI/SPI CS status	0x0
13	R	FRAME_END	Frame end (active high)	0x0

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Bit	Mode	Symbol	Description	Reset
12	R	DBIB_OUT_TRANS_PENDING	Pending output transaction in DBI Type-B interface	0x0
11	R	DBIB_CMD_PENDING	Transferring of command in progress. 0: idle 1: in progress	0x0
10	R	DBIB_DATA_PENDING	Pending RGB data in DBI Type-B interface	0x0
9	-	-	Reserved	0x0
8	R	DBIB_TE	The DBIB tearing effect signal	0x0
7	R	STICKY_UNDERFLOW	Sticky underflow(clear with write in the LCDC_INTERRUPT_REG) 0: There is no underflow 1: Underflow has been detected.Remains high until to be cleared by performing a write access on the register LCDC_INTERRUPT_REG.	0x0
6	R	UNDERFLOW	Underflow on the current transfer. 0: There is no underflow 1: Underflow has been detected.	0x0
5	R	LAST_ROW	Last row (Last row is currently displayed)	0x0
4	R	STAT_CSYNC	CSYNC signal level	0x0
3	R	STAT_VSYNC	VSYNC signal level	0x0
2	R	STAT_HSYNC	HSYNC signal level	0x0
1	R	STAT_DE	Indicates the DE signal status (0 or 1) at the current time of reading	0x0
0	R	STAT_ACTIVE	Active (When not in vertical blanking)	0x0

Table 856: LCDC_COLMOD_REG (0x30030100)

Bit	Mode	Symbol	Description	Reset
31	R	-	Reserved	0x0
30:17	R	-	Reserved	0x1038
16:0	R	COLMODES	16 bit: Indicates that the LUT8 color format is enabled 15 bit: Indicates that the RGBA5551 16-bit color format is enabled 14 bit: Indicates that the RGBA8888 32-bit color format is enabled 13 bit: Indicates that the RGB332 8-bit color format is enabled 12 bit: Indicates that the RGB565 16-bit color format is enabled 11 bit: Indicates that the ARGB8888 32-bit color format is enabled 10 bit: Indicates that the L8 color format is enabled 9 bit: Indicates that the L1 color format is enabled 8 bit: Indicates that the L4 color format is enabled	0xF858

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Bit	Mode	Symbol	Description	Reset
			7 bit: Indicates that the YUYV color format is enabled 6 bit: Indicates that the RGB888 24-bit color format is enabled 5 bit: Indicates that the YUY2 color format is enabled 4 bit: Indicates that the ABGR8888 32-bit color format is enabled 3 bit: Indicates that the BGRA8888 32-bit color format is enabled 2 bit: Indicates that the V_YUV420 color format is enabled 1 bit: Indicates that the TLYUV420 color format is enabled 0 bit: Indicates that the TSc4/TSc6 propietary color format is enabled	

Table 857: LCDC_CRC_REG (0x30030184)

Bit	Mode	Symbol	Description	Reset
31:0	R	CRC	CRC check.	0x0

Table 858: LCDC_FMTCTRL_REG (0x300301A0)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	FMTCTRL	When DBI-Type B Interface is selected: Bits Description 31-22 bits: Reserved 21-16 bits: Specify the number of read cycles for SPI/DBI Type-B. Used along with DBIB_CFG[31:30] register bits 0x0: 1 cycles 0x1: 2 cycles 0x2: 3 cycles ... 0x3E: 63 cycles * 0x3F: 64 cycles 15-0 bits : Reserved When JDI-Parallel Interface is selected: Bits Description 31 bit : Mute DPI outputs 30 bit : Mask DPIREADY input 29 bit : Reserved 28-26 bits : JDI HST width 25-23 bits : JDI HST offset 22-13 bits : JDI VST width 12-3 bits : JDI VST offset	0x0

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Bit	Mode	Symbol	Description	Reset
			2-0 bits : Reserved	

Table 859: LCDC_FMTCTRL_2_REG (0x300301A4)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	FMTCTRL_2	Bits Description When DBI-Type B Interface is selected: Bits Description 31-16 bits: Reserved 15-0 bits: Specify the blanking period length for the X dimension When JDI-Parallel Interface is selected: Bits Description 31-30: Reserved 29-20 bits: JDI XRST offset 19-10 bits: JDI ENB width 9-0 bits: JDI ENB offset	0x0

Table 860: LCDC_CLKCTRL_CG_REG (0x300301A8)

Bit	Mode	Symbol	Description	Reset
31:3	R/W	-	Reserved	0x0
2	R/W	LCDC_SWAP_PIX_FORMAT_CLK	Pixel generation and format clock swap	0x0
1	R/W	LCDC_INV_CLK_POLARITY	Invert (output) clock polarity	0x0
0	R/W	-	Reserved	0x0

Table 861: LCDC_FMTCTRL_3_REG (0x300301AC)

Bit	Mode	Symbol	Description	Reset
31:10	R/W	-	Reserved	0x0
9:0	R/W	XRST_HIGH_STATE	Set the high state of XRST signal in multiple of VCK	0x0

Table 862: LCDC_PALETTE_BASE (0x30030400)

Bit	Mode	Symbol	Description	Reset
23:16	W	PALLETE_R	Gamma ramp red bits	0x0
15:8	W	PALLETE_G	Gamma ramp green bits	0x0
7:0	W	PALLETE_B	Gamma ramp blue bits	0x0

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Table 863: LCDC_PALETTE_255 (0x300307FC)

Bit	Mode	Symbol	Description	Reset
23:16	W	PALLETE_R	Gamma ramp red bits	0x0
15:8	W	PALLETE_G	Gamma ramp green bits	0x0
7:0	W	PALLETE_B	Gamma ramp blue bits	0x0

44.18 Memory Controller Registers

Table 864: Register map MEMCTRL

Address	Register	Description
0x50050004	MEM_PRIO_ARB1_4_REG	Priority Control Register for arbiter 1, 2, 3 and 4
0x50050008	MEM_PRIO_ARB5_8_REG	Priority Control Register for arbiter 5, 6, 7 and 8
0x50050010	MEM_STALL_REG	Maximum Stall cycles Control Register
0x50050014	MEM_STATUS_REG	Memory Arbiter Status Register
0x50050018	MEM_STATUS2_REG	RAM cells Status Register
0x50050020	CMI_CODE_BASE_REG	CMAC code Base Address Register
0x50050024	CMI_DATA_BASE_REG	CMAC data Base Address Register
0x50050028	CMI_SHARED_BASE_REG	CMAC shared data Base Address Register
0x5005002C	CMI_END_REG	CMAC end Address Register
0x50050030	CMAC_STATUS_REG	Memory Arbiter Status Register
0x50050070	BUSY_SET_REG	BSR Set Register
0x50050074	BUSY_SET_REG2	BSR2 Set Register
0x50050078	BUSY_RESET_REG	BSR Reset Register
0x5005007C	BUSY_RESET_REG2	BSR2 Reset Register
0x50050080	BUSY_STAT_REG	BSR Status Register
0x50050084	BUSY_STAT_REG2	BSR2 Status Register

Table 865: MEM_PRIO_ARB1_4_REG (0x50050004)

Bit	Mode	Symbol	Description	Reset
31:30	R	-	Reserved	0x0
29:28	R/W	ARB4_AHB_DMA_PRIO	Priority for the DMA AHB interface of arbiter 4 00: low priority (default) 01: mid priority 1x: high priority	0x0
27:26	R/W	ARB4_AHB_CPUS_PRIO	Priority for the CPUS AHB interface of arbiter 4. 00: low priority (default)	0x0

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Bit	Mode	Symbol	Description	Reset
			01: mid priority 10: high priority 11: top priority	
25:24	R	-	Reserved	0x0
23:22	R	-	Reserved	0x0
21:20	R/W	ARB3_AHB_DMA_PRIO	Priority for the DMA AHB interface of arbiter 3 00: low priority (default) 01: mid priority 1x: high priority	0x0
19:18	R/W	ARB3_AHB_CPUS_PRIO	Priority for the CPUS AHB interface of arbiter 3. 00: low priority (default) 01: mid priority 10: high priority 11: top priority	0x0
17:16	R/W	ARB3_AHB_CPUC_PRIO	Priority for the CPUC AHB interface of arbiter 3. 00: low priority (default) 01: mid priority 10: high priority 11: top priority	0x0
15:14	R/W	ARB2_SNC_PRIO	Priority for the SNC interface of arbiter 2. 00: low priority (default) 01: mid priority 10: high priority 11: top priority	0x0
13:12	R/W	ARB2_AHB_DMA_PRIO	Priority for the DMA AHB interface of arbiter 2. 00: low priority (default) 01: mid priority 1x: high priority	0x0
11:10	R/W	ARB2_AHB_CPUS_PRIO	Priority for the CPUS AHB interface of arbiter 2. 00: low priority (default) 01: mid priority 10: high priority 11: top priority	0x0
9:8	R/W	ARB2_AHB_CPUC_PRIO	Priority for the CPUC AHB interface of arbiter 2. 00: low priority (default) 01: mid priority 10: high priority 11: top priority	0x0
7:6	R/W	ARB1_SNC_PRIO	Priority for the SNC interface of arbiter 1. 00: low priority (default) 01: mid priority 10: high priority 11: top priority	0x0
5:4	R/W	ARB1_AHB_DMA_PRIO	Priority for the DMA AHB interface of arbiter 1. 00: low priority (default) 01: mid priority	0x0

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Bit	Mode	Symbol	Description	Reset
			1x: high priority	
3:2	R/W	ARB1_AHB_CPUS_PRIO	Priority for the CPUS AHB interface of arbiter 1. 00: low priority (default) 01: mid priority 10: high priority 11: top priority	0x0
1:0	R/W	ARB1_AHB_CPUC_PRIO	Priority for the CPUC AHB interface of arbiter 1. 00: low priority (default) 01: mid priority 10: high priority 11: top priority	0x0

Table 866: MEM_PRIO_ARB5_8_REG (0x50050008)

Bit	Mode	Symbol	Description	Reset
31:30	R/W	ARB8_SNC_PRIO	Priority for the SNC interface of arbiter 8. 00: low priority (default) 01: mid priority 10: high priority 11: top priority	0x0
29:28	R/W	ARB8_AHB_DMA_PRIO	Priority for the DMA AHB interface of arbiter 8. 00: low priority (default) 01: mid priority 1x: high priority	0x0
27:26	R/W	ARB8_AHB_CPUS_PRIO	Priority for the CPUS AHB interface of arbiter 8. 00: low priority (default) 01: mid priority 10: high priority 11: top priority	0x0
25:24	R	-	Reserved	0x0
23:22	R	-	Reserved	0x0
21:20	R/W	ARB7_AHB_DMA_PRIO	Priority for the DMA AHB interface of arbiter 7. 00: low priority (default) 01: mid priority 1x: high priority	0x0
19:18	R/W	ARB7_AHB_CPUS_PRIO	Priority for the CPUS AHB interface of arbiter 7. 00: low priority (default) 01: mid priority 10: high priority 11: top priority	0x0
17:16	R	-	Reserved	0x0
15:14	R	-	Reserved	0x0
13:12	R/W	ARB6_AHB_DMA_PRIO	Priority for the DMA AHB interface of arbiter 6. 00: low priority (default) 01: mid priority	0x0

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Bit	Mode	Symbol	Description	Reset
			1x: high priority	
11:10	R/W	ARB6_AHB_CPUS_PRIO	Priority for the CPUS AHB interface of arbiter 6. 00: low priority (default) 01: mid priority 10: high priority 11: top priority	0x0
9:8	R	-	Reserved	0x0
7:6	R	-	Reserved	0x0
5:4	R/W	ARB5_AHB_DMA_PRIO	Priority for the DMA AHB interface of arbiter 5. 00: low priority (default) 01: mid priority 1x: high priority	0x0
3:2	R/W	ARB5_AHB_CPUS_PRIO	Priority for the CPUS AHB interface of arbiter 5. 00: low priority (default) 01: mid priority 10: high priority 11: top priority	0x0
1:0	R	-	Reserved	0x0

Table 867: MEM_STALL_REG (0x50050010)

Bit	Mode	Symbol	Description	Reset
15:12	R/W	SNC_MAX_STALL	Maximum allowed number of stall cycles for the SNC interface. If exceeded, the interface will get high priority. Valid for a single access so the next access (of a burst) might end up in the que for the same number of wait cycles. 0: don't use, not feasible and can block other interfaces 1: max 1 stall cycle 15: max 15 stall cycles	0xF
11:8	R/W	AHB_DMA_MAX_STALL	Maximum allowed number of stall cycles for the DMA AHB interface. If exceeded, the interface will get high priority. Valid for a single access so the next access (of a burst) might end up in the que for the same number of wait cycles. 0: don't use, not feasible and can block other interfaces 1: max 1 stall cycle 15: max 15 stall cycles	0xF
7:4	R/W	AHB_CPUS_MAX_STALL	Maximum allowed number of stall cycles for the CPUS AHB interface. If exceeded, the interface will get high priority. Valid for a single access so the next access (of a burst) might end up in the que for the same number of wait cycles. 0: don't use, not feasible and can block other interfaces 1: max 1 stall cycle 15: max 15 stall cycles	0xF

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Bit	Mode	Symbol	Description	Reset
3:0	R/W	AHB_CPUC_MAX_STALL	Maximum allowed number of stall cycles for the CPUC AHB interface. If exceeded, the interface will get high priority. Valid for a single access so the next access (of a burst) might end up in the que for the same number of wait cycles. 0: don't use, not feasible and can block other interfaces 1: max 1 stall cycle 15: max 15 stall cycles	0xF

Table 868: MEM_STATUS_REG (0x50050014)

Bit	Mode	Symbol	Description	Reset
23:20	R	AHB_SNC_WR_BUFF_CNT	The maximum number of arbiter clock cycles that an SNC AHB access has been buffered.	0x0
19:16	R	AHB_DMA_WR_BUFF_CNT	The maximum number of arbiter clock cycles that an DMA AHB access has been buffered.	0x0
15:12	R	AHB_CPUC_WR_BUFF_CNT	The maximum number of arbiter clock cycles that an CPUC AHB access has been buffered.	0x0
11:8	R	AHB_CPUS_WR_BUFF_CNT	The maximum number of arbiter clock cycles that an CPUS_AHB access has been buffered.	0x0
7	W	AHB_SNC_CLR_WR_BUFF	Writing a 1 clears AHB_SNC_WR_BUFF_CNT.	0x0
6	W	AHB_DMA_CLR_WR_BUFF	Writing a 1 clears AHB_DMA_WR_BUFF_CNT.	0x0
5	W	AHB_CPUC_CLR_WR_BUFF	Writing a 1 clears AHB_CPUC_WR_BUFF_CNT.	0x0
4	W	AHB_CPUS_CLR_WR_BUFF	Writing a 1 clears AHB_CPUS_WR_BUFF_CNT.	0x0
3	R	AHB_SNC_WRITE_BUFF	0: No SNC AHB write access is buffered. 1: Currently a single SNC AHB write access is buffered in the arbiter.	0x0
2	R	AHB_DMA_WRITE_BUFF	0: No DMA AHB write access is buffered. 1: Currently a single DMA AHB write access is buffered in the arbiter.	0x0
1	R	AHB_CPUC_WRITE_BUFF	0: No CPUC AHB write access is buffered. 1: Currently a single CPUC AHB write access is buffered in the arbiter.	0x0
0	R	AHB_CPUS_WRITE_BUFF	0: No CPUS AHB write access is buffered. 1: Currently a single CPUS AHB write access is buffered in the arbiter.	0x0

Table 869: MEM_STATUS2_REG (0x50050018)

Bit	Mode	Symbol	Description	Reset
13	RW1C	RAM13_OFF_BUT_ACCESS	Reading a 1 indicates RAM13 was off but still access was performed.	0x0

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Bit	Mode	Symbol	Description	Reset
			Writing a 1 will clear the status back to 0.	
12	RW1C	RAM12_OFF_BUT_ACCESS	Reading a 1 indicates RAM12 was off but still access was performed. Writing a 1 will clear the status back to 0.	0x0
11	RW1C	RAM11_OFF_BUT_ACCESS	Reading a 1 indicates RAM11 was off but still access was performed. Writing a 1 will clear the status back to 0.	0x0
10	RW1C	RAM10_OFF_BUT_ACCESS	Reading a 1 indicates RAM10 was off but still access was performed. Writing a 1 will clear the status back to 0.	0x0
9	RW1C	RAM9_OFF_BUT_ACCESS	Reading a 1 indicates RAM9 was off but still access was performed. Writing a 1 will clear the status back to 0.	0x0
8	RW1C	RAM8_OFF_BUT_ACCESS	Reading a 1 indicates RAM8 was off but still access was performed. Writing a 1 will clear the status back to 0.	0x0
7	RW1C	RAM7_OFF_BUT_ACCESS	Reading a 1 indicates RAM7 was off but still access was performed. Writing a 1 will clear the status back to 0.	0x0
6	RW1C	RAM6_OFF_BUT_ACCESS	Reading a 1 indicates RAM6 was off but still access was performed. Writing a 1 will clear the status back to 0.	0x0
5	RW1C	RAM5_OFF_BUT_ACCESS	Reading a 1 indicates RAM5 was off but still access was performed. Writing a 1 will clear the status back to 0.	0x0
4	RW1C	RAM4_OFF_BUT_ACCESS	Reading a 1 indicates RAM4 was off but still access was performed. Writing a 1 will clear the status back to 0.	0x0
3	RW1C	RAM3_OFF_BUT_ACCESS	Reading a 1 indicates RAM3 was off but still access was performed. Writing a 1 will clear the status back to 0.	0x0
2	RW1C	RAM2_OFF_BUT_ACCESS	Reading a 1 indicates RAM2 was off but still access was performed. Writing a 1 will clear the status back to 0.	0x0
1	RW1C	RAM1_OFF_BUT_ACCESS	Reading a 1 indicates RAM1 was off but still access was performed. Writing a 1 will clear the status back to 0.	0x0
0	RW1C	RAM0_OFF_BUT_ACCESS	Reading a 1 indicates RAM0 was off but still access was performed. Writing a 1 will clear the status back to 0.	0x0

Table 870: CMI_CODE_BASE_REG (0x50050020)

Bit	Mode	Symbol	Description	Reset
31:20	R	-	Reserved	0x0
19:0	R	CMI_CODE_BASE_ADDR	Base address for CMAC code.	0x0

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Bit	Mode	Symbol	Description	Reset
			Note: Uses the CMAC Physical address space provided by System Memory Controller. That is, 0x0 is base for RAM10.	

Table 871: CMI_DATA_BASE_REG (0x50050024)

Bit	Mode	Symbol	Description	Reset
19:2	R/W	CMI_DATA_BASE_ADDR	Base address for CMAC data with steps of 4 bytes. 0x00001: 4 byte base address 0x00010: 64 byte base address 0x00100: 1 kB base address 0x01000: 16 kB base address 0x10000: 256 kB base address Note: Uses the CMAC Physical address space provided by System Memory Controller. That is, 0x0 is base for RAM10, 0x30000 is base for RAM9, 0x80000 is base for RAM11. This register should only be updated when CMAC is running on DIVN clock or is not running at all.	0x0
1:0	R	-	Reserved	0x0

Table 872: CMI_SHARED_BASE_REG (0x50050028)

Bit	Mode	Symbol	Description	Reset
19:10	R/W	CMI_SHARED_BASE_ADDR	Base address for CMAC shared data with steps of 1 kB. 0x001: 1 kB base address 0x010: 16 kB base address 0x100: 256 kB base address Note: CMAC address scheme is used and should only be used to point to RAM 9 or 10. Note: Uses the CMAC Physical address space provided by System Memory Controller. That is, 0x0 is base for RAM10, 0x30000 is base for RAM9. This register should only be updated when CMAC is running on DIVN clock or is not running at all.	0x0
9:0	R	-	Reserved	0x0

Table 873: CMI_END_REG (0x5005002C)

Bit	Mode	Symbol	Description	Reset
19:10	R/W	CMI_END_ADDR	End address for CMAC code and data accesses with steps of 1 kB. 0x000: accesses up to 1 kB are allowed	0x3FF

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Bit	Mode	Symbol	Description	Reset
			0x001: accesses up to 2 kB are allowed 0x01F: accesses up to 32 kB are allowed 0x1FF: accesses up to 512 kB are allowed Note: Uses the CMAC Physical address space provided by System Memory Controller. That is, 0x0 is base for RAM10, 0x30000 is base for RAM9, 0x80000 is base for RAM11. This register should only be updated when CMAC is running on DIVN clock or is not running at all.	
9:0	R	-	Reserved	0x3FF

Table 874: CMAC_STATUS_REG (0x50050030)

Bit	Mode	Symbol	Description	Reset
13	W	CMI_CLEAR_READY	Writing a 1 clears CMI_NOT_READY bit.	0x0
12	R	CMI_NOT_READY	0: Normal operation 1: CMI access performed which couldn't be handled right away (interface doesn't allow wait cycles)	0x0
11:8	R	AHB_RFMON_WR_BUFF_CNT	The maximum number of arbiter clock cycles that an CPUC AHB access has been buffered.	0x0
7:4	R	AHB_SYS2CMAC_WR_BUFF_CNT	The maximum number of arbiter clock cycles that an CPUS_AHB access has been buffered.	0x0
3	W	AHB_RFMON_CLR_WR_BUFF	Writing a 1 clears AHB_CPUC_WR_BUFF_CNT.	0x0
2	W	AHB_SYS2CMAC_CLR_WR_BUFF	Writing a 1 clears AHB_CPUS_WR_BUFF_CNT.	0x0
1	R	AHB_RFMON_WRITE_BUFF	0: No CPUC AHB write access is buffered. 1: Currently a single CPUC AHB write access is buffered in the arbiter.	0x0
0	R	AHB_SYS2CMAC_WRITE_BUFF	0: No CPUS AHB write access is buffered. 1: Currently a single CPUS AHB write access is buffered in the arbiter.	0x0

Table 875: BUSY_SET_REG (0x50050070)

Bit	Mode	Symbol	Description	Reset
31:30	WS	BUSY_SDADC	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
29:28	WS	BUSY_GPADC	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0).	0x0

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Bit	Mode	Symbol	Description	Reset
			Reading returns 0 to allow read/modify/write to the register.	
27:26	WS	BUSY_SRC2	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
25:24	WS	BUSY_SRC	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
23:22	WS	BUSY_PDM	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
21:20	WS	BUSY_PCM	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
19:18	WS	BUSY_I3C	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
17:16	WS	BUSY_I2C3	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
15:14	WS	BUSY_I2C2	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
13:12	WS	BUSY_I2C	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
11:10	WS	BUSY_SPI3	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
9:8	WS	BUSY_SPI2	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0

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Bit	Mode	Symbol	Description	Reset
7:6	WS	BUSY_SPI	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
5:4	WS	BUSY_UART3	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
3:2	WS	BUSY_UART2	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
1:0	WS	BUSY_UART	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0

Table 876: BUSY_SET_REG2 (0x50050074)

Bit	Mode	Symbol	Description	Reset
31:12	WS	-	Reserved	0x0
11:10	WS	BUSY_TIMER6	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
9:8	WS	BUSY_TIMER5	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
7:6	WS	BUSY_TIMER4	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
5:4	WS	BUSY_TIMER3	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0
3:2	WS	BUSY_TIMER2	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0

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Bit	Mode	Symbol	Description	Reset
1:0	WS	BUSY_TIMER	Writing a non-zero value to this field sets the corresponding BUSY bit, but only if it was not claimed (BUSY=0). Reading returns 0 to allow read/modify/write to the register.	0x0

Table 877: BUSY_RESET_REG (0x50050078)

Bit	Mode	Symbol	Description	Reset
31:30	RW1C	BUSY_SDADC	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
29:28	RW1C	BUSY_GPADC	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
27:26	RW1C	BUSY_SRC2	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
25:24	RW1C	BUSY_SRC	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
23:22	RW1C	BUSY_PDM	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
21:20	RW1C	BUSY_PCM	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
19:18	RW1C	BUSY_I3C	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
17:16	RW1C	BUSY_I2C3	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
15:14	RW1C	BUSY_I2C2	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
13:12	RW1C	BUSY_I2C	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0

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Bit	Mode	Symbol	Description	Reset
11:10	RW1C	BUSY_SPI3	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
9:8	RW1C	BUSY_SPI2	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
7:6	RW1C	BUSY_SPI	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
5:4	RW1C	BUSY_UART3	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
3:2	RW1C	BUSY_UART2	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
1:0	RW1C	BUSY_UART	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0

Table 878: BUSY_RESET_REG2 (0x5005007C)

Bit	Mode	Symbol	Description	Reset
31:12	RW1C	-	Reserved	0x0
11:10	RW1C	BUSY_TIMER6	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
9:8	RW1C	BUSY_TIMER5	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
7:6	RW1C	BUSY_TIMER4	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
5:4	RW1C	BUSY_TIMER3	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0
3:2	RW1C	BUSY_TIMER2	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0

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Bit	Mode	Symbol	Description	Reset
1:0	RW1C	BUSY_TIMER	Clear the BUSY bitfield, by writing the master code which has claimed to this field Reading returns 0 to allow read/modify/write to the register.	0x0

Table 879: BUSY_STAT_REG (0x50050080)

Bit	Mode	Symbol	Description	Reset
31:30	R	BUSY_SDADC	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
29:28	R	BUSY_GPADC	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
27:26	R	BUSY_SRC2	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
25:24	R	BUSY_SRC	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
23:22	R	BUSY_PDM	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
21:20	R	BUSY_PCM	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
19:18	R	BUSY_I3C	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
17:16	R	BUSY_I2C3	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
15:14	R	BUSY_I2C2	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
13:12	R	BUSY_I2C	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
11:10	R	BUSY_SPI3	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
9:8	R	BUSY_SPI2	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
7:6	R	BUSY_SPI	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
5:4	R	BUSY_UART3	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
3:2	R	BUSY_UART2	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
1:0	R	BUSY_UART	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0

Table 880: BUSY_STAT_REG2 (0x50050084)

Bit	Mode	Symbol	Description	Reset
31:12	R	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
11:10	R	BUSY_TIMER6	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
9:8	R	BUSY_TIMER5	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
7:6	R	BUSY_TIMER4	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
5:4	R	BUSY_TIMER3	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
3:2	R	BUSY_TIMER2	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0
1:0	R	BUSY_TIMER	A non-zero value indicates the resource is busy. The value represents which master is using it.	0x0

44.19 Octa/Quad-SPI Flash Controller Registers

Table 881: Register map OQSPIF

Address	Register	Description
0x36000000	OQSPIF_CTRLBUS_REG	SPI Bus control register for the Manual mode
0x36000004	OQSPIF_CTRLMODE_REG	Mode Control register
0x36000008	OQSPIF_RECVDATA_REG	Received data for the Manual mode
0x3600000C	OQSPIF_BURSTCMDA_REG	The way of reading in Auto mode (command register A)
0x36000010	OQSPIF_BURSTCMDB_REG	The way of reading in Auto mode (command register B)
0x36000014	OQSPIF_STATUS_REG	The status register of the OSPI controller
0x36000018	OQSPIF_WRITEDATA_REG	Write data to SPI Bus for the Manual mode
0x3600001C	OQSPIF_READDATA_REG	Read data from SPI Bus for the Manual mode
0x36000020	OQSPIF_DUMMYDATA_REG	Send dummy clocks to SPI Bus for the Manual mode
0x36000024	OQSPIF_ERASECTRL_REG	OSPI Erase control register
0x36000028	OQSPIF_ERASECMDA_REG	The way of erasing in Auto mode (command register A)
0x3600002C	OQSPIF_ERASECMDB_REG	The way of erasing in Auto mode (command register B)
0x36000030	OQSPIF_ERASECMDC_REG	The way of erasing in Auto mode (command register C)
0x36000034	OQSPIF_BURSTBRK_REG	Read break sequence in Auto mode

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Address	Register	Description
0x36000038	OQSPIF_STATUSCMD_REG	The way of reading the status of external device in Auto mode
0x3600003C	OQSPIF_CHCKERASE_REG	Check erase progress in Auto mode
0x36000040	OQSPIF_GP_REG	OSPI General Purpose control register
0x36000100	OQSPIF_CTR_CTRL_REG	Control register for the decryption engine of the OSPIC
0x36000104	OQSPIF_CTR_SADDR_REG	Start address of the encrypted content in the OSPI flash
0x36000108	OQSPIF_CTR_EADDR_REG	End address of the encrypted content in the OSPI flash
0x3600010C	OQSPIF_CTR_NONCE_0_3_REG	Nonce bytes 0 to 3 for the AES-CTR algorithm
0x36000110	OQSPIF_CTR_NONCE_4_7_REG	Nonce bytes 4 to 7 for the AES-CTR algorithm
0x36000114	OQSPIF_CTR_KEY_0_3_REG	Key bytes 0 to 3 for the AES-CTR algorithm
0x36000118	OQSPIF_CTR_KEY_4_7_REG	Key bytes 4 to 7 for the AES-CTR algorithm
0x3600011C	OQSPIF_CTR_KEY_8_11_REG	Key bytes 8 to 11 for the AES-CTR algorithm
0x36000120	OQSPIF_CTR_KEY_12_15_REG	Key bytes 12 to 15 for the AES-CTR algorithm
0x36000124	OQSPIF_CTR_KEY_16_19_REG	Key bytes 16 to 19 for the AES-CTR algorithm
0x36000128	OQSPIF_CTR_KEY_20_23_REG	Key bytes 20 to 23 for the AES-CTR algorithm
0x3600012C	OQSPIF_CTR_KEY_24_27_REG	Key bytes 24 to 27 for the AES-CTR algorithm
0x36000130	OQSPIF_CTR_KEY_28_31_REG	Key bytes 28 to 31 for the AES-CTR algorithm

Table 882: OQSPIF_CTRLBUS_REG (0x36000000)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5	W	OSPIC_DIS_CS	Write 1 to disable the chip select (active low) when the controller is in Manual mode.	0x0
4	W	OSPIC_EN_CS	Write 1 to enable the chip select (active low) when the controller is in Manual mode.	0x0
3	W	OSPIC_SET_OCTAL	Write 1 to set the bus mode in Octal mode when the controller is in Manual mode.	0x0
2	W	OSPIC_SET_QUAD	Write 1 to set the bus mode in Quad mode when the controller is in Manual mode.	0x0
1	W	OSPIC_SET_DUAL	Write 1 to set the bus mode in Dual mode when the controller is in Manual mode.	0x0

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Bit	Mode	Symbol	Description	Reset
0	W	OSPIC_SET_SINGLE	Write 1 to set the bus mode in Single SPI mode when the controller is in Manual mode.	0x0

Table 883: OQSPIF_CTRLMODE_REG (0x36000004)

Bit	Mode	Symbol	Description	Reset
31:28	R/W	OSPIC_IO_UH_DAT	The value of OSPI_IO4-7 pads if OSPI_IO_UH_OEN is 1	0x0
27	R/W	OSPIC_IO_UH_OEN	Forces the output enable for the upper half of the OSPI bus (OSPI_IO4-7). Set this bit to 1 only in SPI, Dual or Quad SPI mode to control the upper half of the OSPI bus. When the Octal SPI is enabled in the flash device, set this bit to zero. 0: The OSPI_IO4-7 pad direction is decided by the controller. 1: The OSPI_IO4-7 pad are outputs. The output values are defined by the corresponding OSPIC_IO_UH_DAT bits.	0x0
26:19	-	-	Reserved	0x0
18	R/W	OSPIC_INC_LIM_EN	This bit has meaning only for the read in auto mode and only when the read access in the AHB bus is an incremental burst of unspecified length. 0: The length of the burst is considered as unspecified. The access in the flash device will be implemented as is defined by the OSPIC BUF_LIM_EN bit. 1: The length of the burst is considered as equal to 8-bytes. The access in the flash device will be implemented by the controller as one or more different bursts, until to be served the access in the AHB bus. Each burst in the flash device will have maximum length of 8 bytes. The setting OSPIC_INC_LIM_EN=1 is useful if we know that the masters that make use of the incremental burst of unspecified length, require no more than 8 bytes.	0x0
17	R/W	OSPIC_RD_ERR_EN	Controls the generation of AHB bus error response when a read is performed in the address space where the flash device is mapped and the Auto mode is not enabled. 0: The controller ignores the access. There is no error response due to the read access. 1: The controller responds with an AHB error response.	0x0
16	R/W	OSPIC_MAN_DIRCHG_MD	Selection of the direction change method in manual mode. 0 : the bus direction goes to input after each access 1 : the bus direction goes to input only after a dummy access	0x0
15	R/W	OSPIC_DMY_MD	Defines the clock cycle where the bus will turn in Hi-z during the transmission of dummy bytes. This is applicable in both Manual and Auto mode.	0x0

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Bit	Mode	Symbol	Description	Reset
			0 : the bus will become Hi-Z on the last clock 1 : the bus will become Hi-Z on the last two clocks	
14	R/W	OSPIC_CMD_X2_EN	Defines the number of bytes that consist the instruction code in the command sequences that produced by the OSPIC during Auto mode. 0 : The instruction code is one byte only. 1 : The instruction code is two bytes. The second byte of the instruction code is the inverse of the first byte. The command sequence that is produced by the OSPIC_BURSTBRK_REG is not affected by this setting.	0x0
13	R/W	OSPIC_USE_32BA	Controls the length of the address that the external memory device uses. 0: The external memory device uses 24 bits address. 1: The external memory device uses 32 bits address. The controller uses this bit in order to decide the number of the address bytes that has to transfer to the external device during Auto mode.	0x0
12	R/W	OSPIC_BUF_LIM_EN	This bit has meaning only for the read in auto mode. Defines the behavior of the controller when the internal buffer is full and there are more data to be retrieved for the current burst. 0: The access in the flash device is not terminated when the internal buffer has no empty space. In this case the OSPI_SCK clock is blocked until to free space in the internal buffer. 1: The access in the flash device is terminated when the internal buffer has no empty space. A new access in the flash device will be initiated when will be requested addresses that are not present in the internal buffer. In both cases the access in the flash device is terminated when there is no any read request.	0x0
11:9	R/W	OSPIC_PCLK_MD	Read pipe clock delay relative to the falling edge of OSPI_SCK. Refer to OSPI Timing for timing parameters and recommended values: 0 to 7	0x0
8	R/W	OSPIC_RPIPE_EN	Controls the use of the data read pipe. 0: The read pipe is disabled; the sampling clock is defined according to the OSPIC_RXD_NEG setting. 1: The read pipe is enabled. The delay of the sampling clock is defined according to the OSPICI_PCLK_MD setting. (Recommended)	0x0
7	R/W	OSPIC_RXD_NEG	Defines the clock edge that is used for the capturing of the received data, when the read pipe is not active (OSPIC_RPIPE_EN = 0). 0: Sampling of the received data with the positive edge of the OSPI_SCK	0x0

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Bit	Mode	Symbol	Description	Reset
			1: Sampling of the received data with the negative edge of the OSPI_SCK The internal OSPI_SCK clock that is used by the controller for the capturing of the received data has a skew in respect of the OSPI_SCK that is received by the external memory device. In order to be improved the timing requirements of the read path, the controller supports a read pipe register with programmable clock delay. See also the OSPIC_RPIPE_EN register.	
6	R/W	OSPIC_HRDY_MD	This configuration bit is useful when the frequency of the OSPI clock is much lower than the clock of the AMBA bus, in order to not locks the AMBA bus for a long time. 0: Adds wait states via hready signal when an access is performed on the OSPIC_CTRLBUS_REG, OSPIC_WRITEDATA, OSPIC_READDATA and OSPIC_DUMMYDATA registers. It is not needed to check the OSPIC_BUSY of the OSPIC_STATUS_REG. 1: The controller don't adds wait states via the hready signal, when is performed access on the OSPIC_CTRLBUS_REG, OSPIC_WRITEDATA, OSPIC_READDATA and OSPIC_DUMMYDATA registers. The OSPIC_BUSY bit of the OSPIC_STATUS_REG must be checked in order to be detected the completion of the requested access. It is applicable only when the controller is in Manual mode. In the case of the Auto mode, the controller always adds wait states via the hready signal.	0x0
5	R/W	OSPIC_IO3_DAT	The value of OSPI_IO3 pad if OSPI_IO3_OEN is 1	0x0
4	R/W	OSPIC_IO2_DAT	The value of OSPI_IO2 pad if OSPI_IO2_OEN is 1	0x0
3	R/W	OSPIC_IO3_OEN	Forces the output enable of the OSPI_IO3. Set this bit to 1 only in SPI or Dual SPI mode to control the /HOLD signal. When the Quad or Octal SPI is enabled in the flash device, set this bit to zero. 0: The OSPI_IO3 pad direction is decided by the controller. 1: The OSPI_IO3 pad is output. The output value is defined by the OSPIC_IO3_DAT.	0x0
2	R/W	OSPIC_IO2_OEN	Forces the output enable of the OSPI_IO2. Set this bit to 1 only in SPI or Dual SPI mode to control the /WP signal. When the Quad or Octal SPI is enabled in the flash device, set this bit to zero. 0: The OSPI_IO2 pad direction is decided by the controller. 1: The OSPI_IO2 pad is output. The output value is defined by the OSPIC_IO2_DAT.	0x0

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Bit	Mode	Symbol	Description	Reset
1	R/W	OSPIC_CLK_MD	Mode of the generated OSPI_SCK clock 0: Use Mode 0 for the OSPI_CLK. The OSPI_SCK is low when OSPI_CS is high. 1: Use Mode 3 for the OSPI_CLK. The OSPI_SCK is high when OSPI_CS is high.	0x0
0	R/W	OSPIC_AUTO_MD	Mode of operation 0: The Manual Mode is selected. 1: The Auto Mode is selected. During an erasing the OSPIC_AUTO_MD goes in read only mode (see OSPIC_ERASE_EN)	0x0

Table 884: OQSPIF_RECVDATA_REG (0x36000008)

Bit	Mode	Symbol	Description	Reset
31:0	R	OSPIC_RECVDATA	This register contains the received data when the OSPIC_READDATA_REG register is used in Manual mode, in order to be retrieved data from the external memory device and OSPIC_HRDY_MD=1 && OSPIC_BUSY=0.	0x0

Table 885: OQSPIF_BURSTCMDA_REG (0x3600000C)

Bit	Mode	Symbol	Description	Reset
31:30	R/W	OSPIC_DMY_TX_MD	It describes the mode of the SPI bus during the Dummy bytes phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Octal	0x0
29:28	R/W	OSPIC_EXT_TX_MD	It describes the mode of the SPI bus during the Extra Byte phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Octal	0x0
27:26	R/W	OSPIC_ADR_TX_MD	It describes the mode of the SPI bus during the address phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Octal	0x0
25:24	R/W	OSPIC_INST_TX_MD	It describes the mode of the SPI bus during the instruction phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Octal	0x0

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Bit	Mode	Symbol	Description	Reset
23:16	R/W	OSPIC_EXT_BYTE	The value of an extra byte which will be transferred after address (only if OSPIC_EXT_BYTE_EN= 1). Usually this is the Mode Bits in Dual/Quad/Octal SPI I/O instructions.	0x0
15:8	R/W	OSPIC_INST_WB	Instruction Value for Wrapping Burst. This value is the selected instruction when OSPIC_WRAP_MD is equal to 1 and the access is a wrapping burst of length and size described by the bit fields OSPIC_WRAP_LEN and OSPIC_WRAP_SIZE respectively.	0x0
7:0	R/W	OSPIC_INST	Instruction Value for Incremental Burst or Single read access. This value is the selected instruction at the cases of incremental burst or single read access. Also this value is used when a wrapping burst is not supported (OSPIC_WRAP_MD)	0x0

Table 886: OQSPIF_BURSTCMDB_REG (0x36000010)

Bit	Mode	Symbol	Description	Reset
31:19	-	-	Reserved	0x0
18:16	R/W	OSPIC_CS_HIGH_MIN	Between the transmissions of two different instructions to the flash memory, the SPI bus stays in idle state (OSPI_CS high) for at least this number of OSPI_SCK clock cycles. See the OSPIC_ERS_CS_HI register for some exceptions.	0x0
15:14	R/W	OSPIC_WRAP_SIZE	It describes the selected data size of a wrapping burst (OSPIC_WRAP_MD). 0x0: byte access (8-bits) 0x1: half word access (16 bits) 0x2: word access (32-bits) 0x3: Reserved	0x0
13:12	R/W	OSPIC_WRAP_LEN	It describes the selected length of a wrapping burst (OSPIC_WRAP_MD). 0x0: 4 beat wrapping burst 0x1: 8 beat wrapping burst 0x2: 16 beat wrapping burst 0x3: Reserved	0x0
11	R/W	OSPIC_WRAP_MD	Wrap mode 0: The OSPIC_INST is the selected instruction at any access. 1: The OSPIC_INST_WB is the selected instruction at any wrapping burst access of length and size described by the registers OSPIC_WRAP_LEN and OSPIC_WRAP_SIZE respectively. In all other cases the OSPIC_INST is the selected instruction. Use this feature only when the serial FLASH memory supports a special instruction for wrapping burst access.	0x0
10	R/W	OSPIC_INST_MD	Instruction mode 0: Transmit instruction at any burst access. 1: Transmit instruction only in the first access after the selection of Auto Mode.	0x0

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Bit	Mode	Symbol	Description	Reset
9	R/W	OSPIC_DMY_EN	Dummy bytes enable 0: Don't send the dummy bytes 1: Send the dummy bytes. The number of the dummy bytes is defined by the OSPIC_DMY_NUM.	0x0
8:4	R/W	OSPIC_DMY_NUM	Number of dummy bytes (minus 1). Can be set 1 up to 32 dummy bytes (values 0 up to 31). The dummy bytes are appied only when OSPIC_DMY_EN=1.	0x0
3	R/W	OSPIC_EXT_HF_DS	Extra half disable output 0: if OSPIC_EXT_BYTE_EN=1, is transmitted the complete OSPIC_EXT_BYTE 1: if OSPIC_EXT_BYTE_EN=1, the output is disabled (hi-z) during the transmission of bits [3:0] of OSPIC_EXT_BYTE. This setting has no meaning if the extra byte is transferred in Octal mode. In this case keep this bit to zero value.	0x0
2	R/W	OSPIC_EXT_BYTE_EN	Extra byte enable 0: Don't send the OSPIC_EXT_BYTE 1: Send the OSPIC_EXT_BYTE	0x0
1:0	R/W	OSPIC_DAT_RX_MD	It describes the mode of the SPI bus during the data phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Octal	0x0

Table 887: OQSPIF_STATUS_REG (0x36000014)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	OSPIC_BUSY	The status of the SPI Bus. 0: The SPI Bus is idle 1: The SPI Bus is active. Read data, write data or dummy data activity is in progress. Has meaning only in Manual mode and only when OSPIC_HRDY_MD = 1.	0x0

Table 888: OQSPIF_WRITEDATA_REG (0x36000018)

Bit	Mode	Symbol	Description	Reset
31:0	W	OSPIC_WRITEDATA	Writing to this register is generating a data transfer from the controller to the external memory device. The data written in this register, is then transferred to the memory using the selected mode of the SPI bus (Single SPI, Dual SPI, Quad SPI or Octal	0x0

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Bit	Mode	Symbol	Description	Reset
			SPI). The data size of the access to this register can be 32-bits / 16-bits/ 8-bits and is equal to the number of the transferred bits. This register has meaning only when the controller is in Manual mode.	

Table 889: OQSPIF_READDATA_REG (0x3600001C)

Bit	Mode	Symbol	Description	Reset
31:0	R	OSPIC_READDATA	A read access at this register generates a data transfer from the external memory device to the OSPIC controller. The data is transferred using the selected mode of the SPI bus (Single SPI, Dual SPI, Quad SPI or Octal SPI). The data size of the access to this register can be 32-bits / 16-bits / 8-bits and is equal to the number of the transferred bits. This register has meaning only when the controller is in Manual mode.	0x0

Table 890: OQSPIF_DUMMYDATA_REG (0x36000020)

Bit	Mode	Symbol	Description	Reset
31:0	W	OSPIC_DUMMYDATA	Writing to this register generates a number of clock pulses to the SPI bus. During the last clock of this activity in the SPI bus, the OSPI_IOx data pads are in hi-z state (see also the OSPIC_DMY_MD). The data size of the access to this register can be 32-bits / 16-bits/ 8-bits. The number of generated pulses is equal to: (size of AHB bus access) / (size of SPI bus). The size of SPI bus is equal to 1, 2, 4 or 8 for Single, Dual, Quad or Octal SPI mode respectively. This register has meaning only when the controller is in Manual mode.	0x0

Table 891: OQSPIF_ERASECTRL_REG (0x36000024)

Bit	Mode	Symbol	Description	Reset
31:29	-	-	Reserved	0x0
28	R/W	OSPIC_ERS_RES_DIS	This configuration bit has meaning when an erase has been suspended. Normally the erase will be resumed when the flash will stay idle (without read accesses) for a predefined number of clock cycles (see OSPIC_ERASECMDB_REG [OSPIC_ERSRES_HLD]). By setting this bit the execution of the erase resume process can be postponed. 0: A suspended erase will be resumed based on the setting in the OSPIC_ERSRES_HLD. 1: The erase will not be resumed even after the expiration of the OSPIC_ERSRES_HLD. The	0x0

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Bit	Mode	Symbol	Description	Reset
			erase can be resumed again only when the OSPIC_ERS_RES_DIS=0.	
27:25	R	OSPIC_ERS_STATE	It shows the progress of sector/block erasing (read only). 0x0: No Erase. 0x1: Pending erase request 0x2: Erase procedure is running 0x3: Suspended Erase procedure 0x4: Finishing the Erase procedure 0x5..0x7: Reserved	0x0
24	R/W	OSPIC_ERASE_EN	During Manual mode (OSPIC_AUTO_MD = 0). This bit is in read only mode. During Auto mode (OSPIC_AUTO_MD = 1). To request the erasing of the block/sector (OSPIC_ERS_ADDR, 12'b0) write 1 to this bit. This bit is cleared automatically with the end of the erasing. Until the end of erasing the OSPIC_ERASE_EN remains in read only mode. During the same time interval the controller remains in Auto Mode (OSPIC_AUTO_MD goes in read only mode).	0x0
23:4	R/W	OSPIC_ERS_ADDR	Defines the address of the block/sector that is requested to be erased. If OSPIC_USE_32BA = 0 (24 bits addressing), bits OSPIC_ERASECTRL_REG[23-12] determine the block/ sector address bits [23-12]. The OSPIC_ERASECTRL_REG[11-4] are ignored by the controller. If OSPIC_USE_32BA = 1 (32 bits addressing) bits OSPIC_ERASECTRL_REG[23-4] determine the block / sectors address bits [31:12]	0x0
3:0	-	-	Reserved	0x0

Table 892: OQSPIF_ERASECMDA_REG (0x36000028)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	OSPIC_RES_INST	The code value of the erase resume instruction	0x0
23:16	R/W	OSPIC_SUS_INST	The code value of the erase suspend instruction.	0x0
15:8	R/W	OSPIC_WEN_INST	The code value of the write enable instruction.	0x0
7:0	R/W	OSPIC_ERS_INST	The code value of the erase instruction.	0x0

Table 893: OQSPIF_ERASECMDB_REG (0x3600002C)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	OSPIC_RESSUS_DLY	Defines a timer that counts the minimum allowed delay between an erase suspend command and the previous erase resume command (or the initial erase command). 0: Don't wait. The controller starts immediately to suspend the erase procedure.	0x0

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Bit	Mode	Symbol	Description	Reset
			1..255: The controller waits for at least this number of 222kHz clock cycles before the suspension of erasing. Time starts counting after the end of the previous erase resume command (or the initial erase command)	
23:20	-	-	Reserved	0x0
19:16	R/W	OSPIC_ERSRES_HLD	The controller must stay without flash memory reading requests for this number of AMBA hclk clock cycles, before to perform the command of erase or erase resume 15 - 0	0x0
15	-	-	Reserved	0x0
14:10	R/W	OSPIC_ERS_CS_HI	After the execution of instructions: write enable, erase, erase suspend and erase resume, the OSPI_CS remains high for at least this number of OSPI bus clock cycles.	0x0
9:8	R/W	OSPIC_EAD_TX_MD	The mode of the OSPI Bus during the address phase of the erase instruction 0x0: Single 0x1: Dual 0x2: Quad 0x3: Octal	0x0
7:6	R/W	OSPIC_RES_TX_MD	The mode of the OSPI Bus during the transmission of the resume instruction 0x0: Single 0x1: Dual 0x2: Quad 0x3: Octal	0x0
5:4	R/W	OSPIC_SUS_TX_MD	The mode of the OSPI Bus during the transmission of the suspend instruction. 0x0: Single 0x1: Dual 0x2: Quad 0x3: Octal	0x0
3:2	R/W	OSPIC_WEN_TX_MD	The mode of the OSPI Bus during the transmission of the write enable instruction. 0x0: Single 0x1: Dual 0x2: Quad 0x3: Octal	0x0
1:0	R/W	OSPIC_ERS_TX_MD	The mode of the OSPI Bus during the instruction phase of the erase instruction 0x0: Single 0x1: Dual 0x2: Quad 0x3: Octal	0x0

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Table 894: OQSPIF_ERASECMDC_REG (0x36000030)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	OSPIC_SUSSTS_DLY	Defines a timer that counts the minimum allowed delay between an erase suspend command and the next read status command. 0: Don't wait. The controller starts immediately to read the status of the flash device. 1..63: The controller waits for at least this number of 222kHz clock cycles before to read the status of the flash device. Time starts counting when the erase resume command is applied.	0x0

Table 895: OQSPIF_BURSTBRK_REG (0x36000034)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23	R/W	OSPIC_BRK_EN	Controls the application of a special command (read burst break sequence) that is used in order to force the device to abandon the continuous read mode. 0: The special command is not applied 1: The special command is applied This special command is applied by the controller to the external device under the following conditions: - the controller is in Auto mode - the OSPIC_INST_MD = 1 - the previous command that has been applied in the external device was read - the controller want to apply to the external device a command different than the read.	0x0
22	R/W	OSPIC_SEC_HF_DS	Disable output during the transmission of the second half (OSPIC_BRK_WRD[3:0]). Setting this bit is only useful if OSPIC_BRK_EN =1 and OSPIC_BRK_SZ >= 1. It is not applicable when the sequence is transferred in Octal mode (OSPIC_BRK_TX_MD=3). 0: The controller drives the OSPI bus during the transmission of the OSPIC_BRK_WRD[3:0]. 1: The controller leaves the OSPI bus in Hi-Z during the transmission of the OSPIC_BRK_WORD[3:0].	0x0
21:20	R/W	OSPIC_BRK_TX_MD	The mode of the OSPI Bus during the transmission of the burst break sequence. 0x0: Single 0x1: Dual 0x2: Quad 0x3: Octal	0x0
19:16	R/W	OSPIC_BRK_SZ	The size of Burst Break Sequence 0: One byte (Send OSPIC_BRK_WRD[15:8]) 1: Two bytes (Send OSPIC_BRK_WRD[15:0])	0x0

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Bit	Mode	Symbol	Description	Reset
			2-15: Three up to 16 bytes will be transferred. All the bytes that will be transferred will have the value of the OSPIC_BRK_WRD[15:8], except of the last byte that will be the OSPIC_BRK_WRD[7:0].	
15:0	R/W	OSPIC_BRK_WRD	This is the value of a special command (read burst break sequence) that is applied by the controller to the external memory device, in order to force the memory device to abandon the continuous read mode.	0x0

Table 896: OQSPIF_STATUSCMD_REG (0x36000038)

Bit	Mode	Symbol	Description	Reset
31	-	-	Reserved	0x0
30	R/W	OSPIC_RSTAT_DMY_ZERO	Defines the value of that is transferred on the OSPI bus during the phase of the dummy bytes. 0: The controller keeps the data in the bus unchanged, until to change the bus direction in input mode. 1: Forces the dummy bytes to get the zero value (only for the cycles that are not in input mode). Only the IO pins that are related with the transfer mode of the dummy bytes (OSPIC_RSTAT_DMY_TX_MD) will get the zero value.	0x0
29:28	R/W	OSPIC_RSTAT_DMY_TX_MD	It describes the mode of the OSPI bus during the dummy bytes phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Octal	0x0
27:24	R/W	OSPIC_RSTAT_DMY_NUM	Number of dummy bytes (minus 1). Can be set 1 up to 16 dummy bytes (values 0 up to 15). The dummy bytes are applied only when OSPIC_RSTAT_DMY_EN=1.	0x0
23	R/W	OSPIC_RSTAT_DMY_EN	Enables the transmission of dummy bytes, immediately after the instruction code of the read status command. 0: Don't send the dummy bytes 1: Send the dummy bytes. The number of the dummy bytes is defined by the OSPIC_RSTAT_DMY_NUM.	0x0
22	R/W	OSPIC_STSDLY_SEL	Defines the timer which is used to count the delay that it has to wait before to read the FLASH Status Register, after an erase or an erase resume command. 0: The delay is controlled by the OSPIC_RESSTS_DLY which counts on the OSPI_CLK clock. 1: The delay is controlled by the OSPIC_RESSUS_DLY which counts on the 222 kHz clock.	0x0

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Bit	Mode	Symbol	Description	Reset
21:16	R/W	OSPIC_RESSTS_DLY	Defines a timer that counts the minimum required delay between the reading of the status register and of the previous erase or erase resume instruction. 0: Don't wait. The controller starts to reading the Flash memory status register immediately. 1..63: The controller waits for at least this number of OSPI_CLK cycles and afterwards it starts to reading the Flash memory status register. The timer starts to count after the end of the previous erase or erase resume command. The actual timer that will be used by the controller before the reading of the Flash memory status register is defined by the OSPIC_STSDLY_SEL.	0x0
15	R/W	OSPIC_BUSY_VAL	Defines the value of the Busy bit which means that the flash is busy. 0: The flash is busy when the Busy bit is equal to 0. 1: The flash is busy when the Busy bit is equal to 1.	0x0
14:12	R/W	OSPIC_BUSY_POS	It describes who from the bits of status represents the Busy bit (7 - 0).	0x0
11:10	R/W	OSPIC_RSTAT_RX_MD	The mode of the OSPI Bus during the receive status phase of the read status instruction 0x0: Single 0x1: Dual 0x2: Quad 0x3: Octal	0x0
9:8	R/W	OSPIC_RSTAT_TX_MD	The mode of the OSPI Bus during the instruction phase of the read status instruction. 0x0: Single 0x1: Dual 0x2: Quad 0x3: Octal	0x0
7:0	R/W	OSPIC_RSTAT_INST	The code value of the read status instruction. It is transmitted during the instruction phase of the read status instruction.	0x0

Table 897: OQSPIF_CHCKERASE_REG (0x3600003C)

Bit	Mode	Symbol	Description	Reset
31:0	W	OSPIC_CHCKERASE	Writing any value to this register during erasing, forces the controller to read the flash memory status register. Depending on the value of the Busy bit, it updates the OSPIC_ERASE_EN.	0x0

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Table 898: OQSPIF_GP_REG (0x36000040)

Bit	Mode	Symbol	Description	Reset
4:3	R/W	OSPIC_PADS_SLEW	QSPI pads slew rate control. Indicative values under certain conditions: 0: Rise=1.7 V/ns, Fall=1.9 V/ns (weak) 1: Rise=2.0 V/ns, Fall=2.3 V/ns 2: Rise=2.3 V/ns, Fall=2.6 V/ns 3: Rise=2.4 V/ns, Fall=2.7 V/ns (strong) Conditions: FLASH pin capacitance 6 pF, Vcc=1.8V, T=25C and Idrive=16mA.	0x0
2:1	R/W	OSPIC_PADS_DRV	QSPI pads drive current 0: 4 mA 1: 8 mA 2: 12 mA 3: 16 mA	0x0
0	-	-	Reserved	0x0

Table 899: OQSPIF_CTR_CTRL_REG (0x36000100)

Bit	Mode	Symbol	Description	Reset
0	R/W	OSPIC_CTR_EN	Controls the AES-CTR decryption feature of the OSPIC, which enables the decryption (on-the-fly) of the data that are retrieved from the flash memory device. 0: The AES-CTR decryption is disabled. 1: The controller will decrypt the content of the flash memory device that is placed in the address space that is defined by the OSPIC_CTR_SADDR_REG and OSPIC_CTR_EADDR_REG registers. The data that are placed outside the previous space are not decrypted by the OSPIC. The decryption is performed by using the AES-CTR algorithm. The AES key is defined by the OSPIC_CTR_KEY_x_y_REG registers and the nonce value by the OSPIC_CTR_NONCE_x_y_REG registers. This configuration bit has meaning only while the controller is in Auto mode. The on-the-fly decryption is not provided in Manual mode.	0x0

Table 900: OQSPIF_CTR_SADDR_REG (0x36000104)

Bit	Mode	Symbol	Description	Reset
31:10	R/W	OSPIC_CTR_SADDR	Defines the bits [31:10] of the start address in the flash memory, where an encrypted image is placed. The bits [9:0] are considered always as zero. This has meaning only when the decryption is active. See also the register OSPIC_CTR_CTRL_REG[OSPIC_CTR_EN].	0x0
9:0	-	-	Reserved	0x0

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Table 901: OQSPIF_CTR_EADDR_REG (0x36000108)

Bit	Mode	Symbol	Description	Reset
31:10	R/W	OSPIC_CTR_EADDR	Defines the bits [31:10] of the end address in the flash memory, where an encrypted image is placed. The bits [9:0] are considered always as 0x3ff. This has meaning only when the decryption is active. See also the register OSPIC_CTR_CTRL_REG[OSPIC_CTR_EN].	0x0
9:0	-	-	Reserved	0x3FF

Table 902: OQSPIF_CTR_NONCE_0_3_REG (0x3600010C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	OSPIC_CTR_NONCE_0_3	Defines the 8 bytes of the nonce value (N0 - N7) that is used by the AES-CTR algorithm in order to be constructed the counter block (CTRB). The total size of the counter block is 128 bits or 16 bytes : CTRB0 CTRB1 CTRB2 CTRB3...CTRB14 CTRB15. The first 8 bytes (CTRB0 - CTRB7) of the counter block consisted by the nonce value. The next 8 bytes of the counter block (CTRB8-CTRB15), are produced automatically by the hardware based on the address offset inside the encrypted image, from where are retrieved the requested data. The mapping of the nonce bytes to the corresponding OSPIC_NONCE_X_Y_REG registers is the following : {CTRB0, CTRB1, CTRB2, CTRB3} = {N0, N1, N2, N3} = OSPIC_NONCE_0_3_REG[31:0] {CTRB4, CTRB5, CTRB6, CTRB7} = {N4, N5, N6, N7} = OSPIC_NONCE_4_7_REG[31:0] All these registers make sense only when OSPIC_CTR_CTRL_REG[OSPIC_CTR_EN] = 1. Do not perform access to an encrypted address range while the updating process of the nonce value is in progress.	0x0

Table 903: OQSPIF_CTR_NONCE_4_7_REG (0x36000110)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	OSPIC_CTR_NONCE_4_7	See the description in the OSPIC_NONCE_0_3.	0x0

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Table 904: OQSPIF_CTR_KEY_0_3_REG (0x36000114)

Bit	Mode	Symbol	Description	Reset
31:0	W	OSPIC_CTR_KEY_0_3	Defines the key that is used by the AES-CTR algorithm, when the on-the-fly decryption is enabled (OSPIC_CTR_CTRL_REG[OSPIC_CTR_EN] = 1). The size of the decryption key is 256bits or 32 bytes : K0 K1 K2 K3...K30 K31. The mapping of the bytes to the corresponding OSPIC_CTR_KEY_X_Y_REG registers is the following : {K0, K1, K2, K3} = OSPIC_CTR_KEY_0_3_REG[31:0] {K4, K5, K6, K7} = OSPIC_CTR_KEY_4_7_REG[31:0] {K8, K9, K10, K11} = OSPIC_CTR_KEY_8_11_REG[31:0] {K12, K13, K14, K15} = OSPIC_CTR_KEY_12_15_REG[31:0] {K16, K17, K18, K19} = OSPIC_CTR_KEY_16_19_REG[31:0] {K20, K21, K22, K23} = OSPIC_CTR_KEY_20_23_REG[31:0] {K24, K25, K26, K27} = OSPIC_CTR_KEY_24_27_REG[31:0] {K28, K29, K30, K31} = OSPIC_CTR_KEY_28_31_REG[31:0] All these registers make sense only when OSPIC_CTR_CTRL_REG[OSPIC_CTR_EN] = 1. Do not perform access to an encrypted address range while the updating process of the decryption key is in progress.	0x0

Table 905: OQSPIF_CTR_KEY_4_7_REG (0x36000118)

Bit	Mode	Symbol	Description	Reset
31:0	W	OSPIC_CTR_KEY_4_7	See the description in the OSPIC_CTR_KEY_0_3.	0x0

Table 906: OQSPIF_CTR_KEY_8_11_REG (0x3600011C)

Bit	Mode	Symbol	Description	Reset
31:0	W	OSPIC_CTR_KEY_8_11	See the description in the OSPIC_CTR_KEY_0_3.	0x0

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Table 907: OQSPIF_CTR_KEY_12_15_REG (0x36000120)

Bit	Mode	Symbol	Description	Reset
31:0	W	OSPIC_CTR_KEY_12_15	See the description in the OSPIC_CTR_KEY_0_3.	0x0

Table 908: OQSPIF_CTR_KEY_16_19_REG (0x36000124)

Bit	Mode	Symbol	Description	Reset
31:0	W	OSPIC_CTR_KEY_16_19	See the description in the OSPIC_CTR_KEY_0_3.	0x0

Table 909: OQSPIF_CTR_KEY_20_23_REG (0x36000128)

Bit	Mode	Symbol	Description	Reset
31:0	W	OSPIC_CTR_KEY_20_23	See the description in the OSPIC_CTR_KEY_0_3.	0x0

Table 910: OQSPIF_CTR_KEY_24_27_REG (0x3600012C)

Bit	Mode	Symbol	Description	Reset
31:0	W	OSPIC_CTR_KEY_24_27	See the description in the OSPIC_CTR_KEY_0_3.	0x0

Table 911: OQSPIF_CTR_KEY_28_31_REG (0x36000130)

Bit	Mode	Symbol	Description	Reset
31:0	W	OSPIC_CTR_KEY_28_31	See the description in the OSPIC_CTR_KEY_0_3.	0x0

44.20 eMMC Controller Registers

Table 912: Register map EMMC

Address	Register	Description
0x30058000	EMMC_SDMASA_R_REG	This register is used to configure a 32-bit Block Count or an SDMA System Address based on the Host Version 4 Enable bit in the Host Control 2 register. This register is applicable for both SD and eMMC modes.
0x30058004	EMMC_BLOCKSIZE_R_REG	This register is used to configure an SDMA buffer boundary and the number of bytes in a data block. This register is applicable for both SD and eMMC modes.
0x30058006	EMMC_BLOCKCOUNT_R_REG	This register is used to configure the number of data blocks. This register is applicable for both SD and eMMC modes.

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Address	Register	Description
0x30058008	EMMC_ARGUMENT_R_REG	This register is used to configure the SD/eMMC command argument.
0x3005800C	EMMC_XFER_MODE_R_REG	This register is used to control the operation of data transfers for an SD/eMMC mode. The Host driver sets this register before issuing a command that transfers data.
0x3005800E	EMMC_CMD_R_REG	This register is used to provide the information related to a command and a response packet. This register is applicable for an SD/eMMC mode.
0x30058010	EMMC_RESP01_R_REG	This register stores 39-08 bits of the Response Field for an SD/eMMC mode. The response for an SD/eMMC command can be a maximum of 128 bits. These 128 bits are segregated into four 32-bit registers: RESP01_R, RESP23_R, RESP45_R and RESP67_R.
0x30058014	EMMC_RESP23_R_REG	This register stores 71-40 bits of the Response Field for an SD/eMMC mode. This register is used to store the response from the cards. The response can be a maximum of 128 bits. These 128 bits are segregated into four 32-bit registers: RESP01_R, RESP23_R, RESP45_R and RESP67_R.
0x30058018	EMMC_RESP45_R_REG	This register stores 103-72 bits of the Response Field for an SD/eMMC mode. The response for SD/eMMC command can be a maximum of 128 bits. These 128 bits are segregated into four 32-bit registers: RESP01_R, RESP23_R, RESP45_R and RESP67_R.
0x3005801C	EMMC_RESP67_R_REG	This register stores 135-104 bits of the Response Field for an SD/eMMC mode. The SD/eMMC response can be a maximum of 128 bis. These 128 bits are segregated into four 32-bit registers: RESP01_R, RESP23_R, RESP45_R and RESP67_R.
0x30058020	EMMC_BUF_DATA_R_REG	This register is used to access the packet buffer. This register is applicable for an SD/eMMC/UHS-II mode.
0x30058024	EMMC_PSTATE_REG	This register indicates the present status of the Host Controller. This register is applicable for an SD/eMMC/UHS-II mode.
0x30058028	EMMC_HOST_CTRL1_R_REG	This register is used to control the operation of the Host Controller. This register is applicable for an SD/eMMC/UHS-II mode.
0x30058029	EMMC_PWR_CTRL_R_REG	This register is used to control the bus power for the Card. This register is applicable for an SD, eMMC, and UHS-II modes.
0x3005802A	EMMC_BGAP_CTRL_R_REG	This register is used by the host driver to control any operation related to Block Gap. This register is applicable for an SD/eMMC/UHS-II mode.
0x3005802B	EMMC_WUP_CTRL_R_REG	This register is mandatory for the Host Controller, but the wakeup functionality depends on the Host Controller system hardware and software. The Host Driver maintains voltage on the SD Bus by setting the SD Bus Power to 1 in the Power Control Register, while a wake-up event through the Card Interrupt is desired.
0x3005802C	EMMC_CLK_CTRL_R_REG	This register controls SDCLK (card clock) in an SD/eMMC mode and RCLK in the UHS-II mode. This register is applicable for an SD/eMMC/UHS-II mode.
0x3005802E	EMMC_TOUT_CTRL_R_REG	This register is used to set the Data Timeout Counter value for an SD/eMMC mode according to the timer clock defined by the Capabilities register, while initializig the Host Controller.
0x3005802F	EMMC_SW_RST_R_REG	This register is used to generate a reset pulse by writing 1 to each bit of this register. After completing the reset, the Host Controller clears each bit. As it takes some time to complete a

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Address	Register	Description
		software reset, the Host Driver confirms that these bits are 0. This register is applicable for an SD/eMMC/UHS-II mode. Note: See Software Reset section in the DWC_mshc Databook for additional details.
0x30058030	EMMC_NORMAL_INT_STAT_R_REG	This register reflects the status of the Normal Interrupt. This register is applicable for an SD/eMMC/UHS-II mode.
0x30058032	EMMC_ERROR_INT_STAT_R_REG	This register enables an interrupt when the Error Interrupt Status Enable is enabled and at least one of the statuses is set to 1. Writing to 1 clears the bit and writing to 0 retains the bit unchanged. Signals defined in this register can be enabled by the Error Interrupt Status Enable register, but not by the Error Interrupt Signal Enable register. More than one status can be cleared with a single register write. This register is applicable for an SD/eMMC/UHS-II mode.
0x30058034	EMMC_NORMAL_INT_STAT_EN_R_REG	This register enables the Interrupt Status for Normal Interrupt Status register (NORMAL_INT_STAT_R) when NORMAL_INT_STAT_R is set to 1. This register is applicable for an SD/eMMC/UHS-II mode.
0x30058036	EMMC_ERROR_INT_STAT_EN_R_REG	This register sets the Interrupt Status for Error Interrupt Status register (ERROR_INT_STAT_R), when ERROR_INT_STAT_EN_R is set to 1. This register is applicable for an SD/eMMC/UHS-II mode.
0x30058038	EMMC_NORMAL_INT_SIGNAL_EN_R_REG	This register is used to select the interrupt status that is indicated to the Host System as the interrupt. All these status bits share the same 1-bit interrupt line. Setting any of these bits to 1, enables interrupt generation. This register is applicable for an SD/eMMC/UHS-II mode.
0x3005803A	EMMC_ERROR_INT_SIGNAL_EN_R_REG	This register is used to select the interrupt status that is notified to the Host System as an interrupt. All these status bits share the same 1-bit interrupt line. Setting any of these bits to 1 enables interrupt generation. This register is applicable for an SD/eMMC/UHS-II mode.
0x3005803C	EMMC_AUTO_CMD_STAT_R_REG	This register is used to indicate the CMD12 response error of Auto CMD12, and the CMD23 response error of Auto CMD23. The Host driver can determine the kind of Auto CMD12/CMD23 errors that can occur in this register. Auto CMD23 errors are indicated in bit 04-01. This register is valid only when Auto CMD Error is set. This register is applicable for an SD/eMMC mode.
0x3005803E	EMMC_HOST_CTRL2_R_REG	This register is used to control how the Host Controller operates. This register is applicable for an SD/eMMC/UHS-II mode.
0x30058040	EMMC_CAPABILITIES1_R_REG	This register provides the Host Driver with information specific to the Host Controller implementation. The host controller may implement these values as fixed or loaded from the flash memory during power on initialization. Capabilities register is segregated into two 32-bit registers: CAPABILITIES1_R and CAPABILITIES2_R. The CAPABILITIES1_R register is the lower part of Capabilities register.
0x30058044	EMMC_CAPABILITIES2_R_REG	This register provides the Host Driver with information specific to the Host Controller implementation. The host controller may implement these values as fixed or as loaded from flash memory during power on initialization. Capabilities register is segregated into two 32-bit registers, namely CAPABILITIES1_R and CAPABILITIES2_R. The CAPABILITIES2_R register is upper part of Capabilities register.
0x30058048	EMMC_CURR_CAPABILITIES1_R_REG	This register indicate the maximum current capability for each voltage, for VDD1. The value is meaningful if the Voltage

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Address	Register	Description
		Support is set in the Capabilities register. If this information is supplied by the Host System through another method, all the Maximum Current Capabilities registers are set to 0.
0x3005804C	EMMC_CURR_CAPABILITIES2_R_REG	This register indicates the maximum current capability for each voltage (for VDD2). The value is meaningful if Voltage Support is set in the Capabilities register. If this information is supplied by the Host System through another method, all the Maximum Current Capabilities registers are set to 0.
0x30058050	EMMC_FORCE_AUTO_CMD_STAT_R_REG	The register is not a physically implemented but is an address at which the Auto CMD Error Status register can be written. This register is applicable for an SD/eMMC mode. 1 : Sets each bit of the Auto CMD Error Status register. 0 : No effect.
0x30058052	EMMC_FORCE_ERROR_INT_STAT_R_REG	This register is not physically implemented but is an address at which the Error Interrupt Status register can be written. The effect of a write to this address is reflected in the Error Interrupt Status register if the corresponding bit of the Error Interrupt Status Enable register is set. This register is applicable for an SD/eMMC/UHS-II mode.
0x30058054	EMMC_ADMA_ERR_STAT_R_REG	This register stores the ADMA state during an ADMA error. This register is applicable for an SD/eMMC/UHS-II mode.
0x30058058	EMMC_ADMA_SA_LOW_R_REG	This register holds the lower 32-bit system address for DMA transfer. This register is applicable for an SD/eMMC/UHS-II mode.
0x30058060	EMMC_PRESET_INIT_R_REG	This register defines Preset Value for Initialization in SD/eMMC mode.
0x30058062	EMMC_PRESET_DS_R_REG	This register defines Preset Value for Default Speed mode in SD mode.
0x30058064	EMMC_PRESET_HS_R_REG	This register defines Preset Value for High Speed mode in SD mode.
0x30058066	EMMC_PRESET_SDR12_R_REG	This register defines Preset Value for SDR12 and Legacy speed mode in SD and eMMC mode respectively.
0x30058068	EMMC_PRESET_SDR25_R_REG	This register defines Preset Value for SDR25 and High Speed SDR speed mode in SD and eMMC mode respectively.
0x3005806A	EMMC_PRESET_SDR50_R_REG	This register defines Preset Value for SDR50 speed mode in SD mode.
0x3005806C	EMMC_PRESET_SDR104_R_REG	This register defines Preset Value for SDR104 and HS200 speed modes in the SD and eMMC modes, respectively.
0x3005806E	EMMC_PRESET_DDR50_R_REG	This register defines the Preset Value for DDR50 and High Speed DDR speed modes in the SD and eMMC modes, respectively.
0x30058074	EMMC_PRESET_UHS2_R_REG	This register is used to hold the preset value for UHS-II and HS400 speed modes in the SD and eMMC modes, respectively.
0x300580E6	EMMC_P_EMBEDDED_CNTRL_REG	This register points to the location of UHS-II embedded control registers.
0x300580E8	EMMC_P_VENDOR_SPECIFIC_AREA_REG	This register used as a pointer for the Vendor Specific Area 1.
0x300580EA	EMMC_P_VNDR2_SPECIFIC_AREA_REG	This register is used as a pointer for the Vendor Specific Area 2.
0x300580FC	EMMC_SLOT_INTR_STATUS_R_REG	This register indicates the Interrupt status of each slot.

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Address	Register	Description
0x300580FE	EMMC_HOST_CNTRL_VERS_R_REG	This register is used to indicate the Host Controller Version number.
0x30058184	EMMC_CQCAP_REG	This register indicates the capabilities of the command queuing engine.
0x30058500	EMMC_VER_ID_R_REG	This register reflects the current release number of eMMC.
0x30058504	EMMC_VER_TYPE_R_REG	This register reflects the current release type of eMMC.
0x30058508	EMMC_CTRL_R_REG	This register is used to control the operation of EMMC Controller.
0x30058510	EMMC_MBIU_CTRL_R_REG	This register is used to select the valid burst types that the AHB Master bus interface can generate. When more than one bit is set the master selects the burst it prefers among those that are enabled in this register.
0x3005852C	EMMC_EMMC_CTRL_R_REG	This register is used to control the eMMC operation.
0x3005852E	EMMC_BOOT_CTRL_R_REG	This register is used to control the eMMC Boot operation.
0x30058540	EMMC_AT_CTRL_R_REG	This register controls some aspects of tuning and auto-tuning features. Do not program this register when HOST_CTRL2_R.SAMPLE_CLK_SEL is 1.
0x30058544	EMMC_AT_STAT_R_REG	Register to read the Center, Left and Right codes used by tuning and auto-tuning engines. Center code field is also used for software managed tuning.
0x30058F6C	EMMC_EMBEDDED_CTRL_R_REG	This register controls the embedded device. When the Host Controller is connected to a removable device, this register is not used.

Table 913: EMMC_SDMASA_R_REG (0x30058000)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	BLOCKCNT_SDMASA	32-bit Block Count (SDMA System Address). - SDMA System Address (Host Version 4 Enable = 0): This register contains the system memory address for an SDMA transfer in the 32-bit addressing mode. When the Host Controller stops an SDMA transfer, this register points to the system address of the next contiguous data position. It can be accessed only if no transaction is executing. Reading this register during data transfers may return an invalid value. - 32-bit Block Count (Host Version 4 Enable = 1): From the Host Controller Version 4.10 specification, this register is redefined as 32-bit Block Count. The Host Controller decrements the block count of this register for every block transfer and the data transfer stops when the count reaches zero. This register must be accessed when no transaction is executing. Reading this register during data transfers may return invalid value.	0x0

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Bit	Mode	Symbol	Description	Reset
			Following are the values for BLOCKCNT_SDMASA: - 0xFFFF_FFFF: 4G - 1 Block - ... - 0x0000_0002: 2 Blocks - 0x0000_0001: 1 Block - 0x0000_0000: Stop Count Note: - For Host Version 4 Enable = 0, the Host driver does not program the system address in this register while operating in ADMA mode. The system address must be programmed in the ADMA System Address register. - For Host Version 4 Enable = 0, the Host driver programs a non-zero 32-bit block count value in this register when Auto CMD23 is enabled for non-DMA and ADMA modes. Auto CMD23 cannot be used with SDMA. - This register must be programmed with a non-zero value for data transfer if the 32-bit Block count register is used instead of the 16-bit Block count register.	

Table 914: EMMC_BLOCKSIZE_R_REG (0x30058004)

Bit	Mode	Symbol	Description	Reset
15	R	-	Reserved	0x0
14:12	R/W	SDMA_BUF_BDARY	SDMA Buffer Boundary. These bits specify the size of contiguous buffer in system memory. The SDMA transfer waits at every boundary specified by these fields and the Host Controller generates the DMA interrupt to request the Host Driver to update the SDMA System Address register. Values: 0x0 (BYTES_4K): 4K bytes SDMA Buffer Boundary 0x1 (BYTES_8K): 8K bytes SDMA Buffer Boundary 0x2 (BYTES_16K): 16K bytes SDMA Buffer Boundary 0x3 (BYTES_32K): 32K bytes SDMA Buffer Boundary 0x4 (BYTES_64K): 64K bytes SDMA Buffer Boundary 0x5 (BYTES_128K): 128K bytes SDMA Buffer Boundary 0x6 (BYTES_256K): 256K bytes SDMA Buffer Boundary 0x7 (BYTES_512K): 512K bytes SDMA Buffer Boundary	0x0

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Bit	Mode	Symbol	Description	Reset
11:0	R/W	XFER_BLOCK_SIZE	Transfer Block Size. These bits specify the block size of data transfers. In case of memory, it is set to 512 bytes. It can be accessed only if no transaction is executing. Read operations during transfers may return an invalid value, and write operations are ignored. Following are the values for XFER_BLOCK_SIZE: - 0x1: 1 byte - 0x2: 2 bytes - 0x3: 3 bytes - ..... - 0x1FF: 511 byte - 0x200: 512 bytes - ..... - 0x800: 2048 bytes Note: This register must be programmed with a non-zero value for data transfer.	0x0

Table 915: EMMC_BLOCKCOUNT_R_REG (0x30058006)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	BLOCK_CNT	16-bit Block Count. - If the Host Version 4 Enable bit is set 0 or the 16-bit Block Count register is set to non-zero, the 16-bit Block Count register is selected. - If the Host Version 4 Enable bit is set 1 and the 16-bit Block Count register is set to zero, the 32-bit Block Count register is selected. Following are the values for BLOCK_CNT: - 0x0: Stop Count - 0x1: 1 Block - 0x2: 2 Blocks - ... - ... - 0xFFFF: 65535 Blocks Note: For Host Version 4 Enable = 0, this register must be set to 0000h before programming the 32-bit block count register when Auto CMD23 is enabled for non-DMA and ADMA modes.	0x0

Table 916: EMMC_ARGUMENT_R_REG (0x30058008)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	ARGUMENT	Command Argument. These bits specify the SD/eMMC command argument that is specified in bits 39-8 of the Command format.	0x0

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Table 917: EMMC_XFER_MODE_R_REG (0x3005800C)

Bit	Mode	Symbol	Description	Reset
15:9	R	-	Reserved	0x0
8	R/W	RESP_INT_DISABLE	Response Interrupt Disable. The Host Controller supports response check function to avoid overhead of response error check by the Host driver. Response types of only R1 and R5 can be checked by the Controller. If Host Driver checks the response error, set this bit to 0 and wait for Command Complete Interrupt and then check the response register. If the Host Controller checks the response error, set this bit to 1 and set the Response Error Check Enable bit to 1. The Command Complete Interrupt is disabled by this bit regardless of the Command Complete Signal Enable. Note: During tuning (when the Execute Tuning bit in the Host Control2 register is set), the Command Complete Interrupt is not generated irrespective of the Response Interrupt Disable setting. Values: 0x0 (ENABLED): Response Interrupt is enabled 0x1 (DISABLED): Response Interrupt is disabled	0x0
7	R/W	RESP_ERR_CHK_ENABLE	Response Error Check Enable. The Host Controller supports response check function to avoid overhead of response error check by Host driver. Response types of only R1 and R5 can be checked by the Controller. If the Host Controller checks the response error, set this bit to 1 and set Response Interrupt Disable to 1. If an error is detected, the Response Error interrupt is generated in the Error Interrupt Status register. Note: - Response error check must not be enabled for any response type other than R1 and R5. - Response check must not be enabled for the tuning command. Values: 0x0 (DISABLED): Response Error Check is disabled 0x1 (ENABLED): Response Error Check is enabled	0x0
6	R/W	RESP_TYPE	Response Type R1/R5. This bit selects either R1 or R5 as a response type when the Response Error Check is selected. Error statuses checked in R1: - OUT_OF_RANGE	0x0

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Bit	Mode	Symbol	Description	Reset
			- ADDRESS_ERROR - BLOCK_LEN_ERROR - WP_VIOLATION - CARD_IS_LOCKED - COM_CRC_ERROR - CARD_ECC_FAILED - CC_ERROR - ERROR Response Flags checked in R5: - COM_CRC_ERROR - ERROR - FUNCTION_NUMBER - OUT_OF_RANGE Values: 0x0 (RESP_R1): R1 (Memory) 0x1 (RESP_R5): R5	
5	R/W	MULTI_BLK_SEL	Multi/Single Block Select. This bit is set when issuing multiple-block transfer commands using the DAT line. If this bit is set to 0, it is not necessary to set the Block Count register. Values: 0x0 (SINGLE): Single Block 0x1 (MULTI): Multiple Block	0x0
4	R/W	DATA_XFER_DIR	Data Transfer Direction Select. This bit defines the direction of DAT line data transfers. This bit is set to 1 by the Host Driver to transfer data from the SD/eMMC card to the Host Controller and it is set to 0 for all other commands. Values: 0x1 (READ): Read (Card to Host) 0x0 (WRITE): Write (Host to Card)	0x0
3:2	R/W	AUTO_CMD_ENABLE	Auto Command Enable. This field determines use of Auto Command functions. Values: 0x0 (AUTO_CMD_DISABLED): Auto Command Disabled 0x1 (AUTO_CMD12_ENABLED): Auto CMD12 Enable 0x2 (AUTO_CMD23_ENABLED): Auto CMD23 Enable	0x0

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Bit	Mode	Symbol	Description	Reset
			0x3 (AUTO_CMD_AUTO_SEL): Auto CMD Auto Select	
1	R/W	BLOCK_COUNT_ENABLE	Block Count Enable. This bit is used to enable the Block Count register, which is relevant for multiple block transfers. If this bit is set to 0, the Block Count register is disabled, which is useful in executing an infinite transfer. The Host Driver must set this bit to 0 when ADMA is used. Values: 0x1 (ENABLED): Enable 0x0 (DISABLED): Disable	0x0
0	R/W	DMA_EN_EMMC	DMA Enable. This bit enables the DMA functionality. If this bit is set to 1, a DMA operation begins when the Host Driver writes to the Command register. You can select one of the DMA modes by using DMA Select in the Host Control 1 register. Values: 0x1 (ENABLED): DMA Data transfer 0x0 (DISABLED): No data transfer or Non-DMA data transfer	0x0

Table 918: EMMC_CMD_R_REG (0x3005800E)

Bit	Mode	Symbol	Description	Reset
15:14	R	-	Reserved	0x0
13:8	R/W	CMD_INDEX	Command Index. These bits are set to the command number that is specified in bits 45-40 of the Command Format.	0x0
7:6	R/W	CMD_TYPE	Command Type. These bits indicate the command type. Note: While issuing Abort CMD using CMD12/CMD52 or reset CMD using CMD0/CMD52, CMD_TYPE field shall be set to 0x3. Values: 0x3 (ABORT_CMD): Abort 0x2 (RESUME_CMD): Resume 0x1 (SUSPEND_CMD): Suspend 0x0 (NORMAL_CMD): Normal	0x0

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Bit	Mode	Symbol	Description	Reset
5	R/W	DATA_PRESENT_SEL	Data Present Select. This bit is set to 1 to indicate that data is present and that the data is transferred using the DAT line. This bit is set to 0 in the following instances: - Command using the CMD line - Command with no data transfer but using busy signal on the DAT[0] line - Resume Command Values: 0x0 (NO_DATA): No Data Present 0x1 (DATA): Data Present	0x0
4	R/W	CMD_IDX_CHK_ENABLE	Command Index Check Enable. This bit enables the Host Controller to check the index field in the response to verify if it has the same value as the command index. If the value is not the same, it is reported as a Command Index error. Note: - Index Check enable must be set to 0 for the command with no response, R2 response, R3 response and R4 response. - For the tuning command, this bit must always be set to enable the index check. Values: 0x0 (DISABLED): Disable 0x1 (ENABLED): Enable	0x0
3	R/W	CMD_CRC_CHK_ENABLE	Command CRC Check Enable. This bit enables the Host Controller to check the CRC field in the response. If an error is detected, it is reported as a Command CRC error. Note: - CRC Check enable must be set to 0 for the command with no response, R3 response, and R4 response. - For the tuning command, this bit must always be set to 1 to enable the CRC check. Values: 0x0 (DISABLED): Disable 0x1 (ENABLED): Enable	0x0
2	R/W	SUB_CMD_FLAG	Sub Command Flag. This bit distinguishes between a main command and a sub command. Values: 0x0 (MAIN): Main Command	0x0

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Bit	Mode	Symbol	Description	Reset
			0x1 (SUB): Sub Command	
1:0	R/W	RESP_TYPE_SELECT	Response Type Select. This bit indicates the type of response expected from the card. Values: 0x0 (NO_RESP): No Response 0x1 (RESP_LEN_136): Response Length 136 0x2 (RESP_LEN_48): Response Length 48 0x3 (RESP_LEN_48B): Response Length 48; Check Busy after response	0x0

Table 919: EMMC_RESP01_R_REG (0x30058010)

Bit	Mode	Symbol	Description	Reset
31:0	R	RESP01	Command Response. These bits reflect 39-8 bits of SD/eMMC Response Field. Note: For Auto CMD, the 32-bit response (bits 39-8 of the Response Field) is updated in the RESP67_R register.	0x0

Table 920: EMMC_RESP23_R_REG (0x30058014)

Bit	Mode	Symbol	Description	Reset
31:0	R	RESP23	Command Response. These bits reflect 71-40 bits of the SD/eMMC Response Field.	0x0

Table 921: EMMC_RESP45_R_REG (0x30058018)

Bit	Mode	Symbol	Description	Reset
31:0	R	RESP45	Command Response. These bits reflect 103-72 bits of the Response Field.	0x0

Table 922: EMMC_RESP67_R_REG (0x3005801C)

Bit	Mode	Symbol	Description	Reset
31:0	R	RESP67	Command Response. These bits reflect bits 135-104 of SD/EMMC Response Field.	0x0

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Bit	Mode	Symbol	Description	Reset
			Note: For Auto CMD, this register also reflects the 32-bit response (bits 39-8 of the Response Field).	

Table 923: EMMC_BUF_DATA_R_REG (0x30058020)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	BUF_DATA	Buffer Data. These bits enable access to the Host Controller packet buffer.	0x0

Table 924: EMMC_PSTATE_REG (0x30058024)

Bit	Mode	Symbol	Description	Reset
31	R	UHS2_IF_DETECT	UHS-II Interface Detection. For SD/eMMC mode, this bit always returns 0. Values: 0x0 (FALSE): UHS-II interface is not detected 0x1 (TRUE): UHS-II interface is detected	0x0
30	R	LANE_SYNC	Lane Synchronization. For SD/eMMC mode, this bit always returns 0. Values: 0x0 (FALSE): UHS-II PHY is not initialized 0x1 (TRUE): UHS-II PHY is initialized	0x0
29	R	IN_DORMANT_ST	In Dormant Status For SD/eMMC mode, this bit always returns 0. Values: 0x0 (FALSE): Not in DORMANT state 0x1 (TRUE): In DORMANT state	0x0
28	R	SUB_CMD_STAT	Sub Command Status. This bit is used to distinguish between a main command and a sub command status. Values: 0x0 (FALSE): Main Command Status 0x1 (TRUE): Sub Command Status	0x0
27	R	CMD_ISSUE_ERR	Command Not Issued by Error. This bit is set if a command cannot be issued after setting the command register due to an error except the Auto CMD12 error.	0x0

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Bit	Mode	Symbol	Description	Reset
			Values: 0x0 (FALSE): No error for issuing a command 0x1 (TRUE): Command cannot be issued	
26	R	-	Reserved	0x0
25	R	HOST_REG_VOL	Host Regulator Voltage Stable. This bit is used to check whether the host regulator voltage is stable for switching the voltage of UHS-I mode. This bit reflects the synchronized value of the host_reg_vol_stable signal. Values: Description 0x0 (FALSE): Host Regulator Voltage is not stable 0x1 (TRUE): Host Regulator Voltage is stable	0x1
24	R	CMD_LINE_LVL	Command-Line Signal Level. This bit is used to check the CMD line level to recover from errors and for debugging. These bits reflect the value of the sd_cmd_in signal.	0x0
23:20	R	DAT_3_0	DAT[3:0] Line Signal Level. This bit is used to check the DAT line level to recover from errors and for debugging. These bits reflect the value of the sd_dat_in (lower nibble) signal.	0x0
19	R	WR_PROTECT_SW_LVL	Write Protect Switch Pin Level. This bit is supported only for memory and combo cards. This bit reflects the synchronized value of the card_write_prot signal. Values: 0x0 (FALSE): Write protected 0x1 (TRUE): Write enabled	0x1
18	R	CARD_DETECT_PIN_LEVEL	Card Detect Pin Level. This bit reflects the inverse synchronized value of the card_detect_n signal. Values: 0x0 (FALSE): No card present 0x1 (TRUE): Card Present	0x1
17	R	CARD_STABLE	Card Stable. This bit indicates the stability of the Card Detect Pin Level. A card is not detected if this bit is set to 1 and the value of the CARD_INSERTED bit is 0. Values: 0x0 (FALSE): Reset or Debouncing 0x1 (TRUE): No Card or Inserted	0x0
16	R	CARD_INSERTED	Card Inserted.	0x0

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Bit	Mode	Symbol	Description	Reset
			This bit indicates whether a card has been inserted. The Host Controller debounces this signal so that Host Driver need not wait for it to stabilize. Values: 0x0 (FALSE): Reset, Debouncing, or No card 0x1 (TRUE): Card Inserted	
15:12	R	-	Reserved	0x0
11	R	BUF_RD_ENABLE	Buffer Read Enable. This bit is used for non-DMA transfers. This bit is set if valid data exists in the Host buffer. Values: 0x0 (DISABLED): Read disable 0x1 (ENABLED): Read enable	0x0
10	R	BUF_WR_ENABLE	Buffer Write Enable. This bit is used for non-DMA transfers. This bit is set if space is available for writing data. Values: 0x0 (DISABLED): Write disable 0x1 (ENABLED): Write enable	0x0
9	R	RD_XFER_ACTIVE	Read Transfer Active. This bit indicates whether a read transfer is active for SD/eMMC mode. Values: 0x0 (INACTIVE): No valid data 0x1 (ACTIVE): Transferring data	0x0
8	R	WR_XFER_ACTIVE	Write Transfer Active. This status indicates whether a write transfer is active for SD/eMMC mode. Values: 0x0 (INACTIVE): No valid data 0x1 (ACTIVE): Transferring data	0x0
7:4	R	DAT_7_4	DAT[7:4] Line Signal Level. This bit is used to check the DAT line level to recover from errors and for debugging. These bits reflect the value of the sd_dat_in (upper nibble) signal.	0x0
3	R	RE_TUNE_REQ	Re-Tuning Request. emmc does not generate retuning request. The software must maintain the Retuning timer.	0x0
2	R	DAT_LINE_ACTIVE	DAT Line Active (SD/eMMC Mode only). This bit indicates whether one of the DAT lines on the SD/eMMC bus is in use.	0x0

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Bit	Mode	Symbol	Description	Reset
			In the case of read transactions, this bit indicates whether a read transfer is executing on the SD/eMMC bus. In the case of write transactions, this bit indicates whether a write transfer is executing on the SD/eMMC bus. For a command with busy, this status indicates whether the command executing busy is executing on an SD or eMMC bus. Values: 0x0 (INACTIVE): DAT Line Inactive 0x1 (ACTIVE): DAT Line Active	
1	R	CMD_INHIBIT_DAT	Command Inhibit (DAT). This bit is applicable for SD/eMMC mode and is generated if either DAT line active or Read transfer active is set to 1. If this bit is set to 0, it indicates that the Host Controller can issue subsequent SD/eMMC commands. Values: 0x0 (READY): Can issue command which used DAT line 0x1 (NOT_READY): Cannot issue command which used DAT line	0x0
0	R	CMD_INHIBIT	Command Inhibit (CMD). This bit indicates the following : - SD/eMMC mode: If this bit is set to 0, it indicates that the CMD line is not in use and the Host controller can issue an SD/eMMC command using the CMD line. This bit is set when the command register is written. This bit is cleared when the command response is received. This bit is not cleared by the response of auto CMD12/23 but cleared by the response of read/write command. Values: 0x0 (READY): Host Controller is ready to issue a command 0x1 (NOT_READY): Host Controller is not ready to issue a command	0x0

Table 925: EMMC_HOST_CTRL1_R_REG (0x30058028)

Bit	Mode	Symbol	Description	Reset
7	R/W	CARD_DETECT_SIG_SEL	Card Detect Signal Selection. This bit selects a source for card detection. When the source for the card detection is switched, the interrupt must be disabled during the switching period.	0x0

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Bit	Mode	Symbol	Description	Reset
			Values: 0x1 (CARD_DT_TEST_LEVEL): Card Detect Test Level is selected (for test purpose) 0x0 (SDCD_PIN): SDCD# (card_detect_n signal) is selected (for normal use)	
6	R/W	CARD_DETECT_TEST_LVL	Card Detect Test Level. This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates whether a card inserted or not. Values: 0x1 (CARD_INSERTED): Card Inserted 0x0 (No_CARD): No Card	0x0
5	R/W	EXT_DAT_XFER	Extended Data Transfer Width. This bit controls 8-bit bus width mode of embedded device. Values: 0x1 (EIGHT_BIT): 8-bit Bus Width 0x0 (DEFAULT): Bus Width is selected by the Data Transfer Width	0x0
4:3	R/W	DMA_SEL	DMA Select. This field is used to select the DMA type. When Host Version 4 Enable is 1 in Host Control 2 register: - 0x0 : SDMA is selected - 0x1 : Reserved - 0x2 : ADMA2 is selected - 0x3 : ADMA2 or ADMA3 is selected When Host Version 4 Enable is 0 in Host Control 2 register: - 0x0 : SDMA is selected - 0x1 : Reserved - 0x2 : 32-bit Address ADMA2 is selected - 0x3 : 64-bit Address ADMA2 is selected Values: 0x0 (SDMA): SDMA is selected 0x1 (RSVD_BIT): Reserved 0x2 (ADMA2): ADMA2 is selected 0x3 (ADMA2_3): ADMA2 or ADMA3 is selected	0x0
2	R/W	HIGH_SPEED_EN	High Speed Enable (SD/eMMC Mode only). In SD/eMMC mode, this bit is used to determine the selection of preset value for High Speed mode. Before setting this bit, the Host Driver checks the High Speed Support in the Capabilities register. Note:emmc always outputs the sd_cmd_out and sd_dat_out lines at the rising edge of cclk_tx clock irrespective of this bit.Please refer the section Connecting the Clock IO interface in the Mobile	0x0

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Bit	Mode	Symbol	Description	Reset
			Storage Host Controller user guide on clocking requirement for an SD/eMMC card. Values: 0x1 (HIGH_SPEED): High Speed mode 0x0 (NORMAL_SPEED): Normal Speed mode	
1	R/W	DAT_XFER_WIDTH	Data Transfer Width. For SD/eMMC mode,this bit selects the data transfer width of the Host Controller. The Host Driver sets it to match the data width of the SD/eMMC card. Values: 0x1 (FOUR_BIT): 4-bit mode 0x0 (ONE_BIT): 1-bit mode	0x0
0	R/W	LED_CTRL	LED Control. This bit is used to caution the user not to remove the card while the SD card is being accessed. The value is reflected on the led_control signal. Values: 0x0 (OFF): LED off 0x1 (ON): LED on	0x0

Table 926: EMMC_PWR_CTRL_R_REG (0x30058029)

Bit	Mode	Symbol	Description	Reset
7:5	R/W	SD_BUS_VOL_VDD2	SD Bus Voltage Select for VDD2. This is irrelevant for SD/eMMC card. Values: 0x7 (NOT_USED7): Not used 0x6 (NOT_USED6): Not used 0x5 (V_1_8): 1.8 V 0x4 (V_1_2): Reserved for 1.2 V 0x3 (RSVD3): Reserved 0x2 (RSVD2): Reserved 0x1 (RSVD1): Reserved 0x0 (NO_VDD2): VDD2 Not Supported	0x0
4	R/W	SD_BUS_PWR_VDD2	SD Bus Power for VDD2. This is irrelevant for SD/eMMC card. Values: 0x0 (OFF): Power off 0x1 (ON): Power on	0x0
3:1	R/W	SD_BUS_VOL_VDD1	SD Bus Voltage Select for VDD1/eMMC Bus Voltage Select for VDD. These bits enable the Host Driver to select the voltage level for an SD/eMMC card. Before setting	0x0

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Bit	Mode	Symbol	Description	Reset
			this register, the Host Driver checks the Voltage Support bits in the Capabilities register. If an unsupported voltage is selected, the Host System does not supply the SD Bus voltage. The value set in this field is available on the emmc output signal (sd_vdd1_sel), which is used by the voltage switching circuitry. SD Bus Voltage Select options: - 0x7 : 3.3 V(Typical) - 0x6 : 3.0 V(Typical) - 0x5 : 1.8 V(Typical) for Embedded - 0x4 : 0x0 - Reserved eMMC Bus Voltage Select options: - 0x7 : 3.3 V(Typical) - 0x6 : 1.8 V(Typical) - 0x5 : 1.2 V(Typical) - 0x4 : 0x0 - Reserved Values: 0x7 (V_3_3): 3.3 V (Typ.) 0x6 (V_3_0): 3.0 V (Typ.) 0x5 (V_1_8): 1.8 V (Typ.) for Embedded 0x4 (RSVD4): Reserved 0x3 (RSVD3): Reserved 0x2 (RSVD2): Reserved 0x1 (RSVD1): Reserved 0x0 (RSVD0): Reserved	
0	R/W	SD_BUS_PWR_VDD1	SD Bus Power for VDD1. This bit enables VDD1 power of the card. This setting is available on the sd_vdd1_on output of emmc so that it can be used to control the VDD1 power supply of the card. Before setting this bit, the SD Host Driver sets the SD Bus Voltage Select bit. If the Host Controller detects a No Card state, this bit is cleared. In SD mode, if this bit is cleared, the Host Controller stops the SD Clock by clearing the SD_CLK_IN bit in the CLK_CTRL_R register. Values: 0x0 (OFF): Power off 0x1 (ON): Power on	0x0

Table 927: EMMC_BGAP_CTRL_R_REG (0x3005802A)

Bit	Mode	Symbol	Description	Reset
7:4	R	-	Reserved	0x0
3	R/W	-	Reserved	0x0
2	R/W	RD_WAIT_CTRL	Read Wait Control.	0x0

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Bit	Mode	Symbol	Description	Reset
			This bit is used to enable the read wait protocol to stop read data using DAT[2] line if the card supports read wait. Otherwise, the Host Controller has to stop the card clock to hold the read data. Values: 0x0 (DISABLE): Disable Read Wait Control 0x1 (ENABLE): Enable Read Wait Control	
1	R/W	CONTINUE_REQ	Continue Request. This bit is used to restart the transaction, which was stopped using the Stop At Block Gap Request. The Host Controller automatically clears this bit when the transaction restarts. If stop at block gap request is set to 1, any write to this bit is ignored. Values: 0x0 (NO_AFFECT): No Affect 0x1 (RESTART): Restart	0x0
0	R/W	STOP_BG_REQ	Stop At Block Gap Request. This bit is used to stop executing read and write transactions at the next block gap for non-DMA, SDMA, and ADMA transfers. Values: 0x0 (XFER): Transfer 0x1 (STOP): Stop	0x0

Table 928: EMMC_WUP_CTRL_R_REG (0x3005802B)

Bit	Mode	Symbol	Description	Reset
7:3	R	-	Reserved	0x0
2	R/W	CARD_REMOVAL	Wakeup Event Enable on SD Card Removal. This bit enables wake-up event through Card Removal assertion in the Normal Interrupt Status register. Values: 0x0 (DISABLED): Disable 0x1 (ENABLED): Enable	0x0
1	R/W	CARD_INSERT	Wakeup Event Enable on SD Card Insertion. This bit enables wake-up event through Card Insertion assertion in the Normal Interrupt Status register. FN_WUS (Wake Up Support) in CIS does not affect this bit. Values: 0x0 (DISABLED): Disable 0x1 (ENABLED): Enable	0x0
0	R/W	CARD_INT	Wakeup Event Enable on Card Interrupt.	0x0

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Bit	Mode	Symbol	Description	Reset
			This bit enables wake-up event through a Card Interrupt assertion in the Normal Interrupt Status register. This bit can be set to 1 if FN_WUS (Wake Up Support) in CIS is set to 1. Values: 0x0 (DISABLED): Disable 0x1 (ENABLED): Enable	

Table 929: EMMC_CLK_CTRL_R_REG (0x3005802C)

Bit	Mode	Symbol	Description	Reset
15:8	R/W	FREQ_SEL	SDCLK/RCLK Frequency Select. These bits are used to select the frequency of the SDCLK signal. These bits depend on setting of Preset Value Enable in the Host Control 2 register. If Preset Value Enable = 0, these bits are set by the Host Driver. If Preset Value Enable = 1, these bits are automatically set to a value specified in one of the Preset Value register. The value is reflected on the lower 8-bit of the card_clk_freq_sel signal. 10-bit Divided Clock Mode: - 0x3FF : 1/2046 Divided clock - N : 1/2N Divided Clock - 0x002 : 1/4 Divided Clock - 0x001 : 1/2 Divided Clock - 0x000 : Base clock (10 MHz - 255 MHz) Programmable Clock Mode : Enables the Host System to select a fine grain SD clock frequency: - 0x3FF : Base clock * M /1024 - N-1 : Base clock * M /N - 0x002 : Base clock * M /3 - 0x001 : Base clock * M /2 - 0x000 : Base clock * M	0x0
7:6	R/W	UPPER_FREQ_SEL	These bits specify the upper 2 bits of 10-bit SDCLK/RCLK Frequency Select control. The value is reflected on the upper 2 bits of the card_clk_freq_sel signal.	0x0
5	R/W	CLK_GEN_SELECT	Clock Generator Select. This bit is used to select the clock generator mode in SDCLK/RCLK Frequency Select. If Preset Value Enable = 0, this bit is set by the Host Driver. If Preset Value Enable = 1, this bit is automatically set to a value specified in one of the Preset Value registers. The value is reflected on the card_clk_gen_sel signal. Values: 0x0 (FALSE): Divided Clock Mode 0x1 (TRUE): Programmable Clock Mode	0x0
4	R	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
3	R/W	PLL_ENABLE	PLL Enable. This bit is used to activate the PLL (applicable when Host Version 4 Enable = 1). When Host Version 4 Enable = 0, INTERNAL_CLK_EN bit may be used to activate PLL. The value is reflected on the card_clk_en signal. Note: If this bit is not used to to active the PLL when Host Version 4 Enable = 1, it is recommended to set this bit to 1 . Values: 0x0 (FALSE): PLL is in low power mode 0x1 (TRUE): PLL is enabled	0x0
2	R/W	SD_CLK_EN	SD/eMMC Clock Enable. This bit stops the SDCLK or RCLK when set to 0. The SDCLK/RCLK Frequency Select bit can be changed when this bit is set to 0. The value is reflected on the clk2card_on pin. Values: 0x0 (FALSE): Disable providing SDCLK/RCLK 0x1 (TRUE): Enable providing SDCLK/RCLK	0x0
1	R	INTERNAL_CLK_STABLE	Internal Clock Stable This bit enables the Host Driver to check the clock stability twice after the Internal Clock Enable bit is set and after the PLL Enable bit is set. This bit reflects the synchronized value of the intclk_stable signal after the Internal Clock Enable bit is set to 1 and also reflects the synchronized value of the card_clk_stable signal after the PLL Enable bit is set to 1. Values: 0x0 (FALSE): Not Ready 0x1 (TRUE): Ready	0x0
0	R/W	INTERNAL_CLK_EN	Internal Clock Enable. This bit is set to 0 when the Host Driver is not using the Host Controller or the Host Controller awaits a wake-up interrupt. The Host Controller must stop its internal clock to enter a very low power state. However, registers can still be read and written to. The value is reflected on the intclk_en signal. Note: If this bit is not used to control the internal clock (base clock and master clock), it is recommended to set this bit to 1. Values: 0x0 (FALSE): Stop 0x1 (TRUE): Oscillate	0x0

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Table 930: EMMC_TOUT_CTRL_R_REG (0x3005802E)

Bit	Mode	Symbol	Description	Reset
7:4	R	-	Reserved	0x0
3:0	R/W	TOUT_CNT	Data Timeout Counter Value. This value determines the interval by which DAT line timeouts are detected. The Timeout clock frequency is generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Data Timeout Error Status Enable (in the Error Interrupt Status Enable register). The values for these bits are: - 0xF : Reserved - 0xE : TMCLK x 2^27 - 0x1 : TMCLK x 2^14 - 0x0 : TMCLK x 2^13 Note: During a boot operating in an eMMC mode, an application must configure the boot data timeout value (approximately 1 sec) in this bit.	0x0

Table 931: EMMC_SW_RST_R_REG (0x3005802F)

Bit	Mode	Symbol	Description	Reset
7:3	R	-	Reserved	0x0
2	R/W	SW_RST_DAT	Software Reset For DAT line. This bit is used in SD/eMMC mode and it resets only a part of the data circuit and the DMA circuit is also reset. The following registers and bits are cleared by this bit: - Buffer Data Port register -- Buffer is cleared and initialized. - Present state register -- Buffer Read Enable -- Buffer Write Enable -- Read Transfer Active -- Write Transfer Active -- DAT Line Active -- Command Inhibit (DAT) - Block Gap Control register -- Continue Request -- Stop At Block Gap Request - Normal Interrupt status register -- Buffer Read Ready -- Buffer Write Ready -- DMA Interrupt -- Block Gap Event -- Transfer Complete Values:	0x0

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Bit	Mode	Symbol	Description	Reset
			0x0 (FALSE): Work 0x1 (TRUE): Reset	
1	R/W	SW_RST_CMD	Software Reset For CMD line. This bit resets only a part of the command circuit to be able to issue a command. This reset is effective only for a command issuing circuit (including response error statuses related to Command Inhibit (CMD) control) and does not affect the data transfer circuit. Host Controller can continue data transfer even after this reset is executed while handling subcommand-response errors. The following registers and bits are cleared by this bit: - Present State register : Command Inhibit (CMD) bit - Normal Interrupt Status register : Command Complete bit - Error Interrupt Status : Response error statuses related to Command Inhibit (CMD) bit Values: 0x0 (FALSE): Work 0x1 (TRUE): Reset	0x0
0	R/W	SW_RST_ALL	Software Reset For All. This reset affects the entire Host Controller except for the card detection circuit. During its initialization, the Host Driver sets this bit to 1 to reset the Host Controller. All registers are reset except the capabilities register. If this bit is set to 1, the Host Driver must issue reset command and reinitialize the card. Values: 0x0 (FALSE): Work 0x1 (TRUE): Reset	0x0

Table 932: EMMC_NORMAL_INT_STAT_R_REG (0x30058030)

Bit	Mode	Symbol	Description	Reset
15	R	ERR_INTERRUPT	Error Interrupt. If any of the bits in the Error Interrupt Status register are set, then this bit is set. Values: 0x0 (FALSE): No Error 0x1 (TRUE): Error	0x0
14	RW1C	CQE_EVENT	Command Queuing Event This status is set if Command Queuing/Crypto related event has occurred in eMMC/SD mode. Read CQHCI's CQIS/CRNQIS register for more details.	0x0

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Bit	Mode	Symbol	Description	Reset
			Values: 0x0 (FALSE): No Event 0x1 (TRUE): Command Queuing Event is detected	
13	R	FX_EVENT	FX Event. This status is set when R[14] of response register is set to 1 and Response Type R1/R5 is set to 0 in Transfer Mode register. This interrupt is used with response check function. Values: 0x0 (FALSE): No Event 0x1 (TRUE): FX Event is detected	0x0
12	R	RE_TUNE_EVENT	Re-tuning Event. This bit is set if the Re-Tuning Request changes from 0 to 1. Re-Tuning request is not supported.	0x0
11	R	INT_C	INT_C (Embedded). This bit is set if INT_C is enabled and if INT_C# pin is in low level. The INT_C# pin is not supported.	0x0
10	R	INT_B	INT_B (Embedded). This bit is set if INT_B is enabled and if INT_B# pin is in low level. The INT_B# pin is not supported.	0x0
9	R	INT_A	INT_A (Embedded). This bit is set if INT_A is enabled and if INT_A# pin is in low level. The INT_A# pin is not supported.	0x0
8	R	CARD_INTERRUPT	Card Interrupt. This bit reflects the synchronized value of: - DAT[1] Interrupt Input for SD Mode - DAT[2] Interrupt Input for UHS-II Mode Values: 0x0 (FALSE): No Card Interrupt 0x1 (TRUE): Generate Card Interrupt	0x0
7	RW1C	CARD_REMOVAL_STAT_R	Card Removal. This bit is set if the Card Inserted in the Present State register changes from 1 to 0. Values: 0x0 (FALSE): Card state stable or Debouncing 0x1 (TRUE): Card Removed	0x0
6	RW1C	CARD_INSERTION	Card Insertion This bit is set if the Card Inserted in the Present State register changes from 0 to 1. Values: 0x0 (FALSE): Card state stable or Debouncing	0x0

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Bit	Mode	Symbol	Description	Reset
			0x1 (TRUE): Card Inserted	
5	RW1C	BUF_RD_READY	Buffer Read Ready. This bit is set if the Buffer Read Enable changes from 0 to 1. Values: 0x0 (FALSE): Not ready to read buffer 0x1 (TRUE): Ready to read buffer	0x0
4	RW1C	BUF_WR_READY	Buffer Write Ready. This bit is set if the Buffer Write Enable changes from 0 to 1. Values: 0x0 (FALSE): Not ready to write buffer 0x1 (TRUE): Ready to write buffer	0x0
3	RW1C	DMA_INTERRUPT	DMA Interrupt. This bit is set if the Host Controller detects the SDMA Buffer Boundary during transfer. In case of ADMA, by setting the Int field in the descriptor table, the Host controller generates this interrupt. This interrupt is not generated after a Transfer Complete. Values: 0x0 (FALSE): No DMA Interrupt 0x1 (TRUE): DMA Interrupt is generated	0x0
2	RW1C	BGAP_EVENT	Block Gap Event. This bit is set when both read/write transaction is stopped at block gap due to a Stop at Block Gap Request. Values: 0x0 (FALSE): No Block Gap Event 0x1 (TRUE): Transaction stopped at block gap	0x0
1	RW1C	XFER_COMPLETE	Transfer Complete. This bit is set when a read/write transfer and a command with status busy is completed. Values: 0x0 (FALSE): Not complete 0x1 (TRUE): Command execution is completed	0x0
0	RW1C	CMD_COMPLETE	Command Complete. In an SD/eMMC Mode, this bit is set when the end bit of a response except for Auto CMD12 and Auto CMD23. This interrupt is not generated when the Response Interrupt Disable in Transfer Mode Register is set to 1. Values: 0x0 (FALSE): No command complete	0x0

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Bit	Mode	Symbol	Description	Reset
			0x1 (TRUE): Command Complete	

Table 933: EMMC_ERROR_INT_STAT_R_REG (0x30058032)

Bit	Mode	Symbol	Description	Reset
15	R	-	Reserved	0x0
14	R	-	Reserved	0x0
13	R	-	Reserved	0x0
12	RW1C	BOOT_ACK_ERR	Boot Acknowledgement Error. This bit is set when there is a timeout for boot acknowledgement or when detecting boot ack status having a value other than 010. This is applicable only when boot acknowledgement is expected in eMMC mode. Values: 0x0 (FALSE): No error 0x1 (TRUE): Error	0x0
11	RW1C	RESP_ERR	Response Error. Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If Response Error Check Enable is set to 1 in the Transfer Mode register, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1.This is applicable in SD/eMMC mode. Values: 0x0 (FALSE): No error 0x1 (TRUE): Error	0x0
10	RW1C	TUNING_ERR	Tuning Error. This bit is set when an unrecoverable error is detected in a tuning circuit except during the tuning procedure (occurrence of an error during tuning procedure is indicated by Sampling Clock Select in the Host Control 2 register). By detecting Tuning Error, Host Driver needs to abort a command executing and perform tuning. To reset tuning circuit, Sampling Clock Select is set to 0 before executing tuning procedure. The Tuning Error is higher priority than the other error interrupts generated during data transfer. By detecting Tuning Error, the Host Driver must discard data transferred by a current read/write command and retry data transfer after the Host Controller retrieved from the tuning circuit error. This is applicable in SD/eMMC mode. Values: 0x0 (FALSE): No error 0x1 (TRUE): Error	0x0

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Bit	Mode	Symbol	Description	Reset
9	RW1C	ADMA_ERR	ADMA Error. This bit is set when the Host Controller detects error during ADMA-based data transfer. The error could be due to following reasons: - Error response received from System bus (Master I/F) - ADMA3,ADMA2 Descriptors invalid - CQE Task or Transfer descriptors invalid When the error occurs, the state of the ADMA is saved in the ADMA Error Status register. In eMMC CQE mode: The Host Controller generates this Interrupt when it detects an invalid descriptor data (Valid=0) at the ST_FDS state. ADMA Error State in the ADMA Error Status indicates that an error has occurred in ST_FDS state. The Host Driver may find that Valid bit is not set at the error descriptor. Values: 0x0 (FALSE): No error 0x1 (TRUE): Error	0x0
8	RW1C	AUTO_CMD_ERR	Auto CMD Error. This error status is used by Auto CMD12 and Auto CMD23 in SD/eMMC mode. This bit is set when detecting that any of the bits D00 to D05 in Auto CMD Error Status register has changed from 0 to 1. D07 is effective in case of Auto CMD12. Auto CMD Error Status register is valid while this bit is set to 1 and may be cleared by clearing of this bit. Values: 0x0 (FALSE): No error 0x1 (TRUE): Error	0x0
7	RW1C	CUR_LMT_ERR	Current Limit Error. By setting the SD Bus Power bit in the Power Control register, the Host Controller is requested to supply power for the SD Bus. If the Host Controller supports the Current Limit function, it can be protected from an illegal card by stopping power supply to the card in which case this bit indicates a failure status. A reading of 1 for this bit means that the Host Controller is not supplying power to the SD card due to some failure. A reading of 0 for this bit means that the Host Controller is supplying power and no error has occurred. The Host Controller may require some sampling time to detect the current limit.emmc Host Controller does not support this function, this bit is always set to 0. Values: 0x0 (FALSE): No error 0x1 (TRUE): Power Fail	0x0

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Bit	Mode	Symbol	Description	Reset
6	RW1C	DATA_END_BIT_ERR	Data End Bit Error. This error occurs in SD/eMMC mode either when detecting 0 at the end bit position of read data that uses the DAT line or at the end bit position of the CRC status. Values: 0x0 (FALSE): No error 0x1 (TRUE): Error	0x0
5	RW1C	DATA_CRC_ERR	Data CRC Error. This error occurs in SD/eMMC mode when detecting CRC error when transferring read data which uses the DAT line, when detecting the Write CRC status having a value of other than 010 or when write CRC status timeout. Values: 0x0 (FALSE): No error 0x1 (TRUE): Error	0x0
4	RW1C	DATA_TOUT_ERR	Data Timeout Error. This bit is set in SD/eMMC mode when detecting one of the following timeout conditions: - Busy timeout for R1b, R5b type - Busy timeout after Write CRC status - Write CRC Status timeout - Read Data timeout Values: 0x0 (FALSE): No error 0x1 (TRUE): Time out	0x0
3	RW1C	CMD_IDX_ERR	Command Index Error. This bit is set if a Command Index error occurs in the command respons in SD/eMMC mode. Values: 0x0 (FALSE): No error 0x1 (TRUE): Error	0x0
2	RW1C	CMD_END_BIT_ERR	Command End Bit Error. This bit is set when detecting that the end bit of a command response is 0 in SD/eMMC mode. Values: 0x0 (FALSE): No error 0x1 (TRUE): End Bit error generated	0x0
1	RW1C	CMD_CRC_ERR	Command CRC Error. Command CRC Error is generated in SD/eMMC mode for following two cases. - If a response is returned and the Command Timeout Error is set to 0 (indicating no timeout), this bit is set to 1 when detecting a CRC error in the command response.	0x0

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Bit	Mode	Symbol	Description	Reset
			- The Host Controller detects a CMD line conflict by monitoring the CMD line when a command is issued. If the Host Controller drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SD clock edge, then the Host Controller aborts the command (stop driving CMD line) and set this bit to 1. The Command Timeout Error is also set to 1 to distinguish a CMD line conflict. Values: 0x0 (FALSE): No error 0x1 (TRUE): CRC error generated	
0	RW1C	CMD_TOUT_ERR	Command Timeout Error. In SD/eMMC Mode,this bit is set only if no response is returned within 64 SD clock cycles from the end bit of the command. If the Host Controller detects a CMD line conflict, along with Command CRC Error bit, this bit is set to 1, without waiting for 64 SD/eMMC card clock cycles. Values: 0x0 (FALSE): No error 0x1 (TRUE): Time out	0x0

Table 934: EMMC_NORMAL_INT_STAT_EN_R_REG (0x30058034)

Bit	Mode	Symbol	Description	Reset
15	R	-	Reserved	0x0
14	R/W	CQE_EVENT_STAT_EN	CQE Event Status Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
13	R/W	FX_EVENT_STAT_EN	FX Event Status Enable This bit is added from Version 4.10. Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
12	R/W	RE_TUNE_EVENT_STAT_EN	Re-Tuning Event (UHS-I only) Status Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
11	R/W	INT_C_STAT_EN	INT_C (Embedded) Status Enable If this bit is set to 0, the Host Controller clears the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_C and may set this bit again after all interrupt requests to	0x0

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Bit	Mode	Symbol	Description	Reset
			INT_C pin are cleared to prevent inadvertent interrupts. Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	
10	R/W	INT_B_STAT_EN	INT_B (Embedded) Status Enable If this bit is set to 0, the Host Controller clears the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_B and may set this bit again after all interrupt requests to INT_B pin are cleared to prevent inadvertent interrupts. Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
9	R/W	INT_A_STAT_EN	INT_A (Embedded) Status Enable If this bit is set to 0, the Host Controller clears the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_A and may set this bit again after all interrupt requests to INT_A pin are cleared to prevent inadvertent interrupts. Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
8	R/W	CARD_INTERRUPT_STAT_EN	Card Interrupt Status Enable If this bit is set to 0, the Host Controller clears the interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1. The Host Driver may clear the Card Interrupt Status Enable before servicing the Card Interrupt and may set this bit again after all interrupt requests from the card are cleared to prevent inadvertent interrupts. By setting this bit to 0, interrupt input must be masked by implementation so that the interrupt input is not affected by external signal in any state (for example, floating). Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
7	R/W	CARD_REMOVAL_STAT_EN	Card Removal Status Enable Values: 0x0 (FALSE): Masked	0x0

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Bit	Mode	Symbol	Description	Reset
			0x1 (TRUE): Enabled	
6	R/W	CARD_INSERTION_STAT_EN	Card Insertion Status Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
5	R/W	BUF_RD_READY_STAT_EN	Buffer Read Ready Status Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
4	R/W	BUF_WR_READY_STAT_EN	Buffer Write Ready Status Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
3	R/W	DMA_INTERRUPT_STAT_EN	DMA Interrupt Status Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
2	R/W	BGAP_EVENT_STAT_EN	Block Gap Event Status Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
1	R/W	XFER_COMPLETE_STAT_EN	Transfer Complete Status Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
0	R/W	CMD_COMPLETE_STAT_EN	Command Complete Status Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0

Table 935: EMMC_ERROR_INT_STAT_EN_R_REG (0x30058036)

Bit	Mode	Symbol	Description	Reset
15	R/W	VENDOR_ERR_STAT_EN3	The 15th bit of Error Interrupt Status Enable register is reserved. Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
14	R/W	VENDOR_ERR_STAT_EN2	The 14th bit of Error Interrupt Status Enable register is reserved. Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0

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Bit	Mode	Symbol	Description	Reset
13	R/W	VENDOR_ERR_STAT_EN1	The 13th bit of Error Interrupt Status Enable register is reserved. Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
12	R/W	BOOT_ACK_ERR_STAT_EN	Boot Acknowledgment Error (eMMC Mode only) Setting this bit to 1 enables setting of Boot Acknowledgment Error in Error Interrupt Status register (ERROR_INT_STAT_R). Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
11	R/W	RESP_ERR_STAT_EN	Response Error Status Enable (SD Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
10	R/W	TUNING_ERR_STAT_EN	Tuning Error Status Enable (UHS-I Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
9	R/W	ADMA_ERR_STAT_EN	ADMA Error Status Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
8	R/W	AUTO_CMD_ERR_STAT_EN	Auto CMD Error Status Enable (SD/eMMC Mode only). Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
7	R/W	CUR_LMT_ERR_STAT_EN	Current Limit Error Status Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
6	R/W	DATA_END_BIT_ERR_STAT_EN	Data End Bit Error Status Enable (SD/eMMC Mode only). Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0

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Bit	Mode	Symbol	Description	Reset
5	R/W	DATA_CRC_ERR_STAT_EN	Data CRC Error Status Enable (SD/eMMC Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
4	R/W	DATA_TOUT_ERR_STAT_EN	Data Timeout Error Status Enable (SD/eMMC Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
3	R/W	CMD_IDX_ERR_STAT_EN	Command Index Error Status Enable (SD/eMMC Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
2	R/W	CMD_END_BIT_ERR_STAT_EN	Command End Bit Error Status Enable (SD/eMMC Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
1	R/W	CMD_CRC_ERR_STAT_EN	Command CRC Error Status Enable (SD/eMMC Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
0	R/W	CMD_TOUT_ERR_STAT_EN	Command Timeout Error Status Enable (SD/eMMC Mode only). Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0

Table 936: EMMC_NORMAL_INT_SIGNAL_EN_R_REG (0x30058038)

Bit	Mode	Symbol	Description	Reset
15	R	-	Reserved	0x0
14	R/W	CQE_EVENT_SIGNAL_EN	Command Queuing Engine Event Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
13	R/W	FX_EVENT_SIGNAL_EN	FX Event Signal Enable Values:	0x0

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Bit	Mode	Symbol	Description	Reset
			0x0 (FALSE): Masked 0x1 (TRUE): Enabled	
12	R/W	RE_TUNE_EVENT_SIGNAL_EN	Re-Tuning Event (UHS-I only) Signal Enable. Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
11	R/W	INT_C_SIGNAL_EN	INT_C (Embedded) Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
10	R/W	INT_B_SIGNAL_EN	INT_B (Embedded) Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
9	R/W	INT_A_SIGNAL_EN	INT_A (Embedded) Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
8	R/W	CARD_INTERRUPT_SIGNAL_EN	Card Interrupt Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
7	R/W	CARD_REMOVAL_SIGNAL_EN	Card Removal Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
6	R/W	CARD_INSERTION_SIGNAL_EN	Card Insertion Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
5	R/W	BUF_RD_READY_SIGNAL_EN	Buffer Read Ready Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
4	R/W	BUF_WR_READY_SIGNAL_EN	Buffer Write Ready Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
3	R/W	DMA_INTERRUPT_SIGNAL_EN	DMA Interrupt Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
2	R/W	BGAP_EVENT_SIGNAL_EN	Block Gap Event Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0

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Bit	Mode	Symbol	Description	Reset
1	R/W	XFER_COMPLETE_SIGNAL_EN	Transfer Complete Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
0	R/W	CMD_COMPLETE_SIGNAL_EN	Command Complete Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0

Table 937: EMMC_ERROR_INT_SIGNAL_EN_R_REG (0x3005803A)

Bit	Mode	Symbol	Description	Reset
15	R/W	VENDOR_ERR_SIGNAL_EN3	The 16th bit of Error Interrupt Signal Enable is reserved. Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
14	R/W	VENDOR_ERR_SIGNAL_EN2	The 15th bit of Error Interrupt Signal Enable is reserved. Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
13	R/W	VENDOR_ERR_SIGNAL_EN1	The 14th bit of Error Interrupt Signal Enable is reserved. Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
12	R/W	BOOT_ACK_ERR_SIGNAL_EN	Boot Acknowledgment Error (eMMC Mode only). Setting this bit to 1 enables generating interrupt signal when Boot Acknowledgement Error in Error Interrupt Status register is set. Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
11	R/W	RESP_ERR_SIGNAL_EN	Response Error Signal Enable (SD Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
10	R/W	TUNING_ERR_SIGNAL_EN	Tuning Error Signal Enable (UHS-I Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
9	R/W	ADMA_ERR_SIGNAL_EN	ADMA Error Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0

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Bit	Mode	Symbol	Description	Reset
8	R/W	AUTO_CMD_ERR_SIGNAL_EN	Auto CMD Error Signal Enable (SD/eMMC Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
7	R/W	CUR_LMT_ERR_SIGNAL_EN	Current Limit Error Signal Enable Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
6	R/W	DATA_END_BIT_ERR_SIGNAL_EN	Data End Bit Error Signal Enable (SD/eMMC Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
5	R/W	DATA_CRC_ERR_SIGNAL_EN	Data CRC Error Signal Enable (SD/eMMC Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
4	R/W	DATA_TOUT_ERR_SIGNAL_EN	Data Timeout Error Signal Enable (SD/eMMC Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
3	R/W	CMD_IDX_ERR_SIGNAL_EN	Command Index Error Signal Enable (SD/eMMC Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
2	R/W	CMD_END_BIT_ERR_SIGNAL_EN	Command End Bit Error Signal Enable (SD/eMMC Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
1	R/W	CMD_CRC_ERR_SIGNAL_EN	Command CRC Error Signal Enable (SD/eMMC Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0
0	R/W	CMD_TOUT_ERR_SIGNAL_EN	Command Timeout Error Signal Enable (SD/eMMC Mode only) Values: 0x0 (FALSE): Masked 0x1 (TRUE): Enabled	0x0

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Table 938: EMMC_AUTO_CMD_STAT_R_REG (0x3005803C)

Bit	Mode	Symbol	Description	Reset
15:8	R	-	Reserved	0x0
7	R	CMD_NOT_ISSUED_AUTO_CMD12	Command Not Issued By Auto CMD12 Error If this bit is set to 1, CMD_wo_DAT is not executed due to an Auto CMD12 Error (D04-D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Values: 0x1 (TRUE): Not Issued 0x0 (FALSE): No Error	0x0
6	R	-	Reserved	0x0
5	R	AUTO_CMD_RESP_ERR	Auto CMD Response Error This bit is set when Response Error Check Enable in the Transfer Mode register is set to 1 and an error is detected in R1 response of either Auto CMD12 or CMD13. This status is ignored if any bit between D00 to D04 is set to 1. Values: 0x1 (TRUE): Error 0x0 (FALSE): No Error	0x0
4	R	AUTO_CMD_IDX_ERR	Auto CMD Index Error This bit is set if the command index error occurs in response to a command. Values: 0x1 (TRUE): Error 0x0 (FALSE): No Error	0x0
3	R	AUTO_CMD_EBIT_ERR	Auto CMD End Bit Error This bit is set when detecting that the end bit of command response is 0. Values: 0x1 (TRUE): End Bit Error Generated 0x0 (FALSE): No Error	0x0
2	R	AUTO_CMD_CRC_ERR	Auto CMD CRC Error This bit is set when detecting a CRC error in the command response. Values: 0x1 (TRUE): CRC Error Generated 0x0 (FALSE): No Error	0x0
1	R	AUTO_CMD_TOUT_ERR	Auto CMD Timeout Error This bit is set if no response is returned with 64 SDCLK cycles from the end bit of the command. If this bit is set to 1, error status bits (D04-D01) are meaningless. Values: 0x1 (TRUE): Time out 0x0 (FALSE): No Error	0x0
0	R	AUTO_CMD12_NOT_EXEC	Auto CMD12 Not Executed If multiple memory block data transfer is not started due to a command error, this bit is not set	0x0

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Bit	Mode	Symbol	Description	Reset
			because it is not necessary to issue an Auto CMD12. Setting this bit to 1 means that the Host Controller cannot issue Auto CMD12 to stop multiple memory block data transfer, due to some error. If this bit is set to 1, error status bits (D04-D01) is meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Values: 0x1 (TRUE): Not Executed 0x0 (FALSE): Executed	

Table 939: EMMC_HOST_CTRL2_R_REG (0x3005803E)

Bit	Mode	Symbol	Description	Reset
15	R/W	PRESET_VAL_ENABLE	Preset Value Enable This bit enables automatic selection of SDCLK frequency and Driver strength Preset Value registers. When Preset Value Enable is set, SDCLK frequency generation (Frequency Select and Clock Generator Select) and the driver strength selection are performed by the controller. These values are selected from set of Preset Value registers based on selected speed mode. Values: 0x0 (FALSE): SDCLK and Driver Strength are controlled by Host Driver 0x1 (TRUE): Automatic Selection by Preset Value are Enabled	0x0
14	R/W	ASYNC_INT_ENABLE	Asynchronous Interrupt Enable This bit can be set if a card supports asynchronous interrupts and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Values: 0x0 (FALSE): Disabled 0x1 (TRUE): Enabled	0x0
13	R/W	ADDRESSING	64-bit Addressing This bit is effective when Host Version 4 Enable is set to 1. Values: 0x0 (FALSE): 32 bits addressing 0x1 (TRUE): 64 bits addressing	0x0
12	R/W	HOST_VER4_ENABLE	Host Version 4 Enable This bit selects either Version 3.00 compatible mode or Version 4 mode. Functions of following fields are modified for Host Version 4 mode: - SDMA Address: SDMA uses ADMA System Address (05Fh-058h) instead of SDMA System Address register (003h-000h)	0x0

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Bit	Mode	Symbol	Description	Reset
			- ADMA2/ADMA3 selection: ADMA3 is selected by DMA select in Host Control 1 register - 64-bit ADMA Descriptor Size: 128-bit descriptor is used instead of 96-bit descriptor when 64-bit Addressing is set to 1 - Selection of 32-bit/64-bit System Addressing: Either 32-bit or 64-bit system addressing is selected by 64-bit Addressing bit in this register - 32-bit Block Count: SDMA System Address register (003h-000h) is modified to 32-bit Block Count register Note: It is recommended not to program ADMA3 Integrated Descriptor Address registers, UHS-II registers and Command Queuing registers (if applicable) while operating in Host version less than 4 mode (Host Version 4 Enable = 0). Values: 0x0 (FALSE): Version 3.00 compatible mode 0x1 (TRUE): Version 4 mode	
11	R/W	CMD23_ENABLE	CMD23 Enable If the card supports CMD23, this bit is set to 1. This bit is used to select Auto CMD23 or Auto CMD12 for ADMA3 data transfer. Values: 0x0 (FALSE): Auto CMD23 is disabled 0x1 (TRUE): Auto CMD23 is enabled	0x0
10	R/W	ADMA2_LEN_MODE	ADMA2 Length Mode This bit selects ADMA2 Length mode to be either 16-bit or 26-bit. Values: 0x0 (FALSE): 16-bit Data Length Mode 0x1 (TRUE): 26-bit Data Length Mode	0x0
9	R	-	Reserved	0x0
8	R/W	UHS2_IF_ENABLE	UHS-II Interface Enable This bit is used to enable the UHS-II Interface. The value is reflected on the uhs2_if_en pin. Values: 0x0 (FALSE): SD/eMMC Interface Enabled 0x1 (TRUE): UHS-II Interface Enabled	0x0
7	R/W	SAMPLE_CLK_SEL	Sampling Clock Select This bit is used by the Host Controller to select the sampling clock in SD/eMMC mode to receive CMD and DAT. This bit is set by the tuning procedure and is valid after the completion of tuning (when Execute Tuning is cleared). Setting this bit to 1 means that tuning is completed successfully and setting this bit to 0 means that tuning has failed. The value is reflected on the sample_cclk_sel pin. Values: 0x0 (FALSE): Fixed clock is used to sample data 0x1 (TRUE): Tuned clock is used to sample data	0x0
6	R/W	EXEC_TUNING	Execute Tuning	0x0

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Bit	Mode	Symbol	Description	Reset
			This bit is set to 1 to start the tuning procedure in UHS-I/eMMC speed modes and this bit is automatically cleared when tuning procedure is completed. Values: 0x0 (FALSE): Not Tuned or Tuning completed 0x1 (TRUE): Execute Tuning	
5:4	R/W	DRV_STRENGTH_SEL	Driver Strength Select This bit is used to select the Host Controller output driver in 1.8 V signaling UHS-I/eMMC speed modes. The bit depends on setting of Preset Value Enable. The value is reflected on the uhs1_drv_sth pin. Values: 0x0 (TYPEB): Driver TYPEB is selected 0x1 (TYPEA): Driver TYPEA is selected 0x2 (TYPEC): Driver TYPEC is selected 0x3 (TYPED): Driver TYPED is selected	0x0
3	R/W	SIGNALING_EN	1.8 V Signaling Enable This bit controls voltage regulator for I/O cell in UHS-I/eMMC speed modes. Setting this bit from 0 to 1 starts changing the signal voltage from 3.3 V to 1.8 V. Host Controller clears this bit if switching to 1.8 signaling fails. The value is reflected on the uhs1_swvolt_en pin. Note: This bit must be set for all UHS-I speed modes (SDR12/SDR25/SDR50/SDR104/DDR50). Values: 0x0 (V_3_3): 3.3 V Signalling 0x1 (V_1_8): 1.8 V Signalling	0x0
2:0	R/W	UHS_MODE_SEL	UHS Mode/eMMC Speed Mode Select These bits are used to select UHS mode in the SD mode of operation. In eMMC mode, these bits are used to select eMMC Speed mode. UHS Mode (SD/UHS-II mode only): - 0x0: SDR12 - 0x1: SDR25 - 0x2: SDR50 - 0x3: SDR104 - 0x4: DDR50 - 0x5: Reserved - 0x6: Reserved - 0x7: UHS-II eMMC Speed Mode (eMMC mode only): - 0x0: Legacy - 0x1: High Speed SDR - 0x2: Reserved - 0x3: HS200 - 0x4: High Speed DDR - 0x5: Reserved - 0x6: Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
			- 0x7: HS400 Values: 0x0 (SDR12): SDR12/Legacy 0x1 (SDR25): SDR25/High Speed SDR 0x2 (SDR50): SDR50 0x3 (SDR104): SDR104/HS200 0x4 (DDR50): DDR50/High Speed DDR 0x5 (RSVD5): Reserved 0x6 (RSVD6): Reserved 0x7 (UHS2): UHS-II/HS400	

Table 940: EMMC_CAPABILITIES1_R_REG (0x30058040)

Bit	Mode	Symbol	Description	Reset
31:30	R	SLOT_TYPE_R	Slot Type These bits indicate usage of a slot by a specific Host System. Values: 0x0 (REMOVABLE_SLOT): Removable Card Slot 0x1 (EMBEDDED_SLOT): Embedded Slot for one Device 0x2 (SHARED_SLOT): Shared Bus Slot (SD mode) 0x3 (UHS2_EMBEDDED_SLOT): UHS-II MultipleEmbedded Devices	0x0
29	R	ASYNC_INT_SUPPORT	Asynchronous Interrupt Support (SD Mode only) Values: 0x0 (FALSE): Asynchronous Interrupt Not Supported 0x1 (TRUE): Asynchronous Interrupt Supported	0x1
28	R	SYS_ADDR_64_V3	64-bit System Address Support for V3 This bit sets the Host controller to support 64-bit System Addressing of V3 mode. SDMA cannot be used in 64-bit Addressing in Version 3 Mode. If this bit is set to 1, 64-bit ADMA2 with using 96-bit Descriptor can be enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 0) and DMA select (DMA_SEL = 11b). Values: 0x0 (FALSE): 64-bit System Address for V3 is Not Supported 0x1 (TRUE): 64-bit System Address for V3 is Supported	0x0
27	R	SYS_ADDR_64_V4	64-bit System Address Support for V4 This bit sets the Host Controller to support 64-bit System Addressing of V4 mode. When this bit is set to 1, full or part of 64-bit address must be used to decode the Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of	0x0

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Bit	Mode	Symbol	Description	Reset
			Host Controller registers is effective regardless of setting to 64-bit Addressing in Host Control 2. If this bit is set to 1, 64-bit DMA Addressing for version 4 is enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 1) and by setting 64-bit Addressing (ADDRESSING =1) in the Host Control 2 register. SDMA can be used and ADMA2 uses 128-bit Descriptor. Values: 0x0 (FALSE): 64-bit System Address for V4 is Not Supported 0x1 (TRUE): 64-bit System Address for V4 is Supported	
26	R	VOLT_18	Voltage Support for 1.8 V Values: 0x0 (FALSE): 1.8 V Not Supported 0x1 (TRUE): 1.8 V Supported	0x0
25	R	VOLT_30	Voltage Support for SD 3.0 V or Embedded 1.2 V Values: 0x0 (FALSE): SD 3.0 V or Embedded 1.2 V Not Supported 0x1 (TRUE): SD 3.0 V or Embedded Supported	0x0
24	R	VOLT_33	Voltage Support for 3.3 V Values: 0x0 (FALSE): 3.3 V Not Supported 0x1 (TRUE): 3.3 V Supported	0x0
23	R	SUS_RES_SUPPORT	Suspense/Resume Support This bit indicates whether the Host Controller supports Suspend/Resume functionality. If this bit is 0, the Host Driver does not issue either Suspend or Resume commands because the Suspend and Resume mechanism is not supported. Values: 0x0 (FALSE): Not Supported 0x1 (TRUE): Supported	0x0
22	R	SDMA_SUPPORT	SDMA Support This bit indicates whether the Host Controller is capable of using SDMA to transfer data between the system memory and the Host Controller directly. Values: 0x0 (FALSE): SDMA not Supported 0x1 (TRUE): SDMA Supported	0x1
21	R	HIGH_SPEED_SUPPORT	High Speed Support This bit indicates whether the Host Controller and the Host System supports High Speed mode and they can supply the SD Clock frequency from 25 MHz to 50 MHz. Values: 0x0 (FALSE): High Speed not Supported	0x1

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Bit	Mode	Symbol	Description	Reset
			0x1 (TRUE): High Speed Supported	
20	R	-	Reserved	0x0
19	R	ADMA2_SUPPORT	ADMA2 Support This bit indicates whether the Host Controller is capable of using ADMA2. Values: 0x0 (FALSE): ADMA2 not Supported 0x1 (TRUE): ADMA2 Supported	0x1
18	R	EMBEDDED_8_BIT	8-bit Support for Embedded Device This bit indicates whether the Host Controller is capable of using an 8-bit bus width mode. This bit is not effective when the Slot Type is set to 10b. Values: 0x0 (FALSE): 8-bit Bus Width not Supported 0x1 (TRUE): 8-bit Bus Width Supported	0x1
17:16	R	MAX_BLK_LEN	Maximum Block Length This bit indicates the maximum block size that the Host driver can read and write to the buffer in the Host Controller. The buffer transfers this block size without wait cycles. The transfer block length is always 512 bytes for the SD Memory irrespective of this bit Values: 0x0 (ZERO): 512 B 0x1 (ONE): 1024 B 0x2 (TWO): 2048 B 0x3 (THREE): Reserved	0x2
15:8	R	BASE_CLK_FREQ	Base Clock Frequency for SD clock These bits indicate the base (maximum) clock frequency for the SD Clock. The definition of these bits depend on the Host Controller Version. - 6-Bit Base Clock Frequency: This mode is supported by the Host Controller version 1.00 and 2.00. The upper 2 bits are not effective and are always 0. The unit values are 1 MHz. The supported clock range is 10 MHz to 63 MHz. -- 0x00 : Get information through another method -- 0x01 : 1 MHz -- 0x02 : 2 MHz -- ..... -- 0x3F : 63 MHz -- 0x40-0xFF : Not Supported - 8-Bit Base Clock Frequency: This mode is supported by the Host Controller version 3.00. The unit values are 1 MHz. The supported clock range is 10 MHz to 255 MHz. -- 0x00 : Get information through another method -- 0x01 : 1 MHz -- 0x02 : 2 MHz -- ..... -- 0xFF : 255 MHz	0x30

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Bit	Mode	Symbol	Description	Reset
			If the frequency is 16.5 MHz, the larger value is set to 0001001b (17 MHz) because the Host Driver uses this value to calculate the clock divider value and it does not exceed the upper limit of the SD Clock frequency. If these bits are all 0, the Host system has to get information using a different method.	
7	R	TOUT_CLK_UNIT	Timeout Clock Unit This bit shows the unit of base clock frequency used to detect Data TImeout Error. Values: 0x0 (kHZ): kHz 0x1 (MHZ): MHz	0x1
6	R	-	Reserved	0x0
5:0	R	TOUT_CLK_FREQ	Timeout Clock Frequency This bit shows the base clock frequency used to detect Data Timeout Error. The Timeout Clock unit defines the unit of timeout clock frequency. It can be kHz or MHz. - 0x00 : Get information through another method - 0x01 : 1 kHz/1 MHz - 0x02 : 2 kHz /2 MHz - 0x03 : 3 kHz/3 MHz - ..... - 0x3F : 63 kHz/63 MHz	0x20

Table 941: EMMC_CAPABILITIES2_R_REG (0x30058044)

Bit	Mode	Symbol	Description	Reset
31:30	R	-	Reserved	0x0
29	R	-	Reserved	0x0
28	R	VDD2_18V_SUPPORT	1.8 V VDD2 Support This bit indicates support of VDD2 for the Host System. Values: 0x0 (FALSE): 1.8 V VDD2 is not Supported 0x1 (TRUE): 1.8 V VDD2 is Supported	0x0
27	R	ADMA3_SUPPORT	ADMA3 Support This bit indicates whether the Host Controller is capable of using ADMA3. Values: 0x0 (FALSE): ADMA3 not Supported 0x1 (TRUE): ADMA3 Supported	0x0
26:24	R	-	Reserved	0x0
23:16	R	CLK_MUL	Clock Multiplier These bits indicate the clock multiplier of the programmable clock generator. Setting these bits	0x0

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Bit	Mode	Symbol	Description	Reset
			to 0 means that the Host Controller does not support a programmable clock generator. - 0x0: Clock Multiplier is not Supported - 0x1: Clock Multiplier M = 2 - 0x2: Clock Multiplier M = 3 - ..... - 0xFF: Clock Multiplier M = 256	
15:14	R	RE_TUNING_MODES	Re-Tuning Modes (UHS-I only) These bits select the re-tuning method and limit the maximum data length. Values: 0x0 (MODE1): Timer 0x1 (MODE2): Timer and Re-Tuning Request (Not supported) 0x2 (MODE3): Auto Re-Tuning (for transfer) 0x3 (RSVD_MODE): Reserved	0x0
13	R	USE_TUNING_SDR50	Use Tuning for SDR50 (UHS-I only)	0x0
12	R	-	Reserved	0x0
11:8	R	RETUNE_CNT	Timer Count for Re-Tuning (UHS-I only) - 0x0: Re-Tuning Timer disabled - 0x1: 1 seconds - 0x2: 2 seconds - 0x3: 4 seconds - ..... - 0xB: 1024 seconds - 0xC: Reserved - 0xD: Reserved - 0xE: Reserved - 0xF: Get information from other source	0x0
7	R	-	Reserved	0x0
6	R	DRV_TYPED	Driver Type D Support (UHS-I only) This bit indicates support of Driver Type D for 1.8 Signaling. Values: Description 0x0 (FALSE): Driver Type D is not supported 0x1 (TRUE): Driver Type D is supported	0x1
5	R	DRV_TYPEC	Driver Type C Support (UHS-I only) This bit indicates support of Driver Type C for 1.8 Signaling. Values: 0x0 (FALSE): Driver Type C is not supported 0x1 (TRUE): Driver Type C is supported	0x1
4	R	DRV_TYPEA	Driver Type A Support (UHS-I only) This bit indicates support of Driver Type A for 1.8 Signaling. Values:	0x1

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Bit	Mode	Symbol	Description	Reset
			0x0 (FALSE): Driver Type A is not supported 0x1 (TRUE): Driver Type A is supported	
3	R	UHS2_SUPPORT	UHS-II Support (UHS-II only) This bit indicates whether Host Controller supports UHS-II. Values: 0x0 (FALSE): UHS-II is not supported 0x1 (TRUE): UHS-II is supported	0x0
2	R	DDR50_SUPPORT	DDR50 Support (UHS-I only) Values: 0x0 (FALSE): DDR50 is not supported 0x1 (TRUE): DDR50 is supported	0x1
1	R	SDR104_SUPPORT	SDR104 Support (UHS-I only) This bit mentions that SDR104 requires tuning. Values: 0x0 (FALSE): SDR104 is not supported 0x1 (TRUE): SDR104 is supported	0x1
0	R	SDR50_SUPPORT	SDR50 Support (UHS-I only) Thsi bit indicates that SDR50 is supported. The bit 13 (USE_TUNING_SDR50) indicates whether SDR50 requires tuning or not. Values: 0x0 (FALSE): SDR50 is not supported 0x1 (TRUE): SDR50 is supported	0x1

Table 942: EMMC_CURR_CAPABILITIES1_R_REG (0x30058048)

Bit	Mode	Symbol	Description	Reset
31:24	R	-	Reserved	0x0
23:16	R	MAX_CUR_18V	Maximum Current for 1.8 V This bit specifies the Maximum Current for 1.8 V VDD1 power supply for the card. - 0: Get information through another method - 1: 4 mA - 2: 8 mA - 3: 13 mA - ..... - 255: 1020 mA	0x0
15:8	R	MAX_CUR_30V	Maximum Current for 3.0 V This bit specifies the Maximum Current for 3.0 V VDD1 power supply for the card. - 0: Get information through another method - 1: 4 mA - 2: 8 mA - 3: 13 mA - ..... - 255: 1020 mA	0x0

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Bit	Mode	Symbol	Description	Reset
7:0	R	MAX_CUR_33V	Maximum Current for 3.3 V This bit specifies the Maximum Current for 3.3 V VDD1 power supply for the card. - 0: Get information through another method - 1: 4 mA - 2: 8 mA - 3: 13 mA - ..... - 255: 1020 mA	0x0

Table 943: EMMC_CURR_CAPABILITIES2_R_REG (0x3005804C)

Bit	Mode	Symbol	Description	Reset
31:8	R	-	Reserved	0x0
7:0	R	MAX_CUR_VDD2_18V	Maximum Current for 1.8 V VDD2 This bit specifies the Maximum Current for 1.8 V VDD2 power supply for the UHS-II card. - 0: Get information through another method - 1: 4 mA - 2: 8 mA - 3: 13 mA - ..... - 255: 1020 mA	0x0

Table 944: EMMC_FORCE_AUTO_CMD_STAT_R_REG (0x30058050)

Bit	Mode	Symbol	Description	Reset
15:8	R	-	Reserved	0x0
7	W	FORCE_CMD_NOT_ISSUED_AUTO_CMD12	Force Event for Command Not Issued By Auto CMD12 Error Values: 0x1 (TRUE): Command Not Issued By Auto CMD12 Error Status is set 0x0 (FALSE): Not Affected	0x0
6	R	-	Reserved	0x0
5	W	FORCE_AUTO_CMD_RESP_ERR	Force Event for Auto CMD Response Error Values: 0x1 (TRUE): Auto CMD Response Error Status is set 0x0 (FALSE): Not Affected	0x0
4	W	FORCE_AUTO_CMD_IDX_ERR	Force Event for Auto CMD Index Error Values: 0x1 (TRUE): Auto CMD Index Error Status is set 0x0 (FALSE): Not Affected	0x0
3	W	FORCE_AUTO_CMD_EBIT_ERR	Force Event for Auto CMD End Bit Error Values:	0x0

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Bit	Mode	Symbol	Description	Reset
			0x1 (TRUE): Auto CMD End Bit Error Status is set 0x0 (FALSE): Not Affected	
2	W	FORCE_AUTO_CMD_CRC_ERR	Force Event for Auto CMD CRC Error Values: 0x1 (TRUE): Auto CMD CRC Error Status is set 0x0 (FALSE): Not Affected	0x0
1	W	FORCE_AUTO_CMD_TOUT_ERR	Force Event for Auto CMD Timeout Error Values: 0x1 (TRUE): Auto CMD Timeout Error Status is set 0x0 (FALSE): Not Affected	0x0
0	W	FORCE_AUTO_CMD12_NOT_EXEC	Force Event for Auto CMD12 Not Executed Values: 0x1 (TRUE): Auto CMD12 Not Executed Status is set 0x0 (FALSE): Not Affected	0x0

Table 945: EMMC_FORCE_ERROR_INT_STAT_R_REG (0x30058052)

Bit	Mode	Symbol	Description	Reset
15	W	FORCE_VENDOR_ERR3	This bit (FORCE_VENDOR_ERR3) of the FORCE_ERROR_INT_STAT_R register is reserved. It always returns 0.	0x0
14	W	FORCE_VENDOR_ERR2	This bit (FORCE_VENDOR_ERR2) of the FORCE_ERROR_INT_STAT_R register is reserved. It always returns 0.	0x0
13	W	FORCE_VENDOR_ERR1	This bit (FORCE_VENDOR_ERR1) of the FORCE_ERROR_INT_STAT_R register is reserved. It always returns 0.	0x0
12	W	FORCE_BOOT_ACK_ERR	Force Event for Boot Ack error Values: 0x0 (FALSE): Not Affected 0x1 (TRUE): Boot ack Error Status is set	0x0
11	W	FORCE_RESP_ERR	Force Event for Response Error (SD Mode only) Values: 0x0 (FALSE): Not Affected 0x1 (TRUE): Response Error Status is set	0x0
10	W	FORCE_TUNING_ERR	Force Event for Tuning Error (UHS-I Mode only)	0x0
9	W	FORCE_ADMA_ERR	Force Event for ADMA Error Values: 0x0 (FALSE): Not Affected 0x1 (TRUE): ADMA Error Status is set	0x0

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Bit	Mode	Symbol	Description	Reset
8	W	FORCE_AUTO_CMD_ERR	Force Event for Auto CMD Error (SD/eMMC Mode only) Values: 0x0 (FALSE): Not Affected 0x1 (TRUE): ADMA Error Status is set	0x0
7	W	FORCE_CUR_LMT_ERR	Force Event for Current Limit Error Values: 0x0 (FALSE): Not Affected 0x1 (TRUE): Current Limit Error Status is set	0x0
6	W	FORCE_DATA_END_BIT_ERR	Force Event for Data End Bit Error (SD/eMMC Mode only) Values: 0x0 (FALSE): Not Affected 0x1 (TRUE): Data End Bit Error Status is set	0x0
5	W	FORCE_DATA_CRC_ERR	Force Event for Data CRC Error (SD/eMMC Mode only) Values: 0x0 (FALSE): Not Affected 0x1 (TRUE): Data CRC Error Status is set	0x0
4	W	FORCE_DATA_TOUT_ERR	Force Event for Data Timeout Error (SD/eMMC Mode only) Values: 0x0 (FALSE): Not Affected 0x1 (TRUE): Data Timeout Error Status is set	0x0
3	W	FORCE_CMD_IDX_ERR	Force Event for Command Index Error (SD/eMMC Mode only) Values: 0x0 (FALSE): Not Affected 0x1 (TRUE): Command Index Error Status is set	0x0
2	W	FORCE_CMD_END_BIT_ERR	Force Event for Command End Bit Error (SD/eMMC Mode only) Values: 0x0 (FALSE): Not Affected 0x1 (TRUE): Command End Bit Error Status is set	0x0
1	W	FORCE_CMD_CRC_ERR	Force Event for Command CRC Error (SD/eMMC Mode only) Values: 0x0 (FALSE): Not Affected 0x1 (TRUE): Command CRC Error Status is set	0x0
0	W	FORCE_CMD_TOUT_ERR	Force Event for Command Timeout Error (SD/eMMC Mode only) Values: 0x0 (FALSE): Not Affected 0x1 (TRUE): Command Timeout Error Status is set	0x0

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Table 946: EMMC_ADMA_ERR_STAT_R_REG (0x30058054)

Bit	Mode	Symbol	Description	Reset
7:3	R	-	Reserved	0x0
2	R	ADMA_LEN_ERR	ADMA Length Mismatch Error States This error occurs in the following instances: - While the Block Count Enable is being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length - When the total data length cannot be divided by the block length Values: 0x0 (NO_ERR): No Error 0x1 (ERROR): Error	0x0
1:0	R	ADMA_ERR_STATES	ADMA Error States These bits indicate the state of ADMA when an error occurs during ADMA data transfer. Values: 0x0 (ST_STOP): Stop DMA - SYS_ADR register points to a location next to the error descriptor 0x1 (ST_FDS): Fetch Descriptor - SYS_ADR register points to the error descriptor 0x2 (UNUSED): Never set this state 0x3 (ST_TFR): Transfer Data - SYS_ADR register points to a location next to the error descriptor	0x0

Table 947: EMMC_ADMA_SA_LOW_R_REG (0x30058058)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	ADMA_SA_LOW	ADMA System Address These bits indicate the lower 32 bits of the ADMA system address. - SDMA: If Host Version 4 Enable is set to 1, this register stores the system address of the data location - ADMA2: This register stores the byte address of the executing command of the descriptor table - ADMA3: This register is set by ADMA3. ADMA2 increments the address of this register that points to the next line, every time a Descriptor line is fetched.	0x0

Table 948: EMMC_PRESET_INIT_R_REG (0x30058060)

Bit	Mode	Symbol	Description	Reset
15:14	R	DRV_SEL_VAL	Driver Strength Select Value	0x0

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Bit	Mode	Symbol	Description	Reset
			These bits indicate that the Driver strength is supported by 1.8 V signaling bus speed modes. These bits are meaningless for 3.3 V signaling. Values: 0x0 (TYPEB): Driver Type B is selected 0x1 (TYPEA): Driver Type A is selected 0x2 (TYPEC): Driver Type C is selected 0x3 (TYPED): Driver Type D is selected	
13:11	R	-	Reserved	0x0
10	R	CLK_GEN_SEL_VAL	Clock Generator Select Value This bit is effective when the Host Controller supports a programmable clock generator. Values: 0x0 (FALSE): Host Controller Ver2.0 Compatible Clock Generator 0x1 (PROG): Programmable Clock Generator	0x0
9:0	R	FREQ_SEL_VAL	SDCLK/RCLK Frequency Select Value 10-bit preset value to be set in SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.	0x0

Table 949: EMMC_PRESET_DS_R_REG (0x30058062)

Bit	Mode	Symbol	Description	Reset
15:14	R	DRV_SEL_VAL	Driver Strength Select Value These bits indicate the Driver strength value supported by 1.8 V signaling bus speed modes. This field is meaningless for the Default speed mode as it uses 3.3 V signaling. Values: 0x0 (TYPEB): Driver Type B is selected 0x1 (TYPEA): Driver Type A is selected 0x2 (TYPEC): Driver Type C is selected 0x3 (TYPED): Driver Type D is selected	0x0
13:11	R	-	Reserved	0x0
10	R	CLK_GEN_SEL_VAL	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. Values: 0x0 (FALSE): Host Controller Ver2.0 Compatible Clock Generator 0x1 (PROG): Programmable Clock Generator	0x0
9:0	R	FREQ_SEL_VAL	SDCLK/RCLK Frequency Select Value 10-bit preset value to be set in SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.	0x0

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Table 950: EMMC_PRESET_HS_R_REG (0x30058064)

Bit	Mode	Symbol	Description	Reset
15:14	R	DRV_SEL_VAL	Driver Strength Select Value These bits indicate the Driver strength value supported by 1.8 V signaling bus speed modes. This field is meaningless for High speed mode as it uses 3.3 V signaling. Values: 0x0 (TYPEB): Driver Type B is selected 0x1 (TYPEA): Driver Type A is selected 0x2 (TYPEC): Driver Type C is selected 0x3 (TYPED): Driver Type D is selected	0x0
13:11	R	-	Reserved	0x0
10	R	CLK_GEN_SEL_VAL	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. Values: 0x0 (FALSE): Host Controller Ver2.0 Compatible Clock Generator 0x1 (PROG): Programmable Clock Generator	0x0
9:0	R	FREQ_SEL_VAL	SDCLK/RCLK Frequency Select Value 10-bit preset value to be set in SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.	0x0

Table 951: EMMC_PRESET_SDR12_R_REG (0x30058066)

Bit	Mode	Symbol	Description	Reset
15:14	R	DRV_SEL_VAL	Driver Strength Select Value These bits indicate the Driver strength value supported for the SDR12 bus speed mode. These bits are meaningless for 3.3 V signaling. Values: 0x0 (TYPEB): Driver Type B is selected 0x1 (TYPEA): Driver Type A is selected 0x2 (TYPEC): Driver Type C is selected 0x3 (TYPED): Driver Type D is selected	0x0
13:11	R	-	Reserved	0x0
10	R	CLK_GEN_SEL_VAL	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator Values: 0x0 (FALSE): Host Controller Ver2.0 Compatible Clock Generator 0x1 (PROG): Programmable Clock Generator	0x0
9:0	R	FREQ_SEL_VAL	SDCLK/RCLK Frequency Select Value 10-bit preset value to be set in SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.	0x0

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Table 952: EMMC_PRESET_SDR25_R_REG (0x30058068)

Bit	Mode	Symbol	Description	Reset
15:14	R	DRV_SEL_VAL	Driver Strength Select Value These bits indicate the Driver strength value supported for the SDR25 bus speed mode. These bits are meaningless for 3.3 V signaling. Values: 0x0 (TYPEB): Driver Type B is selected 0x1 (TYPEA): Driver Type A is selected 0x2 (TYPEC): Driver Type C is selected 0x3 (TYPED): Driver Type D is selected	0x0
13:11	R	-	Reserved	0x0
10	R	CLK_GEN_SEL_VAL	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. Values: 0x0 (FALSE): Host Controller Ver2.0 Compatible Clock Generator 0x1 (PROG): Programmable Clock Generator	0x0
9:0	R	FREQ_SEL_VAL	SDCLK/RCLK Frequency Select Value 10-bit preset value to be set in SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.	0x0

Table 953: EMMC_PRESET_SDR50_R_REG (0x3005806A)

Bit	Mode	Symbol	Description	Reset
15:14	R	DRV_SEL_VAL	Driver Strength Select Value These bits indicate Driver strength value supported for SDR50 bus speed mode. These bits are meaningless for 3.3 V signaling. Values: 0x0 (TYPEB): Driver Type B is selected 0x1 (TYPEA): Driver Type A is selected 0x2 (TYPEC): Driver Type C is selected 0x3 (TYPED): Driver Type D is selected	0x0
13:11	R	-	Reserved	0x0
10	R	CLK_GEN_SEL_VAL	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. Values: 0x0 (FALSE): Host Controller Ver2.0 Compatible Clock Generator 0x1 (PROG): Programmable Clock Generator	0x0
9:0	R	FREQ_SEL_VAL	SDCLK/RCLK Frequency Select Value 10-bit preset value to be set in SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.	0x0

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Table 954: EMMC_PRESET_SDR104_R_REG (0x3005806C)

Bit	Mode	Symbol	Description	Reset
15:14	R	DRV_SEL_VAL	Driver Strength Select Value These bits indicate Driver strength value supported for SDR104 bus speed mode. These bits are meaningless for 3.3 V signaling. Values: 0x0 (TYPEB): Driver Type B is selected 0x1 (TYPEA): Driver Type A is selected 0x2 (TYPEC): Driver Type C is selected 0x3 (TYPED): Driver Type D is selected	0x0
13:11	R	-	Reserved	0x0
10	R	CLK_GEN_SEL_VAL	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. Values: 0x0 (FALSE): Host Controller Ver2.0 Compatible Clock Generator 0x1 (PROG): Programmable Clock Generator	0x0
9:0	R	FREQ_SEL_VAL	SDCLK/RCLK Frequency Select Value These bits specify a 10-bit preset value that must be set in the SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.	0x0

Table 955: EMMC_PRESET_DDR50_R_REG (0x3005806E)

Bit	Mode	Symbol	Description	Reset
15:14	R	DRV_SEL_VAL	Driver Strength Select Value These bits indicate Driver strength value supported for DDR50 bus speed mode. These bits are meaningless for 3.3 V signaling. Values: 0x0 (TYPEB): Driver Type B is selected 0x1 (TYPEA): Driver Type A is selected 0x2 (TYPEC): Driver Type C is selected 0x3 (TYPED): Driver Type D is selected	0x0
13:11	R	-	Reserved	0x0
10	R	CLK_GEN_SEL_VAL	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. Values: 0x0 (FALSE): Host Controller Ver2.0 Compatible Clock Generator 0x1 (PROG): Programmable Clock Generator	0x0
9:0	R	FREQ_SEL_VAL	SDCLK/RCLK Frequency Select Value	0x0

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Bit	Mode	Symbol	Description	Reset
			These bits specify a 10-bit preset value that must be set in the SDCLK/RCLK Frequency Select field of the Clock Control register, as described by a Host System.	

Table 956: EMMC_PRESET_UHS2_R_REG (0x30058074)

Bit	Mode	Symbol	Description	Reset
15:14	R	DRV_SEL_VAL	Driver Strength Select Value These bits indicate the Driver strength value supported by 1.8 V signaling bus speed modes in the SD mode. This field is meaningless for UHS-II mode. In eMMC mode, these bits can be used for selecting the Drive strength value for HS400 mode. Values: 0x0 (TYPEB): Driver Type B is selected 0x1 (TYPEA): Driver Type A is selected 0x2 (TYPEC): Driver Type C is selected 0x3 (TYPED): Driver Type D is selected	0x0
13:11	R	-	Reserved	0x0
10	R	CLK_GEN_SEL_VAL	Clock Generator Select Value This bit is effective when the Host Controller supports a programmable clock generator. Values: 0x0 (FALSE): Host Controller Ver2.0 Compatible Clock Generator 0x1 (PROG): Programmable Clock Generator	0x0
9:0	R	FREQ_SEL_VAL	SDCLK/RCLK Frequency Select Value These bits specify the 10-bit preset value that must be set in the SDCLK/RCLK Frequency Select field of the Clock Control register, as described by a Host System.	0x0

Table 957: EMMC_P_EMBEDDED_CNTRL_REG (0x300580E6)

Bit	Mode	Symbol	Description	Reset
15:12	R	-	Reserved	0x0
11:0	R	REG_OFFSET_EMBEDDED_CNTRL_ADDR	Offset Address of Embedded Control register.	0xF6C

Table 958: EMMC_P_VENDOR_SPECIFIC_AREA_REG (0x300580E8)

Bit	Mode	Symbol	Description	Reset
15:12	R	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
11:0	R	REG_OFFSET_ADDR_VENDOR	Base offset Address for Vendor-Specific registers.	0x500

Table 959: EMMC_P_VNDR2_SPECIFIC_AREA_REG (0x300580EA)

Bit	Mode	Symbol	Description	Reset
15:0	R	REG_OFFSET_ADDR_VNDR2	Base offset Address for Command Queuing registers.	0x180

Table 960: EMMC_SLOT_INTR_STATUS_R_REG (0x300580FC)

Bit	Mode	Symbol	Description	Reset
15:8	R	-	Reserved	0x0
7:0	R	INTR_SLOT	Interrupt signal for each Slot These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot. A maximum of 8 slots can be defined. If one interrupt signal is associated with multiple slots, the Host Driver can identify the interrupt that is generated by reading these bits. By a power on reset or by setting Software Reset For All bit, the interrupt signals are de-asserted and this status reads 00h. - Bit 00: Slot 1 - Bit 01: Slot 2 - Bit 02: Slot 3 - ..... - ..... - Bit 07: Slot 8	0x0

Table 961: EMMC_HOST_CNTRL_VERS_R_REG (0x300580FE)

Bit	Mode	Symbol	Description	Reset
15:8	R	VENDOR_VERSION_NUM	Vendor Version Number This field is reserved for the vendor version number. Host Driver must not use this status.	0x0
7:0	R	SPEC_VERSION_NUM	Specification Version Number These bits indicate the Host controller specification version. The upper and lower 4-bits indicate the version. Values 0x06-0xFF are reserved.	0x5

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Bit	Mode	Symbol	Description	Reset
			Values: 0x0 (VER_1_00): SD Host Controller Specification Version 1.00 0x1 (VER_2_00): SD Host Controller Specification Version 2.00 0x2 (VER_3_00): SD Host Controller Specification Version 3.00 0x3 (VER_4_00): SD Host Controller Specification Version 4.00 0x4 (VER_4_10): SD Host Controller Specification Version 4.10 0x5 (VER_4_20): SD Host Controller Specification Version 4.20	

Table 962: EMMC_CQCAP_REG (0x30058184)

Bit	Mode	Symbol	Description	Reset
31:29	R	-	Reserved	0x0
28	R	CRYPTO_SUPPORT	Crypto Support This bit indicates whether the Host Controller supports cryptographic operations. Values: 0x0 (FALSE): Crypto not Supported 0x1 (TRUE): Crypto Supported	0x0
27:16	R	CQCCAP_RSVD2	These bits [27:16] of the CQCAP register are reserved. They always return 0.	0x0
15:12	R	ITCFMUL	Internal Timer Clock Frequency Multiplier (ITCFMUL) This field indicates the frequency of the clock used for interrupt coalescing timer and for determining the SQS polling period. See ITCFVAL definition for details. Values 0x5 to 0xF are reserved. Values: 0x0 (CLK_1KHz): 1 kHz clock 0x1 (CLK_10KHz): 10 kHz clock 0x2 (CLK_100KHz): 100 kHz clock 0x3 (CLK_1MHz): 1 MHz clock 0x4 (CLK_10MHz): 10 MHz clock	0x3
11:10	R	-	Reserved	0x0
9:0	R	ITCFVAL	Internal Timer Clock Frequency Value (ITCFVAL) This field scales the frequency of the timer clock provided by ITCFMUL. The Final clock frequency of actual timer clock is calculated as ITCFVAL* ITCFMUL.	0xC8

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Table 963: EMMC_VER_ID_R_REG (0x30058500)

Bit	Mode	Symbol	Description	Reset
31:0	R	VER_ID	Current release number An application reading this register in conjunction with the VER_TYPE_R register, gathers details of the current release.	0x3138302A

Table 964: EMMC_VER_TYPE_R_REG (0x30058504)

Bit	Mode	Symbol	Description	Reset
31:0	R	VER_TYPE	Current release type An application reading this register in conjunction with the VER_ID_R register, gathers details of the current release.	0x67612A2A

Table 965: EMMC_CTRL_R_REG (0x30058508)

Bit	Mode	Symbol	Description	Reset
4	R/W	SW_CG_DIS	Internal clock gating disable control This bit must be used to disable IP's internal clock gating when required. when disabled clocks are not gated. Clocks to the core (except hclk) must be stopped when programming this bit. Values: 0x0 (ENABLE): Internal clock gates are active and clock gating is controlled internally 0x1 (DISABLE): Internal clock gating is disabled, clocks are not gated internally	0x0
3:1	R	-	Reserved	0x0
0	R/W	CMD_CONFLICT_CHECK	Command conflict check This bit enables command conflict check. Note:emmc controller monitors the CMD line whenever a command is issued and checks whether the value driven on sd_cmd_out matches the value on sd_cmd_in at next subsequent edge of cclk_tx to determine command conflict error. This bit is cleared only if the feed back delay (including IO Pad delay) is more than (t_card_clk_period - t_setup), where t_setup is the setup time of a flop in emmc. The I/O pad delay is consistent across CMD and DATA lines, and it is within the value: (2*t_card_clk_period - t_setup) Values: 0x0 (DISABLE_CMD_CONFLICT_CHK): Disable command conflict check 0x1 (CMD_CONFLICT_CHK_LAT1): Check for command conflict after 1 card clock cycle	0x1

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Table 966: EMMC_MBIU_CTRL_R_REG (0x30058510)

Bit	Mode	Symbol	Description	Reset
7:4	R	-	Reserved	0x0
3	R/W	BURST_INCR16_EN	INCR16 Burst Controls generation of INCR16 transfers on Master interface. Values: 0x0 (FALSE): AHB INCR16 burst type is not generated on Master I/F 0x1 (TRUE): AHB INCR16 burst type can be generated on Master I/F	0x1
2	R/W	BURST_INCR8_EN	INCR8 Burst Controls generation of INCR8 transfers on Master interface. Values: 0x0 (FALSE): AHB INCR8 burst type is not generated on Master I/F 0x1 (TRUE): AHB INCR8 burst type can be generated on Master I/F	0x1
1	R/W	BURST_INCR4_EN	INCR4 Burst Controls generation of INCR4 transfers on Master interface. Values: 0x0 (FALSE): AHB INCR4 burst type is not generated on Master I/F 0x1 (TRUE): AHB INCR4 burst type can be generated on Master I/F	0x1
0	R/W	UNDEFL_INCR_EN	Undefined INCR Burst Controls generation of undefined length INCR transfer on Master interface. Values: 0x0 (FALSE): Undefined INCR type burst is the least preferred burst on AHB Master I/F 0x1 (TRUE): Undefined INCR type burst is the most preferred burst on AHB Master I/F	0x0

Table 967: EMMC_EMMC_CTRL_R_REG (0x3005852C)

Bit	Mode	Symbol	Description	Reset
15:11	R	-	Reserved	0x0
10:4	R	-	Reserved	0x0
3	R/W	EMMC_RST_N_OE	Output Enable control for EMMC Device Reset signal PAD control. This field drived sd_rst_n_oe output ofemmc Values: 0x1 (ENABLE): sd_rst_n_oe is 1 0x0 (DISABLE): sd_rst_n_oe is 0	0x1
2	R/W	EMMC_RST_N	EMMC Device Reset signal control. This register field controls the sd_rst_n output of emmc	0x1

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Bit	Mode	Symbol	Description	Reset
			Values: 0x1 (RST_DEASSERT): Reset to eMMC device is deasserted 0x0 (RST_ASSERT): Reset to eMMC device asserted (active low)	
1	R/W	DISABLE_DATA_CRC_CHK	Disable Data CRC Check This bit controls masking of CRC16 error for Card Write in eMMC mode. This is useful in bus testing (CMD19) for an eMMC device. In bus testing, an eMMC card does not send CRC status for a block, which may generate CRC error. This CRC error can be masked using this bit during bus testing. Values: 0x1 (DISABLE): DATA CRC check is disabled 0x0 (ENABLE): DATA CRC check is enabled	0x0
0	R/W	CARD_IS_EMMC	eMMC Card present This bit indicates the type of card connected. An application program this bit based on the card connected to the controller Values: 0x1 (EMMC_CARD): Card connected to IP is an eMMC card 0x0 (NON_EMMC_CARD): Card connected to IP is a non-eMMC card	0x0

Table 968: EMMC_BOOT_CTRL_R_REG (0x3005852E)

Bit	Mode	Symbol	Description	Reset
15:12	R/W	BOOT_TOUT_CNT	Boot Ack Timeout Counter Value. This value determines the interval by which boot ack timeout (50 ms) is detected when boot ack is expected during boot operation. - 0xF : Reserved - 0xE : TMCLK x 2^27 - .. - ..... - 0x1 : TMCLK x 2^14 - 0x0 : TMCLK x 2^13	0x0
11:9	R	-	Reserved	0x0
8	R/W	BOOT_ACK_ENABLE	Boot Acknowledge Enable When this bit set, emmc checks for boot acknowledge start pattern of 0-1-0 during boot operation. This bit is applicable for both mandatory and alternate boot mode. Values: 0x1 (TRUE): Boot Ack enable 0x0 (FALSE): Boot Ack disable	0x0
7	W	VALIDATE_BOOT	Validate Mandatory Boot Enable bit This bit is used to validate the MAN_BOOT_EN bit. Values:	0x0

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Bit	Mode	Symbol	Description	Reset
			0x1 (TRUE): Validate Mandatory boot enable bit 0x0 (FALSE): Ignore Mandatory boot Enable bit	
6:1	R	-	Reserved	0x0
0	R/W	MAN_BOOT_EN	Mandatory Boot Enable This bit is used to initiate the mandatory boot operation. The application sets this bit along with VALIDATE_BOOT bit. Writing 0 is ignored. The emmc clears this bit after the boot transfer is completed or terminated. Values: 0x1 (MAN_BOOT_EN): Mandatory boot enable 0x0 (MAN_BOOT_DIS): Mandatory boot disable	0x0

Table 969: EMMC_AT_CTRL_R_REG (0x30058540)

Bit	Mode	Symbol	Description	Reset
26:24	R/W	SWIN_TH_VAL	Sampling window threshold value setting The maximum value that can be set here depends on the length of delayline used for tuning. A delayLine with 128 taps can use values from 0x0 to 0x7F. This field is valid only when SWIN_TH_EN is 1. Should be programmed only when SAMPLE_CLK_SEL is 0 - 0x0 : Threshold values is 0x1, windows of length 1 tap and above can be selected as sampling window. - 0x1 : Threshold values is 0x2, windows of length 2 taps and above can be selected as sampling window. - 0x2 : Threshold values is 0x1, windows of length 3 taps and above can be selected as sampling window. - ..... - 0x7F : Threshold values is 0x1, windows of length 127 taps and above can be selected as sampling window.	0x1
23:21	R	-	Reserved	0x0
20:19	R/W	POST_CHANGE_DLY	Time taken for phase switching and stable clock output. Specifies the maximum time (in terms of cclk cycles) that the delay line can take to switch its output phase after a change in tuning_cclk_sel or autotuning_cclk_sel. Values: 0x0 (LATENCY_LT_1): Less than 1-cycle latency 0x1 (LATENCY_LT_2): Less than 2-cycle latency 0x2 (LATENCY_LT_3): Less than 3-cycle latency 0x3 (LATENCY_LT_4): Less than 4-cycle latency	0x0
18:17	R/W	PRE_CHANGE_DLY	Maximum Latency specification between cclk_tx and cclk_rx.	0x0

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Bit	Mode	Symbol	Description	Reset
			Values: 0x0 (LATENCY_LT_1): Less than 1-cycle latency 0x1 (LATENCY_LT_2): Less than 2-cycle latency 0x2 (LATENCY_LT_3): Less than 3-cycle latency 0x3 (LATENCY_LT_4): Less than 4-cycle latency	
16	R/W	TUNE_CLK_STOP_EN	Clock stopping control for Tuning and auto-tuning circuit. When enabled, clock gate control output of emmc IP (clk2card_on) is pulled low before changing phase select codes on tuning_cclk_sel and autotuning_cclk_sel. This effectively stops the Device/Card clock, cclk_rx and also drift_cclk_rx. Changing phase code when clocks are stopped ensures glitch free phase switching. Set this bit to 0 if the PHY or delayline can guarantee glitch free switching. Values: 0x1 (ENABLE_CLK_STOPPING): Clocks stopped during phase code change 0x0 (DISABLE_CLK_STOPPING): Clocks not stopped. PHY ensures glitch free phase switching.	0x0
15:12	R	-	Reserved	0x0
11:8	R	-	Reserved	0x0
7:5	R	-	Reserved	0x0
4	R/W	SW_TUNE_EN	This fields enables software-managed tuning flow. Values: 0x1 (SW_TUNING_ENABLE): Software-managed tuning enabled. AT_STAT_R.CENTER_PH_CODE Field is now writable. 0x0 (SW_TUNING_DISABLE): Software-managed tuning disabled.	0x0
3	R/W	RPT_TUNE_ERR	Framing errors are not generated when executing tuning. This debug bit allows users to report these errors. Values: 0x1 (DEBUG_ERRORS): Debug mode for reporting framing errors 0x0 (ERRORS_DISABLED): Default mode where as per SD-HCI no errors are reported.	0x0
2	R/W	SWIN_TH_EN	Sampling window Threshold enable Selects the tuning mode Field should be programmed only when SAMPLE_CLK_SEL is 0 Values: 0x1 (THRESHOLD_MODE): Tuning engine selects the first complete sampling window that meets the threshold set by SWIN_TH_VAL field 0x0 (LARGEST_WIN_MODE): Tuning engine sweeps all taps and settles at the largest window	0x1
1:0	R	-	Reserved	0x0

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Table 970: EMMC_AT_STAT_R_REG (0x30058544)

Bit	Mode	Symbol	Description	Reset
31:24	R	-	Reserved	0x0
23:16	R	L_EDGE_PH_CODE	Left Edge Phase code. Reading this field returns the phase code value used by Auto-tuning engine to sample data on Left edge of sampling window.	0x0
15:8	R	R_EDGE_PH_CODE	Right Edge Phase code. Reading this field returns the phase code value used by Auto-tuning engine to sample data on Right edge of sampling window.	0x0
7:0	R/W	CENTER_PH_CODE	Centered Phase code. Reading this field returns the current value on tuning_cclk_sel output. Setting AT_CTRL_R.SW_TUNE_EN enables software to write to this field and its contents are reflected on tuning_cclk_sel.	0x6

Table 971: EMMC_EMBEDDED_CTRL_R_REG (0x30058F6C)

Bit	Mode	Symbol	Description	Reset
31	R	-	Reserved	0x0
30:24	R/W	BACK_END_PWR_CTRL	Back-End Power Control (SD Mode) Each bit of this field controls back-end power supply for an embedded device. - 0 : Back-End Power is off - 1 : Back-End Power is supplied D24 : Back-End Power for Device 1 D25 : Back-End Power for Device 2 D26 : Back-End Power for Device 3 D27 : Back-End Power for Device 4 D28 : Back-End Power for Device 5 D29 : Back-End Power for Device 6 D30 : Back-End Power for Device 7	0x0
23	R	-	Reserved	0x0
22:20	R/W	INT_PIN_SEL	Interrupt Pin Select These bits enable the interrupt pin inputs.	0x0

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Bit	Mode	Symbol	Description	Reset
			- 000 : Interrupts (INT_A,INT_B,INT_C) are disabled - xx1 : INT_A is enabled - x1x : INT_B is enabled - 1xx : INT_C is enabled	
19	R	-	Reserved	0x0
18:16	R/W	CLK_PIN_SEL	Clock Pin Select (SD Mode) This bit is selected by one of clock pin outputs. - 0x0 : Clock pins are disabled - 0x1 : CLK[1] is selected - 0x2 : CLK[2] is selected - . . - . . - . . - 0x7 : CLK[7] is selected	0x0
15	R	-	Reserved	0x0
14:8	R	BUS_WIDTH_PRESET	Bus Width Preset (SD Mode) Each bit of this field specifies the bus width for each embedded device. The shared bus supports mixing of 4-bit and 8-bit bus width devices. - D08 : Bus Width Preset for Device 1 - D09 : Bus Width Preset for Device 2 - D10 : Bus Width Preset for Device 3 - D11 : Bus Width Preset for Device 4 - D12 : Bus Width Preset for Device 5 - D13 : Bus Width Preset for Device 6 - D14 : Bus Width Preset for Device 7 Function of each bit is defined as follows: - 0 : 4-bit bus width mode - 1 : 8-bit bus width mode	0x0
7:6	R	-	Reserved	0x0
5:4	R	NUM_INT_PIN	Number of Interrupt Input Pins This field indicates support of interrupt input pins for an embedded system.	0x0
3	R	-	Reserved	0x0
2:0	R	NUM_CLK_PIN	Number of Clock Pins (SD Mode) This field indicates support of clock pins to select one of devices for shared bus system. Up to 7 clock pins can be supported. - 0x0 : Shared bus is not supported	0x0

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Bit	Mode	Symbol	Description	Reset
			- 0x1 : 1 SDCLK is supported - 0x2 - 2 SDCLK is supported - . . - . . - . . - 0x7 : 7 SDCLK is supported	

44.21 OTP Controller Registers

Table 972: Register map OTPC

Address	Register	Description
0x30070000	OTPC_MODE_REG	Mode register
0x30070004	OTPC_STAT_REG	Status register
0x30070008	OTPC_PADDR_REG	The address of the word that will be programmed, when the PROG mode is used.
0x3007000C	OTPC_PWORD_REG	The 32-bit word that will be programmed, when the PROG mode is used.
0x30070010	OTPC_TIM1_REG	Various timing parameters of the OTP cell.
0x30070014	OTPC_TIM2_REG	Various timing parameters of the OTP cell.

Table 973: OTPC_MODE_REG (0x30070000)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:6	R/W	OTPC_MODE_PRG_SEL	Defines the part of the OTP cell that is programmed by the controller during the PROG mode, for each program request that is applied. 0x0 : Both normal and redundancy arrays are programmed. This is the normal way of programming. 0x1 : Only the normal array is programmed. 0x2 : Only the redundancy array is programmed. 0x3 : Reserved The value of this configuration field can be modified only when the controller is in an inactive mode (DSTBY or STBY). The setting will take effect when will be enabled again the PROG mode.	0x0
5	R/W	OTPC_MODE_HT_MARG_EN	Defines the temperature condition under which is performed a margin read. It affects only the initial margin read (RINI mode) and the programming verification margin read (PVFY). 0 : Regular temperature condition (less than 85°C) 1 : High temperature condition (85°C or more) The value of this configuration field can be modified only when the controller is in an inactive	0x0

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Bit	Mode	Symbol	Description	Reset
			mode (DSTBY or STBY). The selection will take effect at the next PVFY or RINI mode that will be enabled. The READ mode is not affected by the setting of this configuration bit.	
4	R/W	OTPC_MODE_USE_TST_ROW	Selects the memory area of the OTP cell that will be used. 0 - Uses the main memory area of the OTP cell 1 - Uses the test row of the OTP cell The value of this configuration field can be modified only when the controller is in an inactive mode (DSTBY or STBY). The selection will take effect at the next programming or reading mode that will be enabled.	0x0
3	-	-	Reserved	0x0
2:0	R/W	OTPC_MODE_MODE	Defines the mode of operation of the OTPC controller. The encoding of the modes is as follows: 0x0: DSTBY. The OTP memory is in deep standby mode (power supply ON and internal LDO OFF). 0x1: STBY. The OTP memory is powered (power supply ON and internal LDO ON, but is not selected). 0x2: READ. The OTP memory is in the normal read mode. 0x3: PROG. The OTP memory is in programming mode. 0x4: PVFY. The OTP memory is in programming verification mode (margin read after programming). 0x5: RINI. The OTP memory is in initial read mode (initial margin read). 0x6 - 0x7: Reserved Whenever the OTPC_MODE_REG[MODE] is changing, the status bit OTPC_STAT_REG[OTPC_STAT_MRDY] gets the value zero. The new mode will be ready for use when the OTPC_STAT_MRDY become again 1. During the mode transition the OTPC_MODE_REG[MODE] become read only. Do not try to use or change any function of the controller until the OTPC_STAT_MRDY bit to become equal to 1.	0x0

Table 974: OTPC_STAT_REG (0x30070004)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	0x0
2	R	OTPC_STAT_MRDY	Indicates the progress of the transition from a mode of operation to a new mode of operation. 0 : There is a transition in progress in a new mode of operation . Wait until the transition to be completed.	0x1

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Bit	Mode	Symbol	Description	Reset
			1 : The transition to the new mode of operation has been completed. The function that has been enabled by the new mode can be used. A new mode can be applied. This status bit gets the value zero every time where the OTPC_MODE_REG[MODE] is changing. Do not try to use or change any function of the controller until this status bit to become equal to 1.	
1	R	OTPC_STAT_PBUF_EMPTY	Indicates the status of the programming buffer (PBUF). 0 : The PBUF contains the address and the data of a programming request. The OTPC_PADDR_REG and the OTPC_PWORD_REG should not be written as long as this status bit is zero. 1 : The PBUF is empty and a new programming request can be registered in the PBUF by using the OTPC_PADDR_REG and the OTPC_PWORD_REG registers. This status bit gets the value zero every time where a programming is triggered by the OTPC_PADDR_REG (only if the PROG mode is active).	0x1
0	R	OTPC_STAT_PRDY	Indicates the state of the programming process. 0: The controller is busy. A programming is in progress. 1: The logic which performs programming is idle.	0x1

Table 975: OTPC_PADDR_REG (0x30070008)

Bit	Mode	Symbol	Description	Reset
31:10	-	-	Reserved	0x0
9:0	R/W	OTPC_PADDR	The OTPC_PADDR_REG and the OTPC_PWORD_REG consist the PBUF buffer that keeps the information that will be programmed in the OTP, by using the PROG mode. The PBUF holds the address (OTPC_PADDR_REG) and the data (OTPC_PWORD_REG) of each of the programming requests that are applied in the OTP memory. The OTPC_PADDR_REG refers to a word address. The OTPC_PADDR_REG has to be writen after the OTP_PWORD_REG and only if the OTPC_STAT_REG[OTPC_STAT_PBUF_EMPTY] =1. The register is read only for as long the PBUF is not empty (OTPC_STAT_REG[OTPC_STAT_PBUF_EMPTY]=0). A writting to the OTPC_PADDR_REG triggers the controller to start the programming procedure (only if the PROG mode is active).	0x0

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Table 976: OTPC_PWORD_REG (0x3007000C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	OTPC_PWORD	The OTPC_PADDR_REG and the OTPC_PWORD_REG consist the PBUF buffer that keeps the information that will be programmed in the OTP memory, by using the PROG mode. The PBUF holds the address (OTPC_PADDR_REG) and the data (OTPC_PWORD_REG) of each of the programming requests that are applied in the OTP memory. The OTP_PWORD_REG must be written before the OTPC_PADDR_REG and only if OTPC_STAT_REG[OTPC_STAT_PBUF_EMPTY] = 1. The register is read only for as long the PBUF is not empty (OTPC_STAT_REG[OTPC_STAT_PBUF_EMPTY]=0).	0x0

Table 977: OTPC_TIM1_REG (0x30070010)

Bit	Mode	Symbol	Description	Reset
31	-	-	Reserved	0x0
30:24	R/W	OTPC_TIM1_US_T_CSP	The number of microseconds (minus one) that are required after the selection of the OTP memory, until to be ready for programming. It must be: - at least 10 µs - no more than 100 µs	0x9
23:20	R/W	OTPC_TIM1_US_T_CS	The number of microseconds (minus one) that are required after the selection of the OTP memory, until to be ready for any kind of read. It must be at least 10 µs.	0x9
19:16	R/W	OTPC_TIM1_US_T_PL	The number of microseconds (minus one) that are required until to be enabled the LDO of the OTP. It must be at least 10 µs.	0x9
15:12	R/W	OTPC_TIM1_CC_T_RD	Defines the number of hclk_c clock periods that give a time interval at least higher than 120 ns. The calculation of the time interval is performed like this : 2 * (OTPC_TIM1_CC_T_RD + 1) * hclk_clock_period > 120 ns. This timing parameter refers to the access time of the OTP memory.	0x2
11	-	-	Reserved	0x0
10:8	R/W	OTPC_TIM1_CC_T_20NS	The number of hclk_c clock periods (minus one) that give a time interval that is at least higher than 20 ns.	0x0
7:0	R/W	OTPC_TIM1_CC_T_1US	The number of hclk_c clock periods (minus one) that give a time interval equal to 1 µs. This setting affects all the timing parameters that refer to microseconds, due to that defines the correspondence of a microsecond to a number of hclk_c clock cycles.	0x27

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Table 978: OTPC_TIM2_REG (0x30070014)

Bit	Mode	Symbol	Description	Reset
31	R/W	OTPC_TIM2_US_ADD_CC_EN	Adds an additional hclk_c clock cycle at all the time intervals that count in microseconds. 0 : The extra hclk_c clock cycle is not applied 1 : The extra hclk_c clock cycle is applied	0x1
30:29	R/W	OTPC_TIM2_US_T_SAS	The number of microseconds (minus one) that are required after the exit from the deep sleep standby mode and before to become ready to enter in an active mode (reading or programming). It must be at least 2 µs.	0x1
28:24	R/W	OTPC_TIM2_US_T_PPH	The number of microseconds (minus one) that are required after the last programming pulse and before to be disabled the programming mode in the OTP memory. It must be: - at least 5 µs - no more than 20 µs	0x4
23:21	R/W	OTPC_TIM2_US_T_VDS	The number of microseconds (minus one) that are required after the enabling of the power supply of the OTP memory and before to become ready for the enabling of the internal LDO. It must be at least 1 µs.	0x0
20:16	R/W	OTPC_TIM2_US_T_PPS	The number of microseconds (minus one) that are required after the enabling of the programming in the OTP memory and before to be applied the first programming pulse. It must be: - at least 5 µs - no more than 20 µs	0x4
15	-	-	Reserved	0x0
14:8	R/W	OTPC_TIM2_US_T_PPR	The number of microseconds (minus one) for recovery after a programming sequence. It must be: - at least 5 µs - no more than 100 µs	0x4
7:5	R/W	OTPC_TIM2_US_T_PWI	The number of microseconds (minus one) between two consecutive programming pulses. It must be: - at least 1 µs - no more than 5 µs	0x0
4:0	R/W	OTPC_TIM2_US_T_PW	The number of microseconds (minus one) that lasts the programming of each bit. It must be : - at least 10 µs - no more than 20 µs	0x9

44.22 Audio Unit Registers

Table 979: Register map PCM1

Address	Register	Description
0x50030300	PCM1_CTRL_REG	PCM1 Control register

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Address	Register	Description
0x50030304	PCM1_IN1_REG	PCM1 data in 1
0x50030308	PCM1_IN2_REG	PCM1 data in 2
0x5003030C	PCM1_OUT1_REG	PCM1 data out 1
0x50030310	PCM1_OUT2_REG	PCM1 data out 2

Table 980: PCM1_CTRL_REG (0x50030300)

Bit	Mode	Symbol	Description	Reset
31:20	R/W	PCM_FSC_DIV	PCM Framesync divider, Values 7-0xFFF. To divide by N, write N-1. (Minimum value N-1=7 for 8 bits PCM_FSC) Note if PCM_CLK_BIT=1, N must always be even	0x0
19:17	-	-	Reserved	0x0
16	R/W	PCM_FSC_EDGE	0: shift channels 1, 2, 3, 4, 5, 6, 7, 8 after PCM_FSC edge 1: shift channels 1, 2, 3, 4 after PCM_FSC edge shift channels 5, 6, 7, 8 after opposite PCM_FSC edge	0x0
15:11	R/W	PCM_CH_DEL	Channel delay in multiples of 8 bits	0x0
10	R/W	PCM_CLK_BIT	0:One clock cycle per data bit 1:Two cloc cycles per data bit	0x0
9	R/W	PCM_FSCINV	0: PCM FSC 1: PCM FSC inverted	0x0
8	R/W	PCM_CLKINV	0:PCM CLK 1:PCM CLK inverted	0x0
7	R/W	PCM_PPOD	0:PCM DO push pull 1:PCM DO open drain	0x0
6	R/W	PCM_FSCDEL	0:PCM FSC starts one cycle before MSB bit 1:PCM FSC starts at the same time as MSB bit	0x0
5:2	R/W	PCM_FSCLEN	0:PCM FSC length equal to 1 data bit N:PCM FSC length equal to N*8	0x0
1	R/W	PCM_MASTER	0:PCM interface in slave mode 1:PCM interface in master mode	0x0
0	R/W	PCM_EN	0:PCM interface disabled 1:PCM interface enabled	0x0

Table 981: PCM1_IN1_REG (0x50030304)

Bit	Mode	Symbol	Description	Reset
31:0	R	PCM_IN	PCM1_IN1 bits 31-0	0x0

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Table 982: PCM1_IN2_REG (0x50030308)

Bit	Mode	Symbol	Description	Reset
31:0	R	PCM_IN	PCM1_IN2 bits 31-0	0x0

Table 983: PCM1_OUT1_REG (0x5003030C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PCM_OUT	PCM1_OUT1 bits 31-0	0xFFFF FFFF

Table 984: PCM1_OUT2_REG (0x50030310)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PCM_OUT	PCM1_OUT2 bits 31-0	0xFFFF FFFF

Table 985: Register map SRC

Address	Register	Description
0x50030100	SRC1_CTRL_REG	SRC control register
0x50030104	SRC1_IN_FS_REG	SRC Sample input rate
0x50030108	SRC1_OUT_FS_REG	SRC Sample output rate
0x5003010C	SRC1_IN1_REG	SRC data in 1
0x50030110	SRC1_IN2_REG	SRC data in 2
0x50030114	SRC1_OUT1_REG	SRC data out 1
0x50030118	SRC1_OUT2_REG	SRC data out 2
0x5003011C	SRC1_MUX_REG	SRC mux register
0x50030120	SRC1_COEF10_SET1_REG	SRC coefficient 1,0 set 1
0x50030124	SRC1_COEF32_SET1_REG	SRC coefficient 3,2 set 1
0x50030128	SRC1_COEF54_SET1_REG	SRC coefficient 5,4 set 1
0x5003012C	SRC1_COEF76_SET1_REG	SRC coefficient 7,6 set 1
0x50030130	SRC1_COEF98_SET1_REG	SRC coefficient 9,8 set 1
0x50030134	SRC1_COEF0A_SET1_REG	SRC coefficient 10 set 1
0x50030200	SRC2_CTRL_REG	SRC control register
0x50030204	SRC2_IN_FS_REG	SRC Sample input rate
0x50030208	SRC2_OUT_FS_REG	SRC Sample output rate
0x5003020C	SRC2_IN1_REG	SRC data in 1

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Address	Register	Description
0x50030210	SRC2_IN2_REG	SRC data in 2
0x50030214	SRC2_OUT1_REG	SRC data out 1
0x50030218	SRC2_OUT2_REG	SRC data out 2
0x5003021C	SRC2_MUX_REG	SRC mux register
0x50030220	SRC2_COEF10_SET1_REG	SRC coefficient 1,0 set 1
0x50030224	SRC2_COEF32_SET1_REG	SRC coefficient 3,2 set 1
0x50030228	SRC2_COEF54_SET1_REG	SRC coefficient 5,4 set 1
0x5003022C	SRC2_COEF76_SET1_REG	SRC coefficient 7,6 set 1
0x50030230	SRC2_COEF98_SET1_REG	SRC coefficient 9,8 set 1
0x50030234	SRC2_COEF0A_SET1_REG	SRC coefficient 10 set 1

Table 986: SRC1_CTRL_REG (0x50030100)

Bit	Mode	Symbol	Description	Reset
31:30	R/W	SRC_PDM_DO_DEL	PDM_DO output delay line (typical) 0: no delay 1: 8 ns 2: 12 ns 3: 16 ns	0
29:28	R/W	SRC_PDM_MODE	PDM Output mode selection on PDM_DO1 00: No output 01: Right channel (data from SRC1_IN_REG) 10: Left channel (data from SRC2_IN_REG) 11: Left and Right channel	0
27:26	R/W	SRC_PDM_DI_DEL	PDM_DI input delay line (typical) 0: no delay 1: 4 ns 2: 8 ns 3: 12 ns	0
25	R0/W	SRC_OUT_FLOWCLR	Writing a 1 clears the SRC1_OUT Overflow/underflow bits 23-22. No more over/underflow indications while bit is 1. Keep 1 until the over/under flow bit is cleared	0
24	W	SRC_IN_FLOWCLR	Writing a 1 clears the SRC1_IN Overflow/underflow bits 21-20. No more over/underflow indications while bit is 1. Keep 1 until the over/under flow bit is cleared	0
23	R	SRC_OUT_UNFLOW	1 = SRC1_OUT Underflow occurred	0
22	R	SRC_OUT_OVFLOW	1 = SRC1_OUT Overflow occurred	0

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Bit	Mode	Symbol	Description	Reset
21	R	SRC_IN_UNFLOW	1 = SRC1_IN Underflow occurred	0
20	R	SRC_IN_OVFLOW	1 = SRC1_IN Overflow occurred	0
19	R0/W	SRC_RESYNC	1 = SRC will restart synchronisation	0
18	R	SRC_OUT_OK	SRC1_OUT Status 0: acquisition in progress 1: acquisition ready (In manual mode this bit is always 1)	0
17:16	R/W	SRC_OUT_US	SRC1_OUT UpSampling IIR filters setting 00: for sample rates up-to 48kHz 01: for sample rates of 96kHz 10: reserved 11: for sample rates of 192kHz	0
15	-	-	Reserved	0
14	R/W	SRC_OUT_CAL_BYPASS	SRC1_OUT1 upsampiling filter bypass 0:Do not bypass 1:Bypass filter	0
13	R/W	SRC_OUT_AMODE	SRC1_OUT1 Automatic Conversion mode 0:Manual mode 1:Automatic mode	0
12	R/W	SRC_PDM_OUT_INV	Swap the left and the right output PDM channel	0
11	R/W	SRC_FIFO_DIRECTION	0 = SRC fifo is used to store samples from memory to SRC 1 = SRC fifo is used to store sample from SRC to memory	0x0
10	R/W	SRC_FIFO_ENABLE	0 = fifo disable. On each src request, one sample is serviced 1 = fifo enable. Fifo is used to store samples from / to src SRC supports only DMA burst size 4 when fifo is enable else no burst	0x0
9	R/W	SRC_OUT_DSD_MODE	0 = SRC1 OUT PDM mode 1 = SRC1 OUT DSD mode	0x0
8	R/W	SRC_IN_DSD_MODE	0: SRC1 IN PDM mode 1: SRC1 IN DSD mode	0x0
7	R/W	SRC_DITHER_DISABLE	Dithering feature 0: Enable 1: Disable	0
6	R	SRC_IN_OK	SRC1_IN status 0: Acquisition in progress 1: Acquisition ready	0
5:4	R/W	SRC_IN_DS	SRC1_IN UpSampling IIR filters setting 00: for sample rates up-to 48kHz 01: for sample rates of 96kHz 10: reserved 11: for sample rates of 192kHz	0

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Bit	Mode	Symbol	Description	Reset
3	R/W	SRC_PDM_IN_INV	Swap the left and the right input PDM channel	0
2	R/W	SRC_IN_CAL_BYPASS	SRC1_IN upsampeling filter bypass 0: Do not bypass 1: Bypass filter	0
1	R/W	SRC_IN_AMODE	SRC1_IN Automatic conversion mode 0: Manual mode 1: Automatic mode	0
0	R/W	SRC_EN	SRC1_IN and SRC1_OUT enable 0: disabled 1: enabled	0

Table 987: SRC1_IN_FS_REG (0x50030104)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0
23:0	R/W	SRC_IN_FS	SRC_IN Sample rate SRC_IN_FS = SRC_DIV*4096*Sample_rate/100 Sample_rate upper limit is 192 kHz. For 96 kHz and 192 kHz SRC_CTRLx_REG[SRC_IN_DS] must be set as shown below: (for SRC_DIV=1) Sample_rate SRC_IN_FS SRC_IN_DS Audio bandwidth 8000 Hz 0x050000 0 4000 Hz 11025 Hz 0x06E400 0 5512 Hz 16000 Hz 0x0A0000 0 8000 Hz 22050 Hz 0x0DC800 0 11025 Hz 32000 Hz 0x140000 0 16000 Hz 44100 Hz 0x1B9000 0 22050 Hz 48000 Hz 0x1E0000 0 24000 Hz 96000 Hz 0x1E0000 1 24000 Hz 192000 Hz 0x1E0000 3 24000 Hz In manual SRC mode, SRC_IN_FS can be set and adjusted to the desired sample rate at any time. In automatic mode the SRC returns the final sample rate as soon as SRC_IN_OK. Note that SRC_DS is not calculated in automatic mode and must be set manually automatic mode with Sample_rate of 96 and 192 kHz.	0

Table 988: SRC1_OUT_FS_REG (0x50030108)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0
23:0	R/W	SRC_OUT_FS	SRC_OUT Sample rate	0

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Bit	Mode	Symbol	Description	Reset
			SRC_OUT_FS = SRC_DIV*4096*Sample_rate/100 Sample_rate upper limit is 192 kHz. For 96 kHz and 192 kHz SRC_CTRLx_REG[SRC_DS] must be set as shown below: (for SRC_DIV=1) Sample_rate SRC_OUT_FS SRC_OUT_DS Audio bandwidth 8000 Hz 0x050000 0 4000 Hz 11025 Hz 0x06E400 0 5512 Hz 16000 Hz 0x0A0000 0 8000 Hz 22050 Hz 0x0DC800 0 11025 Hz 32000 Hz 0x140000 0 16000 Hz 44100 Hz 0x1B9000 0 22050 Hz 48000 Hz 0x1E0000 0 24000 Hz 96000 Hz 0x1E0000 1 24000 Hz 192000 Hz 0x1E0000 3 24000 Hz In manual SRC mode, SRC_OUT_FS can be set and adjusted to the desired sample rate at any time. In automatic mode the SRC returns the final sample rate as soon as SRC_OUT_OK. Note that SRC_DS is not calculated in automatic mode and must be set manually automatic mode with Sample_rate of 96 and 192k Hz.	

Table 989: SRC1_IN1_REG (0x5003010C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	SRC_IN	SRC1_IN1	0

Table 990: SRC1_IN2_REG (0x50030110)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	SRC_IN	SRC1_IN2	0

Table 991: SRC1_OUT1_REG (0x50030114)

Bit	Mode	Symbol	Description	Reset
31:0	R	SRC_OUT	SRC1_OUT1	0

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Table 992: SRC1_OUT2_REG (0x50030118)

Bit	Mode	Symbol	Description	Reset
31:0	R	SRC_OUT	SRC1_OUT2	0

Table 993: SRC1_MUX_REG (0x5003011C)

Bit	Mode	Symbol	Description	Reset
6	R/W	PDM1_MUX_IN	PDM1 input mux 0 = SRC1_MUX_IN 1 = PDM input	0x0
5:3	R/W	PCM1_MUX_IN	PCM1 input mux 0 = off 1 = SRC1 output 2 = PCM output registers 3 = SRC2 output	0x0
2:0	R/W	SRC1_MUX_IN	SRC1 input mux 0 = off 1 = PCM output 2 = SRC1 input registers 3 = SDADC output	0x0

Table 994: SRC1_COEF10_SET1_REG (0x50030120)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	SRC_COEF1	Coefficient 1	0x7A20
15:0	R/W	SRC_COEF0	Coefficient 0	0x8EC4

Table 995: SRC1_COEF32_SET1_REG (0x50030124)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	SRC_COEF3	Coefficient 3	0x70FD
15:0	R/W	SRC_COEF2	Coefficient 2	0x8936

Table 996: SRC1_COEF54_SET1_REG (0x50030128)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	SRC_COEF5	Coefficient 5	0x9758
15:0	R/W	SRC_COEF4	Coefficient 4	0xB686

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Table 997: SRC1_COEF76_SET1_REG (0x5003012C)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	SRC_COEF7	Coefficient 7	0x89C4
15:0	R/W	SRC_COEF6	Coefficient 6	0x7DF5

Table 998: SRC1_COEF98_SET1_REG (0x50030130)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	SRC_COEF9	Coefficient 9	0x8F18
15:0	R/W	SRC_COEF8	Coefficient 8	0x7771

Table 999: SRC1_COEF0A_SET1_REG (0x50030134)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	SRC_COEF10	Coefficient 10	0x497D

Table 1000: SRC2_CTRL_REG (0x50030200)

Bit	Mode	Symbol	Description	Reset
31:30	R/W	-	Reserved	0
29:28	R/W	SRC_PDM_MODE	PDM Output mode selection on PDM_DO1 00: No output 01: Right channel (data from SRC1_IN_REG) 10: Left channel (data from SRC2_IN_REG) 11: Left and Right channel	0
27:26	R/W	-	Reserved	0
25	R0/W	SRC_OUT_FLOWCLR	Writing a 1 clears the SRC1_OUT Overflow/underflow bits 23-22. No more over/underflow indications while bit is 1. Keep 1 until the over/under flow bit is cleared	0
24	W	SRC_IN_FLOWCLR	Writing a 1 clears the SRC1_IN Overflow/underflow bits 21-20. No more over/underflow indications while bit is 1. Keep 1 until the over/under flow bit is cleared	0
23	R	SRC_OUT_UNFLOW	1 = SRC1_OUT Underflow occurred	0
22	R	SRC_OUT_OVFLOW	1 = SRC1_OUT Overflow occurred	0
21	R	SRC_IN_UNFLOW	1 = SRC1_IN Underflow occurred	0
20	R	SRC_IN_OVFLOW	1 = SRC1_IN Overflow occurred	0
19	R0/W	SRC_RESYNC	1 = SRC will restart synchronisation	0
18	R	SRC_OUT_OK	SRC1_OUT Status 0: acquisition in progress	0

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Bit	Mode	Symbol	Description	Reset
			1: acquisition ready (In manual mode this bit is always 1)	
17:16	R/W	SRC_OUT_US	SRC1_OUT UpSampling IIR filters setting 00: for sample rates up-to 48 kHz 01: for sample rates of 96 kHz 10: reserved 11: for sample rates of 192 kHz	0
15	-	-	Reserved	0
14	R/W	SRC_OUT_CAL_BYPASS	SRC1_OUT1 upsampiling filter bypass 0:Do not bypass 1:Bypass filter	0
13	R/W	SRC_OUT_AMODE	SRC1_OUT1 Automatic Conversion mode 0:Manual mode 1:Automatic mode	0
12	R/W	SRC_PDM_OUT_INV	Swap the left and the right output PDM channel	0
11	R/W	SRC_FIFO_DIRECTION	0 = SRC fifo is used to store samples from memory to SRC 1 = SRC fifo is used to store sample from SRC to memory	0x0
10	R/W	SRC_FIFO_ENABLE	0 = fifo disable. On each src request, one sample is serviced 1 = fifo enable. Fifo is used to store samples from/to src SRC supports only DMA burst size 4 when fifo is enable else no burst	0x0
9	R/W	SRC_OUT_DSD_MODE	0 = SRC1 OUT PDM mode 1 = SRC1 OUT DSD mode	0x0
8	R/W	SRC_IN_DSD_MODE	0: SRC1 IN PDM mode 1: SRC1 IN DSD mode	0x0
7	R/W	SRC_DITHER_DISABLE	Dithering feature 0: Enable 1: Disable	0
6	R	SRC_IN_OK	SRC1_IN status 0: Acquisition in progress 1: Acquisition ready	0
5:4	R/W	SRC_IN_DS	SRC1_IN UpSampling IIR filters setting 00: for sample rates up-to 48 kHz 01: for sample rates of 96 kHz 10: reserved 11: for sample rates of 192 kHz	0
3	R/W	SRC_PDM_IN_INV	Swap the left and the right input PDM channel	0
2	R/W	SRC_IN_CAL_BYPASS	SRC1_IN upsampeling filter bypass 0: Do not bypass 1: Bypass filter	0
1	R/W	SRC_IN_AMODE	SRC1_IN Automatic conversion mode 0: Manual mode	0

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Bit	Mode	Symbol	Description	Reset
			1: Automatic mode	
0	R/W	SRC_EN	SRC1_IN and SRC1_OUT enable 0: disabled 1: enabled	0

Table 1001: SRC2_IN_FS_REG (0x50030204)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0

23:0	R/W	SRC_IN_FS	SRC_IN Sample rate
			SRC_IN_FS = SRC_DIV*4096*Sample_rate/100
			Sample_rate upper limit is 192 kHz. For 96 kHz and 192 kHz SRC_CTRLx_REG[SRC_IN_DS] must be set as shown below:
			(for SRC_DIV=1)
			`Sample_rate SRC_IN_FS SRC_IN_DS Audio bandwidth`
			`8000 Hz 0x050000 0 4000 Hz`
			`11025 Hz 0x06E400 0 5512 Hz`
			`16000 Hz 0x0A0000 0 8000 Hz`
			`22050 Hz 0x0DC800 0 11025 Hz`
			`32000 Hz 0x140000 0 16000 Hz`
			`44100 Hz 0x1B9000 0 22050 Hz`
			`48000 Hz 0x1E0000 0 24000 Hz`
			`96000 Hz 0x1E0000 1 24000 Hz`
			`192000 Hz 0x1E0000 3 24000 Hz`
			In manual SRC mode, SRC_IN_FS can be set and adjusted to the desired sample rate at any time.
			In automatic mode the SRC returns the final sample rate as soon as SRC_IN_OK. Note that SRC_DS is not calculated in automatic mode and must be set manually automatic mode with Sample_rate of 96 and 192 kHz.
				0

Table 1002: SRC2_OUT_FS_REG (0x50030208)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0
23:0	R/W	SRC_OUT_FS	SRC_OUT Sample rate SRC_OUT_FS = SRC_DIV*4096*Sample_rate/100 Sample_rate upper limit is 192 kHz. For 96 kHz and 192 kHz SRC_CTRLx_REG[SRC_DS] must be set as shown below: (for SRC_DIV=1) `Sample_rate SRC_OUT_FS SRC_OUT_DS Audio bandwidth`	0

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Bit	Mode	Symbol	Description	Reset
			8000 Hz 0x050000 0 4000 Hz 11025 Hz 0x06E400 0 5512 Hz 16000 Hz 0x0A0000 0 8000 Hz 22050 Hz 0x0DC800 0 11025 Hz 32000 Hz 0x140000 0 16000 Hz 44100 Hz 0x1B9000 0 22050 Hz 48000 Hz 0x1E0000 0 24000 Hz 96000 Hz 0x1E0000 1 24000 Hz 192000 Hz 0x1E0000 3 24000 Hz In manual SRC mode, SRC_OUT_FS can be set and adjusted to the desired sample rate at any time. In automatic mode the SRC returns the final sample rate as soon as SRC_OUT_OK. Note that SRC_DS is not calculated in automatic mode and must be set manually automatic mode with Sample_rate of 96 and 192k Hz.	

Table 1003: SRC2_IN1_REG (0x5003020C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	SRC_IN	SRC1_IN1	0

Table 1004: SRC2_IN2_REG (0x50030210)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	SRC_IN	SRC1_IN2	0

Table 1005: SRC2_OUT1_REG (0x50030214)

Bit	Mode	Symbol	Description	Reset
31:0	R	SRC_OUT	SRC1_OUT1	0

Table 1006: SRC2_OUT2_REG (0x50030218)

Bit	Mode	Symbol	Description	Reset
31:0	R	SRC_OUT	SRC1_OUT2	0

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Table 1007: SRC2_MUX_REG (0x5003021C)

Bit	Mode	Symbol	Description	Reset
6	R/W	PDM1_MUX_IN	PDM1 input mux 0 = SRC2_MUX_IN 1 = PDM input	0x0
5:3	R/W	PDM_MUX_OUT	PDM output mux 0 = SRC1 PDM output 1 = SRC2 PDM output 2..7 = Reserved	0x0
2:0	R/W	SRC2_MUX_IN	SRC1 input mux 0 = off 1 = PCM output 2 = SRC2 input registers 3 = SDADC output	0x0

Table 1008: SRC2_COEF10_SET1_REG (0x50030220)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	SRC_COEF1	Coefficient 1	0x7A20
15:0	R/W	SRC_COEF0	Coefficient 0	0x8EC4

Table 1009: SRC2_COEF32_SET1_REG (0x50030224)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	SRC_COEF3	Coefficient 3	0x70FD
15:0	R/W	SRC_COEF2	Coefficient 2	0x8936

Table 1010: SRC2_COEF54_SET1_REG (0x50030228)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	SRC_COEF5	Coefficient 5	0x9758
15:0	R/W	SRC_COEF4	Coefficient 4	0xB686

Table 1011: SRC2_COEF76_SET1_REG (0x5003022C)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	SRC_COEF7	Coefficient 7	0x89C4
15:0	R/W	SRC_COEF6	Coefficient 6	0x7DF5

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Table 1012: SRC2_COEF98_SET1_REG (0x50030230)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	SRC_COEF9	Coefficient 9	0x8F18
15:0	R/W	SRC_COEF8	Coefficient 8	0x7771

Table 1013: SRC2_COEF0A_SET1_REG (0x50030234)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	SRC_COEF10	Coefficient 10	0x497D

44.23 Power Domains Controller Registers

Table 1014: Register map PDC

Address	Register	Description
0x50000200	PDC_CTRL0_REG	PDC control register
0x50000204	PDC_CTRL1_REG	PDC control register
0x50000208	PDC_CTRL2_REG	PDC control register
0x5000020C	PDC_CTRL3_REG	PDC control register
0x50000210	PDC_CTRL4_REG	PDC control register
0x50000214	PDC_CTRL5_REG	PDC control register
0x50000218	PDC_CTRL6_REG	PDC control register
0x5000021C	PDC_CTRL7_REG	PDC control register
0x50000220	PDC_CTRL8_REG	PDC control register
0x50000224	PDC_CTRL9_REG	PDC control register
0x50000228	PDC_CTRL10_REG	PDC control register
0x5000022C	PDC_CTRL11_REG	PDC control register
0x50000230	PDC_CTRL12_REG	PDC control register
0x50000234	PDC_CTRL13_REG	PDC control register
0x50000238	PDC_CTRL14_REG	PDC control register
0x5000023C	PDC_CTRL15_REG	PDC control register
0x50000280	PDC_ACKNOWLEDGE_REG	Clear a pending PDC bit
0x50000284	PDC_PENDING_REG	Shows any pending wakup event
0x50000288	PDC_PENDING_SNC_REG	Shows any pending IRQ to SNC
0x5000028C	PDC_PENDING_CM33_REG	Shows any pending IRQ to CM33
0x50000290	PDC_PENDING_CMAC_REG	Shows any pending IRQ to CMAC
0x50000294	PDC_SET_PENDING_REG	Set a pending PDC bit

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Table 1015: PDC_CTRL0_REG (0x50000200)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	Selects which individual bit from the selected bank is used for wakeup. When TRIG_SELECT = 0x0, TRIG_ID contains the PIN id of port 0 When TRIG_SELECT = 0x1, TRIG_ID contains the PIN id of port 1 When TRIG_SELECT = 0x2, TRIG_ID contains the PIN id of port 2 When TRIG_SELECT = 0x3, TRIG_ID selects which IRQ is used from the PDC Peripheral IRQ table.. PDC Peripheral IRQ table: 0x0: Timer 0x1: Timer2 0x2: Timer3 0x3: Timer4 0x4: Timer5 0x5: Timer6 0x6: RTC Alarm/Rollover 0x7: RTC Timer 0x8: CMAC Timer OR wake up from CMAC debugger OR SYS2CMAC_IRQ 0x9: VAD 0xA: XTAL32MRDY_IRQ 0xB: RFDIAG_IRQ 0xC: VBUS Present IRQ OR JTAG present OR Debounced IO 0xD: CMAC2SYS_IRQ 0xE: SNC2SYS_IRQ 0xF: Software trigger only 0x10: GPIO P0 0x11: GPIO P1 0x12: GPIO P2 0x13: CMAC2SNC_IRQ 0x14: SNC2CMAC_IRQ	0x0

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Bit	Mode	Symbol	Description	Reset
			0x15: SYS2CMAC_IRQ 0x16: SYS2SNC_IRQ 0x17: SYS2SNC_IRQ OR CMAC2SNC_IRQ 0x18: SNC2SYS_IRQ OR CMAC2SYS_IRQ 0x9 to 0x1f: Reserved	
1:0	R/W	TRIG_SELECT	Selects which bank is used as wakeup trigger. 0b00: selects GPIO port0 through the WAKEUP block. 0b01 :selects GPIO port1 through the WAKEUP block. 0b10: selects GPIO port2 through the WAKEUP block. 0b11: selects the IRQ table as bank (See TRIG_ID)	0x0

Table 1016: PDC_CTRL1_REG (0x50000204)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

Table 1017: PDC_CTRL2_REG (0x50000208)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0

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Bit	Mode	Symbol	Description	Reset
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

Table 1018: PDC_CTRL3_REG (0x5000020C)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

Table 1019: PDC_CTRL4_REG (0x50000210)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

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Table 1020: PDC_CTRL5_REG (0x50000214)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

Table 1021: PDC_CTRL6_REG (0x50000218)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

Table 1022: PDC_CTRL7_REG (0x5000021C)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0

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Bit	Mode	Symbol	Description	Reset
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

Table 1023: PDC_CTRL8_REG (0x50000220)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

Table 1024: PDC_CTRL9_REG (0x50000224)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

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Table 1025: PDC_CTRL10_REG (0x50000228)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

Table 1026: PDC_CTRL11_REG (0x5000022C)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

Table 1027: PDC_CTRL12_REG (0x50000230)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered	0x0

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Bit	Mode	Symbol	Description	Reset
			0x3: PD_SNC is woken up and SNC is triggered	
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

Table 1028: PDC_CTRL13_REG (0x50000234)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

Table 1029: PDC_CTRL14_REG (0x50000238)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0

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Bit	Mode	Symbol	Description	Reset
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

Table 1030: PDC_CTRL15_REG (0x5000023C)

Bit	Mode	Symbol	Description	Reset
12:11	R/W	PDC_MASTER	Chooses which master is triggered when waking up 0x0: entry is disabled. 0x1: PD_SYS is woken up and CM33 is triggered 0x2: PD_RAD is woken up and CMAC is triggered 0x3: PD_SNC is woken up and SNC is triggered	0x0
10	R/W	EN_SNC	If set, enables PD_SNC. This bit is implied when PDC_MASTER=SNC	0x0
9	R/W	-	Reserved	0x0
8	R/W	EN_TMR	If set, enables PD_TMR	0x0
7	R/W	EN_XTAL	If set, the XTAL32M will be started	0x0
6:2	R/W	TRIG_ID	For description, see PDC_CTRL0_REG.TRIG_ID	0x0
1:0	R/W	TRIG_SELECT	For description, see PDC_CTRL0_REG.TRIG_SELECT	0x0

Table 1031: PDC_ACKNOWLEDGE_REG (0x50000280)

Bit	Mode	Symbol	Description	Reset
4:0	W	PDC_ACKNOWLEDGE	Writing to this field acknowledges the PDC IRQ request. The data controls which request is acknowledged	0x0

Table 1032: PDC_PENDING_REG (0x50000284)

Bit	Mode	Symbol	Description	Reset
15:0	R	PDC_PENDING	Indicates which IRQ ids are pending	0x0

Table 1033: PDC_PENDING_SNC_REG (0x50000288)

Bit	Mode	Symbol	Description	Reset
15:0	R	PDC_PENDING	Indicates which IRQ ids are pending towards the SensorNodeController	0x0

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Table 1034: PDC_PENDING_CM33_REG (0x5000028C)

Bit	Mode	Symbol	Description	Reset
15:0	R	PDC_PENDING	Indicates which IRQ ids are pending towards the CM33	0x0

Table 1035: PDC_PENDING_CMAC_REG (0x50000290)

Bit	Mode	Symbol	Description	Reset
15:0	R	PDC_PENDING	Indicates which IRQ ids are pending towards the CMAC	0x0

Table 1036: PDC_SET_PENDING_REG (0x50000294)

Bit	Mode	Symbol	Description	Reset
4:0	W	PDC_SET_PENDING	Writing to this field sets the PDC wake-up request and IRQ. The data controls which request is acknowledged	0x0

44.24 LED Controller Registers

Table 1037: Register map PWM for LEDs

Address	Register	Description
0x50010600	LEDS_PWM_CTRL_REG	LED PWM control register
0x50010604	LEDS_STATUS_REG	LEDS status register
0x50010608	LED1_PWM_CONF_REG	Defines duty cycle and load sel for LED1
0x5001060C	LED2_PWM_CONF_REG	Defines duty cycle and load sel for LED2
0x50010610	LED3_PWM_CONF_REG	Defines duty cycle and load sel for LED3
0x50010614	LEDS_DRV_CTRL_REG	LED driver control register
0x50010618	LEDS_FREQUENCY_REG	Defines the frequency of all the LEDs
0x5001061C	LED_LOAD_SEL_REG	Load sel for LEDS
0x50010620	LED_CURR_TRIM_REG	Trim values for LEDS

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Table 1038: LEDS_PWM_CTRL_REG (0x50010600)

Bit	Mode	Symbol	Description	Reset
4	R/W	PWM_LEDS_HW_PAUSE_ENABLE	When this bit is set, PWM engines 1-3 are paused when the radio enable is high	0x0
3	R/W	PWM_LEDS_SW_PAUSE	PWM engines1-3 are paused when this bit is set by SW	0x0
2	R/W	LED3_PWM_ENABLE	Enables/Disables the PWM engine	0x0
1	R/W	LED2_PWM_ENABLE	Enables/Disables the PWM engine	0x0
0	R/W	LED1_PWM_ENABLE	Enables/Disables the PWM engine	0x0

Table 1039: LEDS_STATUS_REG (0x50010604)

Bit	Mode	Symbol	Description	Reset
3	R	LED_FREQUENCY_BUSY	LEDS_FREQUENCY_REG is busy with synchronisation. Wait unti this bit is 0 before writing a new value	0x0
2	R	LED3_CONF_BUSY	LED3_CONF_REG is busy with synchronisation. Wait unti this bit is 0 before writing a new value	0x0
1	R	LED2_CONF_BUSY	LED2_CONF_REG is busy with synchronisation. Wait unti this bit is 0 before writing a new value	0x0
0	R	LED1_CONF_BUSY	LED1_CONF_REG is busy with synchronisation. Wait unti this bit is 0 before writing a new value	0x0

Table 1040: LED1_PWM_CONF_REG (0x50010608)

Bit	Mode	Symbol	Description	Reset
23:12	R/W	PWMLED_START_CYCLE	Defines the cycle at which the PWM becomes high. Setting start_cycle = stop_cycle results in 100% duty cycle	0x0
11:0	R/W	PWMLED_STOP_CYCLE	Defines the cycle at which the PWM becomes low. Setting start_cycle = stop_cycle results in 100% duty cycle	0x0

Table 1041: LED2_PWM_CONF_REG (0x5001060C)

Bit	Mode	Symbol	Description	Reset
23:12	R/W	PWMLED_START_CYCLE	Defines the cycle at which the PWM becomes high. Setting start_cycle = stop_cycle results in 100% duty cycle	0x0
11:0	R/W	PWMLED_STOP_CYCLE	Defines the cycle at which the PWM becomes low. Setting start_cycle = stop_cycle results in 100% duty cycle	0x0

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Table 1042: LED3_PWM_CONF_REG (0x50010610)

Bit	Mode	Symbol	Description	Reset
23:12	R/W	PWMLED_START_CYCLE	Defines the cycle at which the PWM becomes high. Setting start_cycle = stop_cycle results in 100% duty cycle	0x0
11:0	R/W	PWMLED_STOP_CYCLE	Defines the cycle at which the PWM becomes low. Setting start_cycle = stop_cycle results in 100% duty cycle	0x0

Table 1043: LEDS_DRV_CTRL_REG (0x50010614)

Bit	Mode	Symbol	Description	Reset
2	R/W	LED3_EN	0 = LED disabled, 1 = LED enabled	0x0
1	R/W	LED2_EN	0 = LED disabled, 1 = LED enabled	0x0
0	R/W	LED1_EN	0 = LED disabled, 1 = LED enabled	0x0

Table 1044: LEDS_FREQUENCY_REG (0x50010618)

Bit	Mode	Symbol	Description	Reset
19:12	R/W	PWM_LEDS_PRESCALE	Defines the clock prescaler that is used for the input clock for PWM LED1-3. Division factor = register value + 1 0x00: Divide by 1 0x01: Divide by 2 0x02: Divide by 3 ... ... 0xFE: Dvide by 255 0xFF: Divide by 256	0x0
11:0	R/W	PWM_LEDS_PERIOD	Defines the period of PWM signals 1-3. Period = Period constant system clock * ((PWMLED_MAX_PERIOD+1) * (PWMLED_PRESCALE+1))	0xFFF

Table 1045: LED_LOAD_SEL_REG (0x5001061C)

Bit	Mode	Symbol	Description	Reset
8:6	R/W	LED3_LOAD_SEL	Defines LED sinking current: 2.5 mA + (LED_LOAD_SEL*2.5 mA). Max = 20 mA	0x7
5:3	R/W	LED2_LOAD_SEL	Defines LEDsinking current: 2.5 mA + (LED_LOAD_SEL*2.5 mA). Max = 20 mA	0x7
2:0	R/W	LED1_LOAD_SEL	Defines LED sinking current: 2.5 mA + (LED_LOAD_SEL*2.5 mA). Max = 20 mA	0x7

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Table 1046: LED_CURR_TRIM_REG (0x50010620)

Bit	Mode	Symbol	Description	Reset
11:8	R/W	LED3_CURR_TRIM	LED current trimming	0x0
7:4	R/W	LED2_CURR_TRIM	LED current trimming	0x0
3:0	R/W	LED1_CURR_TRIM	LED current trimming	0x0

44.25 Quad SPI Controllers Registers

Table 1047: Register map QSPIC

Address	Register	Description
0x46000000	QSPIC_CTRLBUS_REG	SPI Bus control register for the Manual mode
0x46000004	QSPIC_CTRLMODE_REG	Mode control register
0x46000008	QSPIC_RECVDATA_REG	Received data for the Manual mode
0x4600000C	QSPIC_BURSTCMDA_REG	The way of reading in Auto mode (command register A)
0x46000010	QSPIC_BURSTCMDB_REG	The way of reading in Auto mode (command register B)
0x46000014	QSPIC_STATUS_REG	The status register of the QSPI controller
0x46000018	QSPIC_WRITEDATA_REG	Write data to SPI Bus for the Manual mode
0x4600001C	QSPIC_READDATA_REG	Read data from SPI Bus for the Manual mode
0x46000020	QSPIC_DUMMYDATA_REG	Send dummy clocks to SPI Bus for the Manual mode
0x46000024	QSPIC_ERASECTRL_REG	Erase control register
0x46000028	QSPIC_ERASECMDA_REG	The way of erasing in Auto mode (command register A)
0x4600002C	QSPIC_ERASECMDB_REG	The way of erasing in Auto mode (command register B)
0x46000030	QSPIC_BURSTBRK_REG	Read break sequence in Auto mode
0x46000034	QSPIC_STATUSCMD_REG	The way of reading the status of external device in Auto mode
0x46000038	QSPIC_CHCKERASE_REG	Check erase progress in Auto mode
0x4600003C	QSPIC_GP_REG	General purpose QSPIC register
0x46000040	QSPIC_AWRITECMD_REG	The way of writing in Auto mode when the external device is a serial SRAM
0x46000044	QSPIC_MEMBLEN_REG	External memory burst length configuration

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Table 1048: QSPIC_CTRLBUS_REG (0x46000000)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4	W	QSPIC_DIS_CS	Write 1 to disable the chip select (active low) when the controller is in Manual mode.	0x0
3	W	QSPIC_EN_CS	Write 1 to enable the chip select (active low) when the controller is in Manual mode.	0x0
2	W	QSPIC_SET_QUAD	Write 1 to set the bus mode in Quad mode when the controller is in Manual mode.	0x0
1	W	QSPIC_SET_DUAL	Write 1 to set the bus mode in Dual mode when the controller is in Manual mode.	0x0
0	W	QSPIC_SET_SINGLE	Write 1 to set the bus mode in Single SPI mode when the controller is in Manual mode.	0x0

Table 1049: QSPIC_CTRLMODE_REG (0x46000004)

Bit	Mode	Symbol	Description	Reset
31:17	-	-	Reserved	0x0
16	R/W	QSPIC_CLK_FREE_EN	Controls the behavior of the QSPI_SCK when the QSPI_CS is high and the QSPIC_CS_MD=1. 0: Is produced one QSPI_SCK clock pulse after each 0 to 1 transition in the QSPI_CS. 1: The QSPI_SCK clock remains always active, while the QSPI_CS is inactive. This setting has meaning only when the QSPIC_CS_MD=1.	0x0
15	R/W	QSPIC_CS_MD	Controls the clock edge with which is produced the QSPI_CS signal. 0: The QSPI_CS is produced with the rising edge of the QSPI_SCK. The QSPI_SCK is always inactive while the QSPI_CS is high. 1: The QSPI_CS is produced with the falling edge of the QSPI_SCK. The behavior of the QSPI_SCK while the QSPI_CS is high, is controlled by the QSPIC_CLK_FREE_EN.	0x0
14	R/W	QSPIC_SRAM_EN	Defines the type of the external device that is connected on the QSPIC controller 0: The external memory device is a serial Flash 1: The external memory device is a serial SRAM When the external device is a serial SRAM, the erase suspend/ resume functionality of the controller is disabled. In this case the writing of the QSPIC_ERASECTRL_REG[QSPIC_ERASE_EN] bit has no effect. Also, the memory space where the external device is mapped, is considered as writable.	0x0

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Bit	Mode	Symbol	Description	Reset
13	R/W	QSPIC_USE_32BA	Controls the length of the address that the external memory device uses. 0: The external memory device uses 24 bits address. 1: The external memory device uses 32 bits address. The controller uses this bit in order to decide the number of the address bytes that has to transfer to the external device during Auto mode.	0x0
12	R/W	QSPIC_FORCENSEQ_EN	Controls the way with which is addressed by the QSPI controller a burst request from the AMBA bus. 0: The controller translates a burst access on the AMBA bus as a burst access on the QSPI bus. That results to the minimum number of command/address phases. 1: The controller will split a burst access on the AMBA bus into a number of single accesses on the QSPI bus. That results to a separate command for each beat of the burst. E.g a 4-beat word incremental AMBA read access will be split into 4 different sequences on the QSPI bus: command/address/extra clock/read data. The QSPI_CS will be low only for the time that is needed for each of these single access. This configuration bit is usefull when the clock frequency of the QSPI bus is much higher than the clock of the AMBA bus. In this case the interval for which the CS remains low is minimized, achieving lower power dissipation with respect of the case where the QSPIC_FORCENSEQ_EN=0, at cost of performance.	0x0
11:9	R/W	QSPIC_PCLK_MD	Controls the read pipe clock delay relative to the falling edge of QSPI_SCK. Refer to QSPI Timing for timing parameters	0x0
8	R/W	QSPIC_RPIPE_EN	Controls the use of the data read pipe. 0: The read pipe is disabled, the sampling clock is defined according to the QSPIC_RXD_NEG setting. 1: The read pipe is enabled. The delay of the sampling clock is defined according to the QSPI_PCLK_MD setting. (Recommended)	0x0
7	R/W	QSPIC_RXD_NEG	Defines the clock edge that is used for the capturing of the received data, when the read pipe is not active (QSPIC_RPIPE_EN = 0). 0: Sampling of the received data with the positive edge of the QSPI_SCK 1: Sampling of the received data with the negative edge of the QSPI_SCK The internal QSPI_SCK clock that is used by the controller for the capturing of the received data has a skew in respect of the QSPI_SCK that is received by the external memory device. In order to be improved the timing requirements of the read	0x0

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Bit	Mode	Symbol	Description	Reset
			path, the controller supports a read pipe register with programmable clock delay. See also the QSPIC_RPIPE_EN register.	
6	R/W	QSPIC_HRDY_MD	This configuration bit is useful when the frequency of the QSPI clock is much lower than the clock of the AMBA bus, in order to not locks the AMBA bus for a long time. 0: Adds wait states via hready signal when an access is performed on the QSPIC_WRITEDATA, QSPIC_READDATA and QSPIC_DUMMYDATA registers. It is not needed to checked the QSPIC_BUSY of the QSPIC_STATUS_REG. 1: The controller don't adds wait states via the hready signal, when is performed access on the QSPIC_WRITEDATA, QSPIC_READDATA and QSPIC_DUMMYDATA registers. The QSPIC_BUSY bit of the QSPIC_STATUS_REG must be checked in order to be detected the completion of the requested access. It is applicable only when the controller is in Manual mode. In the case of the Auto mode, the controller always adds wait states via the hready signal.	0x0
5	R/W	QSPIC_IO3_DAT	The value of QSPI_IO3 pad if QSPI_IO3_OEN is 1	0x0
4	R/W	QSPIC_IO2_DAT	The value of QSPI_IO2 pad if QSPI_IO2_OEN is 1	0x0
3	R/W	QSPIC_IO3_OEN	QSPI_IO3 output enable. Use this only in SPI or Dual SPI mode to control /HOLD signal. When the Auto Mode is selected (QSPIC_AUTO_MD = 1) and the QUAD SPI is used, set this bit to zero. 0: The QSPI_IO3 pad is input. 1: The QSPI_IO3 pad is output.	0x0
2	R/W	QSPIC_IO2_OEN	QSPI_IO2 output enable. Use this only in SPI or Dual SPI mode to control /WP signal. When the Auto Mode is selected (QSPIC_AUTO_MD = 1) and the QUAD SPI is used, set this bit to zero. 0: The QSPI_IO2 pad is input. 1: The QSPI_IO2 pad is output.	0x0
1	R/W	QSPIC_CLK_MD	Mode of the generated QSPI_SCK clock 0: Use Mode 0 for the QSPI_CLK. The QSPI_SCK is low when QSPI_CS is high. 1: Use Mode 3 for the QSPI_CLK. The QSPI_SCK is high when QSPI_CS is high. See also the register QSPIC_CS_MD and the QSPIC_CLK_FREE_EN	0x0
0	R/W	QSPIC_AUTO_MD	Mode of operation 0: The Manual Mode is selected. 1: The Auto Mode is selected.	0x0

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Bit	Mode	Symbol	Description	Reset
			During an erasing the QSPIC_AUTO_MD goes in read only mode (see QSPIC_ERASE_EN)	

Table 1050: QSPIC_RECVDATA_REG (0x46000008)

Bit	Mode	Symbol	Description	Reset
31:0	R	QSPIC_RECVDATA	This register contains the received data when the QSPIC_READDATA_REG register is used in Manual mode, in order to be retrieved data from the external memory device and QSPIC_HRDY_MD=1 && QSPIC_BUSY=0.	0x0

Table 1051: QSPIC_BURSTCMDA_REG (0x4600000C)

Bit	Mode	Symbol	Description	Reset
31:30	R/W	QSPIC_DMY_TX_MD	It describes the mode of the SPI bus during the Dummy bytes phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
29:28	R/W	QSPIC_EXT_TX_MD	It describes the mode of the SPI bus during the Extra Byte phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
27:26	R/W	QSPIC_ADR_TX_MD	It describes the mode of the SPI bus during the address phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
25:24	R/W	QSPIC_INST_TX_MD	It describes the mode of the SPI bus during the instruction phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
23:16	R/W	QSPIC_EXT_BYTE	The value of an extra byte which will be transferred after address (only if QSPIC_EXT_BYTE_EN= 1). Usually this is the Mode Bits in Dual/Quad SPI I/O instructions.	0x0
15:8	R/W	QSPIC_INST_WB	Instruction Value for Wrapping Burst. This value is the selected instruction when QSPIC_WRAP_MD is equal to 1 and the access is a wrapping burst of length and size described by the bit fields QSPIC_WRAP_LEN and QSPIC_WRAP_SIZE respectively.	0x0

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Bit	Mode	Symbol	Description	Reset
7:0	R/W	QSPIC_INST	Instruction Value for Incremental Burst or Single read access. This value is the selected instruction at the cases of incremental burst or single read access. Also this value is used when a wrapping burst is not supported (QSPIC_WRAP_MD)	0x0

Table 1052: QSPIC_BURSTCMDB_REG (0x46000010)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	0x0
15	R/W	QSPIC_DMY_FORCE	By setting this bit, the number of dummy bytes is forced to be equal to 3. In this case the QSPIC_DMY_NUM field is overruled and has no function. 0: The number of dummy bytes is controlled by the QSPIC_DMY_NUM field 1: Three dummy bytes are used. The QSPIC_DMY_NUM is overruled.	0x0
14:12	R/W	QSPIC_CS_HIGH_MIN	Between the transmission of two different instructions to the flash memory, the qspi bus stays in idle state (QSPI_CS high) for at least this number of QSPI_SCK clock cycles. See the QSPIC_ERS_CS_HI and the QSPIC_WR_CS_HIGH_MIN registers for some exceptions.	0x0
11:10	R/W	QSPIC_WRAP_SIZE	It describes the selected data size of a wrapping burst (QSPIC_WRAP_MD). 0x0: Byte access (8-bits) 0x1: Half word access (16 bits) 0x2: Word access (32-bits) 0x3: Reserved	0x0
9:8	R/W	QSPIC_WRAP_LEN	It describes the selected length of a wrapping burst (QSPIC_WRAP_MD). 0x0: 4 beat wrapping burst 0x1: 8 beat wrapping burst 0x2: 16 beat wrapping burst 0x3: Reserved	0x0
7	R/W	QSPIC_WRAP_MD	Wrap mode 0: The QSPIC_INST is the selected instruction at any access. 1: The QSPIC_INST_WB is the selected instruction at any wrapping burst access of length and size described by the registers QSPIC_WRAP_LEN and QSPIC_WRAP_SIZE respectively. In all other cases the QSPIC_INST is the selected instruction. Use this feature only when the serial FLASH memory supports a special instruction for wrapping burst access.	0x0
6	R/W	QSPIC_INST_MD	Instruction mode 0: Transmit instruction at any burst access.	0x0

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Bit	Mode	Symbol	Description	Reset
			1: Transmit instruction only in the first access after the selection of Auto Mode.	
5:4	R/W	QSPIC_DMY_NUM	Number of Dummy Bytes 0x0: Zero Dummy Bytes (Don't Send Dummy Bytes) 0x1: Send 1 Dummy Byte 0x2: Send 2 Dummy Bytes 0x3: Send 4 Dummy Bytes When QSPIC_DMY_FORCE is enabled, the QSPIC_DMY_NUM is overruled. In this case the number of dummy bytes is defined by the QSPIC_DMY_FORCE and is equal to 3, independent of the value of the QSPIC_DMY_NUM.	0x0
3	R/W	QSPIC_EXT_HF_DS	Extra Half Disable Output 0: if QSPIC_EXT_BYTE_EN=1 then transmit the complete QSPIC_EXT_BYTE 1: if QSPIC_EXT_BYTE_EN=1 then disable (hi-z) output during the transmission of bits [3:0] of QSPIC_EXT_BYTE	0x0
2	R/W	QSPIC_EXT_BYTE_EN	Extra Byte Enable 0: Don't Send QSPIC_EXT_BYTE 1: Send QSPIC_EXT_BYTE	0x0
1:0	R/W	QSPIC_DAT_RX_MD	It describes the mode of the SPI bus during the data phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0

Table 1053: QSPIC_STATUS_REG (0x46000014)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	QSPIC_BUSY	The status of the SPI Bus. 0: The SPI Bus is idle 1: The SPI Bus is active. Read data, write data or dummy data activity is in progress. Has meaning only in Manual mode and only when QSPIC_HRDY_MD = 1.	0x0

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Table 1054: QSPIC_WRITEDATA_REG (0x46000018)

Bit	Mode	Symbol	Description	Reset
31:0	W	QSPIC_WRITEDATA	Writing to this register is generating a data transfer from the controller to the external memory device. The data written in this register, is then transferred to the memory using the selected mode of the SPI bus (SPI, Dual SPI, Quad SPI). The data size of the access to this register can be 32-bits / 16-bits/ 8-bits and is equal to the number of the transferred bits. This register has meaning only when the controller is in Manual mode.	0x0

Table 1055: QSPIC_READDATA_REG (0x4600001C)

Bit	Mode	Symbol	Description	Reset
31:0	R	QSPIC_READDATA	A read access at this register generates a data transfer from the external memory device to the QSPIC controller. The data is transferred using the selected mode of the SPI bus (SPI, Dual SPI, Quad SPI). The data size of the access to this register can be 32-bits / 16-bits / 8-bits and is equal to the number of the transferred bits. This register has meaning only when the controller is in Manual mode.	0x0

Table 1056: QSPIC_DUMMYDATA_REG (0x46000020)

Bit	Mode	Symbol	Description	Reset
31:0	W	QSPIC_DUMMYDATA	Writing to this register generates a number of clock pulses to the SPI bus. During the last clock of this activity in the SPI bus, the QSPI_IOx data pads are in hi-z state. The data size of the access to this register can be 32-bits / 16-bits/ 8-bits. The number of generated pulses is equal to: (size of AHB bus access) / (size of SPI bus). The size of SPI bus is equal to 1, 2 or 4 for Single, Dual or Quad SPI mode respectively. This register has meaning only when the controller is in Manual mode.	0x0

Table 1057: QSPIC_ERASECTRL_REG (0x46000024)

Bit	Mode	Symbol	Description	Reset
31:28	-	-	Reserved	0x0
27:25	R	QSPIC_ERS_STATE	It shows the progress of sector/block erasing (read only). 0x0: No Erase. 0x1: Pending erase request 0x2: Erase procedure is running 0x3: Suspended Erase procedure	0x0

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Bit	Mode	Symbol	Description	Reset
			0x4: Finishing the Erase procedure 0x5..0x7: Reserved	
24	R/W	QSPIC_ERASE_EN	This bit has meaning only when the external device is a serial FLASH (QSPIC_SRAM_EN=0). During Manual mode (QSPIC_AUTO_MD = 0) : This bit is in read only mode. During Auto mode (QSPIC_AUTO_MD = 1). To request the erasing of the block/sector (QSPIC_ERS_ADDR, 12'b0) write 1 to this bit. This bit is cleared automatically with the end of the erasing. Until the end of erasing the QSPIC_ERASE_EN remains in read only mode. During the same period of time the controller remains in Auto Mode (QSPIC_AUTO_MD goes in read only mode). In the case where the external device is a serial SRAM (QSPIC_SRAM_EN=1) this bit is in read only mode.	0x0
23:4	R/W	QSPIC_ERS_ADDR	Defines the address of the block/sector that is requested to be erased. If QSPIC_USE_32BA = 0 (24 bits addressing), bits QSPIC_ERASECTRL_REG[23-12] determine the block/ sector address bits [23-12]. QSPIC_ERASECTRL_REG[11-4] are ignored by the controller. If QSPIC_USE_32BA = 1 (32 bits addressing) bits QSPIC_ERASECTRL_REG[23-4] determine the block / sectors address bits [31:12]	0x0
3:0	-	-	Reserved	0x0

Table 1058: QSPIC_ERASECMDA_REG (0x46000028)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	QSPIC_RES_INST	The code value of the erase resume instruction	0x0
23:16	R/W	QSPIC_SUS_INST	The code value of the erase suspend instruction.	0x0
15:8	R/W	QSPIC_WEN_INST	The code value of the write enable instruction.	0x0
7:0	R/W	QSPIC_ERS_INST	The code value of the erase instruction.	0x0

Table 1059: QSPIC_ERASECMDB_REG (0x4600002C)

Bit	Mode	Symbol	Description	Reset
31:30	-	-	Reserved	0x0
29:24	R/W	QSPIC_RESSUS_DLY	Defines a timer that counts the minimum allowed delay between an erase suspend command and the previous erase resume command (or the initial erase command). 0x00: Dont wait. The controller starts immediately to suspend the erase procedure.	0x0

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Bit	Mode	Symbol	Description	Reset
			0x01..0x3F: The controller waits for at least this number of 288 KHz clock cycles before the suspension of erasing. Time starts counting after the end of the previous erase resume command (or the initial erase command)	
23:20	-	-	Reserved	0x0
19:16	R/W	QSPIC_ERSRES_HLD	The controller must stay without flash memory reading requests for this number of AMBA hclk clock cycles, before to perform the command of erase or erase resume. Allowable range : 0xF - 0x0	0x0
15	-	-	Reserved	0x0
14:10	R/W	QSPIC_ERS_CS_HI	After the execution of instructions: write enable, erase, erase suspend and erase resume, the QSPI_CS remains high for at least this number of QSPI_SCK clock cycles.	0x0
9:8	R/W	QSPIC_EAD_TX_MD	The mode of the SPI Bus during the address phase of the erase instruction 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
7:6	R/W	QSPIC_RES_TX_MD	The mode of the SPI Bus during the transmission of the resume instruction 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
5:4	R/W	QSPIC_SUS_TX_MD	The mode of the SPI Bus during the transmission of the suspend instruction. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
3:2	R/W	QSPIC_WEN_TX_MD	The mode of the SPI Bus during the transmission of the write enable instruction. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
1:0	R/W	QSPIC_ERS_TX_MD	The mode of the SPI Bus during the instruction phase of the erase instruction 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0

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Table 1060: QSPIC_BURSTBRK_REG (0x46000030)

Bit	Mode	Symbol	Description	Reset
31:21	-	-	Reserved	0x0
20	R/W	QSPIC_SEC_HF_DS	Disable output during the transmission of the second half (QSPIC_BRK_WRD[3:0]). Setting this bit is only useful if QSPIC_BRK_EN =1 and QSPIC_BRK_SZ= 1. 0: The controller drives the SPI bus during the transmission of the QSPIC_BRK_WRD[3:0]. 1: The controller leaves the SPI bus in Hi-Z during the transmission of the QSPIC_BRK_WORD[3:0].	0x0
19:18	R/W	QSPIC_BRK_TX_MD	The mode of the SPI Bus during the transmission of the read break sequence. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
17	R/W	QSPIC_BRK_SZ	The size of the read break sequence. 0: One byte (Send QSPIC_BRK_WRD[15:8]) 1: Two bytes (Send QSPIC_BRK_WRD[15:0])	0x0
16	R/W	QSPIC_BRK_EN	Controls the application of a special command (read break sequence) that is used in order to force the device to abandon the continuous read mode. 0: The special command is not applied 1: The special command is applied This special command is applied by the controller to the external device under the following conditions: - the controller is in Auto mode - the QSPIC_INST_MD = 1 - the previous command that has been applied in the external device was read - the controller want to apply to the external device a command different than the read.	0x0
15:0	R/W	QSPIC_BRK_WRD	This is the value of a special command (read break sequence) that is applied by the controller to the external memory device, in order to force the memory device to abandon the continuous read mode.	0x0

Table 1061: QSPIC_STATUSCMD_REG (0x46000034)

Bit	Mode	Symbol	Description	Reset
31:23	-	-	Reserved	0x0
22	R/W	QSPIC_STSDLY_SEL	Defines the timer which is used to count the delay that it has to wait before to read the FLASH Status Register, after an erase or an erase resume command.	0x0

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Bit	Mode	Symbol	Description	Reset
			0: The delay is controlled by the QSPIC_RESSTS_DLY which counts on the qspi clock. 1: The delay is controlled by the QSPIC_RESSUS_DLY which counts on the 288 kHz clock.	
21:16	R/W	QSPIC_RESSTS_DLY	Defines a timer that counts the minimum required delay between the reading of the status register and of the previous erase or erase resume instruction. 0x00: Dont wait. The controller starts to reading the Flash memory status register immediately. 0x01..0x3F: The controller waits for at least this number of QSPI_CLK cycles and afterwards it starts to reading the Flash memory status register. The timer starts to count after the end of the previous erase or erase resume command. The actual timer that will be used by the controller before the reading of the Flash memory status register is defined by the QSPIC_STSDLY_SEL.	0x0
15	R/W	QSPIC_BUSY_VAL	Defines the value of the Busy bit which means that the flash is busy. 0: The flash is busy when the Busy bit is equal to 0. 1: The flash is busy when the Busy bit is equal to 1.	0x0
14:12	R/W	QSPIC_BUSY_POS	Defines the bit of the Flash status register which represents the Busy bit (0x7 - 0x0).	0x0
11:10	R/W	QSPIC_RSTAT_RX_MD	The mode of the SPI Bus during the reception phase of the read status instruction, where the value of status register is retrieved. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
9:8	R/W	QSPIC_RSTAT_TX_MD	The mode of the SPI Bus during the instruction phase of the read status instruction. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
7:0	R/W	QSPIC_RSTAT_INST	The code value of the read status instruction. It is transmitted during the instruction phase of the read status instruction.	0x0

Table 1062: QSPIC_CHCKERASE_REG (0x46000038)

Bit	Mode	Symbol	Description	Reset
31:0	W	QSPIC_CHCKERASE	Writing any value to this register during erasing, forces the controller to read the flash memory status register. Depending on the value of the Busy bit, it updates the QSPIC_ERASE_EN.	0x0

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Bit	Mode	Symbol	Description	Reset
			This register has meaning only when the controller is in Auto mode and there is an erase in progress (QSPIC_ERASE_EN =1). It has no meaning when the external device is a serial SRAM.	

Table 1063: QSPIC_GP_REG (0x4600003C)

Bit	Mode	Symbol	Description	Reset
4:3	R/W	QSPIC_PADS_SLEW	QSPI pads slew rate control. Indicative values under certain conditions: 0x0 : Rise=1.7 V/ns, Fall=1.9 V/ns (weak) 0x1 : Rise=2.0 V/ns, Fall=2.3 V/ns 0x2 : Rise=2.3 V/ns, Fall=2.6 V/ns 0x3 : Rise=2.4 V/ns, Fall=2.7 V/ns (strong) Conditions: FLASH pin capacitance 6 pF, Vcc = 1.8 V, T = 25 °C and Idrive = 16 mA	0x0
2:1	R/W	QSPIC_PADS_DRV	QSPI pads drive current 0x0 : 4 mA 0x1 : 8 mA 0x2 : 12 mA 0x3 : 16 mA	0x0
0	R/W	-	Reserved	0x0

Table 1064: QSPIC_AWRITECMD_REG (0x46000040)

Bit	Mode	Symbol	Description	Reset
31:19	-	-	Reserved	0x0
18:14	R/W	QSPIC_WR_CS_HIGH_MIN	After the execution of the write command, the QSPI_CS remains high for at least this number of QSPI_SCK clock cycles.	0x0
13:12	R/W	QSPIC_WR_DAT_TX_MD	The mode of the SPI Bus during the data phase of the write command. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
11:10	R/W	QSPIC_WR_ADR_TX_MD	The mode of the SPI Bus during the adress phase of the write command. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
9:8	R/W	QSPIC_WR_INST_TX_MD	The mode of the SPI Bus during the instruction phase of the write command. 0x0: Single SPI 0x1: Dual 0x2: Quad	0x0

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Bit	Mode	Symbol	Description	Reset
			0x3: Reserved	
7:0	R/W	QSPIC_WR_INST	This is the value of the instruction that is used, in order to be programmed the external SRAM device.	0x0

Table 1065: QSPIC_MEMBLEN_REG (0x46000044)

Bit	Mode	Symbol	Description	Reset
31:14	-	-	Reserved	0x0
13:4	R/W	QSPIC_T_CEM_CC	Defines the maximum allowed time tCEM for which the QSPIC_CS can stay active (QSPI_CS=0). It has meaning only when QSPIC_T_CEM_EN is equal to 1. See also the description of the QSPIC_T_CEM_EN for more details. The tCEM is expressed in number of qspi clock cycles and can be calculated as follows : tCEM / (qspi_clock_period) If the result of the above equation is higher than 0x3FF, use the value 0x3FF.	0x0
3	R/W	QSPIC_T_CEM_EN	This bit enables the controlling of the maximum time tCEM for which the QSPI_CS remains active. It has meaning only when the Auto mode is active (QSPIC_AUTO_MD=1) and the external device is a serial SRAM (QSPIC_SRAM_EN=1). In the case where the external device is a serial Flash (QSPIC_SRAM_EN=0) or the controller is in Manual mode (QSPIC_AUTO_MD=0), this field has no any effect. This feature is usefull in the case where the external serial device is a dynamic RAM that requires refresh. If the refresh is applied only when the device is in the idle state (QSPI_CS = 1), the time for which the device remains in the active state (QSPI_CS = 0) should be limited by a maximum threshold. 0:There is no any constraint regarding the maximum allowed time for which the QSPI_CS can stay active. This is the case also when QSPIC_SRAM_EN=0 or QSPIC_AUTO_MD=0. 1:There is a maximum allowed time interval tCEM for which the QSPI_CS can stay active during a burst access (for reading or writting of data). For the controller this is considered as equal to QSPIC_T_CEM_CC x qspi_clock_period. In the case where the data transfer requires the QSPI_CS to stays active for more than QSPIC_T_CEM_CC qspi clock cycles, the QSPI controller splits the access on the SPI bus in more than one bursts, by inserting inactive periods	0x0

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Bit	Mode	Symbol	Description	Reset
			(QSPI_CS = 0) between them. This will cost extra clock cycles for the realization of the original acceess, due to the additional commands that are required in the SPI bus. The value in the QSPIC_T_CEM_CC should be updated every time where the frequency of the qspi clock is modified. The qspi clock frequency should not be decreased more than a lowest frequency. This is the lowest frequency that enables the be performed a 32-bit word read and write access, without violating the tCEM timing requirement (the QSPI controller allows to be performed at least the transferring of one beat of the requested burst, independent of the QSPIC_T_CEM_CC limit).	
2:0	R/W	QSPIC_MEMBLEN	In this register is defined the expected behavior of the external memory device regarding the length of a burst operation : 0x0: The external memory device is capable to implement incremental burst of unspecified length. 0x1: The external memory device implements a wrapping burst of length 4 bytes. 0x2: The external memory device implements a wrapping burst of length 8 bytes. 0x3: The external memory device implements a wrapping burst of length 16 bytes. 0x4: The external memory device implements a wrapping burst of length 32 bytes. 0x5: The external memory device implements a wrapping burst of length 64 bytes. 0x6 - 0x7 : Reserved This setting is used by the QSPI controller when the Auto mode is enabled (QSPIC_AUTO_MD=1), in order to handle the various burst requests of the AHB bus, in respect of the requirements of the external memory device. The external memory device may need to be configured by applying special instruction, in order to be defined the kind of the burst operation. This can be implemented by applying this special instruction with the QSPI controller in Manual mode (QSPIC_AUTO_MD=1). Refer to the datasheet of the external device for more information.	0x0

Table 1066: Register map QSPIC2

Address	Register	Description
0x26000000	QSPIC2_CTRLBUS_REG	SPI Bus control register for the Manual mode
0x26000004	QSPIC2_CTRLMODE_REG	Mode control register

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Address	Register	Description
0x26000008	QSPIC2_RECVDATA_REG	Received data for the Manual mode
0x2600000C	QSPIC2_BURSTCMDA_REG	The way of reading in Auto mode (command register A)
0x26000010	QSPIC2_BURSTCMDB_REG	The way of reading in Auto mode (command register B)
0x26000014	QSPIC2_STATUS_REG	The status register of the QSPI controller
0x26000018	QSPIC2_WRITEDATA_REG	Write data to SPI Bus for the Manual mode
0x2600001C	QSPIC2_READDATA_REG	Read data from SPI Bus for the Manual mode
0x26000020	QSPIC2_DUMMYDATA_REG	Send dummy clocks to SPI Bus for the Manual mode
0x26000024	QSPIC2_ERASECTRL_REG	Erase control register
0x26000028	QSPIC2_ERASECMDA_REG	The way of erasing in Auto mode (command register A)
0x2600002C	QSPIC2_ERASECMDB_REG	The way of erasing in Auto mode (command register B)
0x26000030	QSPIC2_BURSTBRK_REG	Read break sequence in Auto mode
0x26000034	QSPIC2_STATUSCMD_REG	The way of reading the status of external device in Auto mode
0x26000038	QSPIC2_CHCKERASE_REG	Check erase progress in Auto mode
0x2600003C	QSPIC2_GP_REG	General purpose QSPIC2 register
0x26000040	QSPIC2_AWRITECMD_REG	The way of writing in Auto mode when the external device is a serial SRAM
0x26000044	QSPIC2_MEMBLEN_REG	External memory burst length configuration

Table 1067: QSPIC2_CTRLBUS_REG (0x26000000)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4	W	QSPIC_DIS_CS	Write 1 to disable the chip select (active low) when the controller is in Manual mode.	0x0
3	W	QSPIC_EN_CS	Write 1 to enable the chip select (active low) when the controller is in Manual mode.	0x0
2	W	QSPIC_SET_QUAD	Write 1 to set the bus mode in Quad mode when the controller is in Manual mode.	0x0
1	W	QSPIC_SET_DUAL	Write 1 to set the bus mode in Dual mode when the controller is in Manual mode.	0x0
0	W	QSPIC_SET_SINGLE	Write 1 to set the bus mode in Single SPI mode when the controller is in Manual mode.	0x0

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Table 1068: QSPIC2_CTRLMODE_REG (0x26000004)

Bit	Mode	Symbol	Description	Reset
31:17	-	-	Reserved	0x0
16	R/W	QSPIC_CLK_FREE_EN	Controls the behavior of the QSPI_SCK when the QSPI_CS is high and the QSPIC_CS_MD=1. 0: Is produced one QSPI_SCK clock pulse after each 0 to 1 transition in the QSPI_CS. 1: The QSPI_SCK clock remains always active, while the QSPI_CS is inactive. This setting has meaning only when the QSPIC_CS_MD=1.	0x0
15	R/W	QSPIC_CS_MD	Controls the clock edge with which is produced the QSPI_CS signal. 0: The QSPI_CS is produced with the rising edge of the QSPI_SCK. The QSPI_SCK is always inactive while the QSPI_CS is high. 1: The QSPI_CS is produced with the falling edge of the QSPI_SCK. The behavior of the QSPI_SCK while the QSPI_CS is high, is controlled by the QSPIC_CLK_FREE_EN.	0x0
14	R/W	QSPIC_SRAM_EN	Defines the type of the external device that is connected on the QSPIC controller 0: The external memory device is a serial Flash 1: The external memory device is a serial SRAM When the external device is a serial SRAM, the erase suspend/ resume functionality of the controller is disabled. In this case the writing of the QSPIC_ERASECTRL_REG[QSPIC_ERASE_EN] bit has no effect. Also, the memory space where the external device is mapped, is considered as writable.	0x0
13	R/W	QSPIC_USE_32BA	Controls the length of the address that the external memory device uses. 0: The external memory device uses 24 bits address. 1: The external memory device uses 32 bits address. The controller uses this bit in order to decide the number of the address bytes that has to transfer to the external device during Auto mode.	0x0
12	R/W	QSPIC_FORCENSEQ_EN	Controls the way with which is addressed by the QSPI controller a burst request from the AMBA bus. 0: The controller translates a burst access on the AMBA bus as a burst access on the QSPI bus. That results to the minimum number of command/address phases. 1: The controller will split a burst access on the AMBA bus into a number of single accesses on the QSPI bus. That results to a separate	0x0

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Bit	Mode	Symbol	Description	Reset
			command for each beat of the burst. E.g a 4-beat word incremental AMBA read access will be split into 4 different sequences on the QSPI bus: command/address/extra clock/read data. The QSPI_CS will be low only for the time that is needed for each of these single access. This configuration bit is usefull when the clock frequency of the QSPI bus is much higher than the clock of the AMBA bus. In this case the interval for which the CS remains low is minimized, achieving lower power dissipation with respect of the case where the QSPIC_FORCENSEQ_EN=0, at cost of performance.	
11:9	R/W	QSPIC_PCLK_MD	Controls the read pipe clock delay relative to the falling edge of QSPI_SCK. Refer to QSPI Timing for timing parameters	0x0
8	R/W	QSPIC_RPIPE_EN	Controls the use of the data read pipe. 0: The read pipe is disabled, the sampling clock is defined according to the QSPIC_RXD_NEG setting. 1: The read pipe is enabled. The delay of the sampling clock is defined according to the QSPI_PCLK_MD setting. (Recommended)	0x0
7	R/W	QSPIC_RXD_NEG	Defines the clock edge that is used for the capturing of the received data, when the read pipe is not active (QSPIC_RPIPE_EN = 0). 0: Sampling of the received data with the positive edge of the QSPI_SCK 1: Sampling of the received data with the negative edge of the QSPI_SCK The internal QSPI_SCK clock that is used by the controller for the capturing of the received data has a skew in respect of the QSPI_SCK that is received by the external memory device. In order to be improved the timing requirements of the read path, the controller supports a read pipe register with programmable clock delay. See also the QSPIC_RPIPE_EN register.	0x0
6	R/W	QSPIC_HRDY_MD	This configuration bit is useful when the frequency of the QSPI clock is much lower than the clock of the AMBA bus, in order to not locks the AMBA bus for a long time. 0: Adds wait states via hready signal when an access is performed on the QSPIC_WRITEDATA, QSPIC_READDATA and QSPIC_DUMMYDATA registers. It is not needed to checked the QSPIC_BUSY of the QSPIC_STATUS_REG. 1: The controller don't adds wait states via the hready signal, when is performed access on the QSPIC_WRITEDATA, QSPIC_READDATA and QSPIC_DUMMYDATA registers. The QSPIC_BUSY bit of the QSPIC_STATUS_REG must be checked in order to be detected the completion of the requested access.	0x0

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Bit	Mode	Symbol	Description	Reset
			It is applicable only when the controller is in Manual mode. In the case of the Auto mode, the controller always adds wait states via the hready signal.	
5	R/W	QSPIC_IO3_DAT	The value of QSPI_IO3 pad if QSPI_IO3_OEN is 1	0x0
4	R/W	QSPIC_IO2_DAT	The value of QSPI_IO2 pad if QSPI_IO2_OEN is 1	0x0
3	R/W	QSPIC_IO3_OEN	QSPI_IO3 output enable. Use this only in SPI or Dual SPI mode to control /HOLD signal. When the Auto Mode is selected (QSPIC_AUTO_MD = 1) and the QUAD SPI is used, set this bit to zero. 0: The QSPI_IO3 pad is input. 1: The QSPI_IO3 pad is output.	0x0
2	R/W	QSPIC_IO2_OEN	QSPI_IO2 output enable. Use this only in SPI or Dual SPI mode to control /WP signal. When the Auto Mode is selected (QSPIC_AUTO_MD = 1) and the QUAD SPI is used, set this bit to zero. 0: The QSPI_IO2 pad is input. 1: The QSPI_IO2 pad is output.	0x0
1	R/W	QSPIC_CLK_MD	Mode of the generated QSPI_SCK clock 0: Use Mode 0 for the QSPI_CLK. The QSPI_SCK is low when QSPI_CS is high. 1: Use Mode 3 for the QSPI_CLK. The QSPI_SCK is high when QSPI_CS is high. See also the register QSPIC_CS_MD and the QSPIC_CLK_FREE_EN	0x0
0	R/W	QSPIC_AUTO_MD	Mode of operation 0: The Manual Mode is selected. 1: The Auto Mode is selected. During an erasing the QSPIC_AUTO_MD goes in read only mode (see QSPIC_ERASE_EN)	0x0

Table 1069: QSPIC2_RECVDATA_REG (0x26000008)

Bit	Mode	Symbol	Description	Reset
31:0	R	QSPIC_RECVDATA	This register contains the received data when the QSPIC_READDATA_REG register is used in Manual mode, in order to be retrieved data from the external memory device and QSPIC_HRDY_MD=1 && QSPIC_BUSY=0.	0x0

Table 1070: QSPIC2_BURSTCMDA_REG (0x2600000C)

Bit	Mode	Symbol	Description	Reset
31:30	R/W	QSPIC_DMY_TX_MD	It describes the mode of the SPI bus during the Dummy bytes phase.	0x0

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Bit	Mode	Symbol	Description	Reset
			0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	
29:28	R/W	QSPIC_EXT_TX_MD	It describes the mode of the SPI bus during the Extra Byte phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
27:26	R/W	QSPIC_ADR_TX_MD	It describes the mode of the SPI bus during the address phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
25:24	R/W	QSPIC_INST_TX_MD	It describes the mode of the SPI bus during the instruction phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
23:16	R/W	QSPIC_EXT_BYTE	The value of an extra byte which will be transferred after address (only if QSPIC_EXT_BYTE_EN= 1). Usually this is the Mode Bits in Dual/Quad SPI I/O instructions.	0x0
15:8	R/W	QSPIC_INST_WB	Instruction Value for Wrapping Burst. This value is the selected instruction when QSPIC_WRAP_MD is equal to 1 and the access is a wrapping burst of length and size described by the bit fields QSPIC_WRAP_LEN and QSPIC_WRAP_SIZE respectively.	0x0
7:0	R/W	QSPIC_INST	Instruction Value for Incremental Burst or Single read access. This value is the selected instruction at the cases of incremental burst or single read access. Also this value is used when a wrapping burst is not supported (QSPIC_WRAP_MD)	0x0

Table 1071: QSPIC2_BURSTCMDB_REG (0x26000010)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	0x0
15	R/W	QSPIC_DMY_FORCE	By setting this bit, the number of dummy bytes is forced to be equal to 3. In this case the QSPIC_DMY_NUM field is overruled and has no function. 0: The number of dummy bytes is controlled by the QSPIC_DMY_NUM field 1: Three dummy bytes are used. The QSPIC_DMY_NUM is overruled.	0x0

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Bit	Mode	Symbol	Description	Reset
14:12	R/W	QSPIC_CS_HIGH_MIN	Between the transmission of two different instructions to the flash memory, the qspi bus stays in idle state (QSPI_CS high) for at least this number of QSPI_SCK clock cycles. See the QSPIC_ERS_CS_HI and the QSPIC_WR_CS_HIGH_MIN registers for some exceptions.	0x0
11:10	R/W	QSPIC_WRAP_SIZE	It describes the selected data size of a wrapping burst (QSPIC_WRAP_MD). 0x0: Byte access (8-bits) 0x1: Half word access (16 bits) 0x2: Word access (32-bits) 0x3: Reserved	0x0
9:8	R/W	QSPIC_WRAP_LEN	It describes the selected length of a wrapping burst (QSPIC_WRAP_MD). 0x0: 4 beat wrapping burst 0x1: 8 beat wrapping burst 0x2: 16 beat wrapping burst 0x3: Reserved	0x0
7	R/W	QSPIC_WRAP_MD	Wrap mode 0: The QSPIC_INST is the selected instruction at any access. 1: The QSPIC_INST_WB is the selected instruction at any wrapping burst access of length and size described by the registers QSPIC_WRAP_LEN and QSPIC_WRAP_SIZE respectively. In all other cases the QSPIC_INST is the selected instruction. Use this feature only when the serial FLASH memory supports a special instruction for wrapping burst access.	0x0
6	R/W	QSPIC_INST_MD	Instruction mode 0: Transmit instruction at any burst access. 1: Transmit instruction only in the first access after the selection of Auto Mode.	0x0
5:4	R/W	QSPIC_DMY_NUM	Number of Dummy Bytes 0x0: Zero Dummy Bytes (Don't Send Dummy Bytes) 0x1: Send 1 Dummy Byte 0x2: Send 2 Dummy Bytes 0x3: Send 4 Dummy Bytes When QSPIC_DMY_FORCE is enabled, the QSPIC_DMY_NUM is overruled. In this case the number of dummy bytes is defined by the QSPIC_DMY_FORCE and is equal to 3, independent of the value of the QSPIC_DMY_NUM.	0x0
3	R/W	QSPIC_EXT_HF_DS	Extra Half Disable Output 0: if QSPIC_EXT_BYTE_EN=1 then transmit the complete QSPIC_EXT_BYTE	0x0

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Bit	Mode	Symbol	Description	Reset
			1: if QSPIC_EXT_BYTE_EN=1 then disable (hi-z) output during the transmission of bits [3:0] of QSPIC_EXT_BYTE	
2	R/W	QSPIC_EXT_BYTE_EN	Extra Byte Enable 0: Don't Send QSPIC_EXT_BYTE 1: Send QSPIC_EXT_BYTE	0x0
1:0	R/W	QSPIC_DAT_RX_MD	It describes the mode of the SPI bus during the data phase. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0

Table 1072: QSPIC2_STATUS_REG (0x26000014)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R	QSPIC_BUSY	The status of the SPI Bus. 0: The SPI Bus is idle 1: The SPI Bus is active. Read data, write data or dummy data activity is in progress. Has meaning only in Manual mode and only when QSPIC_HRDY_MD = 1.	0x0

Table 1073: QSPIC2_WRITEDATA_REG (0x26000018)

Bit	Mode	Symbol	Description	Reset
31:0	W	QSPIC_WRITEDATA	Writing to this register is generating a data transfer from the controller to the external memory device. The data written in this register, is then transferred to the memory using the selected mode of the SPI bus (SPI, Dual SPI, Quad SPI). The data size of the access to this register can be 32-bits / 16-bits/ 8-bits and is equal to the number of the transferred bits. This register has meaning only when the controller is in Manual mode.	0x0

Table 1074: QSPIC2_READDATA_REG (0x2600001C)

Bit	Mode	Symbol	Description	Reset
31:0	R	QSPIC_READDATA	A read access at this register generates a data transfer from the external memory device to the QSPIC controller. The data is transferred using the selected mode of the SPI bus (SPI, Dual SPI, Quad SPI). The data size of the access to this	0x0

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Bit	Mode	Symbol	Description	Reset
			register can be 32-bits / 16-bits / 8-bits and is equal to the number of the transferred bits. This register has meaning only when the controller is in Manual mode.	

Table 1075: QSPIC2_DUMMYDATA_REG (0x26000020)

Bit	Mode	Symbol	Description	Reset
31:0	W	QSPIC_DUMMYDATA	Writing to this register generates a number of clock pulses to the SPI bus. During the last clock of this activity in the SPI bus, the QSPI_IOx data pads are in hi-z state. The data size of the access to this register can be 32-bits / 16-bits/ 8-bits. The number of generated pulses is equal to: (size of AHB bus access) / (size of SPI bus). The size of SPI bus is equal to 1, 2 or 4 for Single, Dual or Quad SPI mode respectively. This register has meaning only when the controller is in Manual mode.	0x0

Table 1076: QSPIC2_ERASECTRL_REG (0x26000024)

Bit	Mode	Symbol	Description	Reset
31:28	-	-	Reserved	0x0
27:25	R	QSPIC_ERS_STATE	It shows the progress of sector/block erasing (read only). 0x0: No Erase. 0x1: Pending erase request 0x2: Erase procedure is running 0x3: Suspended Erase procedure 0x4: Finishing the Erase procedure 0x5..0x7: Reserved	0x0
24	R/W	QSPIC_ERASE_EN	This bit has meaning only when the external device is a serial FLASH (QSPIC_SRAM_EN=0). During Manual mode (QSPIC_AUTO_MD = 0) : This bit is in read only mode. During Auto mode (QSPIC_AUTO_MD = 1). To request the erasing of the block/sector (QSPIC_ERS_ADDR, 12'b0) write 1 to this bit. This bit is cleared automatically with the end of the erasing. Until the end of erasing the QSPIC_ERASE_EN remains in read only mode. During the same period of time the controller remains in Auto Mode (QSPIC_AUTO_MD goes in read only mode). In the case where the external device is a serial SRAM (QSPIC_SRAM_EN=1) this bit is in read only mode.	0x0

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Bit	Mode	Symbol	Description	Reset
23:4	R/W	QSPIC_ERS_ADDR	Defines the address of the block/sector that is requested to be erased. If QSPIC_USE_32BA = 0 (24 bits addressing), bits QSPIC_ERASECTRL_REG[23-12] determine the block/ sector address bits [23-12]. QSPIC_ERASECTRL_REG[11-4] are ignored by the controller. If QSPIC_USE_32BA = 1 (32 bits addressing) bits QSPIC_ERASECTRL_REG[23-4] determine the block / sectors address bits [31:12]	0x0
3:0	-	-	Reserved	0x0

Table 1077: QSPIC2_ERASECMDA_REG (0x26000028)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	QSPIC_RES_INST	The code value of the erase resume instruction	0x0
23:16	R/W	QSPIC_SUS_INST	The code value of the erase suspend instruction.	0x0
15:8	R/W	QSPIC_WEN_INST	The code value of the write enable instruction.	0x0
7:0	R/W	QSPIC_ERS_INST	The code value of the erase instruction.	0x0

Table 1078: QSPIC2_ERASECMDB_REG (0x2600002C)

Bit	Mode	Symbol	Description	Reset
31:30	-	-	Reserved	0x0
29:24	R/W	QSPIC_RESSUS_DLY	Defines a timer that counts the minimum allowed delay between an erase suspend command and the previous erase resume command (or the initial erase command). 0x00: Dont wait. The controller starts immediately to suspend the erase procedure. 0x01..0x3F: The controller waits for at least this number of 288 KHz clock cycles before the suspension of erasing. Time starts counting after the end of the previous erase resume command (or the initial erase command)	0x0
23:20	-	-	Reserved	0x0
19:16	R/W	QSPIC_ERSRES_HLD	The controller must stay without flash memory reading requests for this number of AMBA hclk clock cycles, before to perform the command of erase or erase resume. Allowable range : 0xF - 0x0	0x0
15	-	-	Reserved	0x0
14:10	R/W	QSPIC_ERS_CS_HI	After the execution of instructions: write enable, erase, erase suspend and erase resume, the QSPI_CS remains high for at least this number of QSPI_SCK clock cycles.	0x0
9:8	R/W	QSPIC_EAD_TX_MD	The mode of the SPI Bus during the address phase of the erase instruction 0x0: Single SPI	0x0

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Bit	Mode	Symbol	Description	Reset
			0x1: Dual 0x2: Quad 0x3: Reserved	
7:6	R/W	QSPIC_RES_TX_MD	The mode of the SPI Bus during the transmission of the resume instruction 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
5:4	R/W	QSPIC_SUS_TX_MD	The mode of the SPI Bus during the transmission of the suspend instruction. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
3:2	R/W	QSPIC_WEN_TX_MD	The mode of the SPI Bus during the transmission of the write enable instruction. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
1:0	R/W	QSPIC_ERS_TX_MD	The mode of the SPI Bus during the instruction phase of the erase instruction 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0

Table 1079: QSPIC2_BURSTBRK_REG (0x26000030)

Bit	Mode	Symbol	Description	Reset
31:21	-	-	Reserved	0x0
20	R/W	QSPIC_SEC_HF_DS	Disable output during the transmission of the second half (QSPIC_BRK_WRD[3:0]). Setting this bit is only useful if QSPIC_BRK_EN =1 and QSPIC_BRK_SZ= 1. 0: The controller drives the SPI bus during the transmission of the QSPIC_BRK_WRD[3:0]. 1: The controller leaves the SPI bus in Hi-Z during the transmission of the QSPIC_BRK_WORD[3:0].	0x0
19:18	R/W	QSPIC_BRK_TX_MD	The mode of the SPI Bus during the transmission of the read break sequence. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
17	R/W	QSPIC_BRK_SZ	The size of the read break sequence. 0: One byte (Send QSPIC_BRK_WRD[15:8])	0x0

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Bit	Mode	Symbol	Description	Reset
			1: Two bytes (Send QSPIC_BRK_WRD[15:0])	
16	R/W	QSPIC_BRK_EN	Controls the application of a special command (read break sequence) that is used in order to force the device to abandon the continuous read mode. 0: The special command is not applied 1: The special command is applied This special command is applied by the controller to the external device under the following conditions: - the controller is in Auto mode - the QSPIC_INST_MD = 1 - the previous command that has been applied in the external device was read - the controller want to apply to the external device a command different than the read.	0x0
15:0	R/W	QSPIC_BRK_WRD	This is the value of a special command (read break sequence) that is applied by the controller to the external memory device, in order to force the memory device to abandon the continuous read mode.	0x0

Table 1080: QSPIC2_STATUSCMD_REG (0x26000034)

Bit	Mode	Symbol	Description	Reset
31:23	-	-	Reserved	0x0
22	R/W	QSPIC_STSDLY_SEL	Defines the timer which is used to count the delay that it has to wait before to read the FLASH Status Register, after an erase or an erase resume command. 0: The delay is controlled by the QSPIC_RESSTS_DLY which counts on the qspi clock. 1: The delay is controlled by the QSPIC_RESSUS_DLY which counts on the 288 kHz clock.	0x0
21:16	R/W	QSPIC_RESSTS_DLY	Defines a timer that counts the minimum required delay between the reading of the status register and of the previous erase or erase resume instruction. 0x00: Dont wait. The controller starts to reading the Flash memory status register immediately. 0x01..0x3F: The controller waits for at least this number of QSPI_CLK cycles and afterwards it starts to reading the Flash memory status register. The timer starts to count after the end of the previous erase or erase resume command. The actual timer that will be used by the controller before the reading of the Flash memory status register is defined by the QSPIC_STSDLY_SEL.	0x0
15	R/W	QSPIC_BUSY_VAL	Defines the value of the Busy bit which means that the flash is busy.	0x0

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Bit	Mode	Symbol	Description	Reset
			0: The flash is busy when the Busy bit is equal to 0. 1: The flash is busy when the Busy bit is equal to 1.	
14:12	R/W	QSPIC_BUSY_POS	Defines the bit of the Flash status register which represents the Busy bit (0x7 - 0x0).	0x0
11:10	R/W	QSPIC_RSTAT_RX_MD	The mode of the SPI Bus during the reception phase of the read status instruction, where the value of status register is retrieved. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
9:8	R/W	QSPIC_RSTAT_TX_MD	The mode of the SPI Bus during the instruction phase of the read status instruction. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
7:0	R/W	QSPIC_RSTAT_INST	The code value of the read status instruction. It is transmitted during the instruction phase of the read status instruction.	0x0

Table 1081: QSPIC2_CHCKERASE_REG (0x26000038)

Bit	Mode	Symbol	Description	Reset
31:0	W	QSPIC_CHCKERASE	Writing any value to this register during erasing, forces the controller to read the flash memory status register. Depending on the value of the Busy bit, it updates the QSPIC_ERASE_EN. This register has meaning only when the controller is in Auto mode and there is an erase in progress (QSPIC_ERASE_EN =1). It has no meaning when the external device is a serial SRAM.	0x0

Table 1082: QSPIC2_GP_REG (0x2600003C)

Bit	Mode	Symbol	Description	Reset
4:3	R/W	QSPIC_PADS_SLEW	QSPI pads slew rate control. Indicative values under certain conditions: 0x0 : Rise=1.7 V/ns, Fall=1.9 V/ns (weak) 0x1 : Rise=2.0 V/ns, Fall=2.3 V/ns 0x2 : Rise=2.3 V/ns, Fall=2.6 V/ns 0x3 : Rise=2.4 V/ns, Fall=2.7 V/ns (strong) Conditions: FLASH pin capacitance 6 pF, Vcc = 1.8 V, T = 25 °C and Idrive = 16 mA	0x0
2:1	R/W	QSPIC_PADS_DRV	QSPI pads drive current 0x0 : 4 mA 0x1 : 8 mA	0x0

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Bit	Mode	Symbol	Description	Reset
			0x2 : 12 mA 0x3 : 16 mA	
0	R/W	-	Reserved	0x0

Table 1083: QSPIC2_AWRITECMD_REG (0x26000040)

Bit	Mode	Symbol	Description	Reset
31:19	-	-	Reserved	0x0
18:14	R/W	QSPIC_WR_CS_HIGH_MIN	After the execution of the write command, the QSPI_CS remains high for at least this number of QSPI_SCK clock cycles.	0x0
13:12	R/W	QSPIC_WR_DAT_TX_MD	The mode of the SPI Bus during the data phase of the write command. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
11:10	R/W	QSPIC_WR_ADR_TX_MD	The mode of the SPI Bus during the adress phase of the write command. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
9:8	R/W	QSPIC_WR_INST_TX_MD	The mode of the SPI Bus during the instruction phase of the write command. 0x0: Single SPI 0x1: Dual 0x2: Quad 0x3: Reserved	0x0
7:0	R/W	QSPIC_WR_INST	This is the value of the instruction that is used, in order to be programmed the external SRAM device.	0x0

Table 1084: QSPIC2_MEMBLEN_REG (0x26000044)

Bit	Mode	Symbol	Description	Reset
31:14	-	-	Reserved	0x0
13:4	R/W	QSPIC_T_CEM_CC	Defines the maximum allowed time tCEM for which the QSPIC_CS can stay active (QSPI_CS=0). It has meaning only when QSPIC_T_CEM_EN is equal to 1. See also the description of the QSPIC_T_CEM_EN for more details. The tCEM is expressed in number of qspi clock cycles and can be calculated as follows : tCEM / (qspi_clock_period)	0x0

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Bit	Mode	Symbol	Description	Reset
			If the result of the above equation is higher than 0x3FF, use the value 0x3FF.	
3	R/W	QSPIC_T_CEM_EN	This bit enables the controlling of the maximum time tCEM for which the QSPI_CS remains active. It has meaning only when the Auto mode is active (QSPIC_AUTO_MD=1) and the external device is a serial SRAM (QSPIC_SRAM_EN=1). In the case where the external device is a serial Flash (QSPIC_SRAM_EN=0) or the controller is in Manual mode (QSPIC_AUTO_MD=0), this field has no any effect. This feature is usefull in the case where the external serial device is a dynamic RAM that requires refresh. If the refresh is applied only when the device is in the idle state (QSPI_CS = 1), the time for which the device remains in the active state (QSPI_CS = 0) should be limited by a maximum threshold. 0:There is no any constraint regarding the maximum allowed time for which the QSPI_CS can stay active. This is the case also when QSPIC_SRAM_EN=0 or QSPIC_AUTO_MD=0. 1:There is a maximum allowed time interval tCEM for which the QSPI_CS can stay active during a burst access (for reading or writting of data). For the controller this is considered as equal to QSPIC_T_CEM_CC x qspi_clock_period. In the case where the data transfer requires the QSPI_CS to stays active for more than QSPIC_T_CEM_CC qspi clock cycles, the QSPI controller splits the access on the SPI bus in more than one bursts, by inserting inactive periods (QSPI_CS = 0) between them. This will cost extra clock cycles for the realization of the original acceess, due to the additional commands that are required in the SPI bus. The value in the QSPIC_T_CEM_CC should be updated every time where the frequency of the qspi clock is modified. The qspi clock frequency should not be decreased more than a lowest frequency. This is the lowest frequency that enables the be performed a 32-bit word read and write access, without violating the tCEM timing requirement (the QSPI controller allows to be performed at least the transferring of one beat of the requested burst, independent of the QSPIC_T_CEM_CC limit).	0x0
2:0	R/W	QSPIC_MEMBLEN	In this register is defined the expected behavior of the external memory device regarding the length of a burst operation : 0x0: The external memory device is capable to implement incremental burst of unspecified length. 0x1: The external memory device implements a wrapping burst of length 4 bytes.	0x0

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Bit	Mode	Symbol	Description	Reset
			0x2: The external memory device implements a wrapping burst of length 8 bytes. 0x3: The external memory device implements a wrapping burst of length 16 bytes. 0x4: The external memory device implements a wrapping burst of length 32 bytes. 0x5: The external memory device implements a wrapping burst of length 64 bytes. 0x6 - 0x7 : Reserved This setting is used by the QSPI controller when the Auto mode is enabled (QSPIC_AUTO_MD=1), in order to handle the various burst requests of the AHB bus, in respect of the requirements of the external memory device. The external memory device may need to be configured by applying special instruction, in order to be defined the kind of the burst operation. This can be implemented by applying this special instruction with the QSPI controller in Manual mode (QSPIC_AUTO_MD=1). Refer to the datasheet of the external device for more information.	

44.26 Real Time Clock Registers

Table 1085: Register map RTC

Address	Register	Description
0x50000800	RTC_CONTROL_REG	RTC Control Register
0x50000804	RTC_HOUR_MODE_REG	RTC Hour Mode Register
0x50000808	RTC_TIME_REG	RTC Time Register
0x5000080C	RTC_CALENDAR_REG	RTC Calendar Register
0x50000810	RTC_TIME_ALARM_REG	RTC Time Alarm Register
0x50000814	RTC_CALENDAR_ALARM_REG	RTC Calendar Alram Register
0x50000818	RTC_ALARM_ENABLE_REG	RTC Alarm Enable Register
0x5000081C	RTC_EVENT_FLAGS_REG	RTC Event Flags Register
0x50000820	RTC_INTERRUPT_ENABLE_REG	RTC Interrupt Enable Register
0x50000824	RTC_INTERRUPT_DISABLE_REG	RTC Interrupt Disable Register
0x50000828	RTC_INTERRUPT_MASK_REG	RTC Interrupt Mask Register
0x5000082C	RTC_STATUS_REG	RTC Status Register

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Address	Register	Description
0x50000830	RTC_KEEP_RTC_REG	RTC Keep RTC Register
0x50000880	RTC_EVENT_CTRL_REG	RTC Event Control Register
0x50000888	RTC_PDC_EVENT_PERIOD_REG	RTC PDC Event Period Register
0x5000088C	RTC_PDC_EVENT_CLEAR_REG	RTC PDC Event Clear Register
0x50000894	RTC_PDC_EVENT_CNT_REG	RTC PDC Event Counter Register

Table 1086: RTC_CONTROL_REG (0x50000800)

Bit	Mode	Symbol	Description	Reset
1	R/W	RTC_CAL_DISABLE	When this field is set high the RTC stops incrementing the calendar value.	0x1
0	R/W	RTC_TIME_DISABLE	When this field is set high the RTC stops incrementing the time value.	0x1

Table 1087: RTC_HOUR_MODE_REG (0x50000804)

Bit	Mode	Symbol	Description	Reset
0	R/W	RTC_HMS	When this field is set high the RTC operates in 12 hour clock mode; otherwise, times are in 24 hour clock format.	0x0

Table 1088: RTC_TIME_REG (0x50000808)

Bit	Mode	Symbol	Description	Reset
31	R/W	RTC_TIME_CH	The value in this register has altered since last read. Read and clear.	0x0
30	R/W	RTC_TIME_PM	In 12 hour clock mode, indicates PM when set.	0x0
29:28	R/W	RTC_TIME_HR_T	Hours tens. Represented in BCD digit (0-2).	0x0
27:24	R/W	RTC_TIME_HR_U	Hours units. Represented in BCD digit (0-9).	0x0
23	-	-	Reserved	0x0
22:20	R/W	RTC_TIME_M_T	Minutes tens. Represented in BCD digit (0-5).	0x0
19:16	R/W	RTC_TIME_M_U	Minutes units. Represented in BCD digit (0-9).	0x0
15	-	-	Reserved	0x0
14:12	R/W	RTC_TIME_S_T	Seconds tens. Represented in BCD digit (0-9).	0x0
11:8	R/W	RTC_TIME_S_U	Seconds units. Represented in BCD digit (0-9).	0x0
7:4	R/W	RTC_TIME_H_T	Hundredths of a second tens. Represented in BCD digit (0-9).	0x0
3:0	R/W	RTC_TIME_H_U	Hundredths of a second units. Represented in BCD digit (0-9).	0x0

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Table 1089: RTC_CALENDAR_REG (0x5000080C)

Bit	Mode	Symbol	Description	Reset
31	R/W	RTC_CAL_CH	The value in this register has altered since last read. Read and clear	0x0
30	-	-	Reserved	0x0
29:28	R/W	RTC_CAL_C_T	Century tens. Represented in BCD digit (1-2).	0x2
27:24	R/W	RTC_CAL_C_U	Century units. Represented in BCD digit (0-9).	0x0
23:20	R/W	RTC_CAL_Y_T	Year tens. Represented in BCD digit (0-9).	0x0
19:16	R/W	RTC_CAL_Y_U	Year units. Represented in BCD digit (0-9).	0x0
15:14	-	-	Reserved	0x0
13:12	R/W	RTC_CAL_D_T	Date tens. Represented in BCD digit (0-3).	0x0
11:8	R/W	RTC_CAL_D_U	Date units. Represented in BCD digit (0-9).	0x1
7	R/W	RTC_CAL_M_T	Month tens. Represented in BCD digit (0-1).	0x0
6:3	R/W	RTC_CAL_M_U	Month units. Represented in BCD digit (0-9).	0x1
2:0	R/W	RTC_DAY	Day of the week (arbitrary) units. Represented in BCD digit (0-7).	0x7

Table 1090: RTC_TIME_ALARM_REG (0x50000810)

Bit	Mode	Symbol	Description	Reset
31	-	-	Reserved	0x0
30	R/W	RTC_TIME_PM	In 12 hour clock mode, indicates PM when set.	0x0
29:28	R/W	RTC_TIME_HR_T	Hours tens. Represented in BCD digit (0-2).	0x0
27:24	R/W	RTC_TIME_HR_U	Hours units. Represented in BCD digit (0-9).	0x0
23	-	-	Reserved	0x0
22:20	R/W	RTC_TIME_M_T	Minutes tens. Represented in BCD digit (0-5).	0x0
19:16	R/W	RTC_TIME_M_U	Minutes units. Represented in BCD digit (0-9).	0x0
15	-	-	Reserved	0x0
14:12	R/W	RTC_TIME_S_T	Seconds tens. Represented in BCD digit (0-9).	0x0
11:8	R/W	RTC_TIME_S_U	Seconds units. Represented in BCD digit (0-9).	0x0
7:4	R/W	RTC_TIME_H_T	Hundredths of a second tens. Represented in BCD digit (0-9).	0x0
3:0	R/W	RTC_TIME_H_U	Hundredths of a second units. Represented in BCD digit (0-9).	0x0

Table 1091: RTC_CALENDAR_ALARM_REG (0x50000814)

Bit	Mode	Symbol	Description	Reset
31:14	R/W	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
13:12	R/W	RTC_CAL_D_T	Date tens. Represented in BCD digit (0-3).	0x0
11:8	R/W	RTC_CAL_D_U	Date units. Represented in BCD digit (0-9).	0x0
7	R/W	RTC_CAL_M_T	Month tens. Represented in BCD digit (0-1).	0x0
6:3	R/W	RTC_CAL_M_U	Month units. Represented in BCD digit (0-9).	0x0
2:0	-	-	Reserved	0x0

Table 1092: RTC_ALARM_ENABLE_REG (0x50000818)

Bit	Mode	Symbol	Description	Reset
5	R/W	RTC_ALARM_MNTH_EN	Alarm on month enable. Enable to trigger alarm when data specified in Calendar Alarm Register (M_T and M_U) has been reached.	0x0
4	R/W	RTC_ALARM_DATE_EN	Alarm on date enable. Enable to trigger alarm when data specified in Calendar Alarm Register (D_T and D_U) has been reached.	0x0
3	R/W	RTC_ALARM_HOUR_EN	Alarm on hour enable. Enable to trigger alarm when data specified in Time Alarm Register (PM, HR_T and HR_U) has been reached.	0x0
2	R/W	RTC_ALARM_MIN_EN	Alarm on minute enable. Enable to trigger alarm when data specified in Time Alarm Register (M_T and M_U) has been reached.	0x0
1	R/W	RTC_ALARM_SEC_EN	Alarm on second enable. Enable to trigger alarm when data specified in Time Alarm Register (S_T and S_U) has been reached.	0x0
0	R/W	RTC_ALARM_HOS_EN	Alarm on hundredths of a second enable. Enable to trigger alarm when data specified in Time Alarm Register (H_T and H_U) has been reached.	0x0

Table 1093: RTC_EVENT_FLAGS_REG (0x5000081C)

Bit	Mode	Symbol	Description	Reset
6	R	RTC_EVENT_ALRM	Alarm event flag. Indicate that alarm event occurred since the last reset.	0x0
5	R	RTC_EVENT_MNTH	Month rolls over event flag. Indicate that month rolls over event occurred since the last reset.	0x0
4	R	RTC_EVENT_DATE	Date rolls over event flag. Indicate that date rolls over event occurred since the last reset.	0x0
3	R	RTC_EVENT_HOUR	Hour rolls over event flag. Indicate that hour rolls over event occurred since the last reset.	0x0
2	R	RTC_EVENT_MIN	Minute rolls over event flag. Indicate that minute rolls over event occurred since the last reset.	0x0
1	R	RTC_EVENT_SEC	Second rolls over event flag. Indicate that second rolls over event occurred since the last reset.	0x0
0	R	RTC_EVENT_HOS	Hundredths of a second event flag. Indicate that hundredths of a second rolls over event occurred since the last reset.	0x0

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Table 1094: RTC_INTERRUPT_ENABLE_REG (0x50000820)

Bit	Mode	Symbol	Description	Reset
6	W	RTC_ALRM_INT_EN	Interrupt on alarm enable. Enable to issue the interrupt when alarm event occurred.	0x0
5	W	RTC_MNTH_INT_EN	Interrupt on month enable. Enable to issue the interrupt when month event occurred.	0x0
4	W	RTC_DATE_INT_EN	Interrupt on date enable. Enable to issue the interrupt when date event occurred.	0x0
3	W	RTC_HOUR_INT_EN	Interrupt on hour enable. Enable to issue the interrupt when hour event occurred.	0x0
2	W	RTC_MIN_INT_EN	Interrupt on minute enable. Enable to issue the interrupt when minute event occurred.	0x0
1	W	RTC_SEC_INT_EN	Interrupt on second enable. Enable to issue the interrupt when second event occurred.	0x0
0	W	RTC_HOS_INT_EN	Interrupt on hundredths of a second enable. Enable to issue the interrupt when hundredths of a second event occurred.	0x0

Table 1095: RTC_INTERRUPT_DISABLE_REG (0x50000824)

Bit	Mode	Symbol	Description	Reset
6	W	RTC_ALRM_INT_DIS	Interrupt on alarm disable. Disable to issue the interrupt when alarm event occurred.	0x0
5	W	RTC_MNTH_INT_DIS	Interrupt on month disable. Disable to issue the interrupt when month event occurred.	0x0
4	W	RTC_DATE_INT_DIS	Interrupt on date disable. Disable to issue the interrupt when date event occurred.	0x0
3	W	RTC_HOUR_INT_DIS	IInterrupt on hour disable. Disable to issue the interrupt when hour event occurred.	0x0
2	W	RTC_MIN_INT_DIS	Interrupt on minute disable. Disable to issue the interrupt when minute event occurred.	0x0
1	W	RTC_SEC_INT_DIS	Interrupt on second disable. Disable to issue the interrupt when second event occurred.	0x0
0	W	RTC_HOS_INT_DIS	Interrupt on hundredths of a second disable. Disable to issue the interrupt when hundredths of a second event occurred.	0x0

Table 1096: RTC_INTERRUPT_MASK_REG (0x50000828)

Bit	Mode	Symbol	Description	Reset
6	R	RTC_ALRM_INT_MSK	Mask alarm interrupt. It can be cleared (set) by setting corresponding bit (ALRM) in Interrupt Enable Register (Interrupt Disable Register).	0x1
5	R	RTC_MNTH_INT_MSK	IMask month interrupt. It can be cleared (set) by setting corresponding bit (MNTH) in Interrupt Enable Register (Interrupt Disable Register).	0x1

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Bit	Mode	Symbol	Description	Reset
4	R	RTC_DATE_INT_MSK	Mask date interrupt. It can be cleared (set) by setting corresponding bit (DATE) in Interrupt Enable Register (Interrupt Disable Register).	0x1
3	R	RTC_HOUR_INT_MSK	IMask hour interrupt. It can be cleared (set) by setting corresponding bit (HOUR) in Interrupt Enable Register (Interrupt Disable Register).	0x1
2	R	RTC_MIN_INT_MSK	IMask minute interrupt. It can be cleared (set) by setting corresponding bit (MIN) in Interrupt Enable Register (Interrupt Disable Register).	0x1
1	R	RTC_SEC_INT_MSK	IMask second interrupt. It can be cleared (set) by setting corresponding bit (SEC) in Interrupt Enable Register (Interrupt Disable Register).	0x1
0	R	RTC_HOS_INT_MSK	Mask hundredths of a second interrupt. It can be cleared (set) by setting corresponding bit (HOS) in Interrupt Enable Register (Interrupt Disable Register).	0x1

Table 1097: RTC_STATUS_REG (0x5000082C)

Bit	Mode	Symbol	Description	Reset
3	R	RTC_VALID_CAL_ALM	Valid Calendar Alarm. If cleared then indicates that invalid entry occurred when writing to Calendar Alarm Register.	0x1
2	R	RTC_VALID_TIME_ALM	Valid Time Alarm. If cleared then indicates that invalid entry occurred when writing to Time Alarm Register.	0x1
1	R	RTC_VALID_CAL	Valid Calendar. If cleared then indicates that invalid entry occurred when writing to Calendar Register.	0x1
0	R	RTC_VALID_TIME	Valid Time. If cleared then indicates that invalid entry occurred when writing to Time Register.	0x1

Table 1098: RTC_KEEP_RTC_REG (0x50000830)

Bit	Mode	Symbol	Description	Reset
0	R/W	RTC_KEEP	Keep RTC. When high, the time and calendar registers and any other registers which directly affect or are affected by the time and calendar registers are NOT reset when software reset is applied. When low, the software reset will reset every register except the keep RTC and control registers.	0x1

Table 1099: RTC_EVENT_CTRL_REG (0x50000880)

Bit	Mode	Symbol	Description	Reset
1	R/W	RTC_PDC_EVENT_EN	0 = Event to PDC is disabled. No clear any pending event 1 = Even to PDC is enabled	0x0

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Bit	Mode	Symbol	Description	Reset
0	R/W	-	Reserved	0x0

Table 1100: RTC_PDC_EVENT_PERIOD_REG (0x50000888)

Bit	Mode	Symbol	Description	Reset
12:0	R/W	RTC_PDC_EVENT_PERIOD	RTC wil send an event to PDC (if RTC_PDC_EVENT_EN=1) every (RTC_PDC_EVENT_PERIOD+1)*10ms	0x0

Table 1101: RTC_PDC_EVENT_CLEAR_REG (0x5000088C)

Bit	Mode	Symbol	Description	Reset
0	R	PDC_EVENT_CLEAR	On read, PDC event is cleared	0x0

Table 1102: RTC_PDC_EVENT_CNT_REG (0x50000894)

Bit	Mode	Symbol	Description	Reset
12:0	R	RTC_PDC_EVENT_CNT	It gives the current value of the PDC event counter (0 to RTC_PDC_EVENT_PERIOD)	0x0

44.27 Sensor Node Controller Registers

Table 1103: Register map SNC

Address	Register	Description
0x50021000	SNC_STATUS_REG	Sensor Node Status Register
0x50021004	SNC_WDOG_REG	Sensor Node Watchdog Register

Table 1104: SNC_STATUS_REG (0x50021000)

Bit	Mode	Symbol	Description	Reset
4	R	WDOG_EARLY_NOTICE	0 = Normal operation 1 = Indicates that the SNC Watchdog counter has reached the value 16, while down-counting from the value programmed. This bit is automatically cleared as soon as the Watchdog expires.	0x0
3	R	WDOG_HAS_EXPIRED	0 = Normal operation 1 = Indicates that the SNC Watchdog counter has expired	0x0
2	R	CPU_LOCKED	0 = Normal operation	0x0

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Bit	Mode	Symbol	Description	Reset
			1 = SNC CPU is locked-up. The specific bit-field is set as soon as the corresponding LOCKUP output of the processor is set.	
1	R	CPU_IDLE	0 = Normal operation 1 = SNC CPU is in idle mode, activated when the 'sleeping' bit of Cortex M0+ is set (for instance, when waiting for an interrupt).	0x0
0	R	CPU_HALTED	0 = Normal operation 1 = SNC CPU is halted	0x0

Table 1105: SNC_WDOG_REG (0x50021004)

Bit	Mode	Symbol	Description	Reset
31	R	SYS2SNC_WDOG_FREEZE	This bit-field returns a read-only copy of SET_FREEZE_REG->FRZ_SNC_WDOG value.	0x0
30	R/W	SYS2SNC_WDOG_FREEZE_DIS	If 1, it mask the SYS2SNC_WDOG_FREEZE, which is provided by SET_FREEZE_REG[FRZ_SNC_WDOG]. Setting this field to 1 can be done only by writing ones to the field SNC_WDOG_WRITE_VALID at the same time. The field can only be set to 1, so it can be set during the initilization and it will not change during the reloadings. The asynchronous reset is connected to the SNC CPU reset.	0x0
29	R/W	SNC_WDOG_EXPIRE	This bit automatically set to 1 as soon as SNC_WDOG_CNT = 0, causing: a) The SNC_WDOG_CNT to start down-counting again, now beginning from the value of 16. b) The assertion of SNC_STATUS_REG[WDOG_HAS_EXPIRED], indicating that the SNC Watchdog has expired. If SW writes SNC_WDOG_EXPIRE = 0 and SNC_WDOG_CNT = 0, at the next WDOG clock cycle the SNC_WDOG_EXPIRE will automatically be set to 1. If SW writes SNC_WDOG_EXPIRE = 1 and SNC_WDOG_CNT = 0, at the next WDOG clock cycle SNC_WDOG_SYS_RST_REQ will be automatically set to 1. The SNC_WDOG_SYS_RST_REQ will reset the system and will also update the RESET_STAT_REG[SNC_WDOGRESET_STAT].	0x0
28	R	SNC_WDOG_SYS_RST_REQ	Refer to the SNC_WDOG_EXPIRE bit-field.	0x0
27	R	-	Reserved	0x0
19	R	-	Reserved	0x0
18:17	R0/W	SNC_WDOG_WRITE_VALID	To allow a write of any remaining fields, this value must also be written simultaneously with the value 3 and perform 32-bit write access. Reading this field will always return 0..	0x0

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Bit	Mode	Symbol	Description	Reset
16	R	-	Reserved	0x0
15:13	R	-	Reserved	0x0
12:0	R/W	SNC_WDOG_CNT	Provides access to the counter, which counts down every 10.24 ms. FW should reload the WDOG counter by writing the value (SNC_WDOG_CNT | SNC_WDOG_WRITE_VALID) to SNC_WDOG_REG, which means, write can be done only by writing SNC_WDOG_WRITE_VALID with 1s at the same time. The counter will start counting immediately after the power-up of the power domain and will reset on every SNC CPU reset.	0x1FFF

44.28 SPI Controller Registers

Table 1106: Register map SPI

Address	Register	Description
0x50020300	SPI_CTRL_REG	Spi control register
0x50020304	SPI_CONFIG_REG	Spi control register
0x50020308	SPI_CLOCK_REG	Spi clock register
0x5002030C	SPI_FIFO_CONFIG_REG	Spi fifo configuration register
0x50020310	SPI_IRQ_MASK_REG	Spi interrupt mask register
0x50020314	SPI_STATUS_REG	Spi status register
0x50020318	SPI_FIFO_STATUS_REG	SPI RX/TX fifo status register
0x5002031C	SPI_FIFO_READ_REG	Spi RX fifo read register
0x50020320	SPI_FIFO_WRITE_REG	Spi TX fifo wtite register
0x50020324	SPI_CS_CONFIG_REG	Spi cs configuration register
0x5002032C	SPI_TXBUFFER_FORCE_REG	SPI TX buffer force low value
0x50020400	SPI2_CTRL_REG	Spi control register
0x50020404	SPI2_CONFIG_REG	Spi control register
0x50020408	SPI2_CLOCK_REG	Spi clock register
0x5002040C	SPI2_FIFO_CONFIG_REG	Spi fifo configuration register
0x50020410	SPI2_IRQ_MASK_REG	Spi interrupt mask register
0x50020414	SPI2_STATUS_REG	Spi status register
0x50020418	SPI2_FIFO_STATUS_REG	SPI RX/TX fifo status register

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Address	Register	Description
0x5002041C	SPI2_FIFO_READ_REG	Spi RX fifo read register
0x50020420	SPI2_FIFO_WRITE_REG	Spi TX fifo wtite register
0x50020424	SPI2_CS_CONFIG_REG	Spi cs configuration register
0x5002042C	SPI2_TXBUFFER_FORCE_REG	SPI TX buffer force low value
0x51000200	SPI3_CTRL_REG	Spi control register
0x51000204	SPI3_CONFIG_REG	Spi control register
0x51000208	SPI3_CLOCK_REG	Spi clock register
0x5100020C	SPI3_FIFO_CONFIG_REG	Spi fifo configuration register
0x51000210	SPI3_IRQ_MASK_REG	Spi interrupt mask register
0x51000214	SPI3_STATUS_REG	Spi status register
0x51000218	SPI3_FIFO_STATUS_REG	SPI RX/TX fifo status register
0x5100021C	SPI3_FIFO_READ_REG	Spi RX fifo read register
0x51000220	SPI3_FIFO_WRITE_REG	Spi TX fifo wtite register
0x51000224	SPI3_CS_CONFIG_REG	Spi cs configuration register
0x5100022C	SPI3_TXBUFFER_FORCE_REG	SPI TX buffer force low value

Table 1107: SPI_CTRL_REG (0x50020300)

Bit	Mode	Symbol	Description	Reset
7	R/W	SPI_SWAP_BYTES	0 = normal operation 1 = LSB and MSB are swaped in APB interface In case of 8-bit spi interface, DMA/SPI can be configured in 16-bit mode to off load the bus. Enabling SPI_SWAP_BYTES bytes will read/wrte correctly	0x0
6	R/W	SPI_CAPTURE_AT_NEXT_EDGE	0 = SPI captures data at correct clock edge 1 = SPI captures data at next clock edge. (only for Master mode and high clock)	0x0
5	R/W	SPI_FIFO_RESET	0 = Fifo normal operation 1 = Fifo in reset state	0x0
4	R/W	SPI_DMA_RX_EN	Applicable only when SPI_RX_EN=1 0 = No DMA request for RX 1 = DMA request when SPI_STATUS_RX_FULL=1	0x0

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Bit	Mode	Symbol	Description	Reset
3	R/W	SPI_DMA_TX_EN	Applicable only when SPI_TX_EN=1 0 = No DMA request for TX 1 = DMA request when SPI_STATUS_TX_EMPTY=1	0x0
2	R/W	SPI_RX_EN	0 = RX path is disabled 1 = RX path is enabled Note: if spi mode=1 or spi mode=3 readonly is not supported	0x0
1	R/W	SPI_TX_EN	0 = TX path is disabled 1 = TX path is enabled	0x0
0	R/W	SPI_EN	0 = SPI module is disable 1 = SPI module is enable	0x0

Table 1108: SPI_CONFIG_REG (0x50020304)

Bit	Mode	Symbol	Description	Reset
7	R/W	SPI_SLAVE_EN	0 = SPI module master mode 1 = SPI module slave mode	0x0
6:2	R/W	SPI_WORD_LENGTH	Define the spi word length = 1+ SPI_WORD_LENGTH (range 4 to 32) Note: should be changed with SPI_EN=0	0x0
1:0	R/W	SPI_MODE	Define the spi mode (CPOL, CPHA) 0 = new data on falling, capture on rising, clk low in idle state 1 = new data on rising, capture on falling, Clk low in idle state 2 = new data on rising, capture on falling, Clk high in idle state 3 = new data on falling, capture on rising Clk high in idle state	0x0

Table 1109: SPI_CLOCK_REG (0x50020308)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	SPI_CLK_DIV	Applicable only in master mode Defines the spi clock frequency in master only mode SPI_CLK = module_clk / 2*(SPI_CLK_DIV+1) when SPI_CLK_DIV not 0x7F if SPI_CLK_DIV=0x7F then SPI_CLK=module_clk	0x0

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Table 1110: SPI_FIFO_CONFIG_REG (0x5002030C)

Bit	Mode	Symbol	Description	Reset
15:8	R/W	SPI_RX_TL	Receive FIFO threshold level in bytes. Control the level of bytes in fifo that triggers the RX_FULL interrupt. IRQ is occurred when fifo level is more or equal to SPI_RX_TL+1. Valid FIFO level is from 0 to 32	0x0
7:0	R/W	SPI_TX_TL	Transmit FIFO threshold level in bytes. Control the level of bytes in fifo that triggers the TX_EMPTY interrupt. IRQ is occurred when fifo level is less or equal to SPI_TX_TL. Valid FIFO level is from 0 to 32	0x0

Table 1111: SPI_IRQ_MASK_REG (0x50020310)

Bit	Mode	Symbol	Description	Reset
1	R/W	SPI_IRQ_MASK_RX_FULL	0 = FIFO RX full irq is masked 1 = FIFO RX full irq is enabled	0x0
0	R/W	SPI_IRQ_MASK_TX_EMPTY	0 = FIFO TX empty irq is masked 1 = FIFO TX empy irq is enabled	0x0

Table 1112: SPI_STATUS_REG (0x50020314)

Bit	Mode	Symbol	Description	Reset
1	R	SPI_STATUS_RX_FULL	Auto clear 0 = RX fifo level is less than SPI_RX_TL+1 1 = RX fifo level is more or equal to SPI_RX_TL+1	0x0
0	R	SPI_STATUS_TX_EMPTY	Auto clear 0 = TX fifo level is larger than SPI_TX_TL 1 = TX fifo level is less or equal to SPI_TX_TL	0x1

Table 1113: SPI_FIFO_STATUS_REG (0x50020318)

Bit	Mode	Symbol	Description	Reset
15	R	SPI_TRANSACTION_ACTIVE	In master mode 0 = spi transaction is inactive 1 = spi transaction is active	0x0
14	R	SPI_RX_FIFO_OVFL	When 1, receive data is not written to fifo because fifo was full and interrupt is generated. It clears with SPI_CTRL_REG.SPI_FIFO_RESET	0x0
13	R	SPI_STATUS_TX_FULL	0 = TX fifo is not full 1 = TX fifo is full	0x0

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Bit	Mode	Symbol	Description	Reset
12	R	SPI_STATUS_RX_EMPTY	0 = RX fifo is not empty 1 = RX fifo is empty	0x1
11:6	R	SPI_TX_FIFO_LEVEL	Gives the number of bytes in TX fifo	0x0
5:0	R	SPI_RX_FIFO_LEVEL	Gives the number of bytes in RX fifo	0x0

Table 1114: SPI_FIFO_READ_REG (0x5002031C)

Bit	Mode	Symbol	Description	Reset
31:0	R	SPI_FIFO_READ	Read from RX fifo. Read access is permit only if SPI_RX_FIFO_EMPTY=0.	0x0

Table 1115: SPI_FIFO_WRITE_REG (0x50020320)

Bit	Mode	Symbol	Description	Reset
31:0	R0/W	SPI_FIFO_WRITE	Write to TX fifo. Write access is permit only if SPI_TX_FIFO_FULL is 0	0x0

Table 1116: SPI_CS_CONFIG_REG (0x50020324)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	SPI_CS_SELECT	Control the cs output in master mode 0 = none slave device selected 1 = selected slave device connected to GPIO with FUNC_MODE=SPI_CS0 2 = selected slave device connected to GPIO with FUNC_MODE=SPI_CS1 4 = selected slave device connected to GPIO with FUNC_MODE=GPIO	0x0

Table 1117: SPI_TXBUFFER_FORCE_REG (0x5002032C)

Bit	Mode	Symbol	Description	Reset
31:0	W	SPI_TXBUFFER_FORCE	Write directly the tx buffer . It must to be used only in slave mode	0x0

Table 1118: SPI2_CTRL_REG (0x50020400)

Bit	Mode	Symbol	Description	Reset
7	R/W	SPI_SWAP_BYTES	0 = normal operation 1 = LSB and MSB are swaped in APB interface	0x0

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Bit	Mode	Symbol	Description	Reset
			In case of 8-bit spi interface, DMA/SPI can be configured in 16-bit mode to off load the bus. Enabling SPI_SWAP_BYTES bytes will read/wrte correctly	
6	R/W	SPI_CAPTURE_AT_NEXT_EDGE	0 = SPI captures data at correct clock edge 1 = SPI captures data at next clock edge. (only for Master mode and high clock)	0x0
5	R/W	SPI_FIFO_RESET	0 = Fifo normal operation 1 = Fifo in reset state	0x0
4	R/W	SPI_DMA_RX_EN	Applicable only when SPI_RX_EN=1 0 = No DMA request for RX 1 = DMA request when SPI_STATUS_RX_FULL=1	0x0
3	R/W	SPI_DMA_TX_EN	Applicable only when SPI_TX_EN=1 0 = No DMA request for TX 1 = DMA request when SPI_STATUS_TX_EMPTY=1	0x0
2	R/W	SPI_RX_EN	0 = RX path is disabled 1 = RX path is enabled Note: if spi mode=1 or spi mode=3 readonly is not supported	0x0
1	R/W	SPI_TX_EN	0 = TX path is disabled 1 = TX path is enabled	0x0
0	R/W	SPI_EN	0 = SPI module is disable 1 = SPI module is enable	0x0

Table 1119: SPI2_CONFIG_REG (0x50020404)

Bit	Mode	Symbol	Description	Reset
7	R/W	SPI_SLAVE_EN	0 = SPI module master mode 1 = SPI module slave mode	0x0
6:2	R/W	SPI_WORD_LENGTH	Define the spi word length = 1+ SPI_WORD_LENGTH (range 4 to 32) Note: should be changed with SPI_EN=0	0x0
1:0	R/W	SPI_MODE	Define the spi mode (CPOL, CPHA) 0 = new data on falling, capture on rising, clk low in idle state 1 = new data on rising, capture on falling, Clk low in idle state 2 = new data on rising, capture on falling, Clk high in idle state 3 = new data on falling, capture on rising Clk high in idle state	0x0

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Table 1120: SPI2_CLOCK_REG (0x50020408)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	SPI_CLK_DIV	Applicable only in master mode Defines the spi clock frequency in master only mode SPI_CLK = module_clk / 2*(SPI_CLK_DIV+1) when SPI_CLK_DIV not 0x7F if SPI_CLK_DIV=0x7F then SPI_CLK=module_clk	0x0

Table 1121: SPI2_FIFO_CONFIG_REG (0x5002040C)

Bit	Mode	Symbol	Description	Reset
15:8	R/W	SPI_RX_TL	Receive FIFO threshold level in bytes. Control the level of bytes in fifo that triggers the RX_FULL interrupt. IRQ is occurred when fifo level is more or equal to SPI_RX_TL+1. Valid FIFO level is from 0 to 32	0x0
7:0	R/W	SPI_TX_TL	Transmit FIFO threshold level in bytes. Control the level of bytes in fifo that triggers the TX_EMPTY interrupt. IRQ is occurred when fifo level is less or equal to SPI_TX_TL. Valid FIFO level is from 0 to 32	0x0

Table 1122: SPI2_IRQ_MASK_REG (0x50020410)

Bit	Mode	Symbol	Description	Reset
1	R/W	SPI_IRQ_MASK_RX_FULL	0 = FIFO RX full irq is masked 1 = FIFO RX full irq is enabled	0x0
0	R/W	SPI_IRQ_MASK_TX_EMPTY	0 = FIFO TX empty irq is masked 1 = FIFO TX empy irq is enabled	0x0

Table 1123: SPI2_STATUS_REG (0x50020414)

Bit	Mode	Symbol	Description	Reset
1	R	SPI_STATUS_RX_FULL	Auto clear 0 = RX fifo level is less than SPI_RX_TL+1 1 = RX fifo level is more or equal to SPI_RX_TL+1	0x0
0	R	SPI_STATUS_TX_EMPTY	Auto clear 0 = TX fifo level is larger than SPI_TX_TL 1 = TX fifo level is less or equal to SPI_TX_TL	0x1

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Table 1124: SPI2_FIFO_STATUS_REG (0x50020418)

Bit	Mode	Symbol	Description	Reset
15	R	SPI_TRANSACTION_ACTIVE	In master mode 0 = spi transaction is inactive 1 = spi transaction is active	0x0
14	R	SPI_RX_FIFO_OVFL	When 1, receive data is not written to fifo because fifo was full and interrupt is generated. It clears with SPI_CTRL_REG.SPI_FIFO_RESET	0x0
13	R	SPI_STATUS_TX_FULL	0 = TX fifo is not full 1 = TX fifo is full	0x0
12	R	SPI_STATUS_RX_EMPTY	0 = RX fifo is not empty 1 = RX fifo is empty	0x1
11:6	R	SPI_TX_FIFO_LEVEL	Gives the number of bytes in TX fifo	0x0
5:0	R	SPI_RX_FIFO_LEVEL	Gives the number of bytes in RX fifo	0x0

Table 1125: SPI2_FIFO_READ_REG (0x5002041C)

Bit	Mode	Symbol	Description	Reset
31:0	R	SPI_FIFO_READ	Read from RX fifo. Read access is permit only if SPI_RX_FIFO_EMPTY=0.	0x0

Table 1126: SPI2_FIFO_WRITE_REG (0x50020420)

Bit	Mode	Symbol	Description	Reset
31:0	R0/W	SPI_FIFO_WRITE	Write to TX fifo. Write access is permit only if SPI_TX_FIFO_FULL is 0	0x0

Table 1127: SPI2_CS_CONFIG_REG (0x50020424)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	SPI_CS_SELECT	Control the cs output in master mode 0 = none slave device selected 1 = selected slave device connected to GPIO with FUNC_MODE=SPI_CS0 2 = selected slave device connected to GPIO with FUNC_MODE=SPI_CS1 4 = selected slave device connected to GPIO with FUNC_MODE=GPIO	0x0

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Table 1128: SPI2_TXBUFFER_FORCE_REG (0x5002042C)

Bit	Mode	Symbol	Description	Reset
31:0	W	SPI_TXBUFFER_FORCE	Write directly the tx buffer . It must to be used only in slave mode	0x0

Table 1129: SPI3_CTRL_REG (0x51000200)

Bit	Mode	Symbol	Description	Reset
7	R/W	SPI_SWAP_BYTES	0 = normal operation 1 = LSB and MSB are swaped in APB interface In case of 8-bit spi interface, DMA/SPI can be configured in 16-bit mode to off load the bus. Enabling SPI_SWAP_BYTES bytes will read/wrte correctly	0x0
6	R/W	SPI_CAPTURE_AT_NEXT_EDGE	0 = SPI captures data at correct clock edge 1 = SPI captures data at next clock edge. (only for Master mode and high clock)	0x0
5	R/W	SPI_FIFO_RESET	0 = Fifo normal operation 1 = Fifo in reset state	0x0
4	R/W	SPI_DMA_RX_EN	Applicable only when SPI_RX_EN=1 0 = No DMA request for RX 1 = DMA request when SPI_STATUS_RX_FULL=1	0x0
3	R/W	SPI_DMA_TX_EN	Applicable only when SPI_TX_EN=1 0 = No DMA request for TX 1 = DMA request when SPI_STATUS_TX_EMPTY=1	0x0
2	R/W	SPI_RX_EN	0 = RX path is disabled 1 = RX path is enabled Note: if spi mode=1 or spi mode=3 readonly is not supported	0x0
1	R/W	SPI_TX_EN	0 = TX path is disabled 1 = TX path is enabled	0x0
0	R/W	SPI_EN	0 = SPI module is disable 1 = SPI module is enable	0x0

Table 1130: SPI3_CONFIG_REG (0x51000204)

Bit	Mode	Symbol	Description	Reset
7	R/W	SPI_SLAVE_EN	0 = SPI module master mode 1 = SPI module slave mode	0x0
6:2	R/W	SPI_WORD_LENGTH	Define the spi word length = 1+ SPI_WORD_LENGTH (range 4 to 32) Note: should be changed with SPI_EN=0	0x0

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Bit	Mode	Symbol	Description	Reset
1:0	R/W	SPI_MODE	Define the spi mode (CPOL, CPHA) 0 = new data on falling, capture on rising, clk low in idle state 1 = new data on rising, capture on falling, Clk low in idle state 2 = new data on rising, capture on falling, Clk high in idle state 3 = new data on falling, capture on rising Clk high in idle state	0x0

Table 1131: SPI3_CLOCK_REG (0x51000208)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	SPI_CLK_DIV	Applicable only in master mode Defines the spi clock frequency in master only mode SPI_CLK = module_clk / 2*(SPI_CLK_DIV+1) when SPI_CLK_DIV not 0x7F if SPI_CLK_DIV=0x7F then SPI_CLK=module_clk	0x0

Table 1132: SPI3_FIFO_CONFIG_REG (0x5100020C)

Bit	Mode	Symbol	Description	Reset
15:8	R/W	SPI_RX_TL	Receive FIFO threshold level in bytes. Control the level of bytes in fifo that triggers the RX_FULL interrupt. IRQ is occurred when fifo level is more or equal to SPI_RX_TL+1. Valid FIFO level is from 0 to 4	0x0
7:0	R/W	SPI_TX_TL	Transmit FIFO threshold level in bytes. Control the level of bytes in fifo that triggers the TX_EMPTY interrupt. IRQ is occurred when fifo level is less or equal to SPI_TX_TL. Valid FIFO level is from 0 to 4	0x0

Table 1133: SPI3_IRQ_MASK_REG (0x51000210)

Bit	Mode	Symbol	Description	Reset
1	R/W	SPI_IRQ_MASK_RX_FULL	0 = FIFO RX full irq is masked 1 = FIFO RX full irq is enabled	0x0
0	R/W	SPI_IRQ_MASK_TX_EMPTY	0 = FIFO TX empty irq is masked 1 = FIFO TX empy irq is enabled	0x0

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Table 1134: SPI3_STATUS_REG (0x51000214)

Bit	Mode	Symbol	Description	Reset
1	R	SPI_STATUS_RX_FULL	Auto clear 0 = RX fifo level is less than SPI_RX_TL+1 1 = RX fifo level is more or equal to SPI_RX_TL+1	0x0
0	R	SPI_STATUS_TX_EMPTY	Auto clear 0 = TX fifo level is larger than SPI_TX_TL 1 = TX fifo level is less or equal to SPI_TX_TL	0x1

Table 1135: SPI3_FIFO_STATUS_REG (0x51000218)

Bit	Mode	Symbol	Description	Reset
15	R	SPI_TRANSACTION_ACTIVE	In master mode 0 = spi transaction is inactive 1 = spi transaction is active	0x0
14	R	SPI_RX_FIFO_OVFL	When 1, receive data is not written to fifo because fifo was full and interrupt is generated. It clears with SPI_CTRL_REG.SPI_FIFO_RESET	0x0
13	R	SPI_STATUS_TX_FULL	0 = TX fifo is not full 1 = TX fifo is full	0x0
12	R	SPI_STATUS_RX_EMPTY	0 = RX fifo is not empty 1 = RX fifo is empty	0x1
11:6	R	SPI_TX_FIFO_LEVEL	Gives the number of bytes in TX fifo	0x0
5:0	R	SPI_RX_FIFO_LEVEL	Gives the number of bytes in RX fifo	0x0

Table 1136: SPI3_FIFO_READ_REG (0x5100021C)

Bit	Mode	Symbol	Description	Reset
31:0	R	SPI_FIFO_READ	Read from RX fifo. Read access is permit only if SPI_RX_FIFO_EMPTY=0.	0x0

Table 1137: SPI3_FIFO_WRITE_REG (0x51000220)

Bit	Mode	Symbol	Description	Reset
31:0	R0/W	SPI_FIFO_WRITE	Write to TX fifo. Write access is permit only if SPI_TX_FIFO_FULL is 0	0x0

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Table 1138: SPI3_CS_CONFIG_REG (0x51000224)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	SPI_CS_SELECT	Control the cs output in master mode 0 = none slave device selected 1 = selected slave device connected to GPIO with FUNC_MODE=SPI_CS0 2 = selected slave device connected to GPIO with FUNC_MODE=SPI_CS1 4 = selected slave device connected to GPIO with FUNC_MODE=GPIO	0x0

Table 1139: SPI3_TXBUFFER_FORCE_REG (0x5100022C)

Bit	Mode	Symbol	Description	Reset
31:0	W	SPI_TXBUFFER_FORCE	Write directly the tx buffer . It must to be used only in slave mode	0x0

44.29 Timers Registers

Table 1140: Register map TIMER

Address	Register	Description
0x50010000	TIMER_CTRL_REG	Timer control register
0x50010004	TIMER_TIMER_VAL_REG	Timer counter value
0x50010008	TIMER_STATUS_REG	Timer status register
0x5001000C	TIMER_GPIO1_CONF_REG	Timer gpio1 selection
0x50010010	TIMER_GPIO2_CONF_REG	Timer gpio2 selection
0x50010014	TIMER_SETTINGS_REG	Timer reload value and Delay in shot mode
0x50010018	TIMER_SHOTWIDTH_REG	Timer Shot duration in shot mode
0x50010020	TIMER_CAPTURE_GPIO1_REG	Timer value for event on GPIO1
0x50010024	TIMER_CAPTURE_GPIO2_REG	Timer value for event on GPIO2
0x50010028	TIMER_PRESCALER_VAL_REG	Timer prescaler counter valuew
0x5001002C	TIMER_PWM_CTRL_REG	Timer pwm frequency register
0x50010034	TIMER_GPIO3_CONF_REG	Timer gpio3 selection

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Address	Register	Description
0x50010038	TIMER_GPIO4_CONF_REG	Timer gpio4 selection
0x5001003C	TIMER_CAPTURE_GPIO3_REG	Timer value for event on GPIO1
0x50010040	TIMER_CAPTURE_GPIO4_REG	Timer value for event on GPIO1
0x50010044	TIMER_PULSE_CNT_CTRL_REG	Timer pulse counter ctrl register
0x50010048	TIMER_ONESHOT_TRIGGER_REG	Timer oneshot trigger register
0x5001004C	TIMER_PWM_SYNC_REG	Timer pwm synchronisation register
0x50010054	TIMER_CLEAR_IRQ_REG	Timer clear interrupt
0x50010058	TIMER_CLEAR_IRQ_PULSE_REG	Timer clear pulse interrupt

Table 1141: TIMER_CTRL_REG (0x50010000)

Bit	Mode	Symbol	Description	Reset
31:21	-	-	Reserved	0x0
20	R/W	TIM_SINGLE_EVENT_CAPTURE	When this bit is set, only the first event on captimer1 is captured	0x0
19	R/W	TIM_EDGE_DET_CNT_FALL_EN	Select on which edge the edge detection should react; 0: the counter is triggered on a rising edge 1: the counter is triggered on a falling edge NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	0x0
18	R/W	TIM_EDGE_DET_CNT_EN	Enable edge detection counter. NOTE: In sleep only 80 MHz can be reached at 900 mV	0x0
17	R/W	TIM_ONESHOT_SWITCH	Automatically switch after the completion of the pulse output without the CPU programming anything. 0: No automated switch from OneShot to Counter mode 1: Automated switch from OneShot to Counter mode and start counting down. In case no start value has been programmed (reload=0), the timer keeps generating interrupts until the timer clock is disabled	0x0
16:15	R/W	TIM_ONESHOT_TRIGGER	Oneshot trigger source 00: Select external GPIO as the trigger for one shot 01: Select a register write as the trigger of one shot 10: Either of the two triggers one shot	0x0

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Bit	Mode	Symbol	Description	Reset
			11: None of the two triggers one shot	
14	R/W	-	Reserved	0x0
13	R/W	-	Reserved	0x0
12	R/W	-	Reserved	0x0
11	R/W	-	Reserved	0x0
10	R/W	TIM_IN4_EVENT_FALL_EN	Event input 4 edge type 1 = falling edge 0 = rising edge	0x0
9	R/W	TIM_IN3_EVENT_FALL_EN	Event input 3 edge type 1 = falling edge 0 = rising edge	0x0
8	R/W	TIM_CLK_EN	Timer clock enable 1 = clock enabled 0 = clock disabled	0x0
7	R/W	TIM_SYS_CLK_EN	Select clock 1 = Timer uses the DIVN clock 0 = Timer uses the lp clock NOTE: When switching clock, the timer clock should be disabled (TIM_CLK_EN, bit 8)	0x0
6	R/W	TIM_FREE_RUN_MODE_EN	Valid when timer counts up, if it is 1 timer does not zero when reaches to reload value. it becomes zero only when it reaches the max value.	0x0
5	R/W	TIM_IRQ_EN	Interrupt mask 1 = timer IRQ is unmasked 0 = timer IRQ is masked	0x0
4	R/W	TIM_IN2_EVENT_FALL_EN	Event input 2 edge type 1 = falling edge 0 = rising edge	0x0
3	R/W	TIM_IN1_EVENT_FALL_EN	Event input 1 edge type 1 = falling edge 0 = rising edge	0x0
2	R/W	TIM_COUNT_DOWN_EN	Timer count direction 1: down 0: up NOTE: Only change counter direction when timer is not enabled	0x0
1	R/W	TIM_ONESHOT_MODE_EN	Timer mode 1 = One shot enabled 0 = Counter enabled	0x0
0	R/W	TIM_EN	Timer enable 1 = On 0 = Off	0x0

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Table 1142: TIMER_TIMER_VAL_REG (0x50010004)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_TIMER_VALUE	Gives the current timer value	0x0

Table 1143: TIMER_STATUS_REG (0x50010008)

Bit	Mode	Symbol	Description	Reset
14	R	TIM_IRQ_PULSE_STATUS	Status bit of IRQ pulse counter. When the pulse counter reaches the theshold value, this bit is 1	0x0
13	R	TIM_IN4_STATE	Gives the logic level of the IN4	0x0
12	R	TIM_IN3_STATE	Gives the logic level of the IN3	0x0
11	R	TIM_SWITCHED_TO_DIVN_CLK	Indicates that timer clock has been switched to divn clock	0x0
10	R	TIM_PWM_BUSY	Busy with synchronizing PWM_FREQ_REG and PWM_DC_REG. Do not write a new value to these registers when this bit is high	0x0
9	R	TIM_TIMER_BUSY	Busy with synchronizing PRESCALER_REG, RELOAD_REG and SHOTWIDTH_REG. Do not write a new value to these registers when this bit is high	0x0
8	R	TIM_IRQ_STATUS	IRQ status bit. When an irq has occured, this bit is 1.	0x0
7	R	-	Reserved	0x0
6	R	-	Reserved	0x0
5	R	-	Reserved	0x0
4	R	-	Reserved	0x0
3:2	R	TIM_ONESHOT_PHASE	OneShot phase 0 = Wait for event 1 = Delay phase 2 = Start Shot 3 = Shot phase	0x0
1	R	TIM_IN2_STATE	Gives the logic level of the IN1	0x0
0	R	TIM_IN1_STATE	Gives the logic level of the IN2	0x0

Table 1144: TIMER_GPIO1_CONF_REG (0x5001000C)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO1_CONF	Select one of the 32 GPIOs as IN1, Valid values 0-32. 0: Disable input 1: P0_00	0x0

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Bit	Mode	Symbol	Description	Reset
			2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	

Table 1145: TIMER_GPIO2_CONF_REG (0x50010010)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO2_CONF	Select one of the 32 GPIOs as IN2, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08	0x0

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Bit	Mode	Symbol	Description	Reset
			10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	

Table 1146: TIMER_SETTINGS_REG (0x50010014)

Bit	Mode	Symbol	Description	Reset
31:29	-	-	Reserved	0x0
28:24	R/W	TIM_PRESCALER	Defines the timer count frequency. CLOCK frequency / (TIM_PRESCALER+1)	0x0
23:0	R/W	TIM_RELOAD	Reload or max value in timer mode, Delay phase duration in oneshot mode. Actual delay is the register value plus synchronization time (3 clock cycles)	0x0

Table 1147: TIMER_SHOTWIDTH_REG (0x50010018)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R/W	TIM_SHOTWIDTH	Shot phase duration in oneshot mode	0x0

Table 1148: TIMER_CAPTURE_GPIO1_REG (0x50010020)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
23:0	R	TIM_CAPTURE_GPIO1	Gives the Capture time for event on GPIO1	0x0

Table 1149: TIMER_CAPTURE_GPIO2_REG (0x50010024)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO2	Gives the Capture time for event on GPIO2	0x0

Table 1150: TIMER_PRESCALER_VAL_REG (0x50010028)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4:0	R	TIM_PRESCALER_VAL	Gives the current prescaler counter value	0x0

Table 1151: TIMER_PWM_CTRL_REG (0x5001002C)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	TIM_PWM_DC	Defines the PWM duty cycle. TIM_PWM_DC / (TIM_PWM_FREQ+1)	0x0
15:0	R/W	TIM_PWM_FREQ	Defines the PWM frequency. Timer clock frequency / (TIM_PWM_FREQ+1) Timer clock is clock after prescaler	0x0

Table 1152: TIMER_GPIO3_CONF_REG (0x50010034)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO3_CONF	Select one of the 32 GPIOs as IN3, Valid value 0-32. 1 for the first gpio, 32 for the last gpio. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10	0x0

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Bit	Mode	Symbol	Description	Reset
			12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	

Table 1153: TIMER_GPIO4_CONF_REG (0x50010038)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO4_CONF	Select one of the 32 GPIOs as IN4, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04	0x0

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Bit	Mode	Symbol	Description	Reset
			20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	

Table 1154: TIMER_CAPTURE_GPIO3_REG (0x5001003C)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO3	Gives the Capture time for event on GPIO3	0x0

Table 1155: TIMER_CAPTURE_GPIO4_REG (0x50010040)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO4	Gives the Capture time for event on GPIO4	0x0

Table 1156: TIMER_PULSE_CNT_CTRL_REG (0x50010044)

Bit	Mode	Symbol	Description	Reset
29:24	R/W	PULSE_CNT_GPIO_SEL	Select one of the 32 GPIOs as input for the pulse counter, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10	0x0

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Bit	Mode	Symbol	Description	Reset
			12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17 NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	
23:0	R/W	PULSE_CNT_THRESHOLD	Select after how many pulses an irq is fired for the pulse counter n-2. NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	0x0

Table 1157: TIMER_ONESHOT_TRIGGER_REG (0x50010048)

Bit	Mode	Symbol	Description	Reset
0	R0/W	TIM_ONESHOT_TRIGGER_SW	trigger oneshot	0x0

Table 1158: TIMER_PWM_SYNC_REG (0x5001004C)

Bit	Mode	Symbol	Description	Reset
6	R/W	TIMER6_SYNC	Enable PWM start synchronisation of timer6	0x0
5	R/W	-	Reserved	0x0
4	R/W	TIMER3_SYNC	Enable PWM start synchronisation of timer3	0x0
3	R/W	TIMER2_SYNC	Enable PWM start synchronisation of timer2	0x0
2	R/W	TIMER_SYNC	Enable PWM synchronisation of timer	0x0

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Bit	Mode	Symbol	Description	Reset
1	R/W	SYNC_ENABLE	Enable PWM start synchronisation of the selected timers	0x0
0	R/W	PWM_START	Start PWM of the selected timers	0x0

Table 1159: TIMER_CLEAR_IRQ_REG (0x50010054)

Bit	Mode	Symbol	Description	Reset
0	R0/W	TIM_CLEAR_IRQ	Write any value clear interrupt	0x0

Table 1160: TIMER_CLEAR_IRQ_PULSE_REG (0x50010058)

Bit	Mode	Symbol	Description	Reset
0	R0/W	TIM_CLEAR_PULSE_IRQ	Write any value will clear irq pulse interrupt	0x0

Table 1161: Register map TIMER2

Address	Register	Description
0x50010100	TIMER2_CTRL_REG	Timer control register
0x50010104	TIMER2_TIMER_VAL_REG	Timer counter value
0x50010108	TIMER2_STATUS_REG	Timer status register
0x5001010C	TIMER2_GPIO1_CONF_REG	Timer gpio1 selection
0x50010110	TIMER2_GPIO2_CONF_REG	Timer gpio2 selection
0x50010114	TIMER2_SETTINGS_REG	Timer reload value and Delay in shot mode
0x50010118	TIMER2_SHOTWIDTH_REG	Timer Shot duration in shot mode
0x50010120	TIMER2_CAPTURE_GPIO1_REG	Timer value for event on GPIO1
0x50010124	TIMER2_CAPTURE_GPIO2_REG	Timer value for event on GPIO2
0x50010128	TIMER2_PRESCALER_VAL_REG	Timer prescaler counter value
0x5001012C	TIMER2_PWM_CTRL_REG	Timer pwm frequency register
0x50010144	TIMER2_PULSE_CNT_CTRL_REG	Timer pulse counter ctrl register
0x50010154	TIMER2_CLEAR_IRQ_REG	Timer clear interrupt
0x50010158	TIMER2_CLEAR_IRQ_PULSE_REG	Timer clear pulse interrupt

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Table 1162: TIMER2_CTRL_REG (0x50010100)

Bit	Mode	Symbol	Description	Reset
31:20	-	-	Reserved	0x0
19	R/W	TIM_EDGE_DET_CNT_FALL_EN	Select on which edge the edge detection should react; 0: the counter is triggered on a rising edge 1: the counter is triggered on a falling edge NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	0x0
18	R/W	TIM_EDGE_DET_CNT_EN	Enable edge detection counter	0x0
17:9	-	-	Reserved	0x0
8	R/W	TIM_CLK_EN	Timer clock enable 1 = clock enabled 0 = clock disabled	0x0
7	R/W	TIM_SYS_CLK_EN	Select clock 1 = Timer uses the DIVN clock 0 = Timer uses the lp clock NOTE: when switching clock, the timer clock should be disabled (TIM_CLK_EN, bit 8)	0x0
6	R/W	TIM_FREE_RUN_MODE_EN	Valid when timer counts up, if it is '1' timer does not zero when reaches to reload value. it becomes zero only when it reaches the max value.	0x0
5	R/W	TIM_IRQ_EN	Interrupt mask 1 = timer IRQ is unmasked 0 = timer IRQ is masked	0x0
4	R/W	TIM_IN2_EVENT_FALL_EN	Event input 2 edge type 1 = falling edge 0 = rising edge	0x0
3	R/W	TIM_IN1_EVENT_FALL_EN	Event input 1 edge type 1 = falling edge 0 = rising edge	0x0
2	R/W	TIM_COUNT_DOWN_EN	Timer count direction 1 = down 0 = up NOTE: only change this bit when timer is disabled	0x0
1	R/W	TIM_ONESHOT_MODE_EN	Timer mode 1 = One shot enabled 0 = Counter enabled	0x0
0	R/W	TIM_EN	Timer enable 1 = On 0 = Off	0x0

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Table 1163: TIMER2_TIMER_VAL_REG (0x50010104)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_TIMER_VALUE	Gives the current timer value	0x0

Table 1164: TIMER2_STATUS_REG (0x50010108)

Bit	Mode	Symbol	Description	Reset
14	R	TIM_IRQ_PULSE_STATUS	Status bit of IRQ pulse counter. When the pulse counter reaches the theshold value, this bit is 1	0x0
13:12	-	-	Reserved	0x0
11	R	TIM_SWITCHED_TO_DIVN_CLK	Indicates that timer clock has been switched to divn clock	0x0
10	R	TIM_PWM_BUSY	Busy with synchronizing PWM_FREQ_REG and PWM_DC_REG. Do not write a new value to these registers when this bit is high.	0x0
9	R	TIM_TIMER_BUSY	Busy with synchronizing PRESCALER_REG, RELOAD_REG and SHOTWIDTH_REG. Do not write a new value to these registers when this bit is high.	0x0
8	R	TIM_IRQ_STATUS	IRQ status bit. When an irq has occured, this bit is 1.	0x0
7:4	-	-	Reserved	0x0
3:2	R	TIM_ONESHOT_PHASE	OneShot phase 0 = Wait for event 1 = Delay phase 2 = Start Shot 3 = Shot phase	0x0
1	R	TIM_IN2_STATE	Gives the logic level of the IN1	0x0
0	R	TIM_IN1_STATE	Gives the logic level of the IN2	0x0

Table 1165: TIMER2_GPIO1_CONF_REG (0x5001010C)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO1_CONF	Select one of the 32 GPIOs as IN1, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05	0x0

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Bit	Mode	Symbol	Description	Reset
			7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	

Table 1166: TIMER2_GPIO2_CONF_REG (0x50010110)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO2_CONF	Select one of the 32 GPIOs as IN2, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13	0x0

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Bit	Mode	Symbol	Description	Reset
			15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	

Table 1167: TIMER2_SETTINGS_REG (0x50010114)

Bit	Mode	Symbol	Description	Reset
31:29	-	-	Reserved	0x0
28:24	R/W	TIM_PRESCALER	Defines the timer count frequency. CLOCK frequency / (TIM_PRESCALER+1)	0x0
23:0	R/W	TIM_RELOAD	Reload or max value in timer mode, Delay phase duration in oneshot mode. Actual delay is the register value plus synchronization time (3 clock cycles)	0x0

Table 1168: TIMER2_SHOTWIDTH_REG (0x50010118)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R/W	TIM_SHOTWIDTH	Shot phase duration in oneshot mode	0x0

Table 1169: TIMER2_CAPTURE_GPIO1_REG (0x50010120)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO1	Gives the Capture time for event on GPIO1	0x0

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Table 1170: TIMER2_CAPTURE_GPIO2_REG (0x50010124)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO2	Gives the Capture time for event on GPIO2	0x0

Table 1171: TIMER2_PRESCALER_VAL_REG (0x50010128)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4:0	R	TIM_PRESCALER_VAL	Gives the current prescaler counter value	0x0

Table 1172: TIMER2_PWM_CTRL_REG (0x5001012C)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	TIM_PWM_DC	Defines the PWM duty cycle. TIM_PWM_DC / (TIM_PWM_FREQ+1)	0x0
15:0	R/W	TIM_PWM_FREQ	Defines the PWM frequency. Timer clock frequency / (TIM_PWM_FREQ+1) Timer clock is clock after prescaler	0x0

Table 1173: TIMER2_PULSE_CNT_CTRL_REG (0x50010144)

Bit	Mode	Symbol	Description	Reset
29:24	R/W	PULSE_CNT_GPIO_SEL	Select one of the 32 GPIOs as input for the pulse counter, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03	0x0

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Bit	Mode	Symbol	Description	Reset
			19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17 NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	
23:0	R/W	PULSE_CNT_THRESHOLD	Select after how many pulses an irq is fired for the pulse counter NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	0x0

Table 1174: TIMER2_CLEAR_IRQ_REG (0x50010154)

Bit	Mode	Symbol	Description	Reset
0	R0/W	TIM_CLEAR_IRQ	Write any value clear interrupt	0x0

Table 1175: TIMER2_CLEAR_IRQ_PULSE_REG (0x50010158)

Bit	Mode	Symbol	Description	Reset
0	R0/W	TIM_CLEAR_PULSE_IRQ	Write any value will clear irq pulse interrupt	0x0

Table 1176: Register map TIMER3

Address	Register	Description
0x50010200	TIMER3_CTRL_REG	Timer control register
0x50010204	TIMER3_TIMER_VAL_REG	Timer counter value
0x50010208	TIMER3_STATUS_REG	Timer status register
0x5001020C	TIMER3_GPIO1_CONF_REG	Timer gpio1 selection

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Address	Register	Description
0x50010210	TIMER3_GPIO2_CONF_REG	Timer gpio2 selection
0x50010214	TIMER3_SETTINGS_REG	Timer reload value and Delay in shot mode
0x50010218	TIMER3_SHOTWIDTH_REG	Timer Shot duration in shot mode
0x50010220	TIMER3_CAPTURE_GPIO1_REG	Timer value for event on GPIO1
0x50010224	TIMER3_CAPTURE_GPIO2_REG	Timer value for event on GPIO2
0x50010228	TIMER3_PRESCALER_VAL_REG	Timer prescaler counter value
0x5001022C	TIMER3_PWM_CTRL_REG	Timer pwm frequency register
0x50010244	TIMER3_PULSE_CNT_CTRL_REG	Timer pulse counter ctrl register
0x50010254	TIMER3_CLEAR_IRQ_REG	Timer clear interrupt
0x50010258	TIMER3_CLEAR_IRQ_PULSE_REG	Timer clear pulse interrupt

Table 1177: TIMER3_CTRL_REG (0x50010200)

Bit	Mode	Symbol	Description	Reset
31:20	-	-	Reserved	0x0
19	R/W	TIM_EDGE_DET_CNT_FALL_EN	Select on which edge the edge detection should react; 0: the counter is triggered on a rising edge 1: the counter is triggered on a falling edge NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	0x0
18	R/W	TIM_EDGE_DET_CNT_EN	Enable edge detection counter	0x0
17:9	-	-	Reserved	0x0
8	R/W	TIM_CLK_EN	Timer clock enable 1 = clock enabled 0 = clock disabled	0x0
7	R/W	TIM_SYS_CLK_EN	Select clock 1 = Timer uses the DIVN clock 0 = Timer uses the lp clock NOTE: when switching clock, the timer clock should be disabled (TIM_CLK_EN, bit 8)	0x0

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Bit	Mode	Symbol	Description	Reset
6	R/W	TIM_FREE_RUN_MODE_EN	Valid when timer counts up, if it is '1' timer does not zero when reaches to reload value. it becomes zero only when it reaches the max value.	0x0
5	R/W	TIM_IRQ_EN	Interrupt mask 1 = timer IRQ is unmasked 0 = timer IRQ is masked	0x0
4	R/W	TIM_IN2_EVENT_FALL_EN	Event input 2 edge type 1 = falling edge 0 = rising edge	0x0
3	R/W	TIM_IN1_EVENT_FALL_EN	Event input 1 edge type 1 = falling edge 0 = rising edge	0x0
2	R/W	TIM_COUNT_DOWN_EN	Timer count direction 1 = down 0 = up NOTE: only change this bit when timer is disabled	0x0
1	R/W	TIM_ONESHOT_MODE_EN	Timer mode 1 = One shot enabled 0 = Counter enabled	0x0
0	R/W	TIM_EN	Timer enable 1 = On 0 = Off	0x0

Table 1178: TIMER3_TIMER_VAL_REG (0x50010204)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_TIMER_VALUE	Gives the current timer value	0x0

Table 1179: TIMER3_STATUS_REG (0x50010208)

Bit	Mode	Symbol	Description	Reset
14	R	TIM_IRQ_PULSE_STATUS	Status bit of IRQ pulse counter. When the pulse counter reaches the theshold value, this bit is 1	0x0
13:12	-	-	Reserved	0x0
11	R	TIM_SWITCHED_TO_DIVN_CLK	Indicates that timer clock has been switched to divn clock	0x0
10	R	TIM_PWM_BUSY	Busy with synchronizing PWM_FREQ_REG and PWM_DC_REG. Do not write a new value to these registers when this bit is high.	0x0
9	R	TIM_TIMER_BUSY	Busy with synchronizing PRESCALER_REG, RELOAD_REG and SHOTWIDTH_REG. Do not write a new value to these registers when this bit is high.	0x0

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Bit	Mode	Symbol	Description	Reset
8	R	TIM_IRQ_STATUS	IRQ status bit. When an irq has occured, this bit is 1.	0x0
7:4	-	-	Reserved	0x0
3:2	R	TIM_ONESHOT_PHASE	OneShot phase 0 = Wait for event 1 = Delay phase 2 = Start Shot 3 = Shot phase	0x0
1	R	TIM_IN2_STATE	Gives the logic level of the IN1	0x0
0	R	TIM_IN1_STATE	Gives the logic level of the IN2	0x0

Table 1180: TIMER3_GPIO1_CONF_REG (0x5001020C)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO1_CONF	Select one of the 32 GPIOs as IN1, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14	0x0

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Bit	Mode	Symbol	Description	Reset
			30: P1_15 31: P1_16 32: P1_17	

Table 1181: TIMER3_GPIO2_CONF_REG (0x50010210)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO2_CONF	Select one of the 32 GPIOs as IN2, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	0x0

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Table 1182: TIMER3_SETTINGS_REG (0x50010214)

Bit	Mode	Symbol	Description	Reset
31:29	-	-	Reserved	0x0
28:24	R/W	TIM_PRESCALER	Defines the timer count frequency. CLOCK frequency / (TIM_PRESCALER+1)	0x0
23:0	R/W	TIM_RELOAD	Reload or max value in timer mode, Delay phase duration in oneshot mode. Actual delay is the register value plus synchronization time (3 clock cycles)	0x0

Table 1183: TIMER3_SHOTWIDTH_REG (0x50010218)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R/W	TIM_SHOTWIDTH	Shot phase duration in oneshot mode	0x0

Table 1184: TIMER3_CAPTURE_GPIO1_REG (0x50010220)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO1	Gives the Capture time for event on GPIO1	0x0

Table 1185: TIMER3_CAPTURE_GPIO2_REG (0x50010224)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO2	Gives the Capture time for event on GPIO2	0x0

Table 1186: TIMER3_PRESCALER_VAL_REG (0x50010228)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4:0	R	TIM_PRESCALER_VAL	Gives the current prescaler counter value	0x0

Table 1187: TIMER3_PWM_CTRL_REG (0x5001022C)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	TIM_PWM_DC	Defines the PWM duty cycle. TIM_PWM_DC / (TIM_PWM_FREQ+1)	0x0

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Bit	Mode	Symbol	Description	Reset
15:0	R/W	TIM_PWM_FREQ	Defines the PWM frequency. Timer clock frequency / (TIM_PWM_FREQ+1) Timer clock is clock after prescaler	0x0

Table 1188: TIMER3_PULSE_CNT_CTRL_REG (0x50010244)

Bit	Mode	Symbol	Description	Reset
29:24	R/W	PULSE_CNT_GPIO_SEL	Select one of the 32 GPIOs as input for the pulse counter, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17 NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	0x0
23:0	R/W	PULSE_CNT_THRESHOLD	Select after how many pulses an irq is fired for the pulse counter	0x0

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Bit	Mode	Symbol	Description	Reset
			NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	

Table 1189: TIMER3_CLEAR_IRQ_REG (0x50010254)

Bit	Mode	Symbol	Description	Reset
0	R0/W	TIM_CLEAR_IRQ	Write any value clear interrupt	0x0

Table 1190: TIMER3_CLEAR_IRQ_PULSE_REG (0x50010258)

Bit	Mode	Symbol	Description	Reset
0	R0/W	TIM_CLEAR_PULSE_IRQ	Write any value will clear irq pulse interrupt	0x0

Table 1191: Register map TIMER4

Address	Register	Description
0x50010300	TIMER4_CTRL_REG	Timer control register
0x50010304	TIMER4_TIMER_VAL_REG	Timer counter value
0x50010308	TIMER4_STATUS_REG	Timer status register
0x5001030C	TIMER4_GPIO1_CONF_REG	Timer gpio1 selection
0x50010310	TIMER4_GPIO2_CONF_REG	Timer gpio2 selection
0x50010314	TIMER4_SETTINGS_REG	Timer reload value and Delay in shot mode
0x50010318	TIMER4_SHOTWIDTH_REG	Timer Shot duration in shot mode
0x50010320	TIMER4_CAPTURE_GPIO1_REG	Timer value for event on GPIO1
0x50010324	TIMER4_CAPTURE_GPIO2_REG	Timer value for event on GPIO2
0x50010328	TIMER4_PRESCALER_VAL_REG	Timer prescaler counter valuew
0x5001032C	TIMER4_PWM_CTRL_REG	Timer pwm frequency register
0x50010334	TIMER4_GPIO3_CONF_REG	Timer gpio3 selection
0x50010338	TIMER4_GPIO4_CONF_REG	Timer gpio4 selection

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Address	Register	Description
0x5001033C	TIMER4_CAPTURE_GPIO3_REG	Timer value for event on GPIO1
0x50010340	TIMER4_CAPTURE_GPIO4_REG	Timer value for event on GPIO1
0x50010344	TIMER4_PULSE_CNT_CTRL_REG	Timer pulse counter ctrl register
0x50010348	TIMER4_ONESHOT_TRIGGER_REG	Timer oneshot trigger register
0x50010350	TIMER4_CLEAR_GPIO_EVENT_REG	Timer clear gpio event register
0x50010354	TIMER4_CLEAR_IRQ_REG	Timer clear interrupt
0x50010358	TIMER4_CLEAR_IRQ_PULSE_REG	Timer clear pulse interrupt

Table 1192: TIMER4_CTRL_REG (0x50010300)

Bit	Mode	Symbol	Description	Reset
31:21	-	-	Reserved	0x0
20	R/W	TIM_SINGLE_EVENT_CAPTURE	When this bit is set, only the first event on captimer1 is captured	0x0
19	R/W	TIM_EDGE_DET_CNT_FALL_EN	Select on which edge the edge detection should react; 0: the counter is triggered on a rising edge 1: the counter is triggered on a falling edge NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	0x0
18	R/W	TIM_EDGE_DET_CNT_EN	Enable edge detection counter. NOTE: In sleep only 80 MHz can be reached at 900 mV	0x0
17	R/W	TIM_ONESHOT_SWITCH	Automatically switch after the completion of the pulse output without the CPU programming anything. 0: No automated switch from OneShot to Counter mode 1: Automated switch from OneShot to Counter mode and start counting down. In case no start value has been programmed (reload=0), the timer keeps generating interrupts until the timer clock is disabled	0x0
16:15	R/W	TIM_ONESHOT_TRIGGER	Oneshot trigger source 00: Select external GPIO as the trigger for one shot 01: Select a register write as the trigger of one shot 10: Either of the two triggers one shot 11: None of the two triggers one shot	0x0

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Bit	Mode	Symbol	Description	Reset
14	R/W	TIM_CAP_GPIO4_IRQ_EN	0 = Event on GPIO4 does not create a CAPTIM interrrupt 1 = Event on GPIO4 creates a CAPTIM interrrupt	0x0
13	R/W	TIM_CAP_GPIO3_IRQ_EN	0 = Event on GPIO3 does not create a CAPTIM interrrupt 1 = Event on GPIO3 creates a CAPTIM interrrupt	0x0
12	R/W	TIM_CAP_GPIO2_IRQ_EN	0 = Event on GPIO2 does not create a CAPTIM interrrupt 1 = Event on GPIO2 creates a CAPTIM interrrupt	0x0
11	R/W	TIM_CAP_GPIO1_IRQ_EN	0 = Event on GPIO1 does not create a CAPTIM interrrupt 1 = Event on GPIO1 creates a CAPTIM interrrupt	0x0
10	R/W	TIM_IN4_EVENT_FALL_EN	Event input 4 edge type 1 = falling edge 0 = rising edge	0x0
9	R/W	TIM_IN3_EVENT_FALL_EN	Event input 3 edge type 1 = falling edge 0 = rising edge	0x0
8	R/W	TIM_CLK_EN	Timer clock enable 1 = clock enabled 0 = clock disabled	0x0
7	R/W	TIM_SYS_CLK_EN	Select clock 1 = Timer uses the DIVN clock 0 = Timer uses the lp clock NOTE: when switching clock, the timer clock should be disabled (TIM_CLK_EN, bit 8)	0x0
6	R/W	TIM_FREE_RUN_MODE_EN	Valid when timer counts up, if it is 1 timer does not zero when reaches to reload value. it becomes zero only when it reaches the max value.	0x0
5	R/W	TIM_IRQ_EN	Interrupt mask 1 = timer IRQ is unmasked 0 = timer IRQ is masked	0x0
4	R/W	TIM_IN2_EVENT_FALL_EN	Event input 2 edge type 1 = falling edge 0 = rising edge	0x0
3	R/W	TIM_IN1_EVENT_FALL_EN	Event input 1 edge type 1 = falling edge 0 = rising edge	0x0
2	R/W	TIM_COUNT_DOWN_EN	Timer count direction 1 = down 0 = up NOTE: only change counter direction when timer is not enabled	0x0
1	R/W	TIM_ONESHOT_MODE_EN	Timer mode 1 = One shot enabled	0x0

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Bit	Mode	Symbol	Description	Reset
			0 = Counter enabled	
0	R/W	TIM_EN	Timer enable 1 = On 0 = Off	0x0

Table 1193: TIMER4_TIMER_VAL_REG (0x50010304)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_TIMER_VALUE	Gives the current timer value	0x0

Table 1194: TIMER4_STATUS_REG (0x50010308)

Bit	Mode	Symbol	Description	Reset
14	R	TIM_IRQ_PULSE_STATUS	Status bit of IRQ pulse counter. When the pulse counter reaches the theshold value, this bit is 1	0x0
13	R	TIM_IN4_STATE	Gives the logic level of the IN4	0x0
12	R	TIM_IN3_STATE	Gives the logic level of the IN3	0x0
11	R	TIM_SWITCHED_TO_DIVN_CLK	Indicates that timer clock has been switched to divn clock	0x0
10	R	TIM_PWM_BUSY	Busy with synchronizing PWM_FREQ_REG and PWM_DC_REG. Do not write a new value to these registers when this bit is high	0x0
9	R	TIM_TIMER_BUSY	Busy with synchronizing PRESCALER_REG, RELOAD_REG and SHOTWIDTH_REG. Do not write a new value to these registers when this bit is high	0x0
8	R	TIM_IRQ_STATUS	IRQ status bit. When an irq has occured, this bit is 1.	0x0
7	R	TIM_GPIO4_EVENT_PENDING	When 1, GPIO4 event is pending.	0x0
6	R	TIM_GPIO3_EVENT_PENDING	When 1, GPIO3 event is pending.	0x0
5	R	TIM_GPIO2_EVENT_PENDING	When 1, GPIO2 event is pending.	0x0
4	R	TIM_GPIO1_EVENT_PENDING	When 1, GPIO1 event is pending.	0x0
3:2	R	TIM_ONESHOT_PHASE	OneShot phase 0 = Wait for event 1 = Delay phase 2 = Start Shot 3 = Shot phase	0x0
1	R	TIM_IN2_STATE	Gives the logic level of the IN1	0x0
0	R	TIM_IN1_STATE	Gives the logic level of the IN2	0x0

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Table 1195: TIMER4_GPIO1_CONF_REG (0x5001030C)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO1_CONF	Select one of the 32 GPIOs as IN1, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	0x0

Table 1196: TIMER4_GPIO2_CONF_REG (0x50010310)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO2_CONF	Select one of the 32 GPIOs as IN2, Valid values 0-32. 0: Disable input	0x0

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Bit	Mode	Symbol	Description	Reset
			1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	

Table 1197: TIMER4_SETTINGS_REG (0x50010314)

Bit	Mode	Symbol	Description	Reset
31:29	-	-	Reserved	0x0
28:24	R/W	TIM_PRESCALER	Defines the timer count frequency. CLOCK frequency / (TIM_PRESCALER+1)	0x0
23:0	R/W	TIM_RELOAD	Reload or max value in timer mode, Delay phase duration in oneshot mode. Actual delay is the register value plus synchronization time (3 clock cycles)	0x0

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Table 1198: TIMER4_SHOTWIDTH_REG (0x50010318)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R/W	TIM_SHOTWIDTH	Shot phase duration in oneshot mode	0x0

Table 1199: TIMER4_CAPTURE_GPIO1_REG (0x50010320)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO1	Gives the Capture time for event on GPIO1	0x0

Table 1200: TIMER4_CAPTURE_GPIO2_REG (0x50010324)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO2	Gives the Capture time for event on GPIO2	0x0

Table 1201: TIMER4_PRESCALER_VAL_REG (0x50010328)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4:0	R	TIM_PRESCALER_VAL	Gives the current prescaler counter value	0x0

Table 1202: TIMER4_PWM_CTRL_REG (0x5001032C)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	TIM_PWM_DC	Defines the PWM duty cycle. TIM_PWM_DC / (TIM_PWM_FREQ+1)	0x0
15:0	R/W	TIM_PWM_FREQ	Defines the PWM frequency. Timer clock frequency / (TIM_PWM_FREQ+1) Timer clock is clock after prescaler	0x0

Table 1203: TIMER4_GPIO3_CONF_REG (0x50010334)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO3_CONF	Select one of the 32 GPIOs as IN3, Valid value 0-32. 1 for the first gpio, 32 for the last gpio. 0: Disable input 1: P0_00	0x0

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Bit	Mode	Symbol	Description	Reset
			2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	

Table 1204: TIMER4_GPIO4_CONF_REG (0x50010338)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO4_CONF	Select one of the 32 GPIOs as IN4, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08	0x0

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Bit	Mode	Symbol	Description	Reset
			10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	

Table 1205: TIMER4_CAPTURE_GPIO3_REG (0x5001033C)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO3	Gives the Capture time for event on GPIO3	0x0

Table 1206: TIMER4_CAPTURE_GPIO4_REG (0x50010340)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO4	Gives the Capture time for event on GPIO4	0x0

Table 1207: TIMER4_PULSE_CNT_CTRL_REG (0x50010344)

Bit	Mode	Symbol	Description	Reset
29:24	R/W	PULSE_CNT_GPIO_SEL	Select one of the 32 GPIOs as input for the pulse counter, Valid values 0-32. 0: Disable input 1: P0_00	0x0

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Bit	Mode	Symbol	Description	Reset
			2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17 NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	
23:0	R/W	PULSE_CNT_THRESHOLD	Select after how many pulses an irq is fired for the pulse counter n-2. NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	0x0

Table 1208: TIMER4_ONESHOT_TRIGGER_REG (0x50010348)

Bit	Mode	Symbol	Description	Reset
0	R0/W	TIM_ONESHOT_TRIGGER_SW	trigger oneshot	0x0

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Table 1209: TIMER4_CLEAR_GPIO_EVENT_REG (0x50010350)

Bit	Mode	Symbol	Description	Reset
3	R0/W	TIM_CLEAR_GPIO4_EVENT	1 = Clear GPIO4 event. Return always 0	0x0
2	R0/W	TIM_CLEAR_GPIO3_EVENT	1 = Clear GPIO3 event. Return always 0	0x0
1	R0/W	TIM_CLEAR_GPIO2_EVENT	1 = Clear GPIO2 event. Return always 0	0x0
0	R0/W	TIM_CLEAR_GPIO1_EVENT	1 = Clear GPIO1 event. Return always 0	0x0

Table 1210: TIMER4_CLEAR_IRQ_REG (0x50010354)

Bit	Mode	Symbol	Description	Reset
0	R0/W	TIM_CLEAR_IRQ	Write any value clear interrupt	0x0

Table 1211: TIMER4_CLEAR_IRQ_PULSE_REG (0x50010358)

Bit	Mode	Symbol	Description	Reset
0	R0/W	TIM_CLEAR_PULSE_IRQ	Write any value will clear irq pulse interrupt	0x0

Table 1212: Register map TIMER5

Address	Register	Description
0x50010400	TIMER5_CTRL_REG	Timer control register
0x50010404	TIMER5_TIMER_VAL_REG	Timer counter value
0x50010408	TIMER5_STATUS_REG	Timer status register
0x5001040C	TIMER5_GPIO1_CONF_REG	Timer gpio1 selection
0x50010410	TIMER5_GPIO2_CONF_REG	Timer gpio2 selection
0x50010414	TIMER5_SETTINGS_REG	Timer reload value and Delay in shot mode
0x50010418	TIMER5_SHOTWIDTH_REG	Timer Shot duration in shot mode
0x50010420	TIMER5_CAPTURE_GPIO1_REG	Timer value for event on GPIO1
0x50010424	TIMER5_CAPTURE_GPIO2_REG	Timer value for event on GPIO2
0x50010428	TIMER5_PRESCALER_VAL_REG	Timer prescaler counter value
0x5001042C	TIMER5_PWM_CTRL_REG	Timer pwm frequency register

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Address	Register	Description
0x50010444	TIMER5_PULSE_CNT_CTRL_REG	Timer pulse counter ctrl register
0x50010454	TIMER5_CLEAR_IRQ_REG	Timer clear interrupt
0x50010458	TIMER5_CLEAR_IRQ_PULSE_REG	Timer clear pulse interrupt

Table 1213: TIMER5_CTRL_REG (0x50010400)

Bit	Mode	Symbol	Description	Reset
31:20	-	-	Reserved	0x0
19	R/W	TIM_EDGE_DET_CNT_FALL_EN	Select on which edge the edge detection should react; 0: the counter is triggered on a rising edge 1: the counter is triggered on a falling edge NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	0x0
18	R/W	TIM_EDGE_DET_CNT_EN	Enable edge detection counter	0x0
17:9	-	-	Reserved	0x0
8	R/W	TIM_CLK_EN	Timer clock enable 1 = clock enabled 0 = clock disabled	0x0
7	R/W	TIM_SYS_CLK_EN	Select clock 1 = Timer uses the DIVN clock 0 = Timer uses the lp clock NOTE: when switching clock, the timer clock should be disabled (TIM_CLK_EN, bit 8)	0x0
6	R/W	TIM_FREE_RUN_MODE_EN	Valid when timer counts up, if it is '1' timer does not zero when reaches to reload value. it becomes zero only when it reaches the max value.	0x0
5	R/W	TIM_IRQ_EN	Interrupt mask 1 = timer IRQ is unmasked 0 = timer IRQ is masked	0x0
4	R/W	TIM_IN2_EVENT_FALL_EN	Event input 2 edge type 1 = falling edge 0 = rising edge	0x0
3	R/W	TIM_IN1_EVENT_FALL_EN	Event input 1 edge type 1 = falling edge 0 = rising edge	0x0
2	R/W	TIM_COUNT_DOWN_EN	Timer count direction 1 = down 0 = up	0x0

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Bit	Mode	Symbol	Description	Reset
			NOTE: only change this bit when timer is disabled	
1	R/W	TIM_ONESHOT_MODE_EN	Timer mode 1 = One shot enabled 0 = Counter enabled	0x0
0	R/W	TIM_EN	Timer enable 1 = On 0 = Off	0x0

Table 1214: TIMER5_TIMER_VAL_REG (0x50010404)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_TIMER_VALUE	Gives the current timer value	0x0

Table 1215: TIMER5_STATUS_REG (0x50010408)

Bit	Mode	Symbol	Description	Reset
14	R	TIM_IRQ_PULSE_STATUS	Status bit of IRQ pulse counter. When the pulse counter reaches the theshold value, this bit is 1	0x0
13:12	-	-	Reserved	0x0
11	R	TIM_SWITCHED_TO_DIVN_CLK	Indicates that timer clock has been switched to divn clock	0x0
10	R	TIM_PWM_BUSY	Busy with synchronizing PWM_FREQ_REG and PWM_DC_REG. Do not write a new value to these registers when this bit is high.	0x0
9	R	TIM_TIMER_BUSY	Busy with synchronizing PRESCALER_REG, RELOAD_REG and SHOTWIDTH_REG. Do not write a new value to these registers when this bit is high.	0x0
8	R	TIM_IRQ_STATUS	IRQ status bit. When an irq has occured, this bit is 1.	0x0
7:4	-	-	Reserved	0x0
3:2	R	TIM_ONESHOT_PHASE	OneShot phase 0 = Wait for event 1 = Delay phase 2 = Start Shot 3 = Shot phase	0x0
1	R	TIM_IN2_STATE	Gives the logic level of the IN1	0x0
0	R	TIM_IN1_STATE	Gives the logic level of the IN2	0x0

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Table 1216: TIMER5_GPIO1_CONF_REG (0x5001040C)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO1_CONF	Select one of the 32 GPIOs as IN1, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	0x0

Table 1217: TIMER5_GPIO2_CONF_REG (0x50010410)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO2_CONF	Select one of the 32 GPIOs as IN2, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01	0x0

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Bit	Mode	Symbol	Description	Reset
			3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	

Table 1218: TIMER5_SETTINGS_REG (0x50010414)

Bit	Mode	Symbol	Description	Reset
31:29	-	-	Reserved	0x0
28:24	R/W	TIM_PRESCALER	Defines the timer count frequency. CLOCK frequency / (TIM_PRESCALER+1)	0x0
23:0	R/W	TIM_RELOAD	Reload or max value in timer mode, Delay phase duration in oneshot mode. Actual delay is the register value plus synchronization time (3 clock cycles)	0x0

Table 1219: TIMER5_SHOTWIDTH_REG (0x50010418)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R/W	TIM_SHOTWIDTH	Shot phase duration in oneshot mode	0x0

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Table 1220: TIMER5_CAPTURE_GPIO1_REG (0x50010420)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO1	Gives the Capture time for event on GPIO1	0x0

Table 1221: TIMER5_CAPTURE_GPIO2_REG (0x50010424)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO2	Gives the Capture time for event on GPIO2	0x0

Table 1222: TIMER5_PRESCALER_VAL_REG (0x50010428)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4:0	R	TIM_PRESCALER_VAL	Gives the current prescaler counter value	0x0

Table 1223: TIMER5_PWM_CTRL_REG (0x5001042C)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	TIM_PWM_DC	Defines the PWM duty cycle. TIM_PWM_DC / (TIM_PWM_FREQ+1)	0x0
15:0	R/W	TIM_PWM_FREQ	Defines the PWM frequency. Timer clock frequency / (TIM_PWM_FREQ+1) Timer clock is clock after prescaler	0x0

Table 1224: TIMER5_PULSE_CNT_CTRL_REG (0x50010444)

Bit	Mode	Symbol	Description	Reset
29:24	R/W	PULSE_CNT_GPIO_SEL	Select one of the 32 GPIOs as input for the pulse counter, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06	0x0

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Bit	Mode	Symbol	Description	Reset
			8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17 NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	
23:0	R/W	PULSE_CNT_THRESHOLD	Select after how many pulses an irq is fired for the pulse counter NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	0x0

Table 1225: TIMER5_CLEAR_IRQ_REG (0x50010454)

Bit	Mode	Symbol	Description	Reset
0	R0/W	TIM_CLEAR_IRQ	Write any value clear interrupt	0x0

Table 1226: TIMER5_CLEAR_IRQ_PULSE_REG (0x50010458)

Bit	Mode	Symbol	Description	Reset
0	R0/W	TIM_CLEAR_PULSE_IRQ	Write any value will clear irq pulse interrupt	0x0

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Table 1227: Register map TIMER6

Address	Register	Description
0x50010500	TIMER6_CTRL_REG	Timer control register
0x50010504	TIMER6_TIMER_VAL_REG	Timer counter value
0x50010508	TIMER6_STATUS_REG	Timer status register
0x5001050C	TIMER6_GPIO1_CONF_REG	Timer gpio1 selection
0x50010510	TIMER6_GPIO2_CONF_REG	Timer gpio2 selection
0x50010514	TIMER6_SETTINGS_REG	Timer reload value and Delay in shot mode
0x50010518	TIMER6_SHOTWIDTH_REG	Timer Shot duration in shot mode
0x50010520	TIMER6_CAPTURE_GPIO1_REG	Timer value for event on GPIO1
0x50010524	TIMER6_CAPTURE_GPIO2_REG	Timer value for event on GPIO2
0x50010528	TIMER6_PRESCALER_VAL_REG	Timer prescaler counter value
0x5001052C	TIMER6_PWM_CTRL_REG	Timer pwm frequency register
0x50010544	TIMER6_PULSE_CNT_CTRL_REG	Timer pulse counter ctrl register
0x50010554	TIMER6_CLEAR_IRQ_REG	Timer clear interrupt
0x50010558	TIMER6_CLEAR_IRQ_PULSE_REG	Timer clear pulse interrupt

Table 1228: TIMER6_CTRL_REG (0x50010500)

Bit	Mode	Symbol	Description	Reset
31:20	-	-	Reserved	0x0
19	R/W	TIM_EDGE_DET_CNT_FALL_EN	Select on which edge the edge detection should react; 0: the counter is triggered on a rising edge 1: the counter is triggered on a falling edge NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	0x0
18	R/W	TIM_EDGE_DET_CNT_EN	Enable edge detection counter	0x0
17:9	-	-	Reserved	0x0
8	R/W	TIM_CLK_EN	Timer clock enable 1 = clock enabled	0x0

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Bit	Mode	Symbol	Description	Reset
			0 = clock disabled	
7	R/W	TIM_SYS_CLK_EN	Select clock 1 = Timer uses the DIVN clock 0 = Timer uses the lp clock NOTE: when switching clock, the timer clock should be disabled (TIM_CLK_EN, bit 8)	0x0
6	R/W	TIM_FREE_RUN_MODE_EN	Valid when timer counts up, if it is '1' timer does not zero when reaches to reload value. it becomes zero only when it reaches the max value.	0x0
5	R/W	TIM_IRQ_EN	Interrupt mask 1 = timer IRQ is unmasked 0 = timer IRQ is masked	0x0
4	R/W	TIM_IN2_EVENT_FALL_EN	Event input 2 edge type 1 = falling edge 0 = rising edge	0x0
3	R/W	TIM_IN1_EVENT_FALL_EN	Event input 1 edge type 1 = falling edge 0 = rising edge	0x0
2	R/W	TIM_COUNT_DOWN_EN	Timer count direction 1 = down 0 = up NOTE: only change this bit when timer is disabled	0x0
1	R/W	TIM_ONESHOT_MODE_EN	Timer mode 1 = One shot enabled 0 = Counter enabled	0x0
0	R/W	TIM_EN	Timer enable 1 = On 0 = Off	0x0

Table 1229: TIMER6_TIMER_VAL_REG (0x50010504)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_TIMER_VALUE	Gives the current timer value	0x0

Table 1230: TIMER6_STATUS_REG (0x50010508)

Bit	Mode	Symbol	Description	Reset
14	R	TIM_IRQ_PULSE_STATUS	Status bit of IRQ pulse counter. When the pulse counter reaches the theshold value, this bit is 1	0x0
13:12	-	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
11	R	TIM_SWITCHED_TO_DIVN_CLK	Indicates that timer clock has been switched to divn clock	0x0
10	R	TIM_PWM_BUSY	Busy with synchronizing PWM_FREQ_REG and PWM_DC_REG. Do not write a new value to these registers when this bit is high.	0x0
9	R	TIM_TIMER_BUSY	Busy with synchronizing PRESCALER_REG, RELOAD_REG and SHOTWIDTH_REG. Do not write a new value to these registers when this bit is high.	0x0
8	R	TIM_IRQ_STATUS	IRQ status bit. When an irq has occured, this bit is 1.	0x0
7:4	-	-	Reserved	0x0
3:2	R	TIM_ONESHOT_PHASE	OneShot phase 0 = Wait for event 1 = Delay phase 2 = Start Shot 3 = Shot phase	0x0
1	R	TIM_IN2_STATE	Gives the logic level of the IN1	0x0
0	R	TIM_IN1_STATE	Gives the logic level of the IN2	0x0

Table 1231: TIMER6_GPIO1_CONF_REG (0x5001050C)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO1_CONF	Select one of the 32 GPIOs as IN1, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05	0x0

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Bit	Mode	Symbol	Description	Reset
			21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	

Table 1232: TIMER6_GPIO2_CONF_REG (0x50010510)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5:0	R/W	TIM_GPIO2_CONF	Select one of the 32 GPIOs as IN2, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13	0x0

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Bit	Mode	Symbol	Description	Reset
			29: P1_14 30: P1_15 31: P1_16 32: P1_17	

Table 1233: TIMER6_SETTINGS_REG (0x50010514)

Bit	Mode	Symbol	Description	Reset
31:29	-	-	Reserved	0x0
28:24	R/W	TIM_PRESCALER	Defines the timer count frequency. CLOCK frequency / (TIM_PRESCALER+1)	0x0
23:0	R/W	TIM_RELOAD	Reload or max value in timer mode, Delay phase duration in oneshot mode. Actual delay is the register value plus synchronization time (3 clock cycles)	0x0

Table 1234: TIMER6_SHOTWIDTH_REG (0x50010518)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R/W	TIM_SHOTWIDTH	Shot phase duration in oneshot mode	0x0

Table 1235: TIMER6_CAPTURE_GPIO1_REG (0x50010520)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO1	Gives the Capture time for event on GPIO1	0x0

Table 1236: TIMER6_CAPTURE_GPIO2_REG (0x50010524)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	0x0
23:0	R	TIM_CAPTURE_GPIO2	Gives the Capture time for event on GPIO2	0x0

Table 1237: TIMER6_PRESCALER_VAL_REG (0x50010528)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4:0	R	TIM_PRESCALER_VAL	Gives the current prescaler counter value	0x0

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Table 1238: TIMER6_PWM_CTRL_REG (0x5001052C)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	TIM_PWM_DC	Defines the PWM duty cycle. TIM_PWM_DC / (TIM_PWM_FREQ+1)	0x0
15:0	R/W	TIM_PWM_FREQ	Defines the PWM frequency. Timer clock frequency / (TIM_PWM_FREQ+1) Timer clock is clock after prescaler	0x0

Table 1239: TIMER6_PULSE_CNT_CTRL_REG (0x50010544)

Bit	Mode	Symbol	Description	Reset
29:24	R/W	PULSE_CNT_GPIO_SEL	Select one of the 32 GPIOs as input for the pulse counter, Valid values 0-32. 0: Disable input 1: P0_00 2: P0_01 3: P0_02 4: P0_03 5: P0_04 6: P0_05 7: P0_06 8: P0_07 9: P0_08 10: P0_09 11: P0_10 12: P0_11 13: P0_12 14: P0_13 15: P1_00 16: P1_01 17: P1_02 18: P1_03 19: P1_04 20: P1_05 21: P1_06 22: P1_07 23: P1_08 24: P1_09 25: P1_10 26: P1_11 27: P1_12 28: P1_13 29: P1_14 30: P1_15 31: P1_16 32: P1_17	0x0

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Bit	Mode	Symbol	Description	Reset
			NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	
23:0	R/W	PULSE_CNT_THRESHOLD	Select after how many pulses an irq is fired for the pulse counter NOTE: Only change this when EDGE_DET_CNT_EN=0 in TIMER_CTRL_REG	0x0

Table 1240: TIMER6_CLEAR_IRQ_REG (0x50010554)

Bit	Mode	Symbol	Description	Reset
0	R0/W	TIM_CLEAR_IRQ	Write any value clear interrupt	0x0

Table 1241: TIMER6_CLEAR_IRQ_PULSE_REG (0x50010558)

Bit	Mode	Symbol	Description	Reset
0	R0/W	TIM_CLEAR_PULSE_IRQ	Write any value will clear irq pulse interrupt	0x0

44.30 UART Registers

Table 1242: Register map UART

Address	Register	Description
0x50020000	UART_RBR_THR_DLL_REG	Receive Buffer Register
0x50020004	UART_IER_DLH_REG	Interrupt Enable Register
0x50020008	UART_IIR_FCR_REG	Interrupt Identification Register/FIFO Control Register
0x5002000C	UART_LCR_REG	Line Control Register
0x50020010	UART_MCR_REG	Modem Control Register
0x50020014	UART_LSR_REG	Line Status Register
0x5002001C	UART_SCR_REG	Scratchpad Register
0x50020030	UART_SRBR_STHR0_REG	Shadow Receive/Transmit Buffer Register
0x50020034	UART_SRBR_STHR1_REG	Shadow Receive/Transmit Buffer Register
0x50020038	UART_SRBR_STHR2_REG	Shadow Receive/Transmit Buffer Register
0x5002003C	UART_SRBR_STHR3_REG	Shadow Receive/Transmit Buffer Register
0x50020040	UART_SRBR_STHR4_REG	Shadow Receive/Transmit Buffer Register

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Address	Register	Description
0x50020044	UART_SRBR_STHR5_REG	Shadow Receive/Transmit Buffer Register
0x50020048	UART_SRBR_STHR6_REG	Shadow Receive/Transmit Buffer Register
0x5002004C	UART_SRBR_STHR7_REG	Shadow Receive/Transmit Buffer Register
0x50020050	UART_SRBR_STHR8_REG	Shadow Receive/Transmit Buffer Register
0x50020054	UART_SRBR_STHR9_REG	Shadow Receive/Transmit Buffer Register
0x50020058	UART_SRBR_STHR10_REG	Shadow Receive/Transmit Buffer Register
0x5002005C	UART_SRBR_STHR11_REG	Shadow Receive/Transmit Buffer Register
0x50020060	UART_SRBR_STHR12_REG	Shadow Receive/Transmit Buffer Register
0x50020064	UART_SRBR_STHR13_REG	Shadow Receive/Transmit Buffer Register
0x50020068	UART_SRBR_STHR14_REG	Shadow Receive/Transmit Buffer Register
0x5002006C	UART_SRBR_STHR15_REG	Shadow Receive/Transmit Buffer Register
0x5002007C	UART_USR_REG	UART Status register.
0x50020080	UART_TFL_REG	Transmit FIFO Level
0x50020084	UART_RFL_REG	Receive FIFO Level.
0x50020088	UART_SRR_REG	Software Reset Register.
0x50020090	UART_SBCR_REG	Shadow Break Control Register
0x50020094	UART_SDMAM_REG	Shadow DMA Mode
0x50020098	UART_SFE_REG	Shadow FIFO Enable
0x5002009C	UART_SRT_REG	Shadow RCVR Trigger
0x500200A0	UART_STET_REG	Shadow TX Empty Trigger
0x500200A4	UART_HTX_REG	Halt TX
0x500200A8	UART_DMASA_REG	DMA Software Acknowledge
0x500200C0	UART_DLF_REG	Divisor Latch Fraction Register
0x500200F8	UART_UCV_REG	Component Version
0x500200FC	UART_CTR_REG	Component Type Register
0x50020100	UART2_RBR_THR_DLL_REG	Receive Buffer Register
0x50020104	UART2_IER_DLH_REG	Interrupt Enable Register
0x50020108	UART2_IIR_FCR_REG	Interrupt Identification Register/FIFO Control Register
0x5002010C	UART2_LCR_REG	Line Control Register
0x50020110	UART2_MCR_REG	Modem Control Register

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Address	Register	Description
0x50020114	UART2_LSR_REG	Line Status Register
0x50020118	UART2_MSR_REG	Modem Status Register
0x5002011C	UART2_SCR_REG	Scratchpad Register
0x50020130	UART2_SRBR_STHR0_REG	Shadow Receive/Transmit Buffer Register
0x50020134	UART2_SRBR_STHR1_REG	Shadow Receive/Transmit Buffer Register
0x50020138	UART2_SRBR_STHR2_REG	Shadow Receive/Transmit Buffer Register
0x5002013C	UART2_SRBR_STHR3_REG	Shadow Receive/Transmit Buffer Register
0x50020140	UART2_SRBR_STHR4_REG	Shadow Receive/Transmit Buffer Register
0x50020144	UART2_SRBR_STHR5_REG	Shadow Receive/Transmit Buffer Register
0x50020148	UART2_SRBR_STHR6_REG	Shadow Receive/Transmit Buffer Register
0x5002014C	UART2_SRBR_STHR7_REG	Shadow Receive/Transmit Buffer Register
0x50020150	UART2_SRBR_STHR8_REG	Shadow Receive/Transmit Buffer Register
0x50020154	UART2_SRBR_STHR9_REG	Shadow Receive/Transmit Buffer Register
0x50020158	UART2_SRBR_STHR10_REG	Shadow Receive/Transmit Buffer Register
0x5002015C	UART2_SRBR_STHR11_REG	Shadow Receive/Transmit Buffer Register
0x50020160	UART2_SRBR_STHR12_REG	Shadow Receive/Transmit Buffer Register
0x50020164	UART2_SRBR_STHR13_REG	Shadow Receive/Transmit Buffer Register
0x50020168	UART2_SRBR_STHR14_REG	Shadow Receive/Transmit Buffer Register
0x5002016C	UART2_SRBR_STHR15_REG	Shadow Receive/Transmit Buffer Register
0x5002017C	UART2_USR_REG	UART Status register.
0x50020180	UART2_TFL_REG	Transmit FIFO Level
0x50020184	UART2_RFL_REG	Receive FIFO Level.
0x50020188	UART2_SRR_REG	Software Reset Register.
0x5002018C	UART2_SRTS_REG	Shadow Request to Send
0x50020190	UART2_SBCR_REG	Shadow Break Control Register
0x50020194	UART2_SDMAM_REG	Shadow DMA Mode
0x50020198	UART2_SFE_REG	Shadow FIFO Enable
0x5002019C	UART2_SRT_REG	Shadow RCVR Trigger
0x500201A0	UART2_STET_REG	Shadow TX Empty Trigger

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Address	Register	Description
0x500201A4	UART2_HTX_REG	Halt TX
0x500201A8	UART2_DMASA_REG	DMA Software Acknowledge
0x500201C0	UART2_DLF_REG	Divisor Latch Fraction Register
0x500201C4	UART2_RAR_REG	Receive Address Register
0x500201C8	UART2_TAR_REG	Transmit Address Register
0x500201CC	UART2_LCR_EXT	Line Extended Control Register
0x500201F8	UART2_UCV_REG	Component Version
0x500201FC	UART2_CTR_REG	Component Type Register
0x50020200	UART3_RBR_THR_DLL_REG	Receive Buffer Register
0x50020204	UART3_IER_DLH_REG	Interrupt Enable Register
0x50020208	UART3_IIR_FCR_REG	Interrupt Identification Register/FIFO Control Register
0x5002020C	UART3_LCR_REG	Line Control Register
0x50020210	UART3_MCR_REG	Modem Control Register
0x50020214	UART3_LSR_REG	Line Status Register
0x50020218	UART3_MSR_REG	Modem Status Register
0x5002021C	UART3_CONFIG_REG	ISO7816 Config Register
0x50020230	UART3_SRBR_STHR0_REG	Shadow Receive/Transmit Buffer Register
0x50020234	UART3_SRBR_STHR1_REG	Shadow Receive/Transmit Buffer Register
0x50020238	UART3_SRBR_STHR2_REG	Shadow Receive/Transmit Buffer Register
0x5002023C	UART3_SRBR_STHR3_REG	Shadow Receive/Transmit Buffer Register
0x50020240	UART3_SRBR_STHR4_REG	Shadow Receive/Transmit Buffer Register
0x50020244	UART3_SRBR_STHR5_REG	Shadow Receive/Transmit Buffer Register
0x50020248	UART3_SRBR_STHR6_REG	Shadow Receive/Transmit Buffer Register
0x5002024C	UART3_SRBR_STHR7_REG	Shadow Receive/Transmit Buffer Register
0x50020250	UART3_SRBR_STHR8_REG	Shadow Receive/Transmit Buffer Register
0x50020254	UART3_SRBR_STHR9_REG	Shadow Receive/Transmit Buffer Register
0x50020258	UART3_SRBR_STHR10_REG	Shadow Receive/Transmit Buffer Register
0x5002025C	UART3_SRBR_STHR11_REG	Shadow Receive/Transmit Buffer Register

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Address	Register	Description
0x50020260	UART3_SRBR_STHR12_REG	Shadow Receive/Transmit Buffer Register
0x50020264	UART3_SRBR_STHR13_REG	Shadow Receive/Transmit Buffer Register
0x50020268	UART3_SRBR_STHR14_REG	Shadow Receive/Transmit Buffer Register
0x5002026C	UART3_SRBR_STHR15_REG	Shadow Receive/Transmit Buffer Register
0x5002027C	UART3_USR_REG	UART Status register.
0x50020280	UART3_TFL_REG	Transmit FIFO Level
0x50020284	UART3_RFL_REG	Receive FIFO Level.
0x50020288	UART3_SRR_REG	Software Reset Register.
0x5002028C	UART3_SRTS_REG	Shadow Request to Send
0x50020290	UART3_SBCR_REG	Shadow Break Control Register
0x50020294	UART3_SDMAM_REG	Shadow DMA Mode
0x50020298	UART3_SFE_REG	Shadow FIFO Enable
0x5002029C	UART3_SRT_REG	Shadow RCVR Trigger
0x500202A0	UART3_STET_REG	Shadow TX Empty Trigger
0x500202A4	UART3_HTX_REG	Halt TX
0x500202A8	UART3_DMASA_REG	DMA Software Acknowledge
0x500202C0	UART3_DLF_REG	Divisor Latch Fraction Register
0x500202C4	UART3_RAR_REG	Receive Address Register
0x500202C8	UART3_TAR_REG	Transmit Address Register
0x500202CC	UART3_LCR_EXT	Line Extended Control Register
0x500202E0	UART3_CTRL_REG	ISO7816 Control Register
0x500202E4	UART3_TIMER_REG	ISO7816 Timer Register
0x500202E8	UART3_ERR_CTRL_REG	ISO7816 Error Signal Control Register
0x500202EC	UART3_IRQ_STATUS_REG	ISO7816 Interrupt Status Register
0x500202F8	UART3_UCV_REG	Component Version
0x500202FC	UART3_CTR_REG	Component Type Register

Table 1243: UART_RBR_THR_DLL_REG (0x50020000)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	RBR_THR_DLL	Receive Buffer Register: (RBR). This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If	0x0

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Bit	Mode	Symbol	Description	Reset
			FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Transmit Holding Register: (THR) This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost. Divisor Latch (Low): (DLL) This register makes up the lower 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor) Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications will occur. Also, once the DLL is set, at least 8 clock cycles of the slowest DW_apb_uart clock should be allowed to pass before transmitting or receiving data. Divisor Latch (High): (DLH) (Note: This register is placed in UART_IER_DLH_REG with offset 0x4) Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest DW_apb_uart clock should be allowed to pass before transmitting or receiving data.	

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Table 1244: UART_IER_DLH_REG (0x50020004)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	PTIME_DLH7	Interrupt Enable Register: PTIME, Programmable THRE Interrupt Mode Enable. This is used to enable/disable the generation of THRE Interrupt. 0 = disabled 1 = enabled Divisor Latch (High): Bit[7] of the 8 bit DLH register.	0x0
6:5	R/W	DLH6_5	Divisor Latch (High): Bit[6:5] of the 8 bit DLH register	0x0
4	R/W	ELCOLR_DLH4	Interrupt Enable Register: (read only) ELCOLR, this bit controls the method for clearing the status in the LSR register. This is applicable only for Overrun Error, Parity Error, Framing Error, and Break Interrupt status bits. Always 0 = LSR status bits are cleared either on reading Rx FIFO (RBR Read) or On reading LSR register. Divisor Latch (High): Bit[4] of the 8 bit DLH register	0x0
3	R/W	EDSSI_DLH3	Interrupt Enable Register: reserved Divisor Latch (High): Bit[3] of the 8 bit DLH register	0x0
2	R/W	ELSI_DLH2	Interrupt Enable Register: ELSI, Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0 = disabled 1 = enabled Divisor Latch (High): Bit[2] of the 8 bit DLH register.	0x0
1	R/W	ETBEI_DLH1	Interrupt Enable Register: ETBEI, Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0 = disabled 1 = enabled Divisor Latch (High): Bit[1] of the 8 bit DLH register.	0x0
0	R/W	ERBFI_DLH0	Interrupt Enable Register: ERBFI, Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFO's enabled). These are the second highest priority interrupts. 0 = disabled 1 = enabled Divisor Latch (High): Bit[0] of the 8 bit DLH register.	0x0

Table 1245: UART_IIR_FCR_REG (0x50020008)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	IIR_FCR	On Read Interrupt Identification Register :	0x1

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Bit	Mode	Symbol	Description	Reset
			Bits[7:6], FIFO's Enabled (or FIFOSE): This is used to indicate whether the FIFO's are enabled or disabled. 00 = disabled. 11 = enabled. Bits[5:4],Reserved Bits[3:0], Interrupt ID (or IID): This indicates the highest priority pending interrupt which can be one of the following types: 0001 = no interrupt pending. 0010 = THR empty. 0100 = received data available. 0110 = receiver line status. 0111 = busy detect. 1100 = character timeout. On Write FIFO Control Register Bits[7:6], RCVR Trigger (or RT):. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt will be generated. In auto flow control mode it is used to determine when the rts_n signal will be de-asserted. It also determines when the dma_rx_req_n signal will be asserted when in certain modes of operation. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO 1/4 full 10 = FIFO 1/2 full 11 = FIFO 2 less than full Bits[5:4], TX Empty Trigger (or TET): This is used to select the empty threshold level at which the THRE Interrupts will be generated when the mode is active. It also determines when the dma_tx_req_n signal will be asserted when in certain modes of operation. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO 1/4 full 11 = FIFO 1/2 full Bit[3], DMA Mode (or DMAM): This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals. 0 = mode 0 1 = mode 1 Bit[2], XMIT FIFO Reset (or XFIFOR): This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing' and it is not necessary to clear this bit. Bit[1], RCVR FIFO Reset (or RFIFOR): This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing' and it is not necessary to clear this bit. Bit[0], FIFO Enable (or FIFOE): This enables/disables the transmit (XMIT) and receive (RCVR) FIFO's. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFO's will be reset.	

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Table 1246: UART_LCR_REG (0x5002000C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	UART_DLAB	Divisor Latch Access Bit. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.	0x0
6	R/W	UART_BC	Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared.	0x0
5	-	-	Reserved	0x0
4	R/W	UART_EPS	Even Parity Select. Writeable only when UART is not busy (USR[0] is zero). This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.	0x0
3	R/W	UART_PEN	Parity Enable. Writeable only when UART is not busy (USR[0] is zero) This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0 = parity disabled 1 = parity enabled	0x0
2	R/W	UART_STOP	Number of stop bits. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0 = 1 stop bit 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit	0x0
1:0	R/W	UART_DLS	Data Length Select. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits	0x0

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Table 1247: UART_MCR_REG (0x50020010)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6	R/W	-	Reserved	0x0
5	R/W	-	Reserved	0x0
4	R/W	UART_LB	LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.	0x0
3	R/W	-	Reserved	0x0
2	R/W	-	Reserved	0x0
1	R/W	-	Reserved	0x0
0	R/W	-	Reserved	0x0

Table 1248: UART_LSR_REG (0x50020014)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R	UART_RFE	Receiver FIFO Error bit. This bit is only relevant when FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 0 = no error in RX FIFO 1 = error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.	0x0
6	R	UART_TEMT	Transmitter Empty bit. If FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.	0x1
5	R	UART_THRE	Transmit Holding Register Empty bit.	0x1

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Bit	Mode	Symbol	Description	Reset
			If THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.	
4	R	UART_BI	Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. It is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.	0x0
3	R	UART_FE	Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no framing error 1 = framing error Reading the LSR clears the FE bit.	0x0
2	R	UART_PE	Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO.	0x0

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Bit	Mode	Symbol	Description	Reset
			It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no parity error 1 = parity error Reading the LSR clears the PE bit.	
1	R	UART_OE	Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0 = no overrun error 1 = overrun error Reading the LSR clears the OE bit.	0x0
0	R	UART_DR	Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0 = no data ready 1 = data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.	0x0

Table 1249: UART_SCR_REG (0x5002001C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	UART_SCRATCH_PAD	This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART Ctrl.	0x0

Table 1250: UART_SRBR_STHR0_REG (0x50020030)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The	0x0

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Bit	Mode	Symbol	Description	Reset
			data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1251: UART_SRBR_STHR1_REG (0x50020034)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be	0x0

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Bit	Mode	Symbol	Description	Reset
			transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1252: UART_SRBR_STHR2_REG (0x50020038)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration.	0x0

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Bit	Mode	Symbol	Description	Reset
			Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1253: UART_SRBR_STHR3_REG (0x5002003C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

Table 1254: UART_SRBR_STHR4_REG (0x50020040)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on	0x0

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Bit	Mode	Symbol	Description	Reset
			the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1255: UART_SRBR_STHR5_REG (0x50020044)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit	0x0

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Bit	Mode	Symbol	Description	Reset
			locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1256: UART_SRBR_STHR6_REG (0x50020048)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration.	0x0

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Bit	Mode	Symbol	Description	Reset
			Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1257: UART_SRBR_STHR7_REG (0x5002004C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

Table 1258: UART_SRBR_STHR8_REG (0x50020050)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on	0x0

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Bit	Mode	Symbol	Description	Reset
			the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1259: UART_SRBR_STHR9_REG (0x50020054)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit	0x0

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Bit	Mode	Symbol	Description	Reset
			locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1260: UART_SRBR_STHR10_REG (0x50020058)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration.	0x0

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Bit	Mode	Symbol	Description	Reset
			Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1261: UART_SRBR_STHR11_REG (0x5002005C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

Table 1262: UART_SRBR_STHR12_REG (0x50020060)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on	0x0

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Bit	Mode	Symbol	Description	Reset
			the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1263: UART_SRBR_STHR13_REG (0x50020064)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit	0x0

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Bit	Mode	Symbol	Description	Reset
			locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1264: UART_SRBR_STHR14_REG (0x50020068)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration.	0x0

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Bit	Mode	Symbol	Description	Reset
			Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1265: UART_SRBR_STHR15_REG (0x5002006C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

Table 1266: UART_USR_REG (0x5002007C)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4	R	UART_RFF	Receive FIFO Full. This is used to indicate that the receive FIFO is completely full. 0 = Receive FIFO not full	0x0

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Bit	Mode	Symbol	Description	Reset
			1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.	
3	R	UART_RFNE	Receive FIFO Not Empty. This is used to indicate that the receive FIFO contains one or more entries. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.	0x0
2	R	UART_TFE	Transmit FIFO Empty. This is used to indicate that the transmit FIFO is completely empty. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.	0x1
1	R	UART_TFNF	Transmit FIFO Not Full. This is used to indicate that the transmit FIFO in not full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full.	0x1
0	R	UART_BUSY	UART Busy. This indicates that a serial transfer is in progress, when cleared indicates that the uart is idle or inactive. 0 = uart is idle or inactive 1 =uart is busy (actively transferring data) Note that it is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the uart has no data in the THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the uart. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled) the assertion of this bit will also be delayed by several cycles of the slower clock.	0x0

Table 1267: UART_TFL_REG (0x50020080)

Bit	Mode	Symbol	Description	Reset
4:0	R	UART_TRANSMIT_FIFO_LEVEL	Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO.	0x0

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Table 1268: UART_RFL_REG (0x50020084)

Bit	Mode	Symbol	Description	Reset
4:0	R	UART_RECEIVE_FIFO_LEVEL	Receive FIFO Level. This is indicates the number of data entries in the receive FIFO.	0x0

Table 1269: UART_SRR_REG (0x50020088)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	0x0
2	W	UART_XFR	XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.	0x0
1	W	UART_RFR	RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.	0x0
0	W	UART_UR	UART Reset. This asynchronously resets the UART Ctrl and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset.	0x0

Table 1270: UART_SBCR_REG (0x50020090)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R/W	UART_SHADOW_BREAK_CONTROL	Shadow Break Control Bit. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared.	0x0

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Table 1271: UART_SDMAM_REG (0x50020094)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R/W	UART_SHADOW_DMA_MODE	Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals. 0 = mode 0 1 = mode 1	0x0

Table 1272: UART_SFE_REG (0x50020098)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R/W	UART_SHADOW_FIFO_ENABLE	Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset.	0x0

Table 1273: UART_SRT_REG (0x5002009C)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	0x0
1:0	R/W	UART_SHADOW_RCVR_TRIGGER	Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO ¼ full 10 = FIFO ½ full 11 = FIFO 2 less than full	0x0

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Table 1274: UART_STET_REG (0x500200A0)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	0x0
1:0	R/W	UART_SHADOW_TX_EMPTY_TRIGGER	Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO ¼ full 11 = FIFO ½ full	0x0

Table 1275: UART_HTX_REG (0x500200A4)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R/W	UART_HALT_TX	This register is use to halt transmissions, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 = Halt TX disabled 1 = Halt TX enabled Note, if FIFOs are not enabled, the setting of the halt TX register has no effect on operation.	0x0

Table 1276: UART_DMASA_REG (0x500200A8)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	W	UART_DMASA	This register is use to perform DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This will cause the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing' and it is not necessary to clear this bit.	0x0

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Table 1277: UART_DLF_REG (0x500200C0)

Bit	Mode	Symbol	Description	Reset
3:0	R/W	UART_DLF	The fractional value is added to integer value set by DLH, DLL. Fractional value is equal UART_DLF/16	0x0

Table 1278: UART_UCV_REG (0x500200F8)

Bit	Mode	Symbol	Description	Reset
31:0	R	UART_UCV	Component Version	0x3430312A

Table 1279: UART_CTR_REG (0x500200FC)

Bit	Mode	Symbol	Description	Reset
31:0	R	UART_CTR	Component Type Register	0x44570110

Table 1280: UART2_RBR_THR_DLL_REG (0x50020100)

Bit	Mode	Symbol	Description	Reset
8	R/W	RBR_THR_9BIT	When 9BIT_DATA_EN, On read :Receive Buffer bit 8 - On write Transmit Buffer bit 8 when LCR_EXT[3]=1	0x0
7:0	R/W	RBR_THR_DLL	Receive Buffer Register: (RBR). This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Transmit Holding Register: (THR) This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is	0x0

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Bit	Mode	Symbol	Description	Reset
			full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost. Divisor Latch (Low): (DLL) This register makes up the lower 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor) Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications will occur. Also, once the DLL is set, at least 8 clock cycles of the slowest DW_apb_uart clock should be allowed to pass before transmitting or receiving data. Divisor Latch (High): (DLH) (Note: This register is placed in UART_IER_DLH_REG with offset 0x4) Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest DW_apb_uart clock should be allowed to pass before transmitting or receiving data.	

Table 1281: UART2_IER_DLH_REG (0x50020104)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	PTIME_DLH7	Interrupt Enable Register: PTIME, Programmable THRE Interrupt Mode Enable. This is used to enable/disable the generation of THRE Interrupt. 0 = disabled 1 = enabled Divisor Latch (High): Bit[7] of the 8 bit DLH register.	0x0
6:5	R/W	DLH6_5	Divisor Latch (High): Bit[6:5] of the 8 bit DLH register	0x0
4	R/W	ELCOLR_DLH4	Interrupt Enable Register: ELCOLR (read only), this bit controls the method for clearing the status in the LSR register. This is applicable only for Overrun Error, Parity Error, Framing Error, and Break Interrupt status bits. 0 = LSR status bits are cleared either on reading Rx FIFO (RBR Read) or On reading LSR register.	0x0

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Bit	Mode	Symbol	Description	Reset
			Divisor Latch (High): Bit[4] of the 8 bit DLH register	
3	R/W	EDSSI_DLH3	Interrupt Enable Register: EDSSI, Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0 = disabled 1 = enabled Divisor Latch (High): Bit[3] of the 8 bit DLH register	0x0
2	R/W	ELSI_DLH2	Interrupt Enable Register: ELSI, Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0 = disabled 1 = enabled Divisor Latch (High): Bit[2] of the 8 bit DLH register.	0x0
1	R/W	ETBEI_DLH1	Interrupt Enable Register: ETBEI, Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0 = disabled 1 = enabled Divisor Latch (High): Bit[1] of the 8 bit DLH register.	0x0
0	R/W	ERBFI_DLH0	Interrupt Enable Register: ERBFI, Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFO's enabled). These are the second highest priority interrupts. 0 = disabled 1 = enabled Divisor Latch (High): Bit[0] of the 8 bit DLH register.	0x0

Table 1282: UART2_IIR_FCR_REG (0x50020108)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	IIR_FCR	On Read Interrupt Identification Register : Bits[7:6], FIFO's Enabled (or FIFOSE): This is used to indicate whether the FIFO's are enabled or disabled. 00 = disabled. 11 = enabled. Bits[5:4],Reserved Bits[3:0], Interrupt ID (or IID): This indicates the highest priority pending interrupt which can be one of the following types:0001 = no interrupt pending. 0010 = THR empty. 0100 = received data available. 0110 = receiver line status. 0111 = busy detect. 1100 = character timeout. On Write FIFO Control Register Bits[7:6], RCVR Trigger (or RT):. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt will be generated. In auto flow control mode it is used to determine when the rts_n signal will be de-asserted. It also determines when the	0x1

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Bit	Mode	Symbol	Description	Reset
			dma_rx_req_n signal will be asserted when in certain modes of operation. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO 1/4 full 10 = FIFO 1/2 full 11 = FIFO 2 less than full Bits[5:4], TX Empty Trigger (or TET): This is used to select the empty threshold level at which the THRE Interrupts will be generated when the mode is active. It also determines when the dma_tx_req_n signal will be asserted when in certain modes of operation. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO 1/4 full 11 = FIFO 1/2 full Bit[3], DMA Mode (or DMAM): This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals. 0 = mode 0 1 = mode 1 Bit[2], XMIT FIFO Reset (or XFIFOR): This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing' and it is not necessary to clear this bit. Bit[1], RCVR FIFO Reset (or RFIFOR): This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing' and it is not necessary to clear this bit. Bit[0], FIFO Enable (or FIFOE): This enables/disables the transmit (XMIT) and receive (RCVR) FIFO's. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFO's will be reset.	

Table 1283: UART2_LCR_REG (0x5002010C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	UART_DLAB	Divisor Latch Access Bit. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.	0x0
6	R/W	UART_BC	Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared.	0x0
5	R/W	UART_SP	Stick Parity. (writeable only when UART is not busy USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and	0x0

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Bit	Mode	Symbol	Description	Reset
			checked as a logic 1. If this bit is set to 0, Stick Parity is disabled.	
4	R/W	UART_EPS	Even Parity Select. Writeable only when UART is not busy (USR[0] is zero). This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.	0x0
3	R/W	UART_PEN	Parity Enable. Writeable only when UART is not busy (USR[0] is zero) This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0 = parity disabled 1 = parity enabled	0x0
2	R/W	UART_STOP	Number of stop bits. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0 = 1 stop bit 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit	0x0
1:0	R/W	UART_DLS	Data Length Select. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits	0x0

Table 1284: UART2_MCR_REG (0x50020110)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6	R/W	-	Reserved	0x0
5	R/W	UART_AFCE	Auto Flow Control Enable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in "Auto Flow Control". 0 = Auto Flow Control Mode disabled 1 = Auto Flow Control Mode enabled	0x0

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Bit	Mode	Symbol	Description	Reset
4	R/W	UART_LB	LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. Data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n) are looped back to the inputs, internally.	0x0
3	R/W	-	Reserved	0x0
2	R/W	-	Reserved	0x0
1	R/W	UART_RTS	Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.	0x0
0	R/W	-	Reserved	0x0

Table 1285: UART2_LSR_REG (0x50020114)

Bit	Mode	Symbol	Description	Reset
8	R	UART_ADDR_RCVD	Address Received Bit. If 9Bit data mode (LCR_EXT[0]=1) is enabled, this bit is used to indicate the 9th bit of the receive data is set to 1. This bit can also be used to indicate whether the incoming character is address or data. 1 = Indicates the character is address. 0 = Indicates the character is data. In the FIFO mode, since the 9th bit is associated with a character received, it is revealed when the character with the 9th bit set to 1 is at the top of the FIFO. Reading the LSR clears the 9BIT. Note: User needs to ensure that interrupt gets cleared (reading LSR register) before the next address byte arrives. If there is a delay in clearing the interrupt, then Software will not be able to distinguish between multiple address related interrupt.	0x0

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Bit	Mode	Symbol	Description	Reset
7	R	UART_RFE	Receiver FIFO Error bit. This bit is only relevant when FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 0 = no error in RX FIFO 1 = error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.	0x0
6	R	UART_TEMT	Transmitter Empty bit. If FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.	0x1
5	R	UART_THRE	Transmit Holding Register Empty bit. If THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.	0x1
4	R	UART_BI	Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.	0x0
3	R	UART_FE	Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO.	0x0

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Bit	Mode	Symbol	Description	Reset
			When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no framing error 1 = framing error Reading the LSR clears the FE bit.	
2	R	UART_PE	Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no parity error 1 = parity error Reading the LSR clears the PE bit.	0x0
1	R	UART_OE	Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0 = no overrun error 1 = overrun error Reading the LSR clears the OE bit.	0x0
0	R	UART_DR	Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0 = no data ready 1 = data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.	0x0

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Table 1286: UART2_MSR_REG (0x50020118)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4	R	UART_CTS	Clear to Send. This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the UART Ctrl. 0 = cts_n input is de-asserted (logic 1) 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).	0x1
3:1	-	-	Reserved	0x0
0	R	UART_DCTS	Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0 = no change on cts_n since last read of MSR 1 = change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.	0x0

Table 1287: UART2_SCR_REG (0x5002011C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	UART_SCRATCH_PAD	This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART Ctrl.	0x0

Table 1288: UART2_SRBR_STHR0_REG (0x50020130)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If	0x0

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Bit	Mode	Symbol	Description	Reset
			FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1289: UART2_SRBR_STHR1_REG (0x50020134)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output	0x0

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Bit	Mode	Symbol	Description	Reset
			(sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1290: UART2_SRBR_STHR2_REG (0x50020138)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

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Table 1291: UART2_SRBR_STHR3_REG (0x5002013C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

Table 1292: UART2_SRBR_STHR4_REG (0x50020140)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data	0x0

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Bit	Mode	Symbol	Description	Reset
			in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1293: UART2_SRBR_STHR5_REG (0x50020144)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be	0x0

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Bit	Mode	Symbol	Description	Reset
			written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1294: UART2_SRBR_STHR6_REG (0x50020148)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

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Table 1295: UART2_SRBR_STHR7_REG (0x5002014C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

Table 1296: UART2_SRBR_STHR8_REG (0x50020150)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in	0x0

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Bit	Mode	Symbol	Description	Reset
			an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1297: UART2_SRBR_STHR9_REG (0x50020154)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0]	0x0

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Bit	Mode	Symbol	Description	Reset
			set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1298: UART2_SRBR_STHR10_REG (0x50020158)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

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Table 1299: UART2_SRBR_STHR11_REG (0x5002015C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

Table 1300: UART2_SRBR_STHR12_REG (0x50020160)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in	0x0

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Bit	Mode	Symbol	Description	Reset
			an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1301: UART2_SRBR_STHR13_REG (0x50020164)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0]	0x0

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Bit	Mode	Symbol	Description	Reset
			set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1302: UART2_SRBR_STHR14_REG (0x50020168)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

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Table 1303: UART2_SRBR_STHR15_REG (0x5002016C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

Table 1304: UART2_USR_REG (0x5002017C)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4	R	UART_RFF	Receive FIFO Full. This is used to indicate that the receive FIFO is completely full. 0 = Receive FIFO not full 1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.	0x0
3	R	UART_RFNE	Receive FIFO Not Empty. This is used to indicate that the receive FIFO contains one or more entries.	0x0

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Bit	Mode	Symbol	Description	Reset
			0 = Receive FIFO is empty 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.	
2	R	UART_TFE	Transmit FIFO Empty. This is used to indicate that the transmit FIFO is completely empty. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.	0x1
1	R	UART_TFNF	Transmit FIFO Not Full. This is used to indicate that the transmit FIFO in not full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full.	0x1
0	R	UART_BUSY	UART Busy. This indicates that a serial transfer is in progress, when cleared indicates that the DW_apb_uart is idle or inactive. 0 - DW_apb_uart is idle or inactive 1 - DW_apb_uart is busy (actively transferring data) Note that it is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the DW_apb_uart has no data in the THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the DW_apb_uart. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled) the assertion of this bit will also be delayed by several cycles of the slower clock.	0x0

Table 1305: UART2_TFL_REG (0x50020180)

Bit	Mode	Symbol	Description	Reset
4:0	R	UART_TRANSMIT_FIFO_LEVEL	Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO.	0x0

Table 1306: UART2_RFL_REG (0x50020184)

Bit	Mode	Symbol	Description	Reset
4:0	R	UART_RECEIVE_FIFO_LEVEL	Receive FIFO Level. This is indicates the number of data entries in the receive FIFO.	0x0

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Table 1307: UART2_SRR_REG (0x50020188)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	0x0
2	W	UART_XFR	XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.	0x0
1	W	UART_RFR	RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.	0x0
0	W	UART_UR	UART Reset. This asynchronously resets the UART Ctrl and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset.	0x0

Table 1308: UART2_SRTS_REG (0x5002018C)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R/W	UART_SHADOW_REQUEST_TO_SEND	Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART Ctrl is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, (active MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input.	0x0

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Table 1309: UART2_SBCR_REG (0x50020190)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R/W	UART_SHADOW_BREAK_CONTROL	Shadow Break Control Bit. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared.	0x0

Table 1310: UART2_SDMAM_REG (0x50020194)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R/W	UART_SHADOW_DMA_MODE	Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals. 0 = mode 0 1 = mode 1	0x0

Table 1311: UART2_SFE_REG (0x50020198)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R/W	UART_SHADOW_FIFO_ENABLE	Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset.	0x0

Table 1312: UART2_SRT_REG (0x5002019C)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	0x0
1:0	R/W	UART_SHADOW_RCVR_TRIGGER	Shadow RCVR Trigger.	0x0

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Bit	Mode	Symbol	Description	Reset
			This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO ¼ full 10 = FIFO ½ full 11 = FIFO 2 less than full	

Table 1313: UART2_STET_REG (0x500201A0)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	0x0
1:0	R/W	UART_SHADOW_TX_EMPTY_TRIGGER	Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO ¼ full 11 = FIFO ½ full	0x0

Table 1314: UART2_HTX_REG (0x500201A4)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R/W	UART_HALT_TX	This register is use to halt transmissions, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 = Halt TX disabled 1 = Halt TX enabled Note, if FIFOs are not enabled, the setting of the halt TX register has no effect on operation.	0x0

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Table 1315: UART2_DMASA_REG (0x500201A8)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	W	UART_DMASA	This register is use to perform DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This will cause the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing' and it is not necessary to clear this bit.	0x0

Table 1316: UART2_DLF_REG (0x500201C0)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	0x0
3:0	R/W	UART_DLF	The fractional value is added to integer value set by DLH, DLL. Fractional value is equal UART_DLF/16	0x0

Table 1317: UART2_RAR_REG (0x500201C4)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	UART_RAR	This is an address matching register during receive mode. If the 9-th bit is set in the incoming character then the remaining 8-bits will be checked against this register value. If the match happens then sub-sequent characters with 9-th bit set to 0 will be treated as data byte until the next address byte is received. Note: - This register is applicable only when 'ADDR_MATCH'(LCR_EXT[1] and 'DLS_E' (LCR_EXT[0]) bits are set to 1. RAR should be programmed only when UART is not busy.	0x0

Table 1318: UART2_TAR_REG (0x500201C8)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	UART_TAR	This is an address matching register during transmit mode. If DLS_E (LCR_EXT[0]) bit is enabled, then uart will send the 9-bit character with 9-th bit set to 1 and remaining 8-bit address will be sent from this register provided 'SEND_ADDR' (LCR_EXT[2]) bit is set to 1. Note: - This register is used only to send the address. The normal data should be sent by programming THR register.	0x0

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Bit	Mode	Symbol	Description	Reset
			- Once the address is started to send on the DW_apb_uart serial lane, then 'SEND_ADDR' bit will be auto-cleared by the hardware.	

Table 1319: UART2_LCR_EXT (0x500201CC)

Bit	Mode	Symbol	Description	Reset
3	R/W	UART_TRANSMIT_MODE	Transmit mode control bit. This bit is used to control the type of transmit mode during 9-bit data transfers. 1 = In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding Register (STHR) are 9-bit wide. The user needs to ensure that the THR/STHR register is written correctly for address/data. Address: 9th bit is set to 1, Data : 9th bit is set to 0. Note: Transmit address register (TAR) is not applicable in this mode of operation. 0 = In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding register (STHR) are 8-bit wide. The user needs to program the address into Transmit Address Register (TAR) and data into the THR/STHR register. SEND_ADDR bit is used as a control knob to indicate the uart on when to send the address.	0x0
2	R/W	UART_SEND_ADDR	Send address control bit. This bit is used as a control knob for the user to determine when to send the address during transmit mode. 1 = 9-bit character will be transmitted with 9-th bit set to 1 and the remaining 8-bits will match to what is being programmed in 'Transmit Address Register'. 0 = 9-bit character will be transmitted with 9-th bit set to 0 and the remaining 8-bits will be taken from the TXFIFO which is programmed through 8-bit wide THR/STHR register. Note: 1. This bit is auto-cleared by the hardware, after sending out the address character. User is not expected to program this bit to 0. 2. This field is applicable only when DLS_E bit is set to 1 and TRANSMIT_MODE is set to 0.	0x0
1	R/W	UART_ADDR_MATCH	Address Match Mode.This bit is used to enable the address match feature during receive. 1 = Address match mode; uart will wait until the incoming character with 9-th bit set to 1. And further checks to see if the address matches with what is programmed in 'Receive Address Match Register'. If match is found, then sub-sequent characters will be treated as valid data and DW_apb_uart starts receiving data. 0 = Normal mode; DW_apb_uart will start to receive the data and 9-bit character will be formed and written into the receive RXFIFO. User is	0x0

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Bit	Mode	Symbol	Description	Reset
			responsible to read the data and differentiate b/n address and data. Note: This field is applicable only when DLS_E is set to 1.	
0	R/W	UART_DLS_E	Extension for DLS. This bit is used to enable 9-bit data for transmit and receive transfers.	0x0

Table 1320: UART2_UCV_REG (0x500201F8)

Bit	Mode	Symbol	Description	Reset
31:0	R	UART_UCV	Component Version	0x3430312A

Table 1321: UART2_CTR_REG (0x500201FC)

Bit	Mode	Symbol	Description	Reset
31:0	R	UART_CTR	Component Type Register	0x44570110

Table 1322: UART3_RBR_THR_DLL_REG (0x50020200)

Bit	Mode	Symbol	Description	Reset
8	R/W	RBR_THR_9BIT	When 9BIT_DATA_EN, On read :Receive Buffer bit 8 - On write Transmit Buffer bit 8 when LCR_EXT[3]=1	0x0
7:0	R/W	RBR_THR_DLL	Receive Buffer Register: (RBR). This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Transmit Holding Register: (THR) This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to	0x0

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Bit	Mode	Symbol	Description	Reset
			one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost. Divisor Latch (Low): (DLL) This register makes up the lower 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor) Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications will occur. Also, once the DLL is set, at least 8 clock cycles of the slowest DW_apb_uart clock should be allowed to pass before transmitting or receiving data. Divisor Latch (High): (DLH) (Note: This register is placed in UART_IER_DLH_REG with offset 0x4) Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest DW_apb_uart clock should be allowed to pass before transmitting or receiving data.	

Table 1323: UART3_IER_DLH_REG (0x50020204)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	PTIME_DLH7	Interrupt Enable Register: PTIME, Programmable THRE Interrupt Mode Enable. This is used to enable/disable the generation of THRE Interrupt. 0 = disabled 1 = enabled Divisor Latch (High): Bit[7] of the 8 bit DLH register.	0x0
6:5	R/W	DLH6_5	Divisor Latch (High): Bit[6:5] of the 8 bit DLH register	0x0
4	R/W	ELCOLR_DLH4	Interrupt Enable Register: ELCOLR (read only), this bit controls the method for clearing the status in the LSR register. This is applicable only for Overrun Error, Parity Error, Framing Error, and Break Interrupt status bits.	0x0

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Bit	Mode	Symbol	Description	Reset
			0 = LSR status bits are cleared either on reading Rx FIFO (RBR Read) or On reading LSR register. Divisor Latch (High): Bit[4] of the 8 bit DLH register	
3	R/W	EDSSI_DLH3	Interrupt Enable Register: EDSSI, Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0 = disabled 1 = enabled Divisor Latch (High): Bit[3] of the 8 bit DLH register	0x0
2	R/W	ELSI_DLH2	Interrupt Enable Register: ELSI, Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0 = disabled 1 = enabled Divisor Latch (High): Bit[2] of the 8 bit DLH register.	0x0
1	R/W	ETBEI_DLH1	Interrupt Enable Register: ETBEI, Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0 = disabled 1 = enabled Divisor Latch (High): Bit[1] of the 8 bit DLH register.	0x0
0	R/W	ERBFI_DLH0	Interrupt Enable Register: ERBFI, Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFO's enabled). These are the second highest priority interrupts. 0 = disabled 1 = enabled Divisor Latch (High): Bit[0] of the 8 bit DLH register.	0x0

Table 1324: UART3_IIR_FCR_REG (0x50020208)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	IIR_FCR	On Read Interrupt Identification Register : Bits[7:6], FIFO's Enabled (or FIFOSE): This is used to indicate whether the FIFO's are enabled or disabled. 00 = disabled. 11 = enabled. Bits[5:4],Reserved Bits[3:0], Interrupt ID (or IID): This indicates the highest priority pending interrupt which can be one of the following types:0001 = no interrupt pending. 0010 = THR empty. 0100 = received data available. 0110 = receiver line status. 0111 = busy detect. 1100 = character timeout. On Write FIFO Control Register Bits[7:6], RCVR Trigger (or RT):. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt will	0x1

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Bit	Mode	Symbol	Description	Reset
			be generated. In auto flow control mode it is used to determine when the rts_n signal will be de-asserted. It also determines when the dma_rx_req_n signal will be asserted when in certain modes of operation. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO 1/4 full 10 = FIFO 1/2 full 11 = FIFO 2 less than full Bits[5:4], TX Empty Trigger (or TET): This is used to select the empty threshold level at which the THRE Interrupts will be generated when the mode is active. It also determines when the dma_tx_req_n signal will be asserted when in certain modes of operation. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO 1/4 full 11 = FIFO 1/2 full Bit[3], DMA Mode (or DMAM): This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals. 0 = mode 0 1 = mode 1 Bit[2], XMIT FIFO Reset (or XFIFOR): This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing' and it is not necessary to clear this bit. Bit[1], RCVR FIFO Reset (or RFIFOR): This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing' and it is not necessary to clear this bit. Bit[0], FIFO Enable (or FIFOE): This enables/disables the transmit (XMIT) and receive (RCVR) FIFO's. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFO's will be reset.	

Table 1325: UART3_LCR_REG (0x5002020C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	UART_DLAB	Divisor Latch Access Bit. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.	0x0
6	R/W	UART_BC	Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared.	0x0
5	R/W	UART_SP	Stick Parity. (writeable only when UART is not busy USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to	0x0

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Bit	Mode	Symbol	Description	Reset
			1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled.	
4	R/W	UART_EPS	Even Parity Select. Writeable only when UART is not busy (USR[0] is zero). This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.	0x0
3	R/W	UART_PEN	Parity Enable. Writeable only when UART is not busy (USR[0] is zero) This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0 = parity disabled 1 = parity enabled	0x0
2	R/W	UART_STOP	Number of stop bits. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0 = 1 stop bit 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit	0x0
1:0	R/W	UART_DLS	Data Length Select. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits	0x0

Table 1326: UART3_MCR_REG (0x50020210)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6	R/W	-	Reserved	0x0
5	R/W	UART_AFCE	Auto Flow Control Enable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow	0x0

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Bit	Mode	Symbol	Description	Reset
			Control features are enabled as described in "Auto Flow Control". 0 = Auto Flow Control Mode disabled 1 = Auto Flow Control Mode enabled	
4	R/W	UART_LB	LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. Data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n) are looped back to the inputs, internally.	0x0
3	R/W	-	Reserved	0x0
2	R/W	-	Reserved	0x0
1	R/W	UART_RTS	Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.	0x0
0	R/W	-	Reserved	0x0

Table 1327: UART3_LSR_REG (0x50020214)

Bit	Mode	Symbol	Description	Reset
8	R	UART_ADDR_RCVD	Address Received Bit. If 9Bit data mode (LCR_EXT[0]=1) is enabled, this bit is used to indicate the 9th bit of the receive data is set to 1. This bit can also be used to indicate whether the incoming character is address or data. 1 = Indicates the character is address. 0 = Indicates the character is data. In the FIFO mode, since the 9th bit is associated with a character received, it is revealed when the character with the 9th bit set to 1 is at the top of the FIFO. Reading the LSR clears the 9BIT.	0x0

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Bit	Mode	Symbol	Description	Reset
			Note: User needs to ensure that interrupt gets cleared (reading LSR register) before the next address byte arrives. If there is a delay in clearing the interrupt, then Software will not be able to distinguish between multiple address related interrupt.	
7	R	UART_RFE	Receiver FIFO Error bit. This bit is only relevant when FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 0 = no error in RX FIFO 1 = error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.	0x0
6	R	UART_TEMT	Transmitter Empty bit. If FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.	0x1
5	R	UART_THRE	Transmit Holding Register Empty bit. If THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.	0x1
4	R	UART_BI	Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.	0x0
3	R	UART_FE	Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error	0x0

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Bit	Mode	Symbol	Description	Reset
			occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no framing error 1 = framing error Reading the LSR clears the FE bit.	
2	R	UART_PE	Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no parity error 1 = parity error Reading the LSR clears the PE bit.	0x0
1	R	UART_OE	Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0 = no overrun error 1 = overrun error Reading the LSR clears the OE bit.	0x0
0	R	UART_DR	Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0 = no data ready 1 = data ready	0x0

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Bit	Mode	Symbol	Description	Reset
			This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.	

Table 1328: UART3_MSR_REG (0x50020218)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4	R	UART_CTS	Clear to Send. This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the UART Ctrl. 0 = cts_n input is de-asserted (logic 1) 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).	0x1
3:1	-	-	Reserved	0x0
0	R	UART_DCTS	Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0 = no change on cts_n since last read of MSR 1 = change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.	0x0

Table 1329: UART3_CONFIG_REG (0x5002021C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:3	R/W	ISO7816_SCRATCH_PAD	This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART Ctrl.	0x0
2	R/W	ISO7816_ENABLE	0 : Normal Uart 1 : ISO7816 Enabled	0x0
1	R/W	ISO7816_ERR_SIG_EN	0 : Error Signal feature disabled 1 : Error Signal feature enabled	0x0
0	R/W	ISO7816_CONVENTION	0 : Direct convention 1 : Inverse convention	0x0

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Bit	Mode	Symbol	Description	Reset

Table 1330: UART3_SRBR_STHR0_REG (0x50020230)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

Table 1331: UART3_SRBR_STHR1_REG (0x50020234)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the	0x0

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Bit	Mode	Symbol	Description	Reset
			serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1332: UART3_SRBR_STHR2_REG (0x50020238)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses	0x0

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Bit	Mode	Symbol	Description	Reset
			from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1333: UART3_SRBR_STHR3_REG (0x5002023C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration.	0x0

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Bit	Mode	Symbol	Description	Reset
			Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1334: UART3_SRBR_STHR4_REG (0x50020240)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

Table 1335: UART3_SRBR_STHR5_REG (0x50020244)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on	0x0

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Bit	Mode	Symbol	Description	Reset
			the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1336: UART3_SRBR_STHR6_REG (0x50020248)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit	0x0

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Bit	Mode	Symbol	Description	Reset
			locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1337: UART3_SRBR_STHR7_REG (0x5002024C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration.	0x0

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Bit	Mode	Symbol	Description	Reset
			Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1338: UART3_SRBR_STHR8_REG (0x50020250)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

Table 1339: UART3_SRBR_STHR9_REG (0x50020254)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on	0x0

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Bit	Mode	Symbol	Description	Reset
			the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1340: UART3_SRBR_STHR10_REG (0x50020258)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit	0x0

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Bit	Mode	Symbol	Description	Reset
			locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1341: UART3_SRBR_STHR11_REG (0x5002025C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration.	0x0

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Bit	Mode	Symbol	Description	Reset
			Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1342: UART3_SRBR_STHR12_REG (0x50020260)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	0x0

Table 1343: UART3_SRBR_STHR13_REG (0x50020264)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on	0x0

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Bit	Mode	Symbol	Description	Reset
			the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1344: UART3_SRBR_STHR14_REG (0x50020268)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit	0x0

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Bit	Mode	Symbol	Description	Reset
			locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1345: UART3_SRBR_STHR15_REG (0x5002026C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R/W	SRBR_STHRx	Shadow Receive Buffer Register x: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Shadow Transmit Holding Register 0: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration.	0x0

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Bit	Mode	Symbol	Description	Reset
			Any attempt to write data when the FIFO is full results in the write data being lost.	

Table 1346: UART3_USR_REG (0x5002027C)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4	R	UART_RFF	Receive FIFO Full. This is used to indicate that the receive FIFO is completely full. 0 = Receive FIFO not full 1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.	0x0
3	R	UART_RFNE	Receive FIFO Not Empty. This is used to indicate that the receive FIFO contains one or more entries. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.	0x0
2	R	UART_TFE	Transmit FIFO Empty. This is used to indicate that the transmit FIFO is completely empty. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.	0x1
1	R	UART_TFNF	Transmit FIFO Not Full. This is used to indicate that the transmit FIFO in not full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full.	0x1
0	R	UART_BUSY	UART Busy. This indicates that a serial transfer is in progress, when cleared indicates that the DW_apb_uart is idle or inactive. 0 - DW_apb_uart is idle or inactive 1 - DW_apb_uart is busy (actively transferring data) Note that it is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the DW_apb_uart has no data in the THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the DW_apb_uart. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled) the assertion of this bit will also be delayed by several cycles of the slower clock.	0x0

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Table 1347: UART3_TFL_REG (0x50020280)

Bit	Mode	Symbol	Description	Reset
4:0	R	UART_TRANSMIT_FIFO_LEVEL	Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO.	0x0

Table 1348: UART3_RFL_REG (0x50020284)

Bit	Mode	Symbol	Description	Reset
4:0	R	UART_RECEIVE_FIFO_LEVEL	Receive FIFO Level. This is indicates the number of data entries in the receive FIFO.	0x0

Table 1349: UART3_SRR_REG (0x50020288)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	0x0
2	W	UART_XFR	XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is "self-clearing". It is not necessary to clear this bit.	0x0
1	W	UART_RFR	RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is "self-clearing". It is not necessary to clear this bit.	0x0
0	W	UART_UR	UART Reset. This asynchronously resets the UART Ctrl and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset.	0x0

Table 1350: UART3_SRTS_REG (0x5002028C)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R/W	UART_SHADOW_REQUEST_TO_SEND	Shadow Request to Send.	0x0

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Bit	Mode	Symbol	Description	Reset
			This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART Ctrl is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, (active MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input.	

Table 1351: UART3_SBCR_REG (0x50020290)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R/W	UART_SHADOW_BREAK_CONTROL	Shadow Break Control Bit. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared.	0x0

Table 1352: UART3_SDMAM_REG (0x50020294)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R/W	UART_SHADOW_DMA_MODE	Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals. 0 = mode 0 1 = mode 1	0x0

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Table 1353: UART3_SFE_REG (0x50020298)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R/W	UART_SHADOW_FIFO_ENABLE	Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset.	0x0

Table 1354: UART3_SRT_REG (0x5002029C)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	0x0
1:0	R/W	UART_SHADOW_RCVR_TRIGGER	Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO ¼ full 10 = FIFO ½ full 11 = FIFO 2 less than full	0x0

Table 1355: UART3_STET_REG (0x500202A0)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	0x0
1:0	R/W	UART_SHADOW_TX_EMPTY_TRIGGER	Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 00 = FIFO empty	0x0

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Bit	Mode	Symbol	Description	Reset
			01 = 2 characters in the FIFO 10 = FIFO ¼ full 11 = FIFO ½ full	

Table 1356: UART3_HTX_REG (0x500202A4)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	R/W	UART_HALT_TX	This register is use to halt transmissions, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 = Halt TX disabled 1 = Halt TX enabled Note, if FIFOs are not enabled, the setting of the halt TX register has no effect on operation.	0x0

Table 1357: UART3_DMASA_REG (0x500202A8)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	0x0
0	W	UART_DMASA	This register is use to perform DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This will cause the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing' and it is not necessary to clear this bit.	0x0

Table 1358: UART3_DLF_REG (0x500202C0)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	0x0
3:0	R/W	UART_DLF	The fractional value is added to integer value set by DLH, DLL. Fractional value is equal UART_DLF/16	0x0

Table 1359: UART3_RAR_REG (0x500202C4)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	UART_RAR	This is an address matching register during receive mode. If the 9-th bit is set in the incoming character then the remaining 8-bits will be checked against this register value. If the match happens then sub-sequent characters with 9-th bit set to 0 will be treated as data byte until the next address byte is received.	0x0

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Bit	Mode	Symbol	Description	Reset
			Note: - This register is applicable only when ADDR_MATCH (LCR_EXT[1] and DLS_E (LCR_EXT[0]) bits are set to 1. RAR should be programmed only when UART is not busy.	

Table 1360: UART3_TAR_REG (0x500202C8)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	UART_TAR	This is an address matching register during transmit mode. If DLS_E (LCR_EXT[0]) bit is enabled, then uart will send the 9-bit character with 9-th bit set to 1 and remaining 8-bit address will be sent from this register provided SEND_ADDR (LCR_EXT[2]) bit is set to 1. Note: - This register is used only to send the address. The normal data should be sent by programming THR register. - Once the address is started to send on the DW_apb_uart serial lane, then SEND_ADDR bit will be auto-cleared by the hardware.	0x0

Table 1361: UART3_LCR_EXT (0x500202CC)

Bit	Mode	Symbol	Description	Reset
3	R/W	UART_TRANSMIT_MODE	Transmit mode control bit. This bit is used to control the type of transmit mode during 9-bit data transfers. 1 = In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding Register (STHR) are 9-bit wide. The user needs to ensure that the THR/STHR register is written correctly for address/data. Address: 9th bit is set to 1, Data : 9th bit is set to 0. Note: Transmit address register (TAR) is not applicable in this mode of operation. 0 = In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding register (STHR) are 8-bit wide. The user needs to program the address into Transmit Address Register (TAR) and data into the THR/STHR register. SEND_ADDR bit is used as a control knob to indicate the uart on when to send the address.	0x0
2	R/W	UART_SEND_ADDR	Send address control bit. This bit is used as a control knob for the user to determine when to send the address during transmit mode. 1 = 9-bit character will be transmitted with 9-th bit set to 1 and the remaining 8-bits will match to	0x0

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Bit	Mode	Symbol	Description	Reset
			what is being programmed in 'Transmit Address Register'. 0 = 9-bit character will be transmitted with 9-th bit set to 0 and the remaining 8-bits will be taken from the TXFIFO which is programmed through 8-bit wide THR/STHR register. Note: 1. This bit is auto-cleared by the hardware, after sending out the address character. User is not expected to program this bit to 0. 2. This field is applicable only when DLS_E bit is set to 1 and TRANSMIT_MODE is set to 0.	
1	R/W	UART_ADDR_MATCH	Address Match Mode.This bit is used to enable the address match feature during receive. 1 = Address match mode; uart will wait until the incoming character with 9-th bit set to 1. And further checks to see if the address matches with what is programmed in 'Receive Address Match Register'. If match is found, then sub-sequent characters will be treated as valid data and DW_apb_uart starts receiving data. 0 = Normal mode; DW_apb_uart will start to receive the data and 9-bit character will be formed and written into the receive RXFIFO. User is responsible to read the data and differentiate b/n address and data. Note: This field is applicable only when DLS_E is set to 1.	0x0
0	R/W	UART_DLS_E	Extension for DLS. This bit is used to enable 9-bit data for transmit and receive transfers.	0x0

Table 1362: UART3_CTRL_REG (0x500202E0)

Bit	Mode	Symbol	Description	Reset
31:12	-	-	Reserved	0x0
11	R/W	ISO7816_AUTO_GT	0 : UART sends when tx data is available 1 : UART sends new character after guard time	0x0
10	R/W	ISO7816_ERR_TX_VALUE_IRQMASK	0 : ERR_TX_VALUE IRQ is masked 1 : ERR_TX_VALUE IRQ is enabled	0x0
9	R/W	ISO7816_ERR_TX_TIME_IRQMASK	0 : ERR_TX_TIME IRQ is masked 1 : ERR_TX_TIME IRQ is enabled	0x0
8	R/W	ISO7816_TIM_EXPIRED_IRQMASK	0 : timer expired IRQ is masked 1 : timer expired IRQ is enabled	0x0
7	R	ISO7816_CLK_STATUS	0 : iso7816 clock is stopped 1 : iso7816 clock is running	0x0

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Bit	Mode	Symbol	Description	Reset
6	R/W	ISO7816_CLK_LEVEL	0 : iso7816 clock level low when stopped 1 : iso7816 clock level high when stopped	0x0
5	R/W	ISO7816_CLK_EN	0 : iso7816 clock disabled 1 : iso7816 clock enabled	0x0
4:0	R/W	ISO7816_CLK_DIV	ISO7816 clk freq = sclk/(2*(ISO7816_CLK_DIV+1)	0x0

Table 1363: UART3_TIMER_REG (0x500202E4)

Bit	Mode	Symbol	Description	Reset
31:18	-	-	Reserved	0x0
17	R/W	ISO7816_TIM_MODE	0 : Timer will count up to max value then stops. Timer has to be disabled and enabled again to restart. Timer is clocked with the ISO7816 clock 1 : Timer will count guard time. ISO7816_TIM_MAX has to be 16*GuardTime-1	0x0
16	R/W	ISO7816_TIM_EN	0 : Timer is disabled 1 : Timer is enabled	0x0
15:0	R/W	ISO7816_TIM_MAX	On write : timer will count from 0 to ISO7816_TIM_MAX On read : gives the current timer value	0x0

Table 1364: UART3_ERR_CTRL_REG (0x500202E8)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	0x0
8:4	R/W	ISO7816_ERR_PULSE_WIDTH	When Error Signal feature is enable and receive mode, it gives the width of the error signal in 1/16 etu	0x10
3:0	R/W	ISO7816_ERR_PULSE_OFFSET	When Error Signal feature is enable and receive mode, it gives the offset of the error signal in 1/16 etu from the 9.6 etu	0xE

Table 1365: UART3_IRQ_STATUS_REG (0x500202EC)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	0x0
2	R/W	ISO7816_ERR_TX_VALUE_IRQ	On read 1 : : If error signal is enabled and in transmit mode, module generates IRQ when receiver does not receive correctly the character	0x0

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Bit	Mode	Symbol	Description	Reset
			On Write 1 : Clear IRQ	
1	R/W	ISO7816_ERR_TX_TIME_IRQ	On read 1 : If error signal is enabled and in transmit mode, module generates IRQ when it checks the error signal On Write 1 : Clear IRQ	0x0
0	R	ISO7816_TIM_EXPIRED_IRQ	On read 1 : when Timer is expired. Timer has to be disabled to clear the IRQ. When sclk is lower than pclk then this bit has to be checked if it's cleared before return form the IRQ Handler	0x0

Table 1366: UART3_UCV_REG (0x500202F8)

Bit	Mode	Symbol	Description	Reset
31:0	R	UART_UCV	Component Version	0x3430312A

Table 1367: UART3_CTR_REG (0x500202FC)

Bit	Mode	Symbol	Description	Reset
31:0	R	UART_CTR	Component Type Register	0x44570110

44.31 USB Controller Registers

Table 1368: Register map USB

Address	Register	Description
0x51000000	USB_MCTRL_REG	Main Control Register)
0x51000004	USB_XCVDIAG_REG	Transceiver diagnostic Register (for test purpose only)
0x51000008	USB_TCR_REG	Transceiver configuration Register
0x5100000C	USB_UTR_REG	USB test Register (for test purpose only)
0x51000010	USB_FAR_REG	Function Address Register
0x51000014	USB_NFSR_REG	Node Functional State Register
0x51000018	USB_MAEV_REG	Main Event Register
0x5100001C	USB_MAMSK_REG	Main Mask Register
0x51000020	USB_ALTEV_REG	Alternate Event Register
0x51000024	USB_ALTMSK_REG	Alternate Mask Register

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Address	Register	Description
0x51000028	USB_TXEV_REG	Transmit Event Register
0x5100002C	USB_TXMSK_REG	Transmit Mask Register
0x51000030	USB_RXEV_REG	Receive Event Register
0x51000034	USB_RXMSK_REG	Receive Mask Register
0x51000038	USB_NAKEV_REG	NAK Event Register
0x5100003C	USB_NAKMSK_REG	NAK Mask Register
0x51000040	USB_FWEV_REG	FIFO Warning Event Register
0x51000044	USB_FWMSK_REG	FIFO Warning Mask Register
0x51000048	USB_FNH_REG	Frame Number High Byte Register
0x5100004C	USB_FNL_REG	Frame Number Low Byte Register
0x5100007C	USB_UX20CDR_REG	Transceiver 2.0 Configuration and Diagnostics Register(for test purpose only)
0x51000080	USB_EPC0_REG	Endpoint Control 0 Register
0x51000084	USB_TXD0_REG	Transmit Data 0 Register
0x51000088	USB_TXS0_REG	Transmit Status 0 Register
0x5100008C	USB_TXC0_REG	Transmit command 0 Register
0x51000090	USB_EP0_NAK_REG	EP0 INNAK and OUTNAK Register
0x51000094	USB_RXD0_REG	Receive Data 0 Register
0x51000098	USB_RXS0_REG	Receive Status 0 Register
0x5100009C	USB_RXC0_REG	Receive Command 0 Register
0x510000A0	USB_EPC1_REG	Endpoint Control Register 1
0x510000A4	USB_TXD1_REG	Transmit Data Register 1
0x510000A8	USB_TXS1_REG	Transmit Status Register 1
0x510000AC	USB_TXC1_REG	Transmit Command Register 1
0x510000B0	USB_EPC2_REG	Endpoint Control Register 2
0x510000B4	USB_RXD1_REG	Receive Data Register,1
0x510000B8	USB_RXS1_REG	Receive Status Register 1
0x510000BC	USB_RXC1_REG	Receive Command Register 1
0x510000C0	USB_EPC3_REG	Endpoint Control Register 3
0x510000C4	USB_TXD2_REG	Transmit Data Register 2
0x510000C8	USB_TXS2_REG	Transmit Status Register 2
0x510000CC	USB_TXC2_REG	Transmit Command Register 2
0x510000D0	USB_EPC4_REG	Endpoint Control Register 4
0x510000D4	USB_RXD2_REG	Receive Data Register 2
0x510000D8	USB_RXS2_REG	Receive Status Register 2
0x510000DC	USB_RXC2_REG	Receive Command Register 2
0x510000E0	USB_EPC5_REG	Endpoint Control Register 5
0x510000E4	USB_TXD3_REG	Transmit Data Register 3
0x510000E8	USB_TXS3_REG	Transmit Status Register 3

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Address	Register	Description
0x510000EC	USB_TXC3_REG	Transmit Command Register 3
0x510000F0	USB_EPC6_REG	Endpoint Control Register 6
0x510000F4	USB_RXD3_REG	Receive Data Register 3
0x510000F8	USB_RXS3_REG	Receive Status Register 3
0x510000FC	USB_RXC3_REG	Receive Command Register 3
0x510001A0	USB_DMA_CTRL_REG	USB DMA control register
0x510001AC	USB_CHARGER_STAT_REG	USB Charger Status Register

Table 1369: USB_MCTRL_REG (0x51000000)

Bit	Mode	Symbol	Description	Reset
31:15	-	-	Reserved	0x0
4	R/W	LSMODE	Low Speed Mode This bit enables USB 1.5 Mb/s low speed and swaps D+ and D- pull-up resistors. Changing speed may only be done if USBEN is set to 0. Also D+ and D- rise and fall times are adjusted according to the USB specification.	0x0
3	R/W	USB_NAT	Node Attached This bit indicates that this node is ready to be detected as attached to USB. When cleared to 0 the transceiver forces SE0 on the USB port to prevent the hub (to which this node is connected to) from detecting an attach event. After reset or when the USB node is disabled, this bit is cleared to 0 to give the device time before it must respond to commands. After this bit has been set to 1, the device no longer drives the USB and should be ready to receive Reset signalling from the hub. Note: This bit can only be set is USBEN is 1	0x0
2	-	-	Reserved	0x0
1	R/W	USB_DBG	Debug Mode. When this bit is set, the following registers are writable: Main Event (MAEV), Alternate Event (ALTEV), NAK Event (NAKEV), Transmit Status and Receive Status. Setting the DBG bit forces the node into a locked state. The node states can be read out of the transceiver diagnostic register (XCVDIAG) at location 0xFF6802 by setting the DIAG bit in the Test Control register (UTR). Note: The operation of CoR bits is not effected by entering Debug mode) Note: This bit can only be set is USBEN is 1	0x0
0	R/W	USBEN	USB EnableSetting this bit to 1 enables the Full/Low Speed USB node. If the USBEN bit is cleared to 0, the USB is disabled and the 48 MHz clock within the USB node is stopped. In addition, all USB registers are set to their reset state.	0x0

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Bit	Mode	Symbol	Description	Reset
			Note that the transceiver forces SE0 on the bus to prevent the hub to detected the USB node, when it is disabled (not attached). The USBEN bit is cleared to 0 after reset	

Table 1370: USB_XCVDIAG_REG (0x51000004)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R	USB_VPIN	With Bit0 = 1 this bit shows the level of the USB_Dp receive data from transceiver; D+ <= VSE.	0x0
6	R	USB_VMIN	With Bit0 = 1 this bit shows the level USB_Dm receive data from transceiver; D- <= VSE.	0x0
5	R	USB_RCV	With Bit0 = 1 this bit shows the differential level of the receive comparator.	0x0
4	-	-	Reserved	0x0
3	R/W	USB_XCV_TXEN	With Bit0 = 1, this bit enables test Bits 2,1. Must be kept to 0 for normal operation	0x0
2	R/W	USB_XCV_TXn	With Bit3,0 = 1, this bit sets USB_Dm to a high level, independent of LSMODE selection	0x0
1	R/W	USB_XCV_TXp	With Bit3,0 = 1, this bit sets USB_Dp to a high level, independent of LSMODE selection	0x0
0	R/W	USB_XCV_TEST	Enable USB_XCVDIAG_REG 0: Normal operation, test bits disabled 1: Enable test bits 7,6,5,3,2,1	0x0

Table 1371: USB_TCR_REG (0x51000008)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:5	R/W	USB_VADJ	Reference Voltage/ Threshold voltage AdjustControls the single-ended receiver threshold. Shall not be modified unless instructed by Renesas Electronics Only enabled if USB_UTR_REG[7] = 1	0x4
4:0	R/W	USB_CADJ	Transmitter Current Adjust Controls the driver edge rate control current. Shall not be modified unless instructed by Renesas Electronics Only enabled if USB_UTR_REG[7] = 1	0x10

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Table 1372: USB_UTR_REG (0x5100000C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	USB_DIAG	Diagnostic enable 0: Normal operational. 1: Access to the USB_XCVDIAG_REG and USB_TCR_REG enabled. For diagnostic purposes only	0x0
6	R/W	USB_NCRC	No CRC16 When this bit is set to 1, all packets transmitted by the Full/Low Speed USB node are sent without a trailing CRC16. Receive operations are unaffected. This mode is used to check that CRC errors can be detected by other nodes. For diagnostic purposes only	0x0
5	R/W	USB_SF	Short Frame Enables the Frame timer to lock and track, short, non-compliant USB frame sizes. The Short Frame bit should not be set during normal operation. For test purposes only	0x0
4:0	R/W	USB_UTR_RES	Reserved. Must be kept to 0	0x0

Table 1373: USB_FAR_REG (0x51000010)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	USB_AD_EN	Address Enable When set to 1, USB address field bits 6-0 are used in address comparison When cleared to 0, the device does not respond to any token on the USB bus. Note: If the DEF bit in the Endpoint Control 0 register is set, Endpoint 0 responds to the default address.	0x0
6:0	R/W	USB_AD	Address This field holds the 7-bit function address used to transmit and receive all tokens addressed to this device.	0x0

Table 1374: USB_NFSR_REG (0x51000014)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	0x0
1:0	R/W	USB_NFS	The Node Functional State Register reports and controls the current functional state of the USB node. 00: NodeReset. This is the USB Reset state. This is entered upon a module reset or by software upon detection of a USB Reset. Upon entry, all endpoint pipes are	0x0

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Bit	Mode	Symbol	Description	Reset
			disabled. DEF in the Endpoint Control 0 (EPC0) register and AD_EN in the Function Address (FAR) register should be cleared by software on entry to this state. On exit, DEF should be reset so the device responds to the default address. 01: NodeResume In this state, resume signalling is generated. This state should be entered by firmware to initiate a remote wake-up sequence by the device. The node must remain in this state for at least 1 ms and no more than 15 ms. 10: NodeOperational This is the normal operational state. In this state the node is configured for operation on the USB bus. 11: NodeSuspend Suspend state should be entered by firmware on detection of a Suspend event while in Operational state. While in Suspend state, the transceivers operate in their low-power suspend mode. All endpoint controllers and the bits TX_EN, LAST and RX_EN are reset, while all other internal states are frozen. On detection of bus activity, the RESUME bit in the ALTEV register is set. In response, software can cause entry to NodeOperational state.	

Table 1375: USB_MAEV_REG (0x51000018)

Bit	Mode	Symbol	Description	Reset
31:12	-	-	Reserved	0x0
11	R/W	USB_CH_EV	USB Charger event This bit is set if one of the bits in USB_CHARGER_STAT_REG[2-0] change. This bit is cleared to 0 when if USB_CHARGER_STAT_REG is read.	0x0
10	R/W	USB_EP0_NAK	Endpoint 0 NAK Event This bit is an OR of EP0_NAK_REG[EP0_OUTNAK] and EP0_NAK_REG[EP0_INNAK] bits. USB_EP0_NAK is cleared to 0 when EP0_NAK_REG is read.	0x0
9	R/W	USB_EP0_RX	Endpoint 0 Receive Event This bit is a copy of the RXS0[RX_LAST] and is cleared to 0 when this RXS0 register is read. Note: Since Endpoint 0 implements a store and forward principle, an overrun condition for FIFO0 cannot occur	0x0
8	R/W	USB_EP0_TX	Endpoint 0 Transmit Event This bit is a copy of the TXS0[TX_DONE] bit and is cleared to 0 when the TXS0 register is read. Note: Since Endpoint 0 implements a store and forward principle, an underrun condition for FIFO0 cannot occur.	0x0

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Bit	Mode	Symbol	Description	Reset
7	R/W	USB_INTR	Master Interrupt Enable This bit is hardwired to 0 in the Main Event (MAEV) register; bit 7 in the Main Mask (MAMSK) register is the Master Interrupt Enable.	0x0
6	R/W	USB_RX_EV	Receive Event This bit is set to 1 if any of the unmasked bits in the Receive Event (RXEV) register is set to 1. It indicates that a SETUP or OUT transaction has been completed. This bit is cleared to 0 when all of the RX_LAST bits in each Receive Status (RXSn) register and all RXOVRRN bits in the RXEV register are cleared to 0.	0x0
5	R/W	USB_ULD	Unlocked/Locked Detected This bit is set to 1, when the frame timer has either entered unlocked condition from a locked condition, or has re-entered a locked condition from an unlocked condition as determined by the UL bit in the Frame Number (FNH or FNL) register. This bit is cleared to 0 when the register is read.	0x0
4	R/W	USB_NAK	Negative Acknowledge Event This bit indicates that one of the unmasked NAK Event (NAKEV) register bits has been set to 1. This bit is cleared to 0 when the NAKEV register is read.	0x0
3	R/W	USB_FRAME	Frame Event This bit is set to 1, if the frame counter is updated with a new value. This can be due to the receipt of a valid SOF packet on the USB or to an artificial update if the frame counter was unlocked or a frame was missed. This bit is cleared to 0 when the register is read.	0x0
2	R/W	USB_TX_EV	Transmit Event This bit is set to 1, if any of the unmasked bits in the Transmit Event (TXEV) register (TXFIFOn or TXUNDRNn) is set to 1. Therefore, it indicates that an IN transaction has been completed. This bit is cleared to 0 when all the TX_DONE bits and the TXUNDRN bits in each Transmit Status (TXSn) register are cleared to 0.	0x0
1	R/W	USB_ALT	Alternate Event This bit indicates that one of the unmasked ALTEV register bits has been set to 1. This bit is cleared to 0 by reading the ALTEV register.	0x0
0	R/W	USB_WARN	Warning Event This bit indicates that one of the unmasked bits in the FIFO Warning Event (FWEV) register has been set to 1. This bit is cleared to 0 by reading the FWEV register.	0x0

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Table 1376: USB_MAMSK_REG (0x5100001C)

Bit	Mode	Symbol	Description	Reset
31:12	-	-	Reserved	0x0
11	R/W	USB_M_CH_EV	The Main Mask Register masks out events reported in the MAEV registers. A bit set to 1, enables the interrupts for the respective event in the MAEV register. If the corresponding bit is cleared to 0, interrupt generation for this event is disabled. Same Bit Definition as MAEV Register	0x0
10	R/W	USB_M_EP0_NAK	Same Bit Definition as MAEV Register	0x0
9	R/W	USB_M_EP0_RX	Same Bit Definition as MAEV Register	0x0
8	R/W	USB_M_EP0_TX	Same Bit Definition as MAEV Register	0x0
7	R/W	USB_M_INTR	Same Bit Definition as MAEV Register	0x0
6	R/W	USB_M_RX_EV	Same Bit Definition as MAEV Register	0x0
5	R/W	USB_M_ULD	Same Bit Definition as MAEV Register	0x0
4	R/W	USB_M_NAK	Same Bit Definition as MAEV Register	0x0
3	R/W	USB_M_FRAME	Same Bit Definition as MAEV Register	0x0
2	R/W	USB_M_TX_EV	Same Bit Definition as MAEV Register	0x0
1	R/W	USB_M_ALT	Same Bit Definition as MAEV Register	0x0
0	R/W	USB_M_WARN	Same Bit Definition as MAEV Register	0x0

Table 1377: USB_ALTEV_REG (0x51000020)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	USB_RESUME	Resume Resume signalling is detected on the USB when the device is in Suspend state (NFS in the NFSR register is set to SUSPEND), and a non IDLE signal is present on the USB, indicating that this device should begin it's wake-up sequence and enter Operational state. This bit is cleared when the register is read.	0x0
6	R/W	USB_RESET	Reset This bit is set to 1, when 2.5 µs of SEO have been detected on the upstream port. In response, the functional state should be reset (NFS in the NFSR register is set to RESET), where it must remain for at least 100 µs. The functional state can then return to Operational state. This bit is cleared when the register is read	0x0
5	R/W	USB_SD5	Suspend Detect 5 ms This bit is set to 1 after 5 ms of IDLE have been detected on the upstream port, indicating that this device is permitted to perform a remote wake-up operation. The resume may be initiated under firmware control by writing the resume value to the NFSR register. This bit is cleared when the register is read.	0x0

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Bit	Mode	Symbol	Description	Reset
4	R/W	USB_SD3	Suspend Detect 3 ms This bit is set to 1 after 3 ms of IDLE have been detected on the upstream port, indicating that the device should be suspended. The suspend occurs under firmware control by writing the suspend value to the Node Functional State (NFSR) register. This bit is cleared when the register is read.	0x0
3	R/W	USB_EOP	End of Packet A valid EOP sequence was been detected on the USB. It is used when this device has initiated a Remote wake-up sequence to indicate that the Resume sequence has been acknowledged and completed by the host. This bit is cleared when the register is read.	0x0
2	-	-	Reserved	0x0
1:0	-	-	Reserved	0x0

Table 1378: USB_ALTMSK_REG (0x51000024)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	USB_M_RESUME	A bit set to 1 in this register enables automatic setting of the ALT bit in the MAEV register when the respective event in the ALTEV register occurs. Otherwise, setting MAEV.ALT bit is disabled. Same Bit Definition as ALTEV Register	0x0
6	R/W	USB_M_RESET	Same Bit Definition as ALTEV Register	0x0
5	R/W	USB_M_SD5	Same Bit Definition as ALTEV Register	0x0
4	R/W	USB_M_SD3	Same Bit Definition as ALTEV Register	0x0
3	R/W	USB_M_EOP	Same Bit Definition as ALTEV Register	0x0
2	-	-	Reserved	0x0
1:0	-	-	Reserved	0x0

Table 1379: USB_TXEV_REG (0x51000028)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6:4	R	USB_TXUDRRN31	Transmit Underrun n: 3:1 The bit n is a copy of the respective TX_URUN bit from the corresponding Transmit Status register (TXSn). Whenever any of the Transmit FIFOs underflows, the respective TXUDRRN bit is set to 1. These bits are cleared to 0 when the corresponding Transmit Status register is read	0x0
3	-	-	Reserved	0x0
2:0	R	USB_TXFIFO31	Transmit FIFO n: 3:1	0x0

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Bit	Mode	Symbol	Description	Reset
			The bit n is a copy of the TX_DONE bit from the corresponding Transmit Status register (TXSn). A bit is set to 1 when the IN transaction for the corresponding transmit endpoint n has been completed. These bits are cleared to 0 when the corresponding TXSn register is read.	

Table 1380: USB_TXMSK_REG (0x5100002C)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6:4	R/W	USB_M_TXUDRRN31	The Transmit Mask Register is used to select the bits of the TXEV registers, which causes the TX_EV bit in the MAEV register to be set to 1. When a bit is set to 1 and the corresponding bit in the TXEV register is set to 1, the TX_EV bit in the MAEV register is set to1. When cleared to 0, the corresponding bit in the TXEV register does not cause TX_EV to be set to 1. Same Bit Definition as TXEV Register	0x0
3	-	-	Reserved	0x0
2:0	R/W	USB_M_TXFIFO31	Same Bit Definition as TXEV Register	0x0

Table 1381: USB_RXEV_REG (0x51000030)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6:4	R	USB_RXOVRRN31	Receive Overrun n: 3:1 The bit n is set to 1 in the event of an overrun condition in the corresponding receive FIFO n. They are cleared to 0 when the register is read. The firmware must check the respective RX_ERR bits that packets received for the other receive endpoints (EP2, EP4 and EP6,) are not corrupted by errors, as these endpoints support data streaming (packets which are longer than the actual FIFO depth).	0x0
3	-	-	Reserved	0x0
2:0	R	USB_RXFIFO31	Receive FIFO n: 3:1 The bit n is set to 1 whenever either RX_ERR or RX_LAST in the respective Receive Status register (RXSn) is set to 1. Reading the corresponding RXSn register automatically clears these bits.The CoR function is disabled, when the Freeze signal is asserted.The USB node discards all packets for Endpoint 0 received with errors. This is necessary in case of retransmission due to media errors, ensuring that a good copy of a SETUP packet is captured. Otherwise, the FIFO may potentially be tied up, holding corrupted data and unable to receive a retransmission of the same packet.	0x0

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Bit	Mode	Symbol	Description	Reset
			If data streaming is used for the receive endpoints (EP2, EP4 and EP6, EP8) the firmware must check the respective RX_ERR bits to ensure the packets received are not corrupted by errors.	

Table 1382: USB_RXMSK_REG (0x51000034)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6:4	R/W	USB_M_RXOVRRN31	The Receive Mask Register is used to select the bits of the RXEV registers, which causes the RX_EV bit in the MAEV register to be set to 1. When set to 1 and the corresponding bit in the RXEV register is set to 1, RX_EV bit in the MAEV register is set to1. When cleared to 0, the corresponding bit in the RXEV register does not cause RX_EV to be set to1. Same Bit Definition as RXEV Register	0x0
3	-	-	Reserved	0x0
2:0	R/W	USB_M_RXFIFO31	Same Bit Definition as RXEV Register	0x0

Table 1383: USB_NAKEV_REG (0x51000038)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6:4	R	USB_OUT31	OUT n: 3:1 The bit n is set to 1 when a NAK handshake is generated for an enabled address/endpoint combination (AD_EN in the FAR register is set to 1 and EP_EN in the EPCx register is set to 1) in response to an OUT token. This bit is not set if NAK is generated as result of an overrun condition. It is cleared when the register is read.	0x0
3	-	-	Reserved	0x0
2:0	R	USB_IN31	IN n: 3:1 The bit n is set to 1 when a NAK handshake is generated for an enabled address/endpoint combination (AD_EN in the Function Address, FAR, register is set to 1 and EP_EN in the Endpoint Control, EPCx, register is set to 1) in response to an IN token. This bit is cleared when the register is read.	0x0

Table 1384: USB_NAKMSK_REG (0x5100003C)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6:4	R/W	USB_M_OUT31	When set and the corresponding bit in the NAKEV register is set, the NAK bit in the MAEV register is	0x0

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Bit	Mode	Symbol	Description	Reset
			set. When cleared, the corresponding bit in the NAKEV register does not cause NAK to be set. Same Bit Definition as NAKEV Register	
3	-	-	Reserved	0x0
2:0	R/W	USB_M_IN31	Same Bit Definition as NAKEV Register	0x0

Table 1385: USB_FWEV_REG (0x51000040)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6:4	R	USB_RXWARN31	Receive Warning n: 3:1 The bit n is set to 1 when the respective receive endpoint FIFO reaches the warning limit, as specified by the RFWL bits of the respective EPCx register. This bit is cleared when the warning condition is cleared by either reading data from the FIFO or when the FIFO is flushed.	0x0
3	-	-	Reserved	0x0
2:0	R	USB_TXWARN31	Transmit Warning n: 3:1 The bit n is set to 1 when the respective transmit endpoint FIFO reaches the warning limit, as specified by the TFWL bits of the respective TXCn register, and transmission from the respective endpoint is enabled. This bit is cleared when the warning condition is cleared by either writing new data to the FIFO when the FIFO is flushed, or when transmission is done, as indicated by the TX_DONE bit in the TXSn register.	0x0

Table 1386: USB_FWMSK_REG (0x51000044)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6:4	R/W	USB_M_RXWARN31	The FIFO Warning Mask Register selects, which FWEV bits are reported in the MAEV register. A bit set to 1 and the corresponding bit in the FWEV register is set 1, causes the WARN bit in the MAEV register to be set to 1. When cleared to 0, the corresponding bit in the FWEV register does not cause WARN to be set to 1. Same Bit Definition as FWEV Register	0x0
3	-	-	Reserved	0x0
2:0	R/W	USB_M_TXWARN31	The FIFO Warning Mask Register selects, which FWEV bits are reported in the MAEV register. A bit set to 1 and the corresponding bit in the FWEV register is set 1, causes the WARN bit in the MAEV register to be set to 1. When cleared to 0, the corresponding bit in the FWEV register does not cause WARN to be set to 1. Same Bit Definition as FWEV Register	0x0

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Table 1387: USB_FNH_REG (0x51000048)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R	USB_MF	Missed SOF Flag This flag is set to 1, when the frame number in a valid received SOF does not match the expected next value, or when an SOF is not received within 12060 bit times. This bit is set by the hardware and is cleared by reading the FNH register.	0x1
6	R	USB_UL	Unlock Flag This bit indicates that at least two frames were received without an expected frame number, or that no valid SOF was received within 12060 bit times. If this bit is set, the frame number from the next valid SOF packet is loaded in FN. This bit is set by the hardware and is cleared by reading the FNH register.	0x1
5	R	USB_RFC	Reset Frame Count Writing a 1 to this bit resets the frame number to 00016, after which this bit clears itself to 0 again. This bit always reads 0.	0x0
4:3	-	-	Reserved	0x0
2:0	R	USB_FN_10_8	Frame Number This 3-bit field contains the three most significant bits (MSB) of the current frame number, received in the last SOF packet. If a valid frame number is not received within 12060 bit times (Frame Length Maximum, FLMAX, with tolerance) of the previous change, the frame number is incremented artificially. If two successive frames are missed or are incorrect, the current FN is frozen and loaded with the next frame number from a valid SOF packet. If the frame number low byte was read by firmware before reading the FNH register, the user actually reads the contents of a buffer register which holds the value of the three frame number bits of this register when the low byte was read. Therefore, the correct sequence to read the frame number is: FNL, FNH. Read operations to the FNH register, without first reading the Frame Number Low Byte (FNL) register directly, read the actual value of the three MSBs of the frame number.	0x0

Table 1388: USB_FNL_REG (0x5100004C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R	USB_FN	The Frame Number Low Byte Register holds the low byte of the frame number. To ensure consistency, reading this low byte causes the three frame number bits in the FNH register to be	0x0

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Bit	Mode	Symbol	Description	Reset
			locked until this register is read. The correct sequence to read the frame number is: FNL, FNH.	

Table 1389: USB_UX20CDR_REG (0x5100007C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R	RPU_TEST7	Test bit	0x0
6	R/W	RPU_TEST_SW2	0: Closes SW2 switch to reduced pull-up resistor connected to the USB_Dp and USB_Dm. 1: Opens SW2 switch resistor connected to the USB_Dp and USB_Dm (independent of the VBus state).	0x0
5	R/W	RPU_TEST_SW1	0: Enable the pull-up resistor on USB_Dp (SW1 closed) 1: Disable the pull-up resistor on USB_Dp (SW1 open) (Independent of the VBus state).	0x0
4	R/W	RPU_TEST_EN	Pull-Up Resistor Test Enable 0: Normal operation 1: Enables the test features controlled by RPU_TEST_SW1, RPU_TEST_SW1DM and RPU_TEST_SW2	0x0
3	-	-	Reserved	0x0
2	R/W	RPU_TEST_SW1DM	0: Enable the pull-up resistor on USB_Dm (SW1DM closed) 1: Disable the pull-up resistor on USB_Dm (SW1DM open) (Independent of the VBus state).	0x0
1	R/W	RPU_RCDELAY	Test bit, must be kept 0	0x0
0	R/W	RPU_SSPROTEN	Test bit, must be kept 0	0x0

Table 1390: USB_EPC0_REG (0x51000080)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	USB_STALL	Stall Setting this bit to 1 causes the chip to generate STALL handshakes under the following conditions: - The transmit FIFO is enabled and an IN token is received. - The receive FIFO is enabled and an OUT token is received. Note: A SETUP token does not cause a STALL handshake to be generated when this bit is set. Upon transmitting the STALL handshake, the RX_LAST and the TX_DONE bits in the respective Receive/Transmit Status registers are set to 1.	0x0

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Bit	Mode	Symbol	Description	Reset
6	R/W	USB_DEF	Default Address When set to 1, the device responds to the default address regardless of the contents of FAR6-0/EP03-0 fields. When an IN packet is transmitted for the endpoint, the DEF bit is automatically cleared to 0. This bit aids in the transition from default address to assigned address. The transition from the default address 00000000000b to an address assigned during bus enumeration may not occur in the middle of the SET_ADDRESS control sequence. This is necessary to complete the control sequence. However, the address must change immediately after this sequence finishes in order to avoid errors when another control sequence immediately follows the SET_ADDRESS command. On USB reset, the firmware has 10 ms for set-up, and should write 8016 to the FAR register and 0016 to the EPC0 register. On receipt of a SET_ADDRESS command, the firmware must write 4016 to the EPC0 register and (8016 or <assigned_function_address>) to the FAR register. It must then queue a zero length IN packet to complete the status phase of the SET_ADDRESS control sequence.	0x0
5:4	-	-	Reserved	0x0
3:0	R	USB_EP	Endpoint Address This field holds the 4-bit Endpoint address. For Endpoint 0, these bits are hardwired to 0000b. Writing a 1 to any of the EP bits is ignored.	0x0

Table 1391: USB_TXD0_REG (0x51000084)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	W	USB_TXFD	Transmit FIFO Data Byte The firmware is expected to write only the packet payload data. The PID and CRC16 are created automatically.	0x0

Table 1392: USB_TXS0_REG (0x51000088)

Bit	Mode	Symbol	Description	Reset
12	R	USB_ACK_STAT	Acknowledge Status This bit indicates the status, as received from the host, of the ACK for the packet previously sent. This bit is to be interpreted when TX_DONE is set to 1. It is set to 1, when an ACK is received; otherwise, it remains cleared. This bit is also cleared to 0, when this register is read.	0x0
11	R	USB_TX_DONE	Transmission Done	0x0

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Bit	Mode	Symbol	Description	Reset
			When set to 1, this bit indicates that a packet has completed transmission. It is cleared to 0, when this register is read.	
10:0	R	USB_TCOUNT	Transmission Count This field indicates the number of empty bytes available in the FIFO.	0x40

Table 1393: USB_TXC0_REG (0x5100008C)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	0x0
4	R/W	USB_IGN_IN	Ignore IN Tokens When this bit is set to 1, the endpoint will ignore any IN tokens directed to its configured address.	0x0
3	R/W	USB_FLUSH	Flush FIFO Writing a 1 to this bit flushes all data from the control endpoint FIFOs, resets the endpoint to Idle state, clears the FIFO read and write pointer, and then clears itself. If the endpoint is currently using the FIFO0 to transfer data on USB, flushing is delayed until after the transfer is done. It is equivalent to the FLUSH bit in the RXC0 register.	0x0
2	R/W	USB_TOGGLE_TX0	Toggle This bit specifies the PID used when transmitting the packet. A value of 0 causes a DATA0 PID to be generated, while a value of 1 causes a DATA1 PID to be generated. This bit is not altered by the hardware.	0x0
1	-	-	Reserved	0x0
0	R/W	USB_TX_EN	Transmission Enable This bit enables data transmission from the FIFO. It is cleared to 0 by hardware after transmitting a single packet, or a STALL handshake, in response to an IN token. It must be set to 1 by firmware to start packet transmission. The RX_EN bit in the Receive Command 0 (RXC0) register takes precedence over this bit; i.e. if RX_EN is set, TX_EN bit is ignored until RX_EN is reset. Zero length packets are indicated by setting this bit without writing any data to the FIFO.	0x0

Table 1394: USB_EP0_NAK_REG (0x51000090)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	0x0
1	R	USB_EP0_OUTNAK	End point 0 OUT NAK This bit n is set to 1 when a NAK handshake is generated for an enabled address/endpoint combination (AD_EN in the FAR register is set to 1) in response to an OUT token. This bit is not set	0x0

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Bit	Mode	Symbol	Description	Reset
			if NAK is generated as result of an overrun condition. It is cleared when the register is read.	
0	R	USB_EP0_INNAK	End point 0 IN NAK This bit is set to 1 when a NAK handshake is generated for an enabled address/endpoint combination (AD_EN in the FAR register is set to 1) in response to an IN token. This bit is cleared when the register is read.	0x0

Table 1395: USB_RXD0_REG (0x51000094)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R	USB_RXFD	Receive FIFO Data Byte The firmware should expect to read only the packet payload data. The PID and CRC16 are removed from the incoming data stream automatically. In TEST mode this register allow read/write access.	0x0

Table 1396: USB_RXS0_REG (0x51000098)

Bit	Mode	Symbol	Description	Reset
13	R	USB_SETUP	Setup This bit indicates that the setup packet has been received. This bit is unchanged for zero length packets. It is cleared to 0 when this register is read.	0x0
12	R	USB_TOGGLE_RX0	Toggle This bit specified the PID used when receiving the packet. A value of 0 indicates that the last successfully received packet had a DATA0 PID, while a value of 1 indicates that this packet had a DATA1 PID. This bit is unchanged for zero length packets. It is cleared to 0 when this register is read.	0x0
11	R	USB_RX_LAST	Receive Last Bytes This bit indicates that an ACK was sent upon completion of a successful receive operation. This bit is unchanged for zero length packets. It is cleared to 0 when this register is read.	0x0
10:0	R	USB_RCOUNT	Receive Count This field contains the number of bytes presently in the RX FIFO.	0x0

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Table 1397: USB_RXC0_REG (0x5100009C)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	0x0
5	-	-	Reserved	0x0
4	-	-	Reserved	0x0
3	R/W	USB_FLUSH	Flush Writing a 1 to this bit flushes all data from the control endpoint FIFOs, resets the endpoint to Idle state, clears the FIFO read and write pointer, and then clears itself. If the endpoint is currently using FIFO0 to transfer data on USB, flushing is delayed until after the transfer is done. This bit is cleared to 0 on reset. This bit is equivalent to FLUSH in the TXC0 register.	0x0
2	R/W	USB_IGN_SETUP	Ignore SETUP Tokens When this bit is set to 1, the endpoint ignores any SETUP tokens directed to its configured address.	0x0
1	R/W	USB_IGN_OUT	Ignore OUT Tokens When this bit is set to 1, the endpoint ignores any OUT tokens directed to its configured address.	0x0
0	R/W	USB_RX_EN	Receive Enable OUT packet reception is disabled after every data packet is received, or when a STALL handshake is returned in response to an OUT token. A 1 must be written to this bit to re-enable data reception. Reception of SETUP packets is always enabled. In the case of back-to-back SETUP packets (for a given endpoint) where a valid SETUP packet is received with no other intervening non-SETUP tokens, the Endpoint Controller discards the new SETUP packet and returns an ACK handshake. If any other reasons prevent the Endpoint Controller from accepting the SETUP packet, it must not generate a handshake. This allows recovery from a condition where the ACK of the first SETUP token was lost by the host.	0x0

Table 1398: USB_EPC1_REG (0x510000A0)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	USB_STALL	Stall Setting this bit to 1 causes the chip to generate STALL handshakes under the following conditions: The transmit FIFO is enabled and an IN token is received. The receive FIFO is enabled and an OUT token is received. Setting this bit to 1 does not generate a STALL handshake in response to a SETUP token	0x0
6	-	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
5	R/W	USB_ISO	Isochronous When this bit is set to 1, the endpoint is isochronous. This implies that no NAK is sent if the endpoint is not ready but enabled; i.e. If an IN token is received and no data is available in the FIFO to transmit, or if an OUT token is received and the FIFO is full since there is no USB handshake for isochronous transfers.	0x0
4	R/W	USB_EP_EN	Endpoint Enable When this bit is set to 1, the EP[3:0] field is used in address comparison, together with the AD[6:0] field in the FAR register. When cleared to 0, the endpoint does not respond to any token on the USB bus.	0x0
3:0	R/W	USB_EP	Endpoint Address This 4-bit field holds the endpoint address.	0x0

Table 1399: USB_TXD1_REG (0x510000A4)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	W	USB_TXFD	Transmit FIFO Data Byte The firmware is expected to write only the packet payload data. PID and CRC16 are inserted automatically in the transmit data stream. In TEST mode this register allow read/write access via the core bus.	0x0

Table 1400: USB_TXS1_REG (0x510000A8)

Bit	Mode	Symbol	Description	Reset
13	R	USB_TX_URUN	Transmit FIFO Underrun This bit is set to 1, if the transmit FIFO becomes empty during a transmission, and no new data is written to the FIFO. If so, the Media Access Controller (MAC) forces a bit stuff error followed by an EOP. This bit is cleared to 0, when this register is read.	0x0
12	R	USB_ACK_STAT	Acknowledge Status This bit is interpreted when TX_DONE is set. It's function differs depending on whether ISO (ISO in the EPCx register is set) or non-ISO operation (ISO is reset) is used. For non-ISO operation, this bit indicates the acknowledge status (from the host) about the ACK for the previously sent packet. This bit itself is set to 1, when an ACK is received; otherwise, it is cleared to 0. For ISO operation, this bit is set if a frame number LSB match (see IGN_ISOMSK bit in the USB_TXCx_REG) occurs, and data was sent in response to an IN token. Otherwise, this bit is	0x0

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Bit	Mode	Symbol	Description	Reset
			cleared to 0, the FIFO is flushed and TX_DONE is set. This bit is also cleared to 0, when this register is read.	
11	R	USB_TX_DONE	Transmission Done When set to 1, this bit indicates that the endpoint responded to a USB packet. Three conditions can cause this bit to be set: A data packet completed transmission in response to an IN token with non-ISO operation. The endpoint sent a STALL handshake in response to an IN token A scheduled ISO frame was transmitted or discarded. This bit is cleared to 0 when this register is read.	0x0
10:0	R	USB_TCOUNT	Transmission Count This field indicates the number of empty bytes available in the FIFO.	0x200

Table 1401: USB_TXC1_REG (0x510000AC)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	USB_IGN_ISOMSK	Ignore ISO Mask This bit has an effect only if the endpoint is set to be isochronous. If set to 1, this bit disables locking of specific frame numbers with the alternate function of the TOGGLE bit. Thus data is transmitted upon reception of the next IN token. If cleared to 0, data is only transmitted when FNL0 matches TOGGLE. This bit is cleared to 0 after reset.	0x0
6:5	R/W	USB_TFWL	Transmit FIFO Warning Limit These bits specify how many more bytes can be transmitted from the respective FIFO before an underrun condition occurs. If the number of bytes remaining in the FIFO is equal to or less than the selected warning limit, the TXWARN bit in the FWEV register is set. To avoid interrupts caused by setting this bit while the FIFO is being filled before a transmission begins, TXWARN is only set when transmission from the endpoint is enabled (TX_ENn in the TXCn register is set). TFWL[1:0] : 00: TFWL disabled 01: Less than 5 bytes remaining in FIFO 10: Less than 9 bytes remaining in FIFO 11: Less than 17 bytes remaining in FIFO	0x0
4	R/W	USB_RFF	Refill FIFO Setting the LAST bit to 1 automatically saves the Transmit Read Pointer (TXRP) to a buffer. When the RFF bit is set to 1, the buffered TXRP is reloaded into the TXRP. This allows the user to	0x0

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Bit	Mode	Symbol	Description	Reset
			repeat the last transaction if no ACK was received from the host. If the MAC is currently using the FIFO to transmit, TXRP is reloaded only after the transmission is complete. After reload, this bit is cleared to 0 by hardware.	
3	R/W	USB_FLUSH	Flush FIFO Writing a 1 to this bit flushes all data from the corresponding transmit FIFO, resets the endpoint to Idle state, and clears both the FIFO read and write pointers. If the MAC is currently using the FIFO to transmit, data is flushed after the transmission is complete. After data flushing, this bit is cleared to 0 by hardware.	0x0
2	R/W	USB_TOGGLE_TX	Toggle The function of this bit differs depending on whether ISO (ISO bit in the EPCn register is set to 1) or non-ISO operation (ISO bit is cleared to 0) is used. For non-ISO operation, it specifies the PID used when transmitting the packet. A value of 0 causes a DATA0 PID to be generated, while a value of 1 causes a DATA1 PID to be generated. For ISO operation, this bit and the LSB of the frame counter (FNL0) act as a mask for the TX_EN bit to allow pre-queuing of packets to specific frame numbers; I.e. transmission is enabled only if bit 0 in the FNL register is set to TOGGLE. If an IN token is not received while this condition is true, the contents of the FIFO are flushed with the next SOF. If the endpoint is set to ISO, data is always transferred with a DATA0 PID.	0x0
1	R/W	USB_LAST	Last Byte Setting this bit to 1 indicates that the entire packet has been written into the FIFO. This is used especially for streaming data to the FIFO while the actual transmission occurs. If the LAST bit is not set to 1 and the transmit FIFO becomes empty during a transmission, a stuff error followed by an EOP is forced on the bus. Zero length packets are indicated by setting this bit without writing any data to the FIFO. The transmit state machine transmits the payload data, CRC16 and the EOP signal before clearing this bit.	0x0
0	R/W	USB_TX_EN	Transmission Enable This bit enables data transmission from the FIFO. It is cleared to 0 by hardware after transmitting a single packet or after a STALL handshake in response to an IN token. It must be set to 1 by firmware to start packet transmission.	0x0

Table 1402: USB_EPC2_REG (0x510000B0)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
7	R/W	USB_STALL	Stall Setting this bit to 1 causes the chip to generate STALL handshakes under the following conditions: The transmit FIFO is enabled and an IN token is received. The receive FIFO is enabled and an OUT token is received. Setting this bit to 1 does not generate a STALL handshake in response to a SETUP token	0x0
6	-	-	Reserved	0x0
5	R/W	USB_ISO	Isochronous When this bit is set to 1, the endpoint is isochronous. This implies that no NAK is sent if the endpoint is not ready but enabled; i.e. If an IN token is received and no data is available in the FIFO to transmit, or if an OUT token is received and the FIFO is full since there is no USB handshake for isochronous transfers.	0x0
4	R/W	USB_EP_EN	Endpoint Enable When this bit is set to 1, the EP[3:0] field is used in address comparison, together with the AD[6:0] field in the FAR register. When cleared to 0, the endpoint does not respond to any token on the USB bus.	0x0
3:0	R/W	USB_EP	Endpoint Address This 4-bit field holds the endpoint address.	0x0

Table 1403: USB_RXD1_REG (0x510000B4)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R	USB_RXFD	Receive FIFO Data Byte The firmware should expect to read only the packet payload data. The PID and CRC16 are terminated by the receive state machine. In TEST mode this register allow read/write access via the core bus.	0x0

Table 1404: USB_RXS1_REG (0x510000B8)

Bit	Mode	Symbol	Description	Reset
15	R	USB_RXFULL	Indicates that the RX fifo is full	0x0
14	R	USB_RX_ERR	Receive Error When set to 1, this bit indicates a media error, such as bit-stuffing or CRC. If this bit is set to 1, the firmware must flush the respective FIFO.	0x0
13	R	USB_SETUP	Setup	0x0

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Bit	Mode	Symbol	Description	Reset
			This bit indicates that the setup packet has been received. It is cleared when this register is read.	
12	R	USB_TOGGLE_RX	Toggle The function of this bit differs depending on whether ISO (ISO in the EPCn register is set) or non-ISO operation (ISO is reset) is used. For non-ISO operation, a value of 0 indicates that the last successfully received packet had a DATA0 PID, while a value of 1 indicates that this packet had a DATA1 PID. For ISO operation, this bit reflects the LSB of the frame number (FNL0) after a packet was successfully received for this endpoint. This bit is reset to 0 by reading the RXSn register.	0x0
11	R	USB_RX_LAST	Receive Last This bit indicates that an ACK was sent upon completion of a successful receive operation. This bit is cleared to 0 when this register is read.	0x0
10:0	R	USB_RCOUNT	Receive Count This field contains the number of bytes presently in the RX FIFO.	0x0

Table 1405: USB_RXC1_REG (0x510000BC)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6:5	R/W	USB_RFWL	Receive FIFO Warning Limit These bits specify how many more bytes can be received to the respective FIFO before an overrun condition occurs. If the number of empty bytes remaining in the FIFO is equal to or less than the selected warning limit, the RXWARN bit in the FWEV register is set to 1.RFWL[1:0] : 00: RFWL disabled 01: Less than 5 bytes remaining in FIFO 10: Less than 9 bytes remaining in FIFO 11: Less than 17 bytes remaining in FIFO	0x0
4	-	-	Reserved	0x0
3	R/W	USB_FLUSH	Flush FIFO Writing a 1 to this bit flushes all data from the corresponding receive FIFO, resets the endpoint to Idle state, and resets both the FIFO read and write pointers. If the MAC is currently using the FIFO to receive data, flushing is delayed until after receiving is completed.	0x0
2	R/W	USB_IGN_SETUP	Ignore SETUP Tokens When this bit is set to 1, the endpoint ignores any SETUP tokens directed to its configured address.	0x0
1	-	-	Reserved	0x0
0	R/W	USB_RX_EN	Receive Enable	0x0

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Bit	Mode	Symbol	Description	Reset
			OUT packet cannot be received after every data packet is received, or when a STALL handshake is returned in response to an OUT token. This bit must be written with a 1 to re-enable data reception. SETUP packets can always be received. In the case of back-to-back SETUP packets (for a given endpoint) where a valid SETUP packet has been received with no other intervening non-SETUP tokens, the receive state machine discards the new SETUP packet and returns an ACK handshake. If, for any other reason, the receive state machine cannot accept the SETUP packet, no HANDSHAKE should be generated.	

Table 1406: USB_EPC3_REG (0x510000C0)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	USB_STALL	Stall Setting this bit to 1 causes the chip to generate STALL handshakes under the following conditions: The transmit FIFO is enabled and an IN token is received. The receive FIFO is enabled and an OUT token is received. Setting this bit to 1 does not generate a STALL handshake in response to a SETUP token	0x0
6	-	-	Reserved	0x0
5	R/W	USB_ISO	Isochronous When this bit is set to 1, the endpoint is isochronous. This implies that no NAK is sent if the endpoint is not ready but enabled; i.e. If an IN token is received and no data is available in the FIFO to transmit, or if an OUT token is received and the FIFO is full since there is no USB handshake for isochronous transfers.	0x0
4	R/W	USB_EP_EN	Endpoint Enable When this bit is set to 1, the EP[3:0] field is used in address comparison, together with the AD[6:0] field in the FAR register. When cleared to 0, the endpoint does not respond to any token on the USB bus.	0x0
3:0	R/W	USB_EP	Endpoint Address This 4-bit field holds the endpoint address.	0x0

Table 1407: USB_TXD2_REG (0x510000C4)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
7:0	W	USB_TXFD	Transmit FIFO Data Byte The firmware is expected to write only the packet payload data. PID and CRC16 are inserted automatically in the transmit data stream. In TEST mode this register allow read/write access via the core bus.	0x0

Table 1408: USB_TXS2_REG (0x510000C8)

Bit	Mode	Symbol	Description	Reset
13	R	USB_TX_URUN	Transmit FIFO Underrun This bit is set to 1, if the transmit FIFO becomes empty during a transmission, and no new data is written to the FIFO. If so, the Media Access Controller (MAC) forces a bit stuff error followed by an EOP. This bit is cleared to 0, when this register is read.	0x0
12	R	USB_ACK_STAT	Acknowledge Status This bit is interpreted when TX_DONE is set. It's function differs depending on whether ISO (ISO in the EPCx register is set) or non-ISO operation (ISO is reset) is used. For non-ISO operation, this bit indicates the acknowledge status (from the host) about the ACK for the previously sent packet. This bit itself is set to 1, when an ACK is received; otherwise, it is cleared to 0. For ISO operation, this bit is set if a frame number LSB match (see IGN_ISOMSK bit in the USB_TXCx_REG) occurs, and data was sent in response to an IN token. Otherwise, this bit is cleared to 0, the FIFO is flushed and TX_DONE is set. This bit is also cleared to 0, when this register is read.	0x0
11	R	USB_TX_DONE	Transmission Done When set to 1, this bit indicates that the endpoint responded to a USB packet. Three conditions can cause this bit to be set: A data packet completed transmission in response to an IN token with non-ISO operation. The endpoint sent a STALL handshake in response to an IN token A scheduled ISO frame was transmitted or discarded. This bit is cleared to 0 when this register is read.	0x0
10:0	R	USB_TCOUNT	Transmission Count This field indicates the number of empty bytes available in the FIFO.	0x200

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Table 1409: USB_TXC2_REG (0x510000CC)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	USB_IGN_ISOMSK	Ignore ISO Mask This bit has an effect only if the endpoint is set to be isochronous. If set to 1, this bit disables locking of specific frame numbers with the alternate function of the TOGGLE bit. Thus data is transmitted upon reception of the next IN token. If cleared to 0, data is only transmitted when FNL0 matches TOGGLE. This bit is cleared to 0 after reset.	0x0
6:5	R/W	USB_TFWL	Transmit FIFO Warning Limit These bits specify how many more bytes can be transmitted from the respective FIFO before an underrun condition occurs. If the number of bytes remaining in the FIFO is equal to or less than the selected warning limit, the TXWARN bit in the FWEV register is set. To avoid interrupts caused by setting this bit while the FIFO is being filled before a transmission begins, TXWARN is only set when transmission from the endpoint is enabled (TX_ENn in the TXCn register is set). TFWL[1:0] : 00: TFWL disabled 01: Less than 5 bytes remaining in FIFO 10: Less than 9 bytes remaining in FIFO 11: Less than 17 bytes remaining in FIFO	0x0
4	R/W	USB_RFF	Refill FIFO Setting the LAST bit to 1 automatically saves the Transmit Read Pointer (TXRP) to a buffer. When the RFF bit is set to 1, the buffered TXRP is reloaded into the TXRP. This allows the user to repeat the last transaction if no ACK was received from the host. If the MAC is currently using the FIFO to transmit, TXRP is reloaded only after the transmission is complete. After reload, this bit is cleared to 0 by hardware.	0x0
3	R/W	USB_FLUSH	Flush FIFO Writing a 1 to this bit flushes all data from the corresponding transmit FIFO, resets the endpoint to Idle state, and clears both the FIFO read and write pointers. If the MAC is currently using the FIFO to transmit, data is flushed after the transmission is complete. After data flushing, this bit is cleared to 0 by hardware.	0x0
2	R/W	USB_TOGGLE_TX	Toggle The function of this bit differs depending on whether ISO (ISO bit in the EPCn register is set to 1) or non-ISO operation (ISO bit is cleared to 0) is used. For non-ISO operation, it specifies the PID used when transmitting the packet. A value of 0 causes a DATA0 PID to be generated, while a value of 1 causes a DATA1 PID to be generated. For ISO operation, this bit and the LSB of the frame counter (FNL0) act as a mask for the	0x0

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Bit	Mode	Symbol	Description	Reset
			TX_EN bit to allow pre-queuing of packets to specific frame numbers; I.e. transmission is enabled only if bit 0 in the FNL register is set to TOGGLE. If an IN token is not received while this condition is true, the contents of the FIFO are flushed with the next SOF. If the endpoint is set to ISO, data is always transferred with a DATA0 PID.	
1	R/W	USB_LAST	Last Byte Setting this bit to 1 indicates that the entire packet has been written into the FIFO. This is used especially for streaming data to the FIFO while the actual transmission occurs. If the LAST bit is not set to 1 and the transmit FIFO becomes empty during a transmission, a stuff error followed by an EOP is forced on the bus. Zero length packets are indicated by setting this bit without writing any data to the FIFO. The transmit state machine transmits the payload data, CRC16 and the EOP signal before clearing this bit.	0x0
0	R/W	USB_TX_EN	Transmission Enable This bit enables data transmission from the FIFO. It is cleared to 0 by hardware after transmitting a single packet or after a STALL handshake in response to an IN token. It must be set to 1 by firmware to start packet transmission.	0x0

Table 1410: USB_EPC4_REG (0x510000D0)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	USB_STALL	Stall Setting this bit to 1 causes the chip to generate STALL handshakes under the following conditions: The transmit FIFO is enabled and an IN token is received. The receive FIFO is enabled and an OUT token is received. Setting this bit to 1 does not generate a STALL handshake in response to a SETUP token	0x0
6	-	-	Reserved	0x0
5	R/W	USB_ISO	Isochronous When this bit is set to 1, the endpoint is isochronous. This implies that no NAK is sent if the endpoint is not ready but enabled; i.e. If an IN token is received and no data is available in the FIFO to transmit, or if an OUT token is received and the FIFO is full since there is no USB handshake for isochronous transfers.	0x0
4	R/W	USB_EP_EN	Endpoint Enable When this bit is set to 1, the EP[3:0] field is used in address comparison, together with the AD[6:0] field in the FAR register. When cleared to 0, the	0x0

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Bit	Mode	Symbol	Description	Reset
			endpoint does not respond to any token on the USB bus.	
3:0	R/W	USB_EP	Endpoint Address This 4-bit field holds the endpoint address.	0x0

Table 1411: USB_RXD2_REG (0x510000D4)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R	USB_RXFD	Receive FIFO Data Byte The firmware should expect to read only the packet payload data. The PID and CRC16 are terminated by the receive state machine. In TEST mode this register allow read/write access via the core bus.	0x0

Table 1412: USB_RXS2_REG (0x510000D8)

Bit	Mode	Symbol	Description	Reset
15	R	USB_RXFULL	Indicates that the RX fifo is full	0x0
14	R	USB_RX_ERR	Receive Error When set to 1, this bit indicates a media error, such as bit-stuffing or CRC. If this bit is set to 1, the firmware must flush the respective FIFO.	0x0
13	R	USB_SETUP	Setup This bit indicates that the setup packet has been received. It is cleared when this register is read.	0x0
12	R	USB_TOGGLE_RX	Toggle The function of this bit differs depending on whether ISO (ISO in the EPCn register is set) or non-ISO operation (ISO is reset) is used. For non-ISO operation, a value of 0 indicates that the last successfully received packet had a DATA0 PID, while a value of 1 indicates that this packet had a DATA1 PID. For ISO operation, this bit reflects the LSB of the frame number (FNL0) after a packet was successfully received for this endpoint. This bit is reset to 0 by reading the RXSn register.	0x0
11	R	USB_RX_LAST	Receive Last This bit indicates that an ACK was sent upon completion of a successful receive operation. This bit is cleared to 0 when this register is read.	0x0
10:0	R	USB_RCOUNT	Receive Count This field contains the number of bytes presently in the RX FIFO.	0x0

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Table 1413: USB_RXC2_REG (0x510000DC)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6:5	R/W	USB_RFWL	Receive FIFO Warning Limit These bits specify how many more bytes can be received to the respective FIFO before an overrun condition occurs. If the number of empty bytes remaining in the FIFO is equal to or less than the selected warning limit, the RXWARN bit in the FWEV register is set to 1.RFWL[1:0] : 00: RFWL disabled 01: Less than 5 bytes remaining in FIFO 10: Less than 9 bytes remaining in FIFO 11: Less than 17 bytes remaining in FIFO	0x0
4	-	-	Reserved	0x0
3	R/W	USB_FLUSH	Flush FIFO Writing a 1 to this bit flushes all data from the corresponding receive FIFO, resets the endpoint to Idle state, and resets both the FIFO read and write pointers. If the MAC is currently using the FIFO to receive data, flushing is delayed until after receiving is completed.	0x0
2	R/W	USB_IGN_SETUP	Ignore SETUP Tokens When this bit is set to 1, the endpoint ignores any SETUP tokens directed to its configured address.	0x0
1	-	-	Reserved	0x0
0	R/W	USB_RX_EN	Receive Enable OUT packet cannot be received after every data packet is received, or when a STALL handshake is returned in response to an OUT token. This bit must be written with a 1 to re-enable data reception. SETUP packets can always be received. In the case of back-to-back SETUP packets (for a given endpoint) where a valid SETUP packet has been received with no other intervening non-SETUP tokens, the receive state machine discards the new SETUP packet and returns an ACK handshake. If, for any other reason, the receive state machine cannot accept the SETUP packet, no HANDSHAKE should be generated.	0x0

Table 1414: USB_EPC5_REG (0x510000E0)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	USB_STALL	Stall Setting this bit to 1 causes the chip to generate STALL handshakes under the following conditions: The transmit FIFO is enabled and an IN token is received.	0x0

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Bit	Mode	Symbol	Description	Reset
			The receive FIFO is enabled and an OUT token is received. Setting this bit to 1 does not generate a STALL handshake in response to a SETUP token	
6	-	-	Reserved	0x0
5	R/W	USB_ISO	Isochronous When this bit is set to 1, the endpoint is isochronous. This implies that no NAK is sent if the endpoint is not ready but enabled; i.e. If an IN token is received and no data is available in the FIFO to transmit, or if an OUT token is received and the FIFO is full since there is no USB handshake for isochronous transfers.	0x0
4	R/W	USB_EP_EN	Endpoint Enable When this bit is set to 1, the EP[3:0] field is used in address comparison, together with the AD[6:0] field in the FAR register. When cleared to 0, the endpoint does not respond to any token on the USB bus.	0x0
3:0	R/W	USB_EP	Endpoint Address This 4-bit field holds the endpoint address.	0x0

Table 1415: USB_TXD3_REG (0x510000E4)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	W	USB_TXFD	Transmit FIFO Data Byte The firmware is expected to write only the packet payload data. PID and CRC16 are inserted automatically in the transmit data stream. In TEST mode this register allow read/write access via the core bus.	0x0

Table 1416: USB_TXS3_REG (0x510000E8)

Bit	Mode	Symbol	Description	Reset
13	R	USB_TX_URUN	Transmit FIFO Underrun This bit is set to 1, if the transmit FIFO becomes empty during a transmission, and no new data is written to the FIFO. If so, the Media Access Controller (MAC) forces a bit stuff error followed by an EOP. This bit is cleared to 0, when this register is read.	0x0
12	R	USB_ACK_STAT	Acknowledge Status This bit is interpreted when TX_DONE is set. It's function differs depending on whether ISO (ISO in the EPCx register is set) or non-ISO operation (ISO is reset) is used. For non-ISO operation, this bit indicates the acknowledge status (from the host) about the ACK for the previously sent packet. This bit itself is set	0x0

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Bit	Mode	Symbol	Description	Reset
			to 1, when an ACK is received; otherwise, it is cleared to 0. For ISO operation, this bit is set if a frame number LSB match (see IGN_ISOMSK bit in the USB_TXCx_REG) occurs, and data was sent in response to an IN token. Otherwise, this bit is cleared to 0, the FIFO is flushed and TX_DONE is set. This bit is also cleared to 0, when this register is read.	
11	R	USB_TX_DONE	Transmission Done When set to 1, this bit indicates that the endpoint responded to a USB packet. Three conditions can cause this bit to be set: A data packet completed transmission in response to an IN token with non-ISO operation. The endpoint sent a STALL handshake in response to an IN token A scheduled ISO frame was transmitted or discarded. This bit is cleared to 0 when this register is read.	0x0
10:0	R	USB_TCOUNT	Transmission Count This field indicates the number of empty bytes available in the FIFO.	0x200

Table 1417: USB_TXC3_REG (0x510000EC)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	USB_IGN_ISOMSK	Ignore ISO Mask This bit has an effect only if the endpoint is set to be isochronous. If set to 1, this bit disables locking of specific frame numbers with the alternate function of the TOGGLE bit. Thus data is transmitted upon reception of the next IN token. If cleared to 0, data is only transmitted when FNL0 matches TOGGLE. This bit is cleared to 0 after reset.	0x0
6:5	R/W	USB_TFWL	Transmit FIFO Warning Limit These bits specify how many more bytes can be transmitted from the respective FIFO before an underrun condition occurs. If the number of bytes remaining in the FIFO is equal to or less than the selected warning limit, the TXWARN bit in the FWEV register is set. To avoid interrupts caused by setting this bit while the FIFO is being filled before a transmission begins, TXWARN is only set when transmission from the endpoint is enabled (TX_ENn in the TXCn register is set). TFWL[1:0] : 00: TFWL disabled 01: Less than 5 bytes remaining in FIFO 10: Less than 9 bytes remaining in FIFO	0x0

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Bit	Mode	Symbol	Description	Reset
			11: Less than 17 bytes remaining in FIFO	
4	R/W	USB_RFF	Refill FIFO Setting the LAST bit to 1 automatically saves the Transmit Read Pointer (TXRP) to a buffer. When the RFF bit is set to 1, the buffered TXRP is reloaded into the TXRP. This allows the user to repeat the last transaction if no ACK was received from the host. If the MAC is currently using the FIFO to transmit, TXRP is reloaded only after the transmission is complete. After reload, this bit is cleared to 0 by hardware.	0x0
3	R/W	USB_FLUSH	Flush FIFO Writing a 1 to this bit flushes all data from the corresponding transmit FIFO, resets the endpoint to Idle state, and clears both the FIFO read and write pointers. If the MAC is currently using the FIFO to transmit, data is flushed after the transmission is complete. After data flushing, this bit is cleared to 0 by hardware.	0x0
2	R/W	USB_TOGGLE_TX	Toggle The function of this bit differs depending on whether ISO (ISO bit in the EPCn register is set to 1) or non-ISO operation (ISO bit is cleared to 0) is used. For non-ISO operation, it specifies the PID used when transmitting the packet. A value of 0 causes a DATA0 PID to be generated, while a value of 1 causes a DATA1 PID to be generated. For ISO operation, this bit and the LSB of the frame counter (FNL0) act as a mask for the TX_EN bit to allow pre-queuing of packets to specific frame numbers; I.e. transmission is enabled only if bit 0 in the FNL register is set to TOGGLE. If an IN token is not received while this condition is true, the contents of the FIFO are flushed with the next SOF. If the endpoint is set to ISO, data is always transferred with a DATA0 PID.	0x0
1	R/W	USB_LAST	Last Byte Setting this bit to 1 indicates that the entire packet has been written into the FIFO. This is used especially for streaming data to the FIFO while the actual transmission occurs. If the LAST bit is not set to 1 and the transmit FIFO becomes empty during a transmission, a stuff error followed by an EOP is forced on the bus. Zero length packets are indicated by setting this bit without writing any data to the FIFO. The transmit state machine transmits the payload data, CRC16 and the EOP signal before clearing this bit.	0x0
0	R/W	USB_TX_EN	Transmission Enable This bit enables data transmission from the FIFO. It is cleared to 0 by hardware after transmitting a single packet or after a STALL handshake in response to an IN token. It must be set to 1 by firmware to start packet transmission.	0x0

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Table 1418: USB_EPC6_REG (0x510000F0)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7	R/W	USB_STALL	Stall Setting this bit to 1 causes the chip to generate STALL handshakes under the following conditions: The transmit FIFO is enabled and an IN token is received. The receive FIFO is enabled and an OUT token is received. Setting this bit to 1 does not generate a STALL handshake in response to a SETUP token	0x0
6	-	-	Reserved	0x0
5	R/W	USB_ISO	Isochronous When this bit is set to 1, the endpoint is isochronous. This implies that no NAK is sent if the endpoint is not ready but enabled; i.e. If an IN token is received and no data is available in the FIFO to transmit, or if an OUT token is received and the FIFO is full since there is no USB handshake for isochronous transfers.	0x0
4	R/W	USB_EP_EN	Endpoint Enable When this bit is set to 1, the EP[3:0] field is used in address comparison, together with the AD[6:0] field in the FAR register. When cleared to 0, the endpoint does not respond to any token on the USB bus.	0x0
3:0	R/W	USB_EP	Endpoint Address This 4-bit field holds the endpoint address.	0x0

Table 1419: USB_RXD3_REG (0x510000F4)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	0x0
7:0	R	USB_RXFD	Receive FIFO Data Byte The firmware should expect to read only the packet payload data. The PID and CRC16 are terminated by the receive state machine. In TEST mode this register allow read/write access via the core bus.	0x0

Table 1420: USB_RXS3_REG (0x510000F8)

Bit	Mode	Symbol	Description	Reset
15	R	USB_RXFULL	Indicates that the RX fifo is full	0x0
14	R	USB_RX_ERR	Receive Error When set to 1, this bit indicates a media error, such as bit-stuffing or CRC. If this bit is set to 1, the firmware must flush the respective FIFO.	0x0

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Bit	Mode	Symbol	Description	Reset
13	R	USB_SETUP	Setup This bit indicates that the setup packet has been received. It is cleared when this register is read.	0x0
12	R	USB_TOGGLE_RX	Toggle The function of this bit differs depending on whether ISO (ISO in the EPCn register is set) or non-ISO operation (ISO is reset) is used. For non-ISO operation, a value of 0 indicates that the last successfully received packet had a DATA0 PID, while a value of 1 indicates that this packet had a DATA1 PID. For ISO operation, this bit reflects the LSB of the frame number (FNL0) after a packet was successfully received for this endpoint. This bit is reset to 0 by reading the RXSn register.	0x0
11	R	USB_RX_LAST	Receive Last This bit indicates that an ACK was sent upon completion of a successful receive operation. This bit is cleared to 0 when this register is read.	0x0
10:0	R	USB_RCOUNT	Receive Count This field contains the number of bytes presently in the RX FIFO.	0x0

Table 1421: USB_RXC3_REG (0x510000FC)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6:5	R/W	USB_RFWL	Receive FIFO Warning Limit These bits specify how many more bytes can be received to the respective FIFO before an overrun condition occurs. If the number of empty bytes remaining in the FIFO is equal to or less than the selected warning limit, the RXWARN bit in the FWEV register is set to 1.RFWL[1:0] : 00: RFWL disabled 01: Less than 5 bytes remaining in FIFO 10: Less than 9 bytes remaining in FIFO 11: Less than 17 bytes remaining in FIFO	0x0
4	-	-	Reserved	0x0
3	R/W	USB_FLUSH	Flush FIFO Writing a 1 to this bit flushes all data from the corresponding receive FIFO, resets the endpoint to Idle state, and resets both the FIFO read and write pointers. If the MAC is currently using the FIFO to receive data, flushing is delayed until after receiving is completed.	0x0
2	R/W	USB_IGN_SETUP	Ignore SETUP Tokens When this bit is set to 1, the endpoint ignores any SETUP tokens directed to its configured address.	0x0
1	-	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
0	R/W	USB_RX_EN	Receive Enable OUT packet cannot be received after every data packet is received, or when a STALL handshake is returned in response to an OUT token. This bit must be written with a 1 to re-enable data reception. SETUP packets can always be received. In the case of back-to-back SETUP packets (for a given endpoint) where a valid SETUP packet has been received with no other intervening non-SETUP tokens, the receive state machine discards the new SETUP packet and returns an ACK handshake. If, for any other reason, the receive state machine cannot accept the SETUP packet, no HANDSHAKE should be generated.	0x0

Table 1422: USB_DMA_CTRL_REG (0x510001A0)

Bit	Mode	Symbol	Description	Reset
31:7	-	-	Reserved	0x0
6	R/W	USB_DMA_EN	0 = USB DMA control off. (Normal operation) 1 = USB_DMA on. DMA channels 0 and 1 are connected by USB Endpoint according bits USB_DMA_TX and USB_DMA_RX	0x0
5:3	R/W	USB_DMA_TX	000 = DMA channels 1 is connected Tx USB Endpoint 1 001 = DMA channels 1 is connected Tx USB Endpoint 3 010 = DMA channels 1 is connected Tx USB Endpoint 5 100, 1xx = Reserved	0x0
2:0	R/W	USB_DMA_RX	000 = DMA channels 0 is connected Rx USB Endpoint 2 001 = DMA channels 0 is connected Rx USB Endpoint 4 010 = DMA channels 0 is connected Rx USB Endpoint 6 100, 1xx = Reserved	0x0

Table 1423: USB_CHARGER_STAT_REG (0x510001AC)

Bit	Mode	Symbol	Description	Reset
31:6	R	-	Reserved	0x0
5	R	USB_DM_VAL2	0: USBm < 2.3 V 1: USBm > 2.5 V	0x0
4	R	USB_DP_VAL2	0: USBp < 2.3 V 1: USBp > 2.5 V	0x0
3	R	USB_DM_VAL	0: USBm < 0.8 V	0x0

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Bit	Mode	Symbol	Description	Reset
			1: USBm > 1.5 V (PS2 or Proprietary Charger)	
2	R	USB_DP_VAL	0: USBp < 0.8 V 1: USBp > 1.5 V	0x0
1	R	USB_CHG_DET	0: Standard downstream or nothing connected. 1: Charging Downstream Port (CDP) or Dedicated Charging.	0x0
0	R	USB_DCP_DET	0: Charging downstream port is detected. 1: Dedicated charger is detected. Control bit VDM_SRC_ON must be set to validate this status bit. Note: This register shows the actual status.	0x0

44.32 Voice Activation Detection Controller Registers

Table 1424: Register map VAD

Address	Register	Description
0x50000C00	VAD_CTRL0_REG	VAD Control Register 0
0x50000C04	VAD_CTRL1_REG	VAD Control Register 1
0x50000C08	VAD_CTRL2_REG	VAD Control Register 2
0x50000C0C	VAD_CTRL3_REG	VAD Control Register 3
0x50000C10	VAD_CTRL4_REG	VAD Control Register 4
0x50000C20	VAD_STATUS_REG	VAD Status Register

Table 1425: VAD_CTRL0_REG (0x50000C00)

Bit	Mode	Symbol	Description	Reset
7:6	R/W	VAD_VTRACK	Voice Tracking parameter: This parameter allows to set the adaptation speed of the system depending on the voice input. When the setting of this parameter is low, the high-frequency sensitivity of the VAD increases, some phonem can be detected easily but high-frequency ambient noise can be considered as voice. When the setting of this parameter is high, the high-frequency sensitivity of the VAD decreases, high-frequency ambient noise is filtered but some phonem can be lost. 00: fast 01: default . . . 11: slow	0x1
5:3	R/W	VAD_NTRACK	Background Noise Tracking parameter: This parameter allows to set the speed of the system adaptation to the ambient noise. This parameter gives the flexibility to adapt the VAD to the application environment.	0x4

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Bit	Mode	Symbol	Description	Reset
			000: fast . . . 100: default . . . 111: slow	
2:0	R/W	VAD_PWR_LVL_SNSTVTY	Power Level Sensitivity: Ratio between ambient noise and voice level to be detected. When the setting of this parameter is low, the VAD sensitivity increases, leading to higher VDV and possibly higher NDV. When the setting of this parameter is high, the VAD sensitivity decreases, leading to lower NDV and possibly lower VDV. 000: 2 dB 001: 3 dB 010: 4 dB 011: 5 dB 100: 6 dB (default) 101: 8 dB 110: 10 dB 111: 16 dB	0x4

Table 1426: VAD_CTRL1_REG (0x50000C04)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	0x0
4:3	R/W	VAD_MINDELAY	Minimum Delay: This parameter allows to set the minimum time before a detection when switching to Always listenning mode. This delay is defined as a number of clock cycle, divided from MCLK depending on MCLK_DIV setting. 00: 768 clock cycles (default) 01: 1536 clock cycles 10: 3584 clock cycles 11: 9632 clock cycles	0x0
2:0	R/W	VAD_MINEVENT	Minimum Event Duration: This parameter allows to set the Minimum vocal signal duration that can be detected by the system. When the setting of this parameter is low, the detection latency decreases but the high-frequency ambient noise can be considered as voice. When the setting of this parameter is high, the high-frequency ambient noise is filtered but the detection latency increase. This delay is defined as a number of clock cycle, divided from MCLK depending on MCLK_DIV setting. 000: 1 Mclk cycle 001: 16 Mclk cycles 010: 32 Mclk cycles (default) 011: 64 Mclk cycles	0x2

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Bit	Mode	Symbol	Description	Reset
			100: 128 Mclk cycles 101: 256 Mclk cycles 110: 512 Mclk cycles 111: 1024 Mclk cycles	

Table 1427: VAD_CTRL2_REG (0x50000C08)

Bit	Mode	Symbol	Description	Reset
7:6	R/W	-	Reserved	0x0
5:0	R/W	VAD_NFI_DET	NFI Detection: This parameter defines the NFI threshold above which an IRQ is sent	0x27

Table 1428: VAD_CTRL3_REG (0x50000C0C)

Bit	Mode	Symbol	Description	Reset
7	R/W	VAD_SB	Stand-by mode 0: The VAD block is activated (sleep or listening mode) 1: The VAD block is deactivated (stand-by mode)	0x1
6	R/W	VAD_SLEEP	Sleep mode 0: If SB = 0, The VAD block is in listening mode 1: If SB = 0, The VAD block is in sleep mode Note: It is recommended to set VAD_SLEEP to 1 (sleep mode), during the recording of AIP/AIN audio inputs on ADC path.	0x1
5:3	R/W	VAD_MCLK_DIV	Clock selection - refer to table 3.3* 000: Division ration = 1 001: Division ration = 2 010: Division ration = 4 011: Division ration = 8 100: Division ration = 16 101: Division ration = 24 110: Division ration = 48	0x0
2:0	R/W	-	Reserved	0x0

Table 1429: VAD_CTRL4_REG (0x50000C10)

Bit	Mode	Symbol	Description	Reset
7:3	-	-	Reserved	0x0
2	R/W	VAD_IRQ_MODE	IRQ mode selection 0: The generated IRQ is a high level 1: The generated IRQ is a pulse, which duration is 8 internal clock cycles	0x0
1	R0/WC	VAD_IRQ_FLAG	Interrupt ReQuest flag: IRQ_FLAG is set to 1	0x0

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Bit	Mode	Symbol	Description	Reset
			when a voice detection event occurs. Writing 1 resets the flag and the IRQ to 0. Note: Due to way the VAD is implemented, the delay for the IRQ clearance mechanism is depending on the input voice signal. In order to force the IRQ to '0' for cases of false trigger, the SLEEP mode of the VAD should be used (VAD_CTRL3_REG[SLEEP]).	
0	-	-	Reserved	0x0

Table 1430: VAD_STATUS_REG (0x50000C20)

Bit	Mode	Symbol	Description	Reset
5:0	R	VAD_NFI_RD	VAD NFI output read-out value.	0x28

44.33 Silicon Version Registers

Table 1431: Register map Version

Address	Register	Description
0x50040000	CHIP_ID1_REG	Chip identification register 1.
0x50040004	CHIP_ID2_REG	Chip identification register 2.
0x50040008	CHIP_ID3_REG	Chip identification register 3.
0x5004000C	CHIP_ID4_REG	Chip identification register 4.
0x50040010	CHIP_SWC_REG	Software compatibility register.
0x50040014	CHIP_REVISION_REG	Chip revision register.
0x500400F8	CHIP_TEST1_REG	Chip test register 1.
0x500400FC	CHIP_TEST2_REG	Chip test register 2.

Table 1432: CHIP_ID1_REG (0x50040000)

Bit	Mode	Symbol	Description	Reset
7:0	R	CHIP_ID1	First character of device type in ASCII.	0x33

Table 1433: CHIP_ID2_REG (0x50040004)

Bit	Mode	Symbol	Description	Reset
7:0	R	CHIP_ID2	Second character of device type in ASCII.	0x31

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Table 1434: CHIP_ID3_REG (0x50040008)

Bit	Mode	Symbol	Description	Reset
7:0	R	CHIP_ID3	Third character of device type in ASCII.	0x30

Table 1435: CHIP_ID4_REG (0x5004000C)

Bit	Mode	Symbol	Description	Reset
7:0	R	CHIP_ID4	Fourth character of device type in ASCII.	0x37

Table 1436: CHIP_SWC_REG (0x50040010)

Bit	Mode	Symbol	Description	Reset
3:0	R	CHIP_SWC	**S**oft**Wa**re **C**ompatibility code. Integer (default = 0) which is incremented if a silicon change has impact on the CPU Firmware. Can be used by software developers to write silicon revision dependent code.	0x0

Table 1437: CHIP_REVISION_REG (0x50040014)

Bit	Mode	Symbol	Description	Reset
7:0	R	CHIP_REVISION	Chip version, corresponds with type number in ASCII. 0x41 = A, 0x42 = B	0x41

Table 1438: CHIP_TEST1_REG (0x500400F8)

Bit	Mode	Symbol	Description	Reset
7:0	R	CHIP_LAYOUT_REVISION	Chip layout revision, corresponds with type number in ASCII. 0x41 = A, 0x42 = B	0x42

Table 1439: CHIP_TEST2_REG (0x500400FC)

Bit	Mode	Symbol	Description	Reset
3:0	R	CHIP_METAL_OPTION	Chip metal option value.	0x0

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44.34 Wake-Up Controller Registers

Table 1440: Register map WakeUp

Address	Register	Description
0x50000900	WKUP_CTRL_REG	Control register for the wakeup counter
0x50000904	WKUP_RESET_IRQ_REG	Reset wakeup interrupt
0x50000908	WKUP_SELECT_P0_REG	Select which inputs from P0 port can trigger wkup counter
0x5000090C	WKUP_SELECT_P1_REG	Select which inputs from P1 port can trigger wkup counter
0x50000910	WKUP_SELECT_P2_REG	Select which inputs from P2 port can trigger wkup counter
0x50000914	WKUP_POL_P0_REG	select the sesitivity polarity for each P0 input
0x50000918	WKUP_POL_P1_REG	select the sesitivity polarity for each P1 input
0x5000091C	WKUP_POL_P2_REG	select the sesitivity polarity for each P2 input
0x50000920	WKUP_STATUS_P0_REG	Event status register for P0
0x50000924	WKUP_STATUS_P1_REG	Event status register for P1
0x50000928	WKUP_STATUS_P2_REG	Event status register for P2
0x5000092C	WKUP_CLEAR_P0_REG	Clear event register for P0
0x50000930	WKUP_CLEAR_P1_REG	Clear event register for P1
0x50000934	WKUP_CLEAR_P2_REG	Clear event register for P2
0x50000938	WKUP_SEL_GPIO_P0_REG	Enable fast wakeup and enable GPIO_P0_IRQ
0x5000093C	WKUP_SEL_GPIO_P1_REG	Enable fast wakeup and enable GPIO_P1_IRQ
0x50000940	WKUP_SEL_GPIO_P2_REG	Enable fast wakeup and enable GPIO_P2_IRQ
0x50000944	WKUP_SEL1_GPIO_P0_REG	Configure to generate level or edge sensitive IRQ on P0 events
0x50000948	WKUP_SEL1_GPIO_P1_REG	Configure to generate level or edge sensitive IRQ on P1 events
0x5000094C	WKUP_SEL1_GPIO_P2_REG	Configure to generate level or edge sensitive IRQ on P2 events

Table 1441: WKUP_CTRL_REG (0x50000900)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x0
7	R/W	WKUP_ENABLE_IRQ	0: no interrupt will be enabled 1: if you have an event an IRQ will be generated	0x0

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Bit	Mode	Symbol	Description	Reset
6	R/W	WKUP_SFT_KEYHIT	0 = no effect 1 = emulate key hit. First make this bit 0 before any new key hit can be sensed.	0x0
5:0	R/W	WKUP_DEB_VALUE	Wakeup debounce time. If set to 0, no debouncing will be done. Debounce time: N*1 ms. N =1..63 Note: Depending on the time key is pressed, debounce time can be less than N*1 ms. To make sure that debounce time is bigger than the programmed time, program this register field to ("desired value"+1). So, if at least 2 ms of debounce time is required, program the register to 3.	0x0

Table 1442: WKUP_RESET_IRQ_REG (0x50000904)

Bit	Mode	Symbol	Description	Reset
15:0	W	WKUP_IRQ_RST	Writing any value to this register will reset the interrupt. Reading always returns 0.	0x0

Table 1443: WKUP_SELECT_P0_REG (0x50000908)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	WKUP_SELECT_P0	0: input P0_xx is not enabled for wakeup event 1: input P0_xx is enabled for wakeup event	0x0

Table 1444: WKUP_SELECT_P1_REG (0x5000090C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	WKUP_SELECT_P1	0: input P1_xx is not enabled for wakeup event 1: input P1_xx is enabled for wakeup event	0x0

Table 1445: WKUP_SELECT_P2_REG (0x50000910)

Bit	Mode	Symbol	Description	Reset
14:0	R/W	WKUP_SELECT_P2	0: input P2_xx is not enabled for wakeup event 1: input P2_xx is enabled for wakeup event	0x0

Table 1446: WKUP_POL_P0_REG (0x50000914)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	WKUP_POL_P0	0: enabled input P0_xx will give an event if that input goes high 1: enabled input P0_xx will give an event if that input goes low	0x0

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Table 1447: WKUP_POL_P1_REG (0x50000918)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	WKUP_POL_P1	0: enabled input P1_xx will give an event if that input goes high 1: enabled input P1_xx will give an event if that input goes low	0x0

Table 1448: WKUP_POL_P2_REG (0x5000091C)

Bit	Mode	Symbol	Description	Reset
14:0	R/W	WKUP_POL_P2	0: enabled input P2_xx will give an event if that input goes high 1: enabled input P2_xx will give an event if that input goes low	0x0

Table 1449: WKUP_STATUS_P0_REG (0x50000920)

Bit	Mode	Symbol	Description	Reset
31:0	R	WKUP_STAT_P0	Contains the latched value of any toggle of the GPIOs Port P0. WKUP_STAT_P0[0] -> P0_00.	0x0

Table 1450: WKUP_STATUS_P1_REG (0x50000924)

Bit	Mode	Symbol	Description	Reset
31:0	R	WKUP_STAT_P1	Contains the latched value of any toggle of the GPIOs Port P1. WKUP_STAT_P1[0] -> P1_00.	0x0

Table 1451: WKUP_STATUS_P2_REG (0x50000928)

Bit	Mode	Symbol	Description	Reset
14:0	R	WKUP_STAT_P2	Contains the latched value of any toggle of the GPIOs Port P2. WKUP_STAT_P2[0] -> P2_00.	0x0

Table 1452: WKUP_CLEAR_P0_REG (0x5000092C)

Bit	Mode	Symbol	Description	Reset
31:0	W	WKUP_CLEAR_P0	Clear latched value of the GPIOs P0 when corresponding bit is 1	0x0

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Table 1453: WKUP_CLEAR_P1_REG (0x50000930)

Bit	Mode	Symbol	Description	Reset
31:0	W	WKUP_CLEAR_P1	Clear latched value of the GPIOs P1 when corresponding bit is 1	0x0

Table 1454: WKUP_CLEAR_P2_REG (0x50000934)

Bit	Mode	Symbol	Description	Reset
14:0	W	WKUP_CLEAR_P2	Clear latched value of the GPIOs P2 when corresponding bit is 1	0x0

Table 1455: WKUP_SEL_GPIO_P0_REG (0x50000938)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	WKUP_SEL_GPIO_P0	0: No GPIO_P0_IRQ on input P0_x. Fast wake-up is not enabled if the corresponding WKUP_SEL1_GPIO_P0_REG[x] is 0 too. 1: GPIO_P0_IRQ will be generated on P0_x input event. If WKUP_SEL1_GPIO_P0_REG[x] is 0, IRQ generation is level sensitive. If WKUP_SEL1_GPIO_P0_REG[x] is 1, IRQ generation is edge sensitive (only if there is a change on P0_x input). Fast wake-up from the corresponding P0_x input is enabled.	0x0

Table 1456: WKUP_SEL_GPIO_P1_REG (0x5000093C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	WKUP_SEL_GPIO_P1	0: No GPIO_P1_IRQ on input P1_x. Fast wake-up is not enabled if the corresponding WKUP_SEL1_GPIO_P1_REG[x] is 0 too. 1: GPIO_P1_IRQ will be generated on P1_x input event. If WKUP_SEL1_GPIO_P1_REG[x] is 0, IRQ generation is level sensitive. If WKUP_SEL1_GPIO_P1_REG[x] is 1, IRQ generation is edge sensitive (only if there is a change on P1_x input). Fast wake-up from the corresponding P1_x input is enabled.	0x0

Table 1457: WKUP_SEL_GPIO_P2_REG (0x50000940)

Bit	Mode	Symbol	Description	Reset
14:0	R/W	WKUP_SEL_GPIO_P2	0: No GPIO_P2_IRQ on input P2_x. Fast wake-up is not enabled if the corresponding WKUP_SEL1_GPIO_P2_REG[x] is 0 too. 1: GPIO_P2_IRQ will be generated on P1_x input event. If WKUP_SEL1_GPIO_P2_REG[x] is 0, IRQ generation is level sensitive. If	0x0

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Bit	Mode	Symbol	Description	Reset
			WKUP_SEL1_GPIO_P2_REG[x] is 1, IRQ generation is edge sensitive (only if there is a change on P2_x input). Fast wake-up from the corresponding P2_x input is enabled.	

Table 1458: WKUP_SEL1_GPIO_P0_REG (0x50000944)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	WKUP_SEL1_GPIO_P0	0 (level sensitive): If WKUP_SEL_GPIO_P0_REG[x] is 1, generate GPIO_P0_IRQ based on P0_x level. Fast wake-up is not enabled if the corresponding WKUP_SEL_GPIO_P0_REG[x] is 0 too. 1 (edge sensitive): If WKUP_SEL_GPIO_P0_REG[x] is 1, GPIO_P0_IRQ will be generated only on rising/falling (defined by WKUP_POL_P0_REG) edge on P0_x. Fast wake-up from the corresponding P0_x input is enabled.	0x0

Table 1459: WKUP_SEL1_GPIO_P1_REG (0x50000948)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	WKUP_SEL1_GPIO_P1	0 (level sensitive): If WKUP_SEL_GPIO_P1_REG[x] is 1, generate GPIO_P1_IRQ based on P1_x level. Fast wake-up is not enabled if the corresponding WKUP_SEL_GPIO_P1_REG[x] is 0 too. 1 (edge sensitive): If WKUP_SEL_GPIO_P1_REG[x] is 1, GPIO_P1_IRQ will be generated only on rising/falling (defined by WKUP_POL_P1_REG) edge on P1_x. Fast wake-up from the corresponding P1_x input is enabled.	0x0

Table 1460: WKUP_SEL1_GPIO_P2_REG (0x5000094C)

Bit	Mode	Symbol	Description	Reset
14:0	R/W	WKUP_SEL1_GPIO_P2	0 (level sensitive): If WKUP_SEL_GPIO_P2_REG[x] is 1, generate GPIO_P2_IRQ based on P2_x level. Fast wake-up is not enabled if the corresponding WKUP_SEL_GPIO_P2_REG[x] is 0 too. 1 (edge sensitive): If WKUP_SEL_GPIO_P2_REG[x] is 1, GPIO_P2_IRQ will be generated only on	0x0

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Bit	Mode	Symbol	Description	Reset
			rising/falling (defined by WKUP_POL_P2_REG) edge on P1_x. Fast wake-up from the corresponding P2_x input is enabled.	

44.35 Watchdog Controller Registers

Table 1461: Register map WDOG

Address	Register	Description
0x50000700	WATCHDOG_REG	Watchdog timer register.
0x50000704	WATCHDOG_CTRL_REG	Watchdog control register.

Table 1462: WATCHDOG_REG (0x50000700)

Bit	Mode	Symbol	Description	Reset
31:14	R0/W	WDOG_WEN	Bit [31:14] = 0 = Write enable for Watchdog timer else Write disable. This filter prevents unintentional presetting the watchdog with a SW run-away.	0x0
13	R/W	WDOG_VAL_NEG	0 = Watchdog timer value is positive. 1 = Watchdog timer value is negative.	0x0

12:0	R/W	WDOG_VAL	Write: Watchdog timer reload value. Note that all bits [31-14] must be 0 to reload this register.
			Read: Actual Watchdog timer value. Decremented by 1 every ~10 msec (RC32K) or ~29 msec (RCX), i.e. the Watchdog timer clock tick.
			Bit 13 indicates a negative counter value. 2, 1, 0, $3FFF_{16}$, $3FFE_{16}$ etc. An NMI or WDOG (SYS) reset is generated under the following conditions:
			If WATCHDOG_CTRL_REG[NMI_RST] = 0 then
			If WDOG_VAL = 0 -> NMI (Non Maskable Interrupt)
			if WDOG_VAL =$3FF0_{16}$ -> WDOG reset -> reload $1FFF_{16}$
			If WATCHDOG_CTRL_REG[NMI_RST] = 1 then
			if WDOG_VAL <= 0 -> WDOG reset -> reload $1FFF_{16}$
			Note 1: The programmed value WDOG_VAL is updated in the (independent) Watchdog timer at the 2nd next RC32K or RCX clock tick.
			Note 2: Select RC32K or RCX with CLK_RCX_REG[RCX_ENABLE]. The RC32K is selected by default.
			Note 3: If WATCHDOG_CTRL_REG[NMI_RST] = 0, the time between the NMI generation and the WDOG reset generation is 15 Watchdog timer clock ticks.
				0x1FFF

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Table 1463: WATCHDOG_CTRL_REG (0x50000704)

Bit	Mode	Symbol	Description	Reset
31:4	R	-	Reserved	0x0
3	R	WRITE_BUSY	0 = A new WATCHDOG_REG[WDOG_VAL] can be written. 1 = No new WATCHDOG_REG[WDOG_VAL] can be written. Note: It takes some time before the programmed WDOG_VAL is updated in the (independent) Watchdog timer. During this time it is not possible to write a new value to WATCHDOG_REG[WDOG_VAL].	0x0
2	R/W	WDOG_FREEZE_EN	0 = Watchdog timer can not be frozen when NMI_RST=0. 1 = Watchdog timer can be frozen/resumed using SET_FREEZE_REG[FRZ_WDOG]/ RESET_FREEZE_REG[FRZ_WDOG] when NMI_RST=0. Note: Although this bit is retained during sleep, the SET_FREEZE_REG[FRZ_SYS_WDOG] is not, so the watchdog cannot be frozen during CM33 sleep.	0x1
1	R/W	-	Reserved	0x1
0	R/W	NMI_RST	0 = Watchdog timer generates NMI at value 0, and WDOG (SYS) reset at <= -16. Timer can be frozen/resumed using SET_FREEZE_REG[FRZ_WDOG]/ RESET_FREEZE_REG[FRZ_WDOG]. 1 = Watchdog timer generates a WDOG (SYS) reset at value 0 and can not be frozen by Software. Note that this bit can only be set to 1 by SW and only be reset with a WDOG (SYS) reset or SW reset. The watchdog is always frozen when the Cortex-M33 is halted in DEBUG State.	0x0

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45 Ordering Information

Table 1464: Ordering Information (Samples)

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA14701-00000HZ2	VFBGA142	6.2 x 6 x 0.82	Reel	100/1000
DA14705-00000HZ2	VFBGA142	6.2 x 6 x 0.82	Reel	100/1000
DA14706-00000HZ2	VFBGA142	6.2 x 6 x 0.82	Reel	100/1000
DA14708-00000HZ2	VFBGA142	6.2 x 6 x 0.82	Reel	100/1000

Table 1465: Ordering Information (Production)

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA14701-00000HZ2	VFBGA142	6.2 x 6 x 0.82	Reel	4000
DA14705-00000HZ2	VFBGA142	6.2 x 6 x 0.82	Reel	4000
DA14706-00000HZ2	VFBGA142	6.2 x 6 x 0.82	Reel	4000
DA14708-00000HZ2	VFBGA142	6.2 x 6 x 0.82	Reel	4000

Part Number Legend:

DA1470x-RRXXXYYZ

RR: chip revision number

XXX: variant (00T: High Temperature)

YY: package code (HZ: VFBGA142)

Z: packing method (1: Tray, 2: Reel, A: Mini-Reel)

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46 Package Information

46.1 Moisture Sensitivity Level (MSL)

The MSL is an indicator for the maximum allowable period (floor lifetime) in which a moisture-sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60 % RH before the solder reflow process.

VFBGA packages are qualified for MSL 3.

MSL Level	Floor Lifetime
MSL 4	72 hours
MSL 3	168 hours
MSL 2A	4 weeks
MSL 2	1 year
MSL 1	Unlimited at 30 °C/85 % RH

46.2 Soldering Information

Refer to the JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

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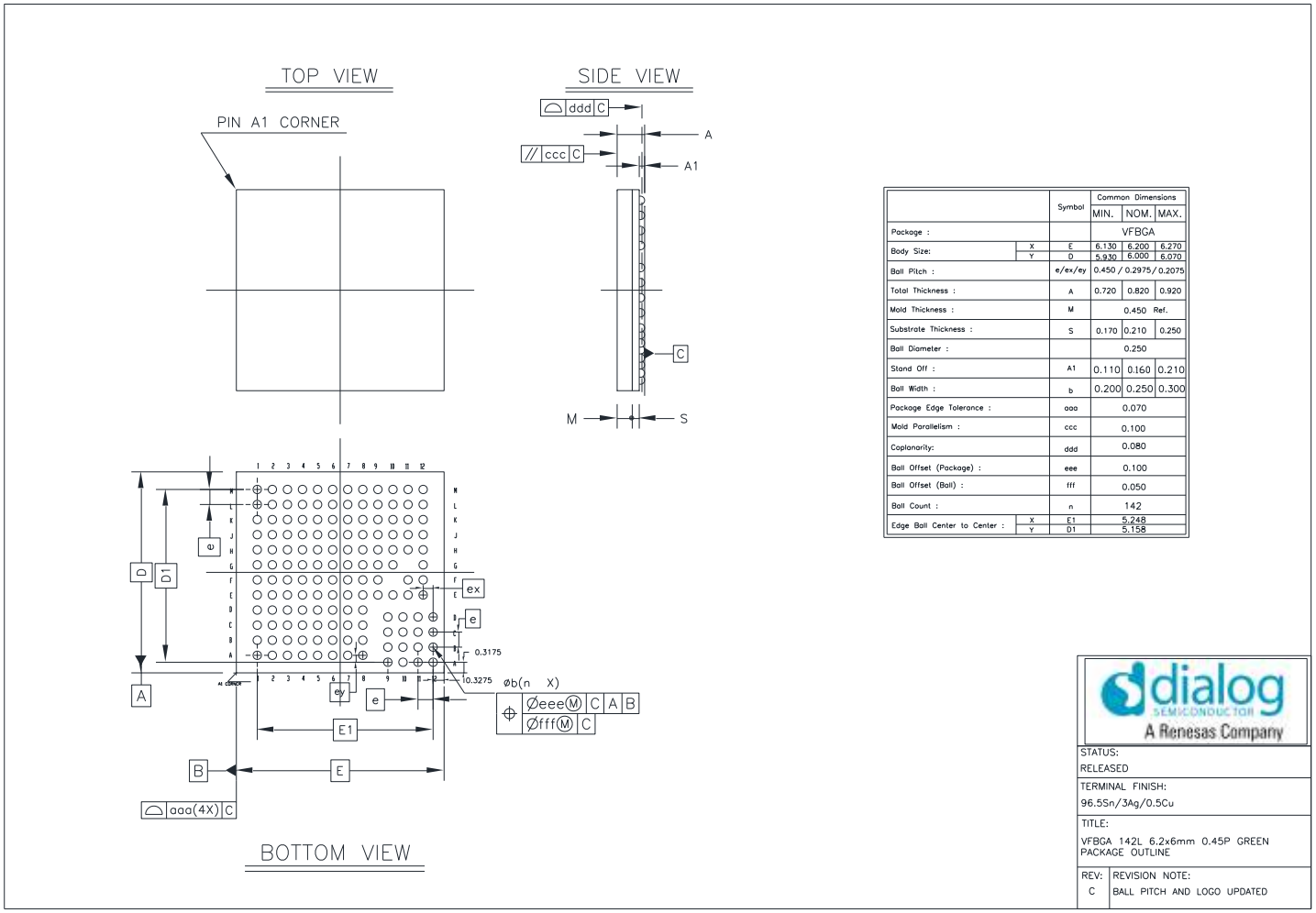
47 Package Outline Drawing



		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package :			VFBGA		
Body Size:	X	E	6.130	6.200	6.270
	Y	D	5.930	6.000	6.070
Ball Pitch :		e/ex/ey	0.450 / 0.2975 / 0.2075		
Total Thickness :		A	0.720	0.820	0.920
Mold Thickness :		M		0.450 Ref.	
Substrate Thickness :		S	0.170	0.210	0.250
Ball Diameter :				0.250	
Stand Off :		A1	0.110	0.160	0.210
Ball Width :		b	0.200	0.250	0.300
Package Edge Tolerance :		aaa		0.070	
Mold Parallelism :		ccc		0.100	
Coplanarity:		ddd		0.080	
Ball Offset (Package) :		eee		0.100	
Ball Offset (Ball) :		fff		0.050	
Ball Count :		n		142	
Edge Ball Center to Center :	X	E1		5.248	
	Y	D1		5.158	

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STATUS:
RELEASED

TERMINAL FINISH:
96.5Sn/3Ag/0.5Cu

TITLE:
VFBGA 142L 6.2x6mm 0.45P GREEN PACKAGE OUTLINE

REV:	REVISION NOTE:
C	BALL PITCH AND LOGO UPDATED

Figure 115: VFBGA142 Package Outline Drawing

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Revision History

Revision	Date	Description
3.2	10-Nov-2022	Product status: Production. Datasheet status: Final.
Changelog: ● Updated specification parameters ● Updated registers ● Updated the Quad SPI FLASH/RAM Controllers section ● Updated Figure 3, Figure 14 ● Updated Table 81 ● Corrected typos		
3.1	10-Jun-2022	Product status: Production. Datasheet status: Final.
Changelog: ● Added the eMMC Host Controller section ● Updated specification parameters ● Updated registers ● Updated key features ● Updated the following sections: ○ LED Drivers ○ Display Controller ○ Configurable MAC ○ Application ADC ● Updated Table 126, Table 179 ● Updated Figure 3, Figure 14, Figure 39 ● Removed the ANT+ and Long Range references		
3.0	19-Nov-2021	Product status: Production. Datasheet status: Final.
Changelog: ● Updated Package Outline Drawing ● Updated SPI timmings ● Updated I2C programming section ● Updated specification parameters ● Updated Product Family members and configurations ● Register description typos and text corrections		
2.1	24-Sept-2021	Product status: Qualification. Datasheet status: Preliminary.
Changelog: ● Updated RCHS precision specification parameter to be depending on calibration ● Updated GPADC block diagram ● Corrected typos		
2.0	05-Aug-2021	Product status: Qualification. Datasheet status: Preliminary.
Changelog: ● Removed DA14707 and DA14709 devices ● Added programming sequences in all chapters ● Changed minimum VBAT voltage specification from 2.8 V to 2.9 V ● Brown-out Detector: Changed block diagram ● LEDs Driver: Changed block diagram ● Rails Discharge: Updated the block diagram ● Updated power-up and wake-up from hibernation timing diagrams		

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Revision	Date	Description
1.3	08-Jun-2021	Product status: Qualification. Datasheet status: Target.
1.2	15-Dec-2020	Product status: Development. Datasheet status: Target.
1.1	05-Oct-2020	Product status: Development. Datasheet status: Target.
1.0	11-Jun-2020	Product status: Development. Datasheet status: Target.

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Status Definitions

Revision	Datasheet status	Product status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via https://www.renesas.com/.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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