

DA14AVDDECT SF01

General Description

The DA14AVDDECT from Renesas is a member of the wireless module family that operates in the interference-free DECT frequency band (1.9 GHz) and can be used in hosted or embedded Audio, Voice, and Data applications. The module includes all the required radio components, antenna, a low-power audio CODEC (DA7218), and a 32 Mb FLASH memory. The module is intended for users who are familiar with application-level software programming but does not require detailed understanding of the DECT protocol to facilitate rapid design-in cycles. The module can be operated as a stand-alone device or from a host through an API interface.

The module is based on Renesas DA14495 chip that supports DQPSK and D8PSK besides the traditional GFSK. This increases the raw air data rate by up to three times.

The module is available with 1.5 mm pitch BGA solder balls for excellent solderability and sufficient connectivity. The dimensions for the module are 17.0 mm × 26.65 mm.

This document describes the hardware of the DA14AVDDECT module. A separate document details the software and APIs.

Key Features

- All RF components are integrated, thus no customer tuning is required
- Supported bands include EU-DECT, DECT 6.0 for North America, and Japan DECT (JDECT)
- On-PCB antenna, the module also supports an optional second external antenna
- Integrated RF shield
- Low power operations
- Audio bandwidth from 20 Hz to 20 kHz
- 32-Mbit FLASH, so program memory available for custom software
- Integrated audio ADC/DAC (external audio ADC/DAC supported through GPIO mapping)
- Limited modular approval for EN301-406 (EU-DECT), FCC Part 15 (DECT 6.0), and TELEC (J-DECT)
- Supports NiMH, alkaline, and Li-Ion batteries
- A Voice Data Stack or an Audio Data Stack are available to be downloaded

Applications (Defined by Software)

- Public Address solution with four microphones
- Tour Guide Systems for up to 1024 listeners
- Conferencing Systems with eight participants
- Wireless Intercom Systems supporting HD Voice
- Wireless Stereo Headphones and Headsets
- Wireless Low Latency Microphones

System Diagram

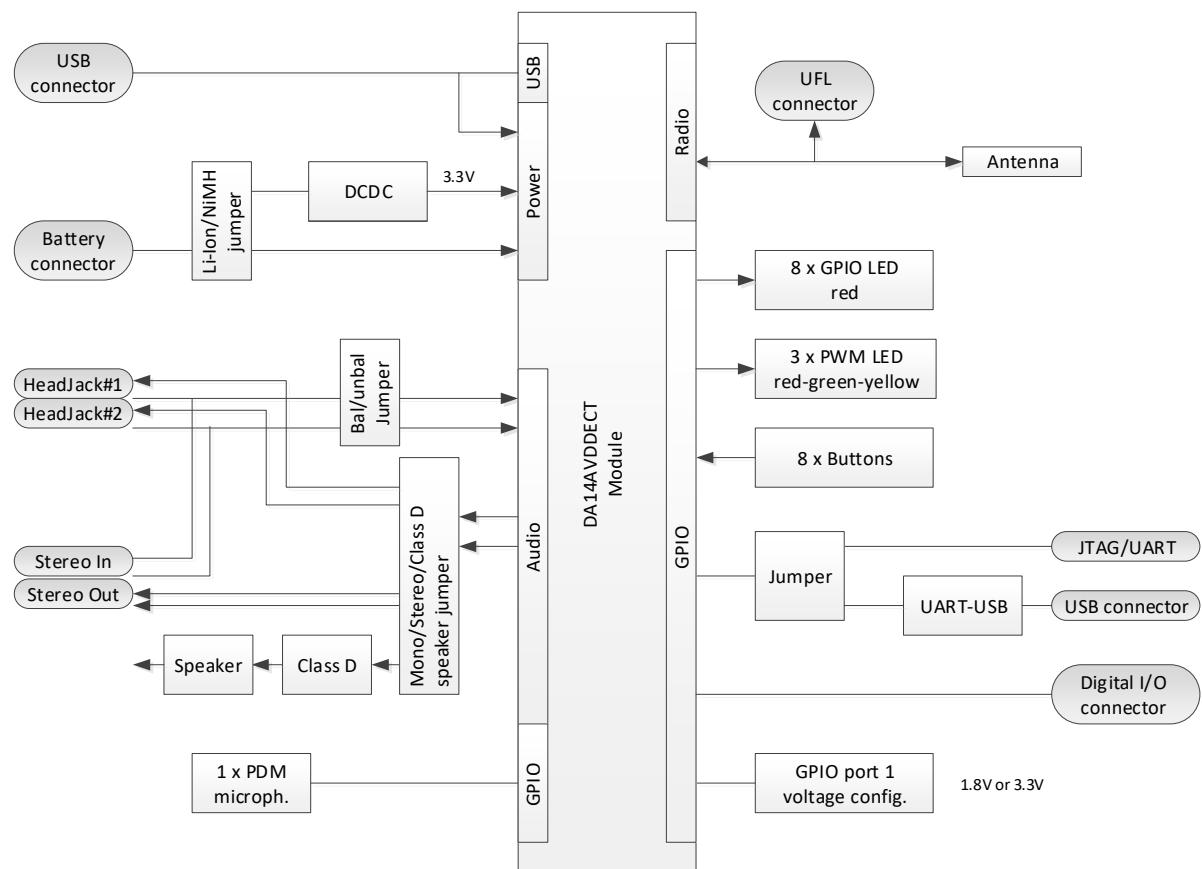


Figure 1. System diagram

Contents

| | |
|---|----|
| General Description | 1 |
| Key Features | 1 |
| Applications (Defined by Software) | 1 |
| System Diagram | 2 |
| Contents | 3 |
| Figures | 3 |
| Tables | 3 |
| 1. References | 4 |
| 2. Block Diagram | 5 |
| 3. Pinout | 6 |
| 4. Characteristics | 12 |
| 4.1 Absolute Maximum Ratings..... | 12 |
| 4.2 Recommended Operating Conditions | 12 |
| 4.3 Electrical Characteristics | 13 |
| 5. Functional Description | 16 |
| 6. Package Information | 17 |
| 6.1 Package Outline Drawing | 17 |
| 6.2 Moisture Sensitivity Level | 18 |
| 6.3 Soldering Information..... | 18 |
| 6.4 Packaging | 19 |
| 7. Ordering Information | 20 |
| 8. Application Information | 21 |
| 8.1 Audio Connections..... | 22 |
| 9. Layout Guidelines | 23 |
| Revision History | 24 |

Figures

| | |
|---|----|
| Figure 1. System diagram..... | 2 |
| Figure 2. Block diagram..... | 5 |
| Figure 3. DA14AVDDECT BGA pinout diagram (top view) | 6 |
| Figure 4. DA14AVDDECT BGA package outline drawing..... | 17 |
| Figure 5. Reflow profile (lead-free) | 18 |
| Figure 6. DA14AVDDECT package marking..... | 19 |
| Figure 7. Connection of analog microphones..... | 22 |
| Figure 8. Keep-out areas | 23 |

Tables

| | |
|---|----|
| Table 1. Pin description | 7 |
| Table 2. Pin type definition | 11 |
| Table 3. Absolute maximum ratings | 12 |
| Table 4. Recommended operating conditions | 12 |
| Table 5. Digital I/O characteristics | 13 |
| Table 6. Radio characteristics | 13 |

| | |
|---|----|
| Table 7. Supply currents (Tour Guide mode) | 13 |
| Table 8. Supply currents (Public Address mode) | 14 |
| Table 9. Supply currents (Voice Conference mode)..... | 14 |
| Table 10. MSL classification | 18 |
| Table 11. DA14AVDDECT package marking table | 19 |
| Table 12. Ordering information..... | 20 |

1. References

- [1] DA14495, Datasheet, Renesas Electronics.
- [2] DA7218, Datasheet, Renesas Electronics.
- [3] UM-D-011, DA14AVDDECT Production Programming and Configuration Manual, User Manual, Renesas Electronics.
- [4] AN-D-236, DA14AVDDECT External Antenna Design, Application Note, Renesas Electronics.
- [5] DA14AVDDECT CVM software.
- [6] DA14AVDDECT WAM software.
- [7] UM-D-012, DA14AVDDECT Software Developer's Guide, User Manual, Renesas Electronics.

2. Block Diagram

The DA14AVDDECT module is built around Renesas DA14495 DECT chip. The module integrates RF components (that is, baluns, switches, RFPA, and crystal) with an integrated antenna. It also allows an additional external antenna to be connected to support antenna diversity.

A low-power audio CODEC from Renesas (DA7218) is integrated to support analog audio applications. A 32-Mb Flash is integrated into custom software.

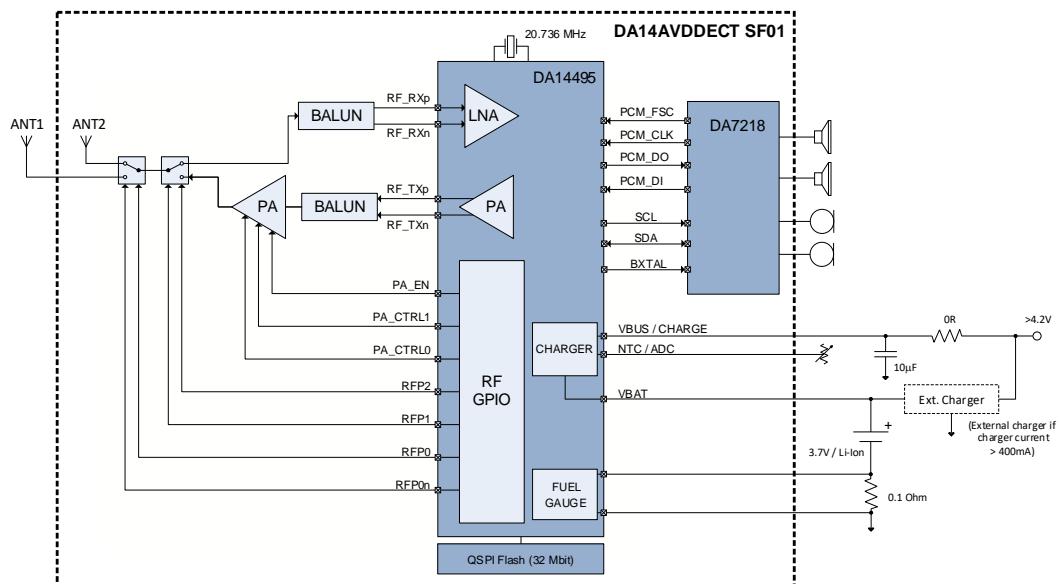


Figure 2. Block diagram

The block diagram in [Figure 2](#) demonstrates the stereo audio capability. The hardware of the DA14AVDDECT supports these connections, but the current software implementations only support mono audio.

3. Pinout

With [Figure 3](#) the pin functions can easily be identified. See Section 6 for an accurate mechanical representation.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---------------|-----------------|--------|-----------|-------------|---------------|--------|-----------------|-------------|-------------|-----------|
| A | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| B | NC | GND | GND | GND | GND | GND | GND | GND | GND | GND | +VRF_PA_2 |
| C | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | +VRF_PA_2 |
| D | ANT1 | GND | GND | GND | GND | GND | GND | GND | P1.8 | GND | |
| E | GND | GND | GND | GND | GND | GND | GND | +VRF_PA_1 | P2.3 | P1.7 | +VSUPPLY |
| F | GND | GND | GND | GND | GND | GND | GND | P2.0 | P2.6 / LED0 | P2.7 / LED1 | P1.4 |
| G | GND | GND | GND | GND | GND | RST | GND | P2.2 | NC | P1.6 | P2.1 |
| H | GND | NC | GND | +1.8V | P0.14 / NTC | P0.13 | NC | P2.8 / LED2 | P1.5 | P1.3 | P1.1 |
| J | GND | NC | GND | GND | SOCN | NC | P0.0 | P0.10 / I2C-CLK | P1.11 | P1.2 | P1.10 |
| K | MICBIAS1 | P0.12 | +3.3V | P0.15 PON | VBAT | SOCP | P0.1 | P0.4 | P1.9 | P1.0 | VDDIO1 |
| L | CODEC ADDRESS | P2.5 / I2C-DATA | GND | NC | VBAT | P0.3 | P0.2 | SWCLK | P0.6 | P0.7 | P1.12 |
| M | MIC2_P | GND | HPLDET | NC | HPR | P0.11 (BXTAL) | USBN | USBP | SWDIO | NC | P0.5 |
| N | MIC2_N | MIC1_P | MIC1_N | MICBIAS2 | GND | HPL | +VDCDC | VBUS / CHARGE | GND | NC | GND |

Figure 3. DA14AVDDECT BGA pinout diagram (top view)

NOTE

On the bottom (ball) side of the module, at the end of the printed antenna pattern, there is a ball "T1" (see the lower left corner of [Figure 4](#)). This is for Renesas production test purposes only and serves no customer application use. The customer application shall not have a solder connection to T1.

Table 1. Pin description

| Pin No. | Pin name | Type (Table 2) | Drive (mA) | Reset state | Description |
|--------------|---------------|-------------------|---------------|----------------|--|
| RF | | | | | |
| D1 | ANT1 | AIO | | | RF connection ANT1 This pin is used together with the integrated printed antenna to connect an external antenna to support antenna diversity. |
| T1 | ANT_TEST | AIO | | | The PCB of a customer application shall not have a solder connection to T1. |
| Power | | | | | |
| E8 | +VRF_PA_1 | PWR | | | Input supply voltage of RFPA bias stage |
| B11, C11 | +VRF_PA_2 | PWR | | | Input supply voltage of RFPA power stage |
| H4 | +1.8V | PWR | | | Output supply voltage 1.8 V It can be used to configure the GPIO voltage of bank 1 (VDDIO1), for example. Note: GPIO voltage of bank 0 and 2 is always supplied from 1.8 V. |
| K3 | +3.3V | PWR | | | Output supply voltage 3.3 V It can be used to configure the GPIO voltage of bank 1 (VDDIO1), for example. |
| K5, L5 | VBAT | PWR | | | Main input supply voltage |
| K11 | VDDIO | PWR | | | Input supply voltage of GPIO bank 1 |
| N7 | +VDCDC | PWR | | | Output supply voltage of internal DCDC converter It can be used as an input when the internal DCDC is disabled. |
| N8 | VBUS/CHARGE | PWR | | | Input supply voltage of the battery charger and/or the USB |
| E11 | VSUPPLY | PWR | | | Output voltage of DA14495 |
| Audio | | | | | |
| K1 | MICBIAS1 | AO | | | Microphone bias output 1 (requires 1 μ F decoupling) |
| N2 | MIC1_P | AI | | | Differential analog microphone 1 input (Pos) |
| N3 | MIC1_N | AI | | | Differential analog microphone 1 input (Neg) |
| N4 | MICBIAS2 | AO | | | Microphone bias output 2 (requires 1 μ F decoupling) |
| M1 | MIC2_P | AI | | | Differential analog microphone 2 input (Pos) |
| N1 | MIC2_N | AI | | | Differential analog microphone 2 input (Neg) |
| M3 | HPLDET | AI | | | Current source for headphone detection |
| M5 | HPR | AO | | | Single-ended headphone output (Right) |
| N6 | HPL | AO | | | Single-ended headphone output (Left) |
| L1 | CODEC ADDRESS | DI | | | Connecting this pin to GND selects the I ₂ C slave address 0x1A; connecting this pin to pin H4 selects the I ₂ C slave address 0x1B. |
| USB | | | | | |

| Pin No. | Pin name | Type (Table 2) | Drive (mA) | Reset state | Description |
|--------------------------|-----------|-------------------|---------------|--|---|
| M7 | USBN | A11 | | Hi-Z | INPUT/OUTPUT. USB-. Typical HS output impedance is 45 Ω. |
| M8 | USBP | A11 | | Hi-Z | INPUT/OUTPUT. USB+. Typical HS output impedance is 45 Ω. |
| JTAG | | | | | |
| L8 | SWCLK | DI-BP | | I_PD | INPUT. Arm debug interface clock. |
| M9 | SWDIO | DIO-BP | 4/8 | I_PU | INPUT/OUTPUT. Arm debug interface data input/output. |
| Special Functions | | | | | |
| G6 | RSTn | A5 | | 25 kΩ pull-up resistor connected to VDD1V2 | INPUT/OPEN DRAIN OUTPUT with internal pull-up. Reset signal (active LOW). No external capacitor required. If the internal VDD1V2 drops below 1.06 V, this pin is pulled low. An external device may not drive this pin higher than VDD1V2 (1.2V). |
| J5 | SOCN | A1 | | I | INPUT. Battery fuel gauge reference ground. Connect as star point. If it is not used, connect it to GND to prevent a false power-on trigger (NEW_BAT) due to a floating pin. |
| K6 | SOCP | A1 | | I | INPUT. Battery fuel gauge positive input. If it is not used, connect it to VSS to prevent a false power-on trigger (NEW_BAT) due to a floating pin. |
| K4 | P0.15/PON | DI | 4/8 | I_PD | INPUT with a selectable pull-up/down resistor. Note: P0.15 cannot be used as output. INPUT. Device Power-on. It can be directly connected to VBAT (max 5 V). If PON has a fixed connection to VBAT, the PD resistor can be disabled to save power. |
| F9 | P2.6/LED0 | DIO-BP DO-BP | 4/8/16 | I_PU | INPUT/OUTPUT with a selectable pull-up/down resistor. OUTPUT: Back drive protected pad for LED0 up to VSUPPLY. A series of resistors is required for LED operation. |
| F10 | P2.7/LED1 | DIO-BP DO-BP | 4/8/16 | I_PU | INPUT/OUTPUT with a selectable pull-up/down resistor. OUTPUT: Back drive protected pad for LED1 up to VSUPPLY. A series of resistors is required for LED operation. |
| H8 | P2.8/LED2 | DIO-BP DO-BP | 4/8/16 | I_PU | INPUT/OUTPUT with a selectable pull-up/down resistor. OUTPUT: Back drive protected pad for LED2 up to VSUPPLY. A series of resistors is required for LED operation. |

| Pin No. | Pin name | Type (Table 2) | Drive (mA) | Reset state | Description |
|---------------------------|---------------|--------------------|---------------|----------------|--|
| H5 | P0.14/NTC | DIO-BP AI AI | 4/8 | I_PD | <p>INPUT/OUTPUT with a selectable pull-up/down resistor.</p> <p>ANALOG INPUT: Analog to Digital Converter (ADC) input 0.</p> <p>ANALOG INPUT: Li-Ion/Li_Po NTC protection which is used to automatically switch off the charger circuit if this input goes beyond the specified voltage ranges.</p> <p>Note: Only GPIO port (I/O), digital input, and the analog function are available; no peripheral outputs are available.</p> |
| L2 | P2.5/I2C_DATA | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| J8 | P0.10/I2C_CLK | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| M6 | P0.11/BXTAL | DIO | 4/8 | I_PD | <p>INPUT/OUTPUT with a selectable pull-up/down resistor.</p> <p>OUTPUT: PLL Codec output (12.288 MHz/24.567 MHz).</p> <p>Supplied from VDDIO_BXTAL.</p> |
| General Purpose IO | | | | | |
| J7 | P0.0 | DIO | 4/8 | I_PU | <p>INPUT/OUTPUT with a selectable pull-up/down resistor.</p> <p>If 0 is on the rising edge of the RSTn pin, boot the module from UART. Assign the module as UTX if the module is booted from UART</p> |
| K7 | P0.1 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. Assign the module as URX if the module is booted from UART. |
| L7 | P0.2 | DIO | 4/8 | I_PD | <p>INPUT/OUTPUT with a selectable pull-up/down resistor.</p> <p>If 1 is on the rising edge of the RSTn pin, the Booter waits in an endless loop for debugging purposes.</p> |
| L6 | P0.3 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| K8 | P0.4 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| M11 | P0.5 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| L9 | P0.6 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| L10 | P0.7 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| K2 | P0.12 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| H6 | P0.13 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |

| Pin No. | Pin name | Type (Table 2) | Drive (mA) | Reset state | Description |
|---|----------|-------------------|---------------|----------------|---|
| K10 | P1.0 | DIO | 4/8/12/16 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| H11 | P1.1 | DIO | 4/8/12/16 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| J10 | P1.2 | DIO | 4/8/12/16 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| H10 | P1.3 | DIO | 4/8/12/16 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| F11 | P1.4 | DIO | 4/8/12/16 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| H9 | P1.5 | DIO | 4/8/12/16 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| G10 | P1.6 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| E10 | P1.7 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| D10 | P1.8 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| K9 | P1.9 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| J11 | P1.10 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| J9 | P1.11 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| L11 | P1.12 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| F8 | P2.0 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| G11 | P2.1 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down pull-up/down resistor. |
| G8 | P2.2 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down pull-up/down resistor. |
| E9 | P2.3 | DIO | 4/8 | I_PD | INPUT/OUTPUT with a selectable pull-up/down resistor. |
| Ground and No Connects | | | | | |
| A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, B2, B3, B4, B5, B6, B7, B8, B9, B10, C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, D2, D3, D4, D5, D6, D7, D8, D9, D11, E1, E2, E3, E4, E5, E6, E7, F1, | GND | GND | | | Analog and digital ground. They are connected on a solid ground plane. |

| Pin No. | Pin name | Type (Table 2) | Drive (mA) | Reset state | Description |
|--|----------|-------------------|---------------|----------------|---|
| F2, F3, F4, F5, F6, F7, G1, G2, G3, G4, G5, G7, H1, H3, J1, J3, J4, L3, M2, N5, N9, N11 | | | | | |
| G9, H7, J6, M4, M10, N10 | NC | NC | | | Not connected. No package ball/pin available on the package. |
| H2, J2, L4 | Keep out | NC | | | Not connected, but package balls/pins are available: implement keep-out on application PCBs to ensure balls/pins are not connected to anything or close to any noise signals. |

Table 2. Pin type definition

| Pin type | Description | Pin type | Description |
|----------|---------------------------------|----------|-------------------------------|
| DI | Digital input | AI | Analog input |
| DO | Digital output | AO | Analog output |
| DIO | Digital input/output | AIO | Analog input/output |
| DIOD | Digital input/output open drain | BP | Back drive protection |
| PU | Pull-up resistor (fixed) | SPU | Switchable pull-up resistor |
| PD | Pull-down resistor (fixed) | SPD | Switchable pull-down resistor |
| PWR | Power | GND | Ground |

4. Characteristics

4.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

| Parameter | Description | Conditions | Min | Max | Unit |
|-----------|---------------------|------------|-----|-----|------|
| VESD | Maximum ESD voltage | HBM | | 2 | kV |
| VBAT | Battery voltage | | | 4.6 | V |
| VBUS | BUS voltage | | | 6.5 | V |

4.2 Recommended Operating Conditions

Table 4. Recommended operating conditions

| Parameter | Description | Conditions | Min | Type | Max | Unit |
|-----------------------|---|---|-----|------|------|------|
| V _{BAT} | Battery supply voltage | Limited by the supply voltage requirements of the SKY77762 power amplifier module from SYKWORKS | 1.9 | | 4.2 | V |
| V _{BUS} | USB voltage | | 4.2 | | 5.75 | V |
| +V _{RF_PA_1} | Bias supply SKY77762 | < 10 mA current draw | 3.0 | | 4.2 | V |
| +V _{RF_PA_2} | Power supply SKY77762 | Up to ~350 mA current draw | 1.9 | 3.3 | 3.6 | V |
| T _A | Ambient operating temperature range | | -20 | | +60 | °C |
| V _{SUPPLY} | Output voltage of DA14495 | | 1.9 | 3.45 | 3.6 | V |
| V _{DCDC} | Output voltage of the DA14495 DCDC converter When the DCDC is disabled, the same pin can be connected to an external supply, overriding the internal DCDC converter. | | 1.4 | | 1.89 | V |

4.3 Electrical Characteristics

Table 5. Digital I/O characteristics

| Parameter | Description | Conditions | Min | Type | Max | Unit |
|----------------------|-------------------------------|--|-------------|-------------|------|------|
| V _{DDIO} | Supply voltage of IO band | | 1.6 | | 3.45 | V |
| V _{PIN_NEG} | Negative voltage on IO pin | | GND - 0.3 | | | V |
| V _{PIN_POS} | Positive voltage on IO pin | | | VDDIO + 0.2 | | V |
| V _{PIN_PON} | Voltage on pin P0.15/PON | | | | 5 | V |
| V _{PIN_USB} | Voltage on pins USBp and USBn | | | | 3.6 | V |
| V _{IH} | High level input voltage | | 0.7 × VDDIO | | | V |
| V _{IL} | Low level input voltage | | | 0.3 × VDDIO | | V |
| V _{DDIO0_2} | IO voltage bank0/2 | | | 1.8 | | V |
| V _{DDIO1} | IO voltage bank 1 | User programmable by connecting the 3V3 (pin K3) or 1V8 (pin H4) from the module to VDDIO1 | | 1.8 3.3 | | V |

Table 6. Radio characteristics

| Parameter | Description | Conditions | Min | Type | Max | Unit |
|------------------------|--|--|-----|------|-----|------|
| F _{operating} | Frequency bands supported | EU-DECT, US-DECT, and J-DECT (K-DECT is not supported) | | | | |
| RX _{sense} | Receiver sensitivity | GFSK, EU-DECT ch5 | | -92 | | dBm |
| P _o | Transmitted output power | GFSK, EU-DECT ch5 | | +22 | | dBm |
| P _{spur} | Spurious emissions | ETSI/FCC compliant | | | | |
| TXACPR1 | Transmitter adjacent channel power ratio M = 1 | P _o = +16 dBm, π/4 DQPSK | | | -33 | dBc |
| TXACPR3 | Transmitter adjacent channel power ratio M = 3 | P _o = +16 dBm, π/4 DQPSK | | | -66 | dBc |
| TXEVM | Transmitter error vector magnitude | P _o = +16 dBm, π/4 DQPSK | | | 6 | % |

Table 7. Supply currents (Tour Guide mode)

| Parameter | Description | Conditions (Note 1) | Min | Type | Max | Unit |
|--------------------------|--|-------------------------------|-----|------|-----|------|
| I _{avg_TG_stby} | Standby supply current (Tour Guide mode) | FP (TX); HPM | | 23 | | mA |
| | | FP (TX); HPM/U | | 20 | | mA |
| | | PP (RX); HPM | | 8 | | mA |
| I _{avg_TG_talk} | Talk mode supply current (Tour Guide mode) | FP (TX); LPM | | 53 | | mA |
| | | FP (TX); HPM | | 71 | | mA |
| | | FP (TX); HPM; Question call | | 91 | | mA |
| | | FP (TX); HPM/U | | 61 | | mA |
| | | FP (TX); HPM/U; Question call | | 76 | | mA |
| | | PP (RX); LPM; RX only | | 31 | | mA |

| Parameter | Description | Conditions (Note 1) | Min | Type | Max | Unit |
|-----------|-------------|--------------------------------|-----|------|-----|------|
| | | PP (RX); LPM; Return channel | | 38 | | mA |
| | | PP (RX); HPM; RX only | | 42 | | mA |
| | | PP (RX); HPM; Return channel | | 49 | | mA |
| | | PP (RX); HPM/U; RX only | | 37 | | mA |
| | | PP (RX); HPM/U; Return channel | | 46 | | mA |

Note 1 VBAT, +VRF_PA_1 and +VRF_PA_2 pins connected to +3.3 V supply; I_{avg} : current drawn from the +3.3 V supply.
Software configuration by default example application. Standby mode: no PP locked to FP.

Table 8. Supply currents (Public Address mode)

| Parameter | Description | Conditions (Note 1) | Min | Type | Max | Unit |
|--------------------------|--|---------------------------|-----|------|-----|------|
| I _{avg_PA_stby} | Standby supply current (Public Address mode) | FP (RX); HPM | | 26 | | mA |
| | | FP (RX); HPM/U | | 20 | | mA |
| | | PP (TX); HPM | | 8 | | mA |
| I _{avg_PA_talk} | Talk mode supply current (Public Address mode) | FP (RX); LPM; 1PP (TX) | | 35 | | mA |
| | | FP (RX); LPM; 2PPs (TX) | | 42 | | mA |
| | | FP (RX); LPM; 3PPs (TX) | | 50 | | mA |
| | | FP (RX); LPM; 4PPs (TX) | | 56 | | mA |
| | | FP (RX); HPM; 1PP (TX) | | 38 | | mA |
| | | FP (RX); HPM; 2PPs (TX) | | 48 | | mA |
| | | FP (RX); HPM; 3PPs (TX) | | 56 | | mA |
| | | FP (RX); HPM; 4PPs (TX) | | 63 | | mA |
| | | FP (RX); HPM/U; 1PP (TX) | | 34 | | mA |
| | | FP (RX); HPM/U; 2PPs (TX) | | 43 | | mA |
| | | FP (RX); HPM/U; 3PPs (TX) | | 51 | | mA |
| | | FP (RX); HPM/U; 4PPs (TX) | | 60 | | mA |
| | | PP (TX); LPM | | 32 | | mA |
| | | PP (TX); HPM | | 44 | | mA |
| | | PP (TX); HPM/U | | 38 | | mA |

Table 9. Supply currents (Voice Conference mode)

| Parameter | Description | Conditions (Note 1) | Min | Type | Max | Unit |
|---------------------------|--|---------------------|-----|------|-----|------|
| I _{avg_CVM_stby} | Standby supply current (Voice Conference mode) | FP; HPM | | 16 | | mA |
| | | PP; HPM | | 8 | | mA |
| I _{avg_CVM_talk} | Talk mode supply current (Voice Conference mode) | FP; HPM; 1PP | | 39 | | mA |
| | | FP; HPM; 2PPs | | 47 | | mA |
| | | FP; HPM; 3PPs | | 58 | | mA |
| | | FP; HPM; 4PPs | | 68 | | mA |
| | | FP; HPM; 5PPs | | 76 | | mA |
| | | FP; HPM; 6PPs | | 86 | | mA |
| | | FP; HPM; 7PPs | | 95 | | mA |
| | | FP; HPM; 8PPs | | 104 | | mA |
| | | FP; HPM/U; 1PP | | 37 | | mA |

| Parameter | Description | Conditions (Note 1) | Min | Type | Max | Unit |
|-----------|-------------|---------------------|-----|------|-----|------|
| | | FP; HPM/U; 2PPs | 45 | | | mA |
| | | FP; HPM/U; 3PPs | 54 | | | mA |
| | | FP; HPM/U; 4PPs | 62 | | | mA |
| | | FP; HPM/U; 5PPs | 69 | | | mA |
| | | FP; HPM/U; 6PPs | 77 | | | mA |
| | | FP; HPM/U; 7PPs | 85 | | | mA |
| | | FP; HPM/U; 8PPs | 91 | | | mA |
| | | PP; HPM | 31 | | | mA |

5. Functional Description

The DA14AVDDECT module is a hardware platform capable of serving multiple functions. The functions fall into two categories, Cordless Voice Module (CVM) and Wireless Audio Module (WAM), and they are defined in the software. These two functions of the DA14AVDDECT are described in their separate CVM and WAM software documents. Consult with your Renesas representative for further details.

Also note that the module is supplied without any software pre-loaded in Flash. See Ref. [3] for programming and configuring the module.

6. Package Information

6.1 Package Outline Drawing

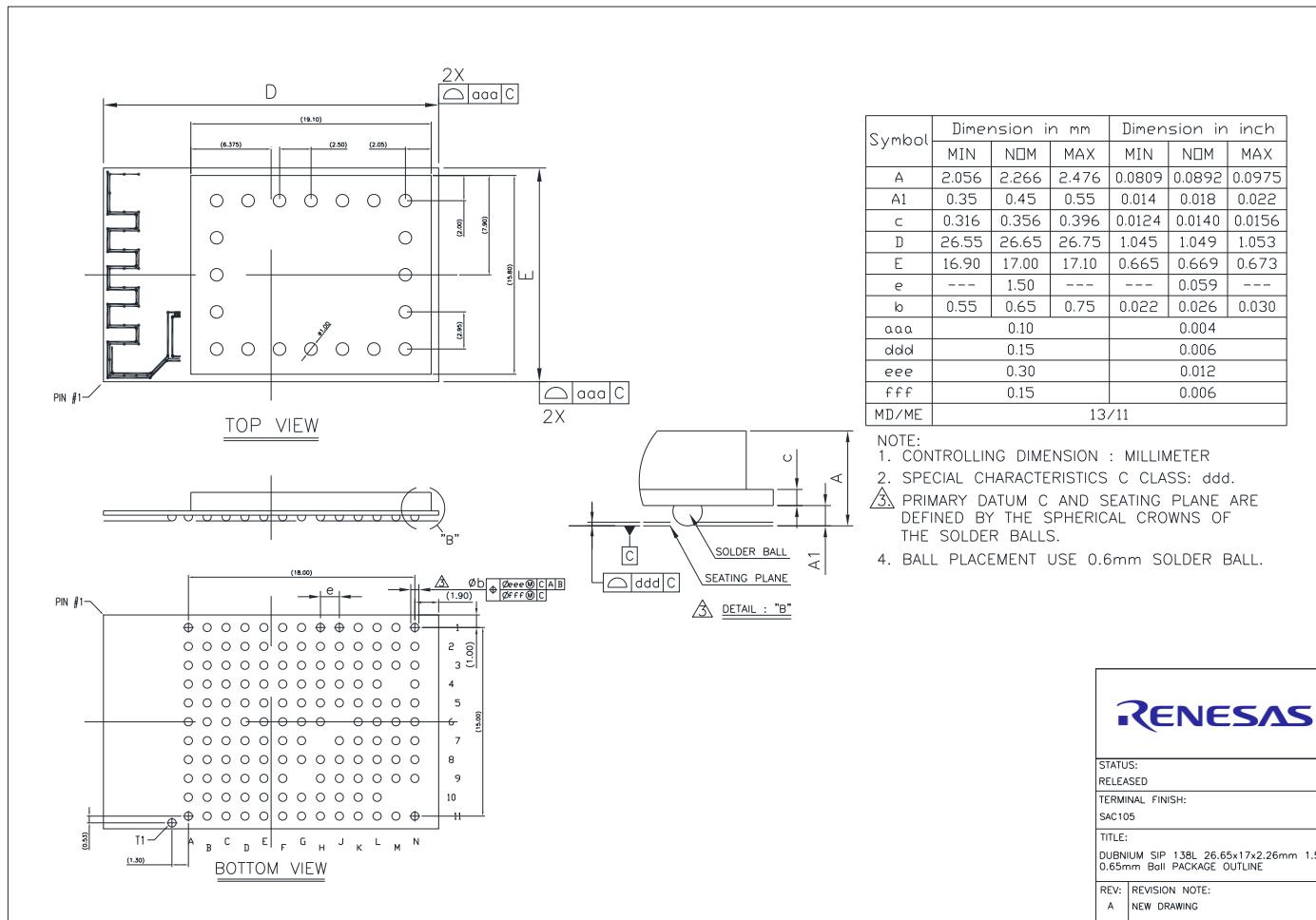


Figure 4. DA14AVDDECT BGA package outline drawing

6.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in [Table 10](#).

For detailed information on MSL levels see the IPC/JEDEC standard J-STD-020, which can be downloaded from <http://www.jedec.org>.

The DA14AVDDECT is qualified for MSL 3.

Table 10. MSL classification

| MSL level | Floor lifetime | Conditions |
|-----------|----------------|----------------|
| MSL 4 | 72 hours | 30 °C / 60% RH |
| MSL 3 | 168 hours | 30 °C / 60% RH |
| MSL 2A | 4 weeks | 30 °C / 60% RH |
| MSL 2 | 1 year | 30 °C / 60% RH |
| MSL 1 | Unlimited | 30 °C / 85% RH |

6.3 Soldering Information

The DA14AVDDECT should be soldered using a lead-free reflow soldering profile as shown in [Figure 5](#). Adjustments to the profile may be necessary, depending on process requirements.

The recommended solder paste for lead-free soldering is Sn 96.5%, Ag 3.0%, and Cu 0.5%.

Temperature

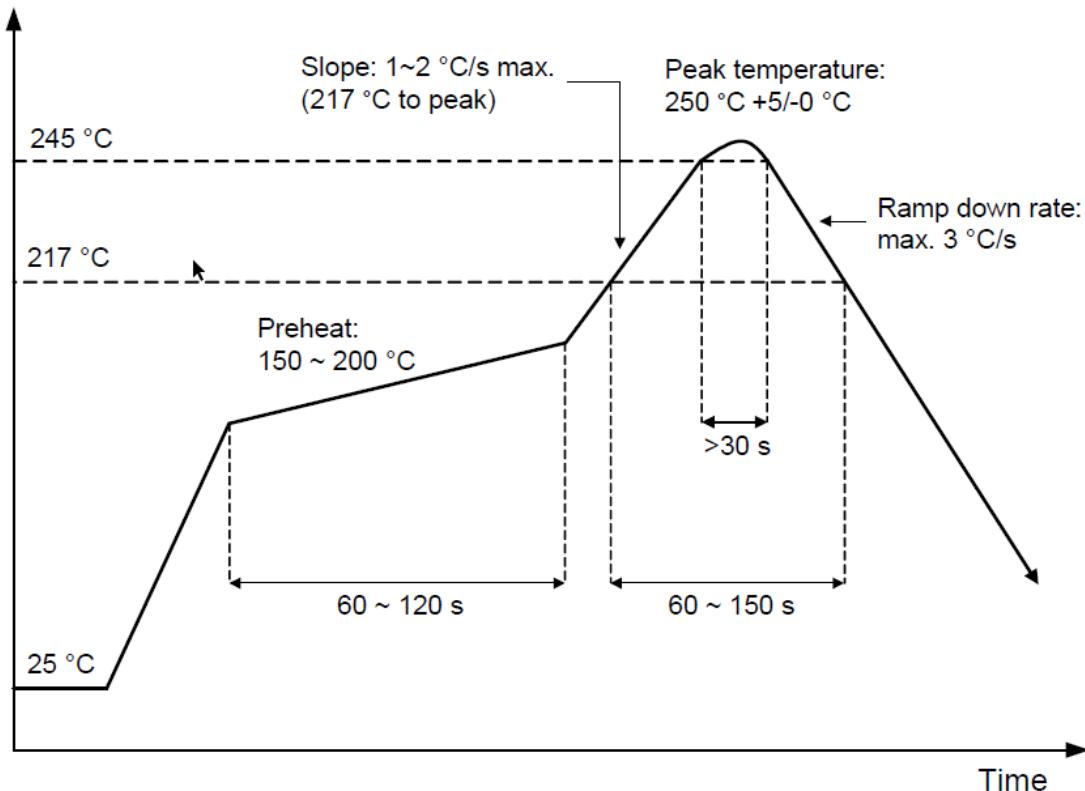


Figure 5. Reflow profile (lead-free)

6.4 Packaging

The DA14AVDDECT is packaged in trays.

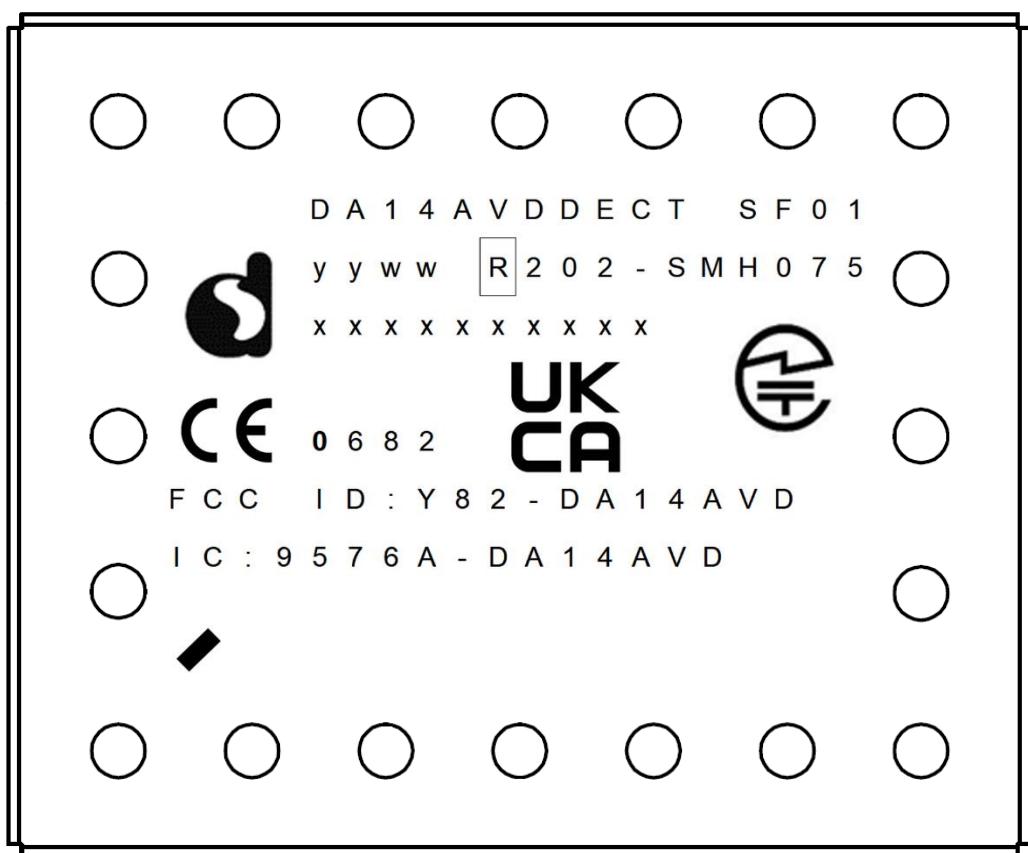


Figure 6. DA14AVDDECT package marking

Table 11. DA14AVDDECT package marking table

| Row/Column | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | | | | | | | | | | | |
|------------|------------------------------|---|---|--------------------------|---|----------------------|---|-----------|---|----|----|------------|----|----|----|----|----|----|----|----|--|--|--|--|--|--|--|--|--|--|--|
| 1. | | | | Manufacturer Part Number | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2. | Dialog Logo | | | Date Code | | TELEC License Number | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3. | | | | Assembly Lot Number | | | | | | | | TELEC mark | | | | | | | | | | | | | | | | | | | |
| 4. | CE mark | | | | | | | UKCA mark | | | | | | | | | | | | | | | | | | | | | | | |
| 5. | | | | Qualification Code | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6. | RF License (FCC) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7. | RF License (Industry Canada) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8. | Pin1 Orientation | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

7. Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, consult your Renesas [local sales representative](#).

Table 12. Ordering information

| Part number | Package | Size module (mm) | Shipment form |
|------------------|------------|--------------------|---------------|
| DA14AVDDECT SF01 | PCB Module | 17.0 mm × 26.65 mm | Tray |

8. Application Information

As mentioned in Section 5, the DA14AVDDECT functionality is defined in software and the software specifics are detailed in separate documents. The DA14AVDDECT can be operated stand-alone or controlled from a host application through the API interface. The on-board Flash memory can be used to store the custom code.

The following points highlight some hardware-specific aspects of application implementation:

- Antennas:
 - The module includes an integrated printed antenna (ANT2).
 - Optionally, an additional external antenna (ANT1) can be connected to support antenna diversity.
 - For an optimal wireless performance, it is recommended to always use two antennas, that is, the internal antenna combined with an external antenna.
 - A special build option may be ordered with a special ordering code that disconnects ANT2 from the internal printed antenna and allows two external antennas to be used.
- Supply voltage of RFPA:
 - +VRF_PA_1 and +VRF_PA_2 need to be connected to external supply voltages.
 - To be able to leverage the Limited Modular Approval certification (for more information see Ref. [4]), the supply circuit should be copied from the reference application used for certification. If it is desired to deviate from the reference application, note the following, and it may not be possible to leverage the Limited Modular Approval any more:
 - +VRF_PA_1 requires a minimum input voltage of 3.0 V (current draw 10 mA), so an external DCDC boost converter is required if two AA applications are targeted.
 - Typically, +VRF_PA_2 is connected to an external 3.3 V supply voltage (up to 350 mA current draw depending on the RF TX output power levels). An optimal battery efficiency is obtained if +VRF_PA_2 is sourced from a DCDC power supply adjusted within 0.5 V to 3.5 V based on the target output power levels.
- The DA14AVDDECT module includes an integrated battery charger and the associated power dissipation increases the module's temperature. Make sure that the chip temperature does not exceed its operational temperature range, especially when other functions are also enabled. Since the module includes an on-board temperature sensor to facilitate chip temperature detection, how to protect the chip from overheating needs to be implemented in software and is not described in further detail in this document.
- The DA14AVDDECT module includes an integrated audio CODEC. To support an external audio CODEC, map the GPIOs accordingly. It is implemented in software and is not described in further detail in this document.
- An external protection IC may be required to protect VBUS from supply circuits with possible high overshoot.

8.1 Audio Connections

Analog microphones can be connected as shown in [Figure 7](#).

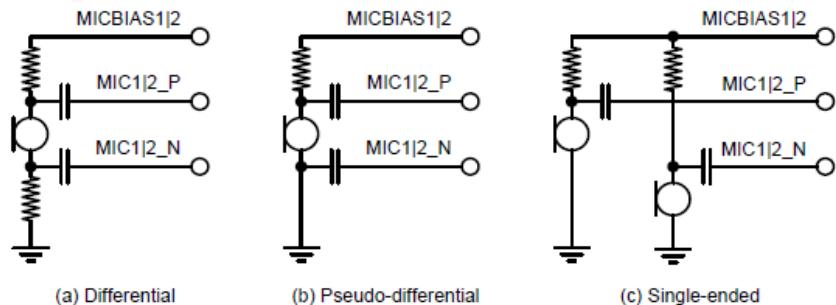


Figure 7. Connection of analog microphones

The bias resistor value shall be selected depending on the microphone requirements and MICBIAS1/2 must be decoupled with 1 μ F capacitors.

The DA14AVDDECT module can support headphone detection. Document UM-D-012 (Ref. [\[7\]](#)) explains how to control this feature in the software. Contact your Renesas representative for further details.

9. Layout Guidelines

The module pinout of DA14AVDDECT has been specifically designed to accommodate easy integration with the PCBs of customer applications without having to add expensive PCB components to increase the cost due to, for example, blind vias or small line/space dimensions.

All standard practice layout rules and guidelines apply. Additional special care may be paid to the antenna and USB areas:

- The application PCB may not extend underneath the antenna area (see [Figure 8](#)).
- Signals from the application PCB containing high harmonic content (for example, clock signals or memory buses) must be kept away from the antenna.
- No metal objects should be placed in the vicinity of the antenna (see [Figure 8](#)).
- The USB data lines should be routed with $90\ \Omega$ differential impedance lines and the line lengths must match.
- Appropriate trace width and number of vias should be used for all power supply paths.
- A common ground plane should be used to allow proper electrical and thermal performances.
- Noise-sensitive analog signals, such as feedback lines or clock connections, should be kept away from the traces carrying pulsed analog or digital signals. This can be achieved by separation (distance) or by shielding the sensitive signals with quiet signals or ground traces.
- Decoupling capacitors should be X5R ceramics and should be placed as near to the module as possible.

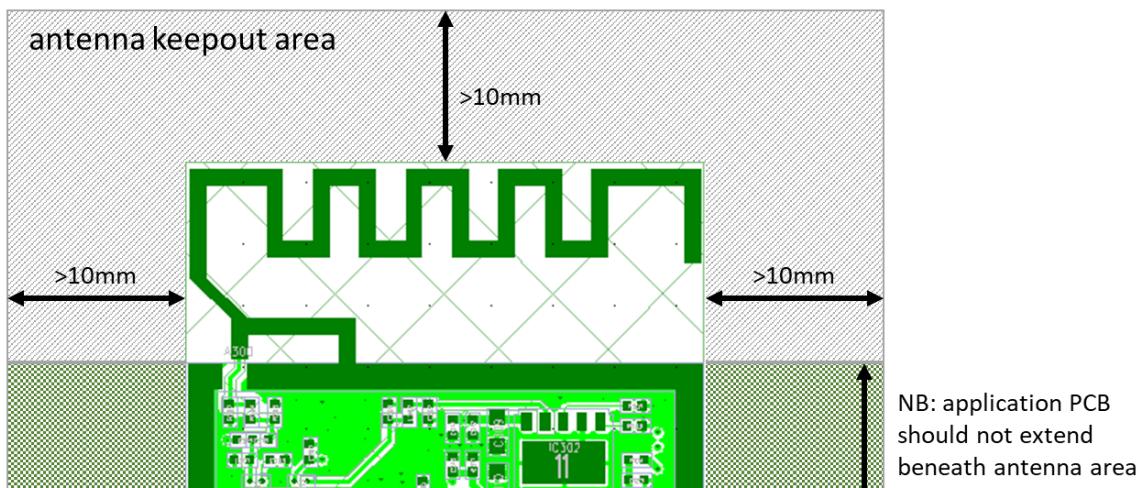


Figure 8. Keep-out areas

It is also advised to use the hardware layout of the DA14AVDDECT evaluation kit as a guideline for customer products. This hardware was used during the certification process and should be regarded as a reference.

See Ref. [\[4\]](#) for more information on the Limited Modular Approval certification and how it can be used, so that no new radio certification needs to be obtained for the end customer products.

Revision History

| Revision | Date | Description |
|----------|---------------|---|
| 3.0 | Nov 27, 2024 | Updated Table 1, Table 6, Section 8.1 |
| 2.4 | Oct 27, 2022 | TW editorial plus subject matter review |
| 2.3 | Dec 31, 2021 | Updated logo, disclaimer, copyright |
| 2.2 | July 30, 2021 | Updated information on antennas in Section 8 |
| 2.1 | June 2, 2020 | Added supply current tables |
| 2.0 | May 14, 2020 | Preliminary datasheet |
| 1.9 | Sept 18, 2019 | Added 'P2.5' to I2C-DATA pin name |
| 1.8 | Sept 9, 2019 | Added reflow profile Changed pin name I2C-DATA Revised H2/J2 in figure 3 to correspond with table 1 Updated figure 9 to the latest EVK schematic snapshot |
| 1.7 | Aug 13, 2019 | Added text at LMA section Corrected pin L4 in the pin diagram (1.6 was erroneously reverted to GND), also corrected some pin naming typos Added wording about SW supporting only mono whereas the HW supports stereo |
| 1.6 | Aug 8, 2019 | Updated pin diagram and table (E11 = Vsupply and others) Corrected B1 and D1 pin descriptions |
| 1.5 | June 6, 2019 | Changed pin L4 to NC, added comment about pin T1 |
| 1.4 | Mar 19, 2019 | Updated POD |
| 1.3 | Mar 7, 2019 | Added keepout area drawing in ch9, changed pins H2, J2 to NC |
| 1.2 | Feb 20, 2019 | Updated package outline drawing; minor cosmetic edits |
| 1.1 | Nov 26, 2018 | Added package outline drawing |
| 1.0 | Oct 31, 2018 | First version of target datasheet |

Status Definitions

| Revision | Datasheet Status | Product Status | Definition |
|----------|------------------|----------------|--|
| 1.<n> | Target | Development | This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice. |
| 2.<n> | Preliminary | Qualification | This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design. |
| 3.<n> | Final | Production | This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com . |

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us

© 2024 Renesas Electronics Corporation. All rights reserved.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.