DA16200MOD

Ultra-Low Power Wi-Fi SoC Module

General Description

The DA16200MOD is a fully integrated Wi-Fi® module with ultra-low power consumption, best RF performance and easy development environment. Such low power operation can extend the battery life as long as a year or more depending on the application.

This module series included DA16200-00000A32, 40 MHz crystal oscillator, 32.768 kHz RTC clock, Lumped RF filter, 4-MB flash memory and chip antenna or u.FL connector. The DA16200MOD has chip antenna type (DA16200MOD-AAC4WA32) and u.FL connector type (DA16200MOD-AAE4WA32) for external antenna.

The Module is built from the ground up for the Internet of Things (IoT) and is ideal for door locks, thermostats, sensors, pet trackers, asset trackers, sprinkler systems, connected lighting, video cameras, video doorbells, wearables, and other IoT devices.

The modules certified Wi-Fi Alliance for IEEE802.11b/g/n, WPS functionalities and it has been approved by many countries including the United States (FCC), Canada (IC), and China (SRRC). Using the Wi-Fi Alliance transfer policy, the Wi-Fi Certifications can be transferred without being tested again. For more information on DA16200MOD, see DA16200-00000A32 datasheet.

Key Features

- Module variants
  - DA16200MOD-AAC4WA32 (chip antenna)
  - DA16200MOD-AAE4WA32 (u.FL connector)
- Highly integrated ultra-low power Wi-Fi system module
  - Sleep current: 3.5 µA, VBAT = 3.3 V
- Best RF performance
  - TX Power: +19 dBm, 1 Mbps DSSS
  - RX Sensitivity: -98.5 dBm, 1 Mbps DSSS
- Full offload: SoC runs full networking OS and TCP/IP stack
- Wi-Fi processor
  - IEEE 802.11b/g/n, 1x1, 20 MHz channel bandwidth, 2.4 GHz
  - Wi-Fi security: WPA/WPA2-Enterprise/Personal, WPA2 SI, WPA3 SAE, and OWE
  - Vendor EAP types: EAP-TTLS/MSCHAPv2, PEAPv0/EAP-MSCHAPv2, PEAPv1, EAP-FAST, and EAP-TLS
  - Operating modes: Station and Soft AP
  - WPS-PIN/PBC for easy Wi-Fi provisioning
  - Connection manager for autonomous and fast Wi-Fi connections
  - Bluetooth® coexistence
  - Antenna switching diversity
- Hardware accelerators
  - General Hardware CRC engine
- Built-in 4-channel auxiliary ADC for sensor interfaces
  - 12-bit SAR ADC: Single-ended four channels
  - Provide dynamic auto switching function
- Support various interfaces
  - eMMC/SD expanded memory
  - SDIO Host/Slave function
  - QSPI for external flash control
  - Three UARTs
  - SPI Master/Slave interface
  - I2C Master/Slave interface
  - I2S for digital audio streaming
  - 4-channel PWM
  - Individually programmable, multiplexed GPIO pins
  - JTAG and SWD
- Wi-Fi alliance certifications:
  - Wi-Fi CERTIFIED™ b/g/n
  - WPA™ - Enterprise, Personal
  - WPA2™ - Enterprise, Personal
  - WPA3™ - Enterprise, Personal
- RF regulatory certifications
  - FCC, IC, CE, KC, TELEC, SRRC, ANATEL
- CPU core subsystem
  - Arm® Cortex®-M4F core w/clock frequency of 30~160 MHz
  - ROM: 256 kB, SRAM: 512 kB, OTP: 8 kB, Retention Memory: 48 kB

  - Hardware zeroing function for fast booting
  - Pseudo random number generator (PRNG)
- Complete software stack
  - Comprehensive networking software stack
  - Provide TCP/IP stack in the form of network socket APIs
- Advanced security
  - Secure booting
  - Secure debugging using JTAG/SWD and UART ports
  - Secure asset storage
- Built-in hardware crypto engines for advanced security
  - TLS/DTLS security protocol functions
  - Crypto engine for key deliberate generic security functions: AES (128, 192, 256), DES/3DES, SHA1/224/256, RSA, DH, ECC, CHACHA, and TRNG
- Power management unit
  - On-Chip RTC
  - Wake-up control of fast booting or full booting with minimal initialization time
  - Support three ultra-low power sleep modes
- SPI flash memory
  - 32-Mbit/4-MB
- External clock source
  - 40 MHz crystal (± 25 ppm) for master clock (initial + temp + aging)
  - 32.768 kHz crystal (± 250 ppm) for RTC clock
- Supply
  - Operating voltage: 2.1 V to 3.6 V (typical: 3.3 V)
  - 2 Digital I/O Supply Voltage: 1.8 V/3.3 V
  - Blackout and brownout detector
- Module dimensions
  - 13.8 mm × 22.1 mm x 3.3 mm, 37 Pins
- Operating temperature range
  - -40 °C to 85 °C

Contents

Figures

Tables

1. Terms and Definitions

API	Application Programming Interface
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IoT	Internet of Things
JTAG	Joint Test Action Group
LDO	Low-dropout Regulator
PLL	Phase-locked Loop
PRNG	Pseudo Random Number Generator
PWM	Pulse Width Modulation
QSPI	Quad-lane SPI
RTC	Real-time Clock
SAR ADC	Successive Approximation Analog-to-Digital Converter
SMD	Surface Mounted Device
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
UART	Universal Asynchronous Receivers and Transmitter

2. References

[1] DA16200, Datasheet, Renesas Electronics.

[2] Arm Cortex M4 Processor Technical Reference Manual.

[3] ITU-T O.150, General Requirements for Instrumentation for Performance Measurements on Digital Transmission Equipment, 1996.

[4] Arm® TrustZone® CryptoCell-312, Revision r1p1, Software Integrators Manual.

[5] IEEE Standard 1149.1, Test Access Port and Boundary-Scan Architecture.

[6] AMBA AHB Bus Specification, Revision 3.0.
(https://developer.arm.com/documentation/ihi0033/bb)

Note 1 References are for the latest published version, unless otherwise indicated.

3. Block Diagram

Figure 1 shows the DA16200MOD hardware block diagram.

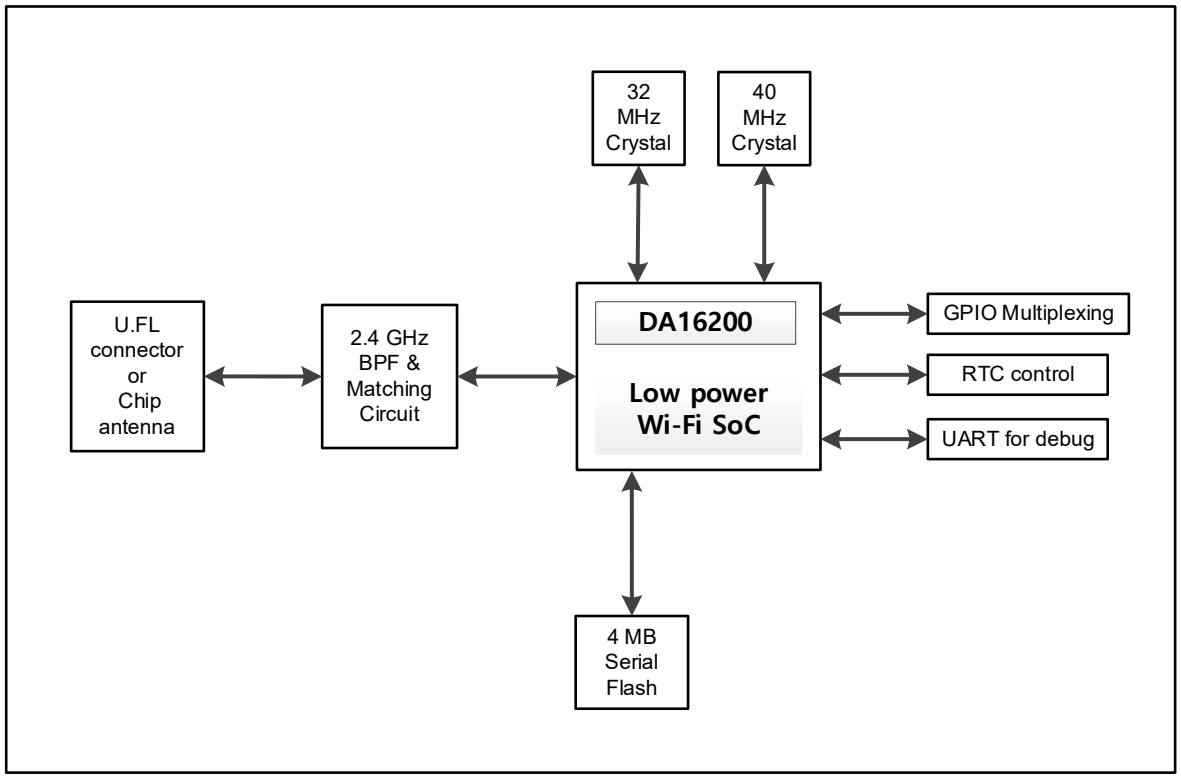


Figure 1. DA16200MOD block diagram

4. Pinout

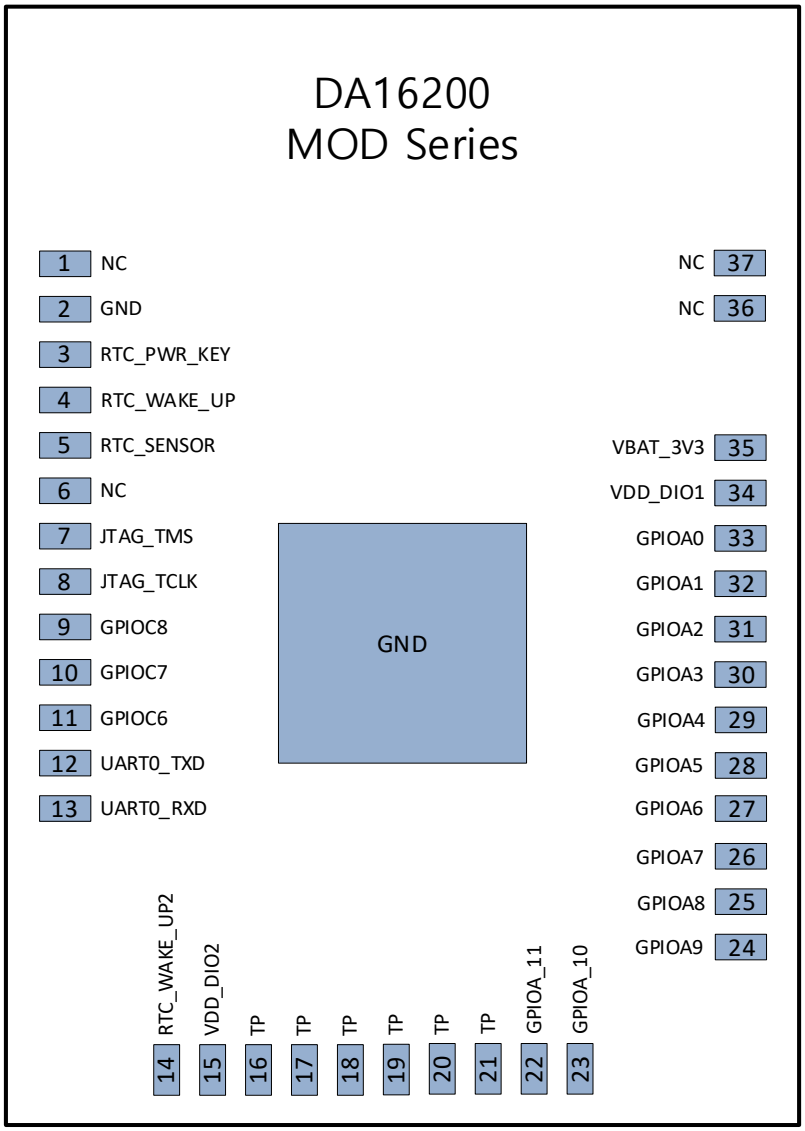


Figure 2. DA16200MOD 37 pinout diagram (top view)

Table 1. Pin description

#Pin	Pin name	Type	Drive (mA)	Reset state	Description
1	NC	NC			Not connected
2	GND	GND			RF VDD
3	RTC_PWR_KEY	DI			RTC block enable signal
4	RTC_WAKE_UP	DI			RTC block wake-up signal
5	RTC_SENSOR	DO			Sensor control signal
6	NC	NC			Not connected
7	JTAG_TMS	DIO	2/4/8/12	I-PU	JTAG I/F, SWDIO
8	JTAG_TCLK	DIO	2/4/8/12	I-PD	JTAG I/F, SWCLK, General Purpose I/O
9	GPIOC8	DIO	2/4/8/12	I-PD	General Purpose I/O
10	GPIOC7	DIO	2/4/8/12	I-PD	General Purpose I/O
11	GPIOC6	DIO	2/4/8/12	I-PD	General Purpose I/O

#Pin	Pin name	Type	Drive (mA)	Reset state	Description
12	UART_TXD	DO	2/4/8/12	O	UART transmit data
13	UART_RXD	DI	2/4/8/12	I	UART receive data
14	RTC_WAKE_UP2	DI			RTC block wake-up signal
15	VDD_DIO2	VDD			Supply power for digital I/O GPIOC6~GPIOC8, TMS/TCLK, TXD/RXD
16	F_CSN	NC			Flash Memory I/F Available as a test point only, W25Q32JW is connected to DA16200 Internally
17	F_IO1	NC			Flash Memory I/F (F_SI) Available as a test point only, W25QJ32W is connected to DA16200 Internally
18	F_IO2	NC			Flash Memory I/F (F_WP) Available as a test point only, W25QJ32W is connected to DA16200 Internally
19	F_IO0	NC			Flash Memory I/F (F_SO) Available as a test point only, W25QJ32W is connected to DA16200 Internally
20	F_IO3	NC			Flash Memory I/F (F_HOLD) Available as a test point only, W25QJ32W is connected to DA16200 Internally
21	F_CLK	NC			External Flash Memory I/F Available as a test point only, W25QJ32W is connected to DA16200 Internally
22	GPIOA11	DIO	2/4/8/12	I-PD	General Purpose I/O
23	GPIOA10	DIO	2/4/8/12	I-PD	General Purpose I/O
24	GPIOA9	DIO	2/4/8/12	I-PD	General Purpose I/O
25	GPIOA8	DIO	2/4/8/12	I-PD	General Purpose I/O
26	GPIOA7	DIO	2/4/8/12	I-PD	General Purpose I/O
27	GPIOA6	DIO	2/4/8/12	I-PD	General Purpose I/O
28	GPIOA5	DIO	2/4/8/12	I-PD	General Purpose I/O
29	GPIOA4	DIO	2/4/8/12	I-PD	General Purpose I/O
30	GPIOA3	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
31	GPIOA2	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
32	GPIOA1	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
33	GPIOA0	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
34	VDD_DIO1	VDD			Supply power for digital I/O
35	VBAT_3V3	VDD			Supply power for integrated power amplifier
36	NC	NC			Not connected
37	NC	NC			Not connected

NOTE

All GPIOs functionality can be referred to the DA16200 datasheets. See Ref. [1].

5. Electrical Specification

5.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Parameter	Pins	Min	Max	Unit
VBAT_3V3	35	-0.2	3.7	V
VDD_DIO1	34	-0.2	3.7	V
VDD_DIO2	15	-0.2	3.7	V
Operating temperature range (TA)		-40	+85	°C
Storage temperature range		-40	+125	°C

5.2 Recommended Operating Conditions

Table 3. Recommended operating conditions

Parameter	Pins	Min	Typ	Max	Unit
VBAT_3V3	35	2.1		3.6	V
VDD_DIO1	34	1.62		3.6	V
VDD_DIO2	15	1.62		3.6	V
Operating temperature range (TA)		-40		+85	°C

5.3 Electrical Characteristics

5.3.1 DC Parameters, 1.8 V IO

Table 4. DC parameters, 1.8 V IO

Parameter	Description	Conditions	Min	Max	Unit
V_{IL}	Input Low Voltage	Guaranteed logic Low level (Note 1)	VSS	0.3 × DVDD	V
V_{IH}	Input High Voltage	Guaranteed logic High level	0.7 × DVDD	DVDD	V
V_{OL}	Output Low Voltage	DVDD = Min	VSS	0.2 × DVDD	V
V_{OH}	Output High Voltage	DVDD = Min	0.8 × DVDD	DVDD	V
R_{PU}	Pull-up Resistor	V_{PAD} = V_{IH}, DIO = Min		32.4	kΩ
R_{PD}	Pull-down Resistor	V_{PAD} = VIL, DIO = Min		32.4	

Note 1 DVDD = 1.8 V, VDD_DIO1, VDD_DIO2 Logic Level.

5.3.2 DC Parameters, 3.3 V IO

Table 5. DC parameters, 3.3 V IO

Parameter	Description	Conditions	Min	Max	Unit
V_{IL}	Input Low Voltage	Guaranteed logic Low level	VSS	0.8	V

Parameter	Description	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage	Guaranteed logic High level	2.0	DVDD	V
V_{OL}	Output Low Voltage	DVDD = Min	VSS	0.4	V
V_{OH}	Output High Voltage	DVDD = Min	2.4	DVDD	V
R_{PU}	Pull-up Resistor	VPAD = VIH, DIO = Min		19.4	kΩ
R_{PD}	Pull-down Resistor	V_{PAD} = V_{IL}, DIO = Min		16.0	

Note 1 DVDD = 3.3 V, VDD_DIO1, VDD_DIO2 Logic Level.

5.3.3 DC Parameters for RTC Block

There are several control pins in RTC block, see Ref. [1] for details.

Table 6. DC parameters for RTC block, 3.3 V VBAT

Parameter	Description	Conditions	Min	Max	Unit
V_{IL}	Input Low Voltage	Guaranteed logic Low level	VSS	0.6	V
V_{IH}	Input High Voltage	Guaranteed logic High level	2.2	VBAT	V

Note 1 (RTC block: RTC_PWR_KEY, RTC_WAKE_UP, RTC_WAKE_UP2)

Table 7. DC parameters for RTC block, 2.1 V VBAT

Parameter	Description	Conditions	Min	Max	Unit
V_{IL}	Input Low Voltage	Guaranteed logic Low level	VSS	0.3	V
V_{IH}	Input High Voltage	Guaranteed logic High level	1.6	VBAT	V

5.3.4 DC Parameters for Digital Wake-up

Several GPIOs can be used for wake-up, see Ref. [1] for details. To use Digital Wake-up, IO voltage should not be over VBAT.

Table 8. DC parameters for digital wake-up, 3.3 V VBAT and 1.8/3.3 V IO

Parameter	Description	Conditions	Min	Max	Unit
V_{IL}	Input Low Voltage	Guaranteed logic Low level	VSS	0.5	V
V_{IH}	Input High Voltage	Guaranteed logic High level	1.4	DVDD	V

Note 1 (DVDD = 1.8/3.3 V, VDD_DIO1, VDD_DIO2 Logic Level, DVDD should not be over VBAT).

Table 9. DC parameters for digital wake-up, 2.1 V VBAT and 1.8 V IO

Parameter	Description	Conditions	Min	Max	Unit
V_{IL}	Input Low Voltage	Guaranteed logic Low level	VSS	0.3	V
V_{IH}	Input High Voltage	Guaranteed logic High level	1.3	DVDD	V

Note 1 (DVDD = 1.8 V, VDD_DIO1, VDD_DIO2 Logic Level, DVDD should not be over VBAT).

5.4 Radio Characteristics

5.4.1 WLAN Receiver Characteristics

TA = +25 °C, VBAT = 3.3 V, CH1 (2412 MHz).

Table 10. WLAN receiver characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates)	1 Mbps DSSS	-99.5	-98.5	-96.5	dBm
	2 Mbps DSSS	-95	-94	-92	
	11 Mbps CCK	-90	-89	-87	
	6 Mbps OFDM	-91	-90	-88	
	9 Mbps OFDM	-91	-90	-88	
	18 Mbps OFDM	-89	-88	-86	
	36 Mbps OFDM	-82	-81	-79	
	54 Mbps OFDM	-76	-75	-73	
	MCS0(GF)	-91	-90	-88	
	MCS7(GF)	-73	-72	-70	
Maximum input level (8% PER for 11b rates, 10% PER for 11g/11n rates)	802.11b	-4	0	0	
	802.11g	-10	-4	-3	

5.4.2 WLAN Transceiver Characteristics

TA = +25 °C, VBAT = 3.3 V, CH1 (2412 MHz).

Table 11. WLAN transmitter characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Maximum Output Power measured form IEEE spectral mask and EVM	1 Mbps DSSS	16.5	19.0	20	dBm
	2 Mbps DSSS	16.5	19.0	20	
	5.5 Mbps CCK	16.5	19.0	20	
	11 Mbps CCK	16.5	19.0	20	
	6 Mbps OFDM	15.5	18.0	19	
	9 Mbps OFDM	15.5	18.0	19	
	12 Mbps OFDM	15.5	18.0	19	
	18 Mbps OFDM	15.5	18.0	19	
	24 Mbps OFDM	14.5	17.0	18	
	36 Mbps OFDM	14.5	17.0	18	
	48 Mbps OFDM	13	15.5	16.5	
	54 Mbps OFDM	12	14.5	15.5	
	MCS0 OFDM	15.5	18.0	19	
	MCS7 OFDM	12	14.5	15.5	
Transmit center frequency accuracy	-	-25		+25	ppm

5.5 Current Consumption

TA = +25 °C, VBAT = 3.3 V, w/ CPU clock is 80 MHz.

Table 12. Current consumption in Active state

Parameter	Conditions			Min	Typ	Max	Unit
ACTIVE	TX	1 Mbps DSSS	@ 19.0 dBm	260	280	320	mA

Parameter	Conditions			Min	Typ	Max	Unit
		6 Mbps OFDM	@ 18.0 dBm	240	260	300	
		54 Mbps OFDM	@ 14.5 dBm	180	200	240	
		MCS7	@ 14.5 dBm	180	200	240	
	RX	No signal (Note 1)		25	29	51	
		1 Mbps DSSS (Note 1)		26.5	30.5	53	
		1 Mbps DSSS		27	37.5	54	
		54 Mbps OFDM		29	38.5	54	
		MCS7		29	38.5	54	

Note 1 Low Power Mode and CPU clock 30 MHz.

TA = +25 °C, VBAT = 3.3 V

Table 13. Current consumption in low power operation

Parameter	Conditions	Min	Typ	Max	Unit
Low Power Operation	Sleep 1	-	0.2	-	µA
	Sleep 2	-	1.8	-	
	Sleep 3	-	3.5	-	

5.6 Radiation Performance

The antenna radiation pattern measurements are carried out in an anechoic chamber. Radiation patterns are presented for three measurement planes: XY-, XZ-, and YZ- planes with horizontal and vertical polarization of the receiving antenna.

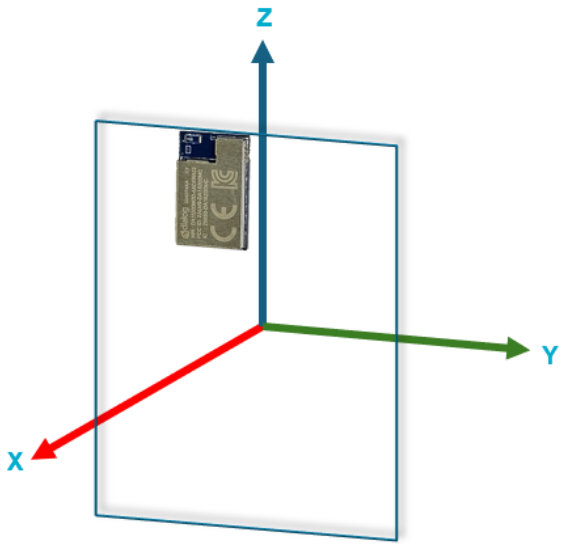


Figure 3: Measurement plane definition

Measurements are carried out for the module installed in the upper left corner on the reference evaluation board.

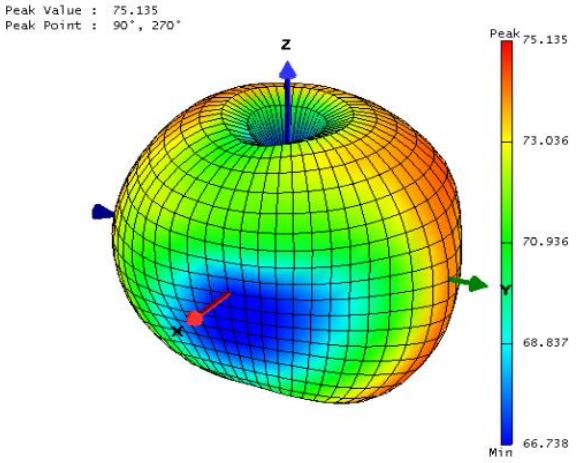


Figure 4. TIS 3D

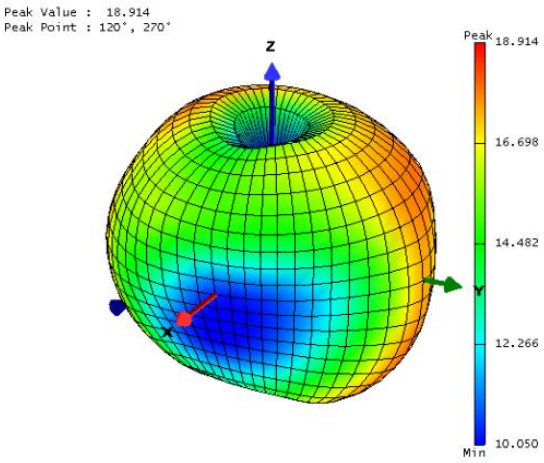


Figure 5. TRP 3D

5.7 ESD Ratings

Table 14. ESD performance

Reliability test	Standards	Test conditions	Result
Human Body Model (HBM)	ANSI/ESDA/JEDEC JS-001-2017	± 2,000 V	Pass
Charge Device Mode (CDM)	ANSI/ESDA/JEDEC JS-002-2018	± 500 V	Pass

5.8 Clock Electrical Characteristics

DA16200MOD has two clock sources, one is the 32.768 kHz clock used by the RTC block, and the other is the 40 MHz clock for the internal processor and Wi-Fi system. More specifically, the 40-MHz clock is used as a source clock for the internal PLL while the PLL output is used for the internal processor and Wi-Fi system block.

5.8.1 RTC Clock Source

The 32.768 kHz RTC clock source is necessary for the free-running counter in the RTC block. The RTC block of the SoC contains an internal 32.768 kHz RC oscillator as well, which is used as a clock for chip initialization before the external 32.768 kHz crystal reaches the stable time in the initial stage. It is necessary to convert it into an external clock for accurate clock counting after the initialization stage. This process is executed through the register setting.

5.8.2 Main Clock Source

DA16200MOD contains a crystal oscillator for the main clock source which supports the external crystal clock. Basically, the external clock is 40 MHz.

6. Power-on Sequence

The sequence after the initial switching from power-off to power-on is shown in Figure 6. The RTC_PWR_KEY of DA16200 is a pin that enables the RTC block. When RTC_PWR_KEY is enabled after VBAT power is supplied, all the internal regulators are switched on automatically in the sequence pre-defined by the RTC block.

When RTC_PWR_KEY is switched on, LDOs for both XTAL and digital I/O are switched on shortly and then the DCDC regulator is switched on according to the pre-defined interval. The enabling intervals can also be modified in the register settings after initial power-up.

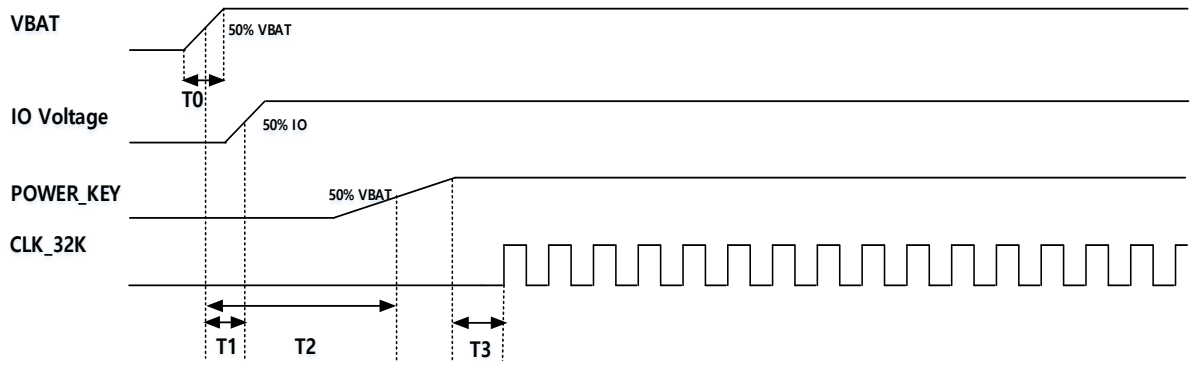


Figure 6. Power-on sequence

Table 15. Power-on sequence timing requirements

Name	Description	Min	Typ	Max	Unit
T0	VBAT power-on time from 10% to 90 % of VBAT	-		-	ms
T1	IO voltage and VCC supply	-	0	-	ms
T2	RTC_PWR_KEY switch-on time from 50% VBAT to 50% POWER_KEY * (Note 1)	-	5*T0	-	ms
T3	Internal RC oscillator wake-up time	-	217	-	µs

Note 1 If the T0 = 10 ms to switch on VBAT, the recommended T2 is 50 ms for the safe booting operation. It can be externally controlled by MCU, or it can be implemented using the RC filter at the input of RTC_PWR_KEY. The recommended C value is 470 nF or 1 µF (not to exceed 1 µF) and R value is chosen to have T2 delay. For example, R and C values will be 82 kΩ and 1 µF when T0 = 10 ms.

7. Application Schematic

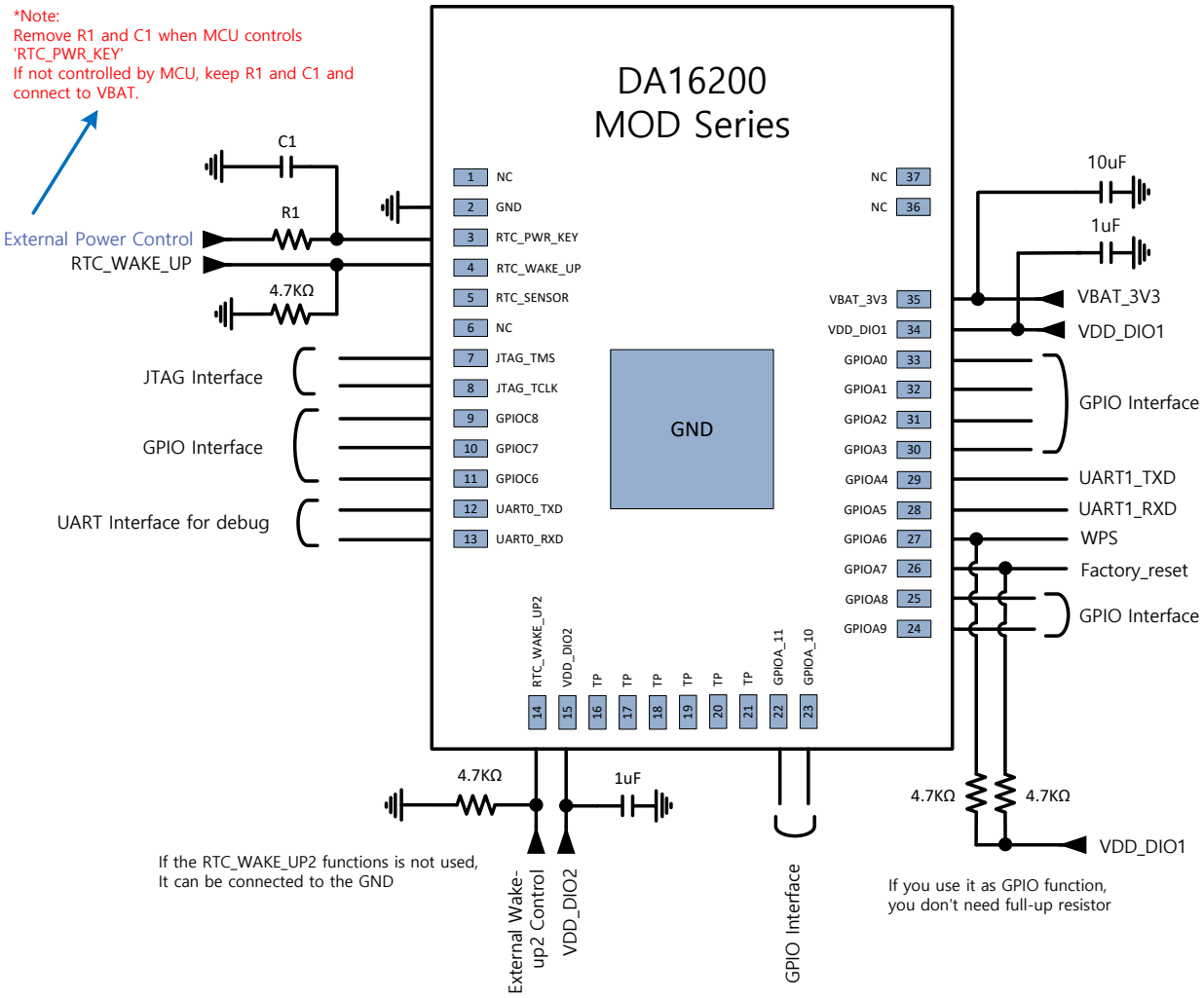


Figure 7. Application schematic

Table 16. Component for RTC power key

Quantity	Part Reference	Value	Description
1	R1	470 kΩ	Remove when MCU control "RTC_PWR_KEY". This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT.
1	C1	1 µF	Remove when MCU control "RTC_PWR_KEY". This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. Not to exceed 1 µF.

8. Mechanical Specifications

8.1 Dimension: DA16200MOD-AAC

Unit: millimeter (mm)

Tolerance: 13.8 (±0.2) x 22.1 (±0.2) x 3.3 (±0.1)

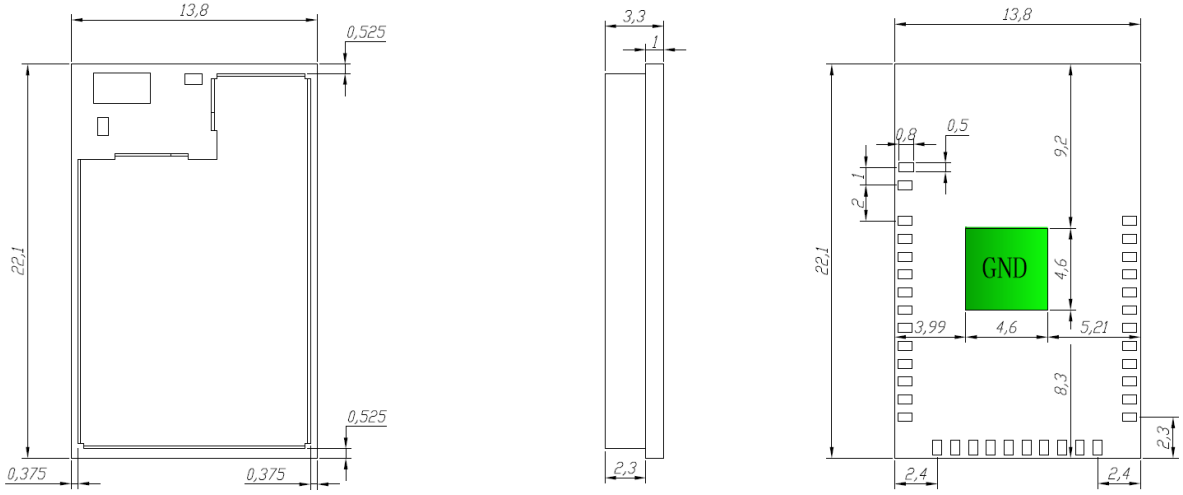


Figure 8. AAC module dimension

8.2 Dimension: DA16200MOD-AAE

Unit: millimeter (mm)

Tolerance: 13.8 (±0.2) x 22.1 (±0.2) x 3.3 (±0.1)

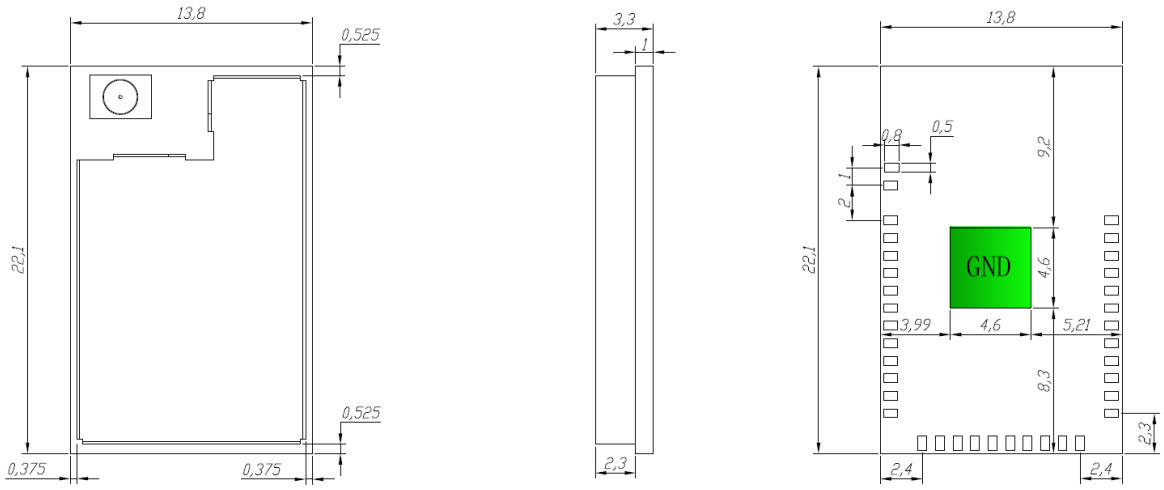
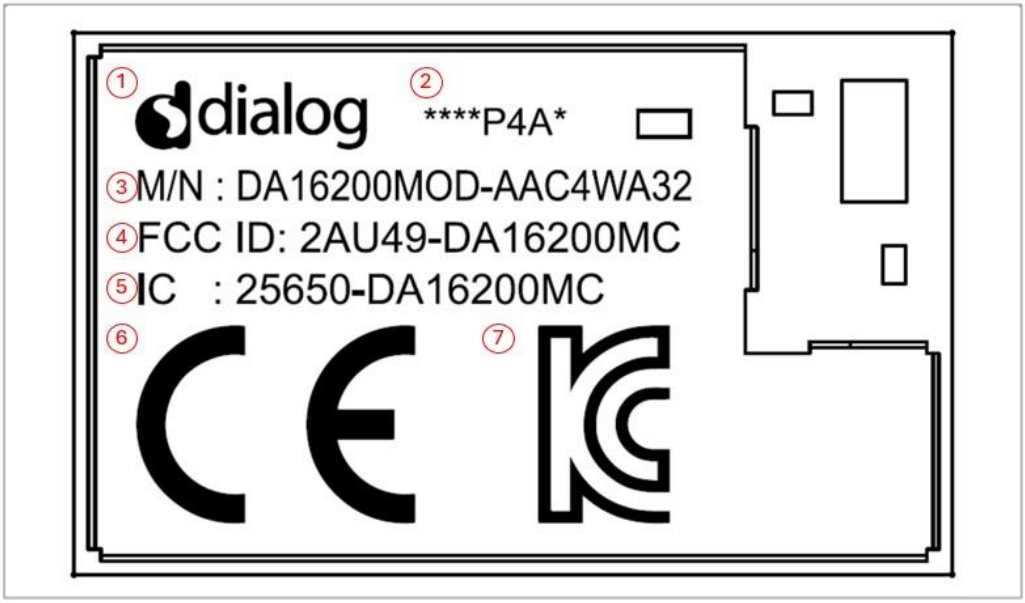


Figure 9. AAE module dimension

8.3 Marking



① Brand Name: Dialog
② Datecode: xxxxP4Ax
③ Model Name: DA162600MOD-AAx4WA32
④ FCC ID
⑤ IC ID
⑥ CE logo
⑦ KCC logo

Figure 10. Module shield marking

9. Design Guidelines

9.1 PCB Land Pattern

Unit: millimeter (mm)

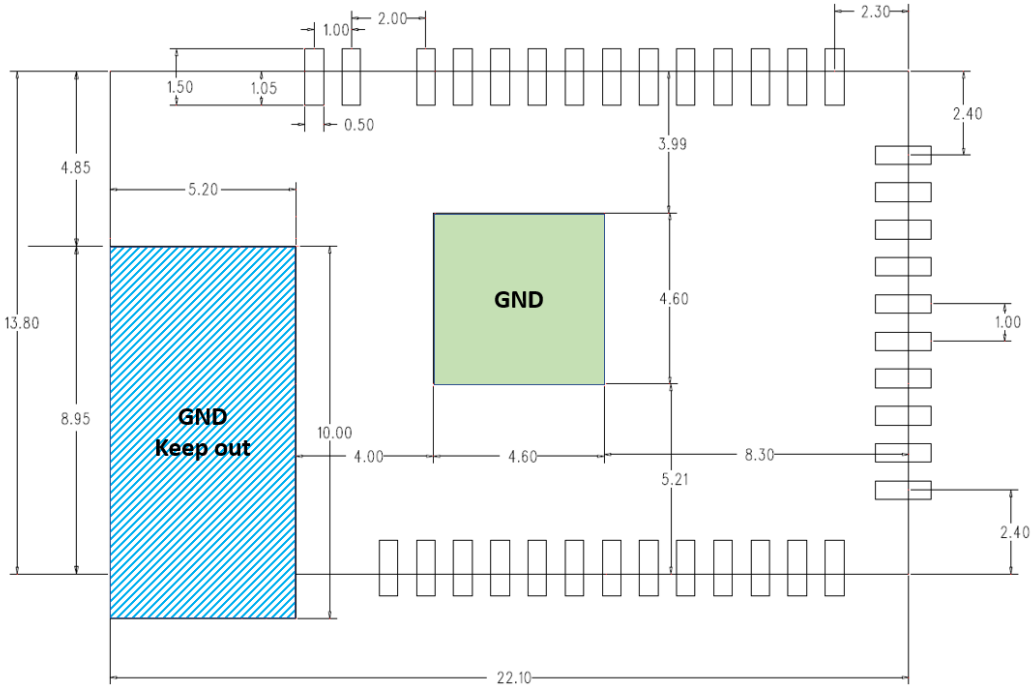


Figure 11. PCB land pattern (top view)

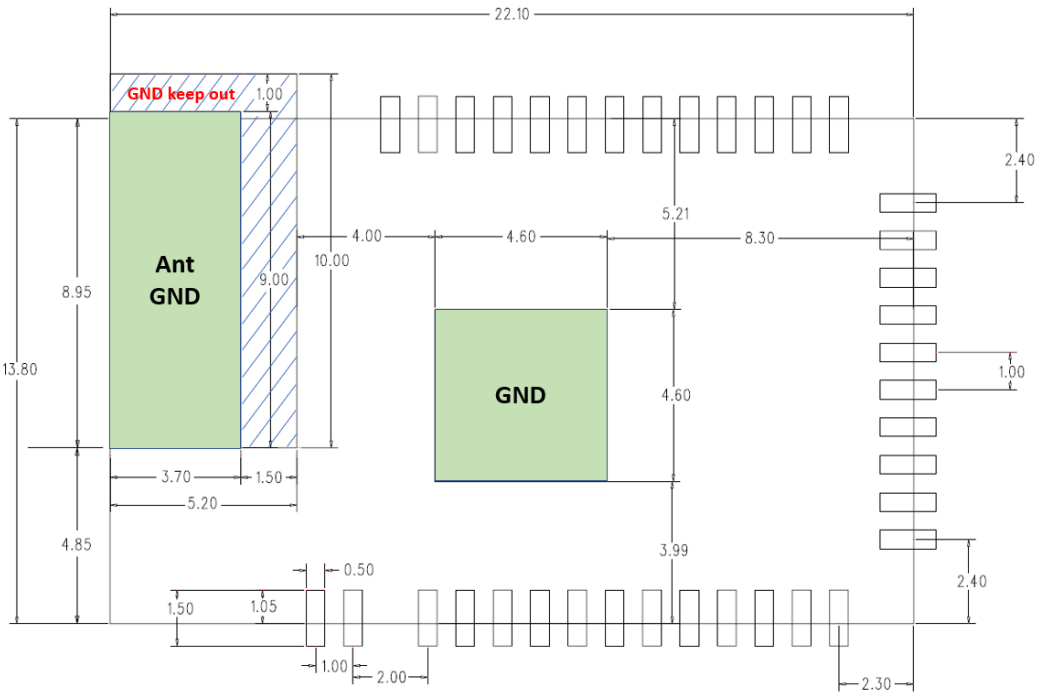


Figure 12. PCB land pattern (bottom view)

9.2 4-Layer PCB Example

Antenna GND is only needed on the bottom of the PCB. GND must be removed for all layers including the inner layer except the bottom.

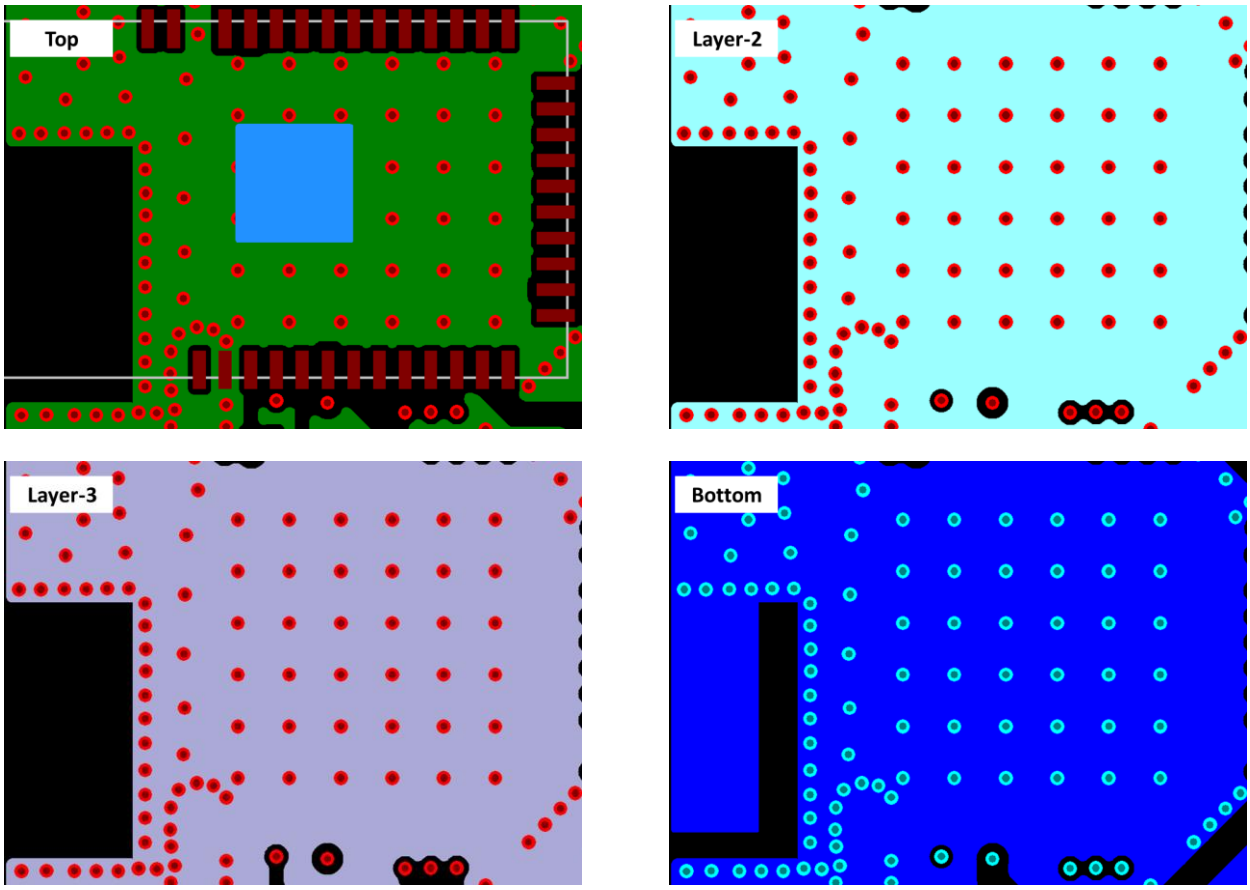


Figure 13. 4-Layer PCB example

9.3 Physical Dimensions of the Module

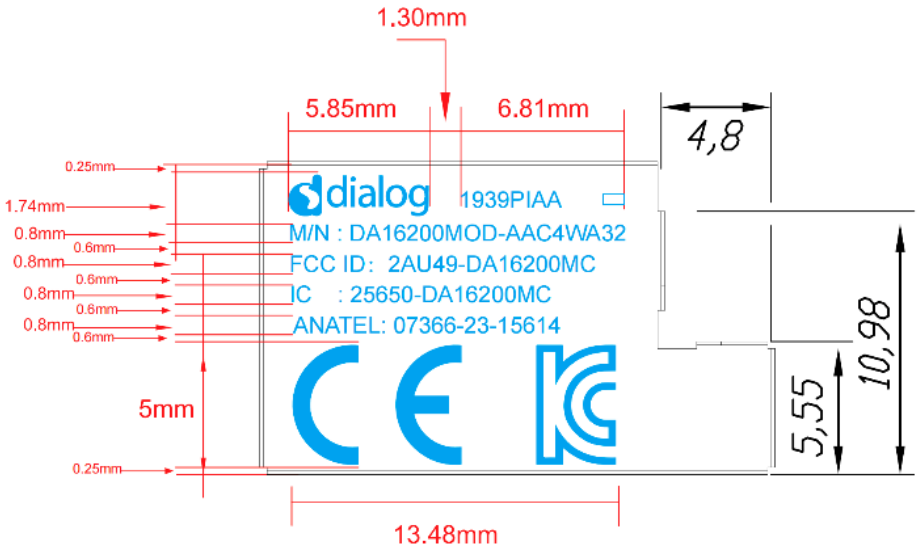


Figure 14. Physical dimensions of the module

10. Soldering

Figure 15 shows the typical process flow for mounting surface mount packages to PCB.

The reflow profile depends on the solder paste being used and the recommendations from the paste manufacture should be followed to determine the proper reflow profile. Figure 16 shows a typical reflow profile when a no-clean paste is used. Oven time above liquidus (260 °C for lead-free solder) is 20 to 40 seconds.

The rework process involves the following steps:

- Component removal
- Site redress
- Solder paste application
- Component placement
- Component attachment.

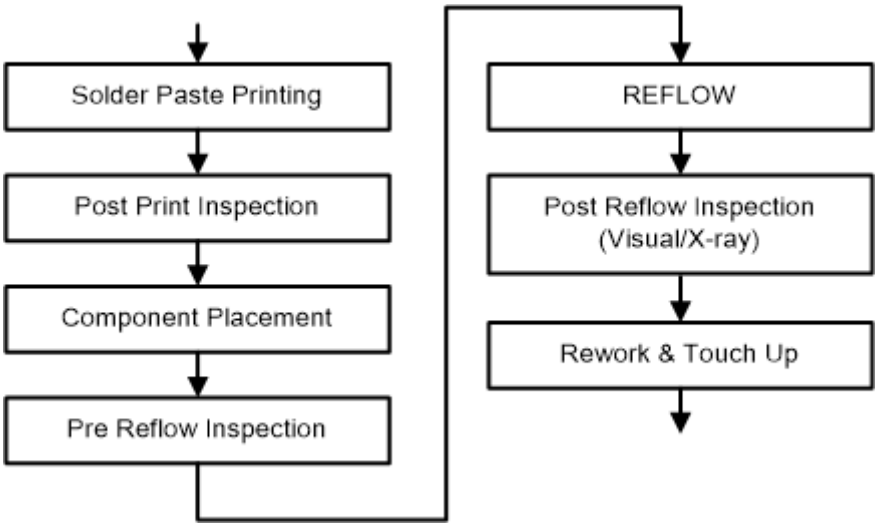


Figure 15. Typical PCB mounting process

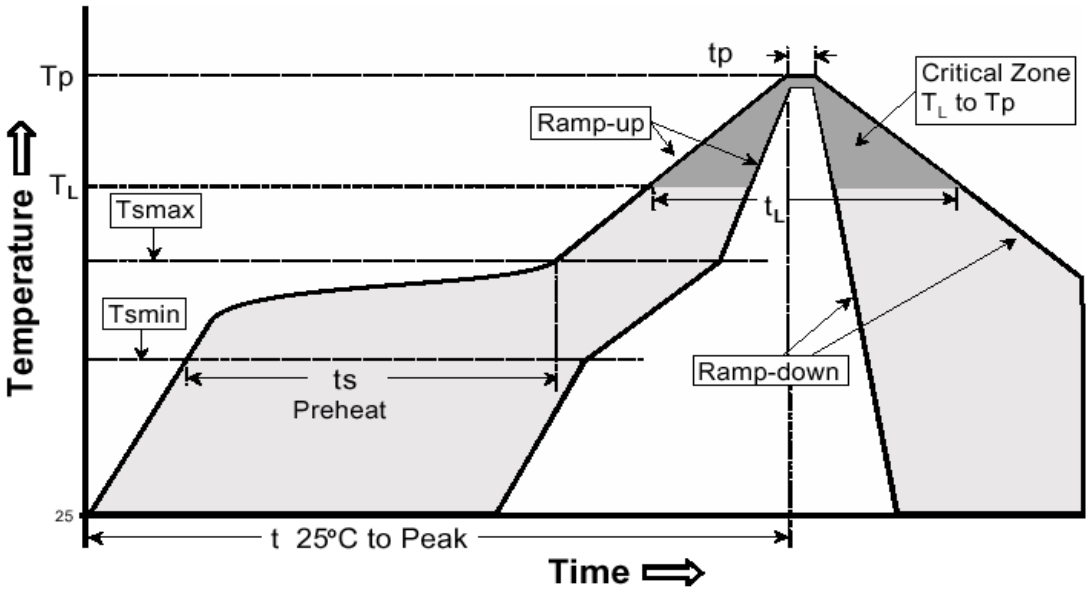


Figure 16. Reflow condition

Table 17. Typical reflow profile (lead free): J-STD-020C

Profile feature	Lead free SMD
Average ramp up rate (Ts_{max} to T_p)	3 °C/s Max
Preheat	
▪ Temperature Min (Ts_{min}) ▪ Temperature Max (Ts_{max}) ▪ Time (Ts_{max} to Ts_{min})	▪ 150 °C ▪ 200 °C ▪ 60 to 180 seconds
Time maintained above	
▪ Temperature (T_L) ▪ Time (t_L)	▪ 217 °C ▪ 60 to 150 seconds
Peak/Classification temperature (T_p)	260 °C
Time within 5 °C of peak temperature (tp)	20 to 40 seconds
Ramp down rate	6 °C/s Max
Time from 25 °C to peak temperature	8 minutes Max

11. Package Information

11.1 Tape and Reel

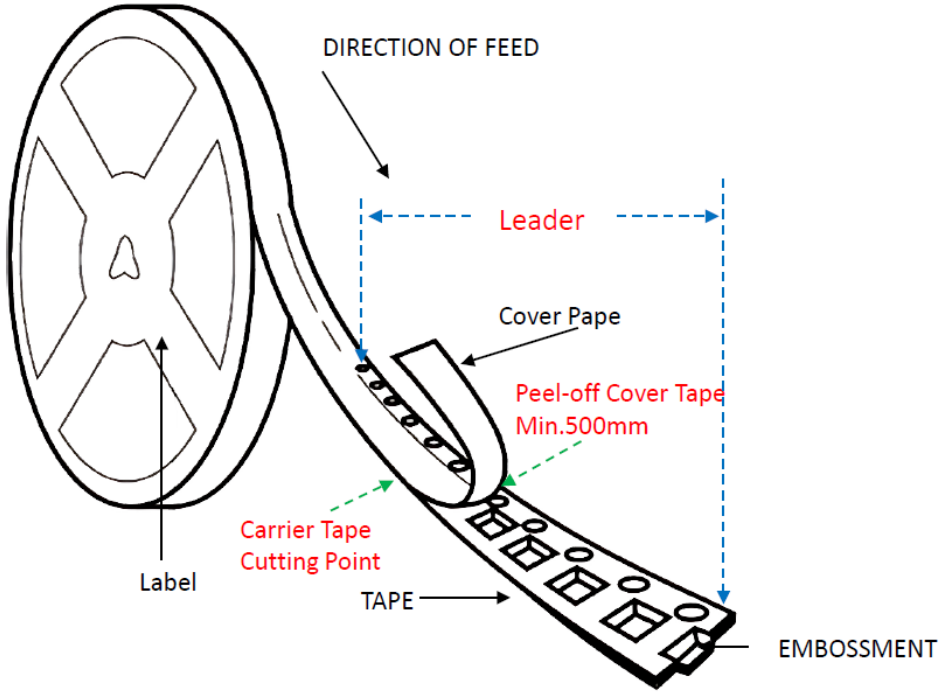


Figure 17. Carrier tape

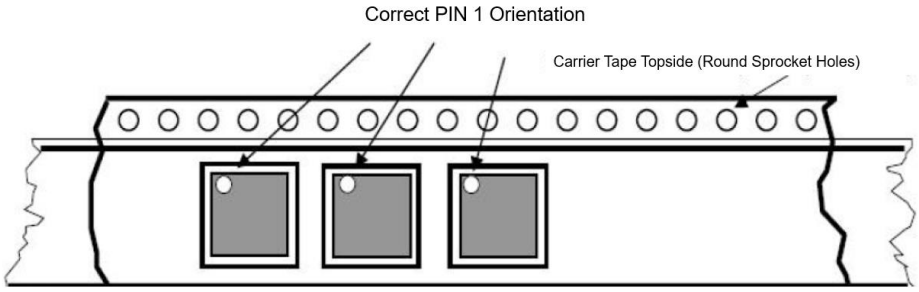
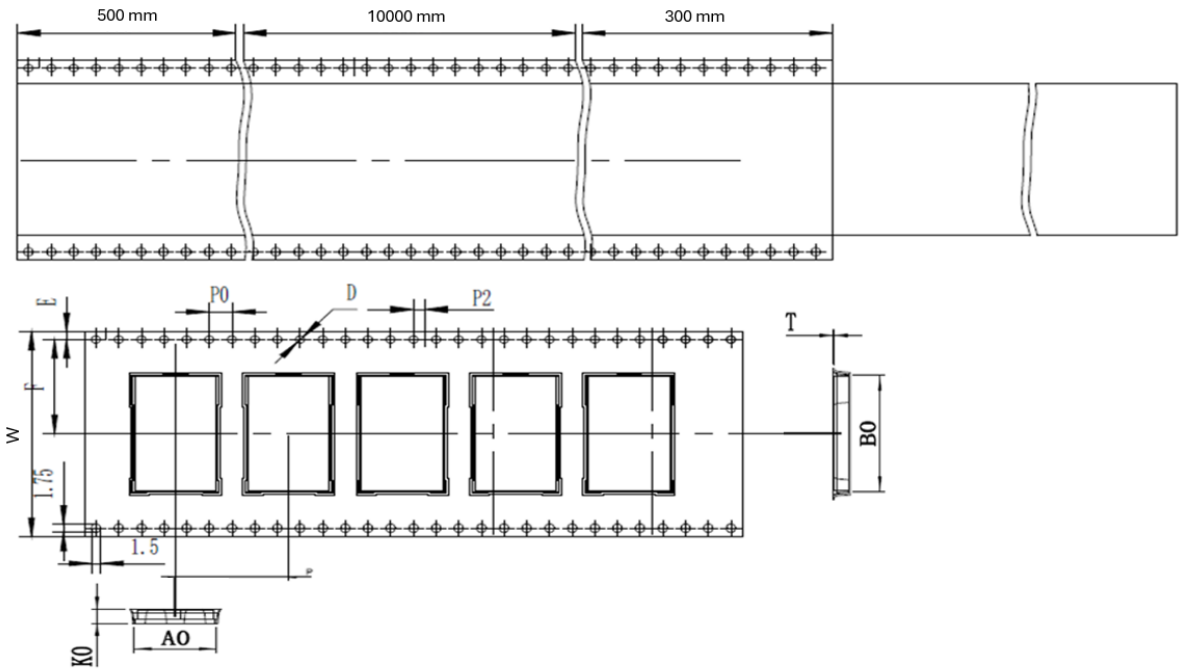


Figure 18. Carrier tape orientation



ITEM	W	A0	B0	K0	E	F	P	P0	P2	D	T
DIM	44.0±0.1	14.2±0.1	22.5±0.1	3.5±0.1	1.75±0.1	20.2±0.1	20.00±0.1	4.00±0.1	2.00±0.1	Ø1.5+0.1	0.35±0.05

Figure 19. Tape and reel

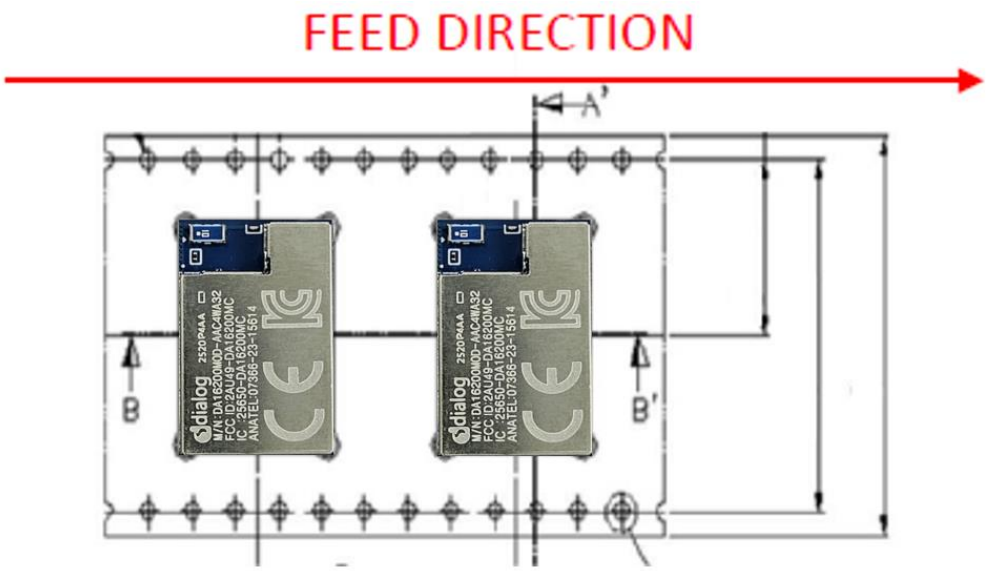


Figure 20. Component direction

Table 18 shows the actual reel specifications.

Table 18. Reel specification

Item	Description
Diameter	13 inches
Reel tape width	44 mm
Tape material	Antistatic
Qty/Reel	500
Leader	Min. 500 mm
Trailer	Min. 500 mm

11.2 Labeling

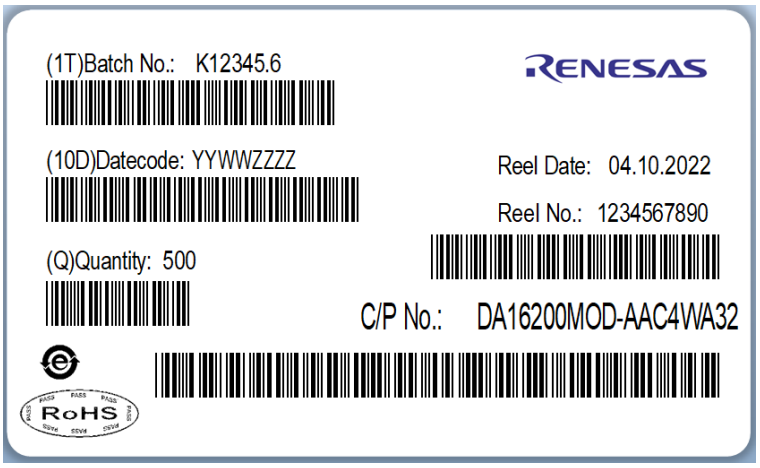


Figure 21. Reel labeling

12. Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, visit the Renesas Electronics website (https://www.renesas.com/kr/en/products/wireless-connectivity/wi-fi/low-power-wi-fi) or contact your local sales representative.

Table 19. Ordering information (production)

Part number	Pins	Size (mm)	Shipment form	Pack quantity
DA16200MOD-AAC4WA32	37	13.8 x 22.1 x 3.3	Reel	MOQ: 500 pcs
DA16200MOD-AAE4WA32	37	13.8 x 22.1 x 3.3	Reel	MOQ: 500 pcs

Part Number Legend:

DA16200MOD-AAC4WA32

AA: Module revision number

C: Select module type

[C] Chip antenna, [E] u.FL connector

4: Flash memory

[4] 4-MB, [2] 2-Mbyte

W: Voltage range

[W] 3.3 V, [L] 1.8 V

A3: Package No.

2: T&R packing

Appendix A Regulatory Approval

DA16200MOD-AAC and DA16200MOD-AAE modules have received regulatory approval for the following countries:

- FCC/United States
  - DA16200MOD-AAC4WA32 FCC ID: 2AU49-DA16200MC
  - DA16200MOD-AAE4WA32 FCC ID: 2AU49-DA16200ME
- IC/Canada
  - DA16200MOD-AAC4WA32 IC ID: 25650-DA16200MCs
  - DA16200MOD-AAE4WA32 IC ID: 25650-DA16200ME
- KCC/Korea
  - DA16200MOD-AAC4WA32 KCC ID: R-C-fci-DA16200M-C4WA3
  - DA16200MOD-AAE4WA32 KCC ID: R-C-fci-DA16200M-E4WA3
- SRRC/China
  - DA16200MOD-AAC4WA32 CMIIT ID: 2020DP0489
  - DA16200MOD-AAE4WA32 CMIIT ID: 2020DJ0161(M)
- TELEC/Japan
  - DA16200MOD-AAC4WA32 TELEC ID:

    
    R 201-190886
  - DA16200MOD-AAE4WA32 TELEC ID:

    
    R 201-190892
- CE/Europe
  - DA16200MOD-AAC4WA32 CE ID: BTL-LVD-1-S1910C136
  - DA16200MOD-AAE4WA32 CE ID: BTL-LVD-1-S1910C137
- WPC/India
  - DA16200MOD-AAC4WA32 WPC ID: ETA-SD-20240807521
  - DA16200MOD-AAE4WA32 WPC ID: ETA-SD-20240807518
- ANATEL/Brazil
  - “este produto contém a placa/módulo DA16200MOD-AAC4WA32 código de homologação Anatel 07366-23-15614”, e os dizeres de radiação restrita conforme Resolução nº 680, de 27 de junho de 2017“ Este equipamento não tem direito à proteção contra interferência prejudicial e não pode causar interferência em sistemas devidamente autorizados. Para maiores informações, consulte o site da ANATEL – (www.anatel.gov.br)”
  - As informações abaixo estão disponibilizadas na Especificação técnica/Manual:

    The information below is available in the Technical Specification/Manual:

    (Model name) Nome do modelo: DA16200MOD-AAC4WA32

    (Country of origin) País de origem: CHINA

    (Manufacturer and address) Fabricante: Renesas Design Korea Inc. B-7F 35, Pangyo-ro 255beon-gil, Bundang-gu, Seongnam-si, Gyeonggi-do, Republic of Korea.

Revision History

Revision	Date	Description
3.8	Sept 12, 2025	▪ Removed Wi-Fi Direct and Wi-Fi Mesh ▪ Added Figure 14 for ANTEL Certification ▪ Updated Figure 20 for ANTEL Certification
3.7	Sept 20, 2024	▪ Added note to pin description table ▪ Added measurement plane definition ▪ Updated Section 11.1 Tape and Reel ▪ Updated Appendix A Regulatory Approval
3.6	Apr 12, 2024	Updated Section 8.3 Marking
3.5	Oct 6, 2023	▪ Removed redundant sections ▪ Added Tape and Reel Information
3.4	May 26, 2023	Added Appendix A Regulatory Approval
3.3	Jan 4, 2023	▪ Section 7.4.1, 8.8.4, Table 17 added details for sleep mode ▪ Updated Table 3 to add storage temperature range and adjusted min max voltages
3.2	June 6, 2022	▪ Updated logo, disclaimer, and copyright ▪ Section 4.1 Updated Flash memory Pin-out Description Table 1 ▪ Section 4.2 Updated Pin Multiplexing Table 2 ▪ Section 7.3.2 Added note about Sleep Mode 2 and 3 for retention I/O ▪ Section 8.3 Fixed typo and added note about SPI slave half-duplex and clock speed calculation ▪ Section 8.4 Added SDIO interface needs pull-up resistors description and Figure 18 ▪ Section 8.5.3 Added I2C Interface Pull-up ▪ Section 8.12 Updated SWD part Table 47 ▪ Section 9 Updated Application Schematic Figure 44
3.1	Feb 3, 2021	▪ Removed BOR part ▪ Added a Note for Power-on Sequence in the Section 6.1, Updated Figure 7, and Table 16 ▪ Section 8.7.3 Fixed typo ▪ Added Section 8.7.1 and 8.7.2 ▪ Updated Applications Schematic
3.0	July 23, 2020	▪ Sync with SoC datasheet v3.1 ▪ Modified Chapter 3 description to Network subsystem layer. ▪ Modified DA16200MOD pin Mux (Table 2) ▪ Added module default pin conditions. ▪ I2C CLK GPIOA2 -> GPIOA3 ▪ Added chapter 5.3.3, 5.3.4 ▪ Modified Rx max input level in chapter 5.4.1(Table 11) ▪ Updated Chapter Note 1 Sleep mode description ▪ Updated RTC_PWR_KEY description and removed one sentence which leads to misunderstanding. Table 17 ▪ Modified I2C timing in Table 30, Table 32 ▪ Added description of chapter 8.9.1 ▪ Updated Chapter 9 application schematics ▪ Changed Module dimension picture Figure 45 and Figure 46 ▪ Removed F_xx pins

Revision	Date	Description
		▪ Changed the link from customer support portal to Dialog website. ▪ Added PCB land pattern Figure 48, Figure 49
2.0	May 8, 2020	▪ Added Tolerance of dimension ▪ Added min/max Radio characteristics in Table 11, Table 12, and Table 13 ▪ Modified Chapter 8.10.3 Baud rate ▪ Updated Reach and RoHS compliance
1.4	Apr 7, 2020	▪ Updated Key Features ▪ Modified DA16200MOD pin Mux Table 2 ▪ Chapter 7.4 Pulse Counter added ▪ Chapter 8.10.1 RS-232 added
1.3	Mar 23, 2020	▪ Added ESD performance, Table 15 ▪ AC characteristics and current consumption of data updated in Table 11, Table 12, and Table 13 ▪ Updated Key Features, about clock source and embedded memory
1.2	Oct 22, 2019	Modified module size
1.0	Oct 03, 2019	Target datasheet

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com.

RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.