DA9083

High Current, Highly Configurable System PMIC

DA9083 is a six-channel, advanced, system power management IC (PMIC) that integrates four buck converters, one LDO, and one load switch. This high current, integrated PMIC is ideal for Client and Enterprise SSD Modules, Hybrid Drives, and other memory management applications. Due to its highly configurable and flexible design, it supports a wide variety of other applications with integrated microcontrollers, DSPs, and FPGAs in embedded applications and a host of other Internet of Things (IoT) and consumer applications.

DA9083 includes many robust protection features, a dedicated I^2C interface, and programmable output voltages. Dynamic voltage control (DVC) enables supply voltage controllability based on the application requirements. This PMIC is capable of achieving high efficiencies and fast transient responses to line and load changes while keeping the overall board space to a minimum. All of these features and functionality is offered in a compact 36-lead CSP package.

Key Features

- Power supply voltage (V_{IN}) 2.9 V to 5.5 V
- 4 buck converters
- Selectable output voltage range for all bucks:
  - 1.5 V to 2.7 V, 20 mV step
  - 0.55 V to 1.9 V, 10 mV step
- Maximum output current:
  - CH1, CH2, CH3 Bucks: 2.5 A
  - CH4 Buck: 5.0 A
- Interleaving of switching phases of bucks
- LDO:
  - V_{OUT}: 1.4 V to 1.9 V, 20 mV step
  - I_{OUT}: 0.1 A (max)
- Load switch (LSW)
  - R_{DS_ON}: 20 mΩ (typ)
  - Current limit at soft start: 100 mA
  - Current limit: 4 A
- Protection functions:
  - Over-current protection
  - Over/Under-voltage protection
  - Thermal shutdown protection
- I^2C control interface:
  - Standard mode (100 kbit/s)
  - Fast mode (400 kbit/s)
  - Fast mode+ (1 Mbit/s)
  - High-speed mode (3.4 Mbit/s)
- I_{OUT}: 0.1 A (max)

Applications

- SSD (solid state drive) module
- Portable devices
- Home entertainment equipment

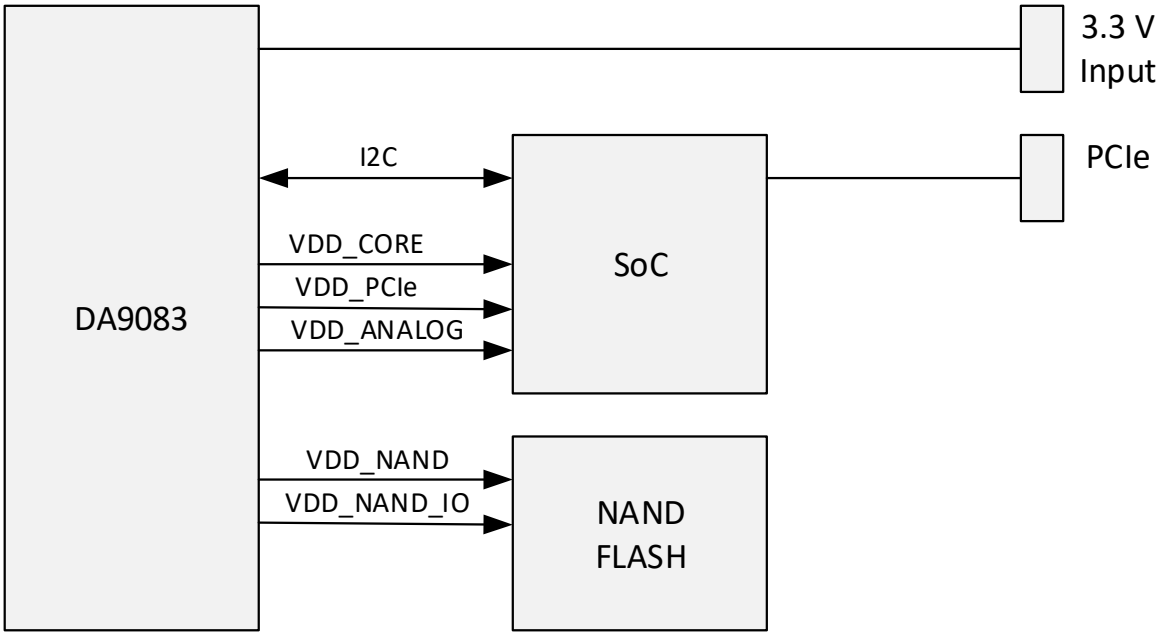

Figure 1. System Diagram

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1. Terms and Definitions

CDM	Charged-device model
CH	Channel
DVC	Dynamic voltage control
ESD	Electrostatic discharge
HBM	Human body model
HPM	High power mode
LPM	Low power mode
OTP	One-time programmable
OVP	Over-voltage protection
POR	Power-on reset
PMIC	Power management integrated circuit
PWM	Pulse width modulation
PFM	Pulse frequency modulation
TSD	Thermal shut down
UVLO	Under-voltage lock out
UVP	Under-voltage protection

2. References

[1] I^2C-Bus Specification Rev 06 UM1010204, issued on 4 April 2014.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Overview

3.1 Block Diagram

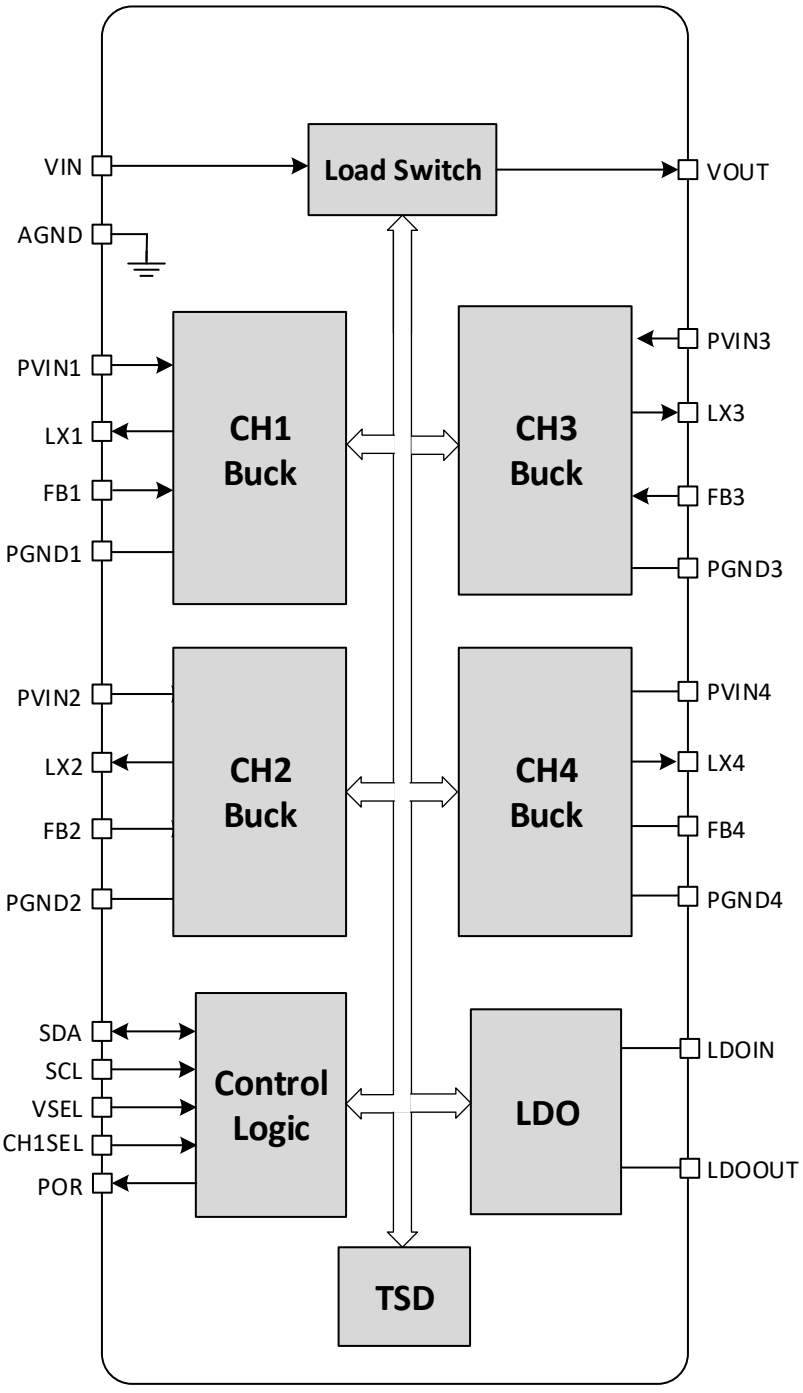


Figure 2. Block Diagram

4. Pin Information

4.1 Pin Assignments

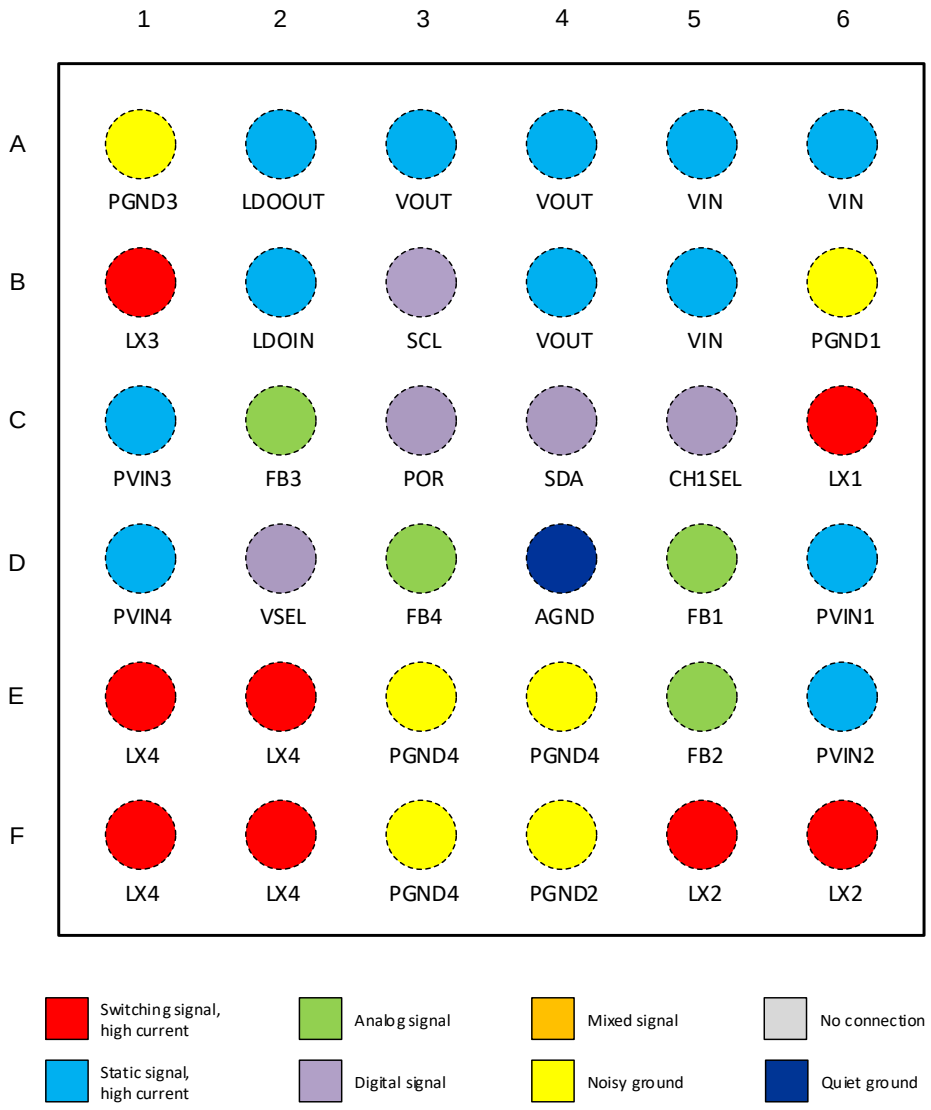


Figure 3. WLCSP Pinout Diagram (Top View)

4.2 Pin Descriptions

Table 1. Pin Description

Pin Number	Pin Name	Type (Table 2)	Description
A1	PGND3	GND	CH3 DCDC buck converter ground
A2	LDOOUT	PWR	LDO output, bypass to ground with ceramic capacitor
A3	VOUT	PWR	Load Switch output
A4	VOUT	PWR	Load Switch output
A5	VIN	PWR	Load Switch input
A6	VIN	PWR	Load Switch input

Pin Number	Pin Name	Type (Table 2)	Description
B1	LX3	PWR	CH3 DCDC buck converter switching node
B2	LDOIN	PWR	LDO input, bypass to ground with a ceramic capacitor
B3	SCL	DI	I^2C interface data, connect SCL to the logic rail through a pull-up resistor
B4	VOUT	PWR	Load Switch output
B5	VIN	PWR	Load Switch input
B6	PGND1	GND	CH1 Buck converter power ground
C1	PVIN3	PWR	CH3 Buck converter input
C2	FB3	AI	CH3 Buck output voltage feedback connection
C3	POR	DOD	Power-on-Reset release output signal (Power Good), output open-drain, active high
C4	SDA	DIOD	I^2C interface data. Connect SDA to the logic rail through a pull-up resistor
C5	CH1SEL	DI	Reserved. Needs to be tied to ground
C6	LX1	PWR	CH1 Buck converter switching node
D1	PVIN4	PWR	CH4 Buck converter power
D2	VSEL	DI	Reserved. Needs to be tied to ground
D3	FB4	AI	CH4 Buck output voltage feedback connection
D4	AGND	GND	Quiet ground connection, Connect to a quiet ground area
D5	FB1	AI	CH1 Buck output voltage feedback connection
D6	PVIN1	PWR	CH1 Buck converter input
E1	LX4	PWR	CH4 Buck converter switching node
E2	LX4	PWR	CH4 Buck converter switching node
E3	PGND4	GND	CH4 Buck converter power ground
E4	PGND4	GND	CH4 Buck converter power ground
E5	FB2	AI	CH2 Buck output voltage feedback connection
E6	PVIN2	PWR	CH2 Buck converter input
F1	LX4	PWR	CH4 Buck converter switching node
F2	LX4	PWR	CH4 Buck converter switching node
F3	PGND4	GND	Power ground for the CH4 Buck converter
F4	PGND2	GND	Power ground for the CH2 Buck converter
F5	LX2	PWR	CH2 Buck converter switching node
F6	LX2	PWR	CH2 Buck converter switching node

Table 2. Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	GND	Ground
DIOD	Digital input/output open drain		
DOD	Digital output open drain		
PWR	Power		

5. Specifications

5.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Table 3. Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
T_{STG}	Storage temperature		-60	150	°C
V_{SYS}	System supply voltage	Referenced to AGND	-0.3	6	V
V_{PIN}	All other terminals	Referenced to AGND	-0.3	6	V

5.2 Electrostatic Discharge Ratings

Table 4. Electrostatic Discharge Ratings

Parameter	Description	Conditions	Rating	Unit
V_{ESD_HBM}	Maximum ESD protection	Human body model (HBM) All exposed pins	2	kV
V_{ESD_CDM}	Maximum ESD protection	Charged device model (CDM)	0.5	kV

5.3 Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature		-40		85	°C
T_J	Operating junction temperature		-40		125	°C
V_{IN}	Input Supply voltage		2.9		5.5	V
V_{PIN}	Voltage on pins		-0.3		V_{IN}+0.3	V
V_{IO}	IO voltage Note 1	SDA and SCL		1.8		V

Note 1 IO voltage is 3.3 V compatible as long as V_{IN} is within the recommended operating range.

5.4 Thermal Specifications

Table 6. Package Ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{Θ_JA}	Package thermal resistance Note 1			28.6		°C/W
P_D	**Power dissipation**	Derating factor above T_A= 70°C, 35 mW/°C (1/R_{Θ_JA})		2450		mW

Note 1 Obtained from package thermal simulation, 4-layer board (JEDEC). Influenced by PCB technology and layout.

5.5 CH1 Buck Converter Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 2.9 V ≤ V_{IN} ≤ 5.5 V, fsw = 2 MHz.

Table 7: CH1 Buck Converter Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External electrical conditions						
V_{IN}	Input voltage of power stage		2.7	3.3	5.5	V
C_{OUT}	Output capacitance, including voltage and temperature coefficient	Only local capacitor without decoupling capacitor at load side.	11	22	29	µF
ESR_{COUT}	Output capacitor series resistance	f > 100 kHz		3		mΩ
L	Inductor value, including current and temperature dependence		0.23	0.47	0.61	µH
DCR_L	Inductor DC resistance			20	50	mΩ
Electrical performance						
I_{Q_LPM}	Quiescent current in Low Power mode (no switching)	V_{IN} = 3.3 V T_A = 27 °C		18		µA
I_{Q_AUTO}	Quiescent current in Auto mode (no switching)	V_{IN} = 3.3 V T_A = 27 °C		42		µA
f_{SW}	Switching frequency		1.9	2	2.1	MHz
$V_{DROPOUT}$	Voltage drop from PVIN to VOUT			1		V
V_{OUT_DIV}	Range of output voltage with divider (OTP option), programmable in 20 mV steps.	PVIN1 = 2.7 V to 5.5 V	1.5		2.7	V
$V_{OUT\_NO\_DIV}$	Range of output voltage without divider (OTP option), programmable in 10 mV steps.	PVIN1 = 2.7 V to 5.5 V	0.5		1.9	V
SR_{SS}	Soft start slew rate			2.5		mV/µs
V_{OUT_ACC}	Output voltage accuracy, including static line and load regulation	V_{OUT} ≥ 1 V T_A = 27 °C	-1		1	%

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OUT_ACC}	Output voltage accuracy, including static line and load regulation	V_{OUT} < 1 V	-10		10	mV
R_{ON_PMOS}	On resistance of switching PMOS	V_{IN} = 3.3 V T_A = 27 °C		62		mΩ
R_{ON_NMOS}	On resistance of switching NMOS	V_{IN} = 3.3 V T_A = 27 °C		28		mΩ
I_{POSLIM}	Positive current limit threshold	With default setting V_{IN} = 3.3 V T_A = 27 °C	3	4		A
$V_{THR\_OVP\_RISE}$	Over-voltage protection threshold		+200	+300	+400	mV
$V_{THR\_UVP\_FALL}$	Under-voltage protection threshold		-400	-300	-200	mV
R_{DCHG}	Discharge resistance for LX node	V_{IN} = 3.3 V T_A = 27 °C		10		Ω
t_{ON_MIN}	Buck minimum On-time	V_{IN} = 3.3 V T_A = 27 °C		20		ns

5.6 CH2 Buck Converter Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 2.9 V ≤ V_{IN} ≤ 5.5 V, fsw = 2 MHz.

Table 8: CH2 Buck Converter Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External electrical conditions						
V_{IN}	Input voltage of power stage		2.7	3.3	5.5	V
C_{OUT}	Output capacitance, including voltage and temperature coefficient	Only local capacitor without decoupling capacitor at load side.	11	22	29	µF
ESR_{COUT}	Output capacitor series resistance	f > 100 kHz		3		mΩ
L	Inductor value, including current and temperature dependence		0.23	0.47	0.61	µH
DCR_L	Inductor DC resistance			20	50	mΩ
Electrical performance						
I_{Q_LPM}	Quiescent current in Low Power mode (no switching)	V_{IN} = 3.3 V T_A = 27 °C		17		µA
I_{Q_AUTO}	Quiescent current in Auto mode (no switching)	V_{IN} = 3.3 V T_A = 27 °C		42		µA
f_{SW}	Switching frequency		1.9	2	2.1	MHz
$V_{DROPOUT}$	Voltage drop from PVIN to VOUT			1		V
V_{OUT_DIV}	Range of output voltage with divider (OTP option), programmable in 20 mV steps.	PVIN2 = 2.7 V to 5.5 V	1.5		2.7	V
$V_{OUT\_NO\_DIV}$	Range of output voltage with no divider (OTP option), programmable in 10 mV steps.	PVIN2 = 2.7 V to 5.5 V	0.5		1.9	V
SR_{SS}	Soft start slew rate			2.5		mV/µs
V_{OUT_ACC}	Output voltage accuracy, including static line and load regulation	V_{OUT} ≥ 1 V T_A = 27 °C	-1		1	%
V_{OUT_ACC}	Output voltage accuracy, including static line and load regulation	V_{OUT} < 1 V	-10		10	mV
R_{ON_PMOS}	On resistance of switching PMOS	V_{IN} = 3.3 V T_A = 27 °C		62		mΩ
R_{ON_NMOS}	On resistance of switching NMOS	V_{IN} = 3.3 V T_A = 27 °C		28		mΩ
I_{POSLIM}	Positive current limit threshold	With default setting V_{IN} = 3.3 V T_A = 27 °C	3	4		A

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{THR\_OVP\_RISE}$	Over-voltage protection threshold		+200	+300	+400	mV
$V_{THR\_UVP\_FALL}$	Under-voltage protection threshold		-400	-300	-200	mV
R_{DCHG}	Discharge resistance for LX node	V_{IN} = 3.3 V T_A = 27 °C		20		Ω
t_{ON_MIN}	Buck minimum On-time	V_{IN} = 3.3 V T_A = 27 °C		20		ns

5.7 CH3 Buck Converter Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 2.9 V ≤ V_{IN} ≤ 5.5 V, fsw = 2 MHz.

Table 9: CH3 Buck Converter Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External electrical conditions						
V_{IN}	Input voltage of power stage		2.7	3.3	5.5	V
C_{OUT}	Output capacitance, including voltage and temperature coefficient	Only local capacitor without decoupling capacitor at load side.	11	22	29	µF
ESR_{COUT}	Output capacitor series resistance	f > 100 kHz		5		mΩ
L	Inductor value, including current and temperature dependence		0.23	0.47	0.61	µH
DCR_L	Inductor DC resistance			20	50	mΩ
Electrical performance						
I_{Q_LPM}	Quiescent current in Low Power mode (no switching)	V_{IN} = 3.3 V T_A = 27 °C		17		µA
I_{Q_AUTO}	Quiescent current in Auto mode (no switching)	V_{IN} = 3.3 V T_A = 27 °C		42		µA
f_{SW}	Switching frequency		1.9	2	2.1	MHz
$V_{DROPOUT}$	Voltage drop from PVIN to VOUT			1		V
V_{OUT_DIV}	Range of output voltage with divider (OTP option), programmable in 20 mV steps.	PVIN3 = 2.7 V to 5.5 V	1.5		2.7	V
$V_{OUT\_NO\_DIV}$	Range of output voltage with no divider (OTP option), programmable in 10 mV steps.	PVIN3 = 2.7 V to 5.5 V	0.5		1.9	V
SR_{SS}	Soft start slew rate			2.5		mV/µs
V_{OUT_ACC}	Output voltage accuracy, including static line and load regulation	V_{OUT} ≥ 1 V T_A = 27 °C	-1		1	%
V_{OUT_ACC}	Output voltage accuracy, including static line and load regulation	V_{OUT} < 1 V	-10		10	mV
R_{ON_PMOS}	On resistance of switching PMOS	V_{IN} = 3.3 V T_A = 27 °C		62		mΩ
R_{ON_NMOS}	On resistance of switching NMOS	V_{IN} = 3.3 V T_A = 27 °C		28		mΩ
I_{POSLIM}	Positive current limit threshold	With default setting V_{IN} = 3.3 V T_A = 27 °C	3	4		A

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{THR\_OVP\_RISE}$	Over-voltage protection threshold		+200	+300	+400	mV
$V_{THR\_UVP\_FALL}$	Under-voltage protection threshold		-400	-300	-200	mV
R_{DCHG}	Discharge resistance for LX node	V_{IN} = 3.3 V T_A = 27 °C		30		Ω
t_{ON_MIN}	Buck minimum On-time	V_{IN} = 3.3 V T_A = 27 °C		20		ns

5.8 CH4 Buck Converter Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 2.9 V ≤ V_{IN} ≤ 5.5 V, fsw = 2 MHz.

Table 10: CH4 Buck Converter Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External electrical conditions						
V_{IN}	Input voltage of power stage		2.7	3.3	5.5	V
C_{OUT}	Output capacitance, including voltage and temperature coefficient	Only local capacitor without decoupling capacitor at load side.	11	22	29	µF
ESR_{COUT}	Output capacitor series resistance	f > 100 kHz		3		mΩ
L	Inductor value, including current and temperature dependence		0.23	0.47	0.61	µH
DCR_L	Inductor DC resistance			20	50	mΩ
Electrical performance						
I_{Q_LPM}	Quiescent current in Low Power mode (no switching)	V_{IN} = 3.3 V T_A = 27 °C		17		µA
I_{Q_AUTO}	Quiescent current in Auto mode (no switching)	V_{IN} = 3.3 V T_A = 27 °C		42		µA
f_{SW}	Switching frequency		1.9	2	2.1	MHz
$V_{DROPOUT}$	Voltage drop from PVIN to VOUT			1		V
V_{OUT_DIV}	Range of output voltage with divider (OTP option), programmable in 20 mV steps.	PVIN4 = 2.7 V to 5.5 V	1.5		2.7	V
$V_{OUT\_NO\_DIV}$	Range of output voltage with no divider (OTP option), programmable in 10 mV steps.	PVIN4 = 2.7 V to 5.5 V	0.5		1.9	V
SR_{SS}	Soft start slew rate			2.5		mV/µs
V_{OUT_ACC}	Output voltage accuracy, including static line and load regulation	V_{OUT} ≥ 1 V T_A = 27 °C	-1		1	%
V_{OUT_ACC}	Output voltage accuracy, including static line and load regulation	V_{OUT} < 1 V	-10		10	mV
R_{ON_PMOS}	On resistance of switching PMOS	V_{IN} = 3.3 V T_A = 27 °C		52		mΩ
R_{ON_NMOS}	On resistance of switching NMOS	V_{IN} = 3.3 V T_A = 27 °C		20		mΩ
I_{POSLIM}	Positive current limit threshold	With default setting V_{IN} = 3.3 V T_A = 27 °C	7	8.5		A

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{THR\_OVP\_RISE}$	Over-voltage protection threshold		+200	+300	+400	mV
$V_{THR\_UVP\_FALL}$	Under-voltage protection threshold		-400	-300	-200	mV
R_{DCHG}	Discharge resistance for LX node	V_{IN} = 3.3 V T_A = 27 °C		25		Ω
t_{ON_MIN}	Buck minimum On-time	V_{IN} = 3.3 V T_A = 27 °C		20		ns

5.9 Load Switch Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 2.9 V ≤ V_{IN} ≤ 5.5 V.

Table 11: Load Switch Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External electrical conditions						
V_{IN}	Input voltage		2.2	3.3	5.5	V
Electrical performance						
I_Q	Quiescent current	V_{IN} = 3.3 V T_A = 27 °C		14.5		µA
R_{ON}	On resistance	V_{IN} = 3.3 V T_A = 27 °C I_{OUT} = 200 mA		20		mΩ
$I_{LIM\_SOFTSTART}$	Current limit at soft start	V_{IN} = 3.3 V T_A = 27 °C	50	100	150	mA
I_{LIM}	Current limit	V_{IN} = 3.3 V T_A = 27 °C	4			A
$t_{SOFTSTART}$	Soft start time	No load condition V_{IN} = 3.3 V C_{OUT} = 50 µF		1.5		ms

5.10 LDO Electrical Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 2.9 V ≤ V_{IN} ≤ 5.5 V.

Table 12: LDO Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External electrical conditions						
V_{IN}	Input voltage of power stage		2.7	3.3	5.5	V
C_{OUT}	Output capacitance, including voltage and temperature coefficient		2.3	4.7	6.1	µF
Electrical performance						
I_Q	Quiescent current	V_{IN} = 3.3 V T_A = 27 °C		3.5		µA
V_{OUT}	Output voltage range		1.4		1.9	V
V_{OUT_STEP}	Output voltage programable step			20		mV
V_{OUT_ACC}	Output voltage accuracy, including static line and load regulation	V_{IN} = 3.3 V V_{LDOOUT} = 1.8 V I_{OUT} = 10 mA T_A = 27 °C,	1.782	1.8	1.818	V
$t_{SOFTSTART}$	Soft start time	No load condition V_{IN} = 3.3 V V_{LDOOUT} = 1.8 V T_A = 27 °C C_{OUT} = 4.7 µF		0.5	0.8	ms
I_{INRUSH}	Inrush current	V_{IN} = 3.3 V T_A = 27 °C C_{OUT} = 4.7 µF			200	mA
I_{LIM}	Current limit threshold	V_{IN} = 3.3 V V_{LDOOUT} = 1.8 V T_A = 27 °C C_{OUT} = 4.7 µF	200			mA
$V_{DROPOUT}$	Voltage drop from LDOIN to LDOOUT	V_{IN} = 3.3 V V_{LDOOUT} = 1.8 V I_{OUT} = 200 mA T_A = 27 °C C_{OUT} = 4.7 µF		250	530	mV
$V_{THR\_OVP\_RISE}$	Over-voltage protection threshold		2.2	2.25	2.3	V
$V_{THR\_UVP\_FALL}$	Under-voltage protection threshold		0.95	1	1.05	V
R_{DCHG}	Discharge resistance			47		Ω

5.11 Supervision Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 2.9 V ≤ V_{IN} ≤ 5.5 V.

Table 13: Supervision Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External electrical conditions						
V_{IN}	Input voltage		2.9		5.5	V
Electrical performance						
I_Q	Quiescent current			11.5		µA
$V_{THR\_OVP\_RISE}$	V_{IN} over-voltage protection threshold for V_{IN} rising		5.6	5.7	5.85	V
$V_{THR\_OVP\_HYS}$	V_{IN} over-voltage protection hysteresis			0.3		V
$V_{THR\_UVLO\_FALL}$	V_{IN} UVLO threshold for V_{IN} falling		2.1		2.3	V
$V_{THR\_UVLO\_HYS}$	V_{IN} UVLO hysteresis			0.1		V
$V_{THR\_POR\_FALL}$	V_{OUT} POR threshold for V_{OUT} falling		2.6	2.7	2.8	V
$V_{THR\_POR\_HYS}$	V_{OUT} POR hysteresis		0.05	0.1	0.15	V
t_{D_POR}	POR delay time until POR pin is asserted.			6		ms
T_{THR_SHDN}	Thermal shutdown threshold		130	140	150	°C
$T_{THR\_SHDN\_HYS}$	Thermal shutdown hysteresis			15		°C

5.12 I²C Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 2.9 V ≤ V_{IN} ≤ 5.5 V.

Table 14: I2C Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical performance						
Standard/Fast/Fast+ Mode						
t_{BUS}	Bus free time between a STOP and START condition		0.5			µs
C_{BUS}	Bus line capacitive load				150	pF
f_{SCL}	SCL clock frequency				1000	kHz
t_{LO_SCL}	SCL low time		0.5			µs
t_{HI_SCL}	SCL high time		0.26			µs
t_{RISE}	SCL and SDA rise time. Requirement for input.				1000	ns
t_{FALL}	SCL and SDA fall time. Requirement for input.				300	ns
t_{SETUP_START}	Start condition setup time		0.26			µs
t_{HOLD_START}	Start condition hold time		0.26			µs
t_{SETUP_STOP}	Stop condition setup time		0.26			µs
t_{DATA}	Data valid time				0.45	µs
t_{DATA_ACK}	Data valid acknowledge time				0.45	µs
t_{SETUP_DATA}	Data setup time		50			ns
t_{HOLD_DATA}	Data hold time		0			ns
t_{SPIKE}	Spike suppression pulse width		0		50	ns
HS Mode						
C_{BUS}	Bus line capacitive load				100	pF
f_{SCL}	SCL clock frequency				3400	kHz
t_{LO_SCL}	SCL low time		160			ns
t_{HI_SCL}	SCL high time		60			ns
t_{RISE}	SCL and SDA rise time. Requirement for input.				160	ns
t_{FALL}	SCL and SDA fall time. Requirement for input.				160	ns
t_{SETUP_START}	Start condition setup time		160			ns
t_{HOLD_START}	Start condition hold time		160			ns
t_{SETUP_STOP}	Stop condition setup time		160			ns

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{SETUP_DATA}	Data setup time		10			ns
t_{HOLD_DATA}	Data hold time		0			ns
t_{SPIKE}	Spike suppression pulse width		0		10	ns

5.13 Digital I/O Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 2.9 V ≤ V_{IN} ≤ 5.5 V.

Table 15: Digital I/O Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical performance						
$V_{IH\_SCL\_SDA}$	Input high voltage, SCL, SDA		1.2			V
$V_{IL\_SCL\_SDA}$	Input low voltage, SCL, SDA				0.4	V
V_{OL_POR}	Output low voltage, POR	I_{OUT} = 3 mA			0.4	V
V_{OL_SDA}	Output low voltage, SDA	I_{OUT} = 3 mA			0.4	V
I_{LKG_POR}	V_{POR} = 3.3 V				1	µA

6. Functional Description

6.1 Function State

The function state flow is described in Figure 4 and Table 16. Normal sequences such as start-up and shut-down are controlled by this flow. Fault protection also follows this flow.

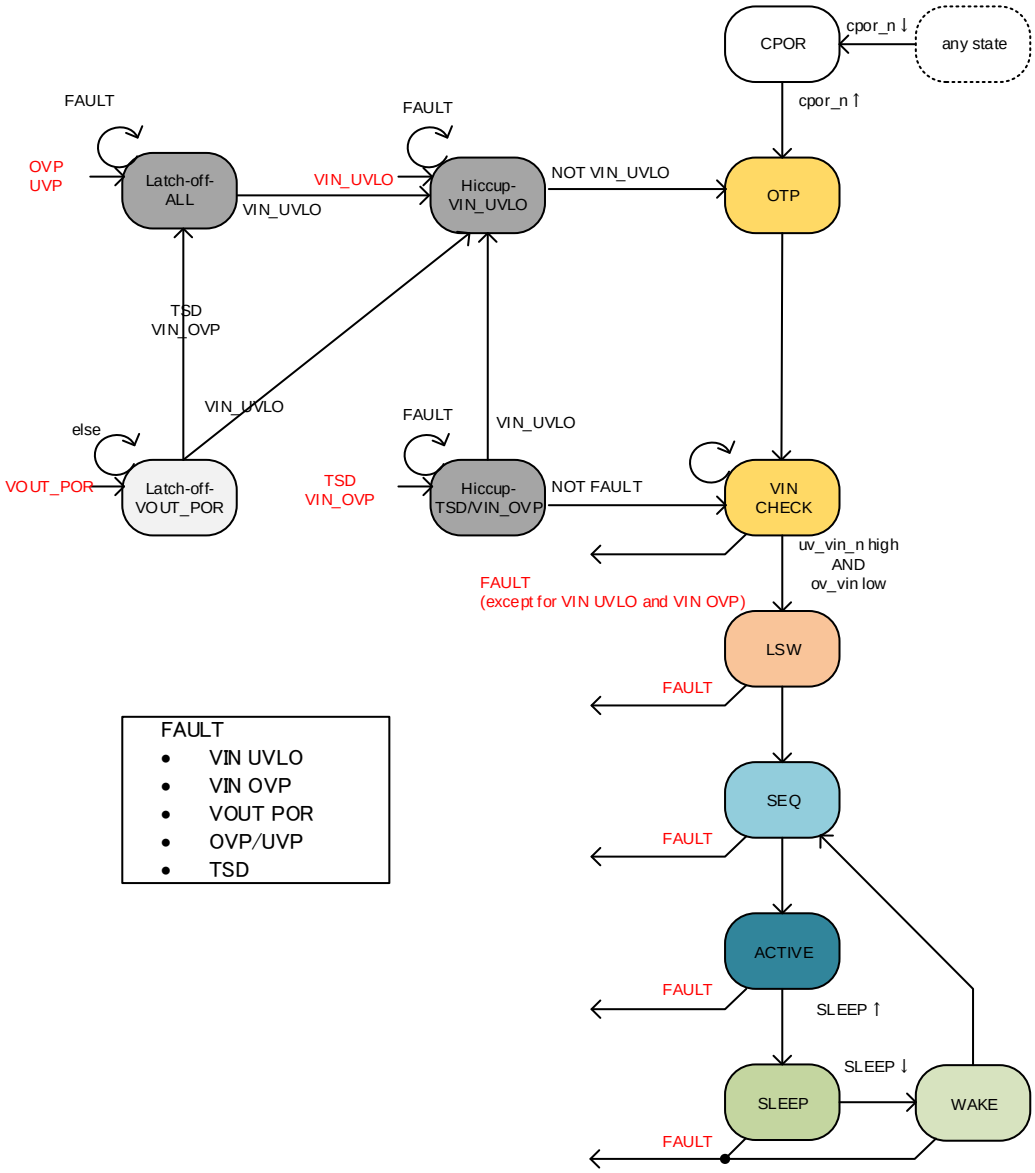


Figure 4: Function State Control Flow

Table 16: Function State

State Name	Function
CPOR	Enter this state when VIN < CPOR (2.0 V). All registers are cleared. (Digital hardware reset)
OTP	Initialize registers by loading OTP contents. Clear all the fault event bits (VOUT POR, OVPs, UVPs and TSD) for transition from Hiccup-VIN_UVLO.
VIN CHECK	Check VIN level and wait until it is within the appropriate range.
LSW	Activate LSW

State Name	Function
SEQ	Activate Buck CH<x> and LDO. Then assert POR pin.
ACTIVE	All rails active, wait for SLEEP command.
SLEEP	Shutdown rails by SLEEP command.
WAKE	Activate rails by WAKE command.
Latch-Off-ALL	Latch-off all rails (CH<x>, LDO, LSW, and POR = L).
Latch-Off-VOUT_POR	Latch-off rails except for LSW (CH<x>, LDO, and POR = L).
Hiccup-VIN_UVLO	Hiccup all rails (CH<x>, LDO, LSW, and POR = L) and go to RESET (OTP) state.
Hiccup-TSD/VIN_OVP	Hiccup all rails (CH<x>, LDO, LSW, and POR = L) and go to Non Reset (VIN CHECK).

6.2 Normal Sequence

6.2.1 Power On and Power Off Sequence

Power on and power off sequence can be configured by OTP. Wake-up timings of all buck converters and the LDO during power-on sequence are selectable from 15 time slots by PMC_CH<x>CH<y>_WAKEUP_TIME and PMC_LDO_WAKEUP_TIME registers. Each time slot is approximately 0.5 ms.

POR delay timing is programmed from 3 ms to 6 ms with 1 ms step.

For an example power on and power off sequence, see Figure 5. This sequence only works at start-up by power on.

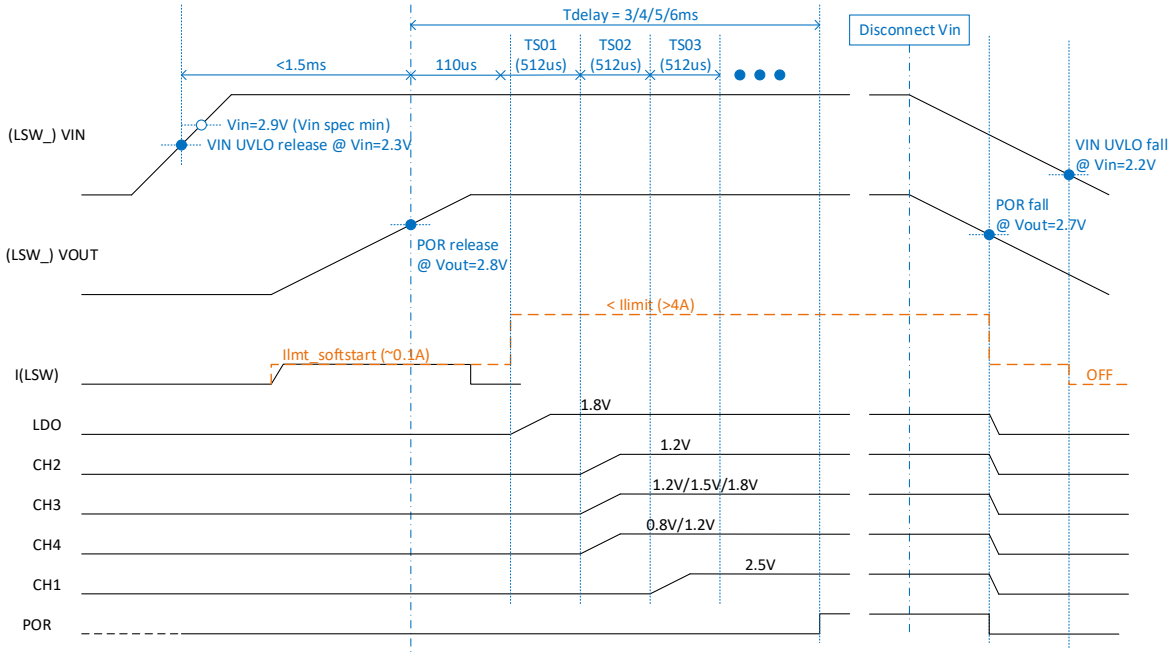


Figure 5: Power On and Off Sequence

NOTE
The LSW is enabled by default to allow the power sequencer to start, regardless of whether the CH<x> and LDO are supplied from VOUT (LSW) or from a different power source.

6.2.2 Sleep Mode Enter and Exit Sequence

DA9083 enters Sleep mode immediately when SLEEP bit of PMC_SLEEP_REG0 register is asserted. All the buck converters and the LDO move to their SLEEP state according to CH<x>_ALIVE and LDO_ALIVE bits of PMC_SLEEP_REG0. Some of them are disabled and the others are in Low Power mode (LPM).

DA9083 exits Sleep mode when SLEEP bit of PMC_SLEEP_REG0 register is negated. Wake-up delays of disabled buck converters and LDO are the same as power-on sequence.

For an example sleep enter and exit sequence, see Figure 6. CH2 wakes up in TS02 and CH1 wakes up in TS03.

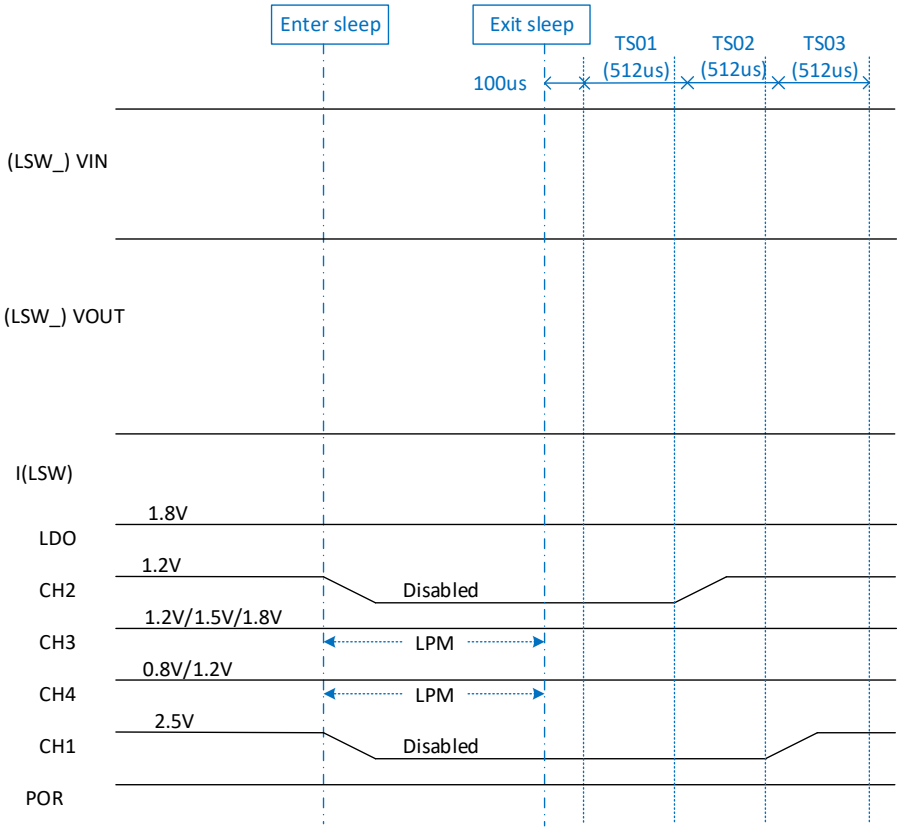


Figure 6: Sleep Enter and Exit Sequence

6.3 Fault and Protection

Protection functions are triggered by fault events. The behavior depends on type of fault event, see Table 17.

Table 17: Fault Events and Protection Functions

Fault Events	Shut-Down Blocks	Recovery from Shut-Down	Register
OCP	None	N/A	N/A
POR (LSW VOUT)	CH1-4 Buck, LDO	Latch-off	Keep
OVP (Buck and LDO)	CH1 Buck to CH4 Buck, LDO, LSW	Latch-off	Keep
UVP (Buck and LDO)	CH1 Buck to CH4 Buck, LDO, LSW	Latch-off	Keep
VIN OVP	CH1 Buck to CH4 Buck, LDO, LSW	Hiccup	Keep
VIN UVLO	CH1 Block to CH4 Block, LDO, LSW	Hiccup	Reset

Fault Events	Shut-Down Blocks	Recovery from Shut-Down	Register
TSD	CH1 Block to CH4 Block, LDO, LSW	Hiccup	Keep

As an OTP option, POR pin can be assigned as IRQ output (open-drain, active high). In this case, fault events such as over-current, over-voltage, under-voltage, and/or over-temperature can be set to trigger IRQ.

NOTE
When DA9083 is in Latch-Off-ALL or Latch-Off-VOUT_POR state, a VIN UVLO event is necessary to send the device back to ACTIVE.

6.4 Buck Converters

DA9083 has four channels of switching buck converters, CH1 Buck to CH4 Buck. Each of the bucks has an I²C programable voltage register, PMC_CH<x>_SEL_REG, which defines the output voltage.

When a buck is enabled, its output voltage gradually goes up with soft-start. When the buck output reaches the target voltage, Power Good condition is shown via the CH<x>_NT_UV_OV status bit in PMC_RAIL_STATUS_REG1 register.

When the buck output drops below $V_{THR\_UVP\_FALL}$, the device sets the CH<x>_UV bit in the PMC_RAIL_STATUS_REG2 register to 0x1. When the buck output increases above $V_{THR\_OVP\_RISE}$ the device sets the CH<x>_OV bit in the PMC_RAIL_STATUS_REG3 register to 0x1. The status of the Power Good indicator, for both a UVP event and an OVP event and for each of the buck converters, can be read back via I²C from the CH<x>_NT_UV_OV, CH<x>_UV, and CH<x>_OV bits.

The Power Good status on each of buck converter is masked during the buck start-up period.

The buck converters support DVC, with the following features:

- When the value of the target voltage (PMC_CH<x>_SEL_REG) changes, the output voltage updates to the new target value.
- The DVC controller operates in pulse width modulation (PWM) mode with synchronous rectification. During DVC operation the PMC_RAIL_STATUS_REG1 register remains at 0xFC to indicate a Power Good condition.
- The slew rate of the DVC transition for each channel is programmed in bits CH<x>_TSTEP<1:0> in registers PMC_CH<x>_CFG_REG.

Each of the bucks has current limit and its threshold is programable with CH<x>_ILMAX<1:0> and OTP option.

A pull-down resistor for each channel is enabled when the channel is disabled. This feature can be disabled by setting register bits CH<x>_DIS to 0x0 (register PMC_DISCHARGE_REG0).

6.4.1 Buck Operation Mode

Buck operation modes are selected, via I²C, by bits CH<X>_ALIVE, LDO_ALIVE and SLEEP in the PMC_SLEEP_REG0 register. Operation mode of CH<X> during High Power mode is selected by CH<X>_PWM. See Table 18.

Table 18: Buck Operation Mode

Operation Mode	Buck Mode	
Normal mode	High Power mode (HPM)	Auto mode
		Force PWM mode
	Low Power mode (LPM)	
	Disable	
Sleep mode	Low Power mode (LPM)	
	Disable	

6.5 LDO

DA9083 has one LDO. It has an I²C programable voltage register (PMC_LDO_SEL_REG) which defines the output voltage. It has soft-start function and its output voltage gradually increases when the LDO is enabled.

When the output voltage reaches the target, a Power Good condition is shown via the LDO_NT_UV_OV status bit in the PMC_RAIL_STATUS_REG1 register. It indicates that the output voltage is higher than the under-voltage protection level ($V_{THR\_UVP\_FALL}$) and lower than the over-voltage protection threshold level ($V_{THR\_OVP\_RISE}$).

When the output drops below $V_{THR\_UVP\_FALL}$, the device sets the LDO_UV bit in the PMC_RAIL_STATUS_REG2 register to 0x1. When the output exceeds $V_{THR\_OVP\_RISE}$, the device sets the LDO_OV bit in the PMC_RAIL_STATUS_REG3 register to 0x1.

The status of the Power Good indicator, UVP event, and OVP event of the LDO can be read via I²C from the LDO_NT_UV_OV, LDO_UV, and LDO_OV bits respectively.

The Power Good status on LDO is masked during the buck start-up period.

6.6 I²C Communication

DA9083 includes an I²C-compatible 2-wire serial interface to access the internal registers. Through the I²C interface, the host processor controls each channel and reads back system status. The DA9083 only operates as a slave device. For detailed information about each register, refer to Section 7 and Section 7.2.

The host processor provides the serial clock at the SCL pin. DA9083 supports I²C Standard-mode at 100 kHz and Fast-mode at 400 kHz, see [1].

DA9083 SLAVE address (7-bit) is 0x1B (or 0x36 on 8-bit)

The I²C data pin, SDA, is open drain which allows multiple devices to share a communication line.

All transmissions begin with a START condition issued from the Master while the bus is in an IDLE state (the bus is free). The START condition is initiated by a high to low transition on SDA while SCL is high. Alternately, a STOP condition is indicated by a low to high transition on SDA while SCL is high, see Figure 7.

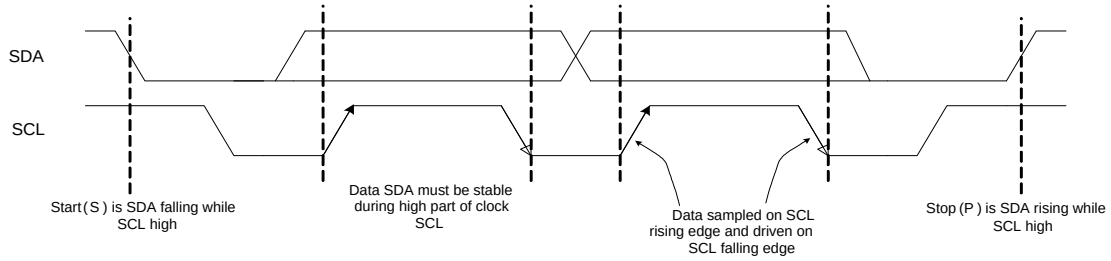


Figure 7: I²C Start (S) and Stop (P)

The I²C interface uses a two-byte serial protocol containing one byte for address and one byte for data. The data and address are transferred with MSB transmitted first for both read and write operations.

DA9083 monitors the serial bus for a valid SLAVE address when the interface is enabled. When it receives its own slave address, DA9083 immediately gives an Acknowledge signal to the host by pulling SDA low during the following clock cycle. A Not Acknowledge signal is given by a logic 1, not pulling down the SDA line.

A single-byte write is shown in Figure 8. Here the slave address is followed by a write bit (low), the register address, and the write data. Finally, the transaction is terminated with a STOP.

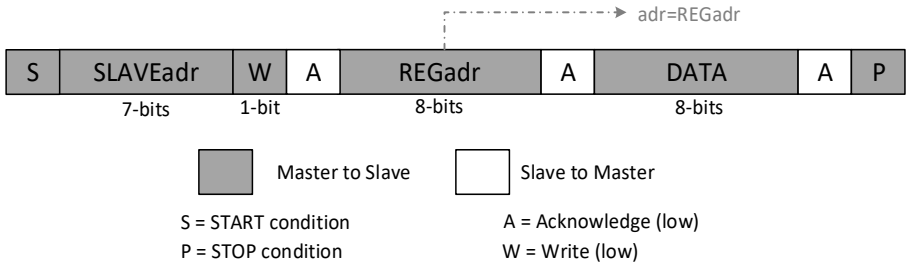


Figure 8: Single Write Command

DA9083 also supports multiple byte writes, shown in Figure 9. By not sending the STOP command, data is written to consecutive addresses.

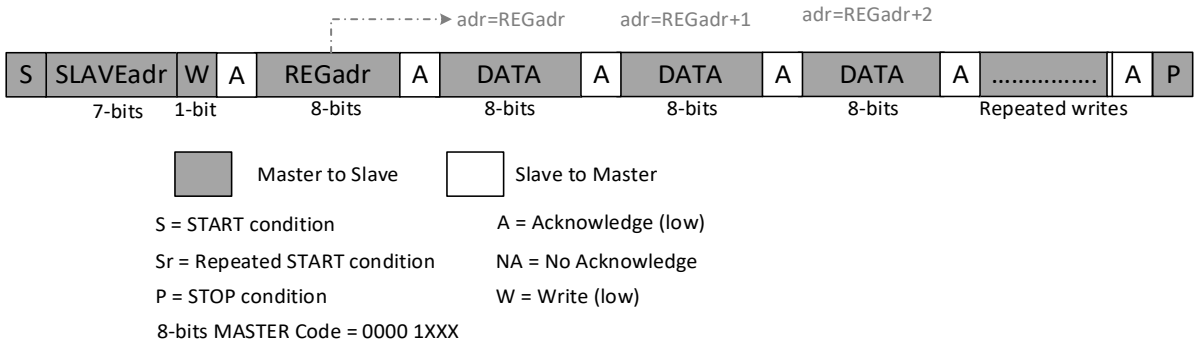


Figure 9: Consecutive Write Command

The data read protocol differs from the write protocol. A read does not have a register address immediately preceding it. To read from a specific address, the register address is given by using a write command followed by a Repeated START. A single-byte read is shown in Figure 10. A Repeated START is followed by the slave address and a read bit. After the read data is returned to the host, the host then responds with a Not Acknowledge and a STOP.

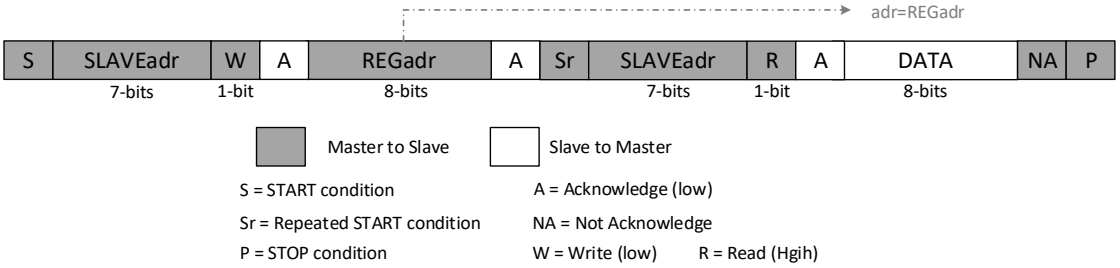


Figure 10: Single Read Command

The DA9083 also supports a multiple byte read protocol. If the host responds to the returned data with an Acknowledge rather than Not Acknowledge and STOP, data will be read from sequential addresses until a Not Acknowledge and STOP command is given, as shown in Figure 11. If a read address is given with a write and Repeated START, consecutive addresses are read from the write address.

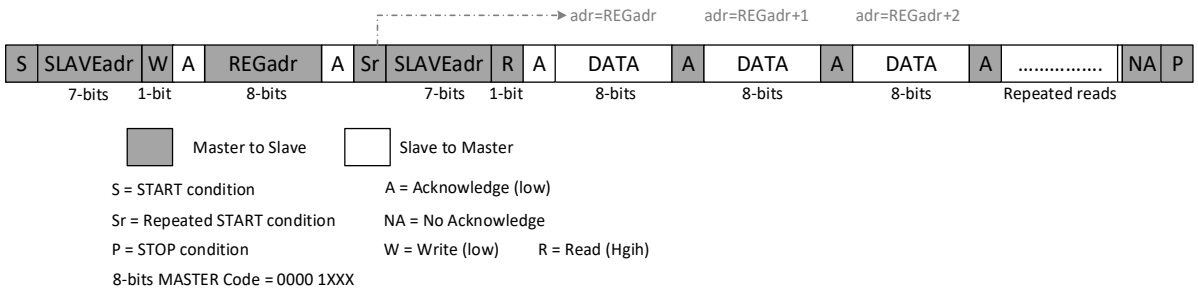


Figure 11: Consecutive Read Command

DA9083 also supports I²C High-Speed mode (HS-mode), which can transfer information at bit rates of up to 3.4 Mbit/s, see [1].

Operation in High Speed mode at 3.4 MHz requires a mode change to enable spike suppression and slope control characteristics compatible with the I²C-bus specification. High-Speed mode can be enabled on a transfer-by-transfer basis by sending the master code (0000 1XXX) at the beginning of the transfer. DA9083 does not make use of clock stretching and delivers read data without additional delay up to 3.4 MHz.

A single-byte write with High-Speed mode is shown in Figure 12. Here the slave address is followed by a write bit (low), the register address, and the write data. Finally, the transaction is terminated with a STOP.

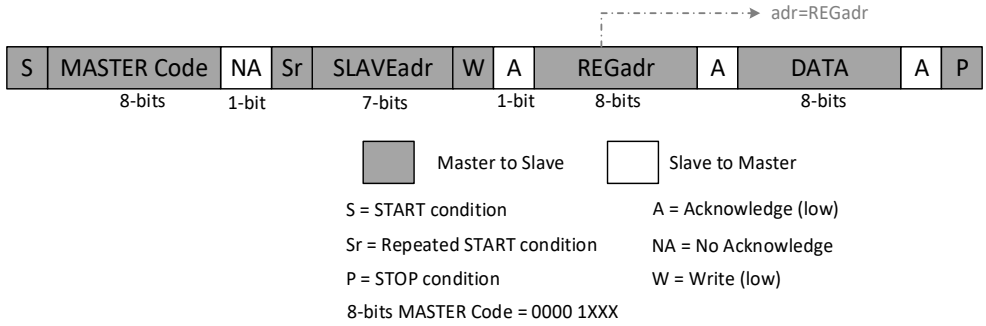


Figure 12: High-Speed-Mode Single Write Command

DA9083 also supports multiple byte writes in High-Speed mode, see Figure 13. By not sending the STOP command, data is written to consecutive addresses.

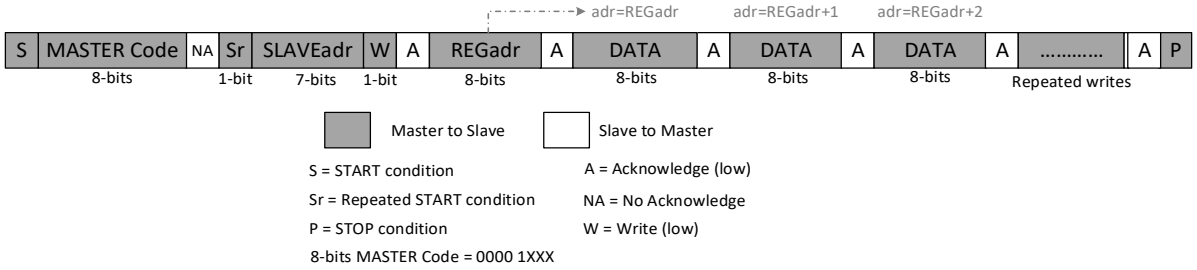


Figure 13: HS-Mode Consecutive Write Command

The data read protocol in High-Speed mode differs in that a read does not have a register address, immediately preceding it. To read from a specific address, the register address is given by using a write command followed by a Repeated START. A single byte read is shown in Figure 14. A Repeated START is followed by the slave address and a read bit. After the read data is returned to the host, the host then responds with a Not Acknowledge and a STOP.

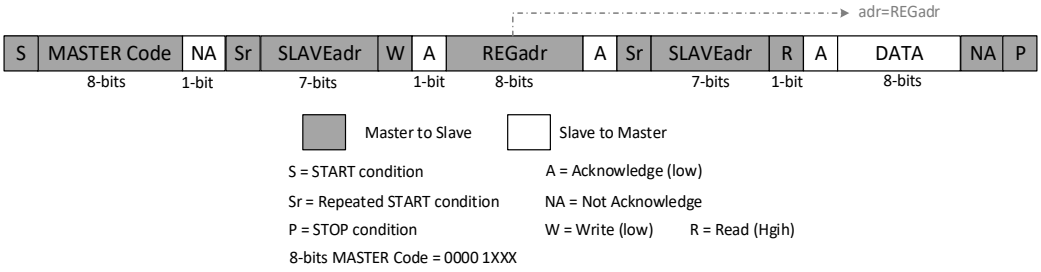


Figure 14: HS-Mode Single Read Command

The DA9083 also supports a multiple byte read protocol in High-Speed mode. If the host responds to the returned data with an Acknowledge rather than Not Acknowledge and STOP, data will be read from sequential addresses until a Not Acknowledge and STOP command is given, see Figure 15. If a read address is given with a write and Repeated START, consecutive addresses are read from the write address.

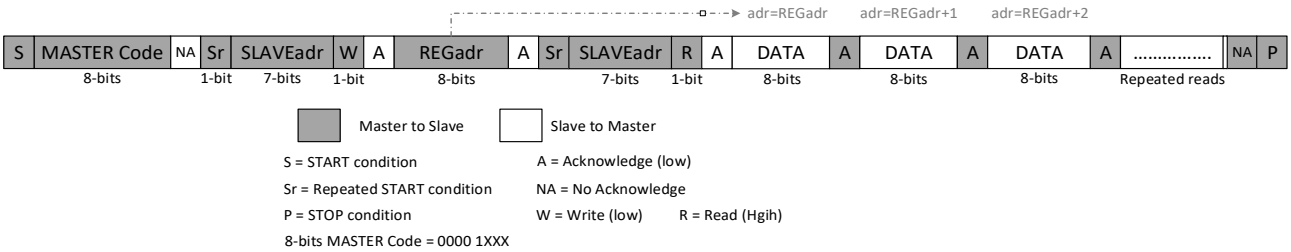


Figure 15: High-Speed Mode Consecutive Read Command

7. Register Definitions

NOTE

The following register fields are password protected.

- PMC_IRQ_MASK0
- PMC_IRQ_MASK1
- PMC_IRQ_MASK2
- PMC_OPTION_06
- CH1_EN_DIVIDER
- CH2_EN_DIVIDER
- CH3_EN_DIVIDER
- CH4_EN_DIVIDER

I^2C access is required to unlock those bits. Send this succession of writes:

WRITE DA9083_I2C 0x005D 0x00
WRITE DA9083_I2C 0x005E 0xB0
WRITE DA9083_I2C 0x005E 0xA9
WRITE DA9083_I2C 0x005E 0x8A
WRITE DA9083_I2C 0x005E 0xA7
WRITE DA9083_I2C 0x005E 0xA8
WRITE DA9083_I2C 0x005E 0xB1

To lock those register fields, send this succession of writes:

WRITE DA9083_I2C 0x005D 0x00
WRITE DA9083_I2C 0x005E 0x00

7.1 Register Map

Addr	Register	7	6	5	4	3	2	1	0	Reset
Functional Registers										
PMIC Function Registers										
0x0000	PMC_RAIL_STATUS_REG1	CH1_NT_UV_OV	CH2_NT_UV_OV	CH3_NT_UV_OV	CH4_NT_UV_OV	LDO_NT_UV_OV	POR	Reserved	Reserved	0x00
0x0001	PMC_RAIL_STATUS_REG2	CH1_UV	CH2_UV	CH3_UV	CH4_UV	LDO_UV	Reserved	Reserved	Reserved	0x00
0x0002	PMC_RAIL_STATUS_REG3	CH1_OV	CH2_OV	CH3_OV	CH4_OV	LDO_OV	VIN_OV	PMIC_OT	Reserved	0x00
0x0003	PMC_CH1_CFG_REG	CH1_ILMAX<1:0>		CH1_TSTEP<1:0>		CH1_FREQ<2:0>			Reserved	0x6A
0x0005	PMC_CH2_CFG_REG	CH2_ILMAX<1:0>		CH2_TSTEP<1:0>		CH2_FREQ<2:0>			Reserved	0x6A
0x0007	PMC_CH3_CFG_REG	CH3_ILMAX<1:0>		CH3_TSTEP<1:0>		CH3_FREQ<2:0>			Reserved	0x6A
0x0009	PMC_CH4_CFG_REG	CH4_ILMAX<1:0>		CH4_TSTEP<1:0>		CH4_FREQ<2:0>			Reserved	0xAA
0x000B	PMC_LDO_SEL_REG	LDO_SEL<4:0>					Reserved	Reserved	Reserved	0xA0
0x000F	PMC_DCDCCTRL0_REG0	LSW_EN	CH1_EN	Reserved	CH2_EN	CH3_EN	CH4_EN	LDO_EN	Reserved	0x00
0x0010	PMC_SLEEP_REG0	CH1_ALIVE	Reserved	CH2_ALIVE	CH3_ALIVE	CH4_ALIVE	LDO_ALIVE	Reserved	SLEEP	0x1C
0x0011	PMC_DCDCCTRL1_REG	CH1_PWM	CH2_PWM	CH3_PWM	CH4_PWM	Reserved	Reserved	Reserved	Reserved	0x00
0x0012	PMC_DISCHARGE_REG0	CH1_DIS	CH2_DIS	CH3_DIS	CH4_DIS	LDO_DIS	LSW_DIS	Reserved	Reserved	0xF8
0x0013	PMC_DCDCCTRL2_REG	CH1_LPM	Reserved	CH2_LPM	CH3_LPM	CH4_LPM	LDO_LPM	Reserved	Reserved	0x00
0x0014	PMC_CH1CH2_WAKEUP_TIME	CH1_WAKEUP_TIME<3:0>				CH2_WAKEUP_TIME<3:0>				0x32
0x0015	PMC_CH3CH4_WAKEUP_TIME	CH3_WAKEUP_TIME<3:0>				CH4_WAKEUP_TIME<3:0>				0x22
0x0016	PMC_LDO_WAKEUP_TIME	LDO_WAKEUP_TIME<3:0>				Reserved	Reserved	Reserved	Reserved	0x10
0x001A	PMC_IRQ_EVENT0	E_CH1_OC	E_CH2_OC	E_CH3_OC	E_CH4_OC	E_LDO_OC	E_LSW_OC	E_POR	Reserved	0x00
0x001B	PMC_IRQ_MASK0	M_CH1_UV	M_CH2_UV	M_CH3_UV	M_CH4_UV	M_LDO_UV	Reserved	Reserved	Reserved	0x00
0x001C	PMC_IRQ_MASK1	M_CH1_OV	M_CH2_OV	M_CH3_OV	M_CH4_OV	M_LDO_OV	M_VIN_OV	M_PMIC_OT	Reserved	0x00
0x001D	PMC_IRQ_MASK2	M_CH1_OC	M_CH2_OC	M_CH3_OC	M_CH4_OC	M_LDO_OC	M_LSW_OC	M_POR	Reserved	0x00
0x001E	PMC_VOUT_CH1	CH1_VOUT<7:0>								0x55
0x001F	PMC_VOUT_CH2	CH2_VOUT<7:0>								0x6E
0x0020	PMC_VOUT_CH3	CH3_VOUT<7:0>								0x6E
0x0021	PMC_VOUT_CH4	CH4_VOUT<7:0>								0x46
0x002E	PMC_OPTION_03	CH1_PHASE	CH2_PHASE					CH3_PHASE	CH4_PHASE	0x00
0x0031	PMC_OPTION_06	Reserved	Reserved	Reserved	Reserved	Reserved	ASSP_IRQ	Reserved	Reserved	0x19
0x004C	CH1_EN_DIVIDER	Reserved	CH1_EN_DIVIDER	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00

Addr	Register	7	6	5	4	3	2	1	0	Reset
0x004D	CH2_EN_DIVIDER	Reserved	CH2_EN_DIVIDER	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x004E	CH3_EN_DIVIDER	Reserved	CH3_EN_DIVIDER	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x004F	CH4_EN_DIVIDER	Reserved	CH4_EN_DIVIDER	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00

7.2 Register Descriptions

7.2.1 PMIC Function Registers

Table 19: PMC_RAIL_STATUS_REG1 (0x0000)

Bit	Type	Field Name	Description	Reset
[7]	R	CH1_NT_UV_OV	Status bit. Indicates UV/OV not triggered on CH1 **Value** **Description** 0x0 CH1 OV or UV triggered. 0x1 CH1 OV and UV not triggered.	0x0
[6]	R	CH2_NT_UV_OV	Status bit. Indicates UV/OV not triggered on CH2 **Value** **Description** 0x0 CH2 OV or UV triggered. 0x1 CH2 OV and UV not triggered.	0x0
[5]	R	CH3_NT_UV_OV	Status bit. Indicates UV/OV not triggered on CH3 **Value** **Description** 0x0 CH3 OV or UV triggered. 0x1 CH3 OV and UV not triggered.	0x0
[4]	R	CH4_NT_UV_OV	Status bit. Indicates UV/OV not triggered on CH4 **Value** **Description** 0x0 CH4 OV or UV triggered. 0x1 CH4 OV and UV not triggered.	0x0
[3]	R	LDO_NT_UV_OV	Status bit. Indicates UV/OV not triggered on LDO **Value** **Description** 0x0 LDO OV or UV triggered. 0x1 LDO OV and UV not triggered.	0x0
[2]	R	POR	Status bit. Indicates POR pin output. **Value** **Description** 0x0 POR pin low 0x1 POR pin high	0x0

Table 20: PMC_RAIL_STATUS_REG2 (0x0001)

Bit	Type	Field Name	Description	Reset
[7]	RW1C	CH1_UV	Status bit. Indicates UV on CH1 **Value** **Description** 0x0 CH1 UV not breached 0x1 CH1 UV breached	0x0
[6]	RW1C	CH2_UV	Status bit. Indicates UV on CH2 **Value** **Description** 0x0 CH2 UV not breached	0x0

Bit	Type	Field Name	Description	Reset
			0x1 CH2 UV breached	
[5]	RW1C	CH3_UV	Status bit. Indicates UV on CH3 **Value** **Description** 0x0 CH3 UV not breached 0x1 CH3 UV breached	0x0
[4]	RW1C	CH4_UV	Status bit. Indicates UV on CH4 **Value** **Description** 0x0 CH4 UV not breached 0x1 CH4 UV breached	0x0
[3]	RW1C	LDO_UV	Status bit. Indicates UV on LDO **Value** **Description** 0x0 LDO UV not breached 0x1 LDO UV breached	0x0

Table 21: PMC_RAIL_STATUS_REG3 (0x0002)

Bit	Type	Field Name	Description	Reset
[7]	RW1C	CH1_OV	Status bit. Indicates OV on CH1 **Value** **Description** 0x0 CH1 OV not breached 0x1 CH1 OV breached	0x0
[6]	RW1C	CH2_OV	Status bit. Indicates OV on CH2 **Value** **Description** 0x0 CH2 OV not breached 0x1 CH2 OV breached	0x0
[5]	RW1C	CH3_OV	Status bit. Indicates OV on CH3 **Value** **Description** 0x0 CH3 OV not breached 0x1 CH3 OV breached	0x0
[4]	RW1C	CH4_OV	Status bit. Indicates OV on CH4 **Value** **Description** 0x0 CH4 OV not breached 0x1 CH4 OV breached	0x0
[3]	RW1C	LDO_OV	Status bit. Indicates OV on LDO **Value** **Description** 0x0 LDO OV not breached 0x1 LDO OV breached	0x0
[2]	RW1C	VIN_OV	Status bit. Indicates OV on VIN **Value** **Description** 0x0 VIN OV not breached	0x0

Bit	Type	Field Name	Description	Reset
			0x1 VIN OV breached	
[1]	RW1C	PMIC_OT	Status bit. Indicates OT on PMIC **Value** **Description** 0x0 PMIC OT not breached 0x1 PMIC OT breached	0x0

Table 22: PMC_CH1_CFG_REG (0x0003)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	CH1_ILMAX	CH1 ILMAX setting (A) **Value** **Description** 0x0 3.0 0x1 4.0 0x2 5.0 0x3 6.0	0x1
[5:4]	RW	CH1_TSTEP	CH1 TSTEP setting **Value** **Description** 0x0 up: 20 mV/µs, down: 5m V/µs 0x1 up: 15 mV/µs, down: 5mV/µs 0x2 up: 10mV/µs, down: 5mV/µs 0x3 up: 5mV/µs, down: 5mV/µs	0x2
[3:1]	RW	CH1_FREQ	CH1 FREQ is fixed to 2 MHz	0x5

Table 23: PMC_CH2_CFG_REG (0x0005)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	CH2_ILMAX	CH2 ILMAX setting (A) **Value** **Description** 0x0 3.0 0x1 4.0 0x2 5.0 0x3 6.0	0x1
[5:4]	RW	CH2_TSTEP	CH2 TSTEP setting **Value** **Description** 0x0 up: 20 mV/µs, down: 5 mV/µs 0x1 up: 15mV/µs, down: 5mV/µs 0x2 up: 10mV/µs, down: 5mV/µs 0x3 up: 5mV/µs, down: 5mV/µs	0x2
[3:1]	RW	CH2_FREQ	CH2 FREQ is fixed to 2 MHz	0x5

Table 24: PMC_CH3_CFG_REG (0x0007)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	CH3_ILMAX	CH3 ILMAX setting (A) **Value** **Description** 0x0 3.0 0x1 4.0 0x2 5.0 0x3 6.0	0x1
[5:4]	RW	CH3_TSTEP	CH3 TSTEP setting **Value** **Description** 0x0 up: 20 mV/µs, down: 5 mV/µs 0x1 up: 15 mV/µs, down: 5 mV/µs 0x2 up: 10 mV/µs, down: 5 mV/µs 0x3 up: 5 mV/µs, down:5 mV/µs	0x2
[3:1]	RW	CH3_FREQ	CH3 FREQ is fixed to 2 MHz	0x5

Table 25: PMC_CH4_CFG_REG (0x0009)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	CH4_ILMAX	CH4 ILMAX setting (A) **Value** **Description** 0x0 5.5 0x1 7.0 0x2 8.5 0x3 10.0	0x2
[5:4]	RW	CH4_TSTEP	CH4 TSTEP setting **Value** **Description** 0x0 up: 20 mV/µs, down: 5 mV/µs 0x1 up: 15 mV/µs, down: 5 mV/µs 0x2 up: 10 mV/µs, down: 5 mV/µs 0x3 up: 5 mV/µs, down: 5 mV/µs	0x2
[3:1]	RW	CH4_FREQ	CH4 FREQ is fixed to 2 MHz	0x5

Table 26: PMC_LDO_SEL_REG (0x000B)

Bit	Type	Field Name	Description	Reset
[7:3]	RW	LDO_SEL	LDO output voltage (V). **Value** **Description** 0x00 1.40 0x01 1.42 0x02 1.44 0x03 1.46 0x04 1.48	0x14

Bit	Type	Field Name	Description	Reset
			0x05 1.50 0x06 1.52 0x07 1.54 0x08 1.56 0x09 1.58 0x0A 1.60 0x0B 1.62 0x0C 1.64 0x0D 1.66 0x0E 1.68 0x0F 1.70 0x10 1.72 0x11 1.74 0x12 1.76 0x13 1.78 0x14 1.80 0x15 1.82 0x16 1.84 0x17 1.86 0x18 1.88 0x19 1.90 0x1A 1.90 0x1F 1.90	

Table 27: PMC_DCDCCTRL0_REG0 (0x000F)

Bit	Type	Field Name	Description	Reset
[7]	RW	LSW_EN	LSW enable **Value** **Description** 0x0 Disable 0x1 Enable	0x0
[6]	RW	CH1_EN	CH1 Buck enable **Value** **Description** 0x0 Disable 0x1 Enable	0x0
[4]	RW	CH2_EN	CH2 Buck enable **Value** **Description** 0x0 Disable 0x1 Enable	0x0
[3]	RW	CH3_EN	CH3 Buck enable	0x0

Bit	Type	Field Name	Description	Reset
			Value **Description** 0x0 Disable 0x1 Enable	
[2]	RW	CH4_EN	CH4 Buck enable **Value** **Description** 0x0 Disable 0x1 Enable	0x0
[1]	RW	LDO_EN	LDO enable **Value** **Description** 0x0 Disable 0x1 Enable	0x0

Table 28: PMC_SLEEP_REG0 (0x0010)

Bit	Type	Field Name	Description	Reset
[7]	RW	CH1_ALIVE	Set CH1 Buck operation during sleep. **Value** **Description** 0x0 When Sleep, CH1 turn off 0x1 When Sleep, CH1 alive and enter LPM	0x0
[5]	RW	CH2_ALIVE	Set CH2 Buck operation during sleep. **Value** **Description** 0x0 When Sleep, CH2 turn off 0x1 When Sleep, CH2 alive and enter LPM	0x0
[4]	RW	CH3_ALIVE	Set CH3 Buck operation during sleep. **Value** **Description** 0x0 When Sleep, CH3 turn off 0x1 When Sleep, CH3 alive and enter LPM	0x1
[3]	RW	CH4_ALIVE	Set CH4 Buck operation during sleep. **Value** **Description** 0x0 When Sleep, CH4 turn off 0x1 When Sleep, CH4 alive and enter LPM	0x1
[2]	RW	LDO_ALIVE	Set LDO operation during sleep. **Value** **Description** 0x0 When Sleep, LDO turn off 0x1 When Sleep, LDO alive and enter LPM	0x1
[0]	RW	SLEEP	Sleep mode setting **Value** **Description** 0x0 Exit Sleep mode 0x1 Enter Sleep mode	0x0

Table 29: PMC_DCDCCTRL1_REG (0x0011)

Bit	Type	Field Name	Description	Reset
[7]	RW	CH1_PWM	CH1 operation mode while not in LPM **Value** **Description** 0x0 Auto mode 0x1 Forced PWM mode	0x0
[6]	RW	CH2_PWM	CH2 operation mode while not in LPM **Value** **Description** 0x0 Auto mode 0x1 Forced PWM mode	0x0
[5]	RW	CH3_PWM	CH3 operation mode while not in LPM **Value** **Description** 0x0 Auto mode 0x1 Forced PWM mode	0x0
[4]	RW	CH4_PWM	CH4 operation mode while not in LPM **Value** **Description** 0x0 Auto mode 0x1 Forced PWM mode	0x0

Table 30: PMC_DISCHARGE_REG0 (0x0012)

Bit	Type	Field Name	Description	Reset
[7]	RW	CH1_DIS	Enable discharge of CH1 output while channel is disabled **Value** **Description** 0x0 Discharge disabled 0x1 Discharge enabled	0x1
[6]	RW	CH2_DIS	Enable discharge of CH2 output while channel is disabled **Value** **Description** 0x0 Discharge disabled 0x1 Discharge enabled	0x1
[5]	RW	CH3_DIS	Enable discharge of CH3 output while channel is disabled **Value** **Description** 0x0 Discharge disabled 0x1 Discharge enabled	0x1
[4]	RW	CH4_DIS	Enable discharge of CH4 output while channel is disabled **Value** **Description** 0x0 Discharge disabled 0x1 Discharge enabled	0x1
[3]	RW	LDO_DIS	Enable discharge of LDO output while channel is disabled **Value** **Description** 0x0 Discharge disabled	0x1

Bit	Type	Field Name	Description		Reset
			0x1	Discharge enabled	
[2]	RW	LSW_DIS	Enable discharge of LSW output while channel is disabled **Value** **Description** 0x0 Discharge disabled 0x1 Discharge enabled		0x0

Table 31: PMC_DCDCCTRL2_REG (0x0013)

Bit	Type	Field Name	Description		Reset
[7]	RW	CH1_LPM	CH1 Buck LPM mode **Value** **Description** 0x0 High Power mode 0x1 Low Power mode		0x0
[5]	RW	CH2_LPM	CH2 Buck LPM mode **Value** **Description** 0x0 High Power mode 0x1 Low Power mode		0x0
[4]	RW	CH3_LPM	CH3 Buck LPM mode **Value** **Description** 0x0 High Power mode 0x1 Low Power mode		0x0
[3]	RW	CH4_LPM	CH4 Buck LPM mode **Value** **Description** 0x0 High Power mode 0x1 Low Power mode		0x0
[2]	RW	LDO_LPM	LDO Buck LPM mode **Value** **Description** 0x0 High Power mode 0x1 Low Power mode		0x0

Table 32: PMC_CH1CH2_WAKEUP_TIME (0x0014)

Bit	Type	Field Name	Description		Reset
[7:4]	RW	CH1_WAKEUP_TIME	The duration between wake-up signal and a rail rising edge, $t_{WAKE\_UP\_DELAY}$ = 150 µs + (N-1) * 512 µs **Value** **Description** 0x0 Disable wake-up 0x1 Time slot 1 0x2 Time slot 2 0x3 Time slot 3 0x4 Time slot 4		0x3

Bit	Type	Field Name	Description	Reset
			0x5 Time slot 5 0x6 Time slot 6 0x7 Time slot 7 0x8 Time slot 8 0x9 Time slot 9 0xA Time slot 10 0xB Time slot 11 0xC Time slot 12 0xD Time slot 13 0xE Time slot 14 0xF Time slot 15	
[3:0]	RW	CH2_WAKEUP_TIME	The duration between wake-up signal and a rail rising edge, $t_{WAKE\_UP\_DELAY}$ = 150µs + (N-1) * 512 µs **Value Description** 0x0 Disable wake-up 0x1 Time slot 1 0x2 Time slot 2 0x3 Time slot 3 0x4 Time slot 4 0x5 Time slot 5 0x6 Time slot 6 0x7 Time slot 7 0x8 Time slot 8 0x9 Time slot 9 0xA Time slot 10 0xB Time slot 11 0xC Time slot 12 0xD Time slot 13 0xE Time slot 14 0xF Time slot 15	0x2

Table 33: PMC_CH3CH4_WAKEUP_TIME (0x0015)

Bit	Type	Field Name	Description	Reset
[7:4]	RW	CH3_WAKEUP_TIME	The duration between wake-up signal and a rail rising edge, $t_{WAKE\_UP\_DELAY}$ = 150 µs + (N-1) * 512 µs **Value Description** 0x0 Disable wake-up 0x1 Time slot 1 0x2 Time slot 2 0x3 Time slot 3	0x2

Bit	Type	Field Name	Description	Reset
			0x4 Time slot 4 0x5 Time slot 5 0x6 Time slot 6 0x7 Time slot 7 0x8 Time slot 8 0x9 Time slot 9 0xA Time slot 10 0xB Time slot 11 0xC Time slot 12 0xD Time slot 13 0xE Time slot 14 0xF Time slot 15	
[3:0]	RW	CH4_WAKEUP_TIME	The duration between wake-up signal and a rail rising edge, $t_{WAKE\_UP\_DELAY}$ = 150 µs + (N-1) * 512 µs **Value** **Description** 0x0 Disable wake-up 0x1 Time slot 1 0x2 Time slot 2 0x3 Time slot 3 0x4 Time slot 4 0x5 Time slot 5 0x6 Time slot 6 0x7 Time slot 7 0x8 Time slot 8 0x9 Time slot 9 0xA Time slot 10 0xB Time slot 11 0xC Time slot 12 0xD Time slot 13 0xE Time slot 14 0xF Time slot 15	0x2

Table 34: PMC_LDO_WAKEUP_TIME (0x0016)

Bit	Type	Field Name	Description	Reset
[7:4]	RW	LDO_WAKEUP_TIME	The duration between wake-up signal and a rail rising edge, $t_{WAKE\_UP\_DELAY}$ = 150 µs + (N-1) * 512 µs **Value** **Description** 0x0 Disable wake-up 0x1 Time slot 1	0x1

Bit	Type	Field Name	Description	Reset
			0x2 Time slot 2 0x3 Time slot 3 0x4 Time slot 4 0x5 Time slot 5 0x6 Time slot 6 0x7 Time slot 7 0x8 Time slot 8 0x9 Time slot 9 0xA Time slot 10 0xB Time slot 11 0xC Time slot 12 0xD Time slot 13 0xE Time slot 14 0xF Time slot 15	

Table 35: PMC_IRQ_EVENT0 (0x001A)

Bit	Type	Field Name	Description	Reset
[7]	RW	E_CH1_OC	Event bit. Indicates OC on CH1 **Value Description** 0x0 CH1 OC not breached 0x1 CH1 OC breached	0x0
[6]	RW	E_CH2_OC	Event bit. Indicates OC on CH2 **Value Description** 0x0 CH2 OC not breached 0x1 CH2 OC breached	0x0
[5]	RW	E_CH3_OC	Event bit. Indicates OC on CH3 **Value Description** 0x0 CH3 OC not breached 0x1 CH3 OC breached	0x0
[4]	RW	E_CH4_OC	Event bit. Indicates OC on CH4 **Value Description** 0x0 CH4 OC not breached 0x1 CH4 OC breached	0x0
[3]	RW	E_LDO_OC	Event bit. Indicates OC on LDO **Value Description** 0x0 LDO OC not breached 0x1 LDO OC breached	0x0
[2]	RW	E_LSW_OC	Event bit. Indicates OC on LSW **Value Description**	0x0

Bit	Type	Field Name	Description	Reset
			0x0 CH4 OC not breached 0x1 CH4 OC breached	
[1]	RW	E_POR	Event bit. Indicates a POR **Value** **Description** 0x0 POR not breached 0x1 POR OC breached	0x0

Table 36: PMC_IRQ_MASK0 (0x001B)

Bit	Type	Field Name	Description	Reset
[7]	RW	M_CH1_UV	IRQ mask bit for CH1_UV **Value** **Description** 0x0 CH1 UV not masked 0x1 CH1 UV masked	0x0
[6]	RW	M_CH2_UV	IRQ mask bit for CH2_UV **Value** **Description** 0x0 CH2 UV not masked 0x1 CH2 UV masked	0x0
[5]	RW	M_CH3_UV	IRQ mask bit for CH1_UV **Value** **Description** 0x0 CH3 UV not masked 0x1 CH3 UV masked	0x0
[4]	RW	M_CH4_UV	IRQ mask bit for CH1_UV **Value** **Description** 0x0 CH4 UV not masked 0x1 CH4 UV masked	0x0
[3]	RW	M_LDO_UV	IRQ mask bit for LDO_UV **Value** **Description** 0x0 LDO UV not masked 0x1 LDO UV masked	0x0

Table 37: PMC_IRQ_MASK1 (0x001C)

Bit	Type	Field Name	Description	Reset
[7]	RW	M_CH1_OV	IRQ mask bit for CH1_OV **Value** **Description** 0x0 CH1 OV not masked 0x1 CH1 OV masked	0x0
[6]	RW	M_CH2_OV	IRQ mask bit for CH2_OV **Value** **Description** 0x0 CH2 OV not masked	0x0

Bit	Type	Field Name	Description	Reset
			0x1 CH2 OV masked	
[5]	RW	M_CH3_OV	IRQ mask bit for CH3_OV **Value** **Description** 0x0 CH3 OV not masked 0x1 CH3 OV masked	0x0
[4]	RW	M_CH4_OV	IRQ mask bit for CH4_OV **Value** **Description** 0x0 CH4 OV not masked 0x1 CH4 OV masked	0x0
[3]	RW	M_LDO_OV	IRQ mask bit for LDO_OV **Value** **Description** 0x0 LDO OV not masked 0x1 LDO OV masked	0x0
[2]	RW	M_VIN_OV	IRQ mask bit for VIN_OV **Value** **Description** 0x0 VIN OV not masked 0x1 VIN OV masked	0x0
[1]	RW	M_PMIC_OT	IRQ mask bit for PMIC_OT **Value** **Description** 0x0 PMIC OT not masked 0x1 PMIC OT masked	0x0

Table 38: PMC_IRQ_MASK2 (0x001D)

Bit	Type	Field Name	Description	Reset
[7]	RW	M_CH1_OC	IRQ mask bit for E_CH1_OC **Value** **Description** 0x0 CH1 OC not masked 0x1 CH1 OC masked	0x0
[6]	RW	M_CH2_OC	IRQ mask bit for E_CH2_OC **Value** **Description** 0x0 CH2 OC not masked 0x1 CH2 OC masked	0x0
[5]	RW	M_CH3_OC	IRQ mask bit for E_CH3_OC **Value** **Description** 0x0 CH3 OC not masked 0x1 CH3 OC masked	0x0
[4]	RW	M_CH4_OC	IRQ mask bit for E_CH4_OC **Value** **Description** 0x0 CH4 OC not masked	0x0

Bit	Type	Field Name	Description	Reset
			0x1 CH4 OC masked	
[3]	RW	M_LDO_OC	IRQ mask bit for E_LDO_OC **Value** **Description** 0x0 LDO OC not masked 0x1 LDO OC masked	0x0
[2]	RW	M_LSW_OC	IRQ mask bit for E_LSW_OC **Value** **Description** 0x0 LSW OC not masked 0x1 LSW OC masked	0x0
[1]	RW	M_POR	IRQ mask bit for E_POR **Value** **Description** 0x0 POR not masked 0x1 POR masked	0x0

Table 39: PMC_VOUT_CH1 (0x001E)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	CH1_VOUT	CH1 output voltage (V). Format is (without divider)/(with divider). **Value** **Description** 0x00 Reserved 0x32 0.50/Reserved 0x33 0.51/Reserved 0x34 0.52/Reserved 0x35 0.53/Reserved 0x36 0.54/Reserved 0x37 0.55/Reserved 0x38 0.56/Reserved 0x39 0.57/Reserved 0x3A 0.58/Reserved 0x3B 0.59/Reserved 0x3C 0.60/Reserved 0x3D 0.61/Reserved 0x3E 0.62/Reserved 0x3F 0.63/Reserved 0x40 0.64/Reserved 0x41 0.65/Reserved 0x42 0.66/Reserved 0x43 0.67/Reserved	0x55

Bit	Type	Field Name	Description	Reset
			0x44 0.68/Reserved 0x45 0.69/Reserved 0x46 0.70/Reserved 0x47 0.71/Reserved 0x48 0.72/Reserved 0x49 0.73/Reserved 0x4A 0.74/Reserved 0x4B 0.75/1.50 0x4C 0.76/1.52 0x4D 0.77/1.54 0x4E 0.78/1.56 0x4F 0.79/1.58 0x50 0.80/1.60 0x51 0.81/1.62 0x52 0.82/1.64 0x53 0.83/1.66 0x54 0.84/1.68 0x55 0.85/1.70 0x56 0.86/1.72 0x57 0.87/1.74 0x58 0.88/1.76 0x59 0.89/1.78 0x5A 0.90/1.80 0x5B 0.91/1.82 0x5C 0.92/1.84 0x5D 0.93/1.86 0x5E 0.94/1.88 0x5F 0.95/1.90 0x60 0.96/1.92 0x61 0.97/1.94 0x62 0.98/1.96 0x63 0.99/1.98 0x64 1.00/2.00 0x65 1.01/2.02 0x66 1.02/2.04 0x67 1.03/2.06 0x68 1.04/2.08 0x69 1.05/2.10	

Bit	Type	Field Name	Description	Reset
			0x6A 1.06/2.12 0x6B 1.07/2.14 0x6C 1.08/2.16 0x6D 1.09/2.18 0x6E 1.10/2.20 0x6F 1.11/2.22 0x70 1.12/2.24 0x71 1.13/2.26 0x72 1.14/2.28 0x73 1.15/2.30 0x74 1.16/2.32 0x75 1.17/2.34 0x76 1.18/2.36 0x77 1.19/2.38 0x78 1.20/2.40 0x79 1.21/2.42 0x7A 1.22/2.44 0x7B 1.23/2.46 0x7C 1.24/2.48 0x7D 1.25/2.50 0x7E 1.26/2.52 0x7F 1.27/2.54 0x80 1.28/2.56 0x81 1.29/2.58 0x82 1.30/2.60 0x83 1.31/2.62 0x84 1.32/2.64 0x85 1.33/2.66 0x86 1.34/2.68 0x87 1.35/2.70 0x88 1.36/Reserved 0x89 1.37/Reserved 0x8A 1.38/Reserved 0x8B 1.39/Reserved 0x8C 1.40/Reserved 0x8D 1.41/Reserved 0x8E 1.42/Reserved 0x8F 1.43/Reserved	

Bit	Type	Field Name	Description	Reset
			0x90 1.44/Reserved 0x91 1.45/Reserved 0x92 1.46/Reserved 0x93 1.47/Reserved 0x94 1.48/Reserved 0x95 1.49/Reserved 0x96 1.50/Reserved 0x97 1.51/Reserved 0x98 1.52/Reserved 0x99 1.53/Reserved 0x9A 1.54/Reserved 0x9B 1.55/Reserved 0x9C 1.56/Reserved 0x9D 1.57/Reserved 0x9E 1.58/Reserved 0x9F 1.59/Reserved 0xA0 1.60/Reserved 0xA1 1.61/Reserved 0xA2 1.62/Reserved 0xA3 1.63/Reserved 0xA4 1.64/Reserved 0xA5 1.65/Reserved 0xA6 1.66/Reserved 0xA7 1.67/Reserved 0xA8 1.68/Reserved 0xA9 1.69/Reserved 0xAA 1.70/Reserved 0xAB 1.71/Reserved 0xAC 1.72/Reserved 0xAD 1.73/Reserved 0xAE 1.74/Reserved 0xAF 1.75/Reserved 0xB0 1.76/Reserved 0xB1 1.77/Reserved 0xB2 1.78/Reserved 0xB3 1.79/Reserved 0xB4 1.80/Reserved 0xB5 1.81/Reserved	

Bit	Type	Field Name	Description	Reset
			0xB6 1.82/Reserved 0xB7 1.83/Reserved 0xB8 1.84/Reserved 0xB9 1.85/Reserved 0xBA 1.86/Reserved 0xBB 1.87/Reserved 0xBC 1.88/Reserved 0xBD 1.89/Reserved 0xBE 1.90/Reserved 0xBF Reserved 0xFF Reserved	

Table 40: PMC_VOUT_CH2 (0x001F)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	CH2_VOUT	CH2 output voltage (V). Format is (without divider)/(with divider). **Value** **Description** 0x00 Reserved 0x36 Reserved 0x37 0.55/Reserved 0x38 0.56/Reserved 0x39 0.57/Reserved 0x3A 0.58/Reserved 0x3B 0.59/Reserved 0x3C 0.60/Reserved 0x3D 0.61/Reserved 0x3E 0.62/Reserved 0x3F 0.63/Reserved 0x40 0.64/Reserved 0x41 0.65/Reserved 0x42 0.66/Reserved 0x43 0.67/Reserved 0x44 0.68/Reserved 0x45 0.69/Reserved 0x46 0.70/Reserved 0x47 0.71/Reserved 0x48 0.72/Reserved 0x49 0.73/Reserved	0x6E

Bit	Type	Field Name	Description	Reset
			0x4A 0.74/Reserved 0x4B 0.75/1.50 0x4C 0.76/1.52 0x4D 0.77/1.54 0x4E 0.78/1.56 0x4F 0.79/1.58 0x50 0.80/1.60 0x51 0.81/1.62 0x52 0.82/1.64 0x53 0.83/1.66 0x54 0.84/1.68 0x55 0.85/1.70 0x56 0.86/1.72 0x57 0.87/1.74 0x58 0.88/1.76 0x59 0.89/1.78 0x5A 0.90/1.80 0x5B 0.91/1.82 0x5C 0.92/1.84 0x5D 0.93/1.86 0x5E 0.94/1.88 0x5F 0.95/1.90 0x60 0.96/1.92 0x61 0.97/1.94 0x62 0.98/1.96 0x63 0.99/1.98 0x64 1.00/2.00 0x65 1.01/2.02 0x66 1.02/2.04 0x67 1.03/2.06 0x68 1.04/2.08 0x69 1.05/2.10 0x6A 1.06/2.12 0x6B 1.07/2.14 0x6C 1.08/2.16 0x6D 1.09/2.18 0x6E 1.10/2.20 0x6F 1.11/2.22	

Bit	Type	Field Name	Description	Reset
			0x70 1.12/2.24 0x71 1.13/2.26 0x72 1.14/2.28 0x73 1.15/2.30 0x74 1.16/2.32 0x75 1.17/2.34 0x76 1.18/2.36 0x77 1.19/2.38 0x78 1.20/2.40 0x79 1.21/2.42 0x7A 1.22/2.44 0x7B 1.23/2.46 0x7C 1.24/2.48 0x7D 1.25/2.50 0x7E 1.26/2.52 0x7F 1.27/2.54 0x80 1.28/2.56 0x81 1.29/2.58 0x82 1.30/2.60 0x83 1.31/2.62 0x84 1.32/2.64 0x85 1.33/2.66 0x86 1.34/2.68 0x87 1.35/2.70 0x88 1.36/Reserved 0x89 1.37/Reserved 0x8A 1.38/Reserved 0x8B 1.39/Reserved 0x8C 1.40/Reserved 0x8D 1.41/Reserved 0x8E 1.42/Reserved 0x8F 1.43/Reserved 0x90 1.44/Reserved 0x91 1.45/Reserved 0x92 1.46/Reserved 0x93 1.47/Reserved 0x94 1.48/Reserved 0x95 1.49/Reserved	

Bit	Type	Field Name	Description	Reset
			0x96 1.50/Reserved 0x97 1.51/Reserved 0x98 1.52/Reserved 0x99 1.53/Reserved 0x9A 1.54/Reserved 0x9B 1.55/Reserved 0x9C 1.56/Reserved 0x9D 1.57/Reserved 0x9E 1.58/Reserved 0x9F 1.59/Reserved 0xA0 1.60/Reserved 0xA1 1.61/Reserved 0xA2 1.62/Reserved 0xA3 1.63/Reserved 0xA4 1.64/Reserved 0xA5 1.65/Reserved 0xA6 1.66/Reserved 0xA7 1.67/Reserved 0xA8 1.68/Reserved 0xA9 1.69/Reserved 0xAA 1.70/Reserved 0xAB 1.71/Reserved 0xAC 1.72/Reserved 0xAD 1.73/Reserved 0xAE 1.74/Reserved 0xAF 1.75/Reserved 0xB0 1.76/Reserved 0xB1 1.77/Reserved 0xB2 1.78/Reserved 0xB3 1.79/Reserved 0xB4 1.80/Reserved 0xB5 1.81/Reserved 0xB6 1.82/Reserved 0xB7 1.83/Reserved 0xB8 1.84/Reserved 0xB9 1.85/Reserved 0xBA 1.86/Reserved 0xBB 1.87/Reserved	

Bit	Type	Field Name	Description	Reset
			0xBC 1.88/Reserved 0xBD 1.89/Reserved 0xBE 1.90/Reserved 0xBF Reserved 0xFF Reserved	

Table 41: PMC_VOUT_CH3 (0x0020)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	CH3_VOUT	CH3 output voltage (V). Format is (without divider)/(with divider). **Value** **Description** 0x00 Reserved 0x36 Reserved 0x37 0.55/Reserved 0x38 0.56/Reserved 0x39 0.57/Reserved 0x3A 0.58/Reserved 0x3B 0.59/Reserved 0x3C 0.60/Reserved 0x3D 0.61/Reserved 0x3E 0.62/Reserved 0x3F 0.63/Reserved 0x40 0.64/Reserved 0x41 0.65/Reserved 0x42 0.66/Reserved 0x43 0.67/Reserved 0x44 0.68/Reserved 0x45 0.69/Reserved 0x46 0.70/Reserved 0x47 0.71/Reserved 0x48 0.72/Reserved 0x49 0.73/Reserved 0x4A 0.74/Reserved 0x4B 0.75/1.50 0x4C 0.76/1.52 0x4D 0.77/1.54 0x4E 0.78/1.56 0x4F 0.79/1.58	0x6E

Bit	Type	Field Name	Description	Reset
			0x50 0.80/1.60 0x51 0.81/1.62 0x52 0.82/1.64 0x53 0.83/1.66 0x54 0.84/1.68 0x55 0.85/1.70 0x56 0.86/1.72 0x57 0.87/1.74 0x58 0.88/1.76 0x59 0.89/1.78 0x5A 0.90/1.80 0x5B 0.91/1.82 0x5C 0.92/1.84 0x5D 0.93/1.86 0x5E 0.94/1.88 0x5F 0.95/1.90 0x60 0.96/1.92 0x61 0.97/1.94 0x62 0.98/1.96 0x63 0.99/1.98 0x64 1.00/2.00 0x65 1.01/2.02 0x66 1.02/2.04 0x67 1.03/2.06 0x68 1.04/2.08 0x69 1.05/2.10 0x6A 1.06/2.12 0x6B 1.07/2.14 0x6C 1.08/2.16 0x6D 1.09/2.18 0x6E 1.10/2.20 0x6F 1.11/2.22 0x70 1.12/2.24 0x71 1.13/2.26 0x72 1.14/2.28 0x73 1.15/2.30 0x74 1.16/2.32 0x75 1.17/2.34	

Bit	Type	Field Name	Description	Reset
			0x76 1.18/2.36 0x77 1.19/2.38 0x78 1.20/2.40 0x79 1.21/2.42 0x7A 1.22/2.44 0x7B 1.23/2.46 0x7C 1.24/2.48 0x7D 1.25/2.50 0x7E 1.26/2.52 0x7F 1.27/2.54 0x80 1.28/2.56 0x81 1.29/2.58 0x82 1.30/2.60 0x83 1.31/2.62 0x84 1.32/2.64 0x85 1.33/2.66 0x86 1.34/2.68 0x87 1.35/2.70 0x88 1.36/Reserved 0x89 1.37/Reserved 0x8A 1.38/Reserved 0x8B 1.39/Reserved 0x8C 1.40/Reserved 0x8D 1.41/Reserved 0x8E 1.42/Reserved 0x8F 1.43/Reserved 0x90 1.44/Reserved 0x91 1.45/Reserved 0x92 1.46/Reserved 0x93 1.47/Reserved 0x94 1.48/Reserved 0x95 1.49/Reserved 0x96 1.50/Reserved 0x97 1.51/Reserved 0x98 1.52/Reserved 0x99 1.53/Reserved 0x9A 1.54/Reserved 0x9B 1.55/Reserved	

Bit	Type	Field Name	Description	Reset
			0x9C 1.56/Reserved 0x9D 1.57/Reserved 0x9E 1.58/Reserved 0x9F 1.59/Reserved 0xA0 1.60/Reserved 0xA1 1.61/Reserved 0xA2 1.62/Reserved 0xA3 1.63/Reserved 0xA4 1.64/Reserved 0xA5 1.65/Reserved 0xA6 1.66/Reserved 0xA7 1.67/Reserved 0xA8 1.68/Reserved 0xA9 1.69/Reserved 0xAA 1.70/Reserved 0xAB 1.71/Reserved 0xAC 1.72/Reserved 0xAD 1.73/Reserved 0xAE 1.74/Reserved 0xAF 1.75/Reserved 0xB0 1.76/Reserved 0xB1 1.77/Reserved 0xB2 1.78/Reserved 0xB3 1.79/Reserved 0xB4 1.80/Reserved 0xB5 1.81/Reserved 0xB6 1.82/Reserved 0xB7 1.83/Reserved 0xB8 1.84/Reserved 0xB9 1.85/Reserved 0xBA 1.86/Reserved 0xBB 1.87/Reserved 0xBC 1.88/Reserved 0xBD 1.89/Reserved 0xBE 1.90/Reserved 0xBF Reserved 0xFF Reserved	

Table 42: PMC_VOUT_CH4 (0x0021)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	CH4_VOUT	CH4 output voltage (V). Format is (without divider)/(with divider). **Value** **Description** 0x00 Reserved 0x36 Reserved 0x37 0.55/Reserved 0x38 0.56/Reserved 0x39 0.57/Reserved 0x3A 0.58/Reserved 0x3B 0.59/Reserved 0x3C 0.60/Reserved 0x3D 0.61/Reserved 0x3E 0.62/Reserved 0x3F 0.63/Reserved 0x40 0.64/Reserved 0x41 0.65/Reserved 0x42 0.66/Reserved 0x43 0.67/Reserved 0x44 0.68/Reserved 0x45 0.69/Reserved 0x46 0.70/Reserved 0x47 0.71/Reserved 0x48 0.72/Reserved 0x49 0.73/Reserved 0x4A 0.74/Reserved 0x4B 0.75/1.50 0x4C 0.76/1.52 0x4D 0.77/1.54 0x4E 0.78/1.56 0x4F 0.79/1.58 0x50 0.80/1.60 0x51 0.81/1.62 0x52 0.82/1.64 0x53 0.83/1.66 0x54 0.84/1.68 0x55 0.85/1.70 0x56 0.86/1.72	0x46

Bit	Type	Field Name	Description	Reset
			0x57 0.87/1.74 0x58 0.88/1.76 0x59 0.89/1.78 0x5A 0.90/1.80 0x5B 0.91/1.82 0x5C 0.92/1.84 0x5D 0.93/1.86 0x5E 0.94/1.88 0x5F 0.95/1.90 0x60 0.96/1.92 0x61 0.97/1.94 0x62 0.98/1.96 0x63 0.99/1.98 0x64 1.00/2.00 0x65 1.01/2.02 0x66 1.02/2.04 0x67 1.03/2.06 0x68 1.04/2.08 0x69 1.05/2.10 0x6A 1.06/2.12 0x6B 1.07/2.14 0x6C 1.08/2.16 0x6D 1.09/2.18 0x6E 1.10/2.20 0x6F 1.11/2.22 0x70 1.12/2.24 0x71 1.13/2.26 0x72 1.14/2.28 0x73 1.15/2.30 0x74 1.16/2.32 0x75 1.17/2.34 0x76 1.18/2.36 0x77 1.19/2.38 0x78 1.20/2.40 0x79 1.21/2.42 0x7A 1.22/2.44 0x7B 1.23/2.46 0x7C 1.24/2.48	

Bit	Type	Field Name	Description	Reset
			0x7D 1.25/2.50 0x7E 1.26/2.52 0x7F 1.27/2.54 0x80 1.28/2.56 0x81 1.29/2.58 0x82 1.30/2.60 0x83 1.31/2.62 0x84 1.32/2.64 0x85 1.33/2.66 0x86 1.34/2.68 0x87 1.35/2.70 0x88 1.36/Reserved 0x89 1.37/Reserved 0x8A 1.38/Reserved 0x8B 1.39/Reserved 0x8C 1.40/Reserved 0x8D 1.41/Reserved 0x8E 1.42/Reserved 0x8F 1.43/Reserved 0x90 1.44/Reserved 0x91 1.45/Reserved 0x92 1.46/Reserved 0x93 1.47/Reserved 0x94 1.48/Reserved 0x95 1.49/Reserved 0x96 1.50/Reserved 0x97 1.51/Reserved 0x98 1.52/Reserved 0x99 1.53/Reserved 0x9A 1.54/Reserved 0x9B 1.55/Reserved 0x9C 1.56/Reserved 0x9D 1.57/Reserved 0x9E 1.58/Reserved 0x9F 1.59/Reserved 0xA0 1.60/Reserved 0xA1 1.61/Reserved 0xA2 1.62/Reserved	

Bit	Type	Field Name	Description	Reset
			0xA3 1.63/Reserved 0xA4 1.64/Reserved 0xA5 1.65/Reserved 0xA6 1.66/Reserved 0xA7 1.67/Reserved 0xA8 1.68/Reserved 0xA9 1.69/Reserved 0xAA 1.70/Reserved 0xAB 1.71/Reserved 0xAC 1.72/Reserved 0xAD 1.73/Reserved 0xAE 1.74/Reserved 0xAF 1.75/Reserved 0xB0 1.76/Reserved 0xB1 1.77/Reserved 0xB2 1.78/Reserved 0xB3 1.79/Reserved 0xB4 1.80/Reserved 0xB5 1.81/Reserved 0xB6 1.82/Reserved 0xB7 1.83/Reserved 0xB8 1.84/Reserved 0xB9 1.85/Reserved 0xBA 1.86/Reserved 0xBB 1.87/Reserved 0xBC 1.88/Reserved 0xBD 1.89/Reserved 0xBE 1.90/Reserved 0xBF Reserved 0xFF Reserved	

Table 43: PMC_OPTION_03 (0x002E)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	CH1_PHASE	CH1 PHASE setting **Value** **Description** 0x0 0 degrees shift 0x1 90 degrees shift 0x2 180 degrees shift 0x3 270 degrees shift	0x0

Bit	Type	Field Name	Description	Reset
[5:4]	RW	CH2_PHASE	CH2 PHASE setting **Value** **Description** 0x0 0 degrees shift 0x1 90 degrees shift 0x2 180 degrees shift 0x3 270 degrees shift	0x0
[3:2]	RW	CH3_PHASE	CH3 PHASE setting **Value** **Description** 0x0 0 degrees shift 0x1 90 degrees shift 0x2 180 degrees shift 0x3 270 degrees shift	0x0
[1:0]	RW	CH4_FREQ	CH4 PHASE setting **Value** **Description** 0x0 0 degrees shift 0x1 90 degrees shift 0x2 180 degrees shift 0x3 270 degrees shift	0x0

Table 44: PMC_OPTION_06 (0x0031)

Bit	Type	Field Name	Description	Reset
[2]	RW	ASSP_IRQ	Bit to configure the POR pin **Value** **Description** 0x0 POR pin is POR 0x1 POR pin is IRQ	0x0

Table 45: CH1_EN_DIVIDER (0x004C)

Bit	Type	Field Name	Description	Reset
[6]	RW	CH1_EN_DIVIDER	Bit to enable the divider mode for CH1 **Value** **Description** 0x0 Without divider - VOUT not doubled 0x1 With divider - VOUT doubled	0x0

Table 46: CH2_EN_DIVIDER (0x004D)

Bit	Type	Field Name	Description	Reset
[6]	RW	CH2_EN_DIVIDER	Bit to enable the divider mode for CH2 **Value** **Description** 0x0 Without divider - VOUT not doubled 0x1 With divider - VOUT doubled	0x0

Table 47: CH3_EN_DIVIDER (0x004E)

Bit	Type	Field Name	Description	Reset
[6]	RW	CH3_EN_DIVIDER	Bit to enable the divider mode for CH3 **Value** **Description** 0x0 Without divider - VOUT not doubled 0x1 With divider - VOUT doubled	0x0

Table 48: CH4_EN_DIVIDER (0x004F)

Bit	Type	Field Name	Description	Reset
[6]	RW	CH4_EN_DIVIDER	Bit to enable the divider mode for CH4 **Value** **Description** 0x0 Without divider - VOUT not doubled 0x1 With divider - VOUT doubled	0x0

8. Package Information

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

8.1 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 49.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The package is qualified for MSL 1.

Table 49: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

8.2 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLCSP package will cause damage to the solder balls. Therefore, a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

8.3 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

9. Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability of OTP variants, please consult your Renesas local sales representative.

Table 50. Ordering Information

Part Number	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type	Temperature Range
DA9083-xxUUC	36 lead, 2.5 x 2.5 mm WLCSP	36-WLCSP	Reel, 3 k	-40 ◦C to +85 ◦C
DA9083-xxUU6			Tray, 500	

Part Number Legend:

xx: OTP variant

10. MPU Compatibility

Table 51 shown the list of MPU devices that are compatible with the specific variant.

Table 51. Target MPU

Feature	OTP-26	OTP-28	OTP-31	-	-	-
Target MPU	N.A. CH<x> & LSW off, AUTO	N.A. CH<x> & LSW off, PWM	RZ/N2L	-	-	-

11. Application Information

The following recommended components are references selected from requirements of a typical application.

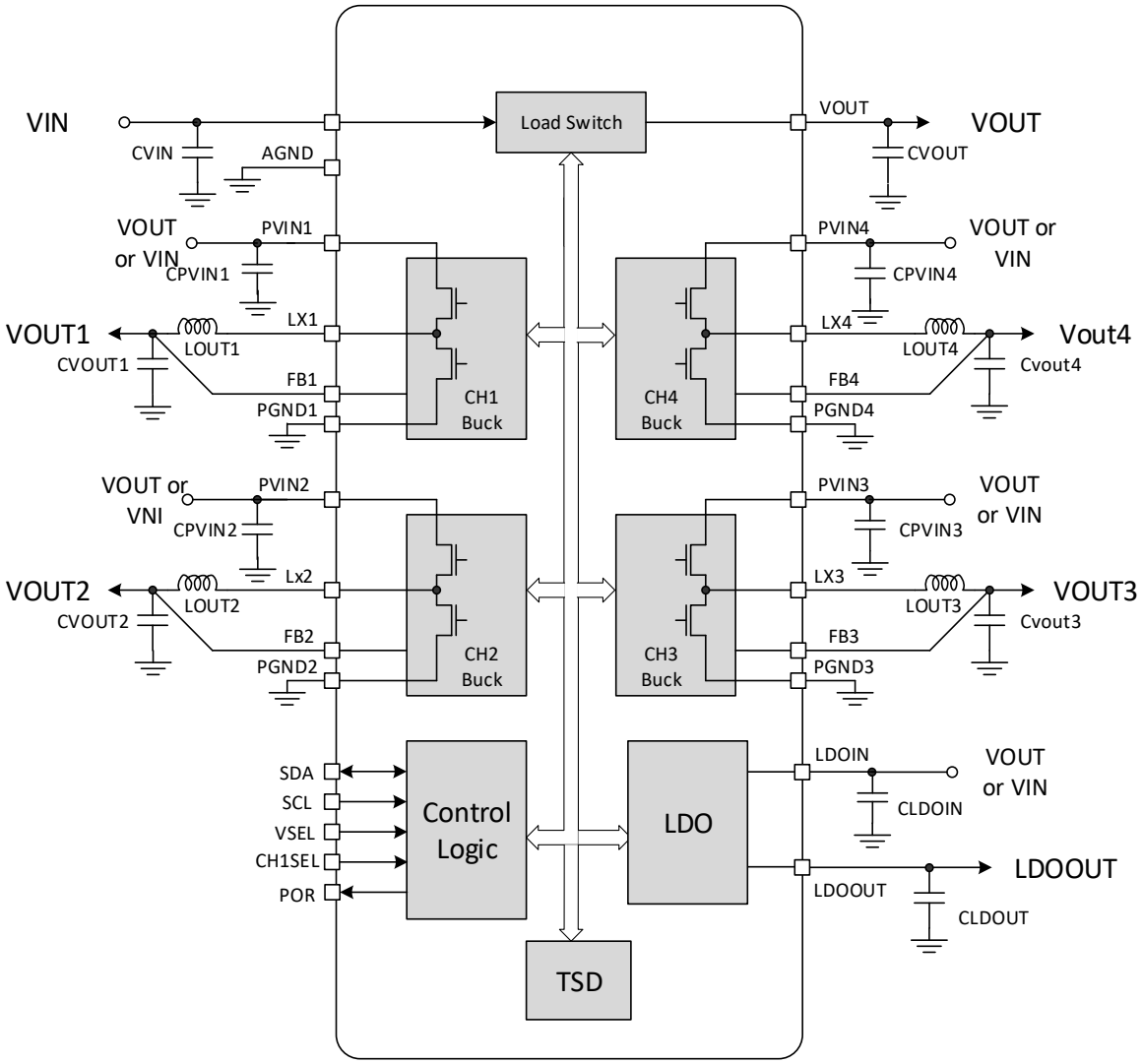


Figure 16: Applications Diagram

11.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account.

Table 52: Recommended Capacitor Types

Application	Value	Size	Temp Char	Tol (%)	Rated (V)	Type
C_{VIN}	100 nF	0201	X5R ±15 %	±10	6.3	Murata GRM033R60J104KE19#
C_{VOUT} (Optional)	10 µF	0402	X5R ±15 %	±20	6.3	Murata GRM155R60J106ME15#
C_{PVIN1}, C_{PVIN2}, C_{PVIN3}, C_{PVIN4}	10 µF	0402	X5R ±15 %	±20	6.3	Murata GRM155R60J106ME15#
C_{VOUT1}, C_{VOUT2}, C_{VOUT3}, C_{VOUT4}	22 µF	0402	X6S ±22 %	±20	4V	Murata GRM158C80G226ME01#

Application	Value	Size	Temp Char	Tol (%)	Rated (V)	Type
C_{LDOIN}	10 µF	0402	X5R ±15 %	±20	6.3	Murata GRM155R60J106ME15#
C_{LDOOUT}	4.7 µF	0402	X5R ±15 %	±20	6.3	Murata GRM155R60J475ME47#

11.2 Inductor Selection

Inductors should be selected based on the following parameters:

- Rated maximum current
- Usually, a coil provides two current limits: ISAT specifies the maximum current at which the inductance drops by 30 % of the nominal value, and IMAX is defined by the maximum power dissipation and is applied to the effective current.
- DC resistance
- Critical for the converter efficiency and should therefore be minimized.

Fully shielded inductor is highly recommended to use. The typical recommended output inductance is 470 nH per phase. Use of larger output inductance degrades the load transient performance of the buck converter.

Table 53: Recommended Inductor Types

Application	Value	Size (WxLxH) (mm)	I_{MAX}(DC) (A)	I_{SAT} (A)	Tol (%)	DC Resistance (mΩ)	Type
L_{OUT1}, L_{OUT2}, L_{OUT3},	470 nH	1.6 x 2.0 x 1.2	5.1	5.8	±20	20	Cyntec HMLQ20161B-R47MDR
L_{OUT4}	470 nH	2.0 x 2.5 x 1.0	5.5	7.2	±20	20	Cyntec HMLR25201T-R47MSR

A. ECAD Design Information

This appendix contains information that supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
DA9083-xxUUC	36	WLCSP	WB0036AA / PSC-5137-01
DA9083-xxUU6	36	WLCSP	WB0036AA / PSC-5137-01

1. xx: OTP variant

A.2 Symbol Pin Information

A.2.1 36-WLCSP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
A1	PGND3	Power	-
A2	LDOOUT	Power	-
A3	VOUT	Power	-
A4	VOUT	Power	-
A5	VIN	Power	-
A6	VIN	Power	-
B1	LX3	Power	-
B2	LDOIN	Power	-
B3	SCL	Input	-
B4	VOUT	Power	-
B5	VIN	Power	-
B6	PGND1	Power	-
C1	PVIN3	Power	-
C2	FB3	Input	-
C3	POR	Output	-
C4	SDA	I/O	-
C5	CH1SEL	Power	-
C6	LX1	Power	-
D1	PVIN4	Power	-
D2	VSEL	Power	-
D3	FB4	Input	-
D4	AGND	Power	-
D5	FB1	Input	-
D6	PVIN1	Power	-
E1	LX4	Power	-
E2	LX4	Power	-
E3	PGND4	Power	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
E4	PGND4	Power	-
E5	FB2	Input	-
E6	PVIN2	Power	-
F1	LX4	Power	-
F2	LX4	Power	-
F3	PGND4	Power	-
F4	PGND2	Power	-
F5	LX2	Power	-
F6	LX2	Power	-

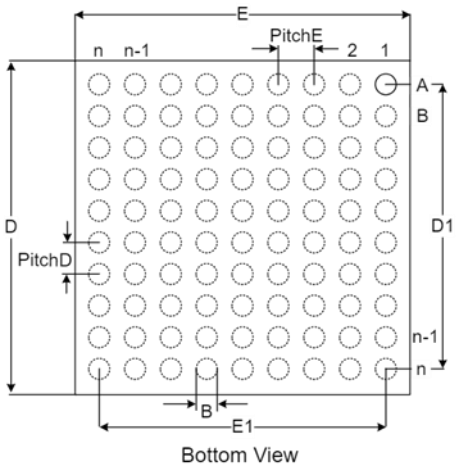
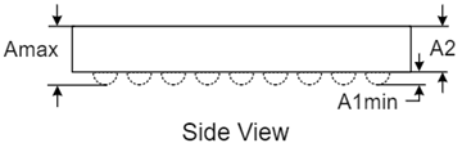
A.3 Symbol Parameters

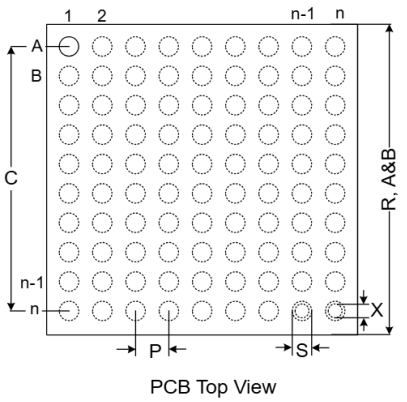
Orderable Part Number	Interface	Max Junction Temperature (T_J)	Max Input Voltage	Min Input Voltage	Max Operating Temperature	Min Operating Temperature	Max Output Current	Max Output Voltage	Min Output Voltage	Mounting Type	Qualification	RoHS	Switching Frequency
DA9083-xxUUC	I2C	+150 °C	5.5 V	2.9 V	+85 °C	-40 °C	5 A	2.7 V	0.55 V	SMD	Industrial	Compliant	2 MHz
DA9083-xxUU6	I2C	+150 °C	5.5 V	2.9 V	+85 °C	-40 °C	5 A	2.7 V	0.55 V	SMD	Industrial	Compliant	2 MHz

A.4 Footprint Design Information

A.4.1 36-WLCSP

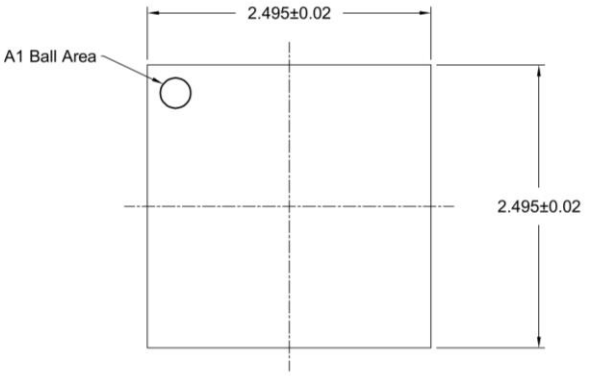
IPC Footprint Type	Package Code/ POD Number	Number of Pins
WLCSP	WB0036AA / PSC-5137-01	36

Description	Dimension	Value (mm)	Diagram
Minimum body Length (vertical side)	Dmin	2.475	
Maximum body Length (vertical side)	Dmax	2.515	
Average length of grid (vertical side)	D1ave	2.000	
Minimum body Width (horizontal side)	Emin	2.475	
Maximum body Width (horizontal side)	Emax	2.515	
Average length of grid (horizontal side)	E1ave	2.000	
Minimum Standoff Height	A1min	0.175	
Maximum Height	Amax	0.550	
Average ball diameter	Bnom	0.270	
Distance between the center of any two adjacent balls (vertical side)	PitchD	0.40	
Distance between the center of any two adjacent balls (horizontal side)	PitchE	0.40	
P = Plain Grid, S = Staggered Grid	GridType	P	
F = Full Matrix, P = Perimeter, SD = Selectively Depopulated, TE = Thermally Enhanced	MatrixType	F	
Number of balls (vertical side)	Rows	6	
Number of balls (horizontal side)	Columns	6	
Maximum number of ball positions (Rows x Columns)	Nmax	36	
Number of actual balls present	PinCount	36	

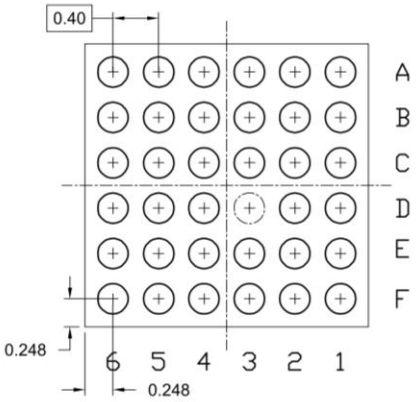
Recommended Land Pattern (NSMD Design)			
Description	**Dimension**	**Value (mm)**	**Diagram**
Diameter of pad. If specified this overrides the calculated value. This can be used to specify a manufacturer's recommended pad size.	X	0.221	
Solder Mask Expansion.	S	0.321	

Package Outline Drawing

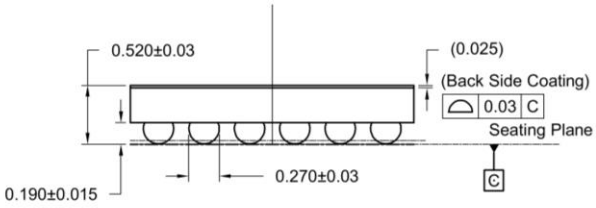
PSC-5137-01
Package Code:WB0036AA
36-WLCSP 2.495 x 2.495 x 0.520 mm Body, 0.40 mm Pitch
Rev.01, Feb 20, 2025



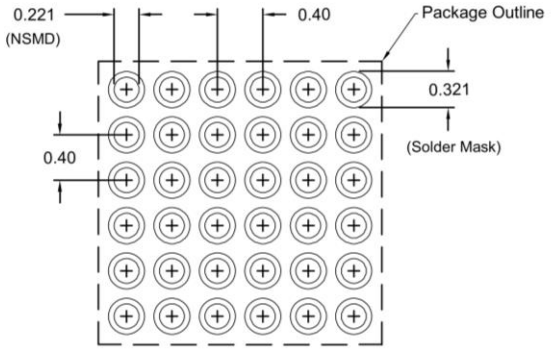
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top view, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimension are in mm and angles are in degrees.
3. Use ±0.05mm for the non-tolerenced dimensions.
4. Numbers in ( ) are for references only.
5. Pre-reflow solder ball diameter is Ø0.25 mm.
6. UBM diameter is Ø0.245 mm.

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