DA9098

Ultra-Low I_Q Charger PMIC with 4-Output SIMO

The **DA9098** is a highly integrated, configurable, ultra-low quiescent current charger PMIC with a host of additional functionality to support the needs of TWS Systems (Hearables), Wearables, and other small Li-Ion battery operated applications.

The Charger PMIC integrates a 500 mA linear battery charger with power-path manager (PPM), a 4-output SIMO capable of delivering 400 mA of total current, four LDOs and a 3-channel LED driver. In addition to this highly integrated functionality, the DA9098 features a complete set of robust protection features, watchdog, additional GPIOs for system flexibility, and I^2C control in a compact WLCSP package.

DA9098 has several power saving modes to increase battery life, whether the product sits on the shelf or is in operation.

DA9098 provides charge current up to 500 mA for fast charging cycle. The charge profile is programmable and includes dynamic power path management which automatically balances current delivered to the system and battery charging.

Suitable for small battery applications, the battery monitor facilitates on-demand battery voltage, charge and discharge current monitors, as well as temperature management.

Key Features

- Increased battery life
- 1.3 µA I_Q in deep sleep mode
- Power saving modes optimized for storage and low-power operation
- Multiple wake-up sources supported for maximum user flexibility
- Charger & Power Path Management
  - Fast charge: 500 mA (max) programmable charge current
  - Programmable pre-charge, fast charge, and termination conditions
  - Dynamic power path
  - Supports adaptive power source voltage to minimize power dissipation
- 4-output 0.5 V to 1.85 V SIMO for total 400 mA
- Four LDOs
  - LDO1/2 V_{OUT}: 0.5 V to 1.2 V, I_{OUT}: 100 mA (max)
  - LDO3 V_{OUT}: 1.8 V, I_{OUT}: 20 mA (max), I_Q = 300 nA (typ)
  - LDO4 V_{OUT}: 1.2 V to 3.3 V, I_{OUT}: 100 mA (max)
- Protection features
  - Over-voltage protection
  - Thermal shutdown protection
  - Over-discharge protection
- LED driver current sinks
- High integration and configurability
  - I^2C enabled battery monitors
  - Charging status monitors
  - Compact 7x7 WLCSP package with 0.35 mm ball pitch

Applications

- TWS systems, hearables
- Wearable devices - Wireless headphones, fitness trackers, smart watches,
- Home automation devices - Smoke detectors, Smart thermostats, Smart door locks
- Health monitoring medical accessories
- Rechargeable toys
- High efficiency, ultra-low power applications

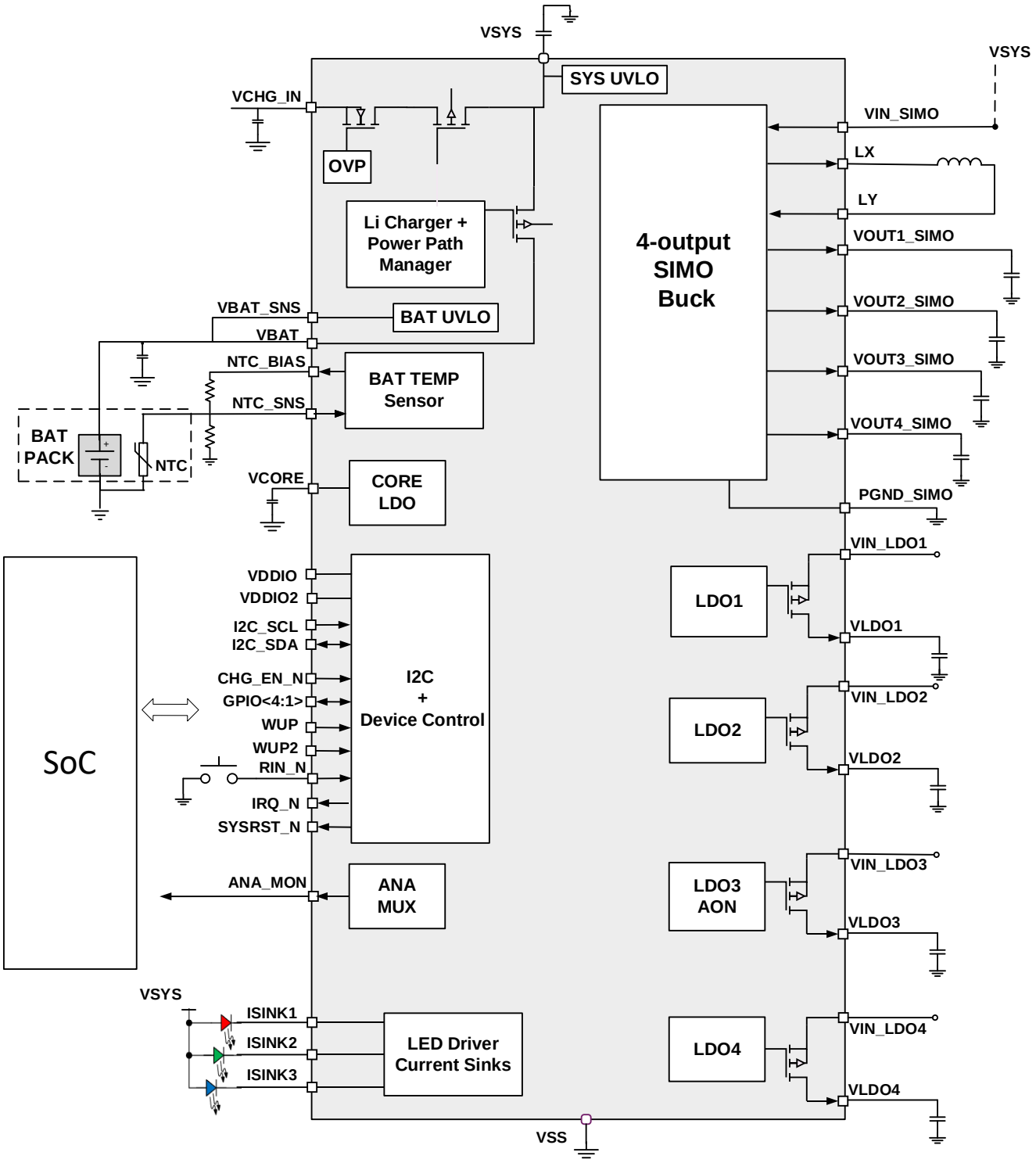

Figure 1. System diagram

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1. Terms and Definitions

DPM	Dynamic power management
DPPM	Dynamic power path management
TWS	True wireless stereo
OTP	One-time programable (memory)

2. References

[1] None

Note 1 References are for the latest published version, unless otherwise indicated.

3. Pin Information

3.1 Pin Assignments

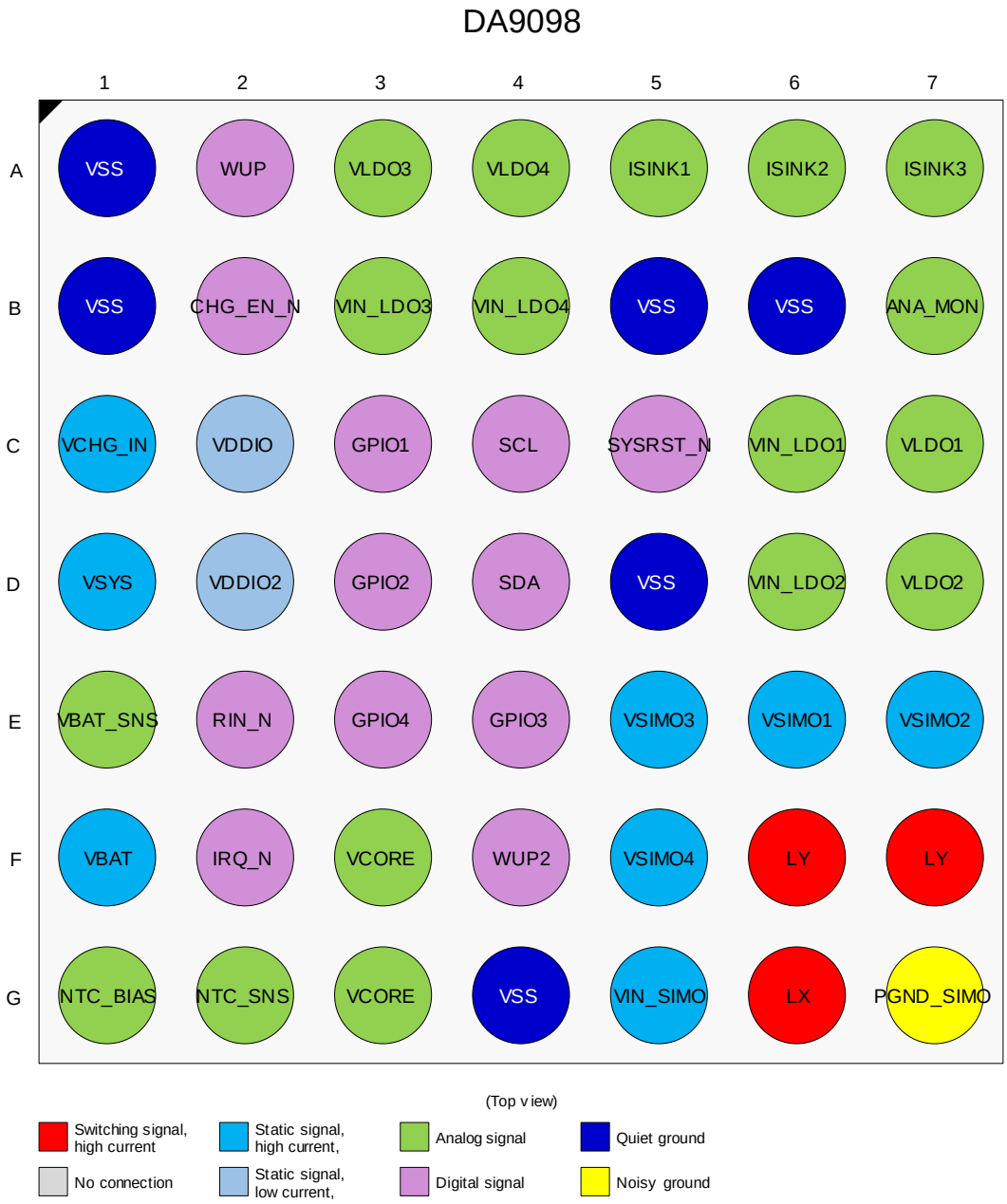


Figure 2. WLCSP pinout diagram (top view)

3.2 Pin Descriptions

Table 1. Pin descriptions

Pin number	Pin name	Type (Table 2)	Drive (mA)	Description
C1	VCHG_IN	PWR	500	Input power supply. In register names the VDD_PWR alias is used
D1	VSYS	PWR	2000	Intermediate supply of power rails
F1	VBAT	PWR	2000	Battery connection
E1	VBAT_SNS	AI	0.1	Sense battery voltage. To be tied with VBAT on PCB
F3	VCORE	PWR	10	1.5 V Core supply
G3	VCORE	PWR	10	1.5 V Core supply
G5	VIN_SIMO	PWR	2000	SIMO Buck input supply
G6	LX	AIO	2000	SIMO Buck switching node
F7	LY	AIO	2000	SIMO switches input node
F6	LY	AIO	2000	SIMO switches input node
E6	VSIMO1	PWR	500	SIMO1 output
E7	VSIMO2	PWR	500	SIMO2 output
E5	VSIMO3	PWR	500	SIMO3 output
F5	VSIMO4	PWR	500	SIMO4 output
G7	PGND_SIMO	GND	2000	SIMO power ground
C6	VIN_LDO1	PWR	250	LDO1 supply input. Connect to VSIMO1
C7	VLDO1	PWR	250	LDO1 output
D6	VIN_LDO2	PWR	250	LDO2 supply input, Connect toVSIMO1
D7	VLDO2	PWR	250	LDO2 output
B3	VIN_LDO3	PWR	250	LDO3 supply input
A3	VLDO3	PWR	250	LDO3 output
B4	VIN_LDO4	PWR	250	LDO4 supply input
A4	VLDO4	PWR	250	LDO4 output
C2	VDDIO	PWR	250	IO supply
D2	VDDIO2	PWR	250	IO supply GPIO3/GPIO4
C3	GPIO1	DIO	10	General purpose IO
D3	GPIO2	DIO	10	General purpose IO
E4	GPIO3	DIO	10	General purpose IO- VDDIO2 supplied
E3	GPIO4	DIO	10	General purpose IO - VDDIO2 supplied
E2	RIN_N	DI	0.1	Manual reset input and wake from SHIP mode. Internal pull-up 18.8 kΩ to max (VBAT ; VCHG_IN)
A2	WUP	DI	10	Dedicated pin for deep sleep mode wake-up
F4	WUP2	DI	10	Additional pin for wake-up from deep sleep mode
C5	SYSRST_N	DO	0.1	System reset output - Host enable
F2	IRQ_N	DO	0.1	Open-drain IRQ output
B2	CHG_EN_N	DI	0.1	Charge enable input. Internal pull-down 900 kΩ
C4	SCL	DIO	10	I^2C clock input
D4	SDA	DIO	1	I^2C data
G1	NTC_BIAS	AIO	1	External temperature monitoring bias
G2	NTC_SNS	AIO	1	External temperature monitoring sense pin
B7	ANA_MON	AO	1	Various Analog signals scaled to 1.5V FS for ext. ADC measurement
A5	ISINK1	AO	250	LED driver Output 1
A6	ISINK2	AO	250	LED driver Output 2
A7	ISINK3	AO	250	LED driver Output 3
B5	VSS	GND	500	

Pin number	Pin name	Type (Table 2)	Drive (mA)	Description
B1	VSS	GND	500	
A1	VSS	GND	500	
B6	VSS	GND	500	
D5	VSS	GND	500	
G4	VSS	GND	500	

Table 2. Pin type definition

Pin type	Description	Pin type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
PWR	Power	GND	Ground

4. Specifications

Unless otherwise specified, typical characteristics (Typ) are reflecting performance under typical External Electrical Conditions at room temperature and limit characteristics (Min, Max) to correspond to performance variation across limit External Electrical Conditions for junction temperature from -40 ºC to 125 ºC.

4.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Table 3. Absolute maximum ratings

Parameter	Description	Conditions	Min	Max	Unit
V_{CHG_IN}	VCHG_IN		-0.3	22	V
V_{SUP}	VBAT, VBAT_SNS VSYS, VDDIO, VDDIO2, VIN_LDO3, VIN_LDO4, VIN_SIMO, LX, LY, VSIMO1, VSIMO2, VSIMO3, VSIMO4, VLDO4, ISINK1, ISINK2, ISINK3, NTC_BIAS, NTC_SNS		-0.3	6	V
V_{CORE}	VIN_LDO1, VLDO1, VIN_LDO2, VLDO2, VCORE, ANA_MON		-0.3	1.8	V
V_{I2C}	SDA, SCL		-0.3	6	V
V_{IO}	All other pins	Absolute voltage must not exceed 6 V	-0.3	V_{SUP} + 0.3	V

4.2 Electrostatic Discharge Ratings

Table 4. Electrostatic discharge ratings

Parameter	Description	Conditions	Rating	Unit
V_{ESD_CDM}	Maximum ESD protection	Charged device model (CDM) Note 1	±500	V
V_{ESD_HBM}	Maximum ESD protection	Human body model (HBM) Note 2		

Note 1 JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Note 2 JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

Table 5. Recommended operating conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating Ambient Temperature		-40		85	ºC
V_{CHG_IN}	Charger Input Supply		3.6	5	5.5	V
V_{BAT}	Battery voltage	Active battery	2.5	3.6	4.7	V
V_{IN_LDO}	LDO input voltage	LDO1 and LDO2	0.7	0.95	1.5	V
		LDO3 and LDO4	2.5	3.6	5.5	V
V_{IN_SIMO}	SIMO input voltage		2.5	3.6	5.5	V
V_{DDIO}	IO supply	VDDIO, VDDIO2	1.7	1.8	5.5	V

VDDIO supplies most of the chip IOs.

VDDIO2 supplies GPIO3 and GPIO4 only.

If GPIO3 or GPIO4 are used, VDDIO2 shall be supplied by one of the DA9098 rails. Otherwise, it can be left unconnected.

One proposed configuration is LDO3 to supply VDDIO and VSYS to supply VDDIO2 .

4.4 Recommended External Components

Component values shown in Table 6 are nominal values (before de-rating).

For capacitors, temperature profile shall be X5R type or better with a DC voltage rating of 2x the maximum applied voltage.

For inductors, the saturation current rating shall be equal or greater than the current limit value.

Table 6. Recommended external components

Parameter	Description	Nominal	Unit
C_{SYS}	VSYS capacitance	10	µF
C_{BAT}	VBAT capacitance	2.2	µF
C_{VCHG_IN}	VCHG_IN capacitance	4.7	µF
C_{CORE}	VCORE capacitance	220	nF
L_{SIMO}	SIMO buck inductor	0.47	µH
C_{I_SIMO}	SIMO input capacitor	not populated	µF
C_{O_SIMO1}	SIMO1 output capacitance	10	µF
C_{O_SIMO2}	SIMO2 output capacitance	10	µF
C_{O_SIMO3}	SIMO3 output capacitance	22	µF
C_{O_SIMO4}	SIMO4 output capacitance	10	µF
C_{I_LDO1}	LDO1 input capacitor	not populated	µF
C_{O_LDO1}	LDO1 output capacitor	2.2	µF
C_{I_LDO2}	LDO2 input capacitor	not populated	µF
C_{O_LDO2}	LDO2 output capacitor	2.2	µF
C_{I_LDO3}	LDO3 input capacitor	not populated	µF
C_{O_LDO3}	LDO3 output capacitor	2.2	µF
C_{I_LDO4}	LDO4 input capacitor	not populated	µF
C_{O_LDO4}	LDO3 output capacitor	2.2	µF
R_{NTC}	Battery thermal sensing resistance	10.0	kΩ
R_{NTC1}	External thermal sensing resistance	14.3	kΩ
R_{NTC2}	Skin thermal sensing resistance	14.3	kΩ

4.5 Current Consumption Characteristics

Table 7: Input currents electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical performance						
I_{BAT_SHIP}	Battery discharge current in SHIP mode	V_{CHG_IN} = 0 V SHIP mode All rails off		100		nA
$I_{BAT\_DEEP\_SLEEP}$	Battery discharge current in deep sleep mode	V_{CHG_IN} = 0 V LDO3 enabled SIMO, LDO1, LDO2 and LDO4 disabled I^2C disabled		1.3		µA
$I_{BAT\_ACT\_RAILS\_OFF}$	Battery discharge current in active mode, power rails off	0 °C < T_J < 85 °C V_{CHG_IN} = 0 V Battery active mode All power rails off		8		µA
I_{BAT_ACT}	Battery discharge current in Active battery mode	V_{CHG_IN} = 0 V Active battery mode All rails on, not loaded ISINK disabled I^2C enabled		33		µA
$I_{IN\_CHG\_READY}$	Supply current for control	0 °C < T_J < 85 °C V_{CHG_IN} = 5 V Charge ready			1.5	mA

4.6 SIMO Buck Regulator Characteristics

Table 8: SIMO buck electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External electrical conditions						
V_{IN}	SIMO Buck input voltage		2.5	3.6	5.5	V
L_{SIMO}	SIMO buck inductor		0.37	0.47	0.56	µH
C_{OUT_SIMO1}	SIMO1 Output capacitance	Effective output capacitance	4.3			µF
C_{OUT_SIMO2}	SIMO2 Output capacitance	Effective output capacitance	4.7			µF
C_{OUT_SIMO3}	SIMO3 Output capacitance	Effective output capacitance	5.2			µF
C_{OUT_SIMO4}	SIMO4 Output capacitance	Effective output capacitance	3.9			µF
Programmable conditions						
V_{OUT_RNG}	Output voltage range per output rail individually programmable	Step size 12.5 mV	0.5		1.85	V
$V_{OUT\_UV\_RNG}$	UV comparator per rail - Absolute threshold	Step size 100 mV	0.4		1.8	V
I_{PEAK_RNG}	Peak coil current limit range	3-bits programmable range	520		1750	mA
Electrical performance						
I_{OUT_MAX}	Maximum DC output current per rail		100			mA
$V_{OUT\_STATIC\_ACC}$	Output voltage static accuracy per rail	V_{IN} = 3.6 V I_{OUT} = 1 mA V_{OUT} = Typ	-2		2	%
$V_{OUT\_TR\_LINE}$	Output voltage transient line response	V_{IN} = 3.6 V to 3.1 V in 1 µs and back I_{OUT} = 100/20/100/20 mA	-10		10	mV
$V_{OUT\_TR\_ACC}$	Output voltage dynamic accuracy	V_{IN} > 3.0 V SIMO1: V_{OUT} = 0.95 V, I_{OUT} = 100 mA, C_{OUT} = 10 µF SIMO2: V_{OUT} = 0.65 V, I_{OUT} = 20 mA, C_{OUT} = 10 µF SIMO3: V_{OUT} =1.8 V, I_{OUT} = 100 mA, C_{OUT} = 22 µF SIMO4: V_{OUT} =1.2 V, I_{OUT} = 20 mA, C_{OUT} = 10 µF Note 1	-55		55	mV
V_{OUT_UV}	UV accuracy	V_{OUT} falling	-8		8	%
R_{PD}	Output discharge resistance			100		Ω
I_Q	Quiescent current	No load - all rails enabled		6		µA

Note 1 Capacitance nominal before derating

4.7 LDO Characteristics

4.7.1 LDO1 Characteristics

Table 9: LDO1 electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External electrical conditions						
V_{IN}	LDO input voltage		0.55	0.95	1.5	V
C_{OUT}	Output capacitance	Effective output capacitance	0.9			µF
I_{OUT_MAX}	Maximum output current		100			mA
Programmable conditions						
V_{OUT}	Selectable output voltage		0.5	0.8	1.2	V
V_{OUT_LSB}	Output voltage programming step size			3.125		mV
Electrical performance						
Static Parameters						
$V_{DROPOUT}$	Dropout voltage	$V_{OUT} = V_{OUT\_SET}$ - 10 mV $I_{OUT} = I_{OUT}$ (Max)			50	mV
$V_{OUT\_STATIC\_TOT}$	Overall output accuracy	Part to part variation T_A = -40 °C to 85°C $V_{IN} = V_{OUT} + V_{DROPOUT}$ to V_{IN} (Max) I_{OUT} = 1 mA to 100 mA $V_{OUT} = V_{OUT}$ (Typ)	-23		23	mV
$V_{OUT\_STATIC\_LD}$	Static load regulation	I_{OUT} = 1 mA to I_{OUT_MAX}	-6		6	mV
Dynamic Parameters						
$V_{OUT\_TR\_LINE}$	Line transient response	$V_{IN} = V_{OUT} + V_{DROPOUT}$ + 100 mV to $V_{IN} = V_{OUT} + V_{DROPOUT}$ V_{OUT} = Min to Max $I_{OUT} = I_{OUT\_MAX}$ $t_{RISE} = t_{FALL}$ = 1 us	-5		5	mV
$V_{OUT\_TR\_LD\_1mA}$	Load transient response	I_{OUT} = 1 mA to I_{OUT_MAX} $t_{RISE} = t_{FALL}$ = 1 µs	-24		24	mV
t_{ON}	Turn-on time	Time to 90 % of V_{OUT_SET} I_{OUT} = 0 mA			1	ms
AC Parameters						
$PSRR_{10Hz\_10kHz\_VIN}$	Power supply rejection ratio	f = 10 Hz to 10 kHz $I_{OUT} = I_{OUT}$ (Max) $V_{OUT} = V_{OUT}$ (Typ) $V_{IN} = V_{IN}$ (Typ)	40			dB
$PSRR_{10kHz\_2MHz\_VIN}$	Power supply rejection ratio	f = 10 kHz to 2 MHz $I_{OUT} = I_{OUT}$ (Max) $V_{OUT} = V_{OUT}$ (Typ) $V_{IN} = V_{IN}$ (Typ)	29			dB

Parameter	Description	Conditions	Min	Typ	Max	Unit
Quiescent Current Specifications						
$I_{Q\_ON\_0mA}$	Quiescent current, no load	I_{OUT} = 0 mA		6		µA
R_{PD}	Output pull-down resistance when OFF	V_{OUT} = 500 mV LDO disabled		61		Ω

4.7.2 LDO3 Characteristics

Table 10: LDO3 electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External electrical conditions						
V_{IN}	LDO input voltage		2.4	3.6	5.5	V
C_{OUT}	Output capacitance	Effective output capacitance	0.34			µF
I_{OUT_MAX}	Maximum output current	$V_{IN} > V_{OUT}$ + 0.2 V	20			mA
Electrical performance						
V_{OUT}	Output voltage	$V_{IN} \geq V_{OUT}$ + 0.2 V I_{OUT} = 1 mA		1.8		V
V_{OUT_PP}	Output voltage part-to-part variation	$V_{IN} \geq V_{OUT}$ + 0.2 V I_{OUT} = 1 mA	-3		3	%
V_{OUT_UV}	Under voltage comparator	20 % below typical output voltage	1.29	1.44	1.59	V
AC Parameters						
$PSRR_{10Hz\_10kHz\_VIN}$	Power supply rejection ratio	f = 10 Hz to 10 kHz I_{OUT} = I_{OUT} (Max) V_{OUT} = V_{OUT} (Typ) V_{IN} = V_{IN} (Typ)	30	40	60	dB
E_N	Integrated output noise	f = 10 Hz to 100 kHz I_{OUT} = 1 mA		180		µV
Dynamic Parameters						
$t_{STARTUP}$	Startup time	Time to 90 % of V_{OUT_SET} I_{OUT} = 0 mA		1.1		ms
$V_{OUT\_TR\_LD}$	Load transient response	0 mA to I_{OUT_MAX}, t_{RISE} = t_{FALL} = 1 µs		53		mV
$V_{OUT\_TR\_LINE}$	Line transient response	V_{IN} = 3.8 V to 3.2 V I_{OUT} = 1 mA t_{RISE} = t_{FALL} = 10 µs		5.7		mV
Quiescent Current Specifications						
$I_{Q\_ON\_NO\_LD}$	Quiescent current, no load	I_{OUT} = 0 mA in normal Iq mode		0.77		µA
$I_{Q\_ON\_LO\_NO\_LD}$	Quiescent current, no load	I_{OUT} = 0 mA in low Iq mode		0.27		µA
$I_{Q\_ON\_1mA}$	Quiescent current, low load	I_{OUT} = 1 mA	15	28	40	µA
R_{PD}	Output pull-down resistance when OFF	V_{OUT} = 0.5 V		120		Ω

Parameter	Description	Conditions	Min	Typ	Max	Unit
Static Parameters						
$V_{OUT\_STATIC\_TOT}$	Output voltage total static accuracy	Part to part variation T_A = -40 °C to 85 °C $V_{IN} = V_{OUT} + V_{DROPOUT}$ to V_{IN} (Max) I_{OUT} = 1 mA to 100 mA $V_{OUT} = V_{OUT}$ (Typ)	1.75		1.86	V
$V_{OUT\_STATIC\_LINE}$	Static line regulation	V_{OUT} + 0.2 V < V_{IN} < 5.5 V, I_{OUT} = 1 mA	-0.4		0.8	%
$V_{OUT\_STATIC\_LD}$	Static load regulation	$V_{IN} \geq V_{OUT}$ + 0.2 V 0 < I_{OUT} < I_{OUT_MAX}	-1.5		1.5	%
$V_{OUT\_STATIC\_TOT\_\%}$	Output voltage total static accuracy	$V_{IN} \geq V_{OUT}$ + 0.2 V, 0 < T_J < 85 °C	-2.7		3.1	%
$V_{DROPOUT}$	Dropout voltage	$V_{OUT} = V_{OUT\_SET}$ - 10 mV $I_{OUT} = I_{OUT}$ (Max)			200	mV

4.7.3 LDO4 Characteristics

Table 11: LDO4 electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External electrical conditions						
V_{IN}	LDO input voltage		2.5	3.6	5.5	V
C_{OUT}	Output capacitance	Effective output capacitance	0.39			µF
I_{OUT_MAX}	Maximum output current		100			mA
Programmable conditions						
V_{OUT}	Selectable output voltage	Step size 5 mV	1.2	3.3	3.3	V
Electrical performance						
Static Parameters						
$V_{OUT\_STATIC\_TOT}$	Overall static output accuracy	V_{OUT} = 3.3 V Part to part + temperature + static line regulation	-3		2.5	%
V_{OUT_TEMP}	Temperature dependence of V_{OUT}	I_{OUT} = 1mA $V_{OUT} = V_{OUT}$ (Typ)	-1		1	%
$V_{DROPOUT}$	Dropout voltage	$V_{OUT} = V_{OUT\_SET}$ - 10 mV $I_{OUT} = I_{OUT}$ (Max)			200	mV
Dynamic Parameters						
$t_{STARTUP}$	Startup time	Time to 90 % of V_{OUT_SET} I_{OUT} = 0 mA			1	ms
$V_{OUT\_TR\_LINE}$	Line transient response	$V_{IN} = V_{OUT} + V_{DROPOUT}$ + 100 mV to $V_{IN} = V_{OUT} + V_{DROPOUT}$ V_{OUT} = Min to Max $I_{OUT} = I_{OUT\_MAX}$ $t_{RISE} = t_{FALL}$ = 1 µs	-20		20	mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{OUT\_TR\_LD}$	Load transient response	I_{OUT} = 1 mA to I_{OUT_MAX} t_{RISE} = t_{FALL} = 1 µs	-50		50	mV
Quiescent Current Specifications						
$I_{Q\_ON\_0mA}$	Quiescent current, no load	I_{OUT} = 0 mA		4		µA
R_{PD}	Output pull-down resistance in OFF	V_{OUT} = 0.5 V LDO disabled		80		Ω

4.8 ISINK - LED Driver Characteristics

Table 12: ISINK electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Programmable conditions						
I_{OUT}	Programmable output current range per sink		0.05		12.8	mA
f_{PWM}	PWM frequency		0.001		1	kHz
Electrical performance						
I_{OUT_ACC}	Absolute output current accuracy	T_A = 25 °C V_{SINK} = 0.2 V I_{SINK} = 3.3 mA	-2		2	%
V_{OUT}	Absolute operating voltage of the sink		0		5.5	V
$V_{DROPOUT}$	Dropout voltage above which sink operates in regulation		0.2			V
I_Q	Quiescent current per active current sink			5	15	µA

4.9 Power Path Management Electrical Characteristics

Table 13: Power-path management electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Programmable conditions						
V_{SYS_RNG}	VSYS output voltage	Programmable in 100 mV steps	3.2		4.8	V
$V_{CHG\_DPM\_RNG}$	DPM voltage threshold	Programmable in 100 mV steps	4.2		4.9	V
$I_{VCHG\_IN\_LIM\_RNG}$	Input current limit	Programmable in 25 mA steps	0		600	mA
Electrical performance						
$V_{CHG\_IN\_DPM\_ACC}$	DPM voltage threshold accuracy		-3		3	%
R_{ON}	On resistance VCHG_IN to VSYS	SYS LDO in pass-through mode, I_{CHG_IN} = 150 mA, V_{CHG_IN} = 3.6 V		280		mΩ
V_{SYS_ACC}	VSYS static accuracy	V_{SYS} = 4.5 V I_{CHG_IN} = 0 to 500 mA	-4		4	%
$I_{CHG\_IN\_LIM\_ACC}$	Input current limit accuracy	$I_{CHG\_IN\_LIM}$ = 500 mA		500	550	mA

4.10 Battery Charger Electrical Characteristics

Table 14: Battery charger electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Programmable conditions						
$I_{BAT\_DCHG\_RNG}$	Discharge current limit setting range	Programmable	0.15		2	A
V_{BAT_CHG}	Charge voltage range	Operating in voltage regulation, programmable in 10 mV steps	3.6		4.65	V
I_{CHG}	Fast charge current range		2.5		500	mA
$I_{TER\_5\%}$	Termination charge current 5 % of ICHG		0.125		25	mA
$I_{TER\_10\%}$	Termination charge current 10 % of ICHG		0.25		50	mA
$I_{TER\_20\%}$	Termination charge current 20 % of ICHG		0.5		100	mA
$I_{TER\_35\%}$	Termination charge current 35 % of ICHG		0.875		175	mA
$I_{PRE\_CHG\_RNG}$	Pre-charge current range	Note 1	0.5		64	mA
V_{RCHG}	Recharge threshold voltage range	V_{BAT} below V_{BAT_CHG} - 2 programmable thresholds	140		300	mV
$V_{VSYS\_DPPM\_THR}$	VSYS DPPM voltage threshold	V_{SYS} falling, relative to V_{BAT} Programmable in 50 mV steps	100		250	mV
$V_{PRE\_TO\_FAST\_CHG\_THR}$	Pre charge to fast charge threshold voltage range	V_{BAT} rising Programmable in 100 mV steps	2.7		3.4	V
Electrical performance						
$R_{ON\_CHG\_INT}$	Battery charger MOSFET on-resistance	Measured from V_{BAT} to V_{SYS} V_{BAT} = 4.35 V, I_{BAT} = 100 mA			175	mΩ
$V_{VBAT\_SM\_THR}$	Threshold to enter the battery supplement mode	$V_{VBAT} > V_{VBAT\_UVLO}$		VSYS < VBAT		V
$V_{BAT\_CHG\_ACC}$	Charge voltage accuracy	0 °C < T_J < 85 °C	-0.5		0.5	%
I_{CHG_ACC}	Fast charge current accuracy	I_{CHG} > 5 mA T_A = 25 °C	-5		5	%
$I_{PRE\_CHG\_ACC}$	Pre-charge current accuracy	V_{BAT} > 2 V	-10		10	%
I_{TER_ACC}	Termination charge current accuracy	I_{TER} = 10 mA T_A = 25 °C	-10		10	%

Note 1 See CHG_IPRECHG_CFG in register map

4.11 Battery Temperature Sensor Characteristics

Table 15: Battery temperature sensor characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical performance						
V_{TEMP_HOT}	Hot temperature threshold	% of V_{SYS},NTC_SNS falling	14.5	15	15.2	%
V_{TEMP_WARM}	Warm threshold	% of V_{SYS},NTC_SNS falling	20.1	20.5	20.8	%
V_{TEMP_COOL}	Cool threshold	% of V_{SYS},NTC_SNS rising	34.4	35	35.4	%
V_{TEMP_COLD}	Cold temperature threshold	% of V_{SYS}, NTC_SNS rising	39.3	39.8	40.2	%
$V_{OFF\_TEMP\_SNS}$	NTC_SNS disable threshold	% of V_{SYS} for rising NTC_SNS	55		60	%
$t_{TEMP\_SNS\_DEGLITCH}$	NTC_SNS deglitch time	NTS_SNS at any threshold		10		ms

4.12 Protection Electrical Characteristics

Table 16: Protection electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Programmable conditions						
T_{WARN_RNG}	Warning temperature	T_J, Programmable in 10 °C steps	70		100	°C
Electrical performance						
$V_{BAT\_SHRT\_THR}$	Battery voltage short detection threshold	V_{BAT} falling, V_{CHG_IN} = 5 V Note 1		2		V
$V_{BAT\_SHRT\_HYS}$	Battery voltage short detection hysteresis			100		mV
$V_{BAT\_UVLO\_THR}$	Battery under-voltage lockout threshold range	Programmable range 100 mV steps V_{BAT} falling	2.5		3	V
$V_{BAT\_UVLO\_ACC}$	Default battery under-voltage lockout accuracy	V_{BAT_UVLO} = 2.5 V	-3		3	%
$V_{BAT\_UVLO\_HYS}$	Battery under-voltage lockout threshold hysteresis			200		mV
$V_{CHG\_IN\_OV}$	V_{CHG_IN} over-voltage protection threshold voltage	V_{CHG_IN} rising	5.5		5.85	V
$V_{CHG\_IN\_OV\_HYS}$	Over-voltage protection hysteresis			100		mV
V_{SLP}	Sleep entry threshold	V_{CHG_IN} - V_{BAT} V_{CHG_IN} falling		85	145	mV
V_{SLP_HYS}	Sleep mode hysteresis	V_{CHG_IN} rising	80	130	200	mV
$V_{SYS\_UVLO\_THR}$	V_{SYS} under-voltage lockout threshold	V_{VSYS} falling		2.5		V
$V_{CHG\_IN\_UVLO\_THR}$	V_{CHG_IN} under-voltage lockout threshold	V_{CHG_IN} rising	3.3		3.6	V
$V_{CHG\_IN\_UVLO\_HYS}$	V_{CHG_IN} under-voltage lockout threshold hysteresis	V_{CHG_IN} falling		150		mV
T_{SHDN}	Thermal shutdown	T_J		125		°C

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_{HYS}	Thermal shutdown hysteresis	T_J		20		°C

Note 1 Charge current is reduced to IPRE_CHG

4.13 Interface Characteristics

Table 17: Interface electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical performance						
I2C						
V_{IL}	Input low voltage	V_{DDIO} = 1.8 V			0.54	V
V_{IH}	Input high voltage	V_{DDIO} = 1.8 V	1.26			V
V_{OL}	Output low voltage	V_{DDIO} = 1.8 V, I_{LD} = 5 mA			0.45	V
RIN_N Input						
V_{IL}	Input low voltage				0.3	V
R_{PU}	Internal pull-up resistance	Pull-up to max(VCHG_IN, VBAT)		18.8		kΩ
CHG_EN_N, WUP, WUP2 Inputs						
V_{IL}	Input low voltage	V_{DDIO} = 1.8 V			0.45	V
V_{IH}	Input high voltage	V_{DDIO} = 1.8 V	1.35			V
GPIO1/2/3/4						
V_{IL}	Input low voltage	V_{DDIO},V_{DDIO2} = 1.8 V			0.45	V
V_{IH}	Input high voltage	V_{DDIO},V_{DDIO2} = 1.8 V	1.35			V
V_{OL}	Output low voltage	V_{DDIO},V_{DDIO2} = 1.8 V, I_{LD} = 1 mA			0.3	V
V_{OH}	Output high voltage	V_{DDIO},V_{DDIO2} = 1.8 V, I_{LD} = 1 mA	1.5			V
R_{PD}	Internal pull-down resistance	GPIOx_PUPD = 0x2		75		kΩ
IRQ_N Output						
V_{OL}	Output low voltage	V_{DDIO} = 1.8 V, I_{LD} = 1 mA			0.3	V
SYSRST_N Output						
V_{OL}	Output low voltage	V_{DDIO} = 1.8 V, I_{LD} = 1 mA			0.3	V
V_{OH}	Output high voltage	V_{DDIO} = 1.8 V, I_{LD} = 1 mA	1.5			V
R_{PU}	GPIO pull-up resistor			75		kΩ

4.14 Timing Characteristics

Table 18: Timing characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Timing characteristics						
Battery Charge Timers						
t_{MAXCHG}	Charge safety timer	Programmable	120	150	540	min
t_{PRECHG}	Pre-charge safety timer			0.25*tMAXCHG		min
Watchdog Timers						
t_{WD_A}	Watchdog timer A	Programmable	1	10	120	s
t_{WD_B}	Watchdog timer B	Programmable	0.1	0.1	4	s
Power Sequence Timers						
t_{CH_EN}	Channel enable timer	Programmable	2		64	ms
Pushbutton Timers						
t_{WAKE1}	Wake1 timer	From RIN_N falling edge to nIRQ being asserted Programmable	0.5		4	s
t_{WAKE2}	Wake2 timer	From RIN_N falling edge to nIRQ being asserted Programmable	1	2	2	s
t_{RST}	Reset timer	Programmable	4	8	14	s
t_{RST_WARN}	Reset warn timer	Time prior to HW reset. Programmable	0.5	1	2	s
$t_{AUTOWAKE}$	Autowake timer	Off-time in power cycle until automatic wake occurs Programmable	0.6	0.6	5	s
TWARN						
t_{TWARN}	TWARN safety timer	Wait time for response on TWARN event Programmable	1	1	16	s
Protection						
t_{DEB_SLP}	Sleep debounce time	Debounce time for VCHG_IN rising above the V_{SLP} + V_{SLP_HYS}		120		µs
$t_{DEB\_VCHG\_IN\_UVLO}$	Debounce time for $V_{CHG\_IN\_UVLO}$ threshold	VCHG_IN rising above the $V_{CHG\_IN\_UVLO}$		120		µs
$t_{DEB\_VCHG\_IN\_OVP}$	Debounce time for $V_{CHG\_IN\_OVP}$ threshold	VCHG_IN falling below $V_{CHG\_IN\_OVP}$		32		ms
$t_{DEB\_VBAT\_UVLO}$	Debounce time for V_{BAT_UVLO} threshold	VBAT rising above V_{BAT_UVLO} + $V_{BAT\_UVLO\_HYS}$		250		ms

4.15 Thermal Characteristics

Table 19. Thermal characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{Θ_JA}	Junction to ambient thermal resistance	JEDEC 4-layer PCB, no airflow, T_A = 85 °C		38.2		ºC/W

5. Functional Description

The operating states and transitions of the system state machine are shown in Figure 3.

5.1 System State Machine

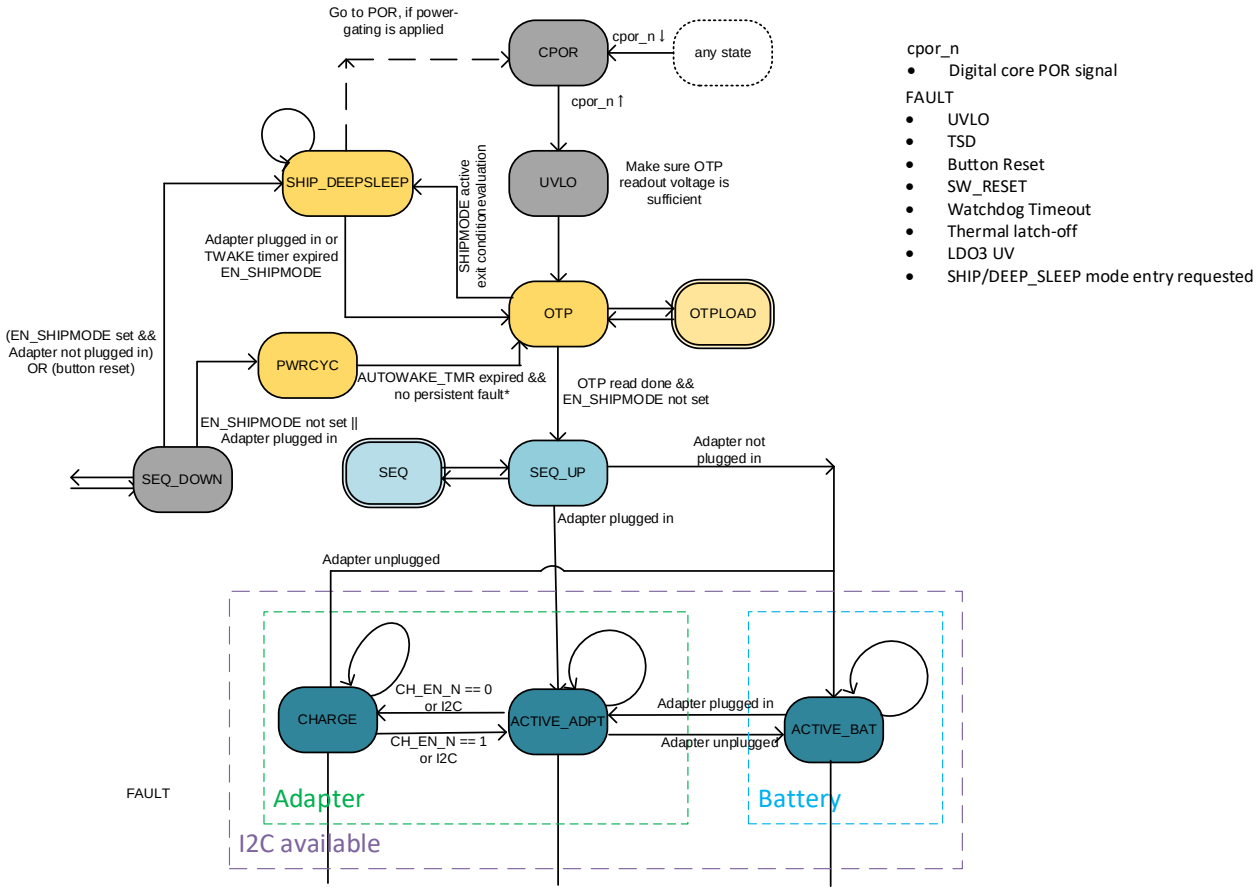


Figure 3. DA9098 MFSM diagram

5.1.1 First Startup and SHIP Mode Entry/Exit

When the battery is inserted (or a valid VCHG_IN is present), DA9098 will transition out of reset. After checking for the proper voltage to make sure the OTP readout can be done, the OTP is read, and the device goes through a sequence to the ACTIVE_BAT state back to SHIP mode via the "FAULT" transition through the SEQ_DOWN sequence.

A device that has already been woken from SHIP mode and is in an ACTIVE state, can later on by SHIP mode entry request (setting the EN_SHIPMODE bit and removing the adapter) be sent back to SHIP mode through the FAULT transition as well. Note that a fault occurring at the same time as a SHIP mode entry request has precedence over the SHIP mode request, thus the power cycle will be done first. Once the device is going back to ACTIVE, the still active EN_SHIPMODE bit will trigger the transition to SHIP mode.

After entering the SHIP mode, the FSM does a handshake with a SHIP mode block and after this the main digital core will be shut off.

If a condition to wake from SHIP mode applies (a button pressed or VCHG_IN applied), the main digital core is activated and goes, after an OTP read, into SHIP_DEEPSLEEP state to detect the condition (wake timer) or valid VCHG_IN or another valid wake source. In case the wake condition is not fulfilled, the main digital core will do a handshake again and will be turned off. If the condition is fulfilled, the EN_SHIPMODE bit is cleared and the device goes through a sequence to activate the rails to an ACTIVE state (ACTIVE_BAT or ACTIVE_ADPT, depending on the presence of a valid VCHG_IN).

5.1.2 Startup Sequence

In the SEQ_UP state the rails and GPIOs are activated in the configured sequence. Once the sequence is done, the FSM automatically moves forward to an ACTIVE state. If an adapter is present this is the ACTIVE_ADPT state, otherwise the ACTIVE_BAT state.

In case the adapter is removed while in startup to adapter state, there will be a 15 ms timeout time, followed by a power cycle and then the device will start in battery mode.

5.1.3 ACTIVE Modes and Transitions

There are two groups of ACTIVE modes: ACTIVE with only the battery present or ACTIVE with a valid VCHG_IN (adapter plugged in).

The transition between the two groups happens whenever an adapter is plugged in or removed, independent of the sub-state in the group, (that is, CHARGE can go to ACTIVE_BAT by removing the adapter without register CH_EN_N_EN or pin CH_EN_N having to go high).

If the adapter is plugged in or removed, an event EVT_ADAPTER is generated. In STA_ADAPTER, the status (attached or detached) can be read. The event can be masked from the IRQ_N using IRQ_ADAPTER.

If the bit EMULATE_ADAPTER_DETACH in register SYSCTRL_CONFIG_0 is set, the adapter is emulated to be detached. With this, the system would always use the power from the battery, even if an adapter is connected. This will prevent the CHARGE and ACTIVE_ADPT states from being entered, as those require an adapter to be connected.

The I^2C interface is available in all these ACTIVE states.

5.1.3.1 ACTIVE_BAT

This is the main ACTIVE state for battery operation with no VCHG_IN attached.

The transition from ACTIVE_BAT to ACTIVE_ADPT is triggered by plugging in an adapter, the transition back by removing the adapter.

5.1.3.2 ACTIVE_ADPT

This is the main ACTIVE state for adapter-supplied operation with VCHG_IN attached.

The transition from ACTIVE_ADPT to CHARGE is triggered by I^2C by writing bit CH_EN_N_EN (default) or the CH_EN_N pin going low, the transition back by I^2C (default) or CH_EN_N pin going high.

The transition from ACTIVE_ADPT to ACTIVE_BAT is triggered by removing the adapter, the transition back by plugging in an adapter.

5.1.3.3 CHARGE

In this ACTIVE mode charging is enabled and executed depending on the battery voltage, charge current, temperature and related settings. More details about the charge operation can be found in the charger chapter.

All these modes can exit to the SEQ_DOWN sequence by a fault (or desired reset) or if EN_SHIPMODE is set and the device is in ACTIVE_BAT state.

5.1.4 SEQ_DOWN Sequence

In case of a fault or if EN_SHIPMODE is high in ACTIVE_BAT state, the FSM moves to a sequence to shut down the rails and deactivates the GPIOs. After the sequence is finished, the FSM moves forward automatically.

If the transition is triggered by button reset, the device will move to SHIP mode.

In case EN_SHIPMODE is set and no adapter is plugged in, it moves to the SHIP_DEEPSLEEP state and activates the SHIP or deep sleep mode from there.

In any other case the device reloads all OTP settings. Locked registers (for example ICHG_MAX) are not being cleared or overwritten by OTP load.

5.1.5 Power Up/Down Sequences

When the device starts up, it goes into the SEQ_UP state. In this state the rails are automatically powered up according to the settings defined in the following registers:

- MFSM_PWRSEQ_CHANNELS_0/1: This register contains enable bits for every available channel. These are the configurable rails, the GPIOs and SYSRST_N. If the EN bit of the channel is set, it will be activated in the power-up sequence.
- MFSM_PWRSEQ_CHANNELS_ENDLY_0/1/2/3/4/5/6: The activation of the channel can happen at one of the configurable times to allow channels to start in a sequence. Each channel has its own *_ENDLY register.

If the device needs to switch off due to a reset, fault condition, DEEPSLEEP, or SHIP mode entry, the SEQ_DOWN sequence powers down the rails in a sequenced manner. The delay for shutting down can be chosen from eight settings for each channel in registers MFSM_PWRSEQ_CHANNELS_DISDLY_0/1/2/3/4/5/6 by using the *_DISDLY setting.

If a power cycle is done (rather than going down to DEEPSLEEP or SHIP mode), the device will keep the rails off for the time configured in AUTOWAKE_TMR. If a fault, like overtemperature or UVLO, caused the shutdown or becomes active after the shutdown, the device may stay off longer until the fault conditions are gone. If DIS_LDO3_IN_PWR_CYC is not set, LDO3 will be re-enabled at the end of the AUTOWAKE time, unless a thermal fault condition (TSD) is present. This is done to ensure the button can be supplied to be able to clear thermal latch-off conditions. After this, the LDO3 enable/disable will be defined by the enable condition for the power sequence.

In the ACTIVE modes the Host can use the enable bits in MFSM_PWRSEQ_CHANNELS_0/1 to turn on and off channels selectively. These will not use the ENDLY/DISDLY, as those are only applicable in the power sequences.

Note: A transition to DEEPSLEEP will keep SYSRST_N high, and LDO3 ON. Refer to section 5.1.7 for details about DEEPSLEEP mode.

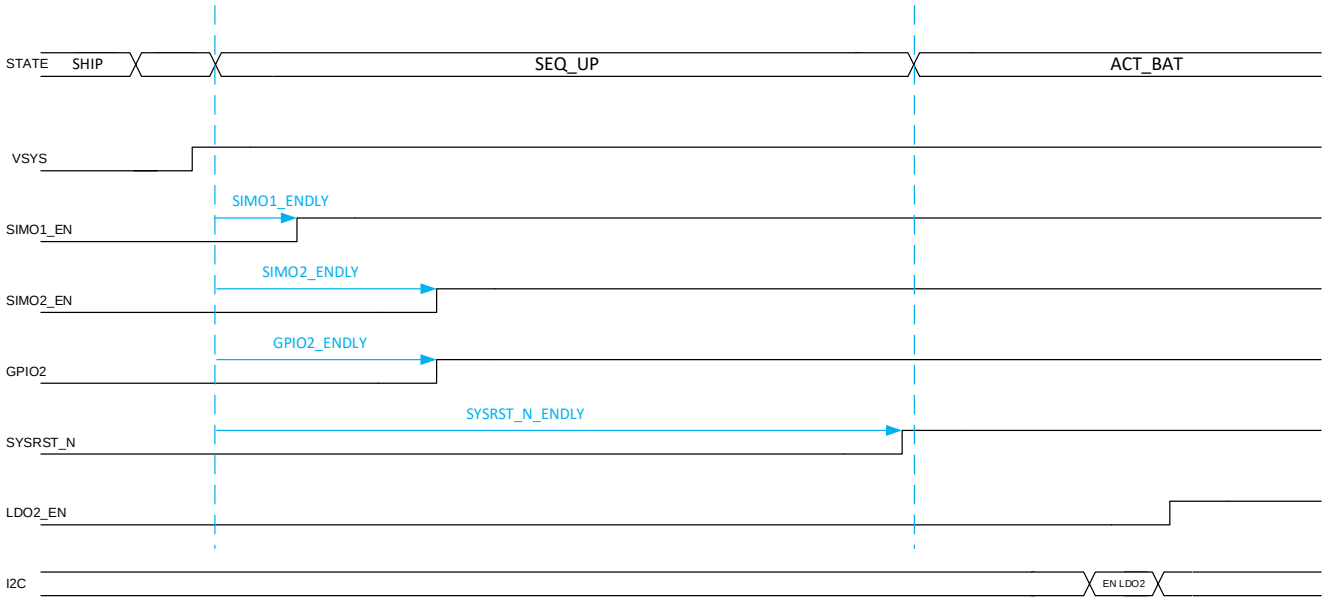


Figure 4. Example of a power-up sequence (SHIP to ACTIVE). LDO2 is enabled later on via I²C

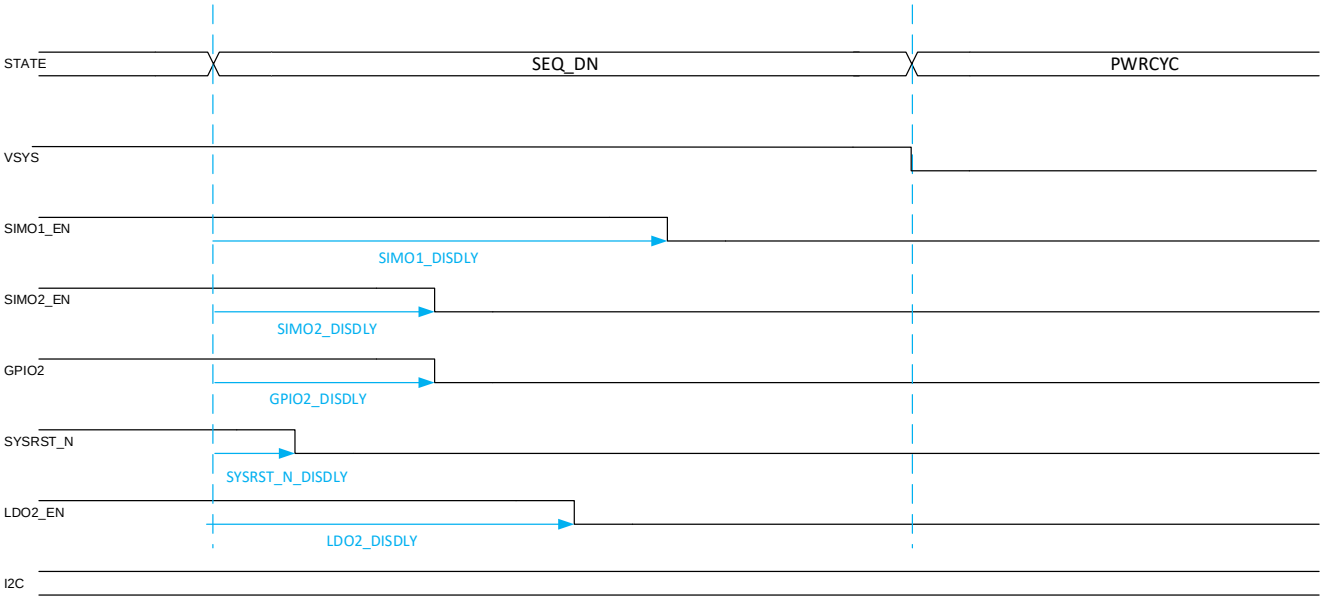


Figure 5. Example of a power-down sequence. LDO2 sequenced down according to the DISDLY setting

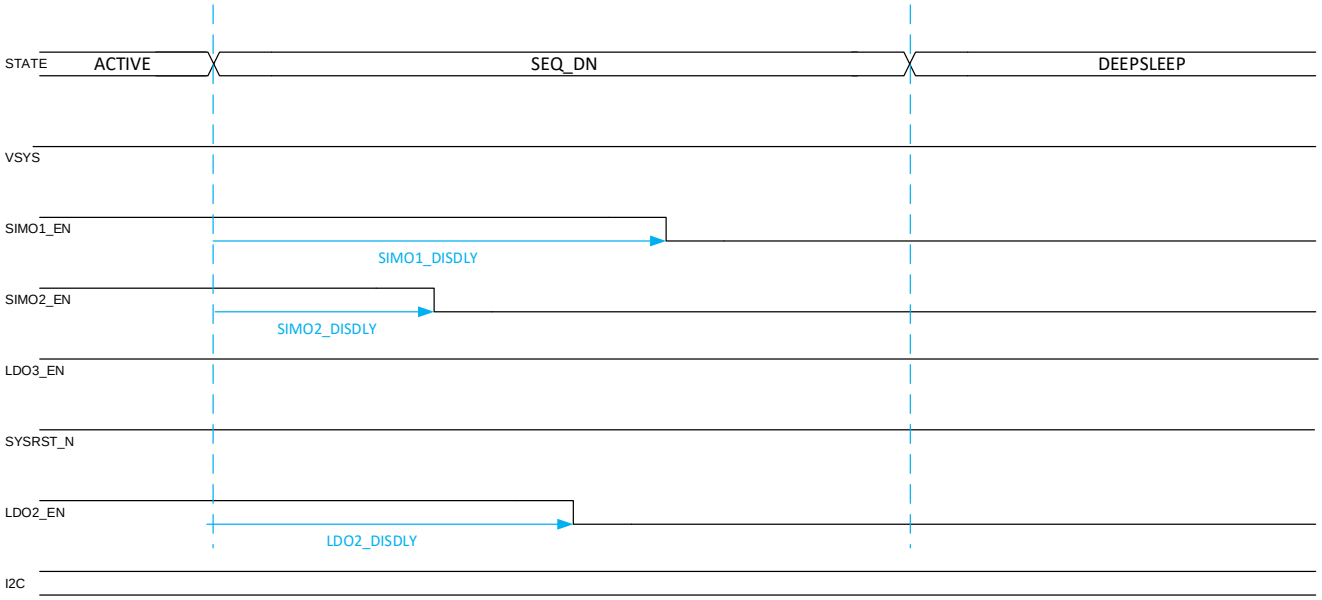


Figure 6. Example for ACTIVE to DEEPSLEEP (EN_SHIPMODE=1, EN_DEEPSLEEP=1)

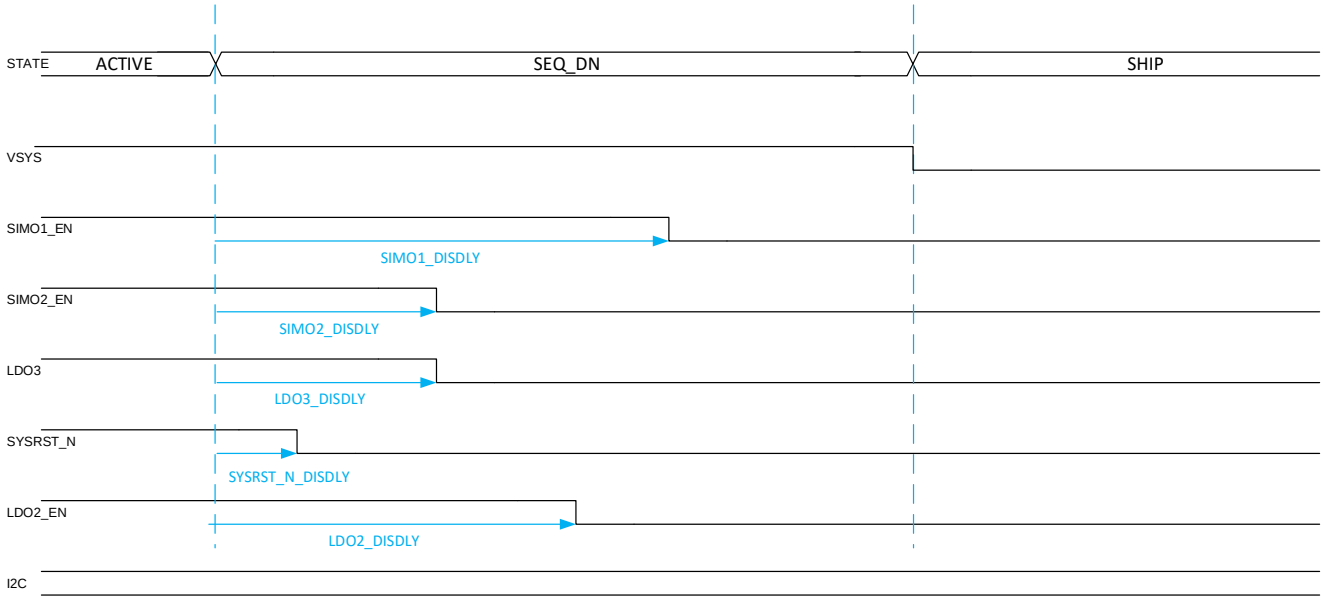


Figure 7. Example of ACTIVE to SHIPMODE (EN_SHIPMODE=1, EN_DEEPSLEEP=0)

5.1.6 SHIP Mode

SHIP mode is an ultra-low current standby state that minimizes battery depletion while the product sits on the shelf.

DA9098 can be sent to SHIP mode from the ACT_BAT state by setting bit EN_SHIPMODE with I²C.

SHIP mode is also entered with a button reset (see section 5.1.9)

In SHIP mode all the supply rails are turned off, I²C communication and the digital logic are also disabled and very low I_Q is achieved.

The device will wake-up when:

- VCHG_IN, charger input voltage, is detected
- RIN_N button is pressed for tWAKE1

When a battery is attached to the device for the first time, the device will automatically wake up to ACTIVE and then move to SHIP mode. It then needs to be woken up from one of the above sources.

5.1.7 DEEPSLEEP Mode

D9098 can enter DEEPSLEEP mode by a command from SoC via digital interface (I²C).

In this mode, all the power rails but the low-IQ always-on LDO3 are off.

Digital is turned off, and I²C communication is disabled.

The suggested steps for a DEEPSLEEP mode entry request are:

1. Set EN_DEEPSLEEP (Register IO_EN_DEEPSLEEP)
2. Set EN_SHIPMODE (Register MFSM_MFSM_CTRL1)

In case DA9098 is requested to enter DEEPSLEEP mode with a charger input present, the bitfield EMULATE_ADPT_DETACH can be used before the DEEPSLEEP mode entry request. It will emulate an adapter detach, even though the input voltage is presented.

The wake-up sources from DEEPSLEEP mode are:

- RIN_N button if kept pressed for tWAKE1, falling edge
- VCHG_IN charger input voltage, rising edge
- WUP IO pin, positive edge detection
- WUP2 IO pin, programmable edge detection
- LDO3 UV detection

The signal that triggers the wakeup must remain asserted until the digital controller has achieved startup.

Once DEEPSLEEP exit sequence is finished, EN_DEEPSLEEP shall be reset.

In DEEPSLEEP mode, the battery switch shall stay on, to maintain VSYS.

In DEEPSLEEP mode, SYSRST_N shall stay asserted.

Several DEEPSLEEP options can be configured with OTP registers:

a. LDO3 low/normal power mode (LDO3_EN_LOWIQ in SYSCTRL_DEEPSLEEP_CONF0)
b. LDO3 UV enable (LDO3_EN_LOWIQ in SYSCTRL_DEEPSLEEP_CONF0)
c. GPIO1-4 configuration in DEEPSLEEP (register IO_DEEPSLEEP_CONFIG1-5)
d. CHG Over Current Protection (CHG_EN_OCP in register SYSCTRL_DEEPSLEEP_CONF1)
e. Battery UVLO selection and threshold configuration (BATUVLO_SEL_VFALL in SYSCTRL_DEEPSLEEP_CONF1)

5.1.7.1 LDO3 UV in DEEPSLEEP

LOD3 UV detection can be enabled in deep sleep mode with bit LDO3_EN_UVLO (register SYSCTRL_DEEPSLEEP_CONF0). If an UV condition occurs in deep sleep mode, wake-up shall take place. The UV condition will be latched for the digital logic. In case an LDO3 UV event happened in deep sleep mode, it can be read back from event bit EVT_DEEPSLEEP_LDO3_UV.

The HOST must clear event bit EVT_DEEPSLEEP_LDO3_UV in ACTIVE state.

If the UV condition is still present when the digital controller has achieved startup and the host has cleared bit EVT_DEEPSLEEP_LDO3_UV, the device shall power cycle all rails.

If the host cannot communicate, the watchdog circuit will initiate the power cycle. If at the end of the power cycle LDO3_UV condition is present, the POWER up sequence will not be performed. The user can initiate a hard reset by pressing RIN_N.

If keeping LDO3 constantly on after waking up from DEEPSLEEP mode is not desired, the EN_DEEPSLEEP bit should be cleared. The same applies for LDO3_EN_UVLO.

5.1.7.2 Bat UVLO & TSD in DEEPSLEEP

If fault conditions bat_uvlo or TSD occur while in DEEPSLEEP mode, the device will transition to SHIP mode, i.e. turn off LDO3 and reset SYSRST_N.

A TSD event in DEEPSLEEP mode is stored and can be read back from EVT_SHIP_TSD when the digital will wake-up next time.

To leave SHIP mode, the usual wake-up sources RIN_N press or VCHG_IN can be used

5.1.8 CHG_EN_N

The pin CHG_EN_N is an active-low pin used to allow charging, if a power source is connected, VCHG_IN is within valid ranges, and no charging fault is present.

The pin is by default overruled by a bitfield. To select between pin or bitfield (default), the bitfield CHG_EN_N_SEL in register CHG_CHG_EN_N_0 can be used. To stimulate the CHG_EN_N behavior in case bitfield is selected, the bitfield CHG_EN_N_EN is used.

5.1.9 Push Button Interface (RIN_N)

RIN_N has a push button wake-up and reset timer function. There are three programmable wake-up and reset timers, namely, WAKE1, WAKE2 and RESET timers as listed in Table 20.

Table 20. Push button wake-up timers and control registers

Name	Period	Timer control register
WAKE1	t_{WAKE1}	RIN_N_PER_WAKE1
WAKE2	t_{WAKE2}	RIN_N_PER_WAKE2
RESET	t_{RST}	RIN_N_PER_RST[1:0]

Each time the timer hits the programmable count, an interrupt will be sent by pulling IRQ_N output low and corresponding event registers are set to show how long RIN_N was pressed as shown in Table 21, Figure 8, and Figure 9.

Table 21. Manual reset timer event registers

Period	Status register
t_{WAKE1}	EVT_RIN_N_WAKE1_TIMEOUT
t_{WAKE2}	EVT_RIN_N_WAKE2_TIMEOUT
t_{RST}	EVT_RESET_WARN will fire at t_{RST}, t_{RST_WARN} before a power-cycle

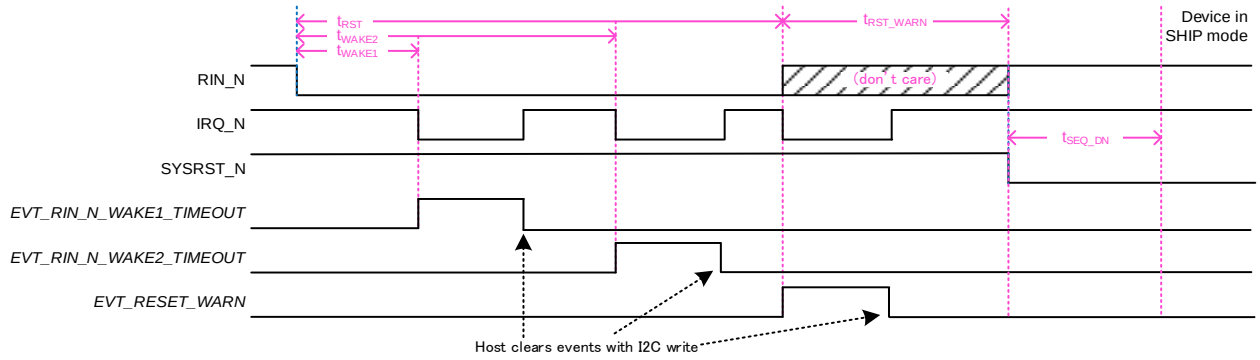


Figure 8. Manual reset to SHIP timing diagram (BUTTON_HARD_RESET_EN=1)

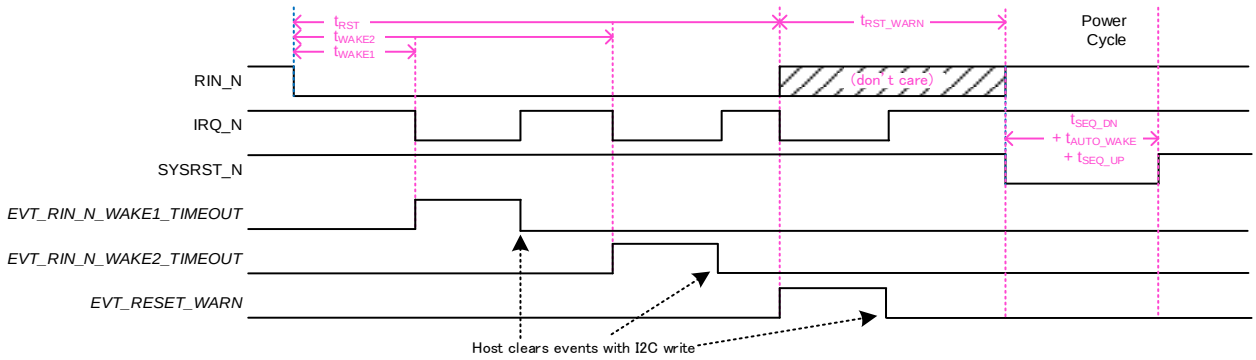


Figure 9. Manual reset to POWER CYCLE timing diagram (BUTTON_HARD_RESET_EN=0)

The bitfield RIN_N_RST_EN (register IO_RESET_WARN) can be used to disable this feature. This will not only disable the reset itself, but also the WAKE1/2 events. If this feature is disabled via this bit in OTP, wakeup from SHIP or DEEPSLEEP mode by button will not work. If enabled in OTP, on SHIP or DEEPSLEEP mode exit the default setting (feature enabled) is loaded.

This bit can be used to stop an upcoming reset (once the HOST has been notified by the event EVT_RESET_WARN); after that the feature should be re-enabled to allow the various button events to be raised again.

OTP register bit BUTTON_HARD_RESET_EN can be used to configure the reset behavior:

BUTTON_HARD_RESET_EN = 0: The device will perform a power cycle

BUTTON_HARD_RESET_EN = 1: The device will go to SHIP mode as soon as an ongoing MFSM transition finishes, and the device enters a stable state.

5.1.10 SW Reset

The Host can trigger a power cycle, which will reset the Host and reload all OTP registers in the PMIC and then power up again, by writing to the SW_RESET bit (register MFSM_MFSM_CTRL1). Note that the shutdown will

start as soon as the bit is written, which may be before the I²C frame ends, thus the acknowledge might be missing.

5.1.11 General Purpose Input Output

The device contains four general purpose input outputs (GPIOs). The GPIOs can be configured to be inputs or outputs (GPIO1/2/3/4_IO_CONFIG).

GPIO1, and 2 are VDDIO supplied, while GPIO3, and 4 are VDDIO2 supplied.

As an input, they can be configured to be level (high, low) or edge (rising, falling, both) sensitive (in GPIO1/2/3/4_IO_TYPE) and generate an event after a programmable debounce (GPIO1/2/3/4_DEB) of the input.

As an output the GPIOs can be configured as open-drain or push-pull output (GPIO1/2/3/4_IO_CONFIG) and the output can be set to high or low value (GPIO1_OUT_LVL).

GPIO1 has an additional special feature. It can generate a pulse on button press (once WAKE1 timer expires) or on other wakeup sources. This feature is enabled with GPIO1_ADP_DET_PLS_EN and the pulse length is configured in GPIO1_ADP_DET_PLS. In case the GPIO output is configured to be at low level, the pulse will be generated as high level, if the GPIO is configured to be at high level, the pulse will be generated as low level. If this feature is desired to be used already for SHIP mode wakeup notification, then this is required to be configured like this in OTP (as I²C is only available after startup).

The GPIOs can be used in the power sequence (for GPIO1 only useful, if it is not configured to the GPIO1_ADP_DET_PLS_EN pulse feature) by setting MFSM_PWRSEQ_CHANNELS_0 bits GPIO1/2/3/4_EN to 1.

The startup delay (point in time in the SEQ_UP sequence, where the GPIO is set) is defined in registers MFSM_PWRSEQ_CHANNELS_ENDLY_4/5 in the bitfields GPIO1/2/3/4_ENDLY.

The shutdown delay (point in time in the SEQ_DOWN sequence, where the GPIO is cleared) is configured in register MFSM_PWRSEQ_CHANNELS_DISDLY_4/5 in bitfields GPIO1/2/3/4_DISDLY.

The GPIOs are set to their respective levels in the SEQ_UP/SEQ_DOWN by inverting the default level configured for this GPIO in GPIO*_OUT_LVL. To allow this to work for the power-up sequence the GPIO configuration and sequence configuration must be defined in OTP already. If the power sequencer enable bit is set (GPIO1/2/3/4_EN), the output level is the inverted value of the value defined in GPIO1/2/3/4_OUT_LVL, until the power-up time is reached, then it changes to the defined level. At power down it will revert back to the inverted value.

If the power sequencer configuration is not enabled at all for the GPIO, its level is always the inversion of the setting in GPIO1/2/3/4_OUT_LVL. This is a side effect of how this IP works together with the power sequencer.

When the device is in deep sleep mode and the main digital core is in reset, the 4 GPIOs can be configured by a set of always on registers according to Figure 10.

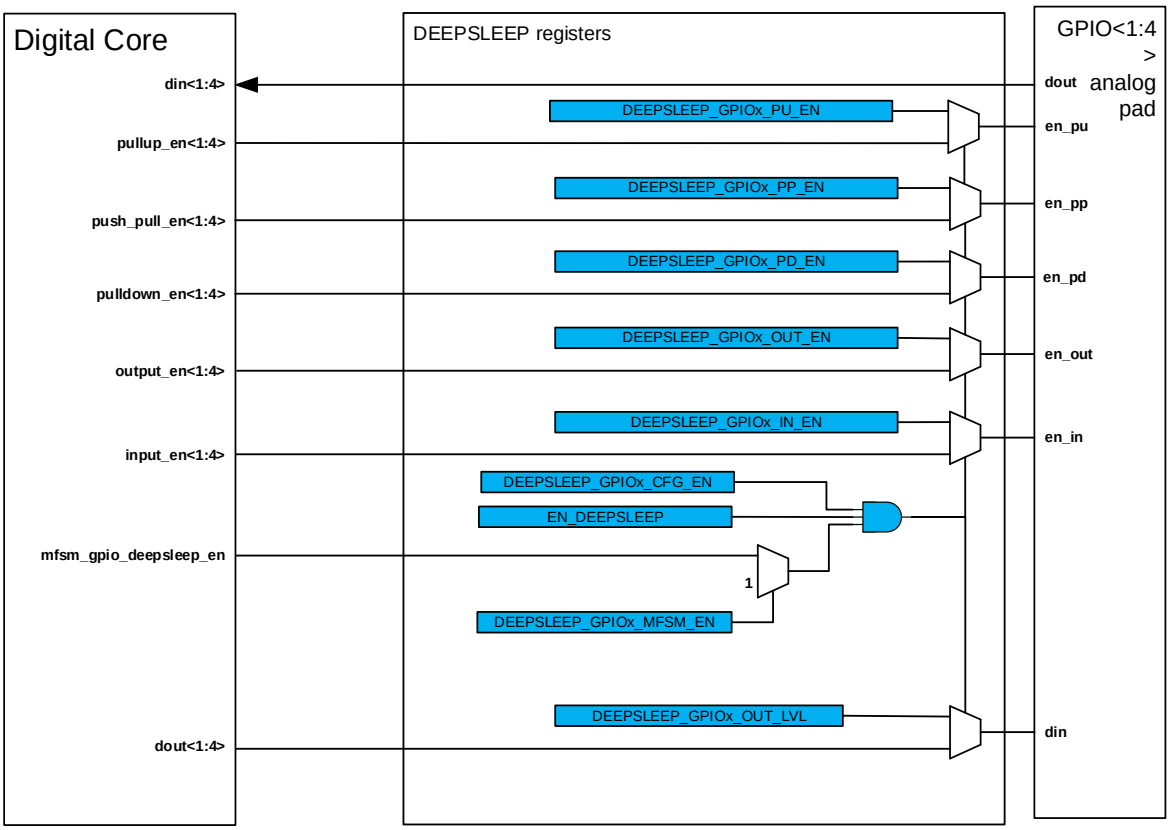


Figure 10. DEEPSLEEP registers for the 4 GPIOs

These registers will reset to 0 in SHIP mode. They will not reset in DEEPSLEEP. These registers are not loaded by OTP. The HOST must configure these registers before starting a transition to DEEPSLEEP. These registers will keep their value until the device wakes from DEEPSLEEP to ACTIVE. Then, the HOST can change their values over I^2C.

MFSM will provide a signal (mfsm_gpio_deepsleep_en, POR value=1) based on MFSM states, to determine when control can switch to the always on registers. Bit DEEPSLEEP_GPIOx_MFSM_EN can be used to disable the control from MFSM (i.e. control will be always static if this bit is 0 and bit EN_DEEPSLEEP is 1). When bit DEEPSLEEP_GPIOx_MFSM_EN is 1, the IO configuration will be static in DEEPSLEEP mode and dynamic otherwise.

5.1.12 Watchdog Reset

A programmable watchdog timer is available to detect a stall of a host by monitoring host activity on the I^2C I/F. The watchdog can be enabled by setting WD_EN to 1. If there is no communication for t_{WD_A} (configured with register field WD_TIMER_A), the device flags a watchdog event in EVT_WD_TO and the IRQ_N pin (unless the event is masked from the IRQ_N using IRQ_WD_TO). After this a second timer starts running.

If t_{WD_B} (configured with register field WD_TIMER_B) passes without communication, a power cycle is initiated.

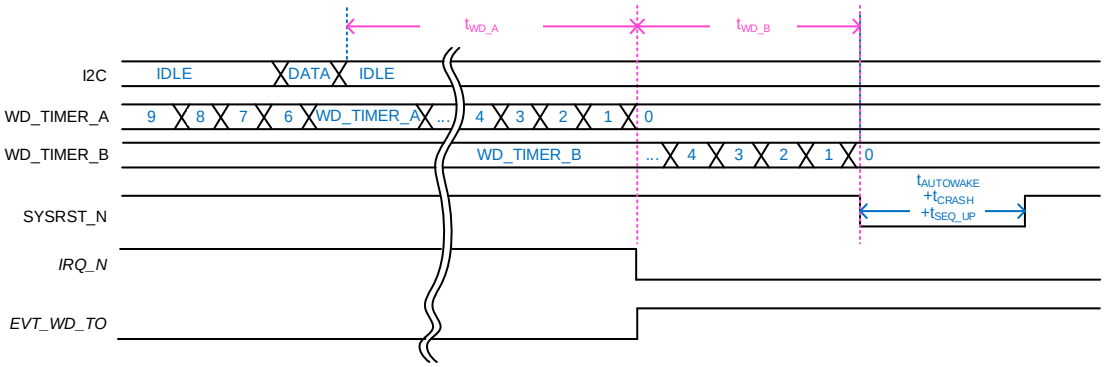


Figure 11. Watchdog reset diagram

5.1.13 IRQ_N Generation

All events in the system (see register map section “Event registers”) can contribute to generate a pull IRQ_N low. Each event can be prevented from generating an IRQ by using the corresponding IRQ mask (register map section “IRQ mask”) by setting the mask bit to “1”.

If one (or more) events fire and the masks for those is “0” the IRQ_N output is pulled low.

5.2 Thermal Protections

5.2.1 Thermal Warning

In ACTIVE state the thermal warning feature monitors the die temperature. If it exceeds a configurable threshold (THERMAL_WARNING_THRESHOLD), an event EVT_TWARN is flagged and an IRQ is generated.

After timer expiration configured by THERMAL_WARNING_TIMER, the device will run through a power cycle.

5.2.2 Thermal Shutdown

The die temperature is additionally checked against a higher temperature threshold, which will lead to a power cycle as well. It is flagged in EVT_TSHDN. This feature is not configurable and cannot be disabled, as it is a device protection mechanism.

If a thermal shutdown event in DEEPSLEEP mode occurs, it will be stored and read by next digital wake-up in EVT_SHIP_TSD.

5.2.3 Thermal Latch-Off

Thermal shutdown can contribute towards a thermal latch-off feature, if THERMAL_LATCHOFF_EN is set to enable it. If the feature is enabled, the number of consecutive thermal shutdowns will be tracked in a counter. If the counter exceeds the setting in THERMAL_LATCHOFF_CYCLES, the device will stay switched off and not power the rails on anymore. Only button reset can re-activate the device. In case a button reset is used to clear the latch-off, the device performs another power cycle.

5.3 Battery Charging

If an adapter has been detected and the CHG_EN_N pin is pulled low (or emulation is used, see section 5.1.8), the device enters CHARGE mode.

Different charging modes are described in Table 22.

Table 22. Charge mode control

VBAT condition	ICHG regulation	VBAT regulation	charge mode	Pre-charge timer	Main timer
< VBAT_PRECHG_THR	IPRE_CHG	-	Pre-charge	Running	Running
> VBAT_PRECHG_THR & < VBATREG	ICHG		CC	Reset	Running
= VBATREG	-	VBATREG	CV	Reset	Running

Pre-charge / fast charge boundary threshold voltage VBAT_PRECHG_THR is programmable by VBPRECHG register.

5.3.1 Pre-Charge and Fast Charge Operation

The device is in charge ready state right after the device enters charge mode. In the beginning of the charge ready state, the device starts charger initialization by waking up analog charger block.

In the charge ready state, the device enters charge in-progress state when all conditions below are met.

- Charge initialization finished
- VCHG_IN_OVP > VCHG_IN > VBAT + VSLP (not in sleep mode) > VCHG_IN_UVLO_THR
- BTS is ready (battery temperature measurement done) and device not in HOT or COLD region

- CH_EN_N input is pulled low

After the device enters charge in-progress state, charging starts. Depending on VBAT and ICHG, the device automatically selects appropriate charge operation as listed below and Table 22.

- Pre-charging (VBAT < VBAT_PRECHG_THR)

During pre-charging mode, charge current is regulated and controlled by IPRECHG register.

Once VBAT becomes higher than VBAT_PRECHG_THR, the device starts CC (constant current) charge operation.

- CC (constant current) charging (VBAT_PRECHG_THR < VBAT < VBATREG)

In CC mode, charge current is regulated and controlled by ICHG register. The max. charge current is limited by the ICHG_MAX register. This register can be written and protected from further changes using the ICHG_MAX_LOCK bit. The lock bit can only be cleared by a special sequence described in 5.9.

When VBAT reaches VBATREG the device ends CC operation and starts CV operation.

- CV (constant voltage) charging (VBAT = VBATREG and ICHG > ITERM)

When VVBAT gets close to VBATREG threshold, the device starts CV charging which is VBAT is regulated at VBATREG.

When the condition ICHG < ITERM is met, the device terminates charging and moves to charge done state.

Termination current is controlled by ITERM register.

5.3.2 Charge Done State and Recharge

When conditions below are met, the device stops charging and enters charge done state.

- ICHG < ITERM (Termination current)
- VBAT = VBATREG (CV operation)

When VBAT falls below VBATREG, the device does not start recharge operation. To prevent unwanted rapid iteration of charging and discharging, the device has voltage threshold at which the device starts recharging. This threshold is configurable in bitfield VRECHG_THR.

After termination, the device starts recharging when the following condition is met.

- VBAT < VBATREG - VRCH

Recharging can be disabled by setting AUTO_RECHG_DIS bit. The EVT_RECHARGE_RDY event is generated if recharging is disabled and recharge condition is met.

5.3.3 Safety Timer

The device has two safety timers, namely pre-charge and main safety timers. The operation of the timers in each charge mode is described in Table 23. The safety timers start counting as soon as the charge cycle begins.

Table 23. Safety timers

Charge mode	Pre-charge timer	Main timer
Pre-charge	Running	Running
CC	Reset	Running
CV	Reset	Running

Depending on charge fault, timer duration may be changed, or timer may be suspended, stopped, or reset as described in Table 24.

Table 24. List of charge faults and timer changes

Fault	Charge control	VSYS source	Safety timer
VDD_PWR OVP	Stop	VBAT	Reset
VDD_PWR UVLO	Stop	VBAT	Reset
VDD_PWR DPM	Continue	VDD_PWR	x2
VDD_PWR ILIM	Continue	VDD_PWR	x2

Fault	Charge control	VSYS source	Safety timer
VBAT UVLO	Pre-charge/Fast-Charge (dep. on BUVLO/VBPRECHG)	VDD_PWR	x1
VBAT DPPM	Continue	VDD_PWR	x2
VBAT Short	Pre-charge	VDD_PWR	x1
Bat. Supply mode	Suspend	VBAT – 50mV	Suspend
TS COLD	Stop	VDD_PWR	Suspend
TS HOT	Stop	VDD_PWR	Suspend
TS COOL	Continue	VDD_PWR	x2
TS WARM	Continue	VDD_PWR	x1
TS_OPEN	Stop	VDD_PWR	Suspend
Over temp.	Stop	Disable	Reset

The duration of pre-charge timer t_{PRECHG} and the duration of main timer t_{MAXCHG} are programmable by the TMR register, but these durations are dependent of each other and are related as follows:

$$t_{PRECHG} = 0.25 \times t_{MAXCHG}$$

Table 25. TMR register settings

TMR	Pre-Charge Timer	Main Timer
0x0	30 min	2 h
0x1	37.5 min	2.5 h
0x2	45 min	3 h
0x3	52.5 min	3.5 h
…	…	…
0xD	127.5 min	8.5 h
0xE	135 min	9 h
0xF	(Disable)	(Disable)

In some situations, the timer duration may be doubled to allow long period to meet the termination condition. This feature can be disabled using TMRX2_EN register.

Table 26. TMRX2_EN register

TMRX2_EN	Description
0x0	Disabled (Duration never doubled.)
0x1	Enabled (Duration doubled when required)

The device generates a safety timer fault when at least one of these timers has expired.

To clear safety timer fault, one of the conditions below must be met.

- Rising edge on CHG_EN_N
- VDD_PWR UVLO (VDD_PWR removal)

5.3.4 Battery Temperature Range Detection

DA9098 has an integrated battery temperature sensing (BTS) mechanism to determine if the battery temperature falls inside five temperature ranges: NORMAL, COOL, WARM, COLD, or HOT.

The sensor monitors the battery's NTC thermistor and adjusts charging settings accordingly.

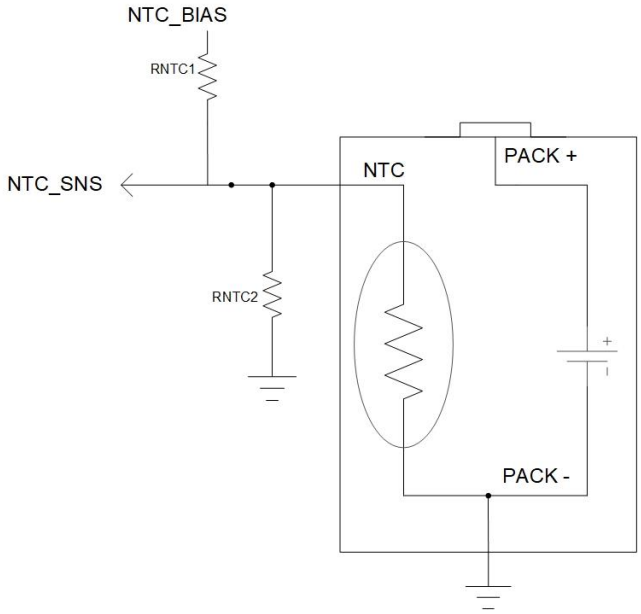


Figure 12. NTC battery temperature sensing with NTC

Setting the Resistor Divider

The resistor divider values (RNTC1and RNTC2) are selected as shown below so that the cold and hot NTC_SNS thresholds are reached at the corresponding NTC values.

Equation 1:

$$R_{(NTC2)} = \frac{R_{(COLD)} \times R_{(HOT)} \times \left(\frac{1}{0.398} - \frac{1}{0.15}\right)}{R_{(HOT)} \times \left(\frac{1}{0.15} - 1\right) - R_{(COLD)} \times \left(\frac{1}{0.398} - 1\right)}$$

Equation 2:

$$R_{(NTC1)} = \frac{\left(\frac{1}{0.398} - 1\right)}{\left(\frac{1}{R_{(NTC2)}} + \frac{1}{R_{(COLD)}}\right)}$$

Where

- R(HOT) = the NTC resistance at the hot temperature
- R(COLD) = the NTC resistance at the cold temperature

The cool and warm thresholds are not independently programmable and are fixed once the cold and hot values are determined. The cool and warm thresholds can be determined by the NTC value at the threshold:

Equation 1:

$$R_{(COOL)} = \frac{R_{(NTC2)} \times R_{(NTC1)} \times 0.35}{R_{(NTC2)} - R_{(NTC2)} \times 0.35 - R_{(NTC1)} \times 0.35}$$

Equation 2:

$$R_{(WARM)} = \frac{R_{(NTC2)} \times R_{(NTC1)} \times 0.205}{R_{(NTC2)} - R_{(NTC2)} \times 0.205 - R_{(NTC1)} \times 0.205}$$

Where

- R(COOL) = the NTC resistance at the cool temperature
- R(WARM) = the NTC resistance at the warm temperature

Normal Hardware based Mode of Operation

If the temperature goes out of the NORMAL range, a different set of ICHG and VBREG settings are used to reduce the charge current/voltage for the WARM and COOL range. The COLD/HOT regions always lead to a suspension of the charging process.

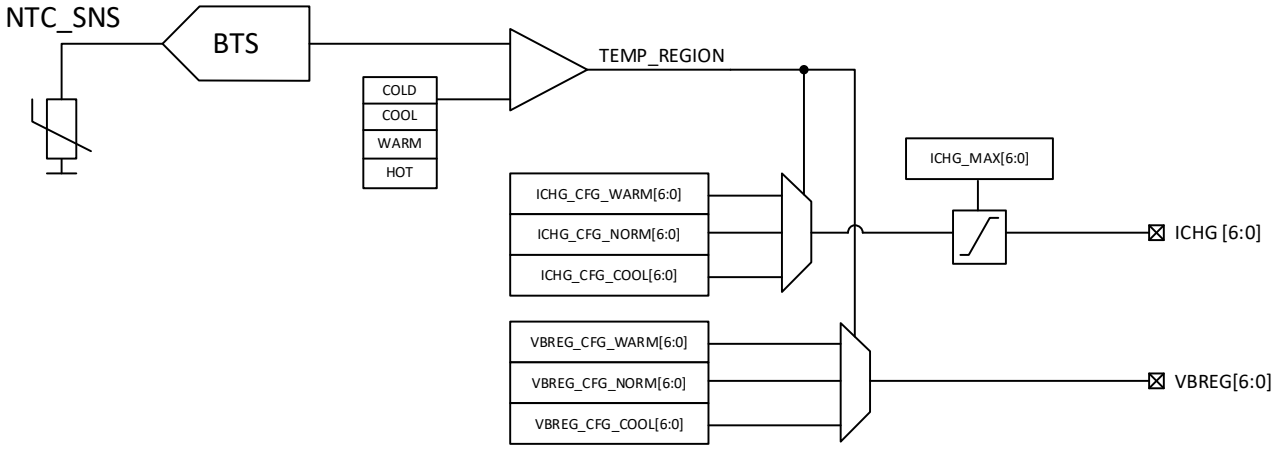


Figure 13. ICHG and VBREG selection depending on NTC_SNS

The used settings can be read back from the device in registers CHG_VBREG_ACTUAL and CHG_ICHG_ACTUAL. The temperature region WARM can be enabled by setting bit TS_WARM_EN in register CHG_BAT_TS_CFG to 1. If the bit is 0 the region will be treated like the normal temperature region (no reductions).

Mixed-mode Operation

Both temperature regions WARM and COOL can be disabled by setting bit TS_SW_EN in register CHG_BAT_TS_CFG to 1. If TS_SW_EN is 1, then regions COOL and WARM will be treated like the normal temperature region.

If TS_SW_EN is set to 1, register bit TS_SUSPEND in register CHG_BAT_TS_CFG can be used to suspend the integrated sensing mechanism. During suspension, the charger will continue to use the latest BTS result before the suspension.

Setting bit TS_SUSPEND will not interrupt an ongoing integrated BTS operation. In such case, the suspension will become effective once the ongoing BTS has finished.

Bit TS_SUSPEND is intended to be used with an external software sensing mechanism that detects the COOL, NORMAL, or WARM regions using the ANA_MON of DA9098 and adapts registers ICHG_CFG_NORMAL and VBREG_CHG_NORMAL accordingly. The integrated BTS needs to be suspended before the external BTS operation is performed. The recommended steps are:

1. Set TS_SW_EN to 1
2. Set TS_SUSPEND to 1
3. Wait 20 ms, to allow an ongoing BTS operation to finish.
4. Configure ANA_MON to measure the battery temperature, perform the SW BTS operation and adapt, if required, ICHG_CFG_NORMAL and VBREG_CFG_NORMAL over I^2C. Then configure ANA_MON to its default settings
5. Set TS_SUSPEND to 0
6. Wait 10 ms

To avoid the application of an outdated result of the integrated BTS, it is the responsibility of the software to suspend the integrated BTS with a timing that allows the integrated BTS to finish between consecutive suspensions.

5.3.5 Dynamic Power Path Management

Dynamic Power Path Management (DPPM) manages the situation in which the total charging and system current exceeds the VSYS current limit. When the input current is clamped, VSYS drops until it reaches VSYS_DPPM_THR (DPPM threshold). In DPPM operation, charging current is reduced as needed to service the

system current at VSYS. DPPM is only active during charging and will send an interrupt over IRQ_N and set event bit EVT_DPPM.

If VSYS drops further due to increasing load, the DA9098 eventually enters battery supplement mode.

5.3.6 Battery Supplement Mode

The DA9098 enters battery supplement mode when VSYS falls below VBAT. Supplement mode occurs when an adapter is attached, regardless of whether the battery is charging or not.

Similarly to DPPM mode, the total current at VSYS exceeds the VCHG_IN current limit, causing VSYS to drop until it reaches the VBAT voltage. In this mode, the battery supplies current to VSYS, thus supplementing the input current to supply the system demands. In battery supplement mode, the discharge current from the battery is limited by the over-discharge protection.

The device exits supplement mode when the system load is reduced and VSYS rises above VBAT.

EVT_BAT_SPPL_MODE will be logged when supplement mode is entered and the battery is being charged.

5.3.7 Adaptive Input Voltage Charging

DA9098 supports active adjustment of the input voltage close to VBAT, in order to minimize power dissipation across the charging path.

A sufficient voltage headroom to VBAT needs to be applied for accurate charging functionality. The voltage headroom depends on the sum of charge current and system load.

The minimum input to be applied at VCHG_IN shall be 3.6 V.

The VINDPM loop shall be disabled.

The power LDO needs to be configured in pass-through mode.

Assuming no VSYS load, V_{BAT} = 3.6 V and typical conditions, the required minimum overhead VCHG_IN to VBAT can be given by below formula:

$$Overhead = 0.598I_{CHG} + 167.1 \quad (1)$$

With Overhead in mV and ICHG in mA.

5.4 Charger Mode Operation and Power Path Management

DA9098 monitors battery voltage and current as well as VCHG_IN input voltage and current during all modes of operation.

At all levels of operation, the appropriate charge current is maintained while protecting the battery, system connections, and the input supply from over-voltage and overcurrent and other potential fault conditions.

The DA9098's power path management features ensure smooth transitions from charging to reduced charging to battery supplementing the load during load peaks.

5.4.1 Input Voltage Dynamic Power Management (VINDPM)

If the charge current and system load exceed the current capability of the VCHG_IN input source, the input voltage will drop.

Dynamic power management (DPM) prevents the input from dropping by scaling down the VCHG_IN current limit (IVCHG_IN_LIM) until it matches current capability of the power source.

This feature becomes active when VCHG_IN falls below VCHG_IN_DPM, which is programmable between 4.2 V and 4.9 V in CHG_VDD_PWR_IDISCHG_CFG register.

The EVT_VINDPM event bit is set to 1, and an interrupt is sent over IRQ_N pin, whenever the DA9098 is in this current-limited mode. In charging mode, termination is ignored to allow the battery to be charged with whatever current is still available.

VINDPM can be disabled with register bitfield PWR_LDO_DPM_EN.

It is required to disable the VINDPM if the input charging voltage is dynamically adjusted to the battery voltage.

5.4.2 VCHG_IN Current Limit (VINILIM)

The VCHG_IN current limit feature protects both the DA9098 and the input supply from excessive current.

The current limit threshold is programmable from 20 mA to 600 mA in 25 mA steps at register CHG_VDD_PWR_CFG_0.

When the input current reaches the set threshold, VCHG_IN current is clamped and an event bit EVT_VINILIM is set.

The DPM function, when enabled, will reduce the current limit threshold if the input voltage starts to drop due to system load.

5.4.3 Under-Voltage Lockout (VCHG_IN_UV)

The UV threshold for VCHG_IN is 3.4 V (typical).

Below this voltage, VCHG_IN will be disconnected from the power path and the DA9098 will be in battery powered operation.

VCHG_IN UV will cause IRQ_N to toggle and will set the EVT_VCHG_IN_UV event bit to 1.

The UVLO threshold has typically 150mV of hysteresis on the rising edge.

When VCHG_IN rises above this threshold, charging is re-enabled.

5.4.4 Sleep Mode (SLP)

Sleep mode behavior is similar to VCHG_IN_UV, but the falling threshold is relative to VBAT. When VCHG_IN falls below VBAT + 65 mV (typical), sleep mode is activated. In sleep mode, VCHG_IN is disconnected from the power path, an interrupt is generated on IRQ_N, and the EVT_SLP event bit is set to 1. When VCHG_IN falls into the range of sleep mode, charger will already be in DPPM mode (VSYS < VBAT_CHG + 0.2 V typical), therefore charge current will already be reduced to zero.

5.4.5 Input Over-Voltage Protection (VCHG_IN_OV)

The DA9098 protects itself (and downstream connections to VSYS) against input over-voltage conditions by disconnecting VCHG_IN from the power path. Over-voltage protection kicks in immediately when VCHG_IN exceeds the VCHG_IN _OVP threshold. Over-voltage events are common at USB plug-ins due to the inductance of the long cable, where the transient overshoot may exceed 10 V depending on cable length, quality, and input capacitance. The VCHG_IN input is capable of withstanding up to 16 V and will remain in VCHG_IN_OV until the voltage returns to nominal levels. During VCHG_IN_OV, VCHG_IN is disconnected from the power path and the DA9098 will be in normal battery powered operation.

When an over-voltage occurs, the event bit is set to 1 and an IRQ is generated.

5.4.6 VSYS Voltage Regulation and Power LDO (LDOPWR)

The DA9098 provides regulated VSYS supply by using a linear voltage regulator. The regulated VSYS voltage can be set from 3.2 V to 4.8 V (VVSYS_RNG) using PWRLDO_PWR_LDO_VSEL_MSB and PWRLDO_PWR_LDO_VSEL_LSB registers.

In order to maintain proper charger operation, the VSYS voltage has to be set above the VBATREG + $V_{VSYS\_DPPM\_THR}$, ideally leaving 250 mV headroom for the battery charger, see also section 5.3.5 (DPPM).

The Power LDO includes a function to provide non-regulated VSYS voltage by passing through the VCHG_IN to VSYS (Pass-Through Mode). This function can be enabled by setting PWR_LDO_EN_PASS_THROUGH bit to "1" (register PWRLDO_PWR_LDO_CONF_A). In the Pass-Through mode the VINDPM and VINILIM functionalities are supported.

5.5 SIMO Buck

DA9098 device offers a high-efficiency single-inductor, 4-outputs SIMO Buck.

The dynamic performance per channel of the SIMO (ripple), depends amongst others on: External passives, SIMO configuration (Output voltage setting, Peak current limit), channel load, total SIMO load.

The SIMO current capability is shared between the channels. The total current capability depends on application as for the dynamic performance.

Each channel can support 100 mA for 400 mA total SIMO load. In case a channel is only lightly loaded, or not used, the other channels can support a higher load.

MFSM_PWRSEQ_CHANNELS_0 register controls the enable of SIMO channels. Depending on application, the four channels can be individually enabled by software and/or OTP.

The regulator operates in single mode PFM/DCM. The SIMO controller is fully asynchronous for maximum efficiency on light load conditions.

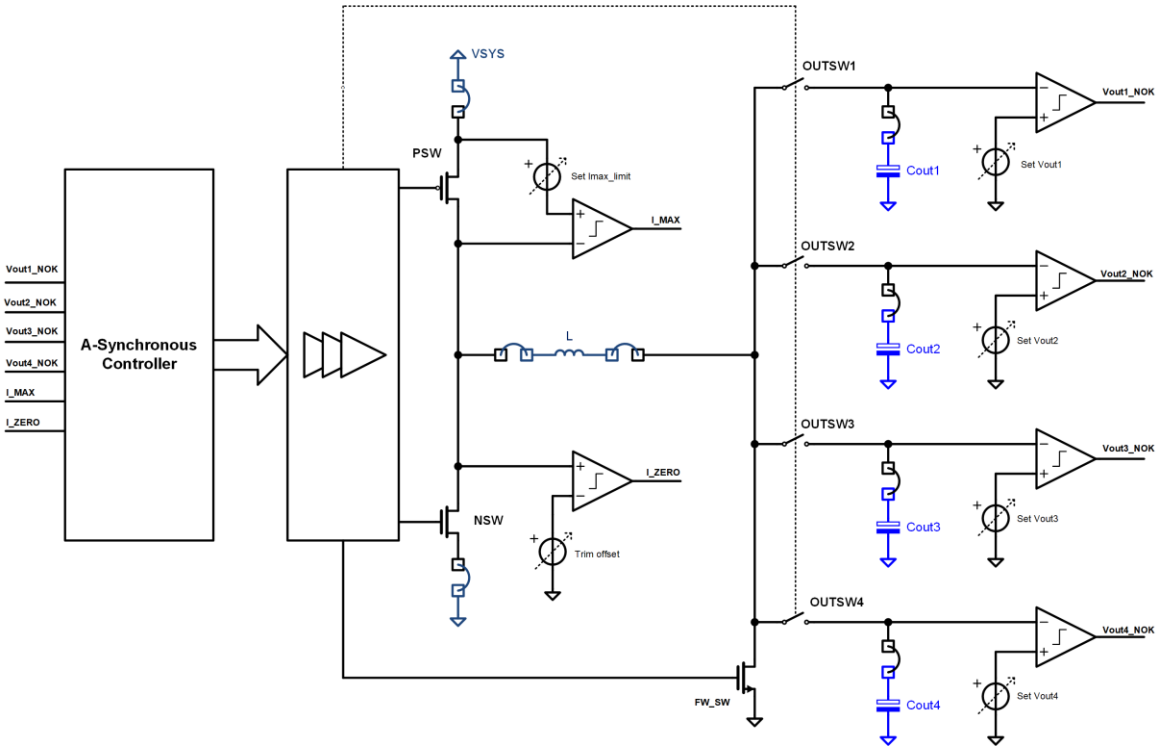


Figure 14. SIMO buck simplified block diagram

The SIMO controller is fully asynchronous for maximum efficiency on light load conditions.

The controller controls the PSW and NSW Buck switches, as well as the Output switches selection.

A freewheel switch may be used to ground the LY pin when the converter is idle for EMI consideration.

If the freewheel mode is enabled, the FW_SW switch is turned on when the control inputs for both the PWS and NSW switches are disabled.

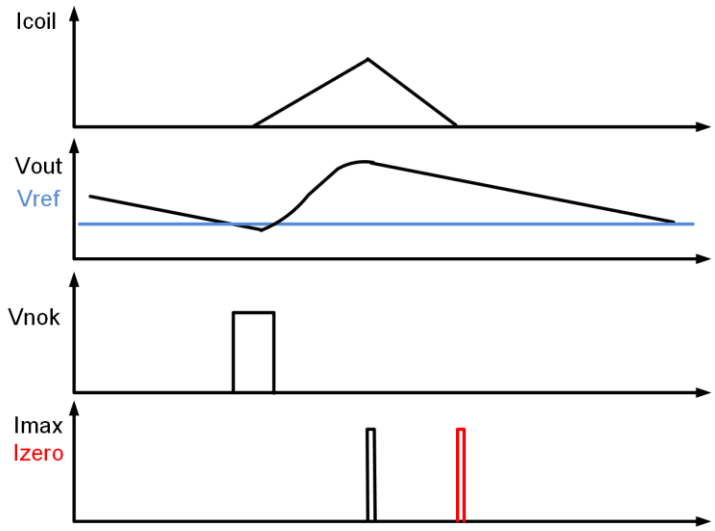


Figure 15. SIMO buck switching cycle

The switching cycle starts when a rail voltage Vout drops below the target voltage. Vnok is flagged to the controller. It contains a FIFO that stores the request from each channel and serves them sequentially.

Power cycle sequence:

1. Vnok is detected
2. Output is placed in FIFO buffer
3. Charge cycle is started, PSW and OUTSW closed
4. Imax is detected / Timeout occurs
5. Charge cycle goes to next state, PSW is opened, NSW is closed.
6. Izero is detected / Timeout occurs
7. Charge cycle finished, NSW and OUTSW opened
8. FIFO buffer is shifted, next output is charged, or system goes into idle mode

5.6 Analog Monitor

Various analog signals of DA9098 can be monitored on ANA_MON output pin during operation.

5.6.1 Channels Selection

Table 27. ANA_MON output signals

Ch	Signal Name	Transfer Characteristics	Description
0	VBAT_SNS	30%, 60% or no scaling of voltage	Battery sense voltage
1	VCHG_IN	30%, 60% or no scaling of voltage	Charger Input voltage
2	VSYS	30%, 60% or no scaling of voltage	Intermediate system voltage
3	NTC_BIAS	30%, 60% or no scaling of voltage	Battery temperature supply voltage
4	NTC_SNS	30%, 60% or no scaling of voltage	Battery temperature sense voltage
5	VCORE	30%, 60% or no scaling of voltage	LDO Core output voltage
6	SIMO1_OUT	30%, 60% or no scaling of voltage	SIMO1 output voltage
7	SIMO2_OUT	30%, 60% or no scaling of voltage	SIMO2 output voltage
8	SIMO3_OUT	30%, 60% or no scaling of voltage	SIMO3 output voltage
9	SIMO4_OUT	30%, 60% or no scaling of voltage	SIMO4 output voltage
10	LDO1	30%, 60% or no scaling of voltage	LDO1 output voltage
11	LDO2	30%, 60% or no scaling of voltage	LDO2 output voltage
12	LDO2	30%, 60% or no scaling of voltage	LDO3 output voltage
13	LDO4	30%, 60% or no scaling of voltage	LDO4 output voltage
14	VSS	30%, 60% or no scaling of voltage	Ground

Ch	Signal Name	Transfer Characteristics	Description
15	RIN_N	30%, 60% or no scaling of voltage	Manual input reset
16	ICHG, IDISCHG, ICHG_IN	$Ichg = 0.43.V_{ANA\_MON}$ $Idischg = 1.37.V_{ANA\_MON}$ $Ichg\_in = 0.43.V_{ANA\_MON}$	Battery charging current Battery discharge current Input VCHG_IN current, voltage converted
17	TDIE	$Tdie = 337 - 244.V_{ANA\_MON}$	Die temperature

For channels 0 to 15, the signals are scalable by 30%, 60% or 100%.

The scaling ratio needs to be configured before the multiplexer is connected outside.

Care must be taken to scale the signal according to the full-scale range of the measurement ADC.

The registers to configure the ANAMON are:

- SYSCTRL_ANA_MON_CTRL0: Specific channel dependent additional configuration
- SYSCTRL_ANA_MON_CTRL1: Channel selection and MUX enable
- SYSCTRL_ANA_MON_CTRL2:
  - ○ Configuration for charger current channels
  - ○ Selection of channel type: direct measurement or with scaling, TDIE, charger current measurement.
- SYSCTRL_ANA_MON_CFG: Scaler configuration

A more detailed description can be found in the register map.

5.6.2 Analog Performances

5.6.2.1 Voltage Scaler

The voltage scaler is intended for signals which can exceed the full-scale range of an external ADC.

When selected, two levels of attenuation can be used: x0.6 and x0.3.

The input voltage range is limited to 1.0 V to V_{DD} (main DA9098 supply) for accurate scaling functionality.

5.6.2.2 Output Impedance

The output impedance seen at ANA_MON is typically in the 3 kΩ to 35 kΩ range and is dominated by the output multiplexer impedance.

The output impedance has a strong dependency to the V_{IN}/V_{DD} ratio and will peak for V_{IN} about one half of the supply.

Under worst-case conditions, the output impedance can reach 249 kΩ at 2.5 V supply, -40 °C, $V_{IN} = V_{DD}/2$ = 1.25 V and slow process corner.

The same corner with 3.0 V supply gives a worst-case output impedance of 140 kΩ.

5.7 LED Driver - Current Sink

DA9098 supports three independent ISINKs with an 8-bit value to control the current from 50 µA to 12.8 mA in steps of 50 µA (ISET_<x> [7:0]).

Under normal operating conditions, each current sink works with a minimum sink voltage of 200 mV. ISINK operation is globally enabled by ISINK_SYS_EN bit. The digital controller of each ISINK<x> can be enabled by ISINK<x>_EN bit to drive ISET_<x>, EN<x> and PWM<x> signals according to the selected operating mode and control source.

5.7.1 Constant Mode

In this mode, the first trigger over I^2C (writing 1 to register bit ISINKx_SW_TRIG) will turn on signal PWM<x>. The second trigger over I^2C will turn off PWM<x> (and so on).

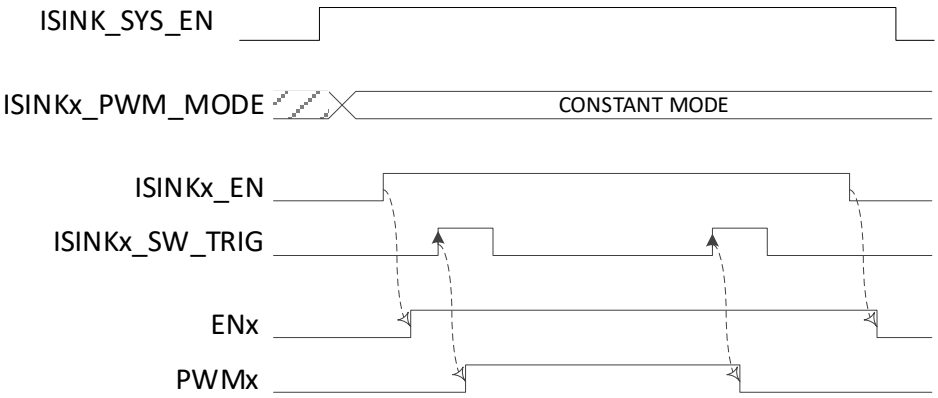


Figure 16. ISINK constant mode

5.7.2 PWM Mode

In this mode, when the first trigger over I²C is detected, the controller starts the generation of a continuous PWM<x> signal. When the second trigger over I²C is detected, the controller completes the current PWM cycle and stops.

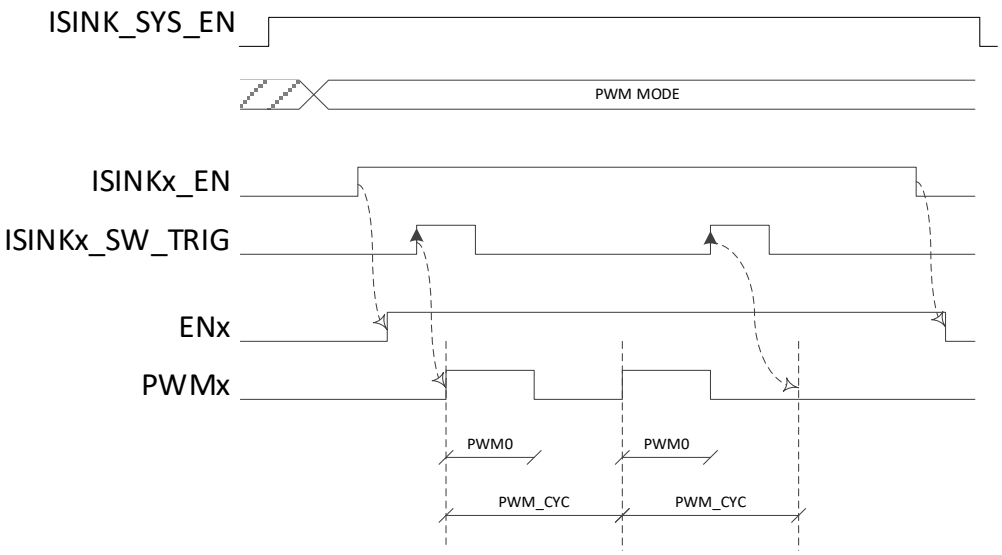


Figure 17. ISINK PWM mode

5.7.3 LED Driver Register Configuration

ISINK core logic runs on the internal 2KHz low power clock domain. Whenever ISINK<x>_CONTROL, ISINK<x>_PWM_CYC, ISINK<x>_PWM0 configuration registers are updated, a synchronization process from internal clock domain to the 2 kHz clock domain is triggered and lasts for three 2 kHz clock cycles (about 1.5 ms).

If any configuration register is written via I²C while synchronization is ongoing, the write operation has no effect and EVT_ISINK<x>_UPDATE_LOST is generated. Host can check if a synchronization is ongoing by reading STA_ISINK<x>_UPDATE.

Each ISINK core handles the synchronization process independently. Software can write to a single configuration register in ISINK1, ISINK2 and ISINK3 in sequence, without any delay between writes. The software must wait for the synchronization process to finish before writing another configuration register in ISINK1, ISINK2 and ISINK3.

5.8 Communication Interface I²C

The DA9098 includes an I²C-compatible 2-wire serial interface to access the internal registers and send commands. Using the I²C interface, the host processor can control each rail and read back the system status.

The I²C supports the following features:

- Operation mode: slave only
- No clock stretching
- Speed modes:
  - Standard mode (Sm), with a bit rate up to 100 kbit/s
  - Fast mode (Fm), with a bit rate up to 400 kbit/s
- 7-bit slave addressing mode
- Slave address is selectable by OTP bit: 0x6B (default setting)
- SDA, SCL deglitch filters
- SDA, SCL slew rate control

The I²C slave address is selected from the OTP during start-up.

The host processor can read and write internal registers through I²C. Also, it can send commands to the system.

The I²C interface is available when MFSM is in ACTIVE states (ACTIVE_ADPT, ACTIVE_BAT, CHARGE).

The slave address is stored in the OTP and available after OTPREAD state.

SDA and SCL pads have analog deglitch filters.

SDA and SCL pads have slew rate control.

5.8.1 Frame Format

The I²C frame consists of the 7-bit slave address, followed by two bytes of register address (totally 16-bit) and one or several 8-bit data.

The data and address are transferred with MSB transmitted first for both read and write operations.

All transmissions begin with a START (S) condition issued from the master while the bus is in an IDLE state (that is, the bus is free). The START condition is initiated by a high to low transition on the SDA line while the SCL is in the high state. A STOP (P) condition is indicated by a low to high transition on the SDA line while the SCL line is in the high state.

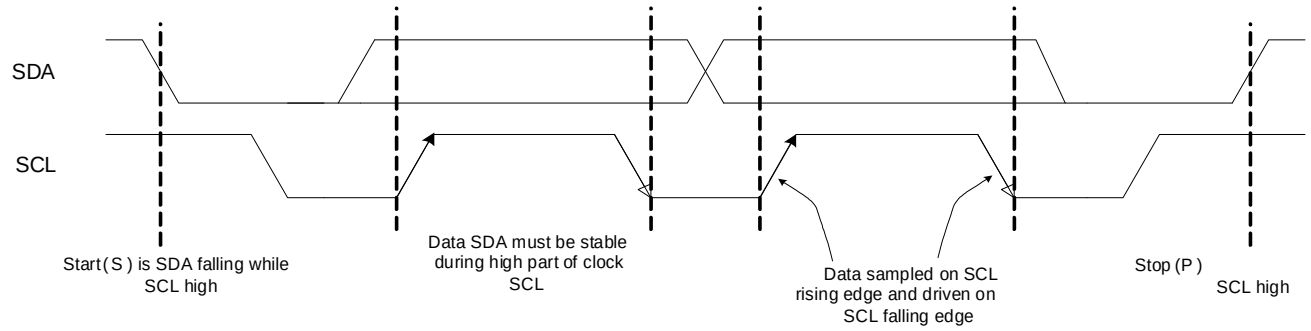


Figure 18. I²C start (S) and stop (P)

The I²C monitors the serial bus for a valid slave address whenever the interface is enabled. When it receives its own slave address, it immediately gives an Acknowledge (A) signal to the host by pulling the SDA line low during the following clock cycle.

A Not Acknowledge (NA) signal is given by the logic 1, not pulling down the SDA line.

5.8.2 Single-Byte Write

A single-byte write is shown in Figure 19. The slave address is followed by a WRITE bit (W = low), the register address, and the data. The transaction is terminated with a STOP.

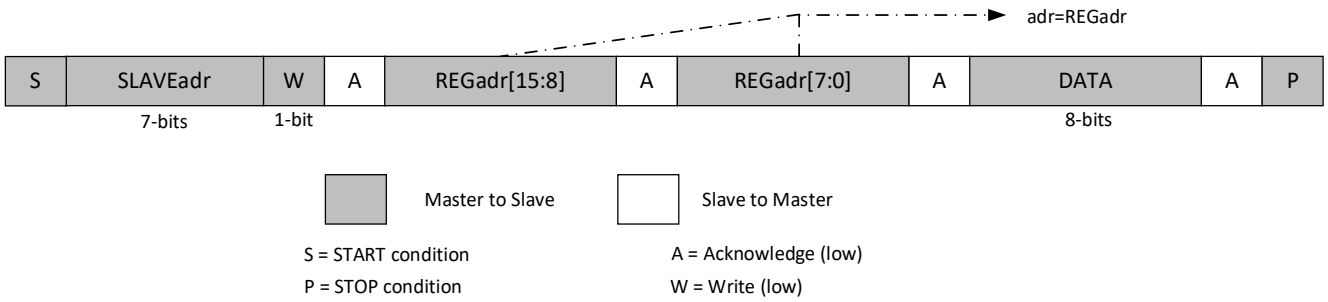


Figure 19. Single write

5.8.3 Multiple-Byte Write

The I²C also supports multiple-byte writes, see Figure 20. By not sending the STOP command, data is written to consecutive addresses.

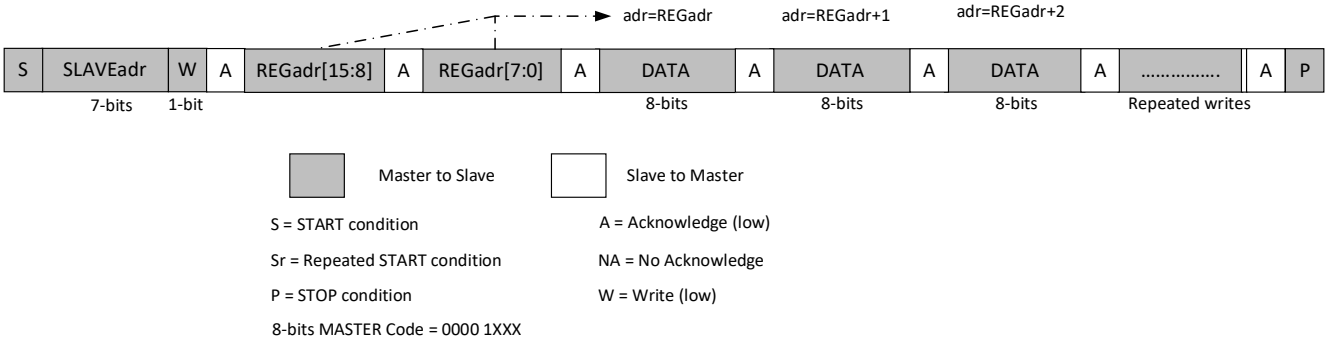


Figure 20. Consecutive write

5.8.4 Single-Byte Read

The data READ protocol does not have a register address immediately preceding it. To read from a specific address, the register address is given by using a write command followed by a Repeated START. A single-byte read is shown in Figure 21. A repeated START (Sr) is followed by the slave address and a READ bit. After the READ data is returned to the host, the host responds with a Not Acknowledge and a STOP.

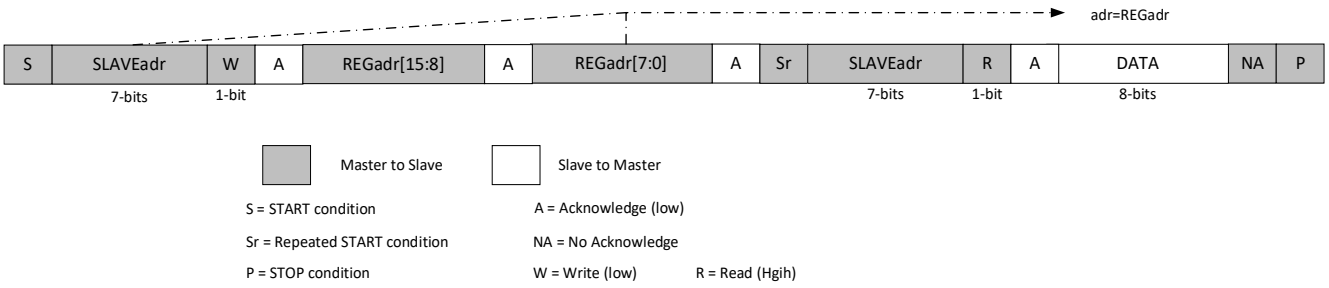


Figure 21. Single read

5.8.5 Multiple-Bytes Read

The I²C also supports a multiple-byte reads. If the host responds to the returned data with an Acknowledge rather than a Not Acknowledge and a STOP, then data will be read from sequential addresses until a Not Acknowledge and a STOP command are given, as shown in Figure 22. If a READ address is given with a WRITE and Repeated START, consecutive addresses are read from the WRITE address.

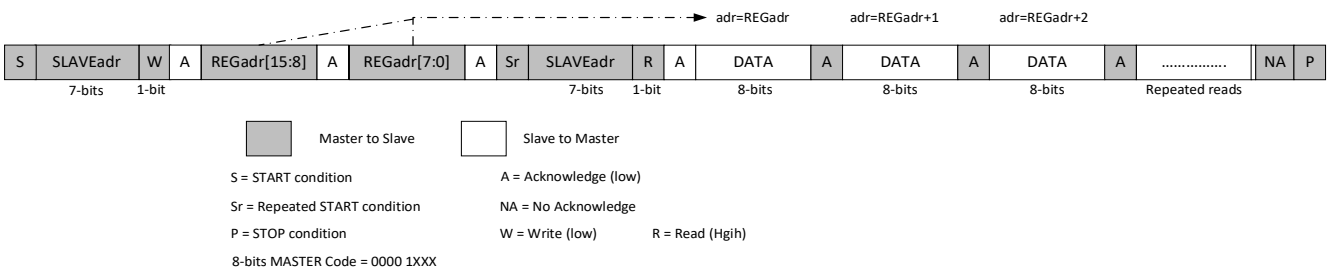


Figure 22. Consecutive read

5.9 Lock Register Handling

If a register is lockable a lock bit is provided to block write access to the register. Only ICHG_MAX is lockable in the DA9098. For this bit the lock bit is ICHG_MAX_LOCK. The behavior is described below:

1. Write to ICHG_MAX.
2. ICHG_MAX can still be changed.
3. Set ICHG_MAX_LOCK to 1.
4. ICHG_MAX cannot be changed anymore.
5. ICHG_MAX_LOCK cannot be set to 0 by writing a 0 to it (lock bit is self-holding).
6. To allow changing ICHG_MAX the lock bit must be cleared by writing a specific 2-byte sequence to SYSCTRL_LOCKCTL_KEY1 and SYSCTRL_LOCKCTL_KEY2.
7. The two bytes need to be the correct values, written in the correct order (SYSCTRL_LOCKCTL_KEY1 before SYSCTRL_LOCKCTL_KEY2) and no other I^2C command may be sent between these two.
8. After clearing the lock by the sequence above the ICHG_MAX can be changed
9. The ICHG_MAX can be write-locked again by setting ICHG_MAX_LOCK to 1

Note that both locks and locked registers are cleared when entering SHIP mode, as the digital core is not powered in this condition.

5.10 Fault and Event Table

Table 28 describes the faults and other events in the device. Events can, as mentioned in section 6.1.13, lead to an IRQ, unless masked by setting the related IRQ_MASK bit of the event (IRQ_*) to 1. Once an event is set it is sticky. To clear it a "1" needs to be written onto the event bit position using I^2C. Each event also has a related status (STA_*) to read the current status of the flag. The column "Interrupt Trigger based on Status Bit Change" in the table defines when the event is generated. If it is rising edge it will only be generated when the condition becomes active. If the event is cleared while the condition persists it will not be set again (but the current status can always be read back through the STA_*). If it is level, then an active level of the defined polarity will lead to re-triggering the event after clearing it, if the condition persists. If the event is on both edges, then both the assertion and the de-assertion of the condition will lead to an event trigger.

Table 28. Fault and event table

Register (Block)	Fault / Flag	Description	Interrupt Trigger based on Status Bit Change
SIMO_EVENT	EVT_SIMO_UV	SIMO UV event. Indicates under voltage threshold has been breached.	Level HIGH
CHG_EVENT_1	EVT_CV_STAT	Constant Voltage charging	Rising edge
CHG_EVENT_1	EVT_CHARGE_DONE	Charge Done status	Rising edge
CHG_EVENT_1	EVT_THERMREG_ACTIVE	Thermal regulation is active (TDIE based current reduction)	Rising edge

Register (Block)	Fault / Flag	Description	Interrupt Trigger based on Status Bit Change
CHG_EVENT_1	EVT_SAFETY_TMR_FAULT	Safety Timer Fault	Rising edge
CHG_EVENT_1	EVT_RECHARGE_RDY	VBAT crossed VBATREG - VRCH threshold. RECHARGE could start manually.	Rising edge
CHG_EVENT_1	EVT_RECHARGE	Re-charge started	Rising edge
CHG_EVENT_1	EVT_CC_STAT	Constant Current charging	Rising edge
CHG_EVENT_1	EVT_PRECHARGE	Pre-charge status	Rising edge
CHG_EVENT_2	EVT_VINILIM	VIN current limit event	Rising edge
CHG_EVENT_2	EVT_DPPM	DPPM event	Rising edge
CHG_EVENT_2	EVT_VINDPM	VIN DPM event	Rising edge
CHG_EVENT_2	EVT_IDISCHG_OCP	Discharge overcurrent protection event	Rising edge
CHG_EVENT_2	EVT_BAT_SPPL_MODE	Battery supplementary mode event occurred while Charging	Rising edge
CHG_EVENT_2	EVT_VBAT_SHORT	Battery short event	Rising edge
CHG_EVENT_3	EVT_TS_COLD	COLD temperature region	Rising edge
CHG_EVENT_3	EVT_TS_COOL	COOL temperature region	Rising edge
CHG_EVENT_3	EVT_TS_WARM	WARM temperature region	Rising edge
CHG_EVENT_3	EVT_TS_HOT	HOT temperature region	Rising edge
CHG_EVENT_3	EVT_TS_OPEN	temperature sense open	Rising edge
IO_EVENT_A	EVT_RIN_N_WAKE1_TIMEOUT	RIN_N active for longer than t_WAKE1	Rising edge
IO_EVENT_A	EVT_RIN_N_WAKE2_TIMEOUT	RIN_N active for longer than t_WAKE2	Rising edge
IO_EVENT_A	EVT_RESET_WARN	Reset warning for reset by RIN_N	Rising edge
IO_EVENT_A	EVT_MANUAL_RESET	Manual reset event on RIN_N. (Not propagated to IRQ_N pin)	Rising edge
IO_EVENT_A	EVT_GPIO1	GPIO event according to the sensitivity selection in the GPIO regs.	Configurable
IO_EVENT_A	EVT_GPIO2	GPIO event according to the sensitivity selection in the GPIO regs.	Configurable
IO_EVENT_A	EVT_GPIO3	GPIO event according to the sensitivity selection in the GPIO regs.	Configurable
IO_EVENT_A	EVT_GPIO4	GPIO event according to the sensitivity selection in the GPIO regs.	Configurable
IO_EVENT_B	EVT_WUP2_RISE	Rising edge of WUP2	Rising Edge
IO_EVENT_B	EVT_WUP2_FALL	Falling edge of WUP2	Rising Edge
IO_EVENT_B	EVT_WUP	Rising Edge of WUP	Rising Edge

Register (Block)	Fault / Flag	Description	Interrupt Trigger based on Status Bit Change
SYSCTRL_EVENT_A	EVT_VCHG_IN_OV	VCHG_IN overvoltage event	Both edges
SYSCTRL_EVENT_A	EVT_UVLO_BAT	UVLO on battery event	Both edges
SYSCTRL_EVENT_A	EVT_WD_TO	Watchdog Timeout event	Rising edge
SYSCTRL_EVENT_A	EVT_TSHDN	Temperature shutdown (device protection) event	Rising edge
SYSCTRL_EVENT_A	EVT_ VCHG_IN_UV	VCHG_IN undervoltage event	Both edges
SYSCTRL_EVENT_A	EVT_UVLO_SYS	UVLO on VSYS event	Both edges
SYSCTRL_EVENT_A	EVT_TWARN	Temperature warning event	Rising edge
SYSCTRL_EVENT_B	EVT_ADAPTER	Adapter attach/removal event	Both edges
SYSCTRL_EVENT_B	EVT_SHIP_TSD	TSD in SHIP mode event	Rising edge
SYSCTRL_EVENT_C	EVT_DSM_LDO3_UV	LDO3 UV in DEEPSLEEP mode event	Rising edge
SYSCTRL_EVENT_C	EVT_LDO3_UV	LDO3 UV event	Rising edge
SYSCTRL_EVENT_B	EVT_SLP	Sleep mode event	Both edges
SYSCTRL_EVENT_B	EVT_PWRSEQ_TO	Power Sequencer Timeout event	Rising edge
SYSCTRL_EVENT_B	EVT_THERMAL_LATCHOFF	Thermal latch-off happened	Rising edge

6. Typical Performance Graphs

6.1 SIMO Efficiency

Setup and measurement conditions:

- Typical supply and temperature conditions (VBAT=VSYS=VIN_SIMO=3.6 V)
- SIMO1 = 0.95 V, 10 µF
- SIMO2 = 0.65 V, 10 µF
- SIMO3 = 1.8 V, 22 µF
- SIMO4 = 1.2 V,10 µF
- 600 mA peak coil current limit setting

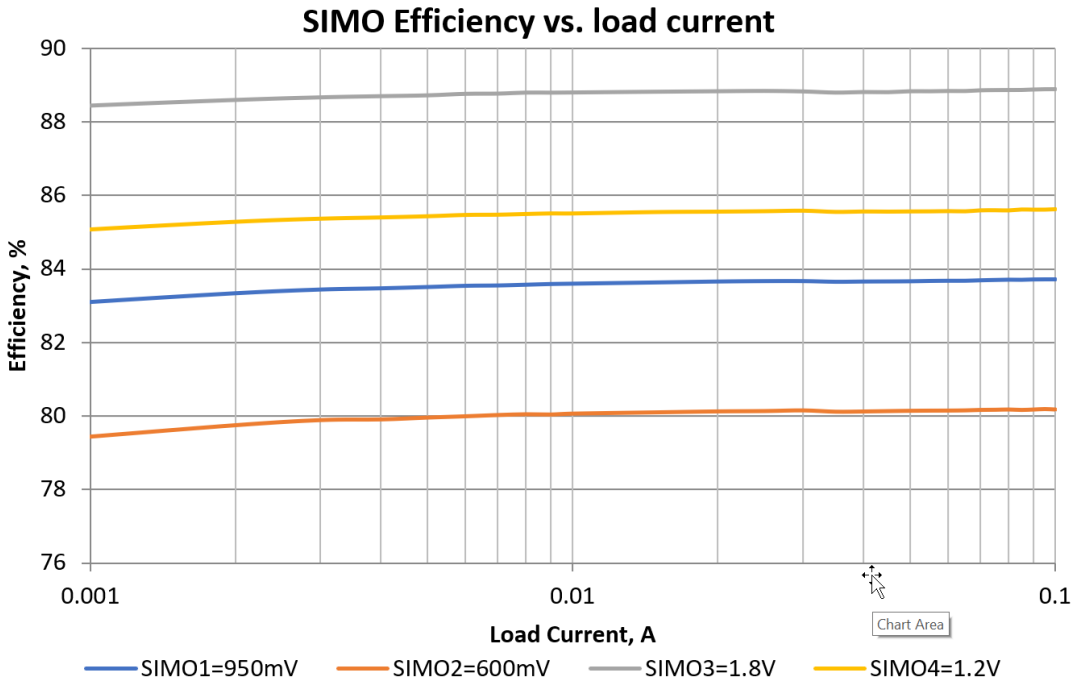


Figure 23. DA9098 typical SIMO efficiency for 4 different voltages

6.2 SIMO Dynamic Performances

6.2.1 Load Transient

6.2.1.1 Light Load

Setup and measurement conditions:

- Typical supply and temperature conditions (VBAT=VSYS=VIN_SIMO=3.6 V)
- SIMO1 = 0.95 V, 10 µF, 1 mA→100 mA→1 mA
- 1 µs ramp-up/dn
- SIMO2 = 0.65 V, 10 µF, ON - NO load
- SIMO3 = 1.8 V, 22 µF, ON - NO load
- SIMO4 = 1.2 V,10 µF, ON - NO load

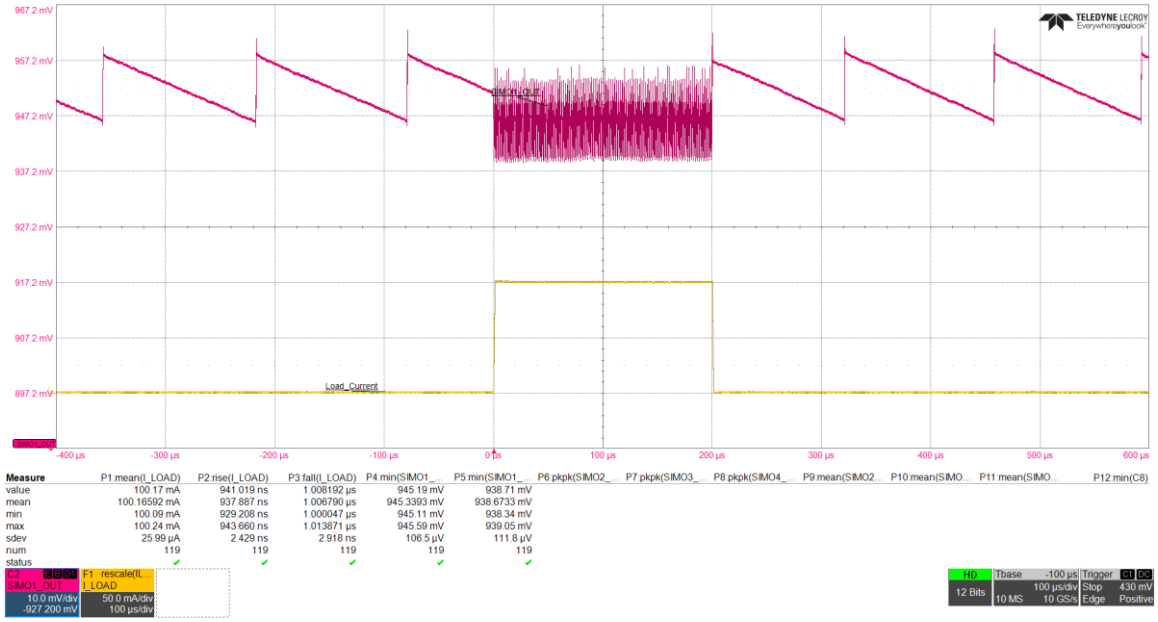


Figure 24. DA9098 SIMO1 load transient response - other rails not loaded

The load transient can hardly be measured and differentiated from the static response and the dynamic behavior.

6.2.1.2 Large Load

Setup and measurement conditions:

- Typical supply and temperature conditions (VBAT=VSYS=VIN_SIMO=3.6 V)
- SIMO1 = 0.95 V, 10 µF, 1 mA→100 mA→1 mA
- SIMO2 = 0.65 V, 10 µF, ON - 20 mA
- SIMO3 = 1.8 V, 22 µF, ON - 100 mA
- SIMO4 = 1.2 V,10 µF, ON - 20 mA

During the load step, the total system load is 240 mA.

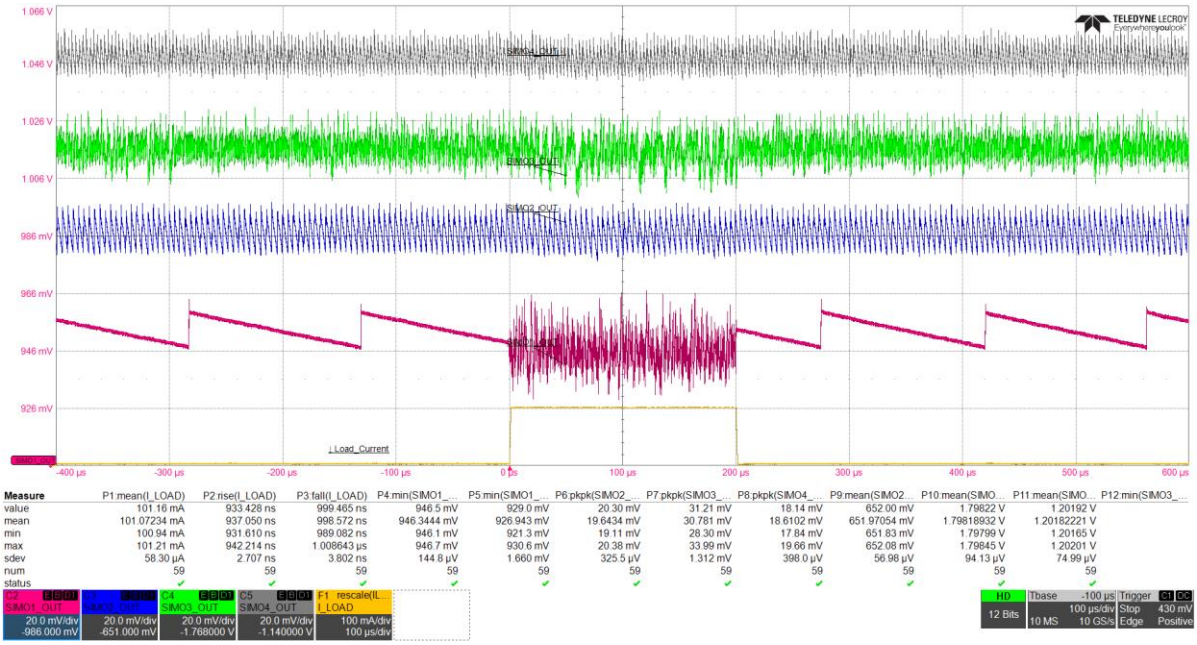


Figure 25. DA9098 SIMO1 load transient response with large total load

The load step response cannot really be differentiated from dynamic transient caused by the total 240 mA system load.

6.2.2 Line Transient

Setup and measurement conditions:

- VBAT = VSYS = VIN_SIMO = 3.1 V→3.6 V→3.1 V
- 500 mV/µs slope
- SIMO1 = 0.95 V, 10 µF, 100 mA
- SIMO2 = 0.65 V, 10 µF, 20 mA
- SIMO3 = 1.8 V, 22 µF, 100 mA
- SIMO4 = 1.2 V,10 µF, 20 mA

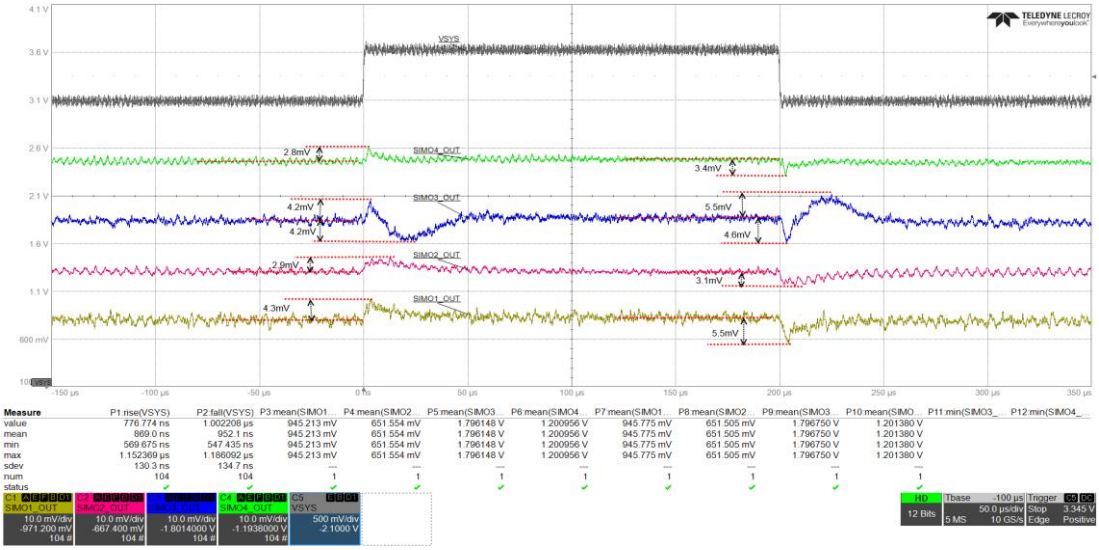


Figure 26. DA9098 SIMO buck line transient response

6.3 LDO PSRR

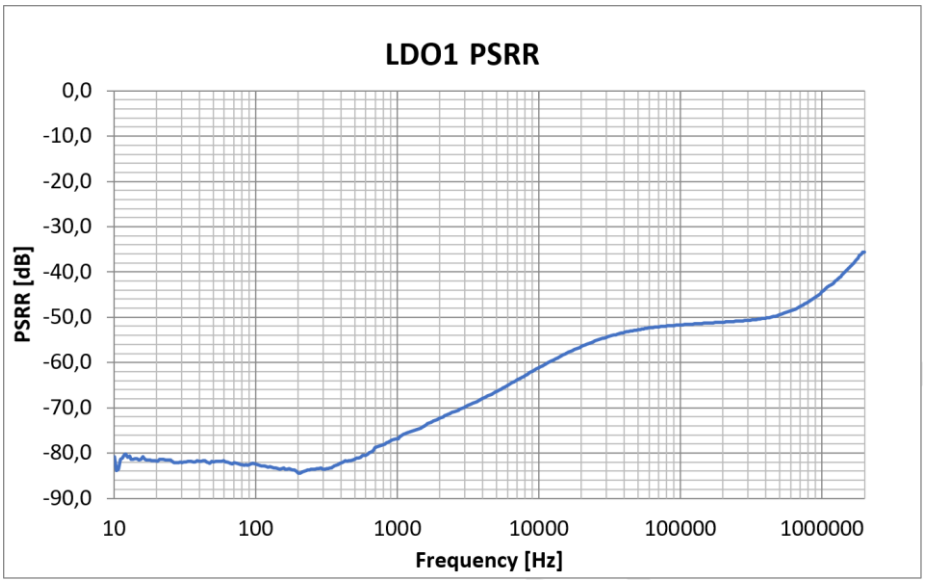


Figure 27. DA9098 LDO1/2 PSRR

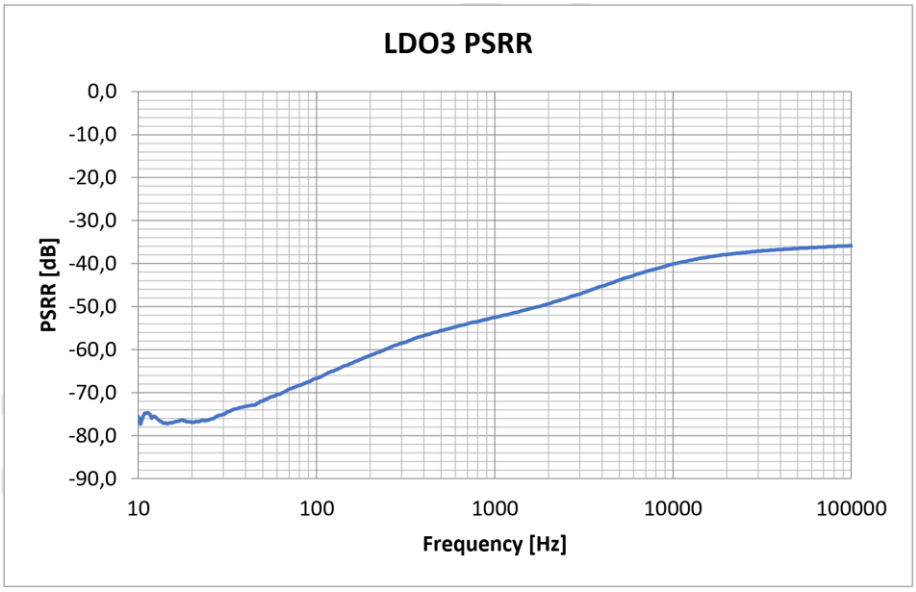


Figure 28. DA9098 LDO3 PSRR

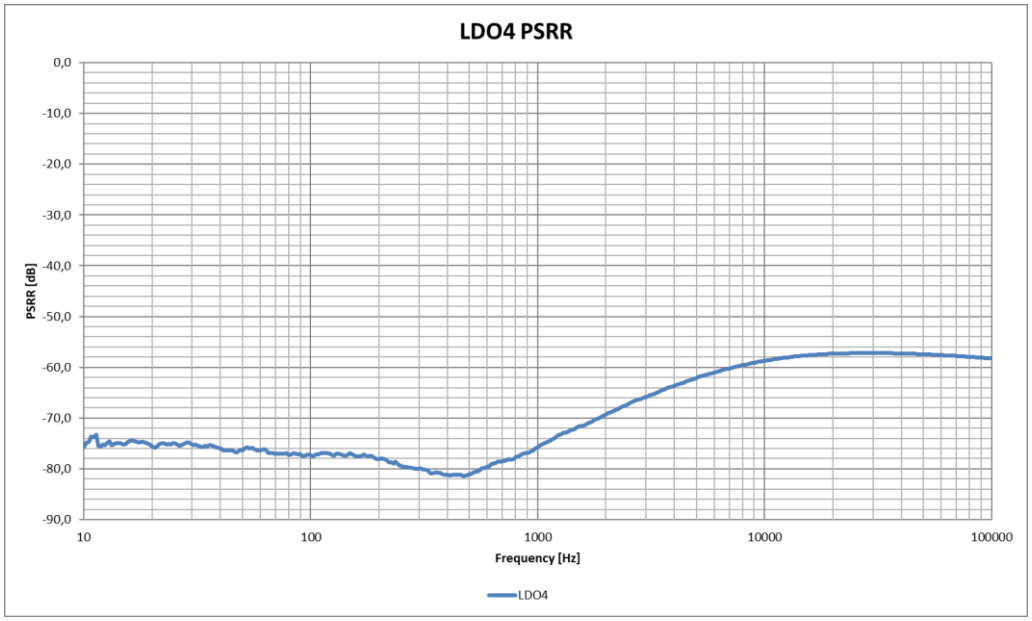


Figure 29. DA9098 LDO4 PSRR

7. Register Definitions

7.1 Snapshot Mechanism

A multi-byte register can be read in a consistent way by using snapshot read-out. When a register is being read-out it can trigger specified register(s) to be saved in a snapshot. When these specified registers are being read, the snapshot data is provided instead of the actual value. The snapshot value is kept until the next snapshot trigger.

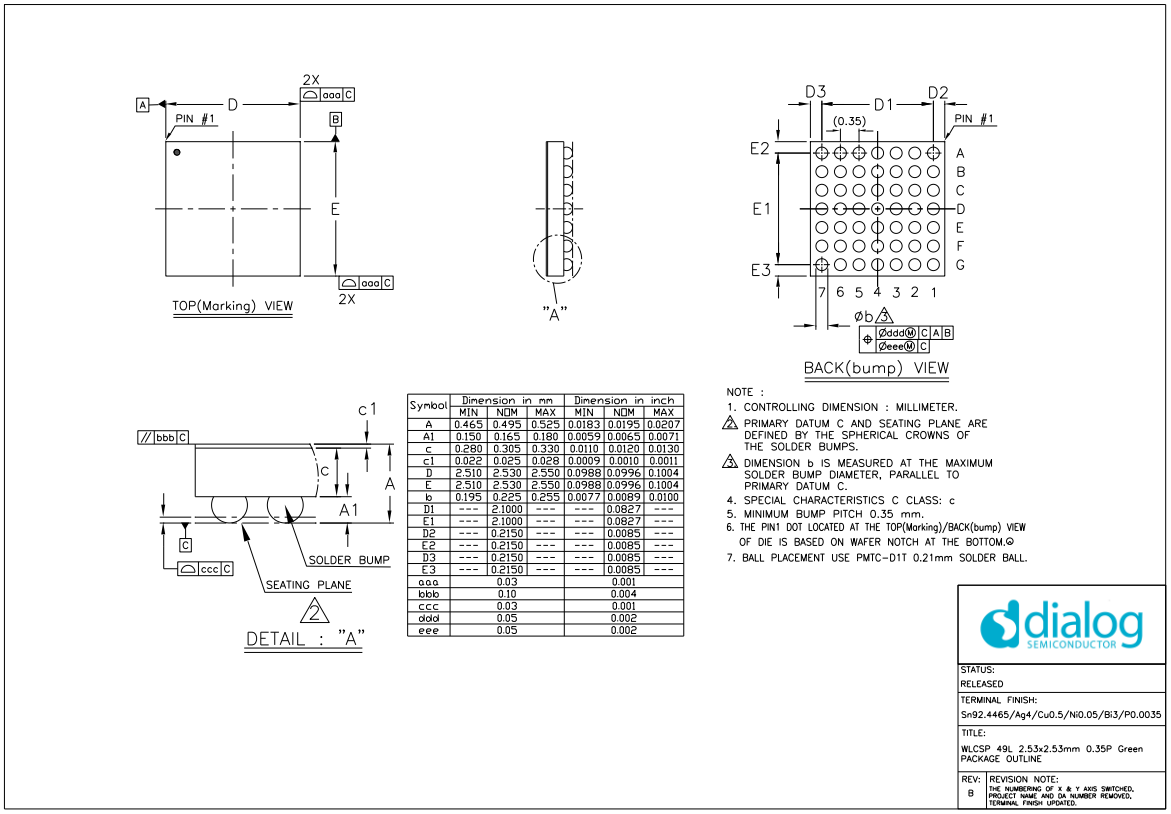
In practice: when the LSB byte is read the MSB byte is saved in a snapshot at the same time. When reading the MSB byte it will be consistent with the already read LSB byte.

7.2 Register Map

The register map is provided as an external HTML document.

8. Package Information

8.1 Package Outlines



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.465	0.495	0.525	0.0183	0.0195	0.0207
A1	0.150	0.165	0.180	0.0059	0.0065	0.0071
c	0.280	0.305	0.330	0.0110	0.0120	0.0130
c1	0.022	0.025	0.028	0.0009	0.0010	0.0011
D	2.510	2.530	2.550	0.0988	0.0996	0.1004
E	2.510	2.530	2.550	0.0988	0.0996	0.1004
b	0.195	0.225	0.255	0.0077	0.0089	0.0100
D1	---	2.1000	---	---	0.0827	---
E1	---	2.1000	---	---	0.0827	---
D2	---	0.2150	---	---	0.0085	---
E2	---	0.2150	---	---	0.0085	---
D3	---	0.2150	---	---	0.0085	---
E3	---	0.2150	---	---	0.0085	---
aaa	0.03			0.001		
bbb	0.10			0.004		
ccc	0.03			0.001		
ddd	0.05			0.002		
eee	0.05			0.002		

Figure 30. WLCSP-49 package outline drawing

8.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 29.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The device package is qualified for MSL 1.

Table 29. MSL classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

8.3 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLCSP package will cause damage to the solder balls. Therefore, a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

8.4 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

9. Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas Electronics local sales representative.

Table 30. Ordering information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9098-AJGT2	WLCSP	2.490 mm x 2.490 mm x 0.52 mm 0.35 mm pitch	Reel	10000

DA9098-XXGT2

XX OTP

10. Layout Guidelines

In order to achieve optimum efficiency, dynamic performance, and guarantee the correct operation of the device, the following points should be considered in the PCB layout:

- VIN_SIMO should be connected through a low impedance path to the VSYS output. Use a wide and short trace to provide a low impedance connection.
- Output capacitors of VSIMO should be placed as close as possible to IC's output and PGND pins.
- Place multiple vias where needed (for example to connect input and output signals through different layers) to reduce the impedance.
- PGND and VSS should be tapped directly from a solid ground plane with minimum impedance to the output capacitors.
- To reduce any influence from an excessively long via stack, it is beneficial to have the ground plane on a layer close to the components layer.

Avoid unshielded crossing of sensitive signal traces with the LX node.

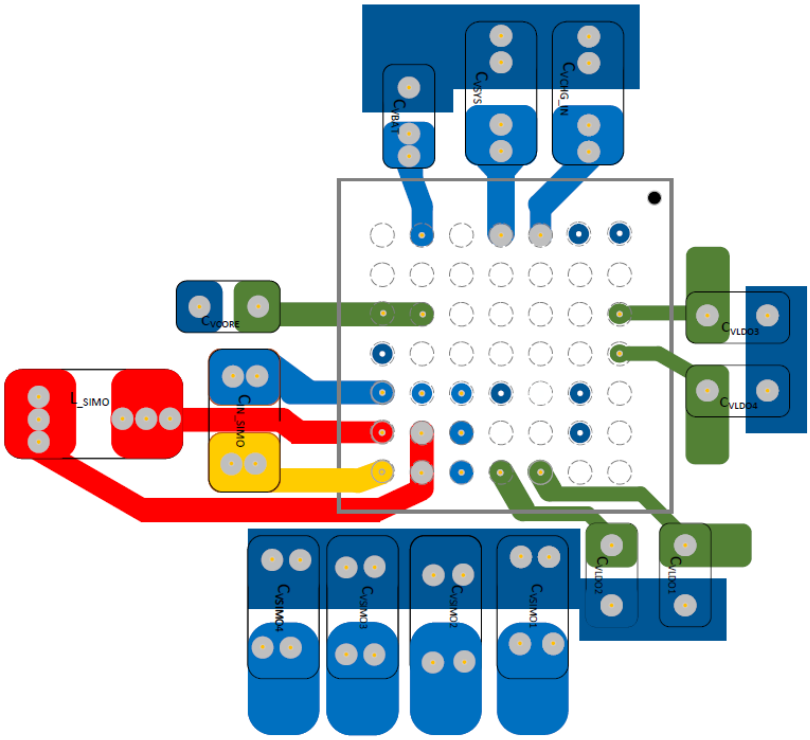


Figure 31. DA9098 layout example

Figure 31 shows an example of the DA9098 layout.

The component sizes are 01005 (LDO CORE), 0201 (LDO1-2-3-4), 0402 (VCHG_IN, VBAT, VSYS, VSIMO1-2-3-4, NTC) and 0603 for the SIMO Buck inductor.

the PGND (yellow) is connected to VSS (dark blue) through multiple vias in the second layer.

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