DA9141

High-Performance, 25 A/40 A Peak, DC-DC Converter

The DA9141 is a high efficiency, 25 A continuous and 40 A peak, four-phase, DC-DC stepdown converter (buck). It is also available as fully AEC-Q100 qualified.

With remote sensing, the DA9141 improves output voltage regulation at the point of load.

Fully integrated switching FETs means no external FETs or Schottky diodes are needed.

A programmable soft startup can be enabled, which limits the inrush current from the input node and secures a slope-controlled rail activation.

The dynamic voltage control (DVC) supports adaptive adjustment of the supply voltage dependent on the processor load, via either a direct register write using the communication interface (I^2C compatible) or with a programmable input pin.

A configurable GPI allows multiple I^2C address selection for multiple instances of DA9141 in the same application.

DA9141 has integrated over-temperature and over-current protection for increased system reliability, without the need for external sensing components.

Key Features

- 2.8 V to 5.5 V input voltage
- 0.5 V to 1.3 V output voltage
- Up to 40 A peak output current, 25 A continuous output current
- 4 MHz nominal switching frequency
- Quad-phase operation
- 110 nH inductor per phase
- 220 µF output capacitor
- ±1% output voltage accuracy (static)
- ±5% load transient
- I^2C-compatible interface (FM+)
- Programmable GPIOs
- Programmable soft startup
- Voltage, current, and temperature supervision
- 60 FC-BGA 4.5 mm x 7 mm (0.65 mm pitch)
- 180 mm^2 total solution area
- Automotive AEC-Q100 qualified also available

Applications

- Navigation systems
- Telematics
- AI engines
- Automotive infotainment
- Advanced driver assistance systems (ADAS)
- SiPP modules

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1. Terms and Definitions

CPU	Central processing unit
DDR	Dual data rate
DVC	Dynamic voltage control
FET	Field effect transistor
FM+	Fast mode plus
GPI	General purpose input
GPIO	General purpose input/output
GPU	Graphics processing unit
IC	Integrated circuit
OTP	One time programmable
PCB	Printed circuit board
SCL	Serial clock
SDA	Serial data
SIPP	Single in-line pin package

2. Overview

2.1 Block Diagram

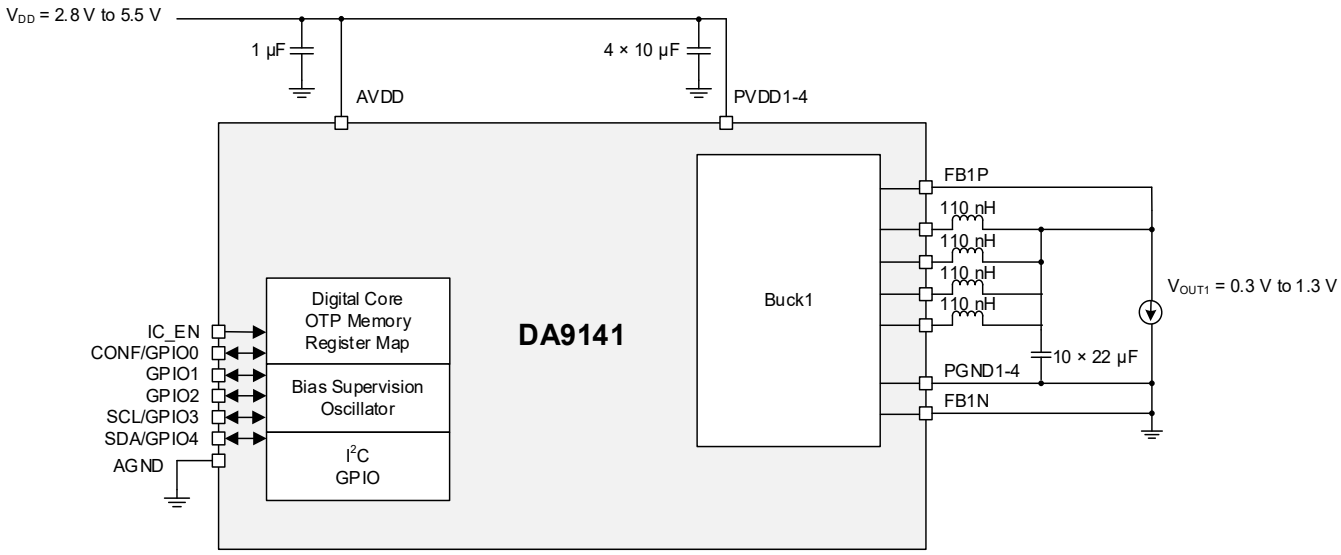


Figure 1. Block Diagram

3. Pin Information

3.1 Pin Assignments

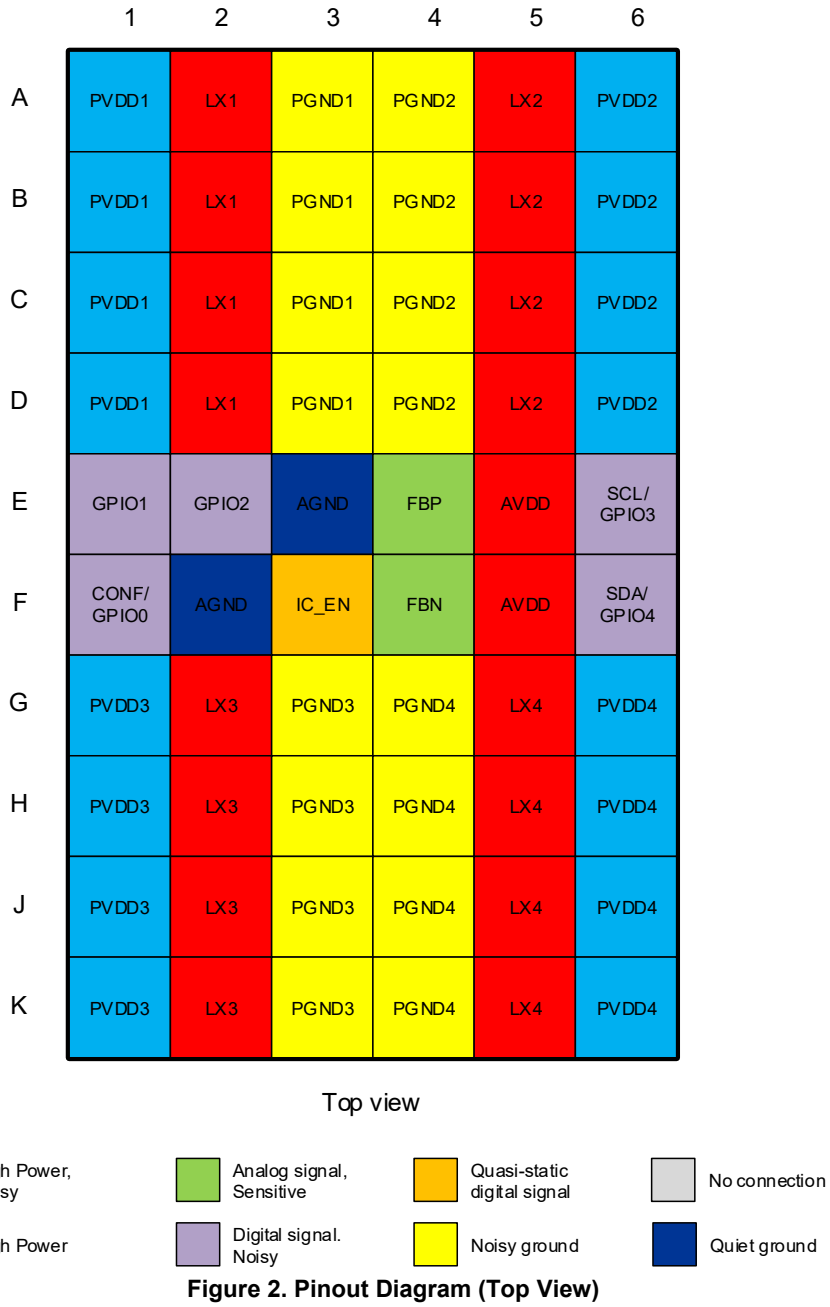


Figure 2. Pinout Diagram (Top View)

3.2 Pin Descriptions

Table 1. Pin Description

Pin Number	Pin Name	Type (Table 2)	Drive (mA)	Description
A1, B1, C1, D1	PVDD1	PWR	10000	Supply voltage for buck power stage, decouple with 10 µF and connect to same source as AVDD
A2, B2, C2, D2	LX1	AIO	10000	Switch node of buck, connect a 100 nH inductor between LX1 and output capacitor

Pin Number	Pin Name	Type (Table 2)	Drive (mA)	Description
A3, B3, C3, D3	PGND1	GND	10000	Buck power stage GND
A4, B4, C4, D4	PGND2	GND	10000	Buck power stage GND
A5, B5, C5, D5	LX2	AIO	10000	Switch node of buck, connect a 100 nH inductor between LX2 and output capacitor
A6, B6, C6, D6	PVDD2	PWR	10000	Supply voltage for buck power stage, decouple with 10 µF and connect to same source as AVDD
E1	GPIO1	DIO	10	General purpose I/O
E2	GPIO2	DIO	10	General purpose I/O
E3, F2	AGND	GND	10	Analog control and auxiliary circuitry GND
E4	FBP	AI	10	Buck positive node of differential voltage feedback, connect to VOUT1 at point of load
E5, F5	AVDD	PWR	10	Supply rail for analog control circuitry, decouple with 1 µF and connect to same source as PVDD
E6	SCL/GPIO3	DIO	15	I^2C clock or general purpose I/O
F1	CONF/GPIO0	AI/DIO	10	Chip configuration or general purpose I/O
F3	IC_EN	AI	10	Powers up I^2C control interface and auxiliary circuitry (including bandgap, oscillator, and references)
F4	FBN	AI	10	Buck negative node of differential voltage feedback, connect to GND at point of load
F6	SDA/GPIO4	DIO	15	I^2C data or general purpose I/O
G1, H1, J1, K1	PVDD3	PWR	10000	Supply voltage for buck power stage, decouple with 10 µF and connect to same source as AVDD
G2, H2, J2, K2	LX3	AIO	10000	Switch node of buck, connect a 100 nH inductor between LX3 and output capacitor
G3, H3, J3, K3	PGND3	GND	10000	Buck power stage VSS rail
G4, H4, J4, K4	PGND4	GND	10000	Buck power stage VSS rail
G5, H5, J5, K5	LX4	AIO	10000	Switch node of buck, connect a 100 nH inductor between LX4 and output capacitor
G6, H6, J6, K6	PVDD4	PWR	10000	Supply voltage for buck power stage, decouple with 10 µF and connect to same source as AVDD

Table 2. Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
PWR	Power	GND	Ground

4. Specifications

4.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Table 3. Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
T_{STG}	Storage temperature		-65	150	°C
T_J	Junction temperature		-40	150	°C
V_{SYS}	System supply voltage		-0.3	6.0	V
V_{PIN}	Voltage on pins		-0.3	6.0	V

4.2 Electrostatic Discharge Ratings

Table 4. Electrostatic Discharge Ratings

Parameter	Description	Conditions	Rating	Unit
V_{ESD_HBM}	Maximum ESD protection	Human body model (HBM) All exposed pins	2	kV
V_{ESD_CDM}	Maximum ESD protection	Charged device model (CDM)	500 Note 1	V

Note 1 Increased to 750 V for corner balls.

4.3 Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{SYS}	System supply voltage		2.8		5.5	V
V_{PIN}	Voltage on pins		-0.3		V_{SYS} + 0.3	V
T_J	Junction temperature		-40		150	°C
T_A	Ambient temperature		-40		125	°C

4.4 Thermal Specifications

Table 6. Package Ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
θ_{JA}	Thermal resistance junction to ambient	No heatsink Note 1		16.4		°C/W
		With heatsink Note 2		9.6		°C/W
θ_{JB}	Thermal resistance junction to board	Note 1		9.2		°C/W
θ_{JC}	Thermal resistance junction to case	Note 1		7.0		°C/W
P_D	Maximum power dissipation	No heatsink Derating factor above T_A = 85°C: 60.9 mW/°C ($1/\theta_{JA}$)	3660	4270		mW
		With heatsink Derating factor above T_A = 85°C:104.1 mW/°C ($1/\theta_{JA}$)	6250	7290		mW

Note 1 Obtained from package thermal simulations, JEDEC 2S2P four-layer board (114.3 mm x 101.6 mm x 1.6 mm), 70 µm (2 oz) copper thickness power planes, 35 µm (1 oz) copper thickness signal layer traces, natural convection (still air)

Note 2 As per Note 1 with addition of aluminum heatsink, 114.3 mm x 101.6 mm x 1.0 mm representing the lid of a case.

4.4.1 Power Derating Curves

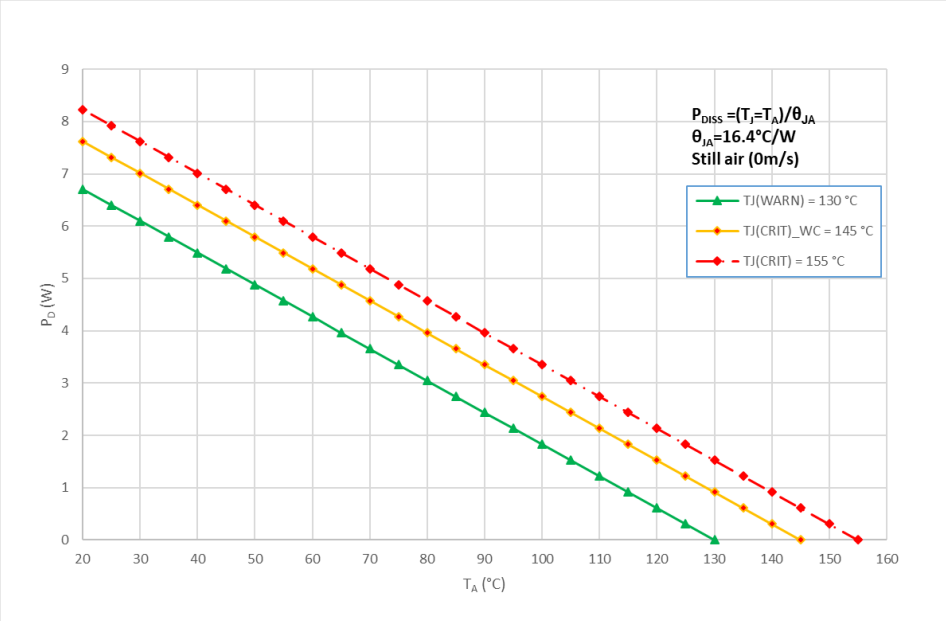


Figure 3. Power Derating Curve

Table 7. Typical Temperatures

	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C
T_{J_WARN}	P_D = 2.74 W	P_D = 1.52 W	P_D = 0.30 W
$T_{J\_CRIT\_WC}$	P_D = 3.66 W	P_D = 2.44 W	P_D = 1.22 W

4.5 Buck1 Characteristics

Unless otherwise noted, the following is valid for T_J = -40 °C to +150 °C, V_{SYS} = 2.8 V to 5.5 V.

Table 8: Quad-Phase Buck Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External electrical conditions						
V_{IN}	Input voltage	V_{IN} = V_{SYS} = V_{AVDD}	2.8		5.5	V
C_{OUT}	Total output capacitance, including voltage and temperature coefficient	Typ 10 x 22 µF -40% to +20%	132	220	264	µF
ESR_{COUT}	Output capacitor series resistance, per capacitor	f > 100 kHz		3		mΩ
L	Inductor value, per phase, including current and temperature dependence		88	110	132	nH
DCR_L	Inductor DC resistance			2		mΩ
Electrical performance						
V_{OUT}	Output voltage, configurable in 10 mV steps	I_{OUT} = 0 mA to $I_{OUT\_MAX\_PK}$ V_{IN} = 2.8 V to 5.5 V	0.5	0.85	1.3	V
V_{OUT_ACC}	Output voltage accuracy, including static line and load regulation	V_{OUT} ≥ 1 V	-1		1	%
V_{OUT_ACC}	Output voltage accuracy, including static line and load regulation	V_{OUT} < 1 V	-10		10	mV
$I_{OUT\_MAX\_CONT}$	Maximum continuous output current	With suitable thermal design	25			A
$I_{OUT\_MAX\_PK}$	Maximum peak output current	With suitable thermal design	40			A
I_{LIM}	Current limit, configureable per phase Note 1 Note 2			14.5		A
I_{LIM_ACC}	Current limit accuracy Note 2		-20		20	%
$V_{THR\_PG\_HYS}$	Power-good voltage threshold hysteresis	V_{OUT} = $V_{THR\_PG\_DWN}$	70	80	90	mV
$V_{THR\_PG\_DWN}$	Power-good voltage threshold for falling	V_{OUT} = V_{BUCK}	-170	-140	-110	mV
V_{THR_HV}	High V_{OUT} voltage threshold	V_{OUT} = V_{BUCK}	130	160	195	mV
$V_{OUT\_TR\_LINE}$	Line transient response	V_{IN} = 3.0 V to 3.6 V V_{OUT} = 1.1 V I_{OUT} = 0.5 * $I_{OUT\_MAX\_PK}$ dt = 10 µs		10		mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{SW}	Switching frequency			4		MHz
t_{ON_MIN}	Minimum turn-on pulse 0% duty is also supported			10		ns
t_{BUCK_EN}	Turn-on time	CH1_EN = high V_{IN} = 3.3 V V_{OUT} = 0.85 V DVC slew rate: 10 mV/8 µs No load Recommended capacitance		600		µs
R_{PD}	Output pull-down resistance for each phase at the LX node, see CH1_PD_DIS	V_{IN} = 3.3 V V_{OUT} = 0.5 V	140	150	160	Ω
R_{ON_PMOS}	On resistance of switching PMOS, per phase	V_{IN} = 3.3 V		12		mΩ
R_{ON_NMOS}	On resistance of switching NMOS, per phase	V_{IN} = 3.3 V		6		mΩ
PWM Mode						
η_{PWM}	Efficiency, PWM	V_{IN} = 3.3 V V_{OUT} = 1.1 V I_{OUT} = 5% ($I_{OUT\_MAX\_PK}$) to 80% ($I_{OUT\_MAX\_PK}$)		80		%
AUTO Mode						
$V_{OUT\_TR\_LD\_RISE}$	Load transient response, phase shedding enabled	V_{OUT} = 1.1 V I_{OUT} = 25% to 75% of $I_{OUT\_MAX\_PK}$ Load rise time = 1 µs	-5			%
$V_{OUT\_TR\_LD\_FALL}$	Load transient response, phase shedding enabled	V_{OUT} = 1.1 V I_{OUT} = 75% to 25% of $I_{OUT\_MAX\_PK}$ Load fall time = 1 µs			5	%
PFM Mode						
$I_{Q\_PFM\_1PH}$	Quiescent current in PFM	V_{IN} = 3.3 V No load No switching		120		µA
η_{PFM}	Efficiency, PFM	V_{IN} = 3.3 V V_{OUT} = 1.1 V I_{OUT} = 100 mA		80		%

Note 1 For applications requiring V_{OUT} < 0.75 V contact Renesas applications support for configuration setting

Note 2 t_{ON} > 40 ns

4.6 Performance and Supervision Characteristics

Table 9: Performance and Supervision Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical performance						
V_{THR_POR}	Power-on-reset threshold	Threshold for AVDD falling		2.1	2.25	V
$V_{THR\_POR\_HYS}$	Power-on-reset hysteresis			200		mV
T_{WARN}	Temperature warning threshold		120	130	140	°C
T_{CRIT}	Temperature shutdown threshold		145	155	165	°C
I_{IN_OFF}	Supply current	OFF state T_A = 27 °C IC_EN = 0		0.1	1	µA
I_{IN_ON}	Supply current	ON state T_A = 27 °C IC_EN = 1 Buck off	5	10	20	µA

4.7 Digital IO Characteristics

Table 10: Digital I/O Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical performance						
V_{IH_EN}	Input high voltage, IC enable		1.2		AVDD	V
V_{IL_EN}	Input low voltage, IC enable				0.4	V
t_{IC_EN}	IC enable time				1000	µs
$V_{IH\_GPIO\_SCL\_SDA}$	Input high voltage GPIO, SCL, SDA		1.2		AVDD	V
$V_{IL\_GPIO\_SCL\_SDA}$	Input low voltage GPIO, SCL, SDA				0.4	V
V_{OH_GPIO}	Output high voltage GPIO	Push-pull mode I_{OUT} = 1 mA	0.8*AVDD		AVDD	V
V_{OL_GPIO}	Output low voltage GPIO	Push-pull mode I_{OUT} = 1 mA			0.2*AVDD	V
V_{OL_SDA}	Output low voltage SDA	I_{OUT} = 3 mA		0.24		V
R_{PD}	GPIO pull-down resistor	V_{SYS} = 3.7 V Note 1	9	15	31	kΩ
R_{PU}	GPIO pull-up resistor	V_{SYS} = 3.7 V Note 1	28	45	72	kΩ

Note 1 Resistance may have greater variation, depending on voltage and temperature.

4.8 Timing Characteristics

Table 11: I2C Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical performance						
t_{BUS}	Bus free time between a STOP and START condition		0.5			µs
C_{BUS}	Bus line capacitive load				150	pF
f_{SCL}	SCL clock frequency		20 Note 1		1000	kHz
t_{LO_SCL}	SCL low time		0.5			µs
t_{HI_SCL}	SCL high time		0.26			µs
t_{RISE}	SCL and SDA rise time	Requirement for input			1000	ns
t_{FALL}	SCL and SDA fall time	Requirement for input			300	ns
t_{SETUP_START}	Start condition setup time		0.26			µs
t_{HOLD_START}	Start condition hold time		0.26			µs
t_{SETUP_STOP}	Stop condition setup time		0.26			µs
t_{DATA}	Data valid time				0.45	µs
t_{DATA_ACK}	Data valid acknowledge time				0.45	µs
t_{SETUP_DATA}	Data setup time		50			ns
t_{HOLD_DATA}	Data hold time		0			ns

Note 1 Minimum clock frequency is limited to 20 kHz if I2C_TIMEOUT is enabled

5. Typical Performance

The static efficiency measurement plots depicted in Figure 4 and Figure 5 were performed at 25°C in a temperature-controlled environment. A continuous load was used for the measurements therefore the peak current limit of 40 A was not reached.

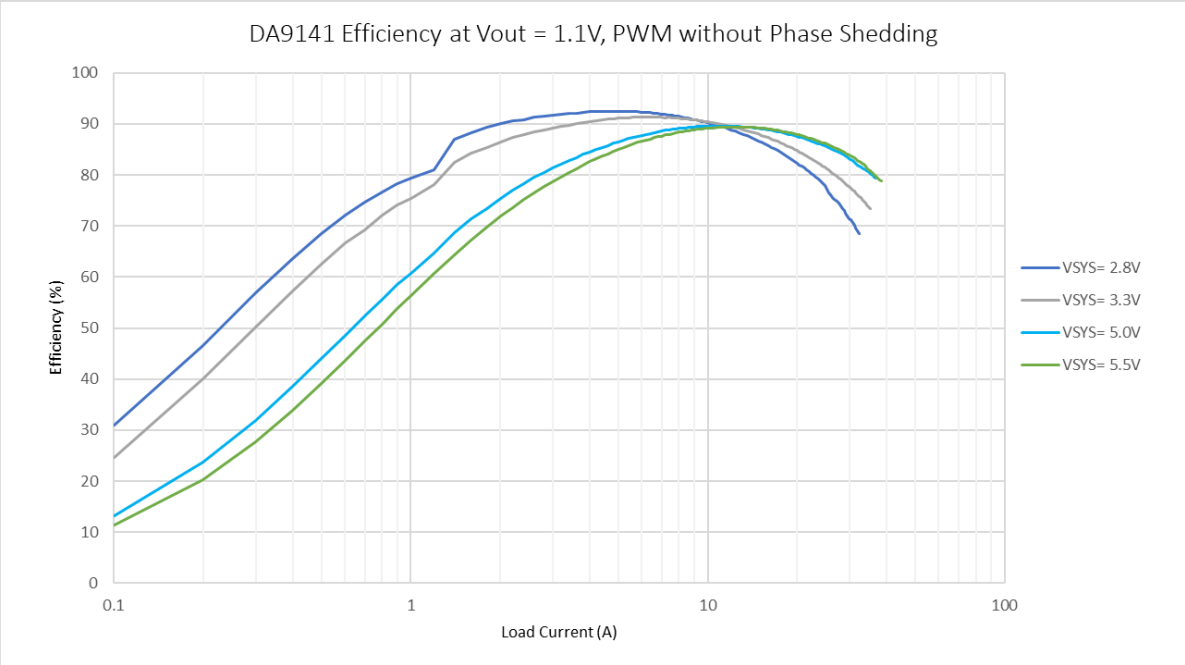


Figure 4. DA9141 Effciency, PWM Mode without Phase Shedding

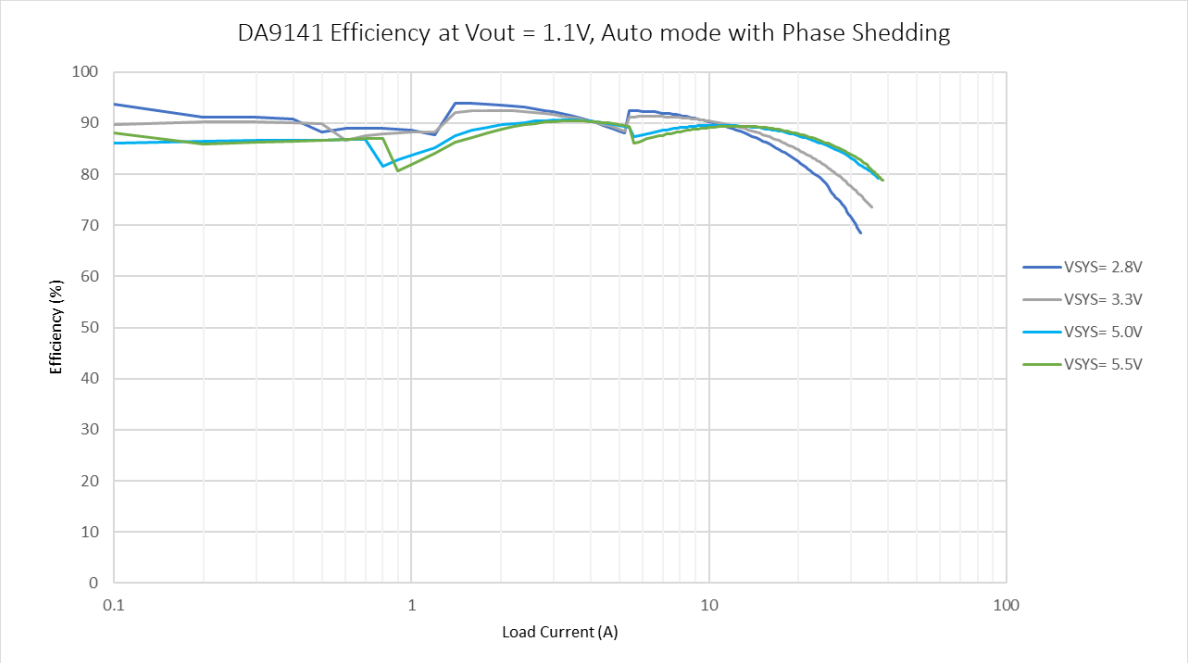


Figure 5. DA9141 Efficiency, Auto Mode with Phase Shedding

6. Functional Description

6.1 Operating Modes

6.1.1 ON

DA9141 is ON when the IC_EN pin is higher than V_{IH_EN} and the supply voltage is higher than V_{THR_POR}. Once enabled, the host processor can start communicating with DA9141 using the control interface, after the t_{IC_EN} delay.

6.1.2 OFF

DA9141 is OFF when the IC_EN pin is lower than V_{IL_EN}. In OFF, the buck is always disabled and the LX nodes are pulled down by a (typically 150 Ω) internal pull-down resistor.

6.2 DC-DC Buck Converter

DA9141 operates as a single-channel, quad-phase buck converter which delivers up to 40 A output current at a 0.5 V to 1.3 V output voltage range.

The buck converter has two configurable output voltage settings. One is the normal output voltage (A), the other offers an alternative retention voltage (B). The bits used to configure the outputs are CH1_A_VOUT and CH1_B_VOUT. In this way, different application power modes are supported. The target output voltage (either A or B) is toggled by either GPI or I²C control interface, providing maximum flexibility for the application's host processor.

When the buck is enabled, its output voltage is monitored and a power-good signal indicates that the buck output voltage has reached a level higher than the power-good rise threshold. The power-good status is lost when the voltage drops below $V_{THR\_PG\_DWN}$ or increases above V_{THR_HV}. $V_{THR\_PG\_HYS}$ is the value that defines the hysteresis between a power-good rise and $V_{THR\_PG\_DWN}$. The status of the power-good indicator is read back via I²C from the PG1 status bit. Alternatively, it can be assigned to any of the GPIOs by setting the GPIO<x>_MODE bits to PG1 output.

The buck converter is capable of supporting DVC transitions that occur when:

- the active and selected A- or B-voltage is updated to a new target value, using bits CH1_A_VOUT and CH1_B_VOUT
- the voltage selection is toggled from the A- to B-voltage (or B- to A-voltage), using bit CH1_VSEL or via GPI control

The DVC operates in pulse-width-modulation (PWM) mode with synchronous rectification. The slew rate of the DVC ramp up and ramp down transitions is programmed at 10 mV per (8, 4, 2, 1, or 0.5) µs in register bits CH1_SR_DVC_DWN and CH1_SR_DVC_UP.

A pull-down resistor (typically 150 Ω) for each phase is always activated when the buck is disabled, unless it is disabled by setting register bits CH1_PD_DIS to 0x1.

6.2.1 Switching Frequency

The buck switching frequency is tuned using register bit OSC_TUNE. The internal 8 MHz oscillator frequency is tuned in ±160 kHz steps. This impacts the buck converter frequency in steps of 80 kHz and helps to mitigate possible disturbances to other high frequency systems in the application.

6.2.2 Operation Modes and Phase Selection

The buck converter operates in PWM or PFM modes. The operating mode is selected using register bits CH1_A_MODE and CH1_B_MODE.

Phase shedding automatically changes between 1- and 4-phase operation at a typical current of 4 A.

If the automatic operation mode (Auto mode) is selected, the buck converter automatically changes between synchronous PWM mode and PFM mode depending on the load current. This improves the efficiency across the range of output load currents.

6.2.3 Output Voltage Selection

The switching converter is configured using the I²C interface.

Two output voltages (Value A and Value B in Figure 6) are pre-configured in registers CH1_A_VOUT and CH1_B_VOUT. The output voltage (VBUCK in Figure 6) is selected by toggling register bit CH1_VSEL, by re-programming the selected voltage control register, or by toggling a GPI if configured to do so. Any of these options will result in ramped voltage transitions.

After being enabled, the buck converter uses, by default, the register settings in CH1_A_VOUT (Value A) unless the output voltage selection is configured via the GPI port to be CH1_B_VOUT.

Register bits CH1_VMAX limit the output voltage that can be set.

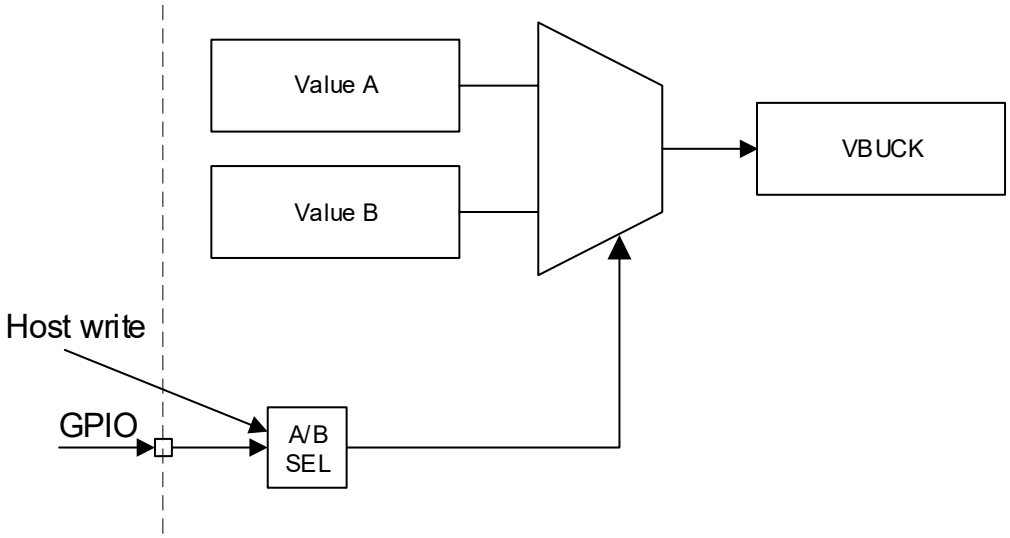


Figure 6. Buck Output Voltage Control Concept

6.2.4 Soft Startup and Shutdown

To limit in-rush current from VSYS, the buck converter performs a soft-start after being enabled. The startup behavior is a compromise between acceptable inrush current from the battery and turn-on time. Ramp times are configured in register CH1_SR_STARTUP.

Note: Rates higher than 5 mV/µs may produce overshoot during the startup phase.

A ramped power down is selected in register bits CH1_SR_SHDN. When no ramp is selected (immediate power down), the output node is discharged only by the pull-down resistor, if enabled, in register CH1_PD_DIS.

6.2.5 Current Limit

The integrated current limit protects the power stages and external coil from excessive current. It should be configured to at least 40% higher than the required maximum per phase output current.

Note: This value is loaded from the OTP.

When the current limit is reached, the buck converter generates an event and an interrupt to the host processor unless the interrupt has been masked using bit M_OC1 in SYS_MASK_1. Register bit OC_DVC_MASK masks over-current events during DVC transitions.

6.2.6 Temperature Protection

DA9141 is protected from internal overheating by temperature-triggered shutdown.

DA9141 uses two flags for temperature protection. When $T_J > T_{WARN}$, meaning that the chip is running close to its thermal limits, an IRQ is raised and an event is set, although the chip continues working.

When $T_J > T_{CRIT}$, another IRQ and event are set, and the bucks are immediately shut down. T_J needs to be below T_{WARN} and the event flags need to be cleared before starting the bucks.

Table 12. Temperature Protection Control Registers

Category	Register Name	Description
Status	TEMP_WARN	Asserts when the temperature warning threshold is reached
	TEMP_CRIT	Asserts when the temperature shutdown threshold is reached
IRQ event	E_TEMP_WARN	TEMP_WARN caused event
	E_TEMP_CRIT	TEMP_CRIT caused event
IRQ mask	M_TEMP_WARN	TEMP_WARN event IRQ mask
	M_TEMP_CRIT	TEMP_CRIT event IRQ mask
	M_VR_HOT	TEMP_WARN status IRQ mask

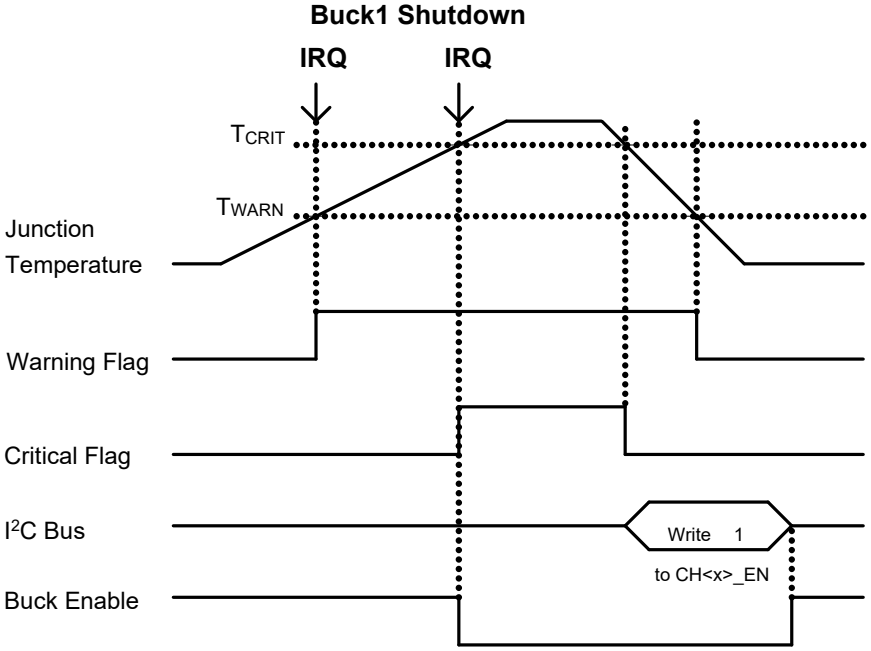


Figure 7. Temperature Protection Operation

6.3 Control Circuits

6.3.1 Chip Enable and Disable

The IC_EN pin enables and disables the IC. When IC_EN = 0, all blocks, except for low I_Q POR, power down and the buck output is pulled down.

6.3.2 GPIO

6.3.2.1 GPIO Pin Assignment

The DA9141 provides up to five GPIO pins, three if the I²C is enabled, see Table 13. The registers that configure the GPIO pin assignments are OTP programmable.

GPIO0 can be programmed (OTP option) to function as chip configuration (CONF), see section 6.3.2.3. When the I²C interface is enabled (OTP option) any register settings for GPIO3 and GPIO4 are ignored and GPIO3 and GPIO4 function as SCL and SDA respectively.

Note: GPIO3 and GPIO4 functions are limited only to output features if I2C_EN = 0.

Table 13. GPIO Pin Assignment

OTP Option		GPIO Pin					Available GPIOs
I²C	CONF	CONF/ GPIO0	GPIO1	GPIO2	SCL/ GPIO3	SDA/ GPIO4	
Disabled	Disabled	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	5
	Enabled	CONF	GPIO1	GPIO2	GPIO3	GPIO4	4
Enabled	Disabled	GPIO0	GPIO1	GPIO2	SCL	SDA	3
	Enabled	CONF	GPIO1	GPIO2	SCL	SDA	2

6.3.2.2 GPIO Function

The GPIO pins are configurable as the following functions in register GPIO<x>_MODE (x = 0 to 4):

- Buck1 enable input (EN1)
- Buck1 DVC control input (DVC1)
- Buck1 OTP setting reload input (RELOAD)
- Buck1 power-good output (PG1)
- Interrupt output (nIRQ)

6.3.2.3 Chip Configuration Select

GPIO0 functions as chip configuration select (CONF) input when enabled as an OTP setting.

Three different chip configurations can be selected according to the CONF pin level.

- GPIO0 low: OTP default or CONF0 on reload
- GPIO0 high: CONF1
- GPIO0 floating: CONF2 - not recommended.

Table 14 lists the device configurations that can be modified if CONF_EN = 1. Register CONF_EN is set by OTP, see section 10.1.

Table 14. GPIO0 Configurable Registers when CONF Enabled

Register Name	Description
IF_SLAVE_ADDR[6:0]	I²C slave address
CH1_A_MODE[1:0]	CH1_A Operation mode select
CH1_B_MODE[1:0]	CH1_B Operation mode select
CH1_VSEL	CH1 output voltage and operation selection

Register Name	Description
CH1_EN	CH1 enable
CH1_A_VOUT[7:0]	CH1 output voltage setting A
CH1_B_VOUT[7:0]	CH1 output voltage setting B
M_PG1_STAT	IRQ mask setting for CH1 power-good status
M_VR_HOT	IRQ mask setting for temp warning status
GPIO1_MODE[3:0]	GPIO1 mode setting
GPIO2_MODE[3:0]	GPIO2 mode setting
GPIO1_OBUF	GPIO1 output buffer select
GPIO2_OBUF	GPIO2 output buffer select
GPIO1_TRIG[1:0]	GPIO1 input trigger select
GPIO1_POL	GPIO1 polarity select
GPIO1_PUPD	GPIO1 pull-up/pull-down enable
GPIO1_DEB[1:0]	GPIO1 input debounce time setting
GPIO1_DEB_RISE	GPIO1 input debounce rising edge enable
GPIO1_DEB_FALL	GPIO1 input debounce falling edge enable
GPIO2_TRIG[1:0]	GPIO2 input trigger select
GPIO2_POL	GPIO2 polarity select
GPIO2_PUPD	GPIO2 pull-up/pull-down enable
GPIO2_DEB[1:0]	GPIO2 input debounce time setting
GPIO2_DEB_RISE	GPIO2 input debounce rising edge enable
GPIO2_DEB_FALL	GPIO2 input debounce falling edge enable

6.3.3 Interrupt

When an event is triggered, the nIRQ interrupt flag is asserted. Trigger conditions and control registers for each interrupt event are listed in Table 15.

Some of these events are categorized as fault events and affect device operation (for example, buck disable), see section 6.2.6.

Table 15. Interrupt List

Name	Trigger	IRQ Status Register	IRQ Mask Register	Deglitch Period
Temperature warning (event)	T_J rising above T_{WARN}	E_TEMP_WARN	M_TEMP_WARN	0 s
Temperature critical (event)	T_J rising above T_{CRIT}	E_TEMP_CRIT	M_TEMP_CRIT	0 s
System good (event)	Buck1 power-good event	E_SG	M_SG	0s
Buck1 power-good (event)	Buck1 V_{OUT} is in power-good voltage range (not under- or over-voltage)	E_PG1	M_PG1	0 s
Buck1 over-voltage (event)	Buck1 V_{OUT} rising above over-voltage threshold (target voltage + 150 mV)	E_OV1	M_OV1	Rise: 8 µs Fall: 8 µs
Buck1 under-voltage (event)	Buck1 V_{OUT} falling below under-voltage threshold (target voltage - $V_{TH\_PG\_FALL}$)	E_UV1	M_UV1	0 s
Buck1 over-current (event)	Buck1 current rising above over-current threshold	E_OC1	M_OC1	0 s
Buck1 power-good (status) (Note 1)	Buck1 V_{OUT} is in power-good voltage range (not under- or over-voltage)	PG1	M_PG1_STAT (Note 2)	0 s
System good (status) (Note 1)	Buck1 power-good is active	SG	S_PG_STAT (Note 2)	0 s
Temperature warning (status) (Note 1)	T_J above T_{WARN}	TEMP_WARN	M_VR_HOT (Note 2)	0 s
GPIO0 change (event)	Detect GPIO0 change for active trigger selected by GPIO0_TRIG register	E_GPIO0	M_GPIO0	100 µs, 1 ms, or 10 ms 100 ms
GPIO1 change (event)	Detect GPIO1 change for active trigger selected by GPIO1_TRIG register	E_GPIO1	M_GPIO1	
GPIO2 change (event)	Detect GPIO2 change for active trigger selected by GPIO2_TRIG register	E_GPIO2	M_GPIO2	

Note 1 Interrupt outputs the status as is. I^2C write is not required for interrupt clear

Note 2 Note 2 OTP load value defined by CONF pin setting (if CONF pin enabled).

Table 16 and Table 17 show the interrupt registers' structure. See section 6.3.2.3 for bitfield descriptions.

Table 16. Interrupt Registers Except for Power-Good Status

Register	Description
E_<name>	Read-only interrupt event register 0: No interrupt 1: Interrupt occurred **Cleared after being written to I²C**. Set until IRQ is removed.
M_<name>	Interrupt mask register 0: Not masked 1: Masked. No IRQ signal sent. Event register (E_<name>) is updated.

Table 17. Interrupt Registers for Power-Good and Temperature Warning Status

Register	Description
PG1	Buck1 power-good status. Asserted as long as Buck1 output voltage is in range (under-voltage threshold < buck output voltage < over-voltage threshold) 0: Not power-good 1: Power-good
M_PG1_STAT	Power-good status interrupt mask register 0: Not masked 1: Masked. No IRQ signal sent. Power-good status register (PG1) is updated
TEMP_WARN	Asserted as long as the temperature warning threshold (T_{WARN}) is reached 0: Junction temperature is below T_{WARN} 1: Junction temperature is above T_{WARN}
M_VR_HOT	Temperature warning status (TEMP_WARN) interrupt mask register 0: Not masked 1: Masked. No IRQ signal sent. Temperature warning status register (TEMP_WARN) is updated

It is possible to route interrupts to a GPIO by setting the bitfield GPIO<x>_MODE = 0xC on the relevant GPIO.

nIRQ's behavior is shown in Figure 8. If GPIO_n_POL = 0, nIRQ will be high under normal operation, when system-good status is high, and pulled low if an event listed in Table 15 occurs.

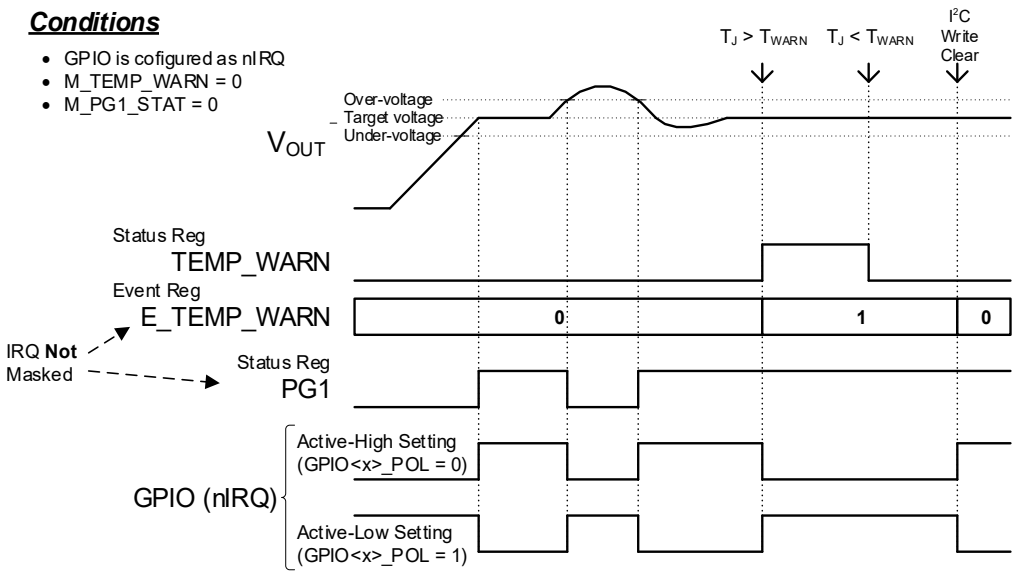


Figure 8. Interrupt Operation Example

6.4 I²C Communication

All features of DA9141 can be controlled with the I²C interface, which is enabled or disabled as an OTP setting.

I²C	Description
Disabled	SCL/GPIO3 and SDA/GPIO4 pins should be used as GPO
Enabled	SCL/GPIO3 and SDA/GPIO4 pins are used as I²C clock input and I²C data input/output.

GPIO3 functions as the I²C clock (SCL) and GPIO4 carries all the power manager bidirectional I²C data (SDA). The I²C interface is open drain supporting multiple devices on a single line. The bus lines have to be pulled high by external pull-up resistors (2 kΩ to 20 kΩ). The standard frequency of the I²C bus is 1 MHz in fast-mode plus (FM+), 400 kHz in fast-mode, or 100 kHz in standard mode.

6.4.1 I²C Protocol

All data is transmitted across the I²C bus in eight-bit groups. To send a bit, the SDA line is driven towards the intended state while the SCL is low (a low SDA indicates a zero bit). Once the SDA has settled, the SCL line is brought high and then low. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two-byte serial protocol is used containing one byte for address and one byte for data. Data and address transfer are transmitted MSB first for both read and write operations. All transmissions begin with the START condition from the master while the bus is in idle state (the bus is free). It is initiated by a high to low transition on the SDA line while the SCL is in the high state (a STOP condition is indicated by a low to high transition on the SDA line while the SCL is in the high state).

Figure 9. I²C START and STOP Condition Timing

The I²C bus is monitored for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. The acknowledge is done by pulling the SDA line low during the following clock cycle (white blocks marked with A in Figure 10 and Figure 11).

The protocol for a register write from master to slave consists of a START condition, a slave address with read/write bit, and the eight-bit register address followed by eight bits of data, terminated by a STOP condition. DA9141 responds to all bytes with acknowledge (A), see Figure 10.

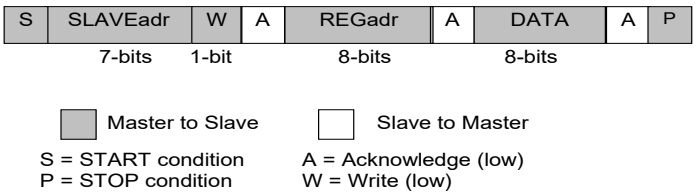


Figure 10. I²C Byte Write (SDA Line)

When the host reads data from a register it first has to write to DA9141 with the target register address and then read from DA9141 with a repeated START, or alternatively a second START, condition. After receiving the data, the host sends no acknowledge (A*) and terminates the transmission with a STOP condition, see Figure 11.

Default I²C address is 0xD4 (0x6A excluding the R/W bit). It is possible to change this address by writing the new address to the register SYS_CFG_SLVADDR, see Table 41.

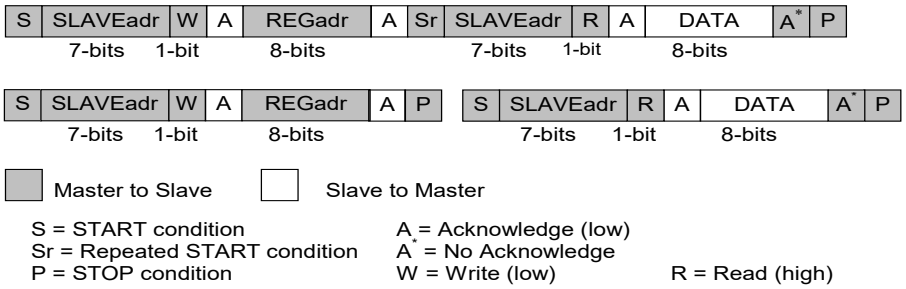


Figure 11. I²C Byte Read (SDA Line) Examples

7. Register Definitions

7.1 Register Map

Table 18: Register Map

Addr	Register	7	6	5	4	3	2	1	0
System Module									
0x01	SYS_STATUS_0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved 0	TEMP_CRIT	TEMP_WARN
0x02	SYS_STATUS_1	Reserved	Reserved	Reserved	Reserved	PG1	OV1	UV1	OC1
0x03	SYS_STATUS_2	Reserved	Reserved	Reserved	Reserved	Reserved	GPIO2	GPIO1	GPIO0
0x04	SYS_EVENT_0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved 0	E_TEMP_CRIT	E_TEMP_WARN
0x05	SYS_EVENT_1	Reserved	Reserved	Reserved	Reserved	E_PG1	E_OV1	E_UV1	E_OC1
0x06	SYS_EVENT_2	Reserved	Reserved	Reserved	Reserved	Reserved	E_GPIO2	E_GPIO1	E_GPIO0
0x07	SYS_MASK_0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved 1	M_TEMP_CRIT	M_TEMP_WARN
0x08	SYS_MASK_1	Reserved	Reserved	Reserved	Reserved	M_PG1	M_OV1	M_UV1	M_OC1
0x09	SYS_MASK_2	Reserved	Reserved	Reserved	Reserved	Reserved	M_GPIO2	M_GPIO1	M_GPIO0
0x0A	SYS_MASK_3	Reserved	Reserved	Reserved	Reserved	M_VR_HOT	Reserved 1	Reserved	M_PG1_STAT
0x0B	SYS_CONFIG_0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x0D	SYS_CONFIG_2	Reserved	OC_LATCHOFF<1:0>		OC_DVC_MASK	PG_DVC_MASK<1:0>		Reserved	Reserved
0x0E	SYS_CONFIG_3	Reserved	OSC_TUNE<2:0>			Reserved	Reserved	I2C_TIMEOUT	Reserved 0
0x10	SYS_GPIO0_0	Reserved	Reserved	Reserved	GPIO0_MODE<3:0>				GPIO0_OBUF
0x11	SYS_GPIO0_1	GPIO0_DEB_FALL	GPIO0_DEB_RISE	GPIO0_DEB<1:0>		GPIO0_PUPD	GPIO0_POL	GPIO0_TRIG<1:0>	
0x12	SYS_GPIO1_0	Reserved	Reserved	Reserved	GPIO1_MODE<3:0>				GPIO1_OBUF
0x13	SYS_GPIO1_1	GPIO1_DEB_FALL	GPIO1_DEB_RISE	GPIO1_DEB<1:0>		GPIO1_PUPD	GPIO1_POL	GPIO1_TRIG<1:0>	
0x14	SYS_GPIO2_0	Reserved	Reserved	Reserved	GPIO2_MODE<3:0>				GPIO2_OBUF
0x15	SYS_GPIO2_1	GPIO2_DEB_FALL	GPIO2_DEB_RISE	GPIO2_DEB<1:0>		GPIO2_PUPD	GPIO2_POL	GPIO2_TRIG<1:0>	
0x16	SYS_GPIO3_0	Reserved	Reserved	Reserved	GPIO3_MODE<3:0>				GPIO3_OBUF
0x17	SYS_GPIO3_1	GPIO3_DEB_FALL	GPIO3_DEB_RISE	GPIO3_DEB<1:0>		GPIO3_PUPD	GPIO3_POL	GPIO3_TRIG<1:0>	
0x18	SYS_GPIO4_0	Reserved	Reserved	Reserved	GPIO4_MODE<3:0>				GPIO4_OBUF
0x19	SYS_GPIO4_1	GPIO4_DEB_FALL	GPIO4_DEB_RISE	GPIO4_DEB<1:0>		GPIO4_PUPD	GPIO4_POL	GPIO4_TRIG<1:0>	

Addr	Register	7	6	5	4	3	2	1	0
Buck Control									
Buck1									
0x20	BUCK_BUCK1_0	Reserved	CH1_SR_DVC_DWN<2:0>			CH1_SR_DVC_UP<2:0>			CH1_EN
0x21	BUCK_BUCK1_1	Reserved	CH1_SR_SHDN<2:0>			CH1_SR_STARTUP<2:0>			CH1_PD_DIS
0x22	BUCK_BUCK1_2	Reserved	Reserved	Reserved	Reserved	CH1_ILIM<3:0>			
0x23	BUCK_BUCK1_3	CH1_VMAX<7:0>							
0x24	BUCK_BUCK1_4	Reserved	Reserved	Reserved	CH1_VSEL	CH1_B_MODE<1:0>		CH1_A_MODE<1:0>	
0x25	BUCK_BUCK1_5	CH1_A_VOUT<7:0>							
0x26	BUCK_BUCK1_6	CH1_B_VOUT<7:0>							
0x27	BUCK_BUCK1_7	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CH1_RIPPLE_CANCEL<1:0>	
OTP Control									
Serialization									
0x48	OTP_DEVICE_ID	DEV_ID<7:0>							
0x49	OTP_VARIANT_ID	MRC<3:0>				VRC<3:0>			
0x4A	OTP_CUSTOMER_ID	CUST_ID<7:0>							
0x4B	OTP_CONFIG_ID	CONFIG_REV<7:0>							

7.2 Register Descriptions

7.2.1 System

Table 19: SYS_STATUS_0 (0x01)

Bit	Type	Field Name	Description
[1]	R	TEMP_CRIT	Asserted when the thermal shutdown threshold is reached
[0]	R	TEMP_WARN	Asserted when the thermal warning threshold is reached

Table 20: SYS_STATUS_1 (0x02)

Bit	Type	Field Name	Description
[3]	R	PG1	Asserted when the buck output voltage is in range
[2]	R	OV1	Asserted when the buck exceeds the over-voltage threshold
[1]	R	UV1	Asserted when the buck exceeds the under-voltage threshold
[0]	R	OC1	Asserted when the buck exceeds the over-current threshold

Table 21: SYS_STATUS_2 (0x03)

Bit	Type	Field Name	Description
[2]	R	GPIO2	GPIO2 input readback status - asserted if the input on GPIO is seen as logic high
[1]	R	GPIO1	GPIO1 input readback status - asserted if the input on GPIO is seen as logic high
[0]	R	GPIO0	GPIO0 input readback status - asserted if the input on GPIO is seen as logic high

Table 22: SYS_EVENT_0 (0x04)

Bit	Type	Field Name	Description
[1]	RW1C	E_TEMP_CRIT	An over-temperature event has occurred. Write 0x1 to reset this bit to 0x0 when the event source has been released.
[0]	RW1C	E_TEMP_WARN	A temperature warning event has occurred. Write 0x1 to reset this bit to 0x0 when the event source has been released.

Table 23: SYS_EVENT_1 (0x05)

Bit	Type	Field Name	Description
[3]	RW1C	E_PG1	PG1 caused event. Write 0x1 to reset this bit to 0x0 when the event source has been released.
[2]	RW1C	E_OV1	OV1 caused event. Write 0x1 to reset this bit to 0x0 when the event source has been released.
[1]	RW1C	E_UV1	UV1 caused event. Write 0x1 to reset this bit to 0x0 when the event source has been released.
[0]	RW1C	E_OC1	OC1 caused event. Write 0x1 to reset this bit to 0x0 when the event source has been released.

Table 24: SYS_EVENT_2 (0x06)

Bit	Type	Field Name	Description
[2]	RW1C	E_GPIO2	GPIO2 caused event. Write 0x1 to reset this bit to 0x0 when the event source has been released.

Bit	Type	Field Name	Description
[1]	RW1C	E_GPIO1	GPIO1 caused event. Write 0x1 to reset this bit to 0x0 when the event source has been released.
[0]	RW1C	E_GPIO0	GPIO0 caused event. Write 0x1 to reset this bit to 0x0 when the event source has been released.

Table 25: SYS_MASK_0 (0x07)

Bit	Type	Field Name	Description
[1]	RW	M_TEMP_CRIT	Thermal shutdown can cause an interrupt. Write 0x1 to mask this cause of interrupt.
[0]	RW	M_TEMP_WARN	Temperature warning can cause an interrupt. Write 0x1 to mask this cause of interrupt.

Table 26: SYS_MASK_1 (0x08)

Bit	Type	Field Name	Description
[3]	RW	M_PG1	PG1 event can cause an interrupt. Write 0x1 to mask this cause of interrupt.
[2]	RW	M_OV1	OV1 event can cause an interrupt. Write 0x1 to mask this cause of interrupt.
[1]	RW	M_UV1	UV1 event can cause an interrupt. Write 0x1 to mask this cause of interrupt.
[0]	RW	M_OC1	OC1 event can cause an interrupt. Write 0x1 to mask this cause of interrupt.

Table 27: SYS_MASK_2 (0x09)

Bit	Type	Field Name	Description
[2]	RW	M_GPIO2	GPIO2 event can cause an interrupt. Write 0x1 to mask this cause of interrupt.
[1]	RW	M_GPIO1	GPIO1 event can cause an interrupt. Write 0x1 to mask this cause of interrupt.
[0]	RW	M_GPIO0	GPIO0 event can cause an interrupt. Write 0x1 to mask this cause of interrupt.

Table 28: SYS_MASK_3 (0x0A)

Bit	Type	Field Name	Description
[3]	RW	M_VR_HOT	Temperature warning status IRQ mask. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)
[0]	RW	M_PG1_STAT	PG1 status IRQ mask. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)

Table 29: SYS_CONFIG_2 (0x0D)

Bit	Type	Field Name	Description
[6:5]	RW	OC_LATCHOFF	Over-current latch-off time (Debounce duration). Buck shuts down after over-current persists for 8 µs, 1 ms or 3 ms unless setting is disabled setting. An IRQ is generated unless masked. **Value** **Description** 0x0 Latch off disable 0x1 Latch off after 8 µs

Bit	Type	Field Name	Description
			0x2 Latch off after 1 ms 0x3 Latch off after 3 ms
[4]	RW	OC_DVC_MASK	Over-current event mask during DVC ramp-up and ramp-down. Write 0x1 to mask over-current during DVC causing IRQ and LATCHOFF.
[3:2]	RW	PG_DVC_MASK	Power good mask during DVC **Value** **Description** 0x0 No mask 0x1 Mask as not power good 0x2 Mask as power good 0x3 Reserved

Table 30: SYS_CONFIG_3 (0x0E)

Bit	Type	Field Name	Description
[6:4]	RW	OSC_TUNE	Tune oscillator frequency, tuned frequency = current frequency + OSC_TUNE * 160 kHz **Value** **Description** 0x3 3 0x2 2 0x1 1 0x0 0 0x7 -1 0x6 -2 0x5 -3 0x4 -4
[1]	RW	I2C_TIMEOUT	Enable automatic reset of 2 wire interface (if SDA stays low for > 50 ms).

Table 31: SYS_GPIO0_0 (0x10)

Bit	Type	Field Name	Description
[4:1]	RW	GPIO0_MODE	GPIO function mode select **Value** **Description** 0x0 GPIO disable 0x1 EN1 input 0x2 Reserved 0x3 EN1 input 0x4 DVC1 input 0x5 Reserved 0x6 DVC1 input 0x7 RELOAD input 0x8 PG1 output 0x9 Low output

Bit	Type	Field Name	Description
			0xA Low output 0xB PG1 output 0xC nIRQ output 0xD Reserved 0xE Low output 0xF High output
[0]	RW	GPIO0_OBUF	GPIO output buffer select **Value** **Description** 0x0 open-drain output 0x1 push-pull output

Table 32: SYS_GPIO0_1 (0x11)

Bit	Type	Field Name	Description
[7]	RW	GPIO0_DEB_FALL	GPI debounce falling edge
[6]	RW	GPIO0_DEB_RISE	GPI debounce rising edge
[5:4]	RW	GPIO0_DEB	GPI debounce time **Value** **Description** 0x0 100 µs debounce 0x1 1 ms debounce 0x2 10 ms debounce 0x3 100 ms debounce
[3]	RW	GPIO0_PUPD	GPIO pull-up/pull-down enable **Value** **Description** 0x0 GPI: pull-down disabled, GPO: pull-up to AVDD disabled 0x1 GPI: pull-down enabled, GPO: pull-up to AVDD enabled
[2]	RW	GPIO0_POL	GPIO polarity **Value** **Description** 0x0 GPIO is active-high 0x1 GPIO is active-low
[1:0]	RW	GPIO0_TRIG	GPI trigger type **Value** **Description** 0x0 Dual-edge triggered 0x1 Positive-edge triggered 0x2 Negative-edge triggered 0x3 Reserved (No trigger)

Table 33: SYS_GPIO1_0 (0x12)

Bit	Type	Field Name	Description
[4:1]	RW	GPIO1_MODE	GPIO function mode select. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) **Value** **Description** 0x0 GPIO disable 0x1 EN1 input 0x2 Reserved 0x3 EN1 input 0x4 DVC1 input 0x5 Reserved 0x6 DVC1 input 0x7 RELOAD input 0x8 PG1 output 0x9 Low output 0xA Low output 0xB PG1 output 0xC nIRQ output 0xD Reserved 0xE Low output 0xF High output
[0]	RW	GPIO1_OBUF	GPIO output buffer select. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting). **Value** **Description** 0x0 open-drain output 0x1 push-pull output

Table 34: SYS_GPIO1_1 (0x13)

Bit	Type	Field Name	Description
[7]	RW	GPIO1_DEB_FALL	GPI debounce falling edge. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)
[6]	RW	GPIO1_DEB_RISE	GPI debounce rising edge. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)
[5:4]	RW	GPIO1_DEB	GPI debounce time. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) **Value** **Description** 0x0 100 µs debounce 0x1 1 ms debounce 0x2 10 ms debounce 0x3 100 ms debounce
[3]	RW	GPIO1_PUPD	GPIO pull-up/pull-down enable. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)

Bit	Type	Field Name	Description
			Value **Description** 0x0 GPI: pull-down disabled, GPO: pull-up to AVDD disabled 0x1 GPI: pull-down enabled, GPO: pull-up to AVDD enabled
[2]	RW	GPIO1_POL	GPIO polarity. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) **Value** **Description** 0x0 GPIO is active-high 0x1 GPIO is active-low
[1:0]	RW	GPIO1_TRIG	GPI trigger type. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) **Value** **Description** 0x0 Dual-edge triggered 0x1 Positive-edge triggered 0x2 Negative-edge triggered 0x3 Reserved (No trigger)

Table 35: SYS_GPIO2_0 (0x14)

Bit	Type	Field Name	Description
[4:1]	RW	GPIO2_MODE	GPIO function mode select. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) **Value** **Description** 0x0 GPIO disable 0x1 EN1 input 0x2 Reserved 0x3 EN1 input 0x4 DVC1 input 0x5 Reserved 0x6 DVC1 input 0x7 RELOAD input 0x8 PG1 output 0x9 Low output 0xA Low output 0xB PG1 output 0xC nIRQ output 0xD Reserved 0xE Low output 0xF High output
[0]	RW	GPIO2_OBUF	GPIO output buffer select. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)

Bit	Type	Field Name	Description
			Value **Description** 0x0 open-drain output 0x1 push-pull output

Table 36: SYS_GPIO2_1 (0x15)

Bit	Type	Field Name	Description
[7]	RW	GPIO2_DEB_FALL	GPI debounce falling edge. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)
[6]	RW	GPIO2_DEB_RISE	GPI debounce rising edge. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)
[5:4]	RW	GPIO2_DEB	GPI debounce time. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) **Value** **Description** 0x0 100 µs debounce 0x1 1 ms debounce 0x2 10 ms debounce 0x3 100 ms debounce
[3]	RW	GPIO2_PUPD	GPIO pull-up/pull-down enable. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) **Value** **Description** 0x0 GPI: pull-down disabled, GPO: pull-up to AVDD disabled 0x1 GPI: pull-down enabled, GPO: pull-up to AVDD enabled
[2]	RW	GPIO2_POL	GPIO polarity. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) **Value** **Description** 0x0 GPIO is active-high 0x1 GPIO is active-low
[1:0]	RW	GPIO2_TRIG	GPI trigger type. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) **Value** **Description** 0x0 Dual-edge triggered 0x1 Positive-edge triggered 0x2 Negative-edge triggered 0x3 Reserved (No trigger)

Table 37: SYS_GPIO3_0 (0x16)

Bit	Type	Field Name	Description
[4:1]	R	GPIO3_MODE	GPIO function mode select **Value** **Description** 0x0 GPIO disable

Bit	Type	Field Name	Description
			0x1 EN1 input 0x2 Reserved 0x3 EN1 input 0x4 DVC1 input 0x5 Reserved 0x6 DVC1 input 0x7 RELOAD input 0x8 PG1 output 0x9 Low output 0xA Low output 0xB PG1 output 0xC nIRQ output 0xD Reserved 0xE Low output 0xF High output
[0]	R	GPIO3_OBUF	GPIO output buffer select **Value** **Description** 0x0 open-drain output 0x1 push-pull output

Table 38: SYS_GPIO3_1 (0x17)

Bit	Type	Field Name	Description
[7]	R	GPIO3_DEB_FALL	GPI debounce falling edge
[6]	R	GPIO3_DEB_RISE	GPI debounce rising edge
[5:4]	R	GPIO3_DEB	GPI debounce time **Value** **Description** 0x0 100 µs debounce 0x1 1 ms debounce 0x2 10 ms debounce 0x3 100 ms debounce
[3]	R	GPIO3_PUPD	GPIO pull-up/pull-down enable **Value** **Description** 0x0 GPI: pull-down disabled, GPO: pull-up to AVDD disabled 0x1 GPI: pull-down enabled, GPO: pull-up to AVDD enabled
[2]	R	GPIO3_POL	GPIO polarity **Value** **Description** 0x0 GPIO is active-high 0x1 GPIO is active-low

Bit	Type	Field Name	Description
[1:0]	R	GPIO3_TRIG	GPI trigger type **Value** **Description** 0x0 Dual-edge triggered 0x1 Positive-edge triggered 0x2 Negative-edge triggered 0x3 Reserved (No trigger)

Table 39: SYS_GPIO4_0 (0x18)

Bit	Type	Field Name	Description
[4:1]	R	GPIO4_MODE	GPIO function mode select **Value** **Description** 0x0 GPIO disable 0x1 EN1 input 0x2 Reserved 0x3 EN1 input 0x4 DVC1 input 0x5 Reserved 0x6 DVC1 input 0x7 RELOAD input 0x8 PG1 output 0x9 Low output 0xA Low output 0xB PG1 output 0xC nIRQ output 0xD Reserved 0xE Low output 0xF High output
[0]	R	GPIO4_OBUF	GPIO output buffer select **Value** **Description** 0x0 open-drain output 0x1 push-pull output

Table 40: SYS_GPIO4_1 (0x19)

Bit	Type	Field Name	Description
[7]	R	GPIO4_DEB_FALL	GPI debounce falling edge
[6]	R	GPIO4_DEB_RISE	GPI debounce rising edge
[5:4]	R	GPIO4_DEB	GPI debounce time **Value** **Description** 0x0 100 µs debounce 0x1 1 ms debounce

Bit	Type	Field Name	Description
			0x2 10 ms debounce 0x3 100 ms debounce
[3]	R	GPIO4_PUPD	GPIO pull-up/pull-down enable **Value** **Description** 0x0 GPI: pull-down disabled, GPO: pull-up to AVDD disabled 0x1 GPI: pull-down enabled, GPO: pull-up to AVDD enabled
[2]	R	GPIO4_POL	GPIO polarity **Value** **Description** 0x0 GPIO is active-high 0x1 GPIO is active-low
[1:0]	R	GPIO4_TRIG	GPI trigger type **Value** **Description** 0x0 Dual-edge triggered 0x1 Positive-edge triggered 0x2 Negative-edge triggered 0x3 Reserved (No trigger)

Table 41: SYS_CFG_SLVADDR (0xA1)

Bit	Type	Symbol	Description
[6:0]	RW	I2C_SLAVE_ADDR	Slave address of the device.

7.2.2 Buck1

Table 42: BUCK_BUCK1_0 (0x20)

Bit	Type	Field Name	Description
[6:4]	RW	CH1_SR_DVC_DWN	Voltage slew-rate for DVC ramp-down **Value** **Description** 0x0 10 mV / 8 µs 0x1 10 mV / 4 µs 0x2 10 mV / 2 µs 0x3 10 mV / 1 µs 0x4 20 mV / 1 µs 0x5 Reserved 0x6 Reserved 0x7 Reserved
[3:1]	RW	CH1_SR_DVC_UP	Voltage slew-rate for DVC ramp-up **Value** **Description** 0x0 10 mV / 8 µs 0x1 10 mV / 4 µs 0x2 10 mV / 2 µs

Bit	Type	Field Name	Description
			0x3 10 mV / 1 µs 0x4 20 mV / 1 µs 0x5 40 mV / 1 µs 0x6 Reserved 0x7 Reserved
[0]	RW	CH1_EN	Channel enable. Write 0x1 to enable the buck. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)

Table 43: BUCK_BUCK1_1 (0x21)

Bit	Type	Field Name	Description
[6:4]	RW	CH1_SR_SHDN	Voltage slew-rate during shut-down **Value** **Description** 0x0 10 mV / 8 µs 0x1 10 mV / 4 µs 0x2 10 mV / 2 µs 0x3 10 mV / 1 µs 0x4 20 mV / 1 µs 0x5 Reserved 0x6 Reserved 0x7 Immediate power-down
[3:1]	RW	CH1_SR_STARTUP	Voltage slew-rate during start-up **Value** **Description** 0x0 10 mV / 8 µs 0x1 10 mV / 4 µs 0x2 10 mV / 2 µs 0x3 10 mV / 1 µs 0x4 20 mV / 1 µs 0x5 40 mV / 1 µs 0x6 Reserved 0x7 Reserved
[0]	RW	CH1_PD_DIS	LX Pull down while BUCK is off. Write 0x1 to disable this function.

Table 44: BUCK_BUCK1_2 (0x22)

Bit	Type	Field Name	Description
[3:0]	RW	CH1_ILIM	Select OCP threshold (A) **Value** **Description** 0x0 Reserved 0x1 6.5 0x2 7.5

Bit	Type	Field Name	Description
			0x3 8.5 0x4 9.5 0x5 10.5 0x6 11.5 0x7 12.5 0x8 13.5 0x9 14.5 0xA 15.5 0xB 16.5 0xC 17.5 0xD 18.5 0xE 19.5 0xF Disable

Table 45: BUCK_BUCK1_3 (0x23)

Bit	Type	Field Name	Description
[7:0]	R	CH1_VMAX	VOUT max setting (V): From 0.50 V (0x32) to 1.30 V (0x82) in steps of 10 mV This is a read-only register. **Value** **Description** 0x00 Reserved 0x31 Reserved 0x32 0.5 0x33 0.51 ... +0.01 steps 0x63 0.99 0x64 1 0x65 1.01 ... +0.01 steps 0x81 1.29 0x82 1.3 0x83 Reserved 0xFF Reserved

Table 46: BUCK_BUCK1_4 (0x24)

Bit	Type	Field Name	Description
[4]	RW	CH1_VSEL	Output voltage and operation selection: 0: A, 1: B. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)
[3:2]	RW	CH1_B_MODE	Operation mode selection. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)

Bit	Type	Field Name	Description
			Value **Description** 0x0 Force PFM operation 0x1 Force PWM operation (full phase) 0x2 Force PWM operation (with phase shedding) 0x3 Auto mode
[1:0]	RW	CH1_A_MODE	Operation mode selection. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) **Value** **Description** 0x0 Force PFM operation 0x1 Force PWM operation (full phase) 0x2 Force PWM operation (with phase shedding) 0x3 Auto mode

Table 47: BUCK_BUCK1_5 (0x25)

Bit	Type	Field Name	Description
[7:0]	RW	CH1_A_VOUT	Output voltage setting A: Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) From 0.50 V (0x32) to 1.30 V (0x82) in steps of 10 mV **Value** **Description** 0x00 Reserved 0x31 Reserved 0x32 0.5 0x33 0.51 ... +0.01 steps 0x63 0.99 0x64 1 0x65 1.01 ... +0.01 steps 0x81 1.29 0x82 1.3 0x83 Reserved 0xFF Reserved

Table 48: BUCK_BUCK1_6 (0x26)

Bit	Type	Field Name	Description
[7:0]	RW	CH1_B_VOUT	Output voltage setting B: Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) From 0.50 V (0x32) to 1.30 V (0x82) in steps of 10 mV **Value** **Description** 0x00 Reserved 0x31 Reserved

Bit	Type	Field Name	Description
			0x32 0.5 0x33 0.51 ... +0.01 steps 0x63 0.99 0x64 1 0x65 1.01 ... +0.01 steps 0x81 1.29 0x82 1.3 0x83 Reserved 0xFF Reserved

Table 49: BUCK_BUCK1_7 (0x27)

Bit	Type	Field Name	Description
[1:0]	RW	CH1_RIPPLE_CANCEL	Ripple cancel control **Value** **Description** 0x0 No ripple cancel 0x1 Small ripple cancel 0x2 Mid ripple cancel 0x3 Large ripple cancel

7.2.3 OTP Control

7.2.3.1 Serialization

Table 50: OTP_DEVICE_ID (0x48)

Bit	Type	Field Name	Description
[7:0]	R	DEV_ID	Device ID; hard-coded or metal-programmed

Table 51: OTP_VARIANT_ID (0x49)

Bit	Type	Field Name	Description
[7:4]	R	MRC	Mask Revision Code
[3:0]	R	VRC	Chip Variant Code; e.g. package variants.

Table 52: OTP_CUSTOMER_ID (0x4A)

Bit	Type	Field Name	Description
[7:0]	R	CUST_ID	Customer ID

Table 53: OTP_CONFIG_ID (0x4B)

Bit	Type	Field Name	Description
[7:0]	R	CONFIG_REV	OTP settings revision

8. Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 54.

For detailed information on MSL levels, refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The DA9141 package is qualified for MSL 3.

Table 54. MSL Classification

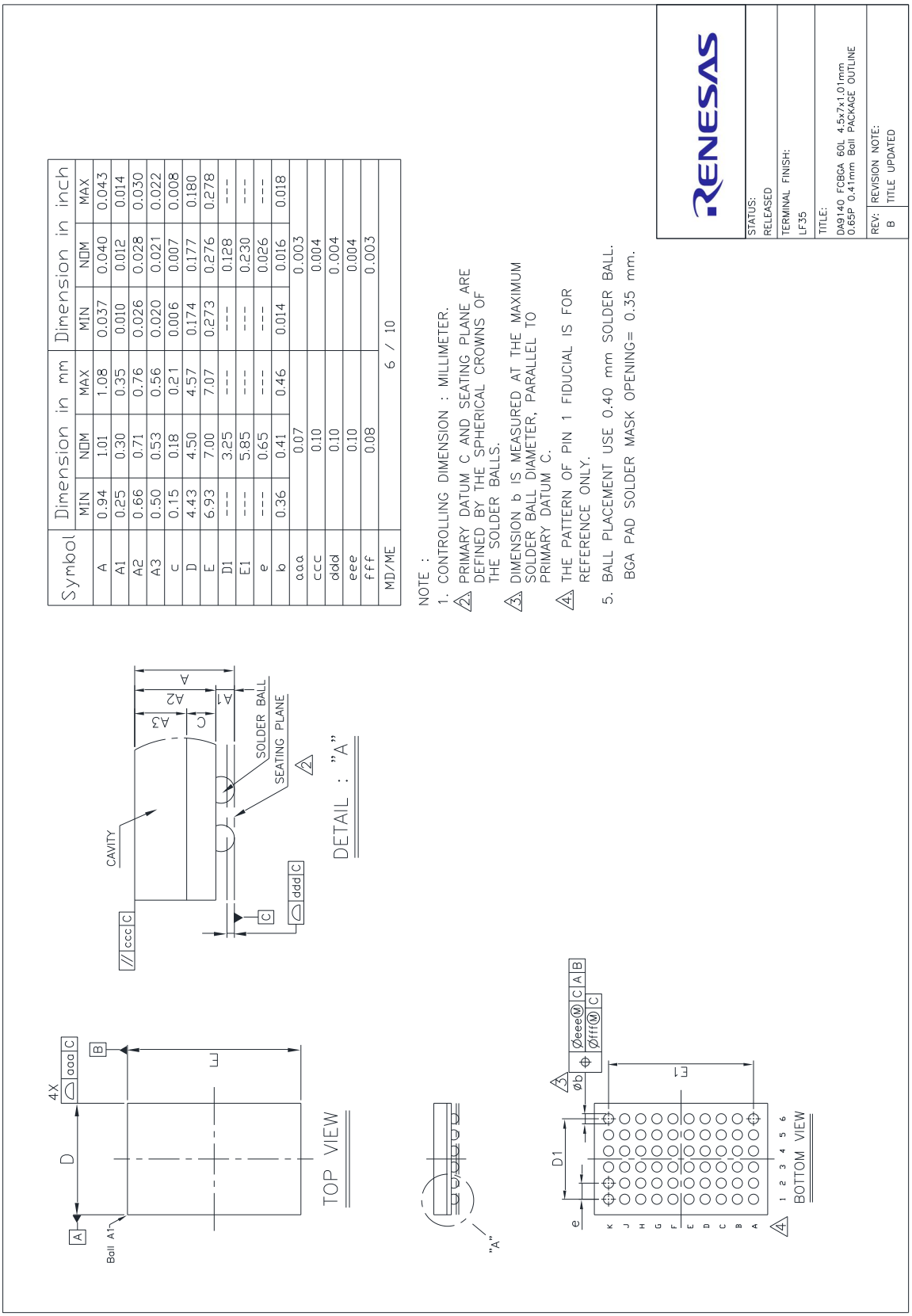
MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C/60% RH
MSL 3	168 hours	30 °C/60% RH
MSL 2A	4 weeks	30 °C/60% RH
MSL 2	1 year	30 °C/60% RH
MSL 1	Unlimited	30 °C/85% RH

8.1 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

9. Package Outline Drawings

9.1 Package Outline



9.2 Package Marking

Figure 12. Package Outline Drawing

Package Marking		
A1 Corner >	Marking Content	Format
1st		Pin 1 ID
2nd		
3rd		
4th		Part No./Option
5th		OTP
6th		Date Code
-A optionally indicate the Automotive test options.		
xx identifies the OTP Variant		
Date Code Format: yy = Year, ww = Week, zzzz = Traceability		

Figure 13. Chip Marking Details

10. Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas local sales representative.

Table 55. Ordering Information for Consumer/Industrial Applications

Part Number	Package Description	Size (mm)	Carrier Type	Pack Quantity
DA9141-xxF71	60 FCBGA	4.5 x 7 x 1.01 0.65 mm pitch	Tray	364
DA9141-xxF72	60 FCBGA	4.5 x 7 x 1.01 0.65 mm pitch	Reel	2600

Table 56. Ordering Information for Automotive Applications

Part Number	Package Description	Size (mm)	Carrier Type	Pack Quantity
DA9141-xxF71-A	60 FCBGA	4.5 x 7 x 1.01 0.65 mm pitch	Tray	364
DA9141-xxF72-A	60 FCBGA	4.5 x 7 x 1.01 0.65 mm pitch	Reel	2600

10.1 Variants Ordering Information

DA9141 supports delivery of variants indicated by xx in the part number above, where xx is replaced with the actual variant number. Please contact your Renesas local sales representative to discuss requirements.

11. Application Information

11.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account.

Table 57: Recommended Non-Automotive-Grade Capacitor Types

Application	Value (µF)	Size	Temp. Char. Note 1	Tol. (%)	V-Rate (V)	Type
VOUT output bypass	22	1206	X7R	±20	6.3	Murata GRM31CR70J226ME19L
	22	0805	X7T	±20	6.3	Murata GRM21BD70J226ME44L
PVDDx bypass	10	0805	X7S	±10	16	Murata GRM21BC71C106KE11L
	10	0603	X6S	±20	16	Murata GRM188C81C106MA73D
PVDDx bypass for VSYS < 4V	10	0603	X7T	±20	6.3	Murata GRM188D70J106MA73D
	10	0402	X6S	±20	6.3	Murata GRM155C80J106ME18D
AVDD bypass	1	0805	X7R	±10	50	Murata GRM21BR71H105KA12L
	1	0603	X7T	±10	50	Murata GRM188D71H105KE01D

Note 1 Select suitable Temperature Characteristics for the expected operating conditions.

Table 58: Recommended Automotive-Grade Capacitor Types

Application	Value (µF)	Size	Temp. Char.	Tol. (%)	V-Rate (V)	Type
VOUT output bypass	22	1206	X7R	±20	6.3	Murata GCM31CR70J226ME23L
PVDDx bypass	10	0805	X7S	±10	16	Murata GCM21BC71C106KE36L
PVDDx bypass for VSYS < 4V	10	0603	X7T	±20	6.3	Murata GCM188D70J106ME36L
AVDD bypass	1	0805	X7R	±10	50	Murata GCM21BR71H105KA03L

11.2 Inductor Selection

Inductors should be selected based on the following parameters:

- Rated maximum current and ISAT
  ISAT specifies the maximum current at which the inductance drops by 30% of the nominal value, and IMAX is defined by the maximum power dissipation and is applied to the effective current at 40 °C temperature rise.
- DC resistance
  Critical for the converter efficiency and should therefore be minimized.

Table 59: Recommended Inductor Types

Value (nH)	Size (mm)	I_{MAX} (DC) (A)	I_{SAT} (A)	Tol. (%)	DC Resistance (mΩ)	Type
112	3.2 x 2.5 x 2.5	20	31	20	1.9	TDK CLT3225AR11MI3
110	4.0 x 4.0 x 2.1	29	29	20	1.4	Coilcraft XGL4020-111MEC
100	5.3 x 5.1 x 3.0	18.3	37.1	20	2.7	TDK SPM5030VT-R10M-D

12. Layout Guidelines

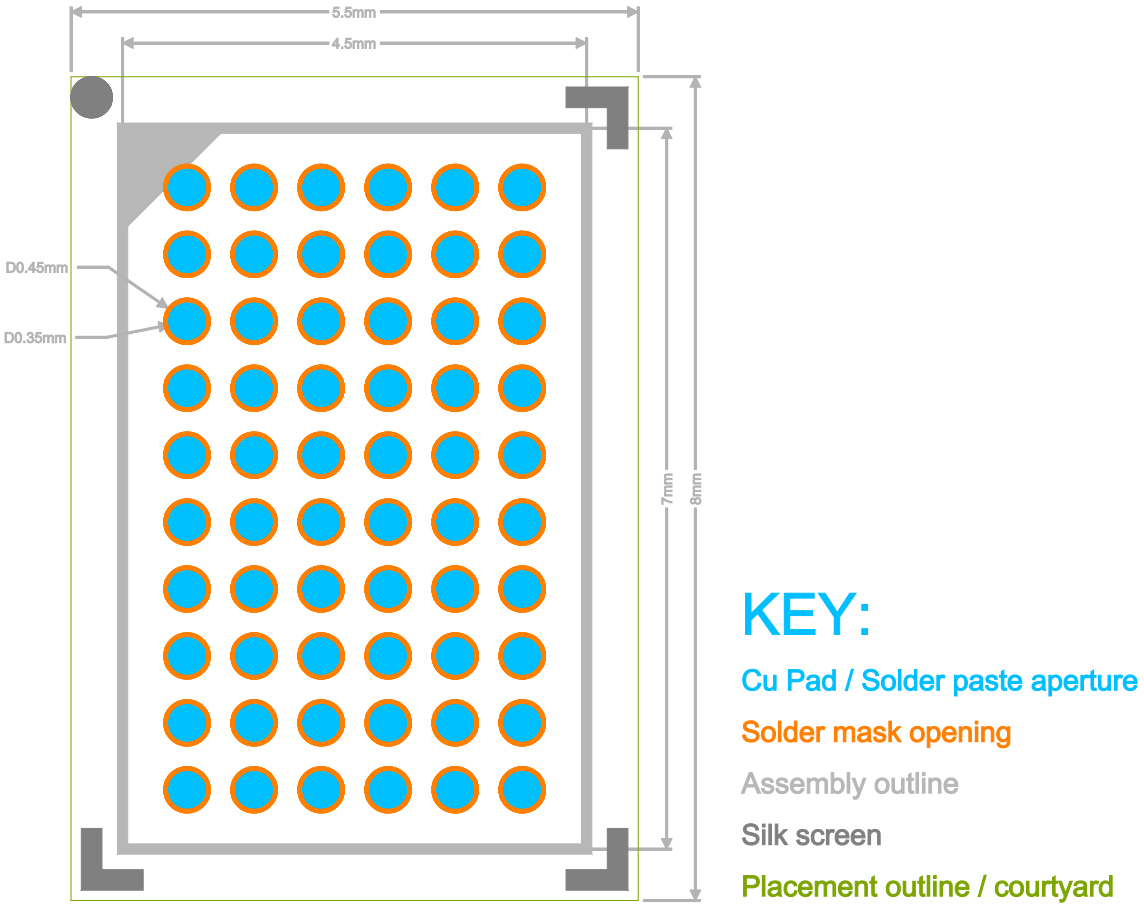


Figure 14. DA9141 Footprint

RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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