EL5411T

60MHz Rail-to-Rail Input-Output Operational Amplifier

FN6837
Rev 2.00
August 3, 2010

The EL5411T is a high voltage rail-to-rail input-output amplifier with low power consumption. The EL5411T contains four amplifiers. Each amplifier exhibits beyond the rail input capability, rail-to-rail output capability and is unity gain stable.

The maximum operating voltage range is from 4.5V to 19V. It can be configured for single or dual supply operation, and typically consumes only 3mA per amplifier. The EL5411T has an output short circuit capability of ±300mA and a continuous output current capability of ±70mA.

The EL5411T features a high slew rate of 100V/µs, and fast settling time. Also, the device provides common mode input capability beyond the supply rails, rail-to-rail output capability, and a bandwidth of 60MHz (-3dB). This enables the amplifiers to offer maximum dynamic range at any supply voltage. These features make the EL5411T an ideal amplifier solution for use in TFT-LCD panels as a V_{COM} driver or static gamma buffer, and in high speed filtering and signal conditioning applications. Other applications include battery power and portable devices, especially where low power consumption is important.

The EL5411T is available in a 14 Ld HTSSOP and a space saving thermally enhanced 16 Ld 4mmx4mm TQFN package. The device operates over an ambient temperature range of -40°C to +85°C.

Features

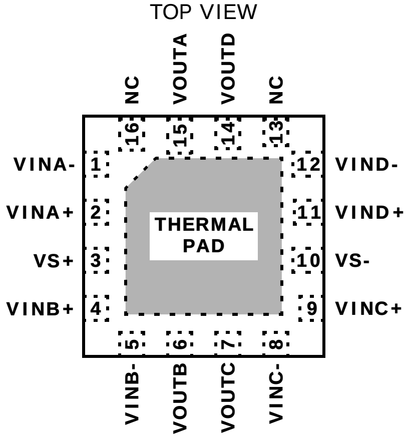
- 60MHz (-3dB) Bandwidth
- 4.5V to 19V Maximum Supply Voltage Range
- 100V/µs Slew Rate
- 3mA Supply Current (per Amplifier)
- ±70mA Continuous Output Current
- ±300mA Output Short Circuit Current
- Unity-gain Stable
- Beyond the Rails Input Capability
- Rail-to-rail Output Swing
- Built-in Thermal Protection
- -40°C to +85°C Ambient Temperature Range
- Pb-Free (RoHS Compliant)

Applications

- TFT-LCD Panels
- V_{COM} Amplifiers
- Static Gamma Buffers
- Drivers for A/D Converters
- Data Acquisition
- Video Processing
- Audio Processing
- Active Filters
- Test Equipment
- Battery-powered Applications
- Portable Equipment

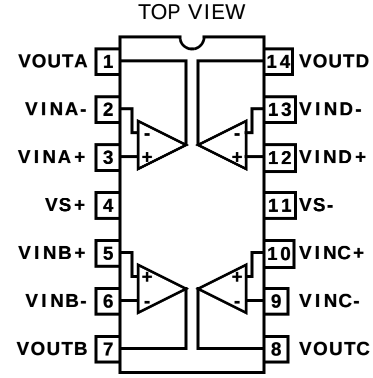
Pin Configurations

EL5411T
(16 LD 4X4 TQFN)
TOP VIEW



THERMAL PAD
CONNECTS TO VS-

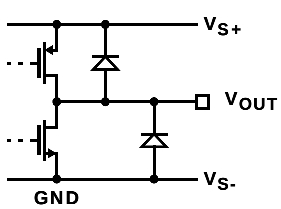
EL5411T
(14 LD HTSSOP)
TOP VIEW



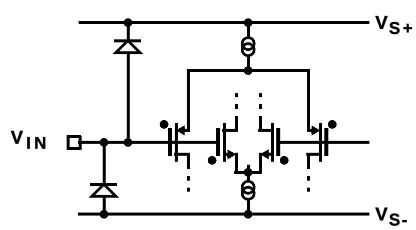
THERMAL PAD
CONNECTS TO VS-

Pin Descriptions

EL5411T (14 LD HTSSOP)	EL5411T (16 LD TQFN)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1	15	VOUTA	Amplifier A output	(Reference Circuit 1)
2	1	VINA-	Amplifier A inverting input	(Reference Circuit 2)
3	2	VINA+	Amplifier A non-inverting input	(Reference Circuit 2)
4	3	VS+	Positive power supply	
5	4	VINB+	Amplifier B non-inverting input	(Reference Circuit 2)
6	5	VINB-	Amplifier B inverting input	(Reference Circuit 2)
7	6	VOUTB	Amplifier B output	(Reference Circuit 1)
8	7	VOUTC	Amplifier C output	(Reference Circuit 1)
9	8	VINC-	Amplifier C inverting input	(Reference Circuit 2)
10	9	VINC+	Amplifier C non-inverting input	(Reference Circuit 2)
11	10	VS-	Negative power supply (connects to GND for single supply operation)	
12	11	VIND+	Amplifier D non-inverting input	(Reference Circuit 2)
13	12	VIND-	Amplifier D inverting input	(Reference Circuit 2)
14	14	VOUTD	Amplifier D output	(Reference Circuit 1)
	13, 16	NC	Not connected	
pad	pad	Thermal Pad	Functions as a heat sink. Connects to most negative potential, VS-	



CIRCUIT 1



CIRCUIT 2

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
EL5411TIREZ	5411TIRE Z	14 Ld HTSSOP	M14.173A
EL5411TILZ	5411TIL Z	16 Ld TQFN	L16.4x4F

NOTES:

1. Add “T7” or “T13” suffix for Tape and Reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for EL5411T. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- . . . . +19.8V
Input Voltage Range (V_{INx+}, V_{INx-}) . V_S- - 0.5V, V_S+ + 0.5V
Input Differential Voltage (V_{INx+} - V_{INx-}) . . . . (V_S+ + 0.5V)-(V_S- - 0.5V)
Maximum Continuous Output Current . . . . ±70mA
ESD Rating
Human Body Model 3000V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld HTSSOP (Notes 4, 5) . . .	38	8
16 Ld TQFN (Notes 4, 5)	40	8.5

Storage Temperature. . . . . -65°C to +150°C
Ambient Operating Temperature . . . . -40°C to +85°C
Maximum Junction Temperature . . . . +150°C
Power Dissipation . . . . See Figures 32 and 33
Pb-Free Reflow Profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_L = 1kΩ to 0V, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		3.5	17	mV
TCV_{OS}	Average Offset Voltage Drift (Note 6)	14 LD HTSSOP package		26		µV/°C
		16 LD TQFN package		4		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	60	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-5.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	For V_{IN} from -5.5V to 5.5V	50	73		dB
A_{VOL}	Open-Loop Gain	-4.5V ≤ V_{OUTx} ≤ 4.5V	62	78		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		-4.94	-4.85	V
V_{OH}	Output Swing High	I_L = +5mA	4.85	4.94		V
I_{SC}	Short-Circuit Current	V_{CM} = 0V, Source: V_{OUTx} short to V_S-, Sink: V_{OUTx} short to V_S+		±300		mA
I_{OUT}	Output Current			±70		mA
POWER SUPPLY PERFORMANCE						
(V_S+) - (V_S-)	Supply Voltage Range		4.5		19	V
I_S	Supply Current	V_{CM} = 0V, No load		11	15	mA
PSRR	Power Supply Rejection Ratio	Supply is moved from ±2.25V to ±9.5V	60	75		dB
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 7)	-4.0V ≤ V_{OUTx} ≤ 4.0V, 20% to 80%		100		V/µs
t_S	Settling to +0.1% (Note 8)	A_V = +1, V_{OUTx} = 2V step, R_L = 1kΩ ‖ 1kΩ (probe), C_L = 1.5pF		85		ns
BW	-3dB Bandwidth	R_F = 1kΩ, C_L = 1.5pF		60		MHz
GBWP	Gain-Bandwidth Product	A_V = -10, R_F = 1kΩ, R_G = 100Ω R_L = 1kΩ ‖ 1kΩ (probe), C_L = 1.5pF		32		MHz

Electrical Specifications $V_S+ = +5V$, $V_S- = -5V$, $R_L = 1k\Omega$ to 0V, $T_A = +25°C$, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
PM	Phase Margin	$A_V = -10$, $R_F = 1k\Omega$, $R_G = 100\Omega$ $R_L = 1k\Omega \| 1k\Omega$ (probe), $C_L = 1.5pF$		50		°
CS	Channel Separation	f = 5MHz		90		dB

Electrical Specifications $V_S+ = +5V$, $V_S- = 0V$, $R_L = 1k\Omega$ to 2.5V, $T_A = +25°C$, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 2.5V$		3.5	17	mV
TCV_{OS}	Average Offset Voltage Drift (Note 6)	14 LD HTSSOP package		23		µV/°C
		16 LD TQFN package		3		µV/°C
I_B	Input Bias Current	$V_{CM} = 2.5V$		2	60	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	For V_{IN} from -0.5V to 5.5V	45	68		dB
A_{VOL}	Open-Loop Gain	$0.5V \le V_{OUTx} \le 4.5V$	62	82		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -4.2mA$		60	150	mV
V_{OH}	Output Swing High	$I_L = +4.2mA$	4.85	4.94		V
I_{SC}	Short-circuit Current	$V_{CM} = 2.5V$, Source: V_{OUTx} short to V_S-, Sink: V_{OUTx} short to V_S+		±110		mA
I_{OUT}	Output Current			±70		mA
POWER SUPPLY PERFORMANCE						
$(V_S+) - (V_S-)$	Supply Voltage Range		4.5		19	V
I_S	Supply Current	$V_{CM} = 2.5V$, No load		12	15	mA
PSRR	Power Supply Rejection Ratio	Supply is moved from 4.5V to 19V	60	75		dB
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 7)	$1V \le V_{OUTx} \le 4V$, 20% to 80%		75		V/µs
t_S	Settling to +0.1% (Note 8)	$A_V = +1$, $V_{OUTx} = 2V$ step, $R_L = 1k\Omega \| 1k\Omega$ (probe), $C_L = 1.5pF$		90		ns
BW	-3dB Bandwidth	$R_F = 1k\Omega$, $C_L = 1.5pF$		60		MHz
GBWP	Gain-Bandwidth Product	$A_V = -10$, $R_F = 1k\Omega$, $R_G = 100\Omega$ $R_L = 1k\Omega \| 1k\Omega$ (probe), $C_L = 1.5pF$		32		MHz
PM	Phase Margin	$A_V = -10$, $R_F = 1k\Omega$, $R_G = 100\Omega$ $R_L = 1k\Omega \| 1k\Omega$ (probe), $C_L = 1.5pF$		50		°
CS	Channel Separation	f = 5MHz		90		dB

Electrical Specifications

$V_S+ = +18V$, $V_S- = 0V$, $R_L = 1k\Omega$ to 9V, $T_A = +25°C$, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 9V$		3.5	17	mV
TCV_{OS}	Average Offset Voltage Drift (Note 6)	14 LD HTSSOP package		21		µV/°C
		16 LD TQFN package		5		µV/°C
I_B	Input Bias Current	$V_{CM} = 9V$		2	60	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+18.5	V
CMRR	Common-Mode Rejection Ratio	For V_{IN} from -0.5V to 18.5V	53	75		dB
A_{VOL}	Open-Loop Gain	$0.5V \le V_{OUTx} \le 17.5V$	62	104		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -6mA$		80	150	mV
V_{OH}	Output Swing High	$I_L = +6mA$	17.85	17.92		V
I_{SC}	Short-circuit Current	$V_{CM} = 9V$, Source: V_{OUTx} short to V_S-, Sink: V_{OUTx} short to V_S+		±300		mA
I_{OUT}	Output Current			±70		mA
POWER SUPPLY PERFORMANCE						
$(V_S+) - (V_S-)$	Supply Voltage Range		4.5		19	V
I_S	Supply Current	$V_{CM} = 9V$, No load		12.3	15	mA
PSRR	Power Supply Rejection Ratio	Supply is moved from 4.5V to 19V	60	75		dB
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 7)	$1V \le V_{OUTx} \le 17V$, 20% to 80%		100		V/µs
t_S	Settling to +0.1% (Note 8)	$A_V = +1$, $V_{OUTx} = 2V$ step, $R_L = 1k\Omega \parallel 1k\Omega$ (probe), $C_L = 1.5pF$		100		ns
BW	-3dB Bandwidth	$R_F = 1k\Omega$, $C_L = 1.5pF$		60		MHz
GBWP	Gain-Bandwidth Product	$A_V = -10$, $R_F = 1k\Omega$, $R_G = 100\Omega$ $R_L = 1k\Omega \parallel 1k\Omega$ (probe), $C_L = 1.5pF$		32		MHz
PM	Phase Margin	$A_V = -10$, $R_F = 1k\Omega$, $R_G = 100\Omega$ $R_L = 1k\Omega \parallel 1k\Omega$ (probe), $C_L = 1.5pF$		50		°
CS	Channel Separation	f = 5MHz		90		dB

NOTES:

6. Measured over -40°C to +85°C ambient operating temperature range. See the typical TCV_{OS} production distribution shown in the “Typical Performance Curves” on page 6.
7. Typical slew rate is an average of the slew rates measured on the rising (20% to 80%) and the falling (80% to 20%) edges of the output signal.
8. Settling time measured as the time from when the output level crosses the final value on rising/falling edge to when the output level settles within a ±0.1% error band. The range of the error band is determined by: Final Value(V) ± [Full Scale(V) * 0.1%].

Typical Performance Curves

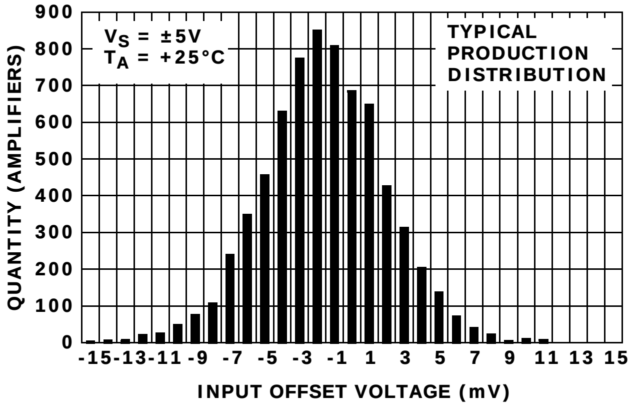


FIGURE 1. INPUT OFFSET VOLTAGE DISTRIBUTION

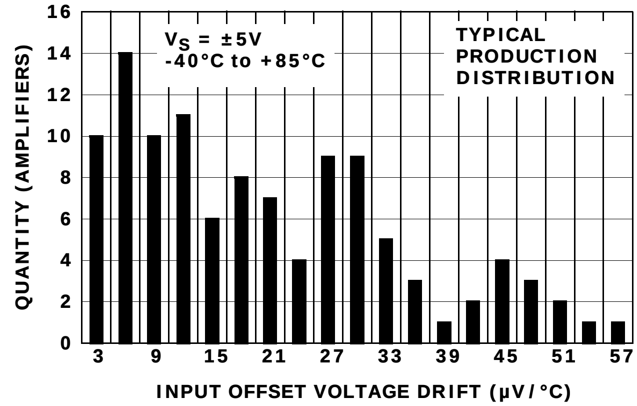


FIGURE 2. INPUT OFFSET VOLTAGE DRIFT (HTSSOP)

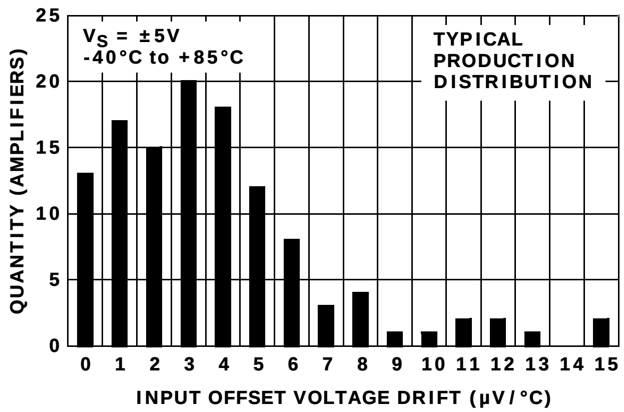


FIGURE 3. INPUT OFFSET VOLTAGE DRIFT (TQFN)

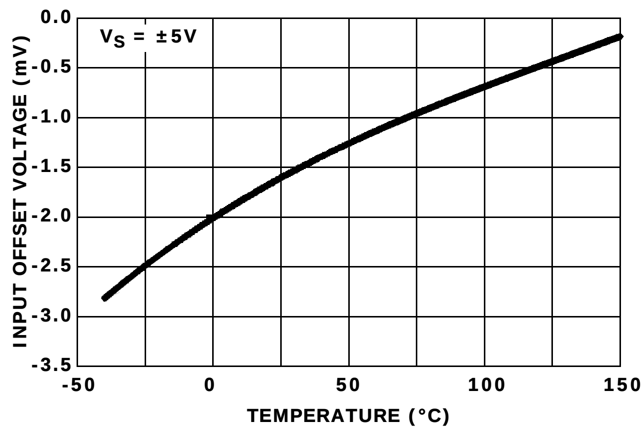


FIGURE 4. INPUT OFFSET VOLTAGE vs TEMPERATURE

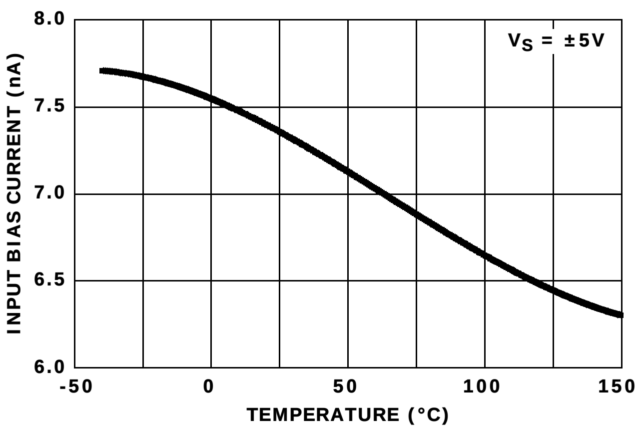


FIGURE 5. INPUT BIAS CURRENT vs TEMPERATURE

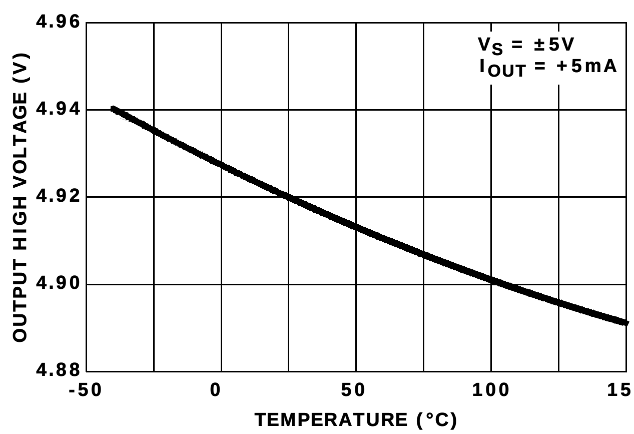


FIGURE 6. OUTPUT HIGH VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

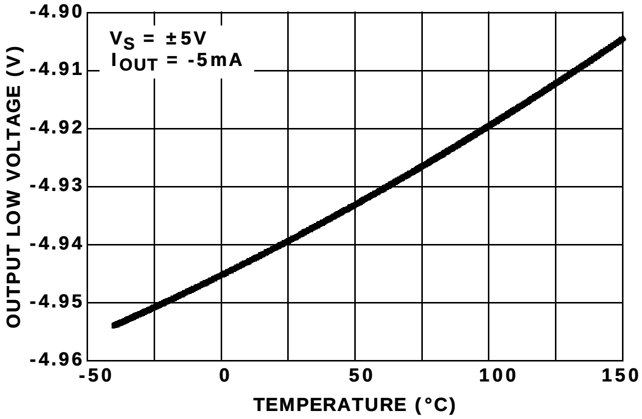


FIGURE 7. OUTPUT LOW VOLTAGE vs TEMPERATURE

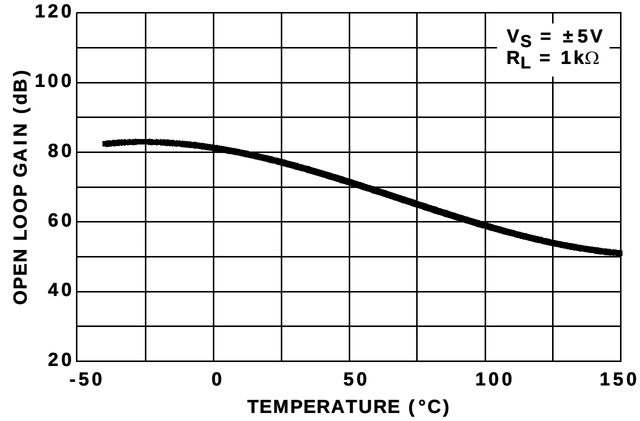


FIGURE 8. OPEN-LOOP GAIN vs TEMPERATURE

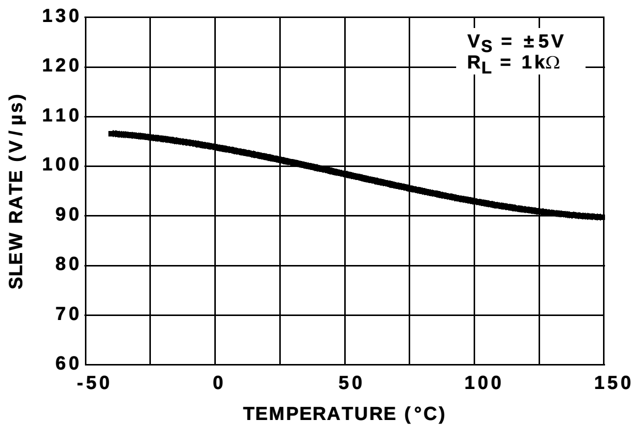


FIGURE 9. SLEW RATE vs TEMPERATURE

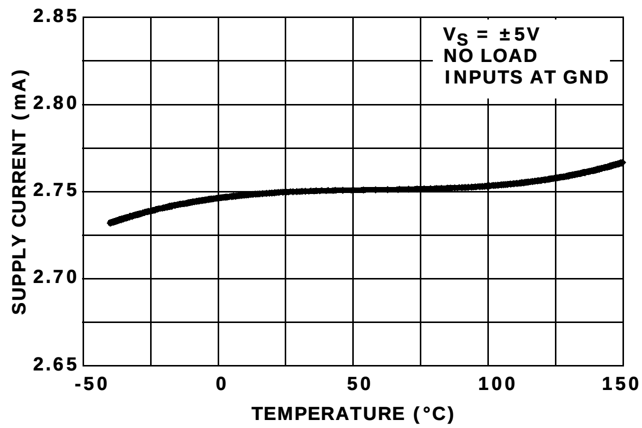


FIGURE 10. SUPPLY CURRENT PER AMPLIFIER vs TEMPERATURE

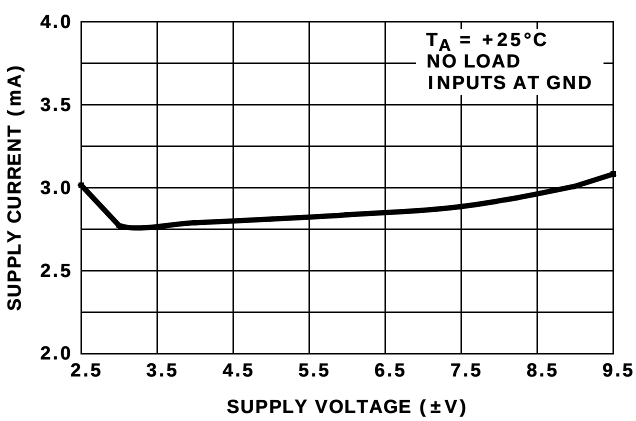


FIGURE 11. SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

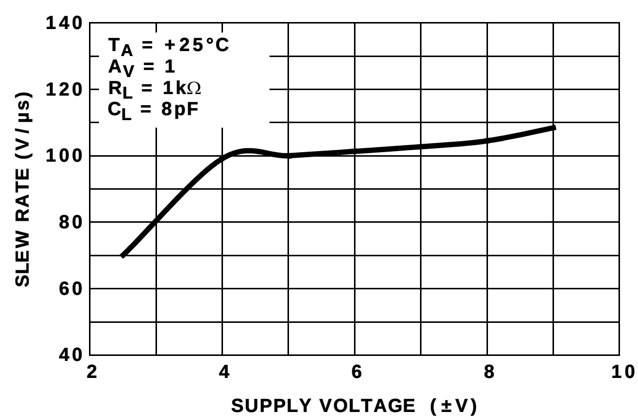


FIGURE 12. SLEW RATE vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

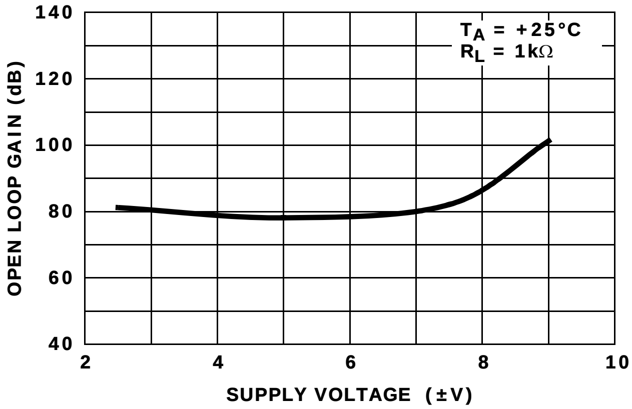


FIGURE 13. OPEN LOOP GAIN vs SUPPLY VOLTAGE

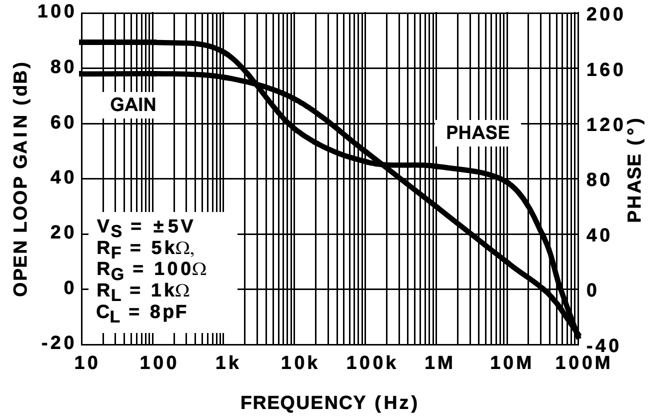


FIGURE 14. OPEN LOOP GAIN AND PHASE vs FREQUENCY

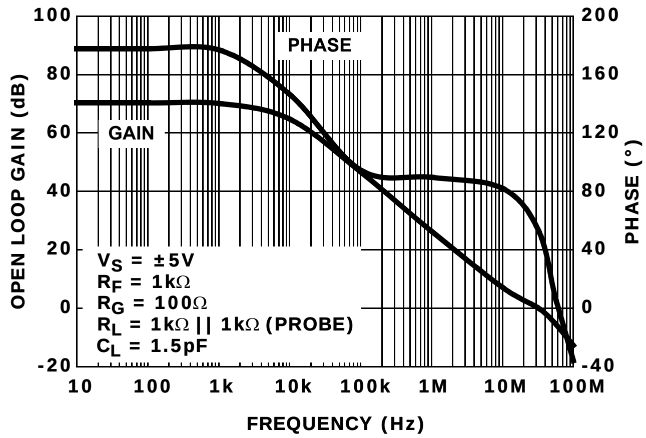


FIGURE 15. OPEN LOOP GAIN AND PHASE vs FREQUENCY

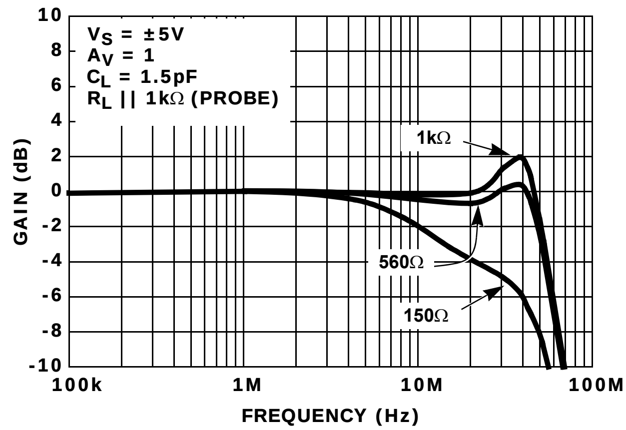


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS R_L

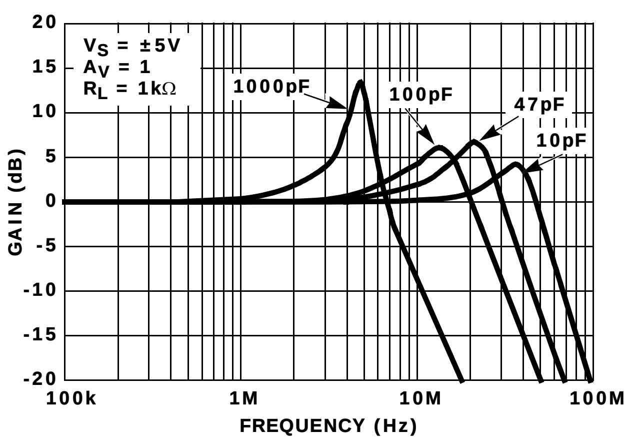


FIGURE 17. FREQUENCY RESPONSE FOR VARIOUS C_L

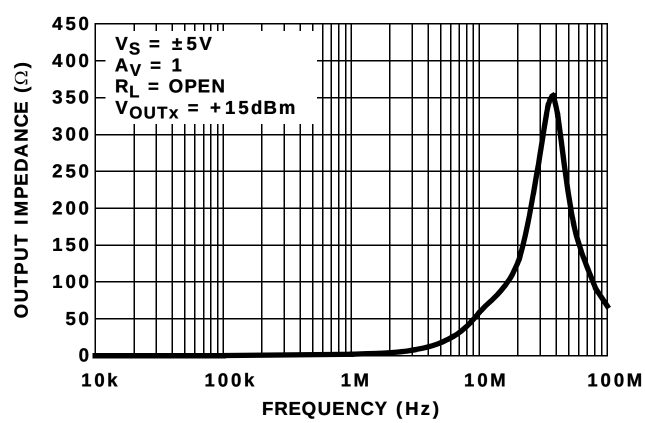


FIGURE 18. CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

Typical Performance Curves (Continued)

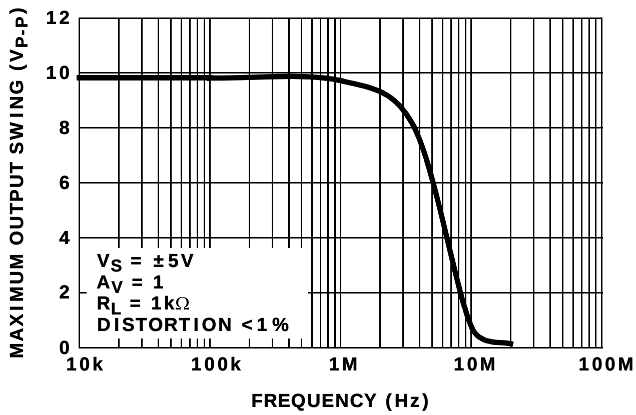


FIGURE 19. MAXIMUM OUTPUT SWING vs FREQUENCY

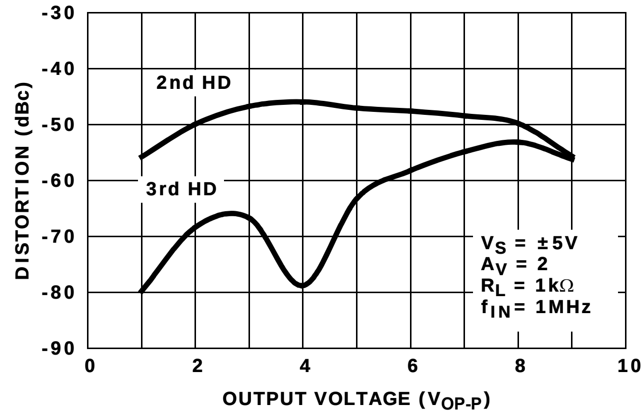


FIGURE 20. HARMONIC DISTORTION vs V_{OP-P}

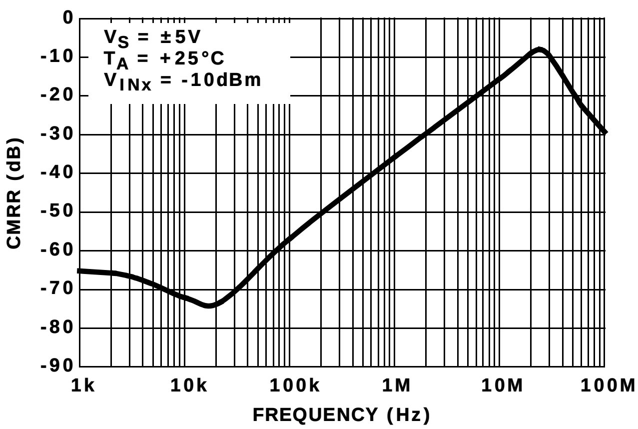


FIGURE 21. CMRR vs FREQUENCY

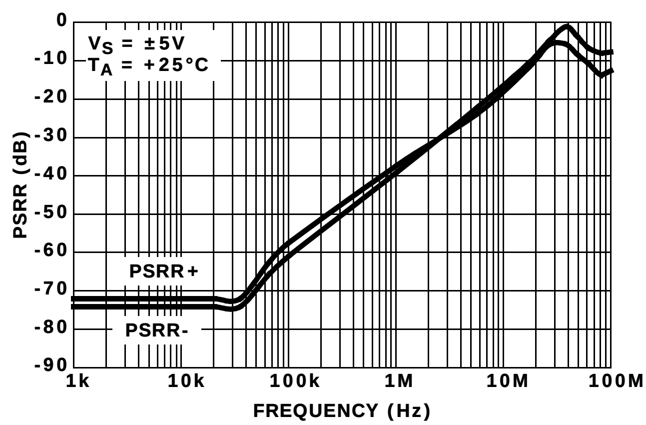


FIGURE 22. PSRR vs FREQUENCY

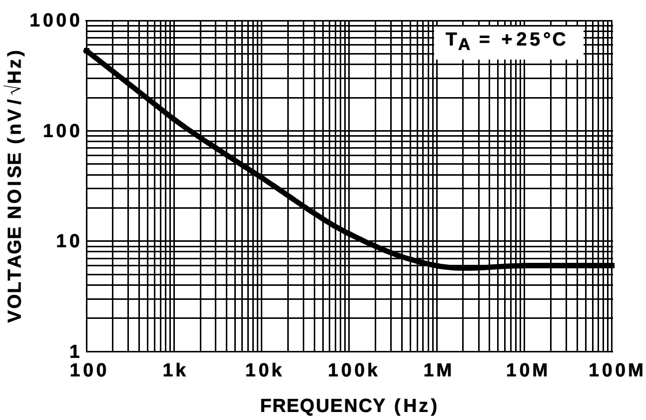


FIGURE 23. INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

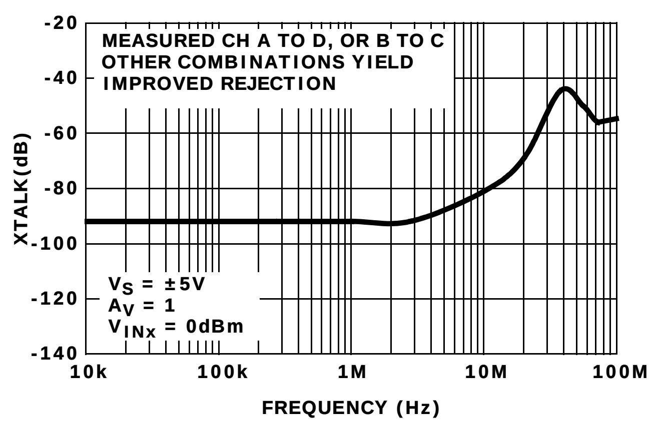


FIGURE 24. CHANNEL SEPARATION vs FREQUENCY

Typical Performance Curves (Continued)

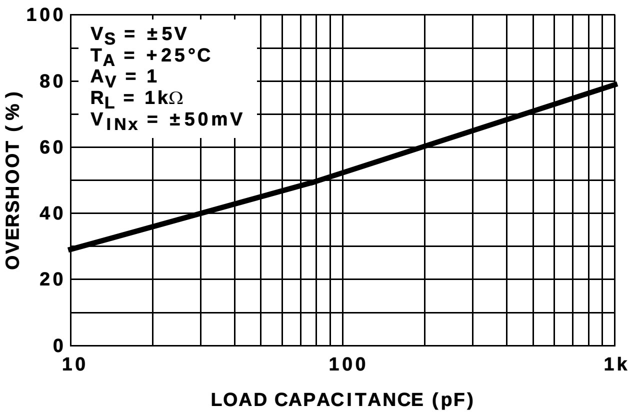


FIGURE 25. SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

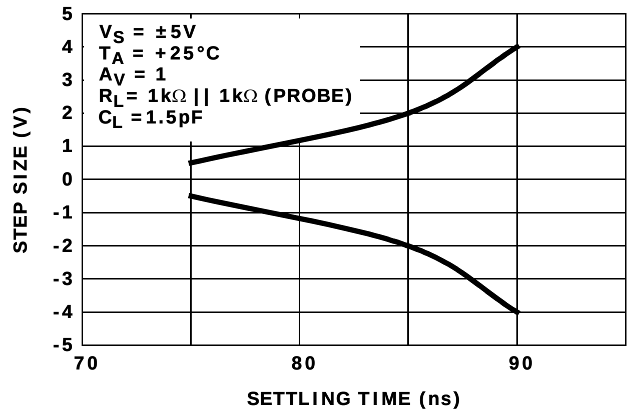


FIGURE 26. STEP SIZE vs SETTLING TIME

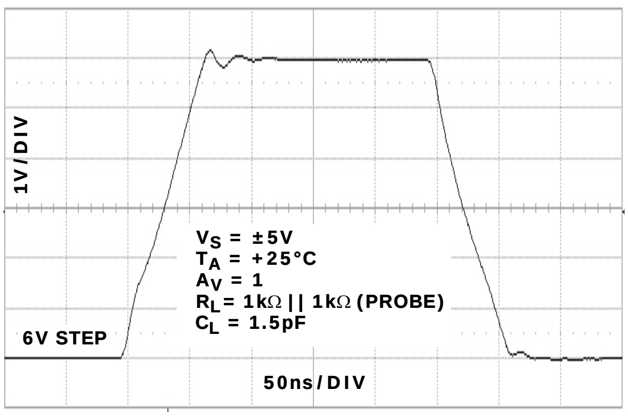


FIGURE 27. LARGE SIGNAL TRANSIENT RESPONSE

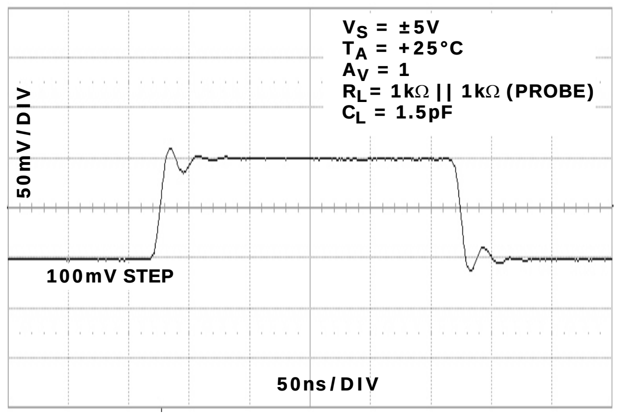


FIGURE 28. SMALL SIGNAL TRANSIENT RESPONSE

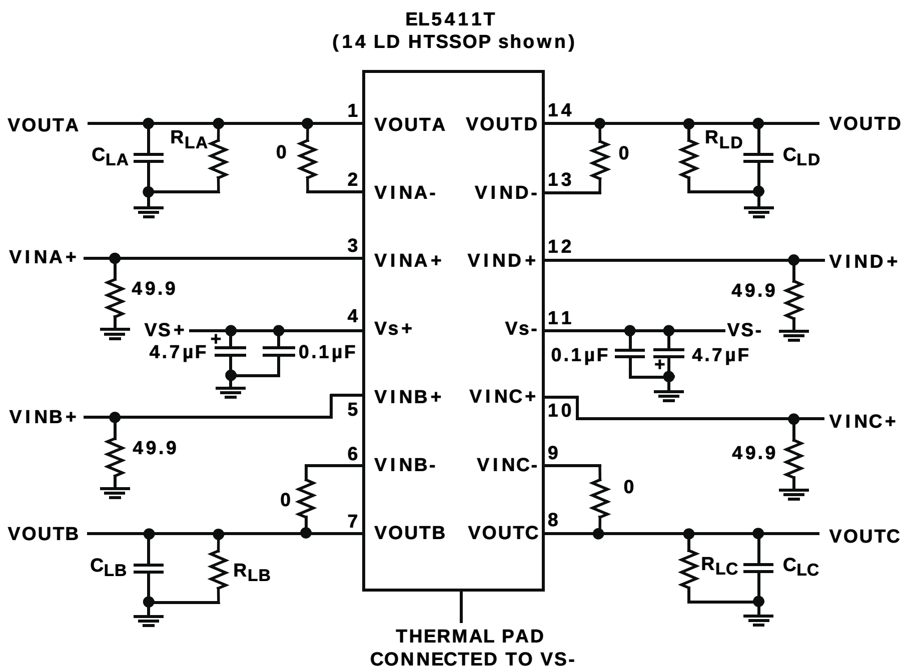


FIGURE 29. BASIC TEST CIRCUIT

Applications Information

Product Description

The EL5411T is a high voltage rail-to-rail input-output amplifier with low power consumption. The EL5411T contains four amplifiers. Each amplifier exhibits beyond the rail input capability, rail-to-rail output capability and is unity gain stable.

The EL5411T features a high slew rate of 100V/µs, and fast settling time. Also, the device provides common mode input capability beyond the supply rails, rail-to-rail output capability, and a bandwidth of 60MHz (-3dB). This enables the amplifiers to offer maximum dynamic range at any supply voltage.

Operating Voltage, Input and Output Capability

The EL5411T can operate on a single supply or dual supply configuration. The EL5411T operating voltage ranges from a minimum of 4.5V to a maximum of 19V. This range allows for a standard 5V (or ±2.5V) supply voltage to dip to -10%, or a standard 18V (or ±9V) to rise by +5.5% without affecting performance or reliability.

The input common-mode voltage range of the EL5411T extends 500mV beyond the supply rails. Also, the EL5411T is immune to phase reversal. However, if the common mode input voltage exceeds the supply voltage by more than 0.5V, electrostatic protection diodes in the input stage of the device begin to conduct. Even though phase reversal will not occur, to maintain optimal reliability it is suggested to avoid input overvoltage conditions. Figure 30 shows the input voltage driven 500mV beyond the supply rails and the device output swinging between the supply rails.

The EL5411T output typically swings to within 50mV of positive and negative supply rails with load currents of ±5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 31 shows the input and output waveforms for the device in a unity-gain configuration. Operation is from ±5V supply with a 1kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid and the output voltage is approximately $9.9V_{P-P}$.

Refer to the “Electrical Specifications” Table beginning on page 3 for specific device parameters. Parameter variations with operating voltage, loading and/or temperature are shown in the “Typical Performance Curves” on page 6.

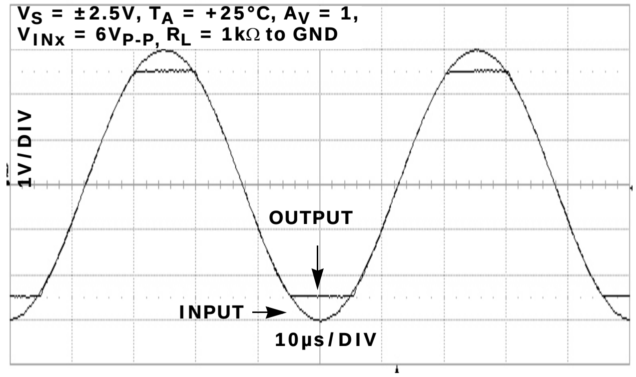


FIGURE 30. OPERATION WITH BEYOND-THE-RAILS INPUT

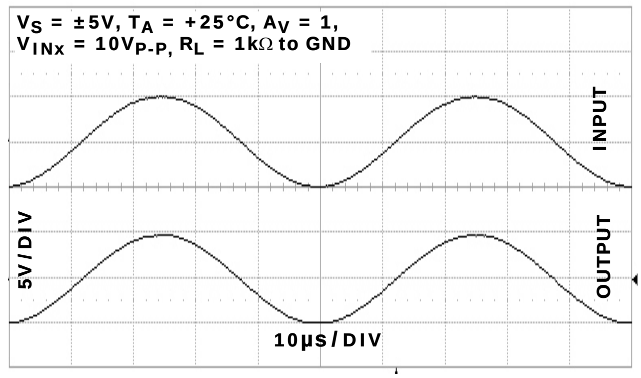


FIGURE 31. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

Output Current

The EL5411T is capable of output short circuit currents of 300mA (source and sink), and the device has built-in protection circuitry which limits the short circuit current to ±300mA (typical).

To maintain maximum reliability, the continuous output current should never exceed ±70mA. This ±70mA limit is determined by the characteristics of the internal metal interconnects. Also, see “Power Dissipation” on page 12 for detailed information on ensuring proper device operation and reliability for temperature and load conditions.

Unused Amplifiers

It is recommended that any unused amplifiers be configured as a unity gain follower. The inverting input should be directly connected to the output and the non-inverting input tied to the ground.

Driving Capacitive Loads

As load capacitance increases, the -3dB bandwidth will decrease and peaking can occur. Depending on the application, it may be necessary to reduce peaking and to improve device stability. To improve device stability a snubber circuit or a series resistor may be added to the output of the EL5411T.

A snubber is a shunt load consisting of a resistor in series with a capacitor. An optimized snubber can improve the phase margin and the stability of the EL5411T. The advantage of a snubber circuit is that it does not draw any DC load current or reduce the gain.

Another method to reduce peaking is to add a series output resistor (typically between 1Ω to 10Ω). Depending on the capacitive loading, a small value resistor may be the most appropriate choice to minimize any reduction in gain.

Power Dissipation

With the high-output drive capability of the EL5411T amplifiers, it is possible to exceed the +150°C absolute maximum junction temperature under certain load current conditions. It is important to calculate the maximum power dissipation of the EL5411T in the application. Proper load conditions will ensure that the EL5411T junction temperature stays within a safe operating region.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad \text{(EQ. 1)}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- Θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation allowed

The total power dissipation produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power dissipation in the IC due to the loads, or:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_S + - V_{OUT}i) \times I_{LOAD}i] \quad \text{(EQ. 2)}$$

when sourcing, and:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_{OUT}i - V_S -) \times I_{LOAD}i] \quad \text{(EQ. 3)}$$

when sinking,

where:

- i = 1 to 4

  (1, 2, 3, 4 corresponds to Channel A, B, C, D respectively)
- V_S = Total supply voltage (V_S+ - V_S-)
- V_S+ = Positive supply voltage
- V_S- = Negative supply voltage
- I_{SMAX} = Maximum supply current per amplifier

  (I_{SMAX} = EL5411T quiescent current ÷ 4)
- V_{OUT} = Output voltage
- I_{LOAD} = Load current

Device overheating can be avoided by calculating the minimum resistive load condition, R_{LOAD}, resulting in the highest power dissipation. To find R_{LOAD} set the two P_{DMAX} equations equal to each other and solve for V_{OUT}/I_{LOAD}. Reference the package power dissipation curves, Figures 32 and 33, for further information.

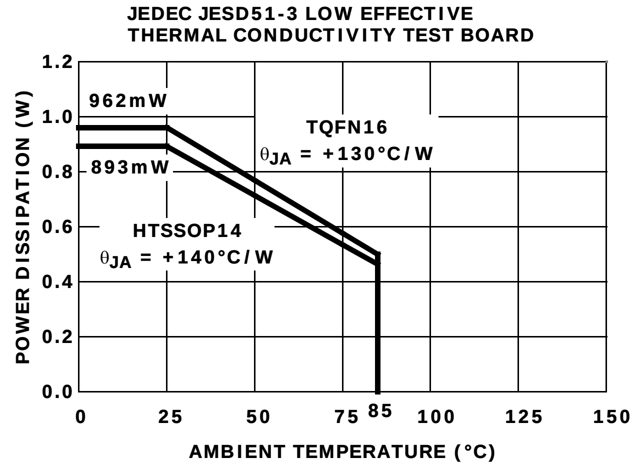


FIGURE 32. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

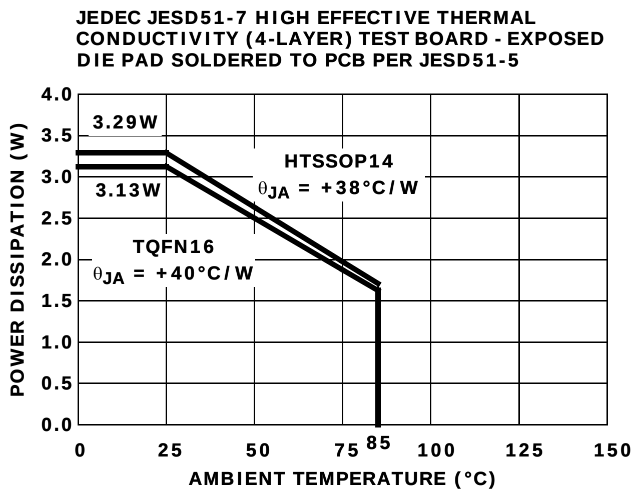


FIGURE 33. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Thermal Shutdown

The EL5411T has a built-in thermal protection which ensures safe operation and prevents internal damage to the device due to overheating. When the die temperature reaches +165°C (typical) the device automatically shuts OFF the outputs by putting them in a high impedance state. When the die cools by +15°C (typical) the device automatically turns ON the outputs by putting them in a low impedance (normal) operating state.

Power Supply Bypassing and Printed Circuit Board Layout

The EL5411T can provide gain at high frequency, so good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, trace lengths should be as short as possible and the power supply pins must be well bypassed to reduce any risk of oscillation.

For normal single supply operation (the V_S- pin is connected to ground) a 4.7µF capacitor should be placed from V_S+ to ground, then a parallel 0.1µF capacitor should be connected as close to the amplifier as possible. One 4.7µF capacitor may be used for multiple devices. For dual supply operation the same capacitor combination should be placed at each supply pin to ground.

It is highly recommended that EL5411T exposed thermal pad packages should always have the pad connected to the lowest potential, V_S-, to optimize thermal and operating performance. PCB vias should be placed below the device’s exposed thermal pad to transfer heat to the V_S- plane and away from the device.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
8/3/10	FN6837.2	Converted to New Intersil Data Sheet Template. Changed Theta JC for 16 Ld TQFN in "Thermal Information" on page 3 from "9" to "8.5" Corrected Theta JA Note 4 from "θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board." to "θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features." Numbered notes in "Ordering Information" on page 2 and added MSL Note 3. Moved "Ordering Information" from page 1 to page 2 and "Pin Configurations" from page 2 to page 1. Moved "Pin Descriptions" from page 11 to page 2. Added "Products" on page 14. Updated "Package Outline Drawing" on page 15 (M14.173A). Added land pad for exposed die attach pad.
10/8/09	FN6837.1	Updated Ordering Information by removing "contact factory for availability". add "vs FREQUENCY" to the plot titles in Fig 14,15,18,21,22,23,24: Fig 21: changed y-axis label to read "CMRR (dB)" Fig 22: changed y-axis label to read "PSRR (dB)" Fig 26: changed label to read "STEP SIZE vs SETTLING TIME" Changed 1st sentence in pages 1 and 12 from "The EL5411T is a low power, high voltage rail-to-rail input-output amplifier" to "The EL5411T is a high voltage rail-to-rail input-output amplifier with low power consumption". Updated package outline drawing M14.173A to add land pattern and move dimensions from table onto drawing
8/21/09	FN6837.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: EL5411T

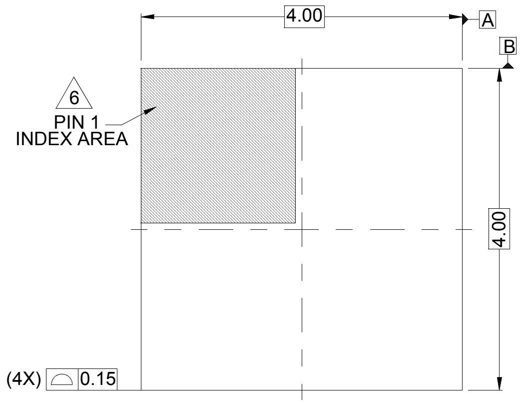
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

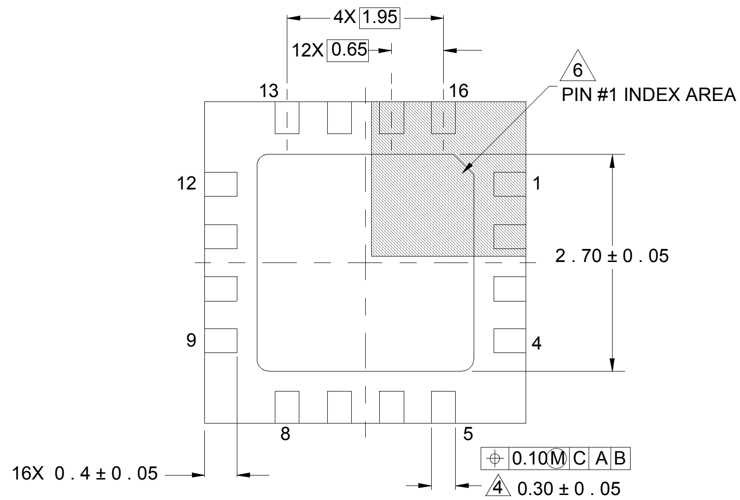
Package Outline Drawing

L16.4x4F

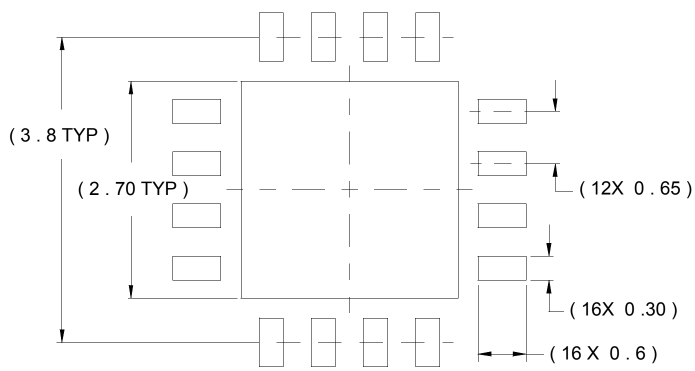
16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 04/09



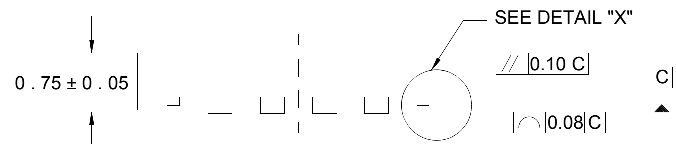
TOP VIEW



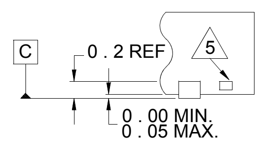
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

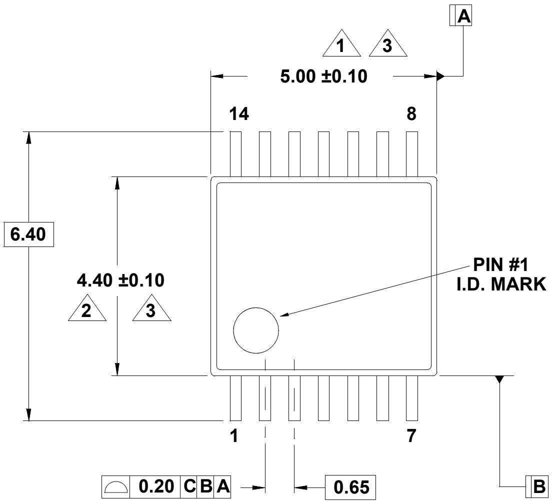
NOTES:

1. **Dimensions are in millimeters.**
   Dimensions in ( ) for Reference Only.
2. **Dimensioning and tolerancing conform to AMSE Y14.5m-1994.**
3. **Unless otherwise specified, tolerance : Decimal ± 0.05**
4. **Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.**
5. **Tiebar shown (if present) is a non-functional feature.**
6. **The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.**

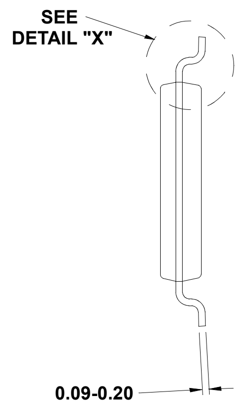
Package Outline Drawing

M14.173A

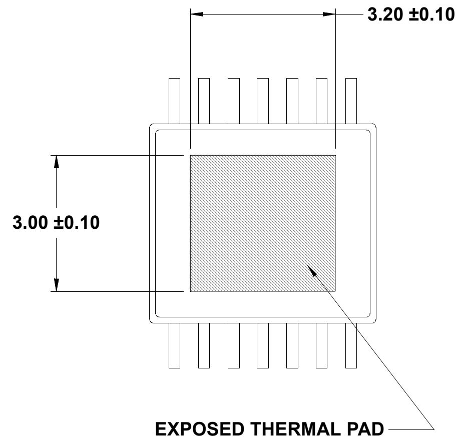
14 LEAD HEAT-SINK THIN SHRINK SMALL OUTLINE PACKAGE (HTSSOP)
Rev 2, 10/09



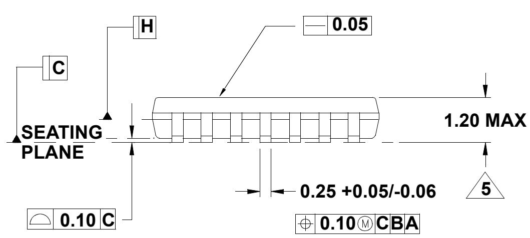
TOP VIEW



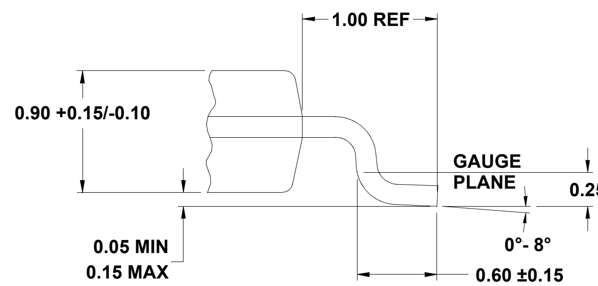
END VIEW



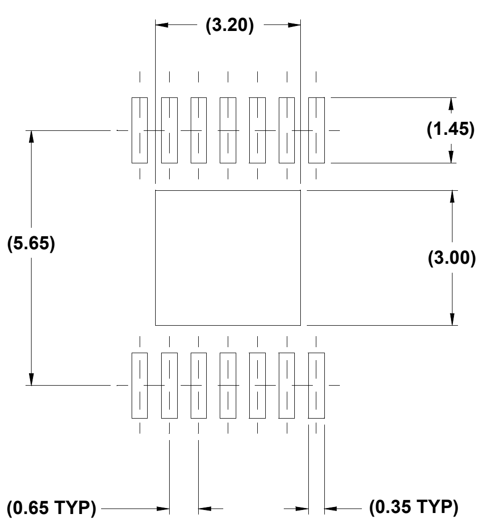
BOTTOM VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.