F0448

Dual Matched Broadband RF DVGA 3.3GHz to 4.2GHz

The F0448 is a 3.3GHz to 4.2GHz dual RF digital variable gain amplifier (DVGA) designed for use in receivers.

This dual RF DVGA provides two independent receiver channels each with 13dB typical maximum gain and 6dB noise figure designed to operate with a single +5V supply. For each channel, gain control is split into three separate attenuators: DSA0, a single 6dB step using a single control pin; DSA1, a 23dB SPI-controlled gain adjustment in 1dB steps; and DSA2, includes 18dB attenuation in 6dB steps controlled using two control pins. The F0448 offers +37dBm nominal output IP3 using 220mA total ICC.

This device is packaged in a 6 × 6 mm, 36-QFN with 50Ω single-ended RF input and RF output impedances for ease of integration into the signal-channel lineup for each of the two channels.

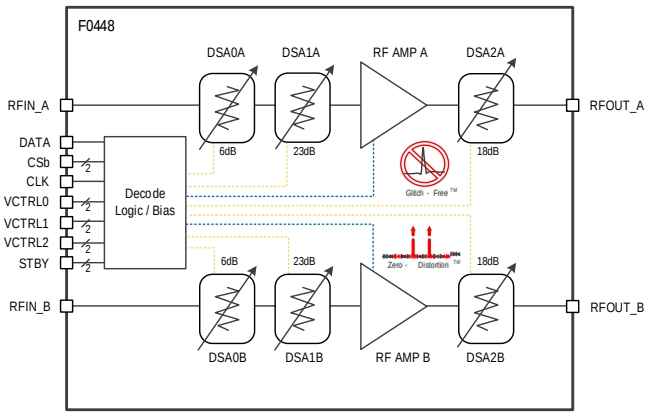

Figure 1. Block Diagram

Features

- RF Frequency Range: 3.3GHz to 4.2GHz
- Dual Channel RF amp and DSAs for Diversity / MIMO Receivers
- < 2dB overshoot between DSA transitions
- 13dB typical maximum gain at 3.6GHz
- DSA0: Single 6dB coarse step
- DSA1: 23dB total gain range in 1dB steps
- DSA2: 18dB gain range in 6dB steps
- +37dBm OIP3 at 3.6GHz
- 6dB Noise figure at 3.6GHz
- +5V Supply voltage
- I_{CC} = 220mA
- Independent standby: 7mA standby current
- SPI interface for DSA1
- 1-bit control for DSA0
- 2-bit control for DSA2
- 50Ω input and output impedance
- Internally matched
- Temperature range: -40°C to +105°C
- 6 × 6 × 0.75 mm, 36-QFN package

Applications

- Multi-mode, Multi-carrier Receivers
- PHS/PAS Base Stations
- Distributed Antenna Systems
- Digital Radio

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1. Pin Information

1.1 Pin Assignments

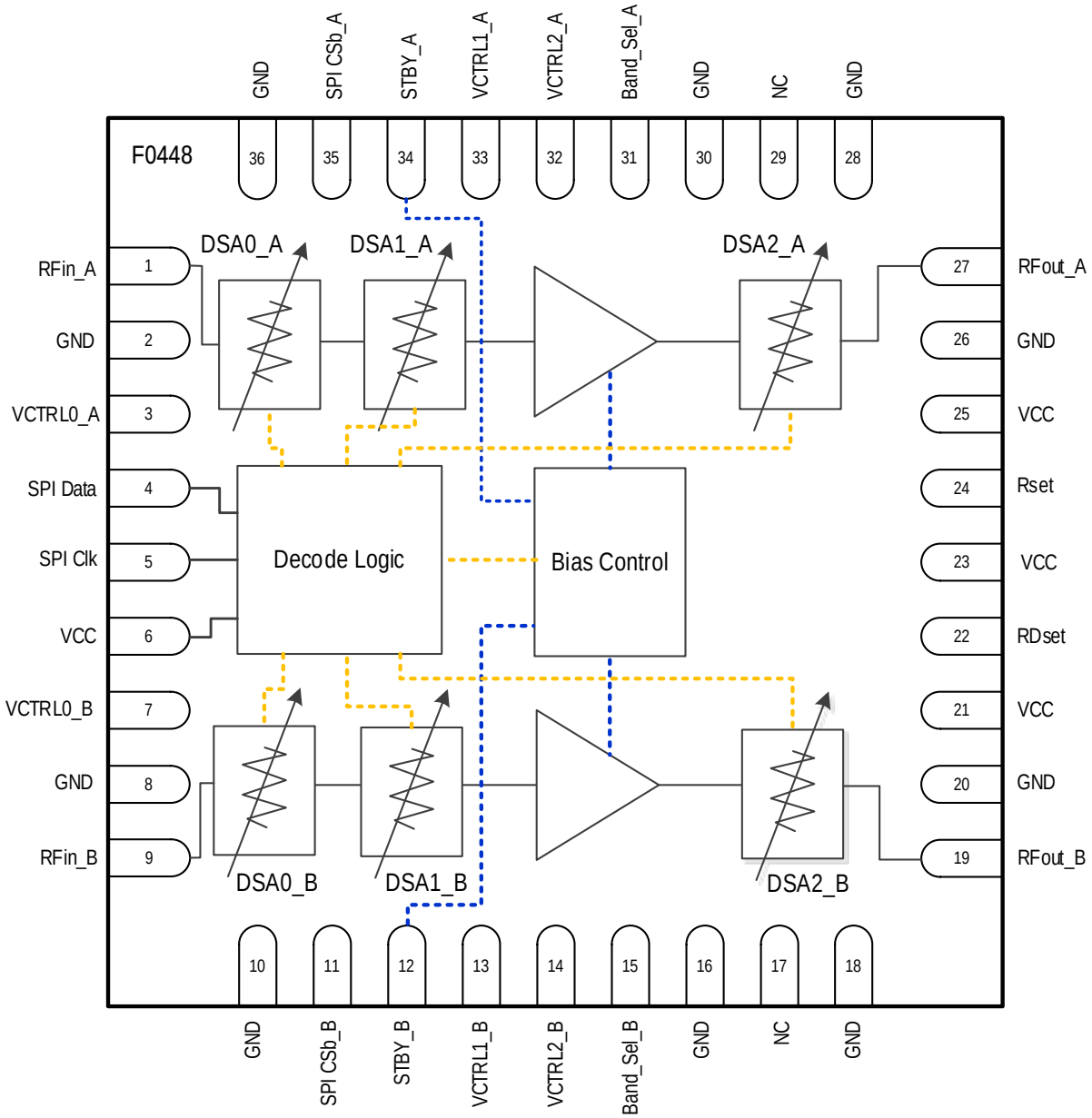


Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Number	Name	Description
1	RFIN_A	Input RF port for channel A which is internally matched to 50Ω. Must use external DC block.
2, 8, 15, 16, 17, 29, 30, 31	GND	Internally grounded. This pin must be grounded with a via as close to the pin as possible.

Number	Name	Description
3	VCTRL0_A	1-bit DSA0 6dB attenuator control for channel A. Logic HIGH is for 6dB attenuated and logic LOW is for 0dB attenuated.
4	DATA	Data input: 3.3V or 1.8V CMOS compatible.
5	CLK	Clock input: 3.3V or 1.8V CMOS compatible.
6, 21, 23, 25	V_{CC}	Power Supply. Use bypass capacitors as close to pin as possible.
7	VCTRL0_B	1-bit DSA0 6dB attenuator control for channel B. Logic HIGH is for 6dB attenuated and logic LOW is for 0dB attenuated.
9	RFIN_B	Input RF port for channel B that is internally matched to 50Ω. Must use external DC block.
10, 18, 20, 26, 28, 36	NC	No internal connection. These pins can be left unconnected or be connected to ground (recommended). Use a via as close to the pin as possible if grounded.
11	CSb_B	Chip Select bar input for channel B: 3.3V or 1.8V CMOS compatible. Logic LOW allows data to be shifted in.
12	STBY_B	Standby pin for channel B (LOW/Open = device power ON, HIGH = device power OFF with SPI still powered ON). An internal pull-down resistor of 57kΩ connects between this pin and GND.
13	VCTRL1_B	Bit 0 for DSA2 channel B attenuator. Logic HIGH is for 6dB attenuated and logic LOW is for 0dB attenuated.
14	VCTRL2_B	Bit 1 for DSA2 channel B attenuator. Logic HIGH is for 12dB attenuated and logic LOW is for 0dB attenuated.
19	RFOUT_B	Output RF port for channel B. Use external DC block as close to the pin as possible.
22	RDSET	Connect external resistor to GND to optimize amplifier bias. Used with pin 24.
24	RSET	Connect external resistor to GND to optimize amplifier bias. Used with pin 22.
27	RFOUT_A	Output RF port for channel A. Use external DC block as close to the pin as possible.
32	VCTRL2_A	Bit 1 for DSA2 channel A attenuator. Logic HIGH is for 12dB attenuated and logic LOW is for 0dB attenuated.
33	VCTRL1_A	Bit 0 for DSA2 channel A attenuator. Logic HIGH is for 6dB attenuated and logic LOW is for 0dB attenuated.
34	STBY_A	Standby pin for channel A (LOW/Open = device power ON, HIGH = device power OFF with SPI still powered ON). An internal pull-down resistor of 57kΩ connects between this pin and GND.
35	CSb_A	Chip Select bar input for channel A: 3.3V or 1.8V CMOS compatible. Logic LOW allows data to be shifted in.
	— EPAD	Exposed paddle. Internally connected to ground. Solder this exposed paddle to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

2. Specifications

2.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F0448 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
V_{CC} to GND	V_{CC}	-0.3	+5.5	V
DATA, CSb_A, CSb_B, CLK, VCTRL0_A, VCTRL0_B	V_{LOGIC1}	-0.3	Lower of (V_{CC}, 3.6)	V
STBY_A, STBY_B, VCTRL1_A, VCTRL1_B, VCTRL2_A, VCTRL2_B	V_{LOGIC2}	-0.3	V_{CC} + 0.25	V
RFIN_A, RFIN_B externally applied DC voltage	V_{RFIN}	+1.4	+3.6	V
RFOUT_A, RFOUT_B, externally applied DC voltage	V_{RFOUT}	+1.4	+3.6	V
RF Input Power (RFIN_A or RFIN_B) applied for 24 hours max. [1]	P_{MAX}		+22	dBm
Continuous Power Dissipation	P_{DISS}		1.5	W
Storage Temperature Range	T_{ST}	-65	150	°C
Lead Temperature (soldering, 10s)			260	°C
ElectroStatic Discharge – HBM (JEDEC/ESDA JS-001-2012)			2000 Class 2	V
ElectroStatic Discharge – CDM (JEDEC 22-C101F)			1000 Class C3	V

1. Exposure to these maximum RF levels can result in significant V_{CC} current draw due to overdriving the amplifier stage.

2.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Supply Voltage	V_{CC}	All V_{CC} pins	4.75	5.00	5.25	V
Operating Temperature Range	T_{EPAD}	Exposed paddle	-40		+105	°C
Junction Temperature	T_J				+125	°C
RF Frequency Range	f_{RF}		3.3		4.2	GHz
Maximum RF Input Power	P_{IP}	DSA0 = DSA1 = 0dB			0	dBm
RF Source Impedance	Z_{RFI}	Single ended		50		Ω
RF Load Impedance	Z_{RFO}	Single ended		50		Ω

2.3 Electrical Characteristics (3.4GHz to 3.8GHz)

See F0448 Typical Application Circuit. V_{CC} = +5V, T_C = +25°C, f_{RF} = 3.6GHz specifications apply when operated as a dual-channel RF DVGA, maximum gain setting, P_{OUT} = 0dBm, $Z_{RFI} = Z_{RFO}$ = 50Ω, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated. For BOM details of this specific band, see Table 11.

Table 3. Electrical Characteristics (3.4GHz to 3.8GHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Input High	V_{IH}	Applies for all logic levels.	1.07 [1]			V
Logic Input Low	V_{IL}	Applies for all logic levels.			0.63	V
Logic Current (CLK, DATA, CSb_A, CSb_B, VCTRL0_A, VCTRL1_A, VCTRL2_A, VCTRL0_B, VCTRL1_B, VCTRL2_B)	I_{IH}, I_{IL}		-5		5	µA
Logic Current for Standby (STBY_A, STBY_B) [2]	I_{IH-SB}, I_{IL-SB}	5V logic	-5		127	µA
		3.3V logic	-5		87	
		1.8V logic	-5		47	
Supply Current	I_{CC_2}	Both channels on		220	***270***	mA
	I_{CC_1}	One channel on		110	***142***	
	I_{CC_STBY}	Standby Mode		7	***14***	
Startup Time	t_{START}	50% of STBY going LOW to Gain within ± 1dB with no attenuation.		74		ns
DSA0 Adjustment Range	A_{ADJ0}	6dB step size		6		dB
DSA1 Adjustment Range	A_{ADJ1}	1dB step size		23		dB
DSA2 Adjustment Range	A_{ADJ2}	6dB step size		18		dB
Maximum Attenuation Glitch	$ATTN_G$			2		dB
DSA0 Gain Settling Time	t_{DSA0_1}	50% CTRL to within 0.1dB final value, 0dB state to 6dB state		24	35	ns
	t_{DSA0_2}	50% CTRL to within 0.1dB final value, 6dB state to 0dB state		18	35	
DSA1 Gain Settling Time	t_{DSA1}	50% of CSb to within 0.1dB final value		300		ns
DSA2 Gain Settling Time	t_{DSA2_1}	50% CTRL to within 0.1dB final value, 0dB state to 18dB state		16	35	ns
	t_{DSA2_2}	50% CTRL to within 0.1dB final value, 18dB state to 0dB state		15	35	

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DSA0 Phase Settling Time	$t_{DSA0\_1\_PH}$	50% CTRL to within 1 degree of final value, 0dB state to 6dB state		24	35	ns
	$t_{DSA0\_2\_PH}$	50% CTRL to within 1 degree of final value, 6dB state to 0dB state		18	35	
DSA2 Phase Settling Time	$t_{DSA2\_1\_PH}$	50% CTRL to within 1 degree of final value, 0dB state to 18dB state		16	35	ns
	$t_{DSA0\_1\_PH}$	50% CTRL to within 1 degree of final value, 18dB state to 0dB state		15	35	
Stability K factor	K_{FACT}	Over entire temperature range	1.4			unit
Serial Clock Speed	SPI_{CLK}				***10***	MHz
CSb_A, CSb_B to first serial clock rising edge	t_{LS}	SPI 3 wire bus. 50% of CSb falling edge to 50% of CLK rising edge.	10			ns
Serial Data Hold Time	t_H	SPI 3 wire bus. 50% of CLK rising edge to 50% of Data falling edge.	10			ns
Final serial clock rising edge to CSb	t_{LC}	SPI 3 wire bus. 50% of CLK rising edge to 50% of CSb rising edge.	10			ns
RF Input Return Loss	RL_{IN}			15		dB
RF Output Return Loss	RL_{OUT}			20		dB
Gain	G_{MAX}		***12***	***13***	***13.5***	dB
	G_{MIN}	Maximum attenuation	-38.1	-32	-26.4	
	G_{TEMP}	Variation over temperature		±0.15		
	G_{VAR}	Variation over frequency [3]		±0.2		
DSA0 Absolute Accuracy	INL_{DSA0}			0.52		dB
DSA1 Step Error	DNL_{DSA1}			0.16		dB
DSA1 Absolute Accuracy	INL_{DSA1}			0.55		dB
DSA2 Step Error	DNL_{DSA2}			0.32		dB
DSA2 Absolute Accuracy	INL_{DSA2}			0.43		dB
Relative Phase DSA0	Φ_{PH_DSA0}			6.6		deg
Phase Deviation DSA1	Φ_{PH_DSA1}	Between adjacent states		3		deg

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Relative Phase DSA2	Φ_{PH_DSA2}	Any State		6.6		deg
Noise Figure	NF			5.9		dB
	NF_{HOT}	T_{EPAD} = +105°C		6.6		
	NF_{22}	DSA1 22dB attenuation		27.7		
Output Third Order Intercept Point	$OIP3_1$	1MHz tone separation	34	37		dBm
	$OIP3_2$	1MHz tone separation P_{OUT} = -10dBm/tone	33	35		
	$OIP3_{6dB}$	1MHz tone separation DSA0 full attenuation		37		
	$OIP3_3$	1MHz tone separation Worst case over temp range	33	36		
	$OIP3_{18dB}$	P_{OUT} = -18dBm/tone 1MHz tone separation DSA2 full 18dB attenuation		21		
Input 1dB Compression [4]	IP1dB	Full attenuation		24		dBm
Output 1dB Compression	OP1dB			18		dBm
Reverse Isolation	REV_{ISO}		19	22		dB
Channel Isolation [5]	CH_{ISO}		35	39		dB
		Over voltage and temperature		39		

1. Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.
2. During standby mode, SPI is to be left ON and previous state is maintained when device is powered up.
3. Including frequency and ripple variations valid within each individual 3GPP band.
4. Input 1dB compression point is a linearity figure of merit. For maximum RF input power, see Absolute Maximum Ratings.
5. Signal applied to RFIN_A (RFIN_B), measure desired signal at RFOUT_A (RFOUT_B) and compare to signal level at RFOUT_B (RFOUT_A). Maximum gain setting.

2.4 Electrical Characteristics – For Wideband Performance (3.3GHz to 4.2GHz)

V_{CC} = +5V, T_C = +25°C, f_{RF} = 4.0GHz specifications apply when operated as a dual-channel RF DVGA, maximum gain setting, P_{OUT} = 0dBm, Z_{RFI} = Z_{RFO} = 50Ω, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated. For BOM details of this specific band, see Table 12.

Table 4. Electrical Characteristics (3.3GHz to 4.2GHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RF Input Return Loss	RL_{IN}			13		dB
RF Output Return Loss	RL_{OUT}			20		dB
Gain	G_{MAX}			12		dB
	G_{MIN}	Maximum attenuation		-36.5		
	G_{TEMP}	Variation over temperature		±0.4		
	G_{VAR}	Variation over frequency [3]		±0.6		
DSA0 Absolute Accuracy	INL_{DSA0}			2		dB
DSA1 Step Error	DNL_{DSA1}			0.7		dB
DSA1 Absolute Accuracy	INL_{DSA1}			2		dB
DSA2 Step Error	DNL_{DSA2}			0.6		dB
DSA2 Absolute Accuracy	INL_{DSA2}			0.7		dB
Relative Phase DSA0	Φ_{PH_DSA0}			6.3		deg
Phase Deviation DSA1	Φ_{PH_DSA1}	Between adjacent states		5.8		deg
Relative Phase DSA2	Φ_{PH_DSA2}	Any State		5.9		deg
Noise Figure	NF			7.7		dB
	NF_{HOT}	T_{EPAD} = +105°C		8.4		
	NF_{22}	DSA1 22dB attenuation		29.4		
Output Third Order Intercept Point	$OIP3_1$	1MHz tone separation		38		dBm
	$OIP3_2$	1MHz tone separation P_{OUT} = -10dBm/tone		34		
	$OIP3_{6dB}$	1MHz tone separation DSA0 full attenuation		32		
	$OIP3_3$	1MHz tone separation Worst case over temp range		31.5		
	$OIP3_{18dB}$	P_{OUT} = -18dBm/tone 1MHz tone separation DSA2 full 18dB attenuation		16		

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input 1dB Compression [4]	IP1dB	Full attenuation		25.5		dBm
Output 1dB Compression	OP1dB			17.5		dBm
Reverse Isolation	REV_{ISO}			21.5		dB
Channel Isolation [5]	CH_{ISO}			49		dB
		Over voltage and temperature		48		
Stability K factor	K_{FACT}	Over entire temperature range Up to 9GHz, V_{CC} = 4.75V to 5.25V	1			unit

1. Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.
2. During standby mode, SPI is to be left ON and previous state is maintained when device is powered up.
3. Including frequency and ripple variations valid within each individual 3GPP band.
4. Input 1dB compression point is a linearity figure of merit. For maximum RF input power, see Absolute Maximum Ratings.
5. Signal applied to RFIN_A (RFIN_B), measure desired signal at RFOUT_A (RFOUT_B) and compare to signal level at RFOUT_B (RFOUT_A). Maximum gain setting.

2.5 Thermal Characteristics

Table 5. Package Thermal Characteristics

Parameter	Symbol	Value	Unit
Junction to Ambient Thermal Resistance.	θ_{JA}	37.1	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	$\theta_{JC\text{-}BOT}$	9.1	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

3. Typical Performance Graphs

Unless otherwise noted, for the typical performance graphs on the following pages, the following conditions apply:

- V_{cc} = 5.0V
- $Z_L = Z_S$ = 50Ω Single ended
- f_{RF} = 3.6GHz
- T_{EPAD} = +25°C
- Gain setting = Maximum gain
- STBY = LOW
- P_{OUT} = 0dBm/tone
- 1MHz Tone Spacing
- ATTN setting = 0dB (Maximum gain; DSA0 = DSA1 = DSA2 = 0dB)
- All temperatures are referenced to the exposed paddle
- Evaluation Kit traces and connector losses are de-embedded

3.1 Typical Performance Characteristics (3.4GHz to 3.8GHz)

Figure 3. Maximum Gain vs. Frequency

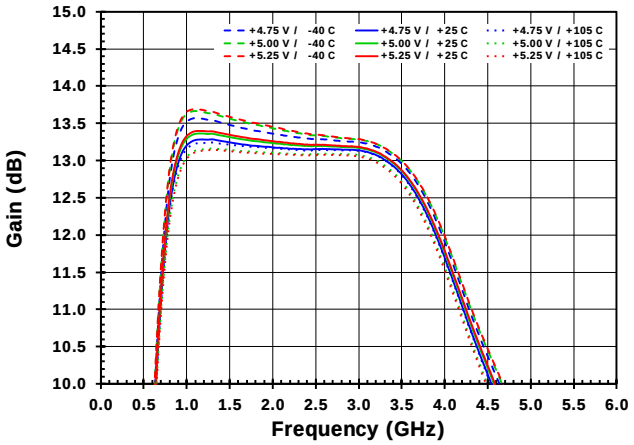


Figure 4. Gain vs. Frequency for DSA0 Settings

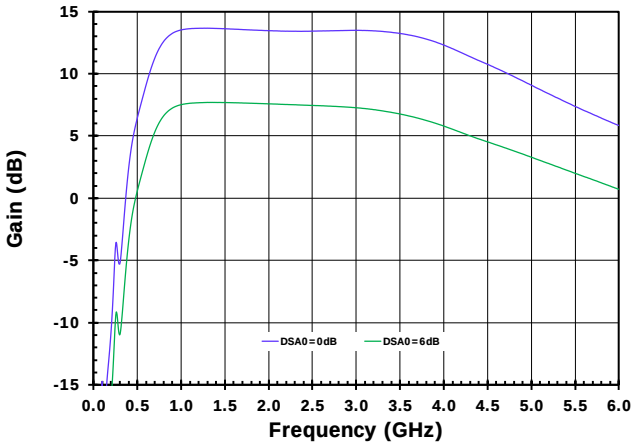


Figure 5. Gain vs. Frequency for DSA1 Settings

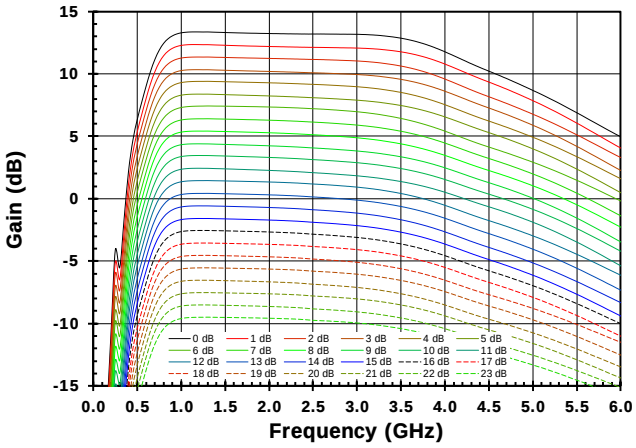


Figure 6. Gain vs. Frequency for DSA2 Settings

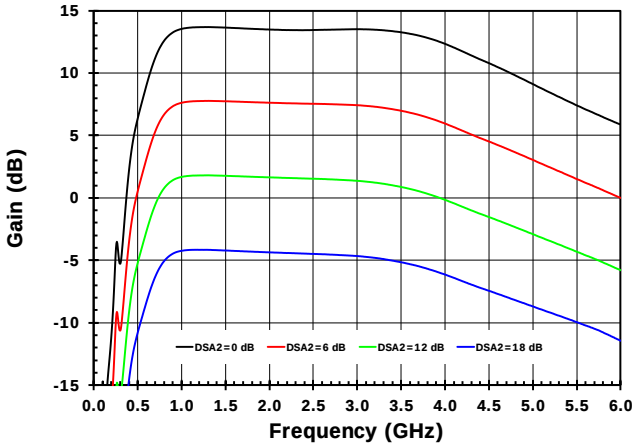


Figure 7. Stability vs. Frequency as a Function of Voltage and Temperature

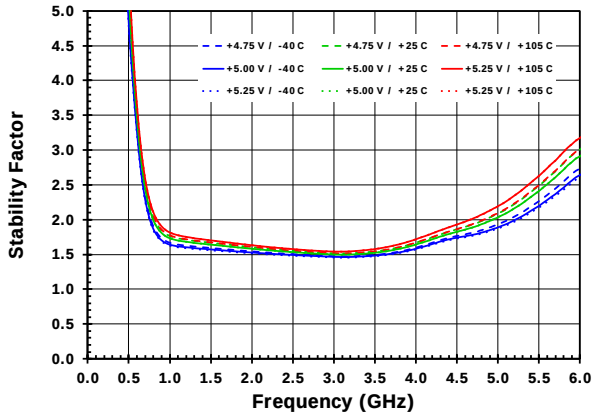


Figure 8. Input Return Loss for DSA0 Settings

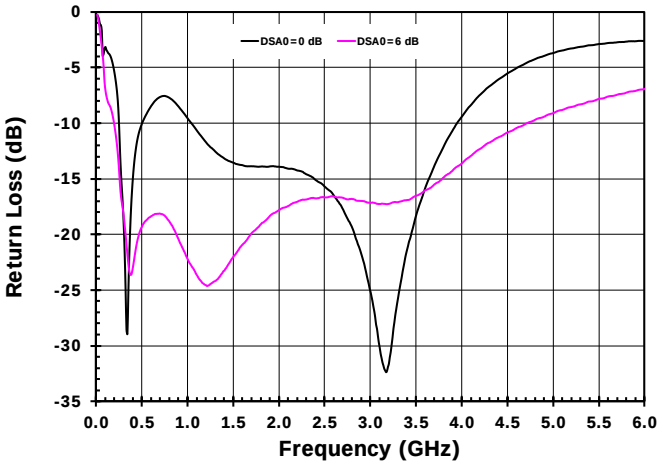


Figure 9. Output Return Loss for DSA0 Settings

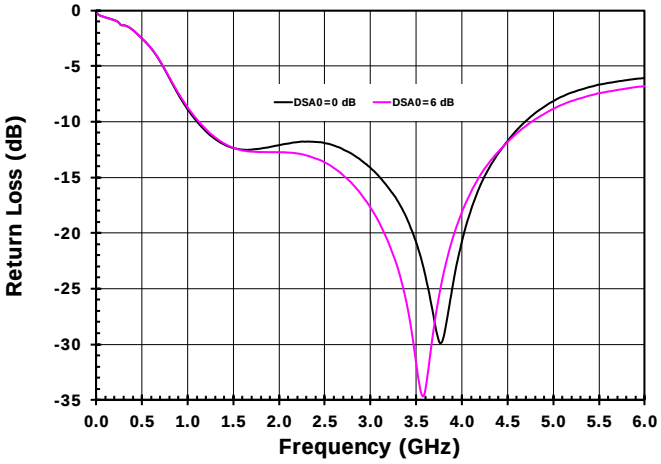


Figure 10. Input Return Loss for DSA1 Settings

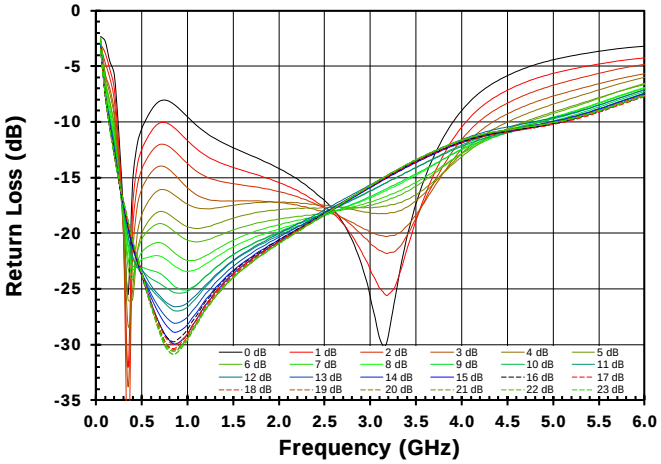


Figure 11. Output Return Loss for DSA1 Settings

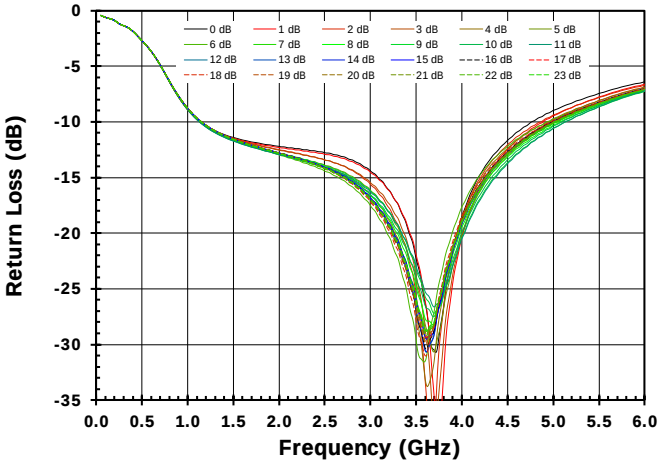


Figure 12. Input Return Loss for DSA2 Settings

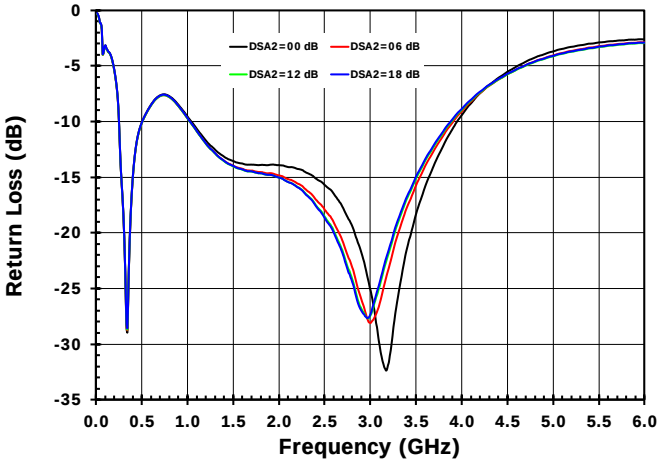


Figure 13. Output Return Loss for DSA2 Settings

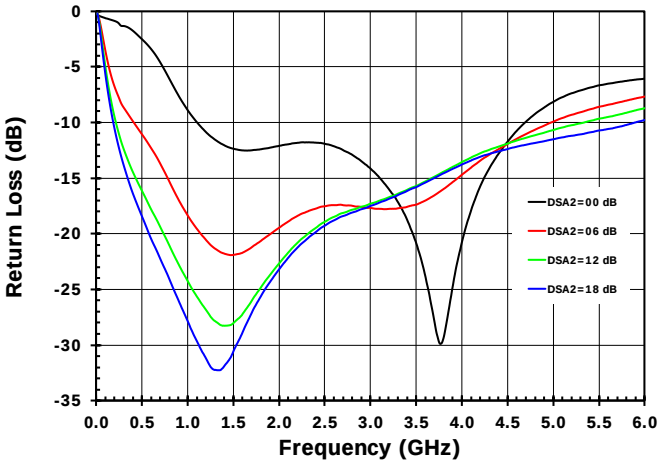


Figure 14. Reverse Isolation for DSA0 Settings

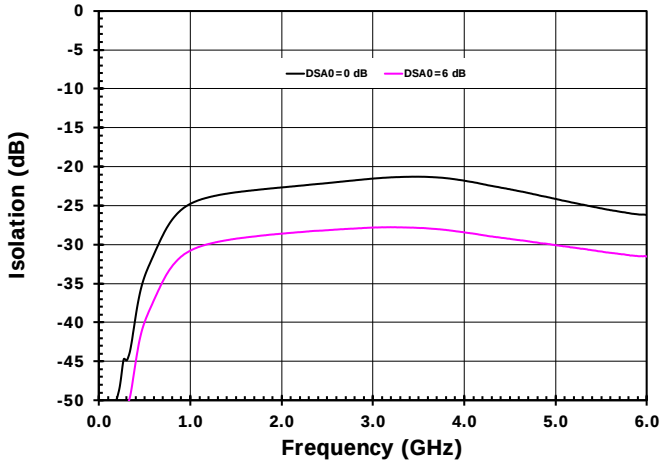


Figure 15. Phase Deviation Between Adjacent States vs. DSA0 Setting (3.6GHz)

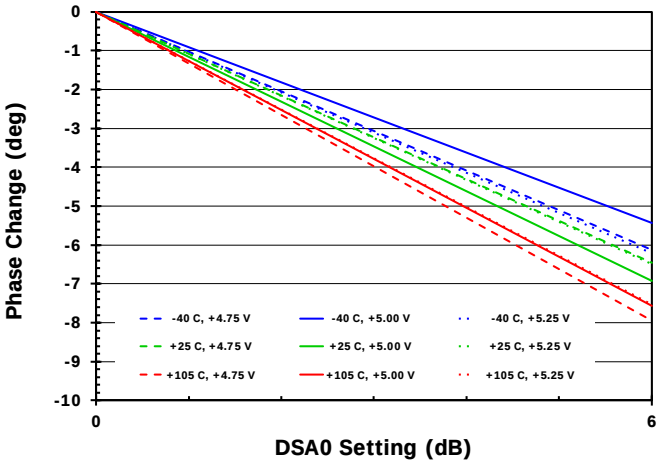


Figure 16. Reverse Isolation for DSA1 Settings

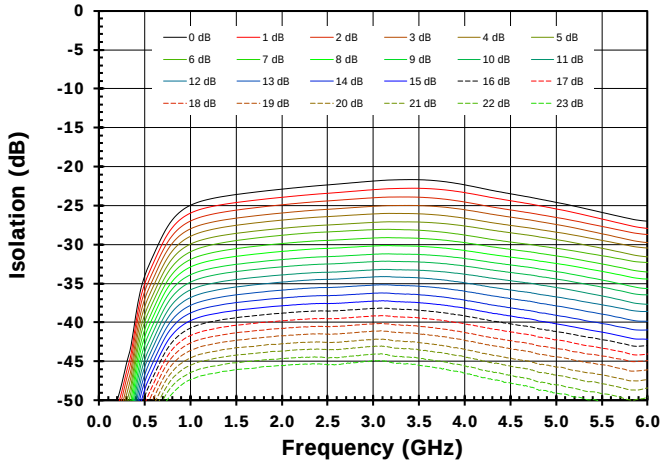


Figure 17. Phase Deviation Between Adjacent States vs. DSA1 Setting (3.6GHz)

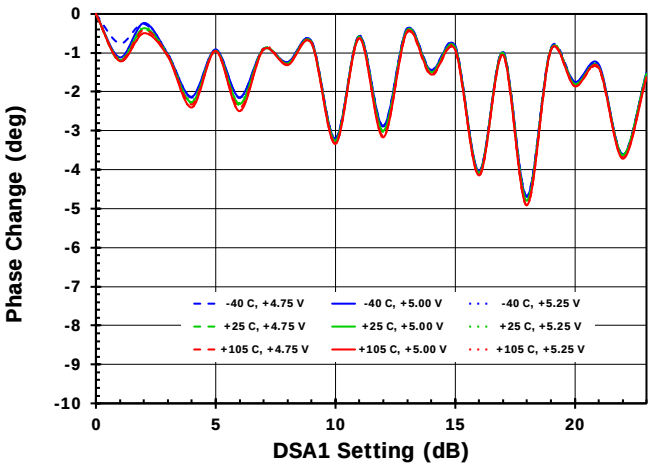


Figure 18. Reverse Isolation for DSA2 Settings

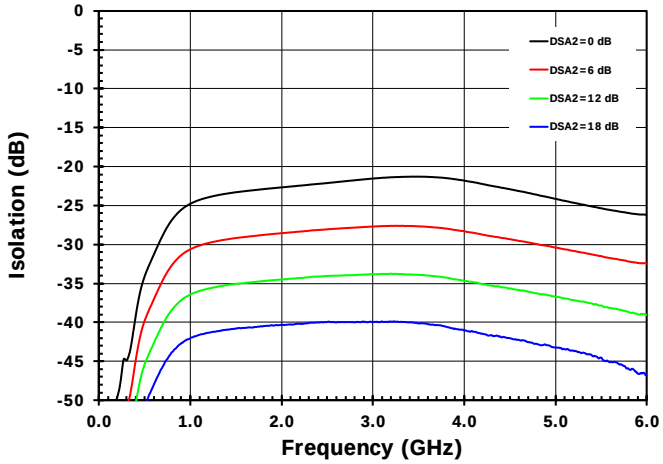


Figure 19. Phase Deviation Between Adjacent States vs. DSA2 Setting (3.6GHz)

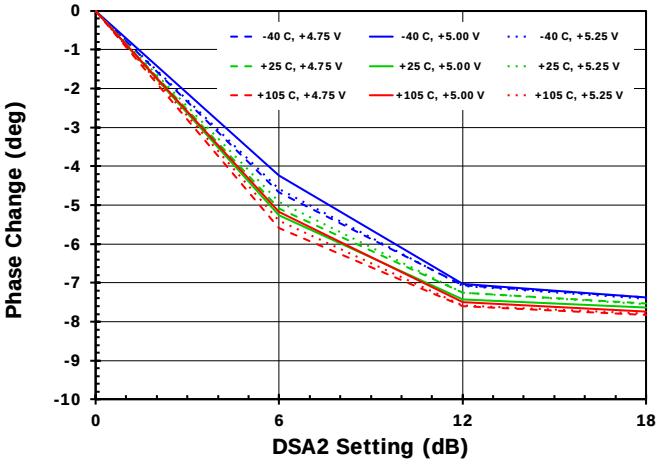


Figure 20. DSA0 Absolute Attenuation Error (INL) at 3.6GHz

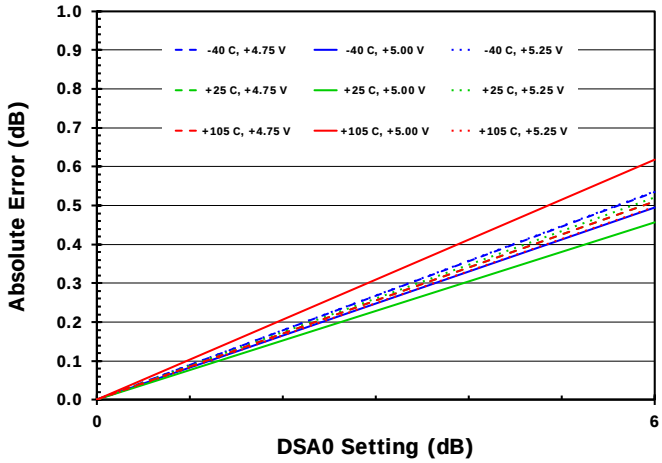


Figure 21. DSA0 Attenuator Step Error (DNL) at 3.6GHz

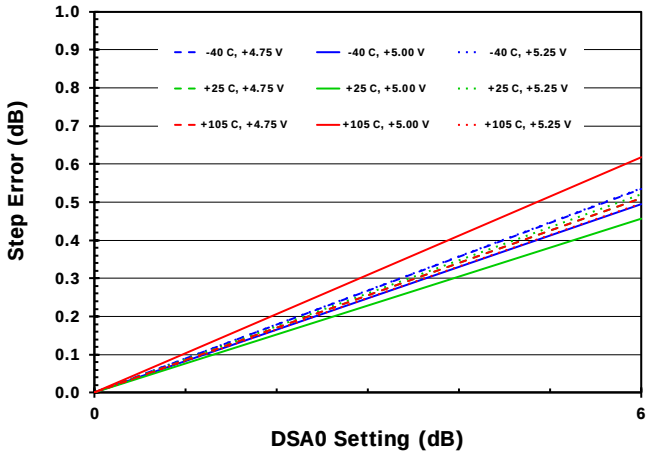


Figure 22. DSA1 Absolute Attenuation Error (INL) at 3.6GHz

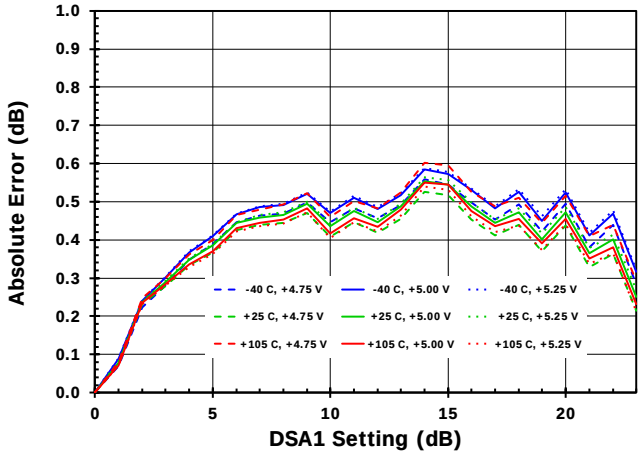


Figure 23. DSA1 Attenuator Step Error (DNL) at 3.6GHz

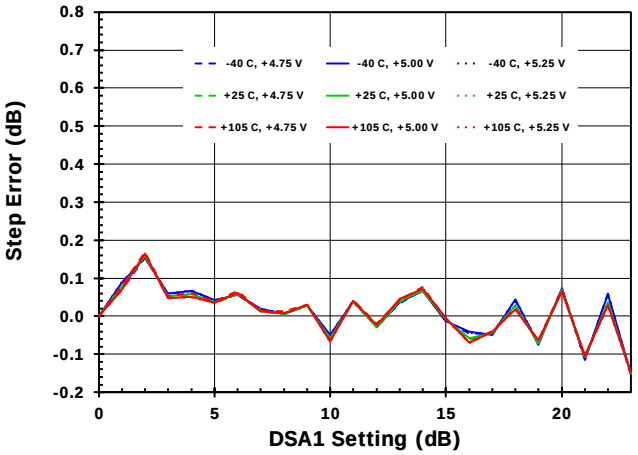


Figure 24. DSA2 Absolute Attenuation Error (INL) at 3.6GHz

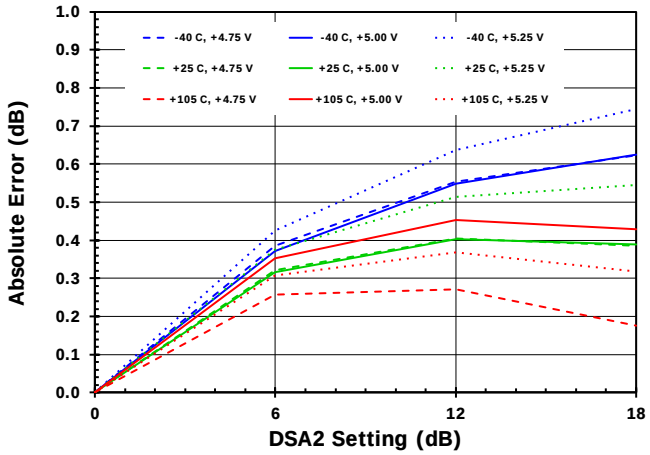


Figure 25. DSA2 Attenuator Step Error (DNL) at 3.6GHz

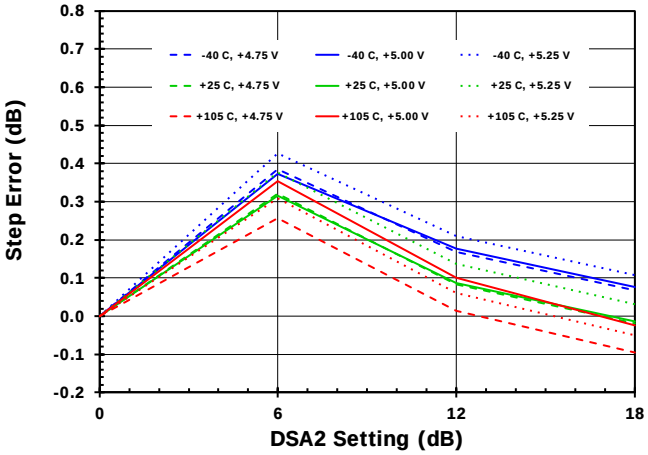


Figure 26. OIP3 vs. Frequency with P_{OUT} = 0dBm/Tone and Max Gain

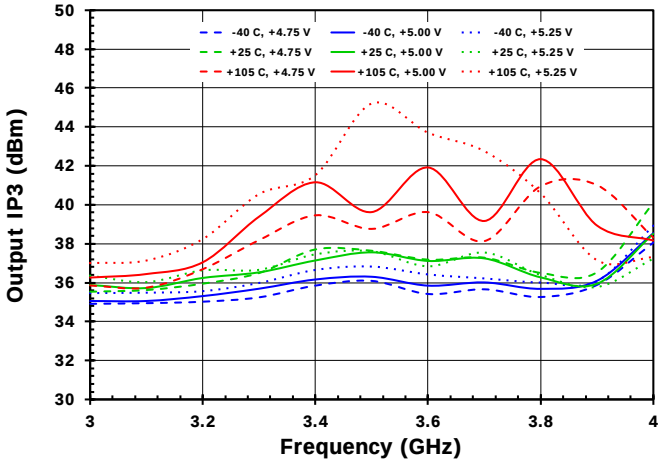


Figure 27. OIP3 vs. Frequency with P_{OUT} = -10dBm/Tone and Max Gain

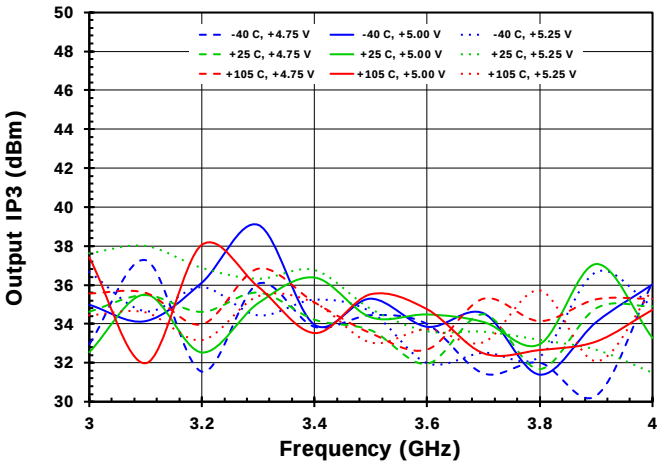


Figure 28. OIP3 vs. Frequency with P_{OUT} = -18dBm/Tone and DSA2 = 18dB

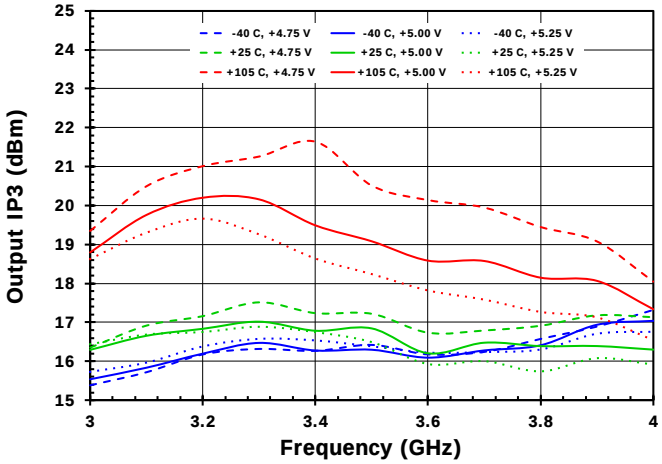


Figure 29. OIP3 vs. Frequency as a Function of Tone Spacing with P_{OUT} = 0dBm/Tone at 3.6GHz

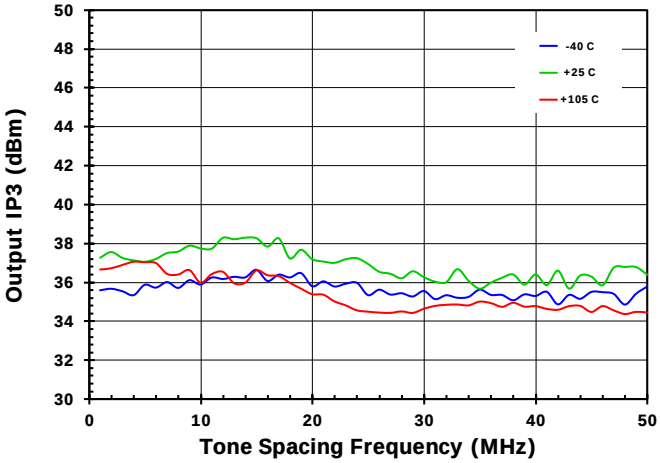


Figure 30. OIP3 vs. Frequency with P_{OUT} = 0dBm/Tone and DSA0 = 6dB

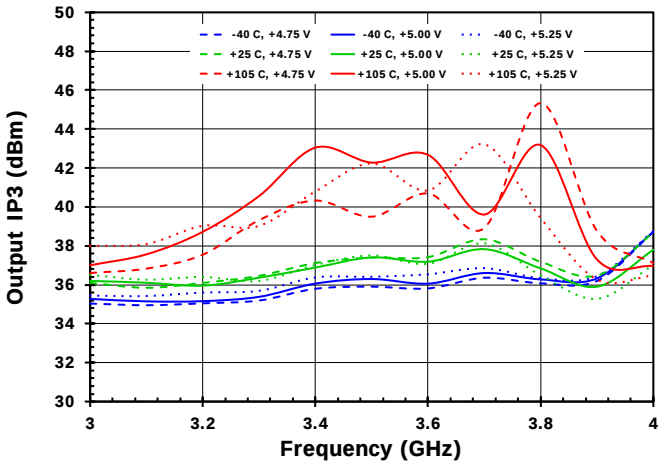


Figure 31. Wideband OIP2 vs. Frequency with P_{OUT} = -10dBm/Tone

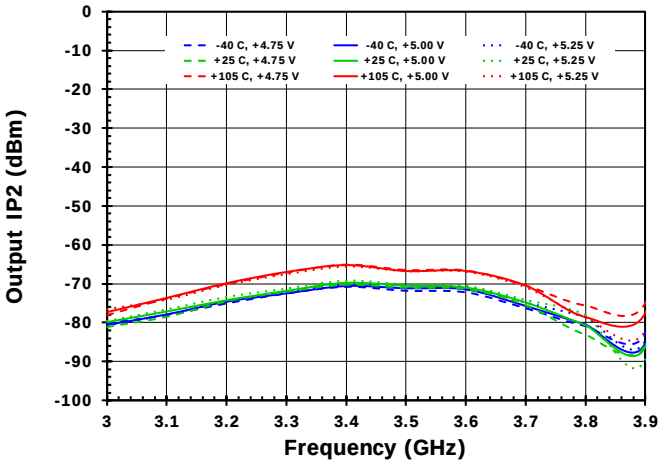


Figure 32. Wideband OIP2 vs. Frequency with P_{OUT} = 0dBm/Tone

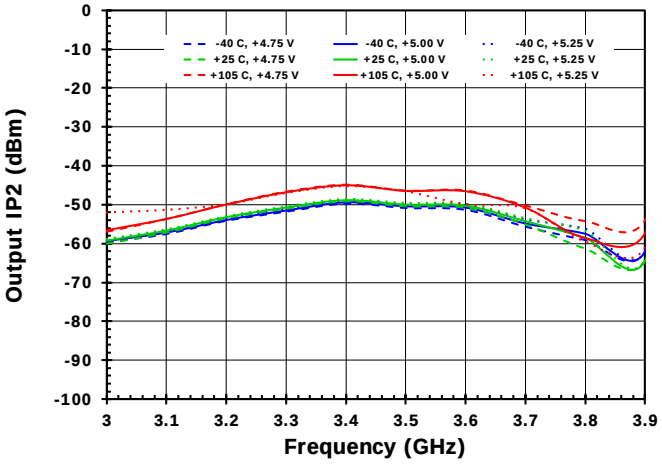


Figure 33. NF vs. Frequency as a Function of Temperature at Max Gain

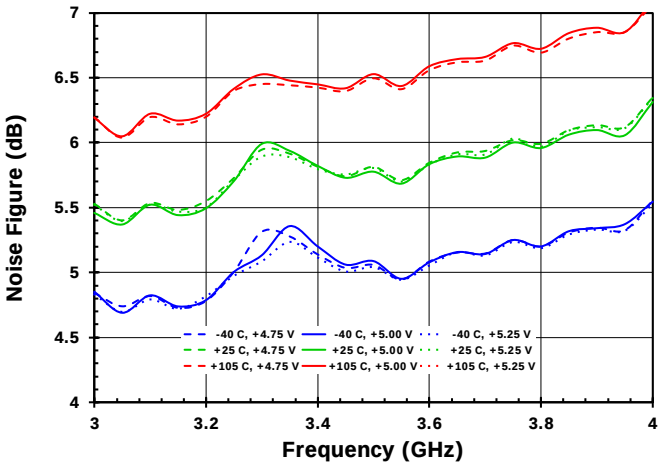


Figure 34. NF vs. Frequency as a Function of Temperature with DSA1 = 22dB

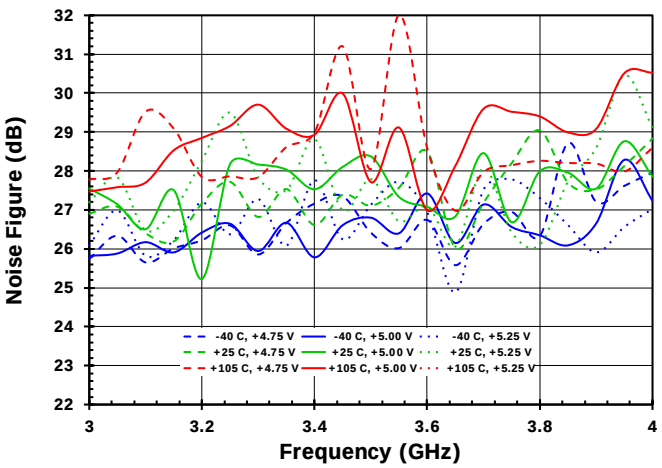


Figure 35. Gain Compression at f_{RF} = 3.6GHz

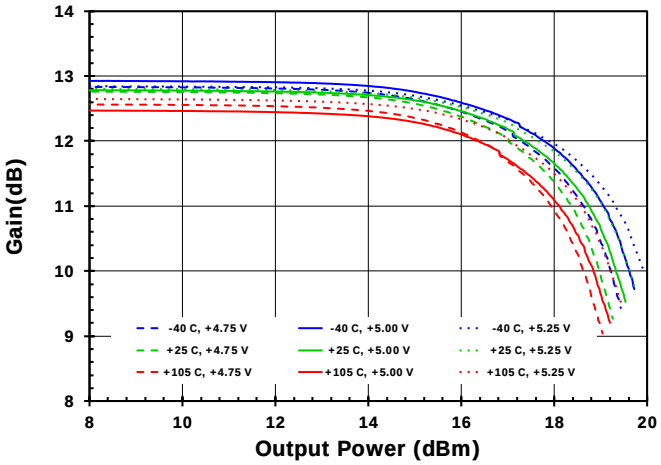
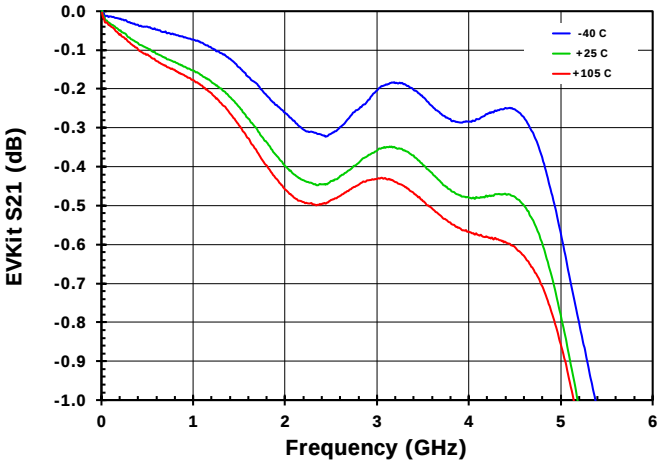


Figure 36. EVKit Connector and Trace Losses



3.2 Typical Performance Characteristics (3.3GHz to 4.2GHz)

Figure 37. Maximum Gain vs. Frequency

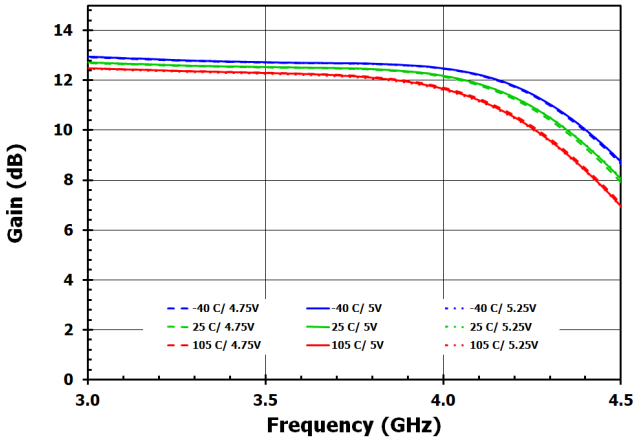


Figure 38. Gain vs. Frequency for DSA0 Settings

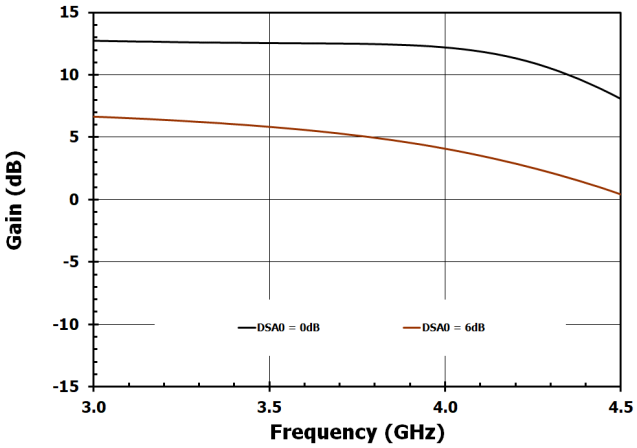


Figure 39. Gain vs. Frequency for DSA1 Settings

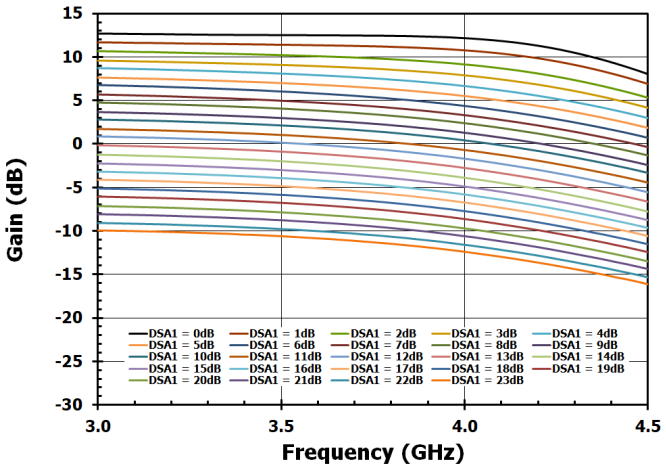


Figure 40. Gain vs. Frequency for DSA2 Settings

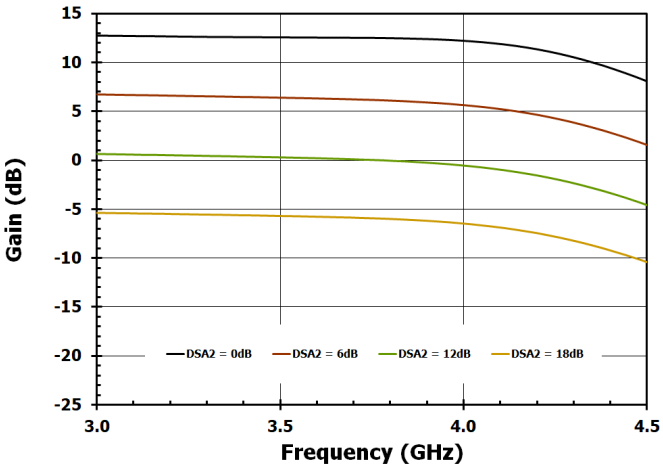


Figure 41. Input Return Loss vs. Frequency

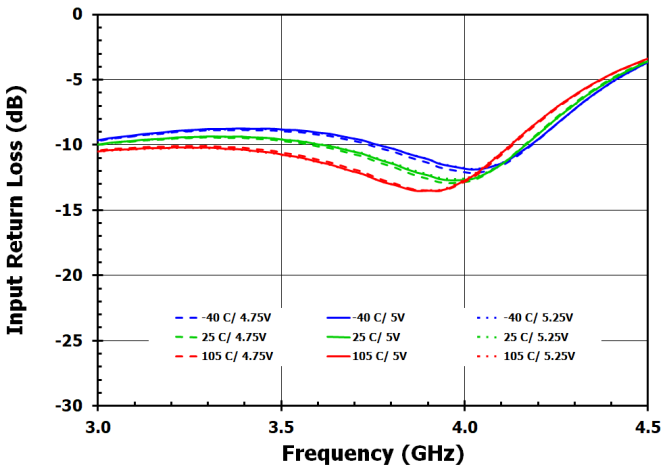


Figure 42. Output Return Loss vs. Frequency

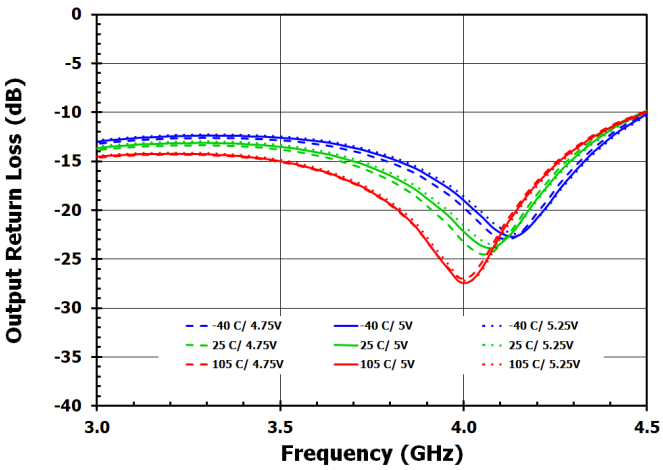


Figure 43. Input Return Loss for DSA0 Settings

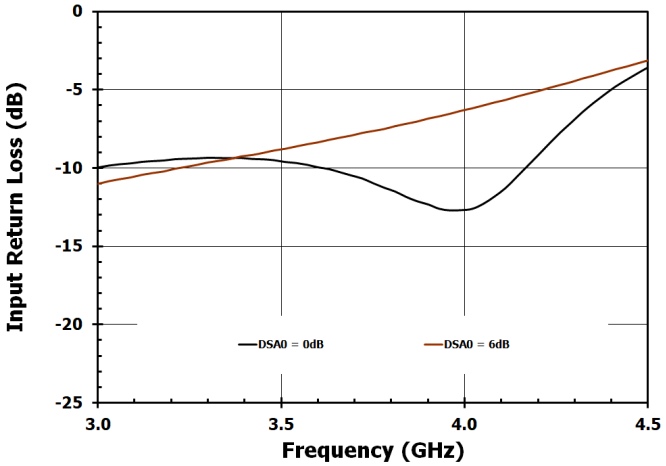


Figure 44. Output Return Loss for DSA0 Settings

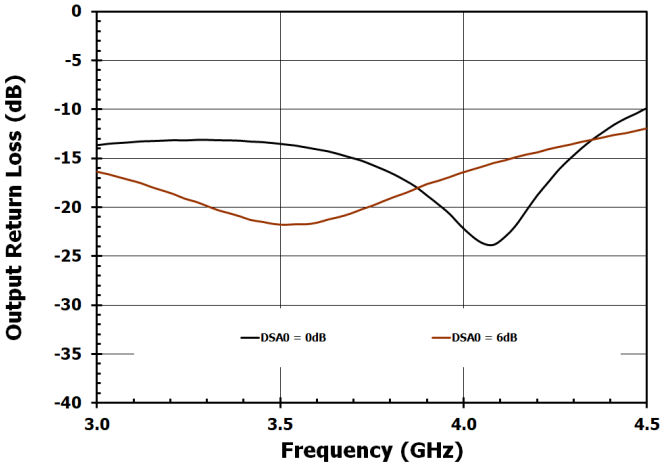


Figure 45. Input Return Loss for DSA1 Settings

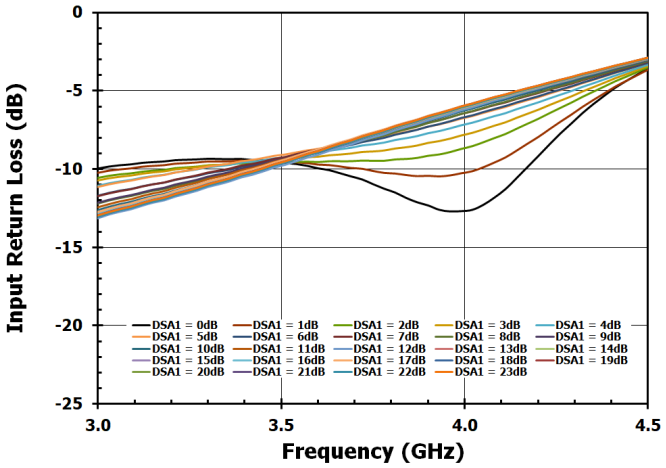


Figure 46. Output Return Loss for DSA1 Settings

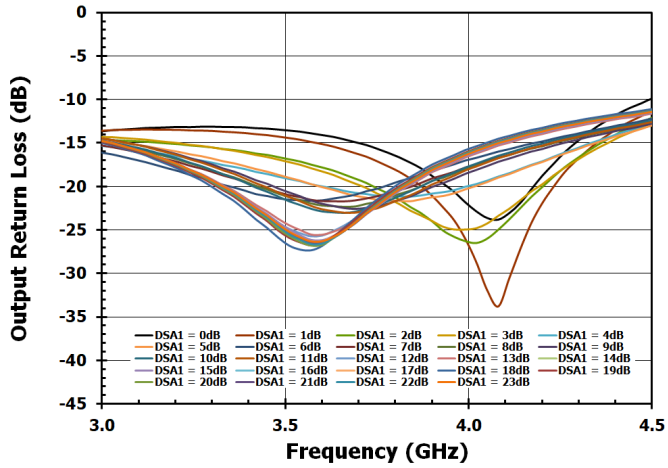


Figure 47. Input Return Loss for DSA2 Settings

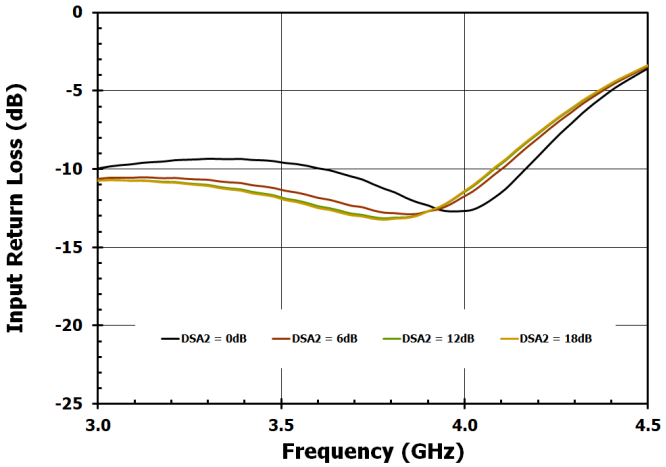


Figure 48. Output Return Loss for DSA2 Settings

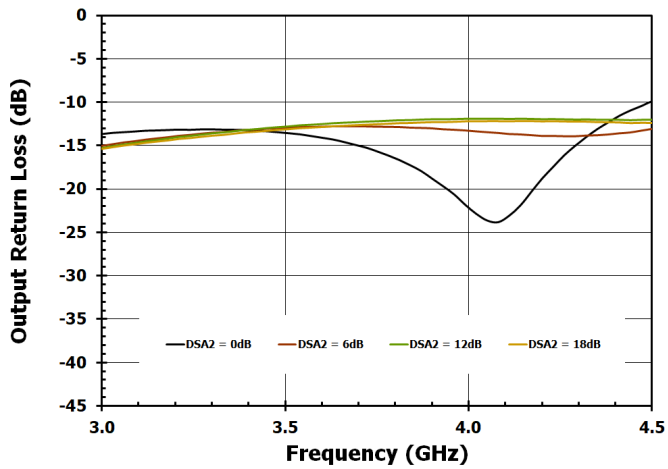


Figure 49. Reverse Isolation for DSA0 Settings

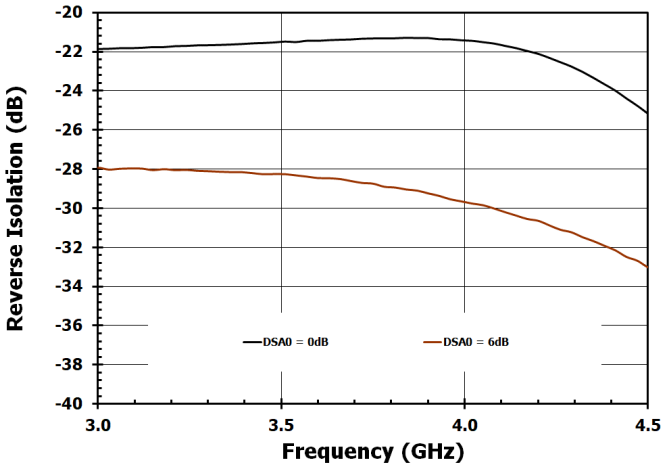


Figure 50. Phase Deviation Between Adjacent States vs. DSA0 Setting (4GHz)

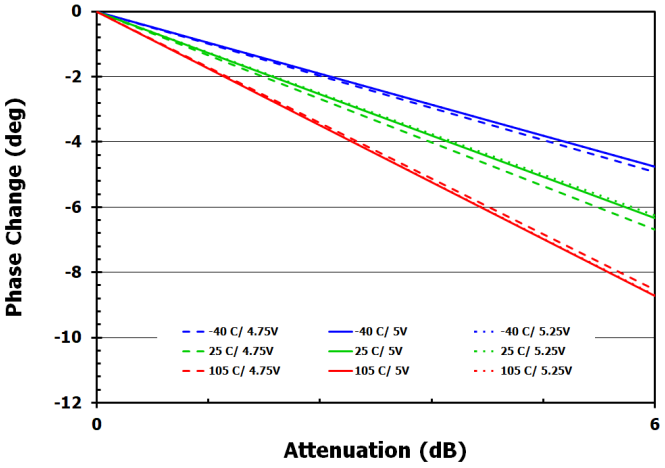


Figure 51. Reverse Isolation for DSA1 Settings

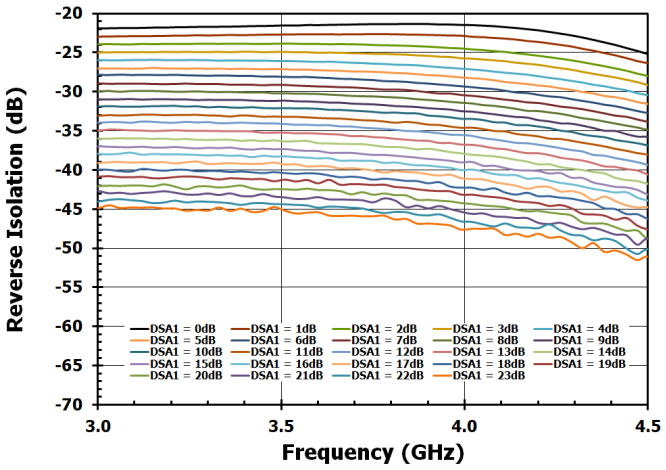


Figure 52. Phase Deviation Between Adjacent States vs. DSA1 Setting (4GHz)

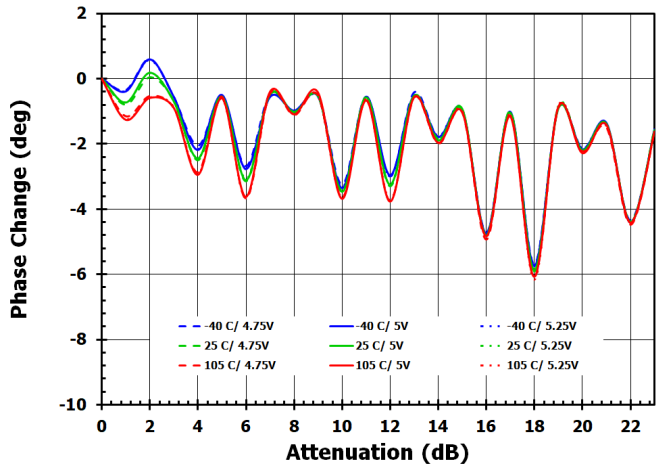


Figure 53. Reverse Isolation for DSA2 Settings

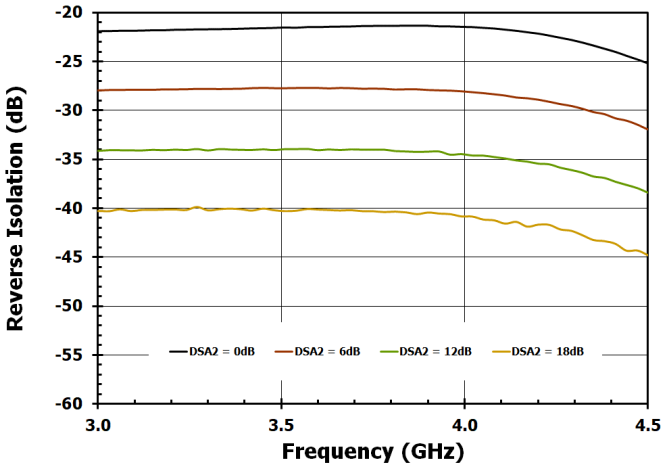


Figure 54. Phase Deviation Between Adjacent States vs. DSA2 Setting (4GHz)

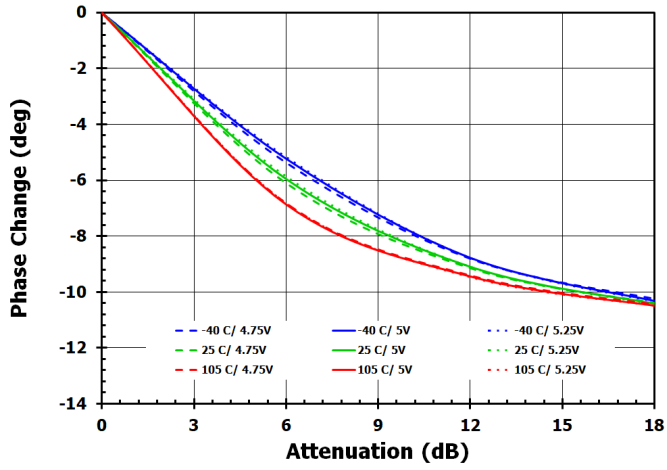


Figure 55. DSA0 Absolute Attenuation Error (INL) at 4GHz

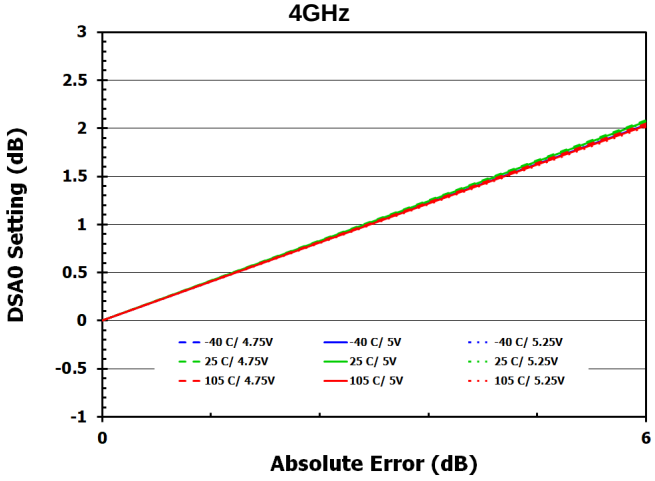


Figure 56. DSA0 Attenuator Step Error (DNL) at 4GHz

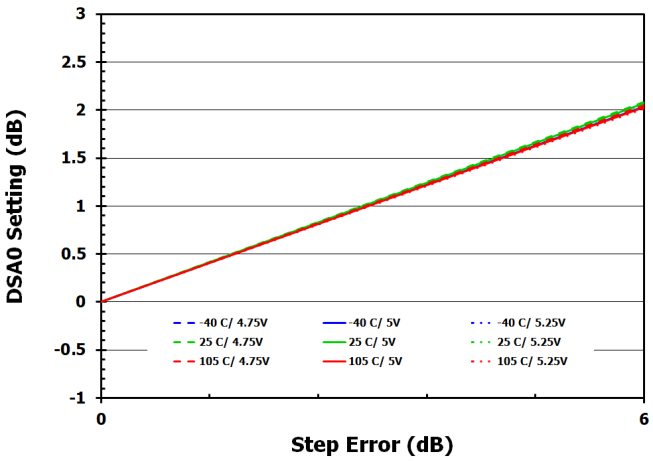


Figure 57. DSA1 Absolute Attenuation Error (INL) at 4GHz

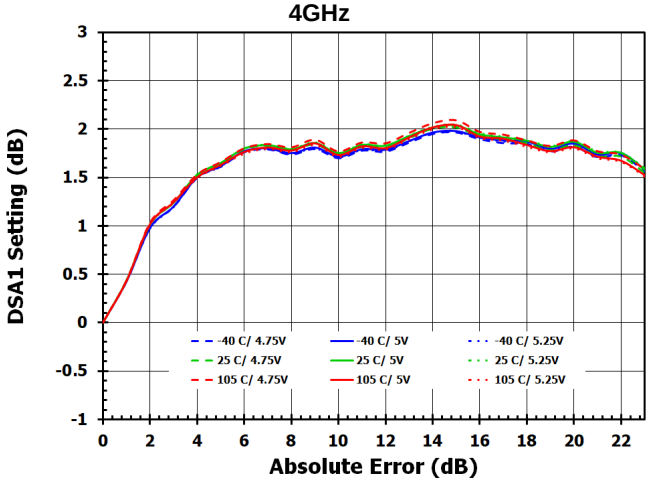


Figure 58. DSA1 Attenuator Step Error (DNL) at 4GHz

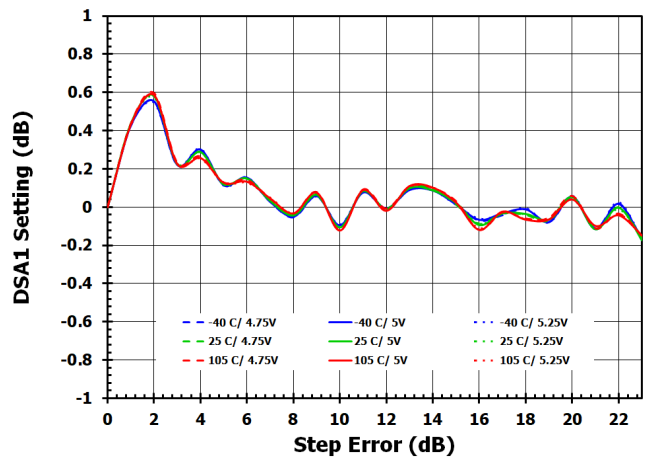


Figure 59. DSA2 Absolute Attenuation Error (INL) at 4GHz

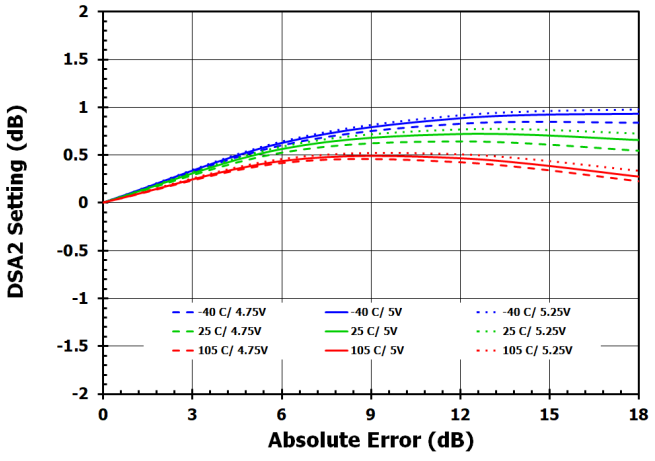


Figure 60. DSA2 Attenuator Step Error (DNL) at 4GHz

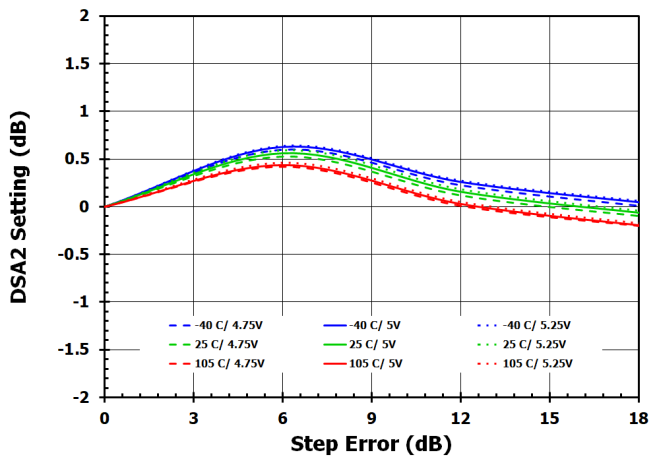


Figure 61. OIP3 vs. Frequency with P_{OUT} = 0dBm/Tone and Max Gain

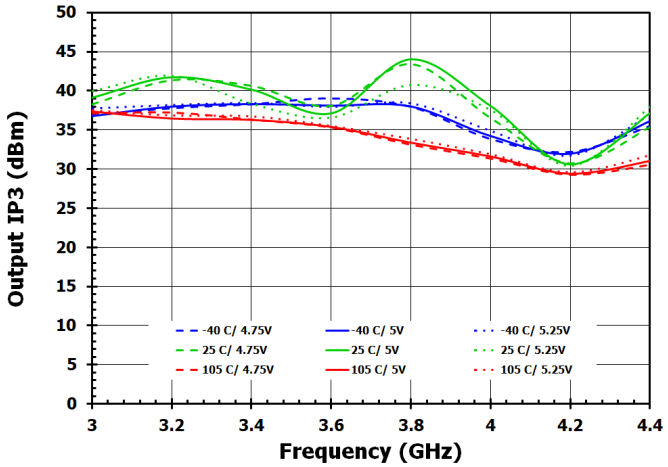


Figure 62. OIP3 vs. Frequency with P_{OUT} = -10dBm/Tone and Max Gain

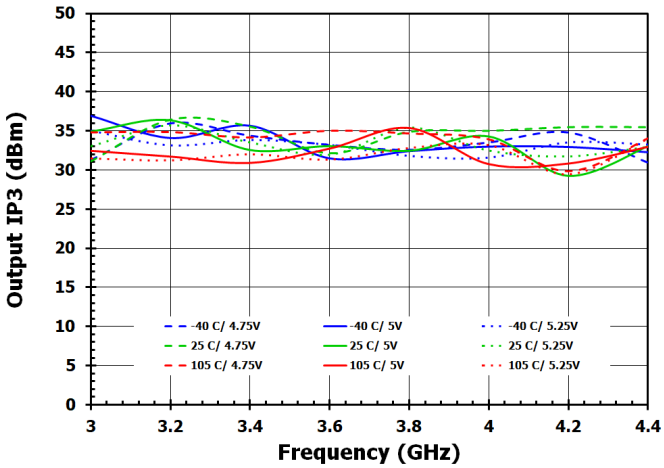


Figure 63. OIP3 vs. Frequency with P_{OUT} = -18dBm/Tone and DSA2 = 18dB

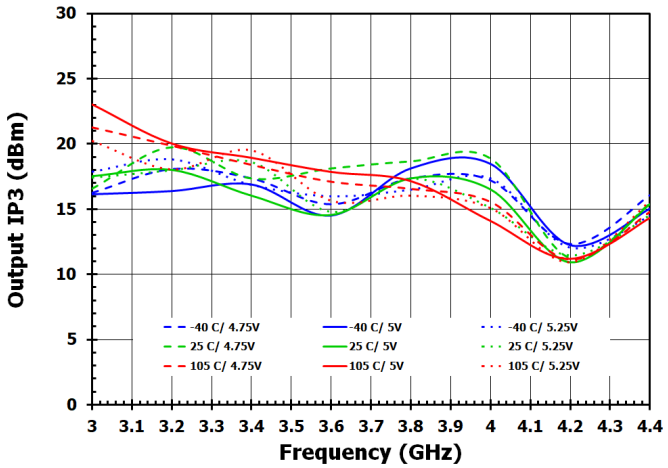


Figure 64. OIP3 vs. Frequency with P_{OUT} = 0dBm/Tone and DSA0 = 6dB

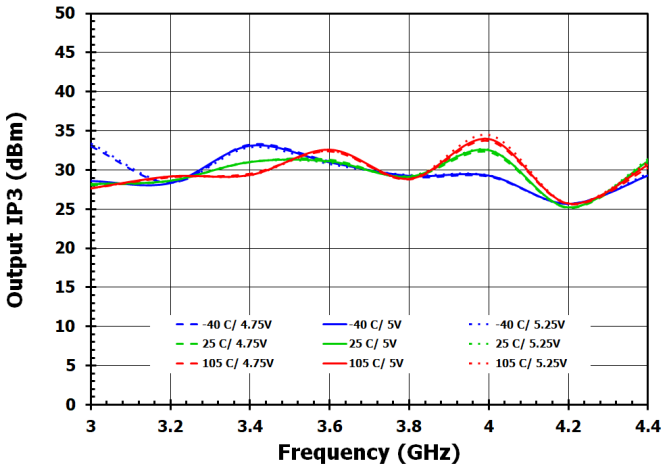


Figure 65. Output 1dB Compression

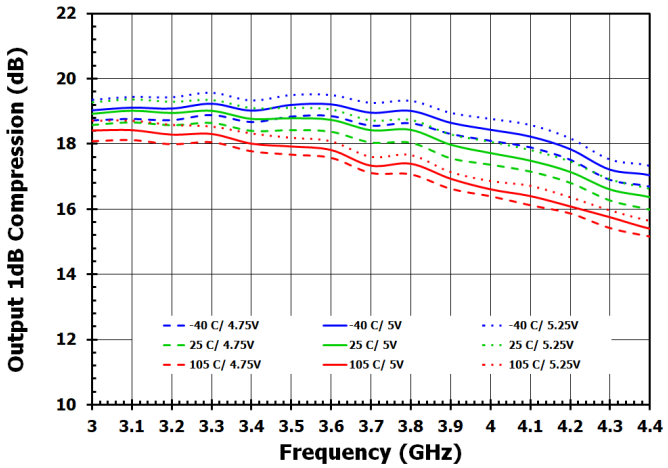


Figure 66. Stability Factor (K)

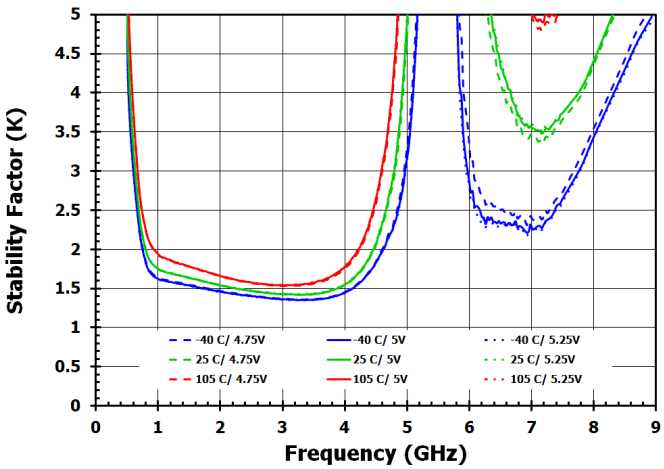
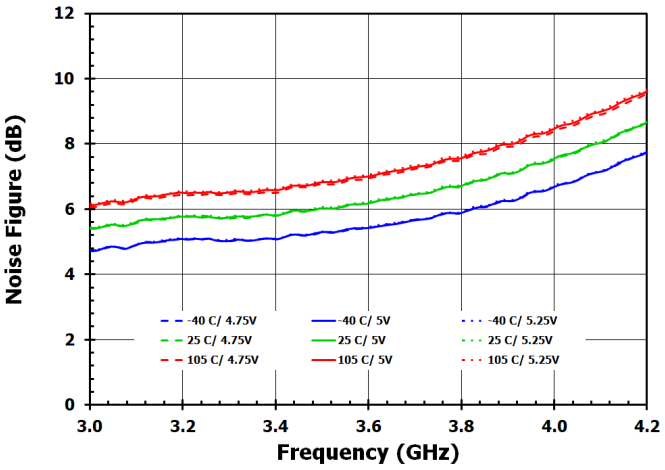


Figure 67. NF vs. Frequency as a Function of Temperature at Max Gain



4. Programming

The F0448 is programmed in both the serial and parallel. The 23dB attenuator (DSA1) is programmed using a three-wire serial control line. You choose which channel is programmed by using either or both CSb lines. Parallel pins are used for the one-bit 6dB attenuator ((DSA0_A, DSA0_B) and two-bit 18dB (6dB step) attenuator (DSA2_A, DSA2_B). The standby pins are also controlled by the parallel pin. All logic is both 1.8V and 3.3V compatible.

4.1 Serial Control – DSA1

The serial interface uses an 8-bit word with only 5 bits used. The serial word is shifted in LSB (D0) first.

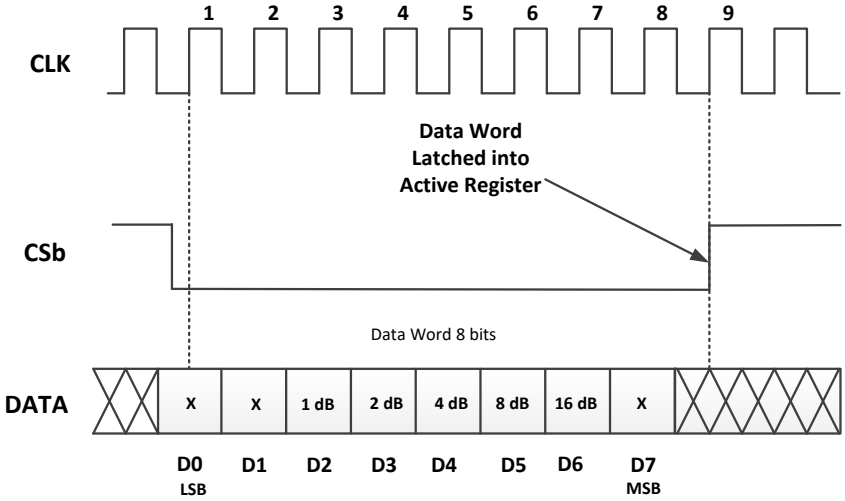


Figure 68. Serial Register Data Flow Diagram (LSB Clock in First)

When the device is first powered up, DSA1 will default to the **Maximum Attenuation** setting as shown.

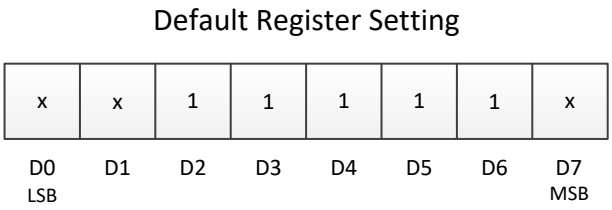


Figure 69. DSA1 Default Condition

The F0448 includes a CLK inhibit feature designed to minimize sensitivity to CLK bus noise when the device is not being programmed. When CSb is high (> V_{IH}), the CLK input is disabled and serial data (DATA) is not clocked into the shift register. It is recommended that CSb be pulled high (> V_{IH}) when the device is not being programmed.

Table 6. DSA1 Attenuation Word Truth Table (LSB = First In)

D7 (MSB)	Attenuation word							Attenuation Setting (dB)
	D6	D5	D4	D3	D2	D1	D0 (LSB)	
x	LOW	LOW	LOW	LOW	LOW	x	x	0
x	LOW	LOW	LOW	LOW	HIGH	x	x	1
x	LOW	LOW	LOW	HIGH	LOW	x	x	2
x	LOW	LOW	HIGH	LOW	LOW	x	x	4
x	LOW	HIGH	LOW	LOW	LOW	x	x	8
x	HIGH	LOW	LOW	LOW	LOW	x	x	16
x	HIGH	LOW	HIGH	HIGH	LOW	x	x	22
x	HIGH	LOW	HIGH	HIGH	HIGH	x	x	23 (max)
x	HIGH	HIGH	LOW	LOW	LOW	x	x	23 (max)
x	HIGH	HIGH	LOW	LOW	HIGH	x	x	23 (max)
x	HIGH	HIGH	LOW	HIGH	LOW	x	x	23 (max)
x	HIGH	HIGH	LOW	HIGH	HIGH	x	x	23 (max)
x	HIGH	HIGH	HIGH	LOW	LOW	x	x	23 (max)
x	HIGH	HIGH	HIGH	LOW	HIGH	x	x	23 (max)
x	HIGH	HIGH	HIGH	HIGH	LOW	x	x	23 (max)
x	HIGH	HIGH	HIGH	HIGH	HIGH	x	x	23 (max)

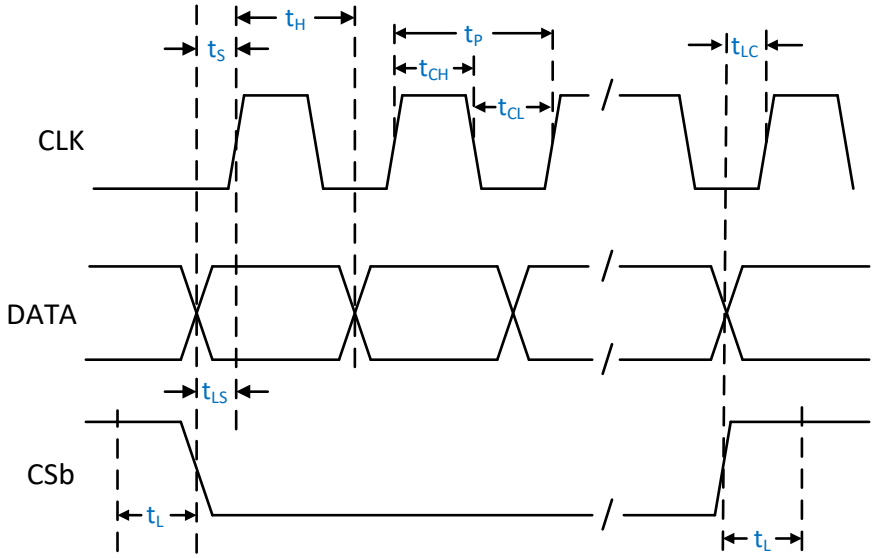


Figure 70. Serial Timing Diagram

Table 7. SPI Timing Diagram Values for Figure 70

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Unit
CLK Frequency	f_C				10	MHz
CLK High Duration Time	t_{CH}		50			ns
CLK Low Duration Time	t_{CL}		50			ns
DATA to CLK Setup Time	t_S		10			ns
CLK Period [a]	t_P		100			ns
CLK to DATA Hold Time	t_H		10			ns
CSb to CLK Setup Time	t_{LS}		10			ns
CSb Trigger Pulse Width	t_L		10			ns
CSb Trigger to CLK Setup Time [b]	t_{LC}		10			ns

[a] $(t_{CH} + t_{CL}) \geq 1/f_C$

[b] Once all desired DATA is clocked in, t_{LC} represents the time a CSb high needs to occur before any subsequent CLK signals.

5. Parallel Control Mode – DSA0, DSA2, STBY

Externally set the parallel control pins either logic LOW or HIGH.

Table 8. DSA0 Truth Table

VCTRL0_A (VCTRL0_B)	ATTENUATION SETTING (dB) DSA0_A or DSA0_B
LOW	0 (Reference IL)
HIGH	6

Table 9. DSA2 Truth Table

VCTRL1_A (VCTRL1_B)	VCTRL2_A (VCTRL2_B)	ATTENUATION SETTING (dB) DSA2_A or DSA2_B
LOW	LOW	0 (Reference IL)
HIGH	LOW	6
LOW	HIGH	12
HIGH	HIGH	18

Table 10. STANDBY Truth Table

Control Pins	Logic Level	Function
STBY_A, STBY_B	LOW (or open)	Channel Powered On
	HIGH	Channel Powered OFF

6. Typical Application Circuit

Figure 71 is a typical circuit that can be used in a design for the F0448.

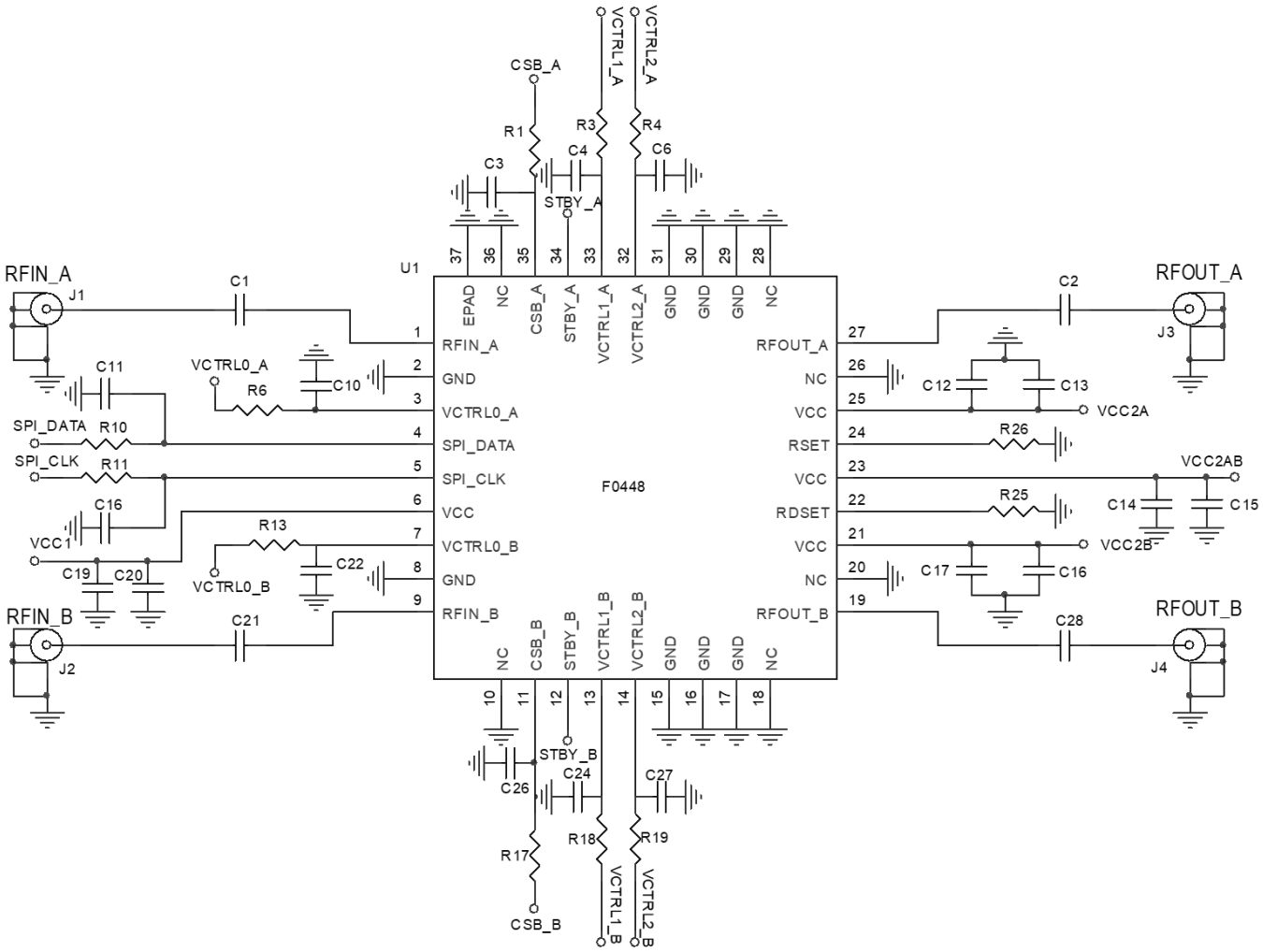


Figure 71. Typical Application Schematic

7. Evaluation Board

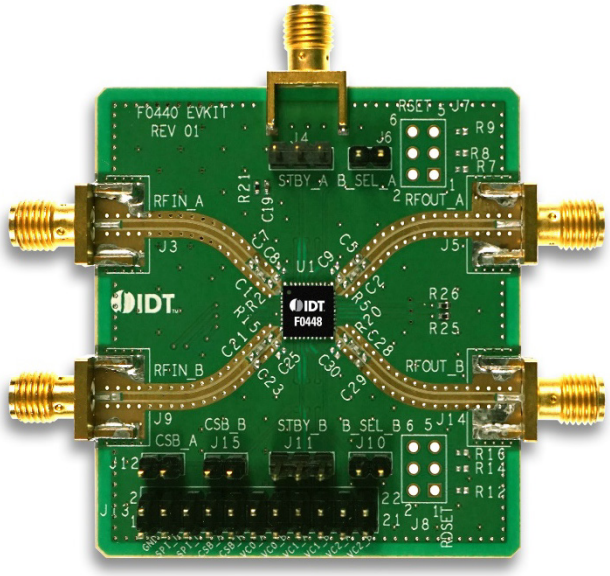


Figure 72. Evaluation Board – Top View

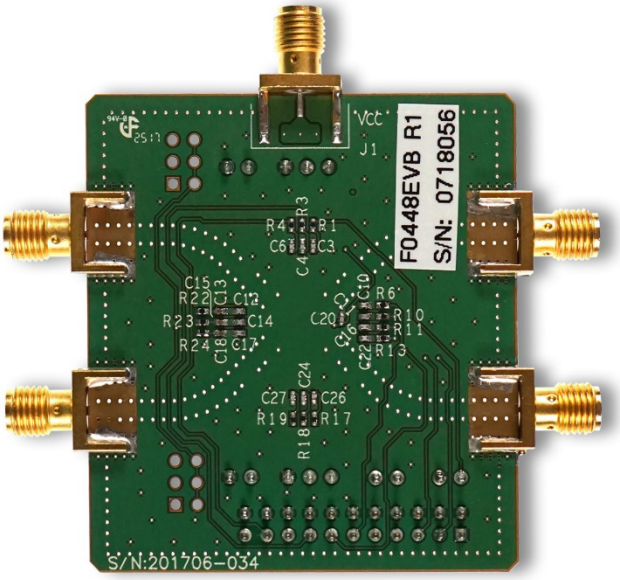


Figure 73. Evaluation Board – Bottom View

7.1 Evaluation Board Schematic

Figure 74 is the evaluation board schematic.

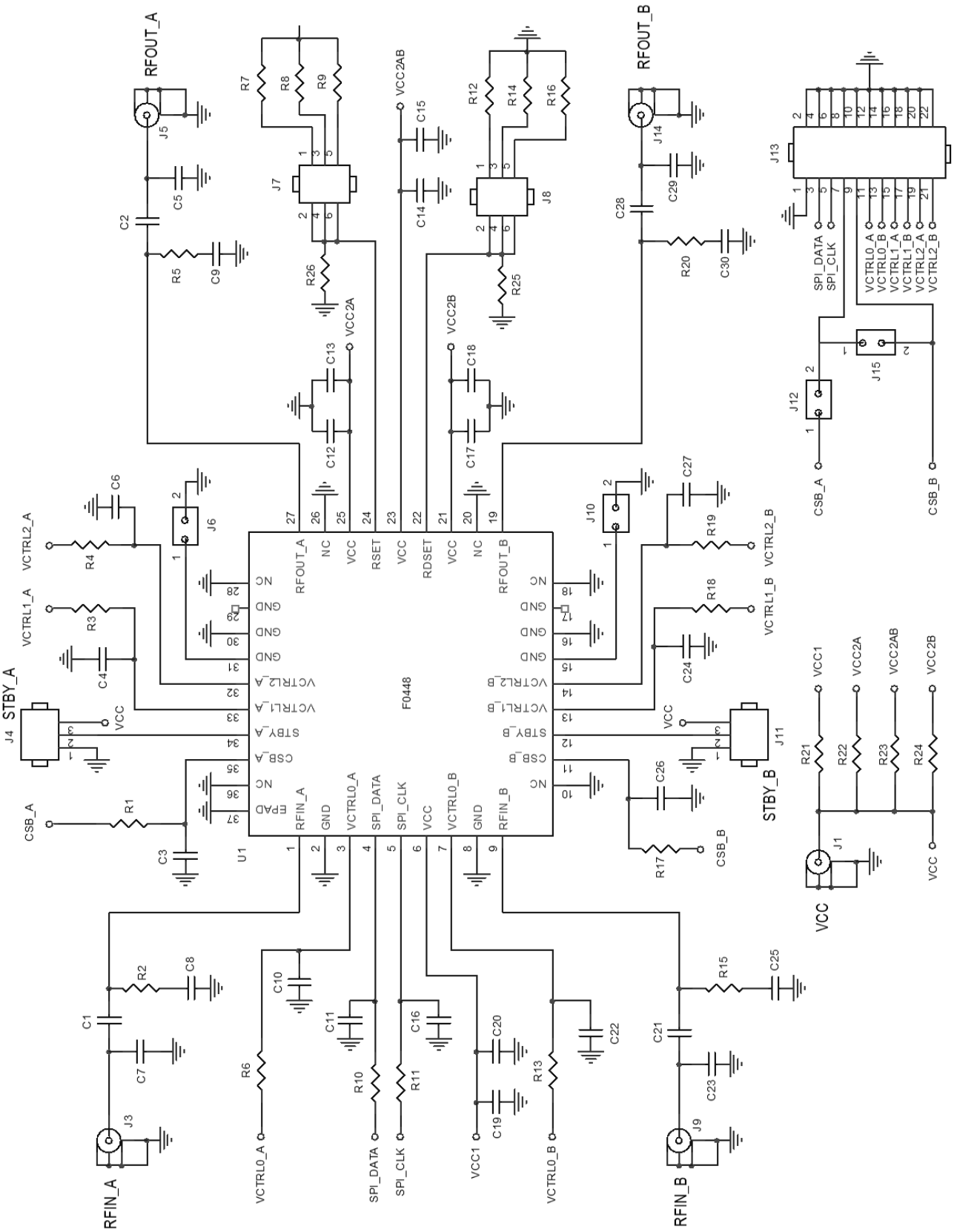


Figure 74. Evaluation Board Schematic

7.2 Evaluation Board BOM (3.4GHz to 3.8GHz)

Table 11. Bill of Materials (3.4GHz to 3.8GHz)

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C1, C2, C21, C28	4	47pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H470J	Murata
C3, C4, C6, C10, C11, C16, C22, C24, C26, C27	10	2pF ±0.1pF, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H2R0B	Murata
C12, C14, C17, C20	4	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	Murata
C13, C15, C18, C19	4	0.1µF ±10%, 16V, X7R Ceramic Capacitor (0402)	GRM155R71C104K	Murata
R1, R3, R4, R6, R10, R11, R13, R17, R18, R19	10	5.11kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF5111X	Panasonic
R21, R22, R23, R24	4	0Ω Resistor (0402)	ERJ-2GE0R00X	Panasonic
R25, R26	2	4.42kΩ ±1%, 1/10W, Resistor (0402)	ERJ-3EKF4421V	Panasonic
J1, J3, J5, J9, J14	5	Edge Launch SMA (0.375 inch pitch ground tabs)	142-0701-851	Emerson Johnson
J4, J11	2	CONN HEADER VERT SGL 3 X 1 POS GOLD	961103-6404-AR	3M
J6, J10, J12, J15	4	CONN HEADER VERT SGL 2 X 1 POS	961102-6404-AR	3M
J13	1	CONN HEADER VERT SGL 11 X 2 POS GOLD	67997-122HLF	FCI
U1	1	Dual DVGA	F0448NBGK	Renesas
	1	Printed Circuit Board	F0440 EVKIT REV 01	Renesas
C5, C7, C8, C9, C23, C25, C29, C30, R2, R5, R15, R20, R7, R8, R9, R12, R14, R16, J7, J8		DNP		

7.3 Evaluation Board BOM – For Wideband Performance (3.3GHz to 4.2GHz)

Table 12. Bill of Materials – For Wideband Performance (3.3GHz to 4.2GHz)

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C1, C21, C2, C28	4	47pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H470J	Murata
C3, C4, C6, C10, C11, C16, C22, C24, C26, C27	10	2pF ±0.1pF, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H2R0B	Murata
C12, C14, C17, C20	4	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	Murata
C13, C15, C18, C19	4	0.1µF ±10%, 16V, X7R Ceramic Capacitor (0402)	GRM155R71C104K	Murata
R1, R3, R4, R6, R10, R11, R13, R17, R18, R19	10	5.11kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF5111X	Panasonic
R21, R22, R23, R24, C8, C25	6	0Ω Resistor (0402)	ERJ-2GE0R00X	Panasonic
R25, R26	2	4.42kΩ ±1%, 1/10W, Resistor (0402)	ERJ-3EKF4421V	Panasonic
R2, R15	2	0.6 pF ±1pF, 50V, Ceramic Capacitor (0402)	GRM0225C1HR60BA	Murata
J1, J3, J5, J9, J14	5	Edge Launch SMA (0.375 inch pitch ground tabs)	142-0701-851	Emerson Johnson
J4, J11	2	CONN HEADER VERT SGL 3 X 1 POS GOLD	961103-6404-AR	3M
J6, J10, J12, J15	4	CONN HEADER VERT SGL 2 X 1 POS	961102-6404-AR	3M
J13	1	CONN HEADER VERT SGL 11 X 2 POS GOLD	67997-122HLF	FCI
U1	1	Dual DVGA	F0448NBGK	Renesas
	1	Printed Circuit Board	F0440 EVKIT REV 01	Renesas
C5, C7, C9, C23, C29, C30, R5, R20, R7, R8, R9, R12, R14, R16, J7, J8		DNP		

7.4 Evaluation Board Operation

7.4.1. Power Supply Setup

Set up a power supply in the voltage range of 4.75V to 5.25V with the power supply output disabled. The voltage is applied via the SMA connector, J1, show in Figure 75 and Figure 76.

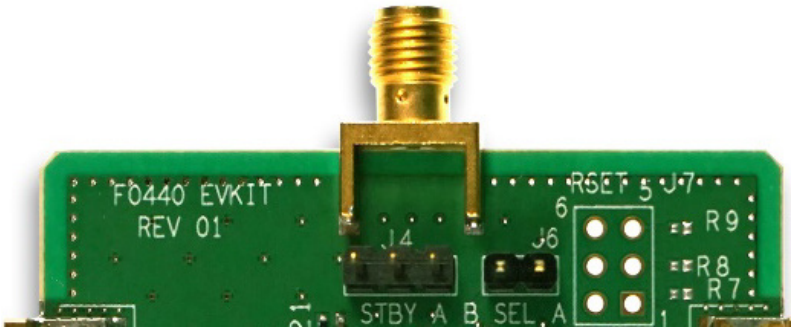


Figure 75. Power Supply Connections – Top View

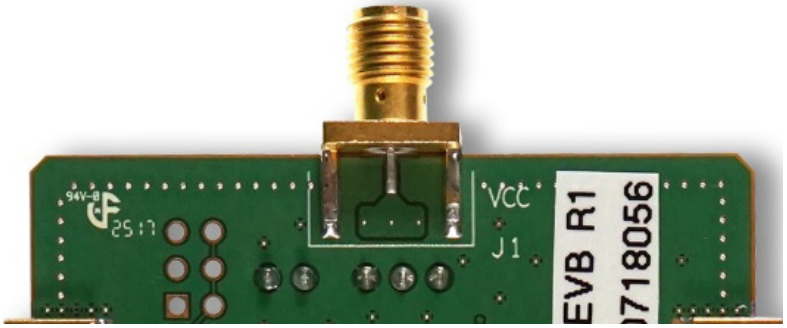


Figure 76. Power Supply Connections – Bottom View

7.4.2. GND Jumpers

Headers J6 and J10 must be jumped (grounded) for optimum RF performance. Figure 77 shows the header locations.

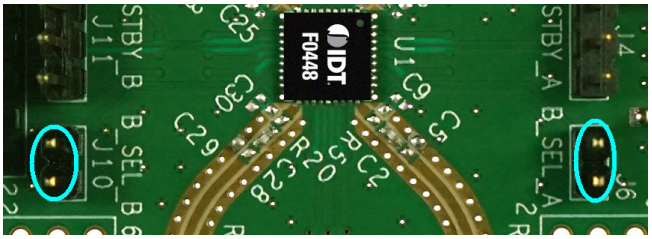


Figure 77. Two Ground Jumper Connections

7.4.3. Standby (STBY) Pin

The Evaluation Board can control the F0448 for standby operation. The standby pin is the center pin of the J4 and J11 header as shown in Figure 78. VCC (logic HIGH) and ground (logic LOW) pins are available to make a connection with a jumper.

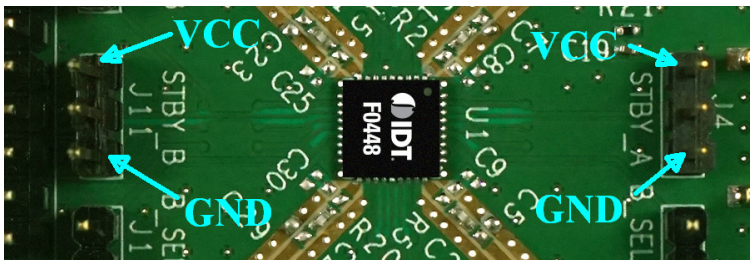


Figure 78. Two Standby Pin Connections

To place channel A in the normal operation mode (on), use one of these options:

- Make no connections on J4.
- Apply a logic LOW signal to STBY (pin 2 of J4 or the middle pin).
- Make a connection between pin 1 (GND) and pin 2 (STBY, the middle pin) of J4.

To place channel A in the standby mode (off), use one of these options:

- Apply a logic HIGH signal to the STBY (pin 2 of J4 or the middle pin).
- Make a connection between pin 3 (VCC) and pin 2 (STBY, the middle pin) of J4.

To place channel B in the normal operation mode (on), use one of these options:

- Make no connections on J11.
- Apply a logic LOW signal to STBY (pin 2 of J11 or the middle pin).
- Make a connection between pin 1 (GND) and pin 2 (STBY, the middle pin) of J11.

To place channel B in the standby mode (off), use one of these options:

- Apply a logic HIGH signal to the STBY (pin 2 of J11 or the middle pin).
- Make a connection between pin 3 (VCC) and pin 2 (STBY, the middle pin) of J11.

7.4.4. Serial Control

Both channels have a digital controlled attenuator, DSA1_A and DSA1_B, which share the serial control word. The serial control pins are on header J13 and are shown in Figure 79. Table 13 lists the pin functions on header J13.

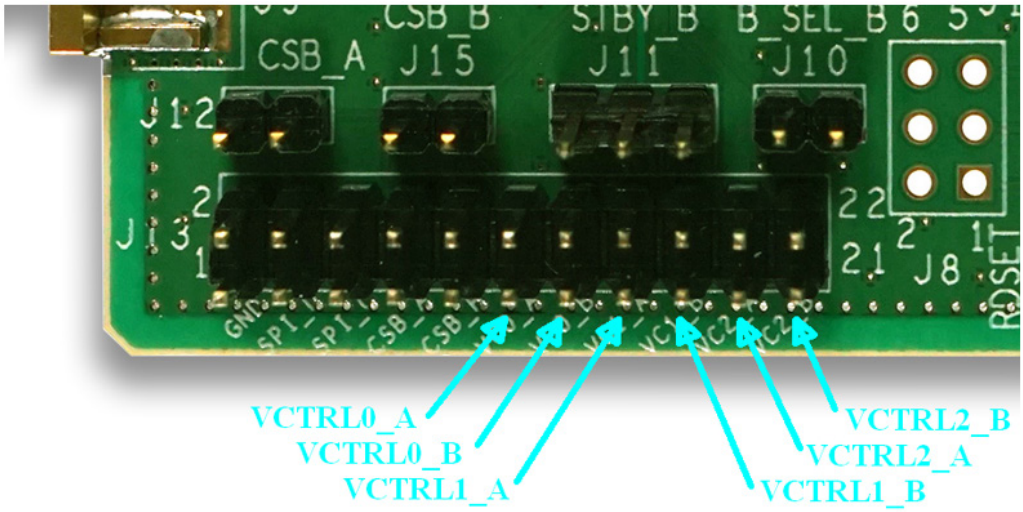


Figure 79. Two Jumpers for Serial Programming Connections

Table 13. J13 Header Pins

Pin	Label	Pin	Label
1	GND	2	GND
3	DATA	4	GND
5	CLK	6	GND
7	CSb_A	8	GND
9	CSb_B	10	GND
11	VCTRL0_A	12	GND
13	VCTRL0_B	14	GND
15	VCTRL1_A	16	GND
17	VCTRL1_B	18	GND
19	VCTRL2_A	20	GND
21	VCTRL2_B	22	GND

Each channel has its own latch pins, CSB_A and CSB_B (pin 7 of J13 and pin 9 of J13) so each channel attenuator can be independently controlled. If you only have one latch signal, the ability to control each channel attenuator achieved using headers J12 and J15. The latch signal must be applied to CSb_A (pin 7 of J13). Table 14 lists the operation for the connections on these headers. Figure 54 shows the J12 and J15 headers.

Table 14. Attenuator Control Using One Latch Signal

CSb_A (J12)	CSb_B (J15)	Function
OPEN	OPEN	No control of attenuators
OPEN	CLOSED	DSA1_B attenuator is controlled
CLOSED	OPEN	DSA1_A attenuator is controlled
CLOSED	CLOSED	DSA1_A attenuator is controlled DSA1_B attenuator is controlled

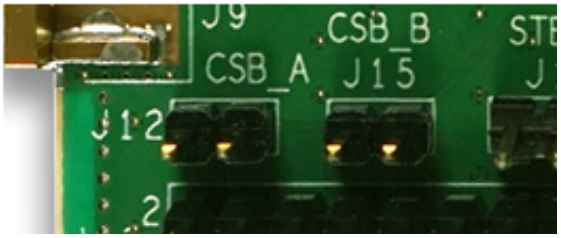


Figure 80. Jumpers for Serial Programming Connections

7.4.5. Parallel Control Pins

Both channels have two other attenuators, DSA0 and DSA2, which are parallel controlled. These parallel pins are located on header J13 shown in Figure 81. Table 14 lists the pin functions on header J13.

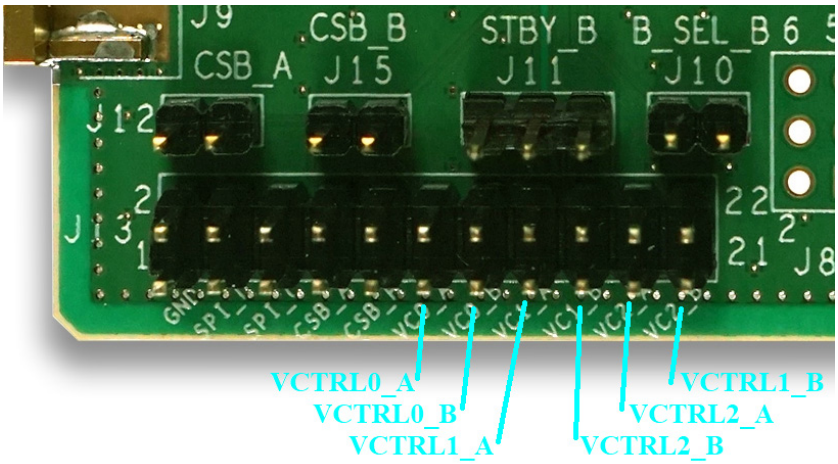


Figure 81. Parallel Pin Connections

See Table 8 and Table 9 for the attenuation control.

7.4.6. Power-On Procedure

Set up the voltage supplies and Evaluation Board as described in “Power Supply Setup” with the “Standby Pin” set for logic LOW, then enable the power supply.

7.4.7. Power-Off Procedure

Disable the power supply.

8. Application Information

The F0448 is optimized for use in high-performance RF applications from 3.3GHz to 4.2GHz.

8.1 Power Supplies

Bypass supply pins with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µS. In addition, all control pins should remain at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

8.2 RSET and RDSET

The F0448 is optimized for gain and intermodulation products by adjusting the bias resistors RSET and RDSET. For the optimized setting, RSET (R26) and RDSET (R25) are 4.42kΩ.

8.3 Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 3-7, 11-14, and 32-35 as shown below. Note the recommended resistor and capacitor values do not necessarily match the EVKit BOM for the case of poor control signal integrity.

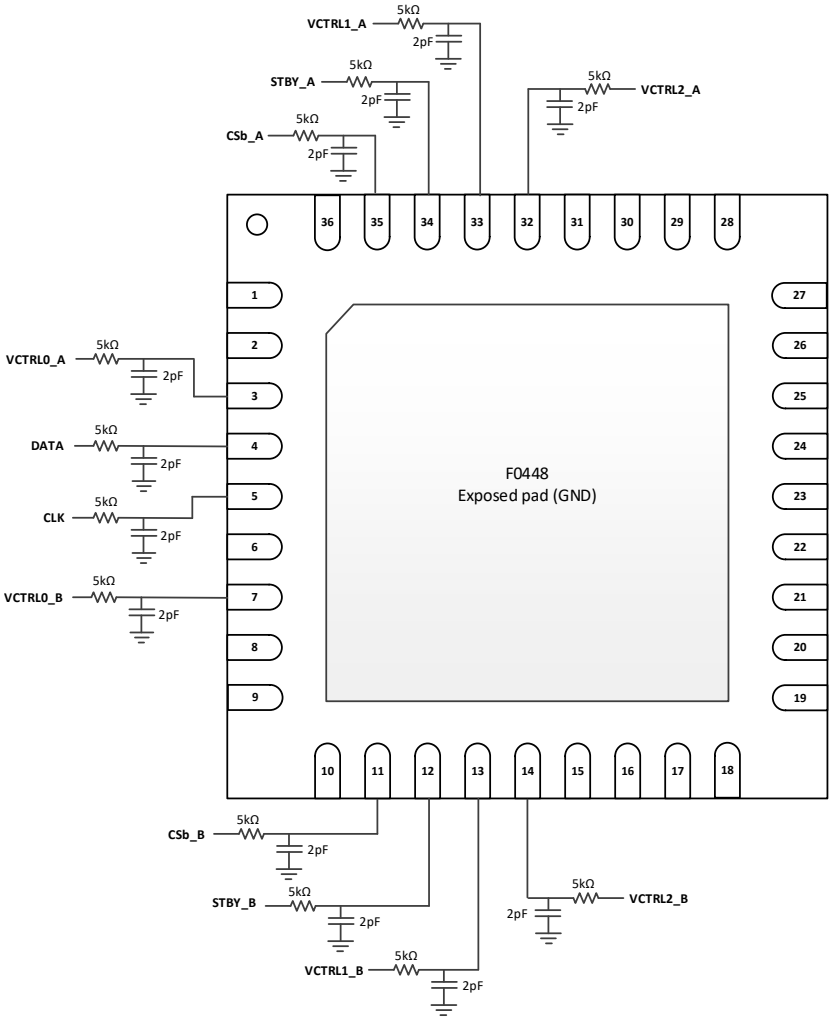


Figure 82. Control Pin Interface

9. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

10. Marking Diagram

- Line 1 and 2 are the part number.
- Line 3 “ZW” is for die version.
- Line 3 “yyww = 1707 has two digits for the year and week that the part was assembled.
- Line 3 “L” denotes Assembly Site.
- Line 4 “Q86A034MY” is the Assembly Lot number.

11. Ordering Information

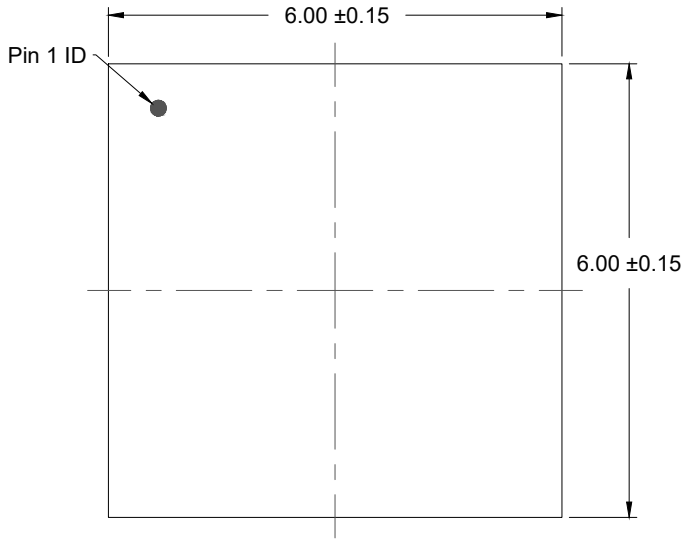
Orderable Part Number	Package Description	MSL Rating	Carrier Type	Temperature
F0448NBGK	6 × 6 × 0.75 mm, 36-QFN	1	Tray	-40°C to +105°C
F0448NBGK8	6 × 6 × 0.75 mm, 36-QFN	1	Tape and Reel	-40°C to +105°C
F0448EVB	Evaluation Board			
F0448EVS	Evaluation Solution			

12. Revision History

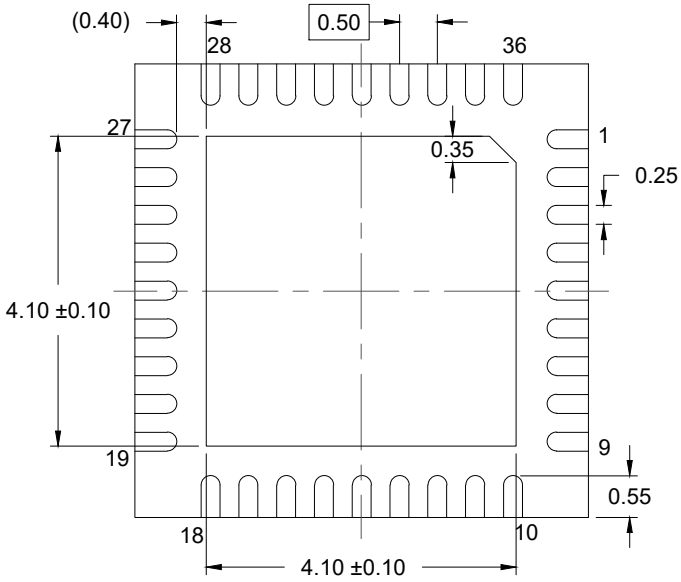
Revision	Date	Description
1.4	Feb 17, 2021	▪ Updated spec table, plots, and BOM for wideband frequency tune ▪ Added Plots and a BOM for wide band operation of the device from 3.3GHz to 4.2GHz. The Operating Range has also been appropriately adjusted. ▪ Updated the document to the latest template
1.3	Oct 24, 2018	▪ Removed “or pin open” from Pin Descriptions ▪ Removed “or open” from Table 8 and Table 9 ▪ Updated Figure 79
1.2	Oct 18, 2018	▪ Updated various logic levels ▪ Update Typical Performance Characteristics ▪ Completed other minor improvements
1.1	Aug 29, 2018	Added θ_{JA} and $\theta_{JC\text{-}BOT}$ values to Table 5
1.0	Aug 8, 2018	Initial release.

Package Outline Drawing

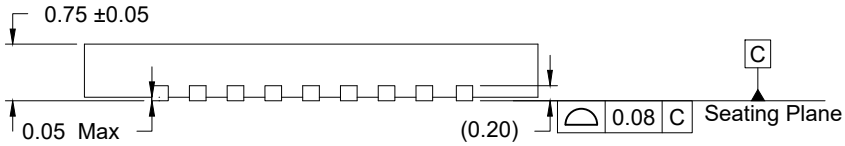
Package Code: NBG36P2
36-VFQFPN 6.0 x 6.0 x 0.75 mm Body, 0.5mm Pitch
PSC-4311-02, Revision: 02, Date Created: Oct 9, 2024



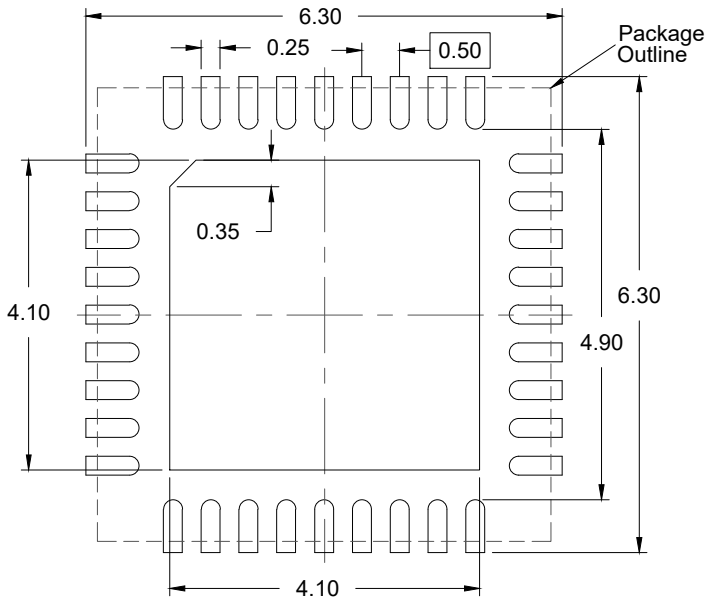
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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