

# HCS138MS

Radiation Hardened Inverting 3-to-8 Line Decoder/Demultiplexer

FN2473  
Rev 3.01  
Feb 24, 2022

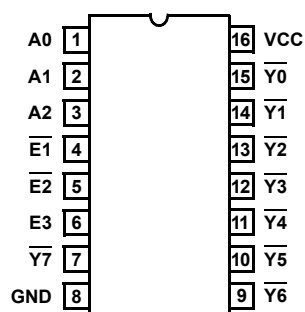
The [HCS138MS](#) is a Radiation Hardened 3-to-8 line Decoder/Demultiplexer. The outputs are active in the low state. Two active low and one active high enables ( $\overline{E1}$ ,  $\overline{E2}$ ,  $E3$ ) are provided. If the device is enabled, the binary inputs ( $A0$ ,  $A1$ ,  $A2$ ) determine which one of the eight normally high outputs will go to a low logic level.

The HCS138MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

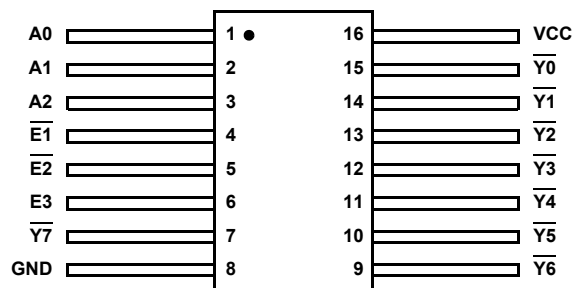
The HCS138MS is supplied in a 16 lead Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

## Pinouts

**16 LEAD CERAMIC DUAL-IN-LINE  
METAL SEAL PACKAGE (SBDIP)  
MIL-STD-1835 CDIP2-T16  
TOP VIEW**



**16 LEAD CERAMIC METAL SEAL  
FLATPACK PACKAGE (FLATPACK)  
MIL-STD-1835 CDFP4-F16  
TOP VIEW**



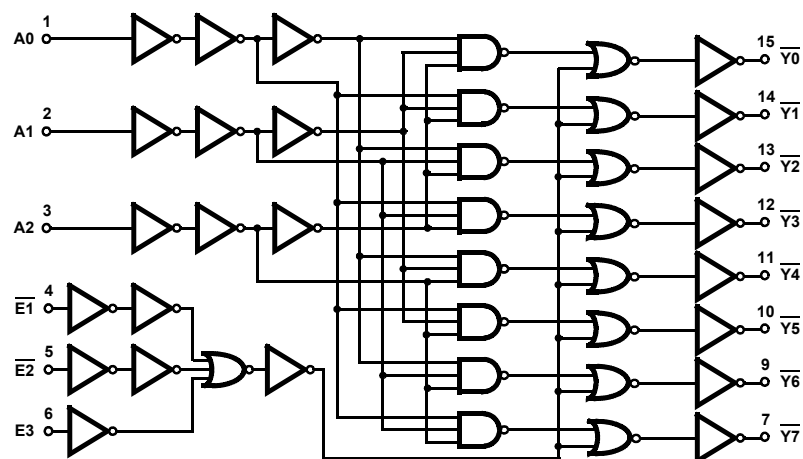
## Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K RAD (Si)
- SEP Effective LET No Upsets: >100 MEV-cm<sup>2</sup>/mg
- Single Event Upset (SEU) Immunity < 2 x 10<sup>-9</sup> Errors/Bit-Day (Typ)
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs - 10 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - $V_{IL}$  = 0.3 VCC Max
  - $V_{IH}$  = 0.7 VCC Min
- Input Current Levels  $I_i \leq 5\mu A$  at VOL, VOH

## Ordering Information

PART NUMBER	TEMP RANGE	SCREENING LEVEL	PACKAGE
HCS138DMSR	-55°C to +125°C	Renesas Class S Equivalent	16 Lead SBDIP
HCS138KMSR	-55°C to +125°C	Renesas Class S Equivalent	16 Lead Ceramic Flatpack
HCS138HMSR	+25°C	Die	Die

## Functional Diagram



TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE													
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don't Care

**Absolute Maximum Ratings**

Supply Voltage (VCC)	-0.5V to +7.0V
Input Voltage Range, All Inputs	-0.5V to VCC +0.5V
DC Input Current, Any One Input	±10mA
DC Drain Current, Any One Output (All Voltage Reference to the VSS Terminal)	±25mA
Storage Temperature Range (TSTG)	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+265°C
Junction Temperature (TJ)	+175°C
ESD Classification	Class 1

**Reliability Information**

Thermal Resistance	$\theta_{JA}$	$\theta_{JC}$
SBDIP Package . . . . .	73°C/W	24°C/W
Ceramic Flatpack Package . . . . .	114°C/W	29°C/W
Maximum Package Power Dissipation at +125°C Ambient		
SBDIP Package . . . . .	0.68W	
Ceramic Flatpack Package . . . . .	0.44W	
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:		
SBDIP Package . . . . .	13.7mW/°C	
Ceramic Flatpack Package . . . . .	8.8mW/°C	

**CAUTION:** As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

**Operating Conditions**

Supply Voltage	+4.5V to +5.5V	Input Low Voltage (VIL)	0.0V to 30% of VCC
Input Rise and Fall Times at VCC = 4.5V (TR, TF)	500ns Max	Input High Voltage (VIH)	70% of VCC to VCC
Operating Temperature Range (TA)	-55°C to +125°C		

**TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	μA
			2, 3	+125°C, -55°C	-	750	μA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50μA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50μA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50μA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC - 0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50μA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC - 0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	μA
			2, 3	+125°C, -55°C	-	±5.0	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

**NOTES:**

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Address to Output	TPLH	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	34	ns
	TPHL	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	34	ns
Enable to Output	TPLH	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	33	ns
	TPHL	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	33	ns

## NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume  $R_L = 500\Omega$ ,  $C_L = 50\text{pF}$ , Input  $T_R = T_F = 3\text{ns}$ ,  $V_{IL} = \text{GND}$ ,  $V_{IH} = V_{CC}$ .

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	-	78	pF
			1	+125°C	-	113	pF
Input Capacitance	CIN	VCC = 5.0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

## NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP.	200K RAD LIMITS		UNITS
				MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC - 0.4V	+25°C	-6.0	-	mA

**TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)**

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP.	200K RAD LIMITS		UNITS
				MIN	MAX	
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), IOL = 50 $\mu$ A	+25°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), IOH = -50 $\mu$ A	+25°C	VCC - 0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	$\pm$ 5	$\mu$ A
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), (Note 3)	+25°C	-	-	-
Address to Output	TPLH	VCC = 4.5V	+25°C	2	34	ns
	TPHL	VCC = 4.5V	+25°C	2	34	ns
Enable to Output	TPLH	VCC = 4.5V	+25°C	2	33	ns
	TPHL	VCC = 4.5V	+25°C	2	33	ns

## NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500 $\Omega$ , CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO  $\geq$  4.0V is recognized as a logic "1", and VO  $\leq$  0.5V is recognized as a logic "0".

**TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)**

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12 $\mu$ A
IOL/IOH	5	-15% of 0 Hour

**TABLE 6. APPLICABLE SUBGROUPS**

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 7, 9	

## NOTE:

1. Alternate group A inspection in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
7, 9 - 15	1 - 6, 8		16		
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
7, 9 - 15	8	-	1 - 6, 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	4, 5, 8	7, 9 - 15	3, 6, 16	2	1

NOTES:

1. Each pin except VCC and GND will have a resistor of  $10K\Omega \pm 5\%$  for static burn-in
2. Each pin except VCC and GND will have a resistor of  $680\Omega \pm 5\%$  for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
7, 9 - 15	8	1 - 6, 16

NOTE: Each pin except VCC and GND will have a resistor of  $47K\Omega \pm 5\%$  for irradiation testing.  
Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

## Space Level Product Flow - 'MS'

Wafer Lot Acceptance (All Lots) Method 5007  
(Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019,  
4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C,  
10 Cycles

100% Constant Acceleration, Method 2001, Condition per  
Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 24 hrs. min.,  
+125°C min., Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% Static Burn-In 2, Condition A or B, 24 hrs. min.,  
+125°C min., Method 1015

100% Interim Electrical Test 2 (T2)

100% Delta Calculation (T0-T2)

100% PDA 1, Method 5004 (Notes 1 and 2)

100% Dynamic Burn-In, Condition D, 240 hrs., +125°C or  
Equivalent, Method 1015

100% Interim Electrical Test 3 (T3)

100% Delta Calculation (T0-T3)

100% PDA 2, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic, Method 2012 (Note 3)

100% External Visual, Method 2009

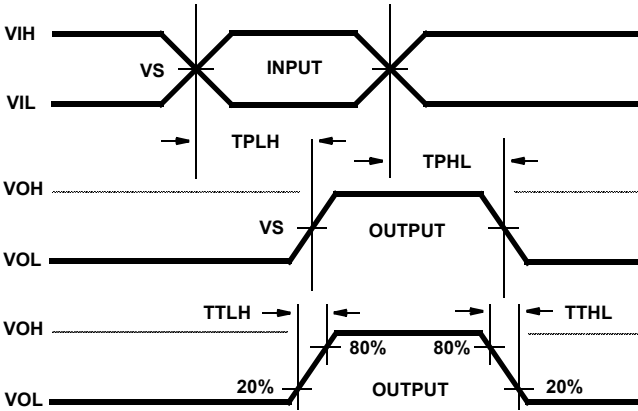
Sample - Group A, Method 5005 (Note 4)

100% Data Package Generation (Note 5)

### NOTES:

1. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
2. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Data Package Contents:
  - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Part Number, Lot Number, Quantity).
  - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
  - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Renesas.
  - X-Ray report and film. Includes penetrometer measurements.
  - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
  - Lot Serial Number Sheet (Good units serial number and lot number).
  - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
  - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

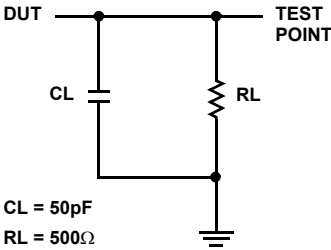
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit





**Die Characteristics****DIE DIMENSIONS:**

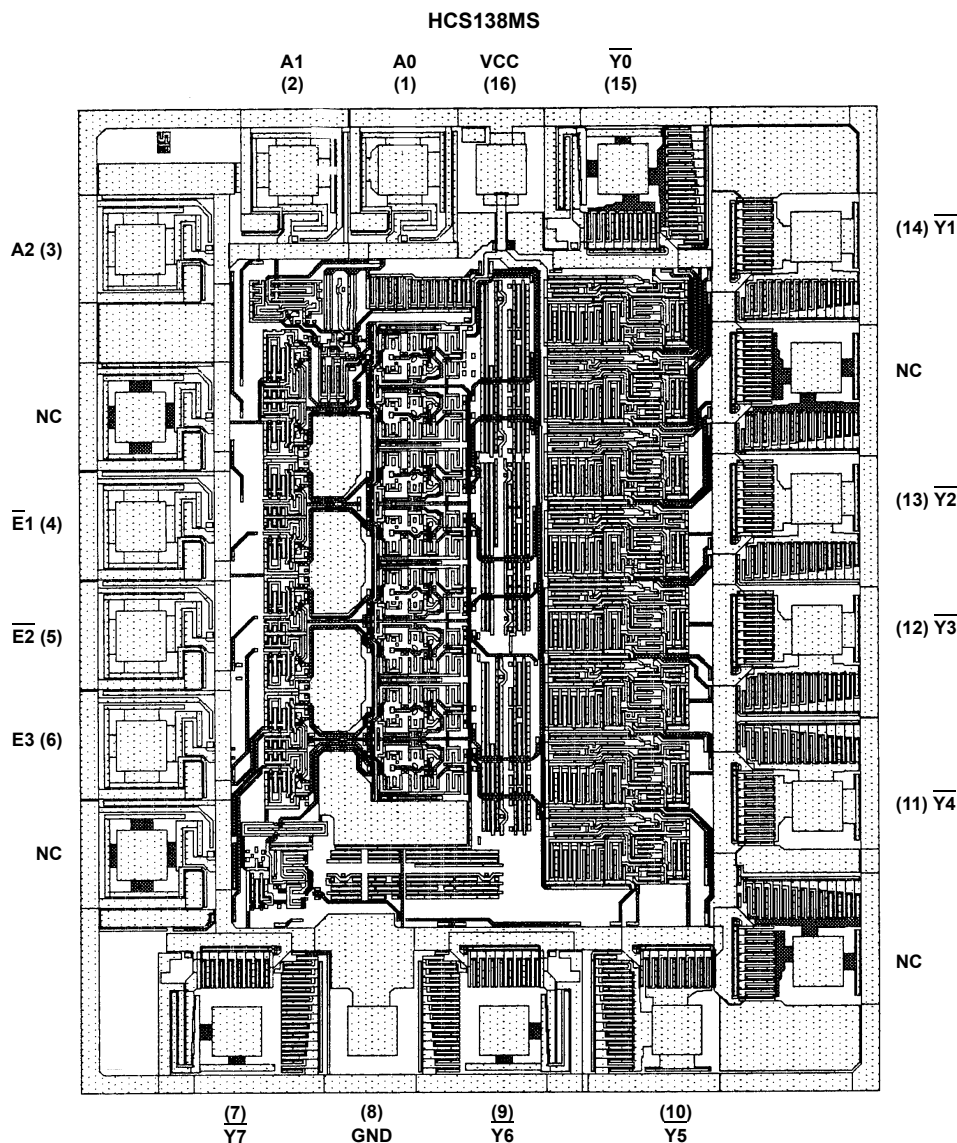
85 x 101 mils

**METALLIZATION:**

Type: SiAl

Metal Thickness:  $11\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$ **GLASSIVATION:**Type:  $\text{SiO}_2$ Thickness:  $13\text{k}\text{\AA} \pm 2.6\text{k}\text{\AA}$ **WORST CASE CURRENT DENSITY:** $<2.0 \times 10^5 \text{A/cm}^2$ **BOND PAD SIZE:** $100\mu\text{m} \times 100\mu\text{m}$ 

4 x 4 mils

**Metallization Mask Layout**

NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCS138 is TA14361A.

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## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Feb 24, 2022	3.01	Updated the Functional Diagram. Added Revision History section.

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(Rev.1.0 Mar 2020)

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