To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74AC107/HD74ACT107

Dual JK Flip-Flop (with Separate Clear and Clock)

REJ03D0243–0200Z
(Previous ADE-205-363 (Z))
Rev.2.00
Jul.16.2004

Description

The HD74AC107/HD74ACT107 dual JK master/slave flip-flops have a separate clock for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from J and K inputs to master; 3) disable J and K inputs; 4) transfer information from master to slave.

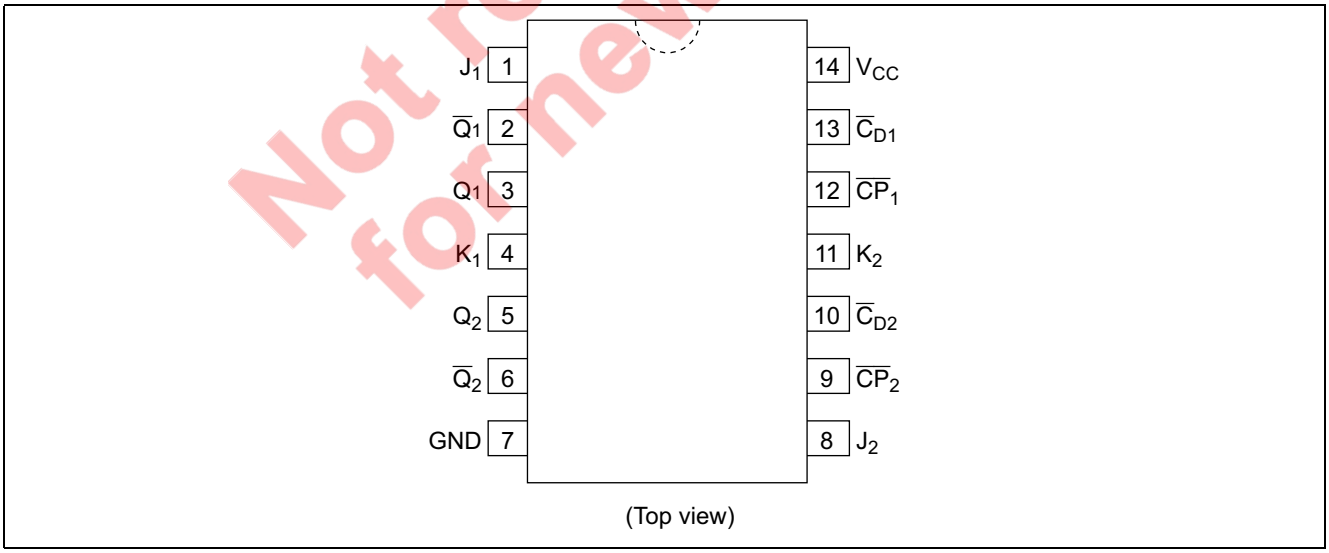
Features

- Outputs Source/Sink 24 mA
- HD74ACT107 has TTL-Compatible Inputs
- Ordering Information: Ex. HD74AC107

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC107FPEL	SOP-14 pin (JEITA)	FP-14DAV	FP	EL (2,000 pcs/reel)
HD74AC107RPEL	SOP-14 pin (JEDEC)	FP-14DNV	RP	EL (2,500 pcs/reel)

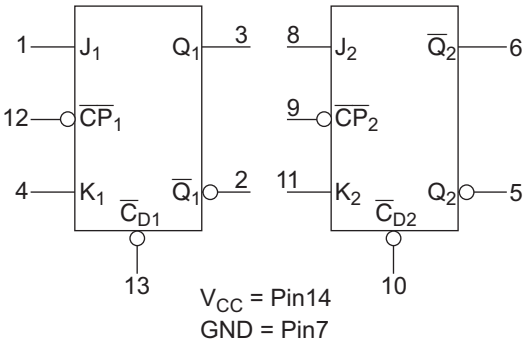
Notes: 1. Please consult the sales office for the above package availability.
2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



(Top view)

Logic Symbol



Pin Names

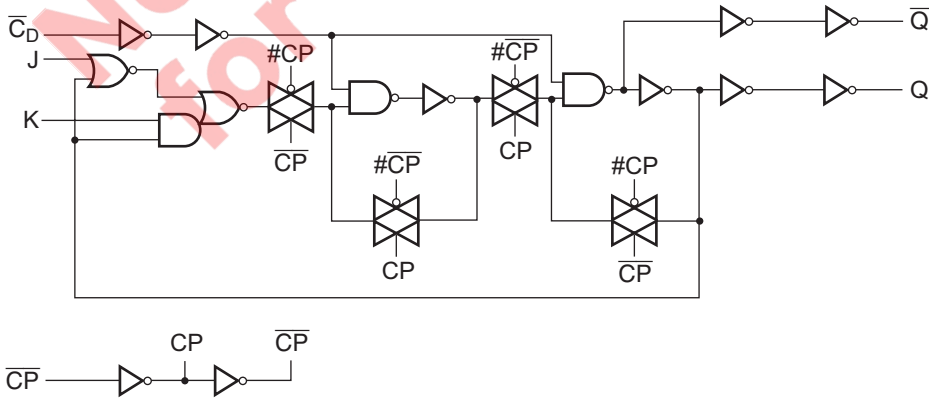
J_1, J_2, K_1, K_2	Data Inputs
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active Low)
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs

Truth Table

Inputs		Outputs
@ t_n		@ t_{n+1}
J	**K**	**Q**
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Q}$n

H : High Voltage Level
L : Low Voltage Level
t_n : Bit time before clock pulse.
t_{n+1} : Bit time after clock pulse.

Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	–0.5 to 7	V	
DC input diode current	I_{IK}	–20	mA	V_I = –0.5V
		20	mA	V_I = Vcc+0.5V
DC input voltage	V_I	–0.5 to Vcc+0.5	V	
DC output diode current	I_{OK}	–50	mA	V_O = –0.5V
		50	mA	V_O = Vcc+0.5V
DC output voltage	V_O	–0.5 to Vcc+0.5	V	
DC output source or sink current	I_O	±50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	±50	mA	
Storage temperature	Tstg	–65 to +150	°C	

Recommended Operating Conditions: HD74AC107

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	tr, tf	8	ns/V	V_{CC} = 3.0V
				V_{CC} = 4.5 V
				V_{CC} = 5.5 V

DC Characteristics: HD74AC107

Item	Sym-bol	Vcc (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input Voltage	V_{IH}	3.0	2.1	1.5	—	2.1	—	V	V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	3.15	2.25	—	3.15	—			
		5.5	3.85	2.75	—	3.85	—			
	V_{IL}	3.0	—	1.50	0.9	—	0.9		V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	—	2.25	1.35	—	1.35			
		5.5	—	2.75	1.65	—	1.65			
Output voltage	V_{OH}	3.0	2.9	2.99	—	2.9	—	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = –50 µA	
		4.5	4.4	4.49	—	4.4	—			
		5.5	5.4	5.49	—	5.4	—			
		3.0	2.58	—	—	2.48	—		V_{IN} = V_{IL} or V_{IH}	I_{OH} = –12 mA
		4.5	3.94	—	—	3.80	—			I_{OH} = –24 mA
		5.5	4.94	—	—	4.80	—			I_{OH} = –24 mA
	V_{OL}	3.0	—	0.002	0.1	—	0.1		V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 µA	
		4.5	—	0.001	0.1	—	0.1			
		5.5	—	0.001	0.1	—	0.1			
		3.0	—	—	0.32	—	0.37		V_{IN} = V_{IL} or V_{IH}	I_{OL} = 12 mA
		4.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
		5.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
Input leakage current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	V_{OLD} = 1.1 V	
	I_{OHD}	5.5	—	—	—	–75	—	mA	V_{OHD} = 3.85 V	
Quiescent supply current	I_{CC}	5.5	—	—	4.0	—	40	µA	V_{IN} = V_{CC} or ground	

*Maximum test duration 2.0 ms, one output loaded at a time.

Recommended Operating Conditions: HD74ACT107

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 0.8 to 2.0 V	tr, tf	8	ns/V	V_{CC} = 4.5V V_{CC} = 5.5V

DC Characteristics: HD74ACT107

Item	Sym-bol	V_{CC} (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input voltage	V_{IH}	4.5	2.0	1.5	—	2.0	—	V	V_{OUT} = 0.1 V or Vcc–0.1 V	
		5.5	2.0	1.5	—	2.0	—			
	V_{IL}	4.5	—	1.5	0.8	—	0.8		V_{OUT} = 0.1 V or Vcc–0.1 V	
		5.5	—	1.5	0.8	—	0.8			
Output voltage	V_{OH}	4.5	4.4	4.49	—	4.4	—	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = –50 µA	
		5.5	5.4	5.49	—	5.4	—			
		4.5	3.94	—	—	3.80	—		V_{IN} = V_{IL}	I_{OH} = –24 mA
		5.5	4.94	—	—	4.80	—			I_{OH} = –24 mA
	V_{OL}	4.5	—	0.001	0.1	—	0.1		V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 µA	
		5.5	—	0.001	0.1	—	0.1			
		4.5	—	—	0.32	—	0.37		V_{IN} = V_{IL}	I_{OL} = 24 mA
		5.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
Input current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
I_{CC}/input current	I_{CCT}	5.5	—	0.6	—	—	1.5	mA	V_{IN} = V_{CC}–2.1 V	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	V_{OLD} = 1.1 V	
	I_{OHD}	5.5	—	—	—	–75	—	mA	V_{OHD} = 3.85 V	
Quiescent supply current	I_{CC}	5.5	—	—	4.0	—	40	µA	V_{IN} = V_{CC} or ground	

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics: HD74AC107

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	3.3	125	—	—	100	—	MHz
		5.0	150	—	—	125	—	
Propagation delay $\overline{C_P}$ to Q or $\overline{Q}$	t_{PLH}	3.3	1.0	9.5	13.0	1.0	14.0	ns
		5.0	1.0	7.5	10.0	1.0	11.0	
Propagation delay $\overline{C_P}$ to Q or $\overline{Q}$	t_{PHL}	3.3	1.0	10.0	13.5	1.0	14.5	ns
		5.0	1.0	8.0	10.5	1.0	11.5	
Propagation delay $\overline{C_D}$ to $\overline{Q}$	t_{PLH}	3.3	1.0	9.5	13.0	1.0	14.0	ns
		5.0	1.0	7.5	10.0	1.0	11.0	
Propagation delay $\overline{C_D}$ to $\overline{Q}$	t_{PHL}	3.3	1.0	9.5	13.0	1.0	14.0	ns
		5.0	1.0	7.5	10.0	1.0	11.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Operating Requirements: HD74AC107

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF		Ta = –40°C to +85°C, C_L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time J or k to $\overline{C}_P$	t_{su}	3.3	3.0	5.5	6.0	ns
		5.0	2.0	4.0	4.5	
Hold time $\overline{C}_P$ to J or k	t_h	3.3	–1.5	0.0	0.0	
		5.0	–0.5	0.0	0.0	
Pulse width $\overline{C}_P$ or $\overline{C}_D$	t_w	3.3	2.0	5.5	7.0	
		5.0	2.0	4.5	5.0	
Recovery time $\overline{C}_D$ to $\overline{C}_P$	t_{rec}	3.3	1.5	3.0	3.0	
		5.0	1.0	3.0	3.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT107

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF			Ta = –40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	5.0	100	—	—	80	—	MHz
Propagation delay $\overline{C}_P$ to Q or $\overline{Q}$	t_{PLH}	5.0	1.0	9.5	12.5	1.0	13.5	ns
Propagation delay $\overline{C}_P$ to Q or $\overline{Q}$	t_{PHL}	5.0	1.0	10.5	13.0	1.0	14.0	
Propagation delay $\overline{C}_D$ to $\overline{Q}$	t_{PLH}	5.0	1.0	8.5	11.0	1.0	12.0	
Propagation delay $\overline{C}_D$ to Q	t_{PHL}	5.0	1.0	8.5	11.0	1.0	12.0	

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Operating Requirements: HD74ACT107

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF		Ta = –40°C to +85°C, C_L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time J or k to $\overline{C}_P$	t_{su}	5.0	2.5	7.0	8.0	ns
Hold time $\overline{C}_P$ to J or k	t_h	5.0	0.0	1.5	1.5	
Pulse width $\overline{C}_P$ or $\overline{C}_D$	t_w	5.0	4.5	7.0	8.0	
Recovery time $\overline{C}_D$ to $\overline{C}_P$	t_{rec}	5.0	—	3.0	3.0	

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

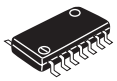
Capacitance

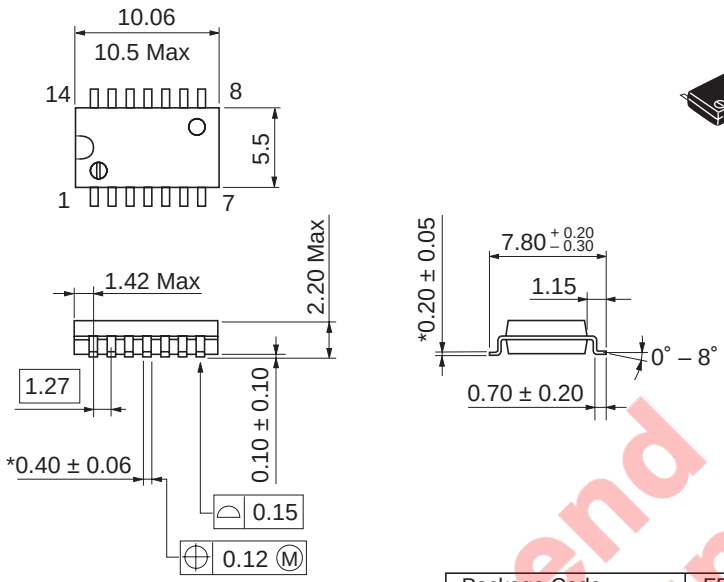
Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	35.0	pF	V_{CC} = 5.0 V

Package Dimensions

As of January, 2003

Unit: mm



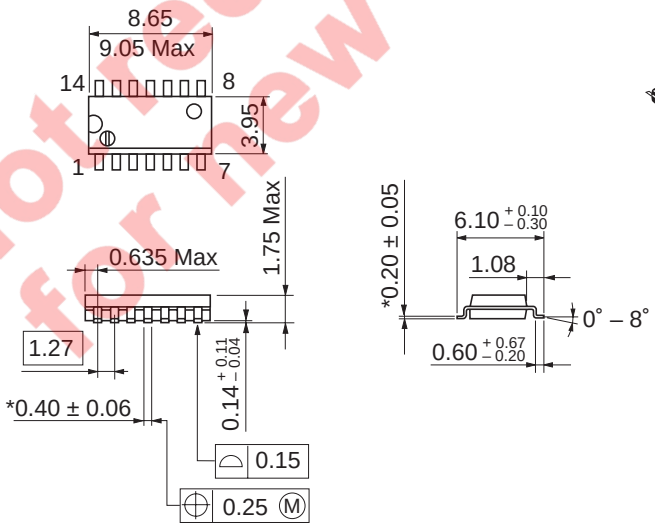


Package Code	FP-14DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.23 g

*Ni/Pd/Au plating

As of January, 2003

Unit: mm



Package Code	FP-14DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.13 g

*Ni/Pd/Au plating

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