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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HD74ALVCH162830

## 1-bit to 2-bit Address Driver with 3-state Outputs

REJ03D0040-0200Z  
(Previous ADE-205-197(Z))  
Rev.2.00  
Oct.02.2003

### Description

This 1-bit to 2-bit address driver is designed for 2.3 V to 3.6 V  $V_{CC}$  operation. To ensure the high impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current sinking capability of the driver. Active bus hold circuitry is provided to hold unused or floating inputs at a valid logic level. All outputs, which are designed to sink up to 12 mA, include equivalent 26  $\Omega$  resistors to reduce overshoot and undershoot.

### Features

- $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$
- Typical  $V_{OL}$  ground bounce  $< 0.8 \text{ V}$  ( $@V_{CC} = 3.3 \text{ V, } T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot  $> 2.0 \text{ V}$  ( $@V_{CC} = 3.3 \text{ V, } T_a = 25^\circ\text{C}$ )
- High output current  $\pm 12 \text{ mA}$  ( $@V_{CC} = 3.0 \text{ V}$ )
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors
- All outputs have equivalent 26  $\Omega$  series resistors, so no external resistors are required

**Function Table**

Inputs			Outputs	
$\overline{OE1}$	$\overline{OE2}$	A	1Yn	2Yn
L	H	H	H	Z
L	H	L	L	Z
H	L	H	Z	H
H	L	L	Z	L
L	L	H	H	H
L	L	L	L	L
H	H	X	Z	Z

H : High level

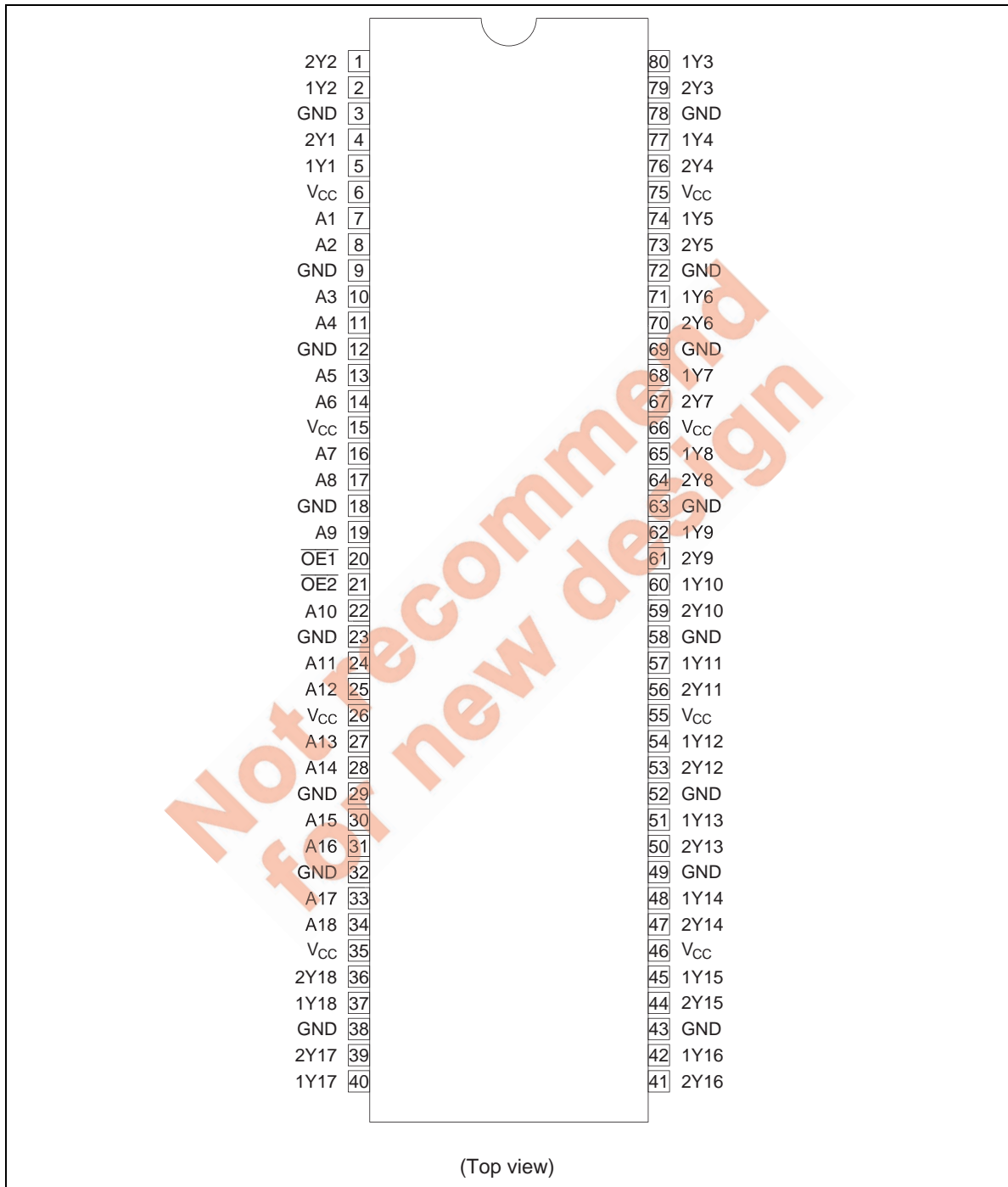
L : Low level

X : Immaterial

Z : High impedance

Not recommended  
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## Pin Arrangement



**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	−0.5 to 4.6	V	
Input voltage <sup>*1</sup>	$V_I$	−0.5 to 4.6	V	
Output voltage <sup>*1, 2</sup>	$V_O$	−0.5 to $V_{CC} + 0.5$	V	
Input clamp current	$I_{IK}$	−50	mA	$V_I < 0$
Output clamp current	$I_{OK}$	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	±50	mA	$V_O = 0$ to $V_{CC}$
$V_{CC}$ , GND current / pin	$I_{CC}$ or $I_{GND}$	±100	mA	
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) <sup>*3</sup>	$P_T$	1	W	TVSOP
Storage temperature	$T_{stg}$	−65 to 150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

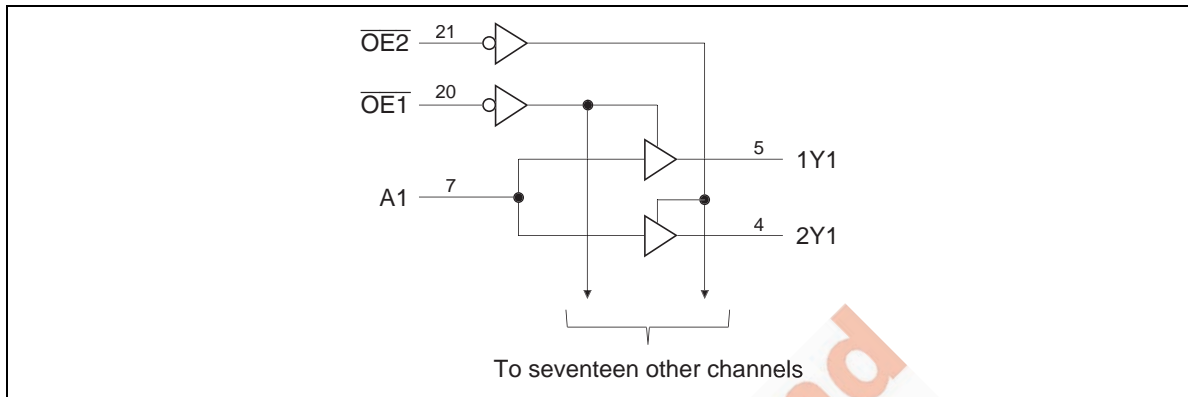
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils.

**Recommended Operating Conditions**

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	$V_{CC}$	2.3	3.6	V	
Input voltage	$V_I$	0	$V_{CC}$	V	
Output voltage	$V_O$	0	$V_{CC}$	V	
High level output current	$I_{OH}$	—	−6	mA	$V_{CC} = 2.3\text{ V}$
		—	−8		$V_{CC} = 2.7\text{ V}$
		—	−12		$V_{CC} = 3.0\text{ V}$
Low level output current	$I_{OL}$	—	6	mA	$V_{CC} = 2.3\text{ V}$
		—	8		$V_{CC} = 2.7\text{ V}$
		—	12		$V_{CC} = 3.0\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	$T_a$	−40	85	°C	

Note: Unused control inputs must be held high or low to prevent them from floating.

## Logic Diagram



## Electrical Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V <sub>IL</sub>	2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
Output voltage	V <sub>OH</sub>	2.3 to 3.6	V <sub>CC</sub> -0.2	—	V	I <sub>OH</sub> = -100 µA
		2.3	1.9	—		I <sub>OH</sub> = -4 mA, V <sub>IH</sub> = 1.7 V
		2.3	1.7	—		I <sub>OH</sub> = -6 mA, V <sub>IH</sub> = 1.7 V
		3.0	2.4	—		I <sub>OH</sub> = -6 mA, V <sub>IH</sub> = 2.0 V
		2.7	2.0	—		I <sub>OH</sub> = -8 mA, V <sub>IH</sub> = 2.0 V
		3.0	2.0	—		I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2.0 V
	V <sub>OL</sub>	2.3 to 3.6	—	0.2		I <sub>OL</sub> = 100 µA
		2.3	—	0.4		I <sub>OL</sub> = 4 mA, V <sub>IL</sub> = 0.7 V
		2.3	—	0.55		I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.7 V
		3.0	—	0.55		I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.8 V
		2.7	—	0.6		I <sub>OL</sub> = 8 mA, V <sub>IL</sub> = 0.8 V
		3.0	—	0.8		I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.8 V
	I <sub>IN</sub>	3.6	—	±5		V <sub>IN</sub> = V <sub>CC</sub> or GND
		I <sub>IN</sub> (hold)	2.3	45		V <sub>IN</sub> = 0.7 V
			2.3	-45		V <sub>IN</sub> = 1.7 V
			3.0	75		V <sub>IN</sub> = 0.8 V
			3.0	-75		V <sub>IN</sub> = 2.0 V
			3.6	—		V <sub>IN</sub> = 0 to 3.6 V <sup>*1</sup>
Off state output current	I <sub>OZ</sub>	3.6	—	±10	µA	V <sub>OUT</sub> = V <sub>CC</sub> or GND
Quiescent supply current	I <sub>CC</sub>	3.6	—	40	µA	V <sub>IN</sub> = V <sub>CC</sub> or GND
	ΔI <sub>CC</sub>	3.0 to 3.6	—	750	µA	V <sub>IN</sub> = one input at (V <sub>CC</sub> -0.6) V, other inputs at V <sub>CC</sub> or GND

Note: 1. This is the bus hold maximum dynamic current required to switch the input from one state to another.

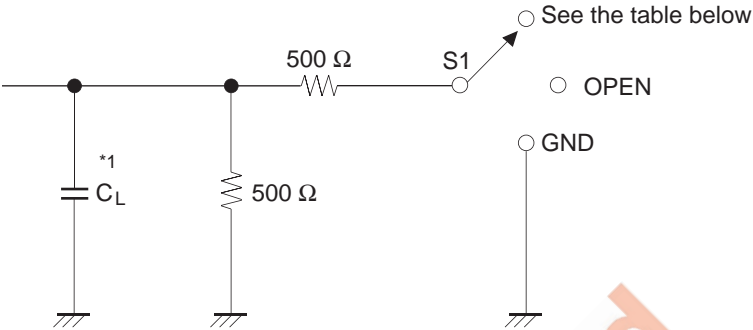


## Switching Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Propagation delay time	t <sub>PLH</sub>	2.5±0.2	1.2	—	3.8	ns	A	Y
	t <sub>PHL</sub>	2.7	—	—	4.0			
		3.3±0.3	1.7	—	3.5			
Output enable time	t <sub>ZH</sub>	2.5±0.2	1.0	—	5.7	ns	$\overline{\text{OE}}$	Y
	t <sub>ZL</sub>	2.7	—	—	5.7			
		3.3±0.3	1.0	—	4.8			
Output disable time	t <sub>HZ</sub>	2.5±0.2	1.5	—	6.2	ns	$\overline{\text{OE}}$	Y
	t <sub>LZ</sub>	2.7	—	—	5.4			
		3.3±0.3	1.7	—	5.2			
Input capacitance	C <sub>IN</sub>	3.3	—	4.5	—	pF	Control inputs	
		3.3	—	5.0	—		Data inputs	
Output capacitance	C <sub>O</sub>	3.3	—	7.5	—	pF		

Test Circuit

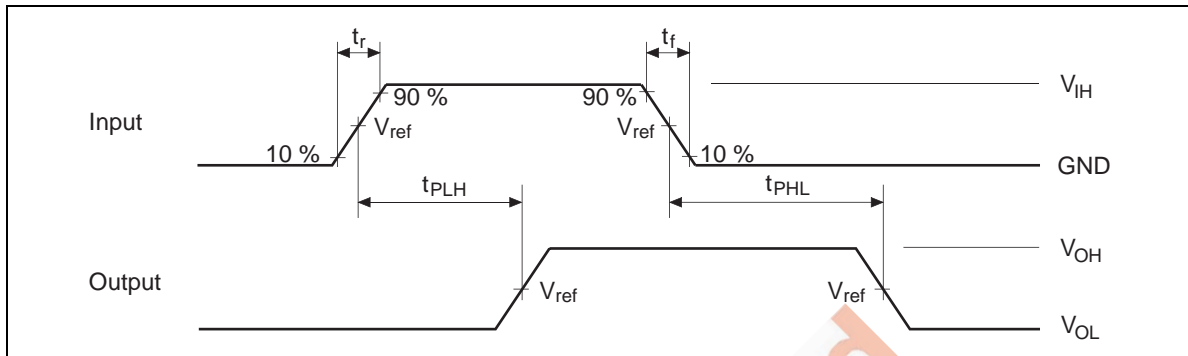


Load Circuit for Outputs

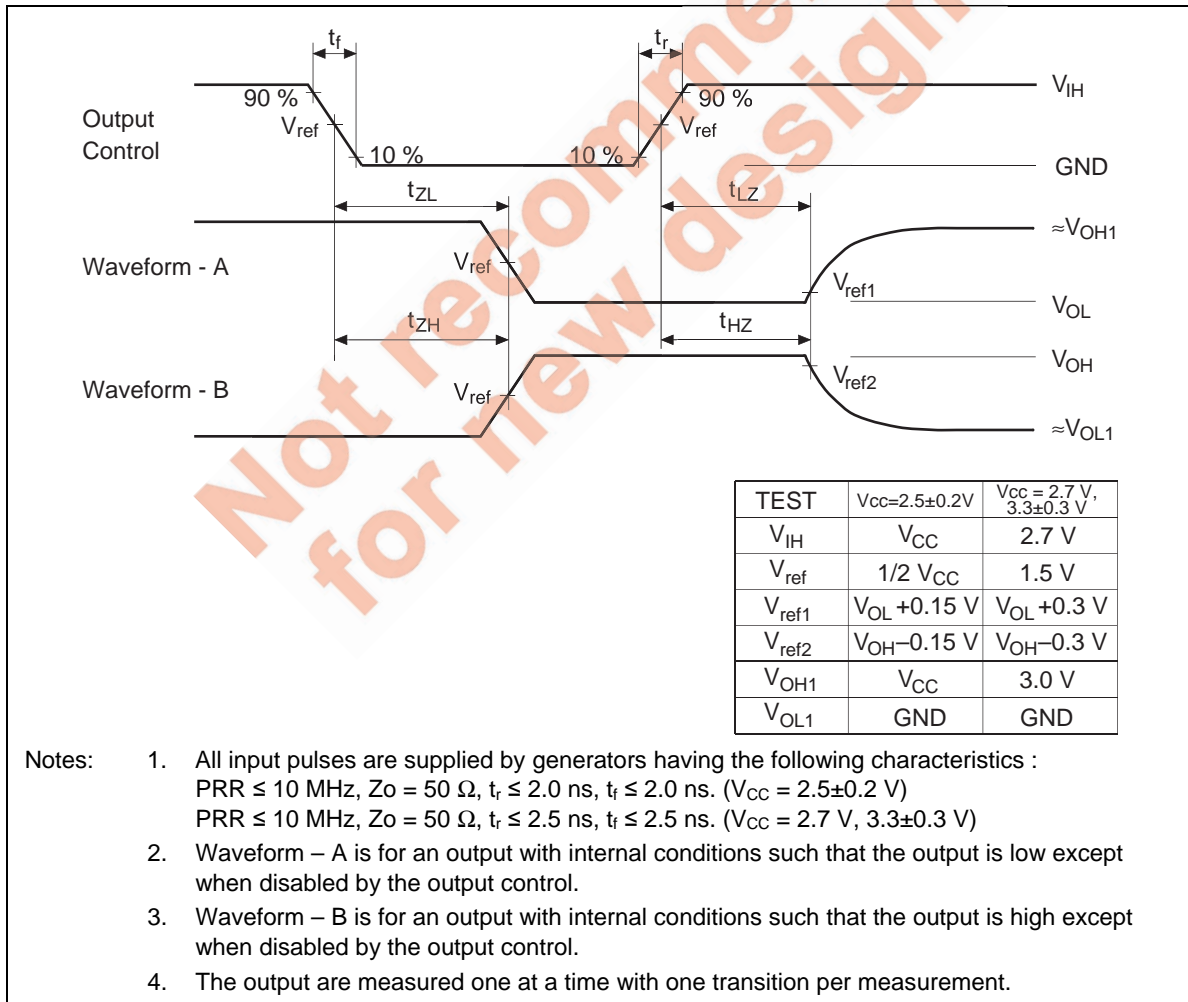
Symbol	$V_C = 2.5 \pm 0.2 \text{ V}$	$V_{CC} = 2.7 \text{ V}, 3.3 \pm 0.3 \text{ V}$
$t_{PLH} / t_{PHL}$	OPEN	OPEN
$t_{ZH} / t_{HZ}$	GND	GND
$t_{ZL} / t_{LZ}$	$2 \times V_{CC}$	6.0 V
$C_L$	30 pF	50 pF

Note: 1.  $C_L$  includes probe and jig capacitance.

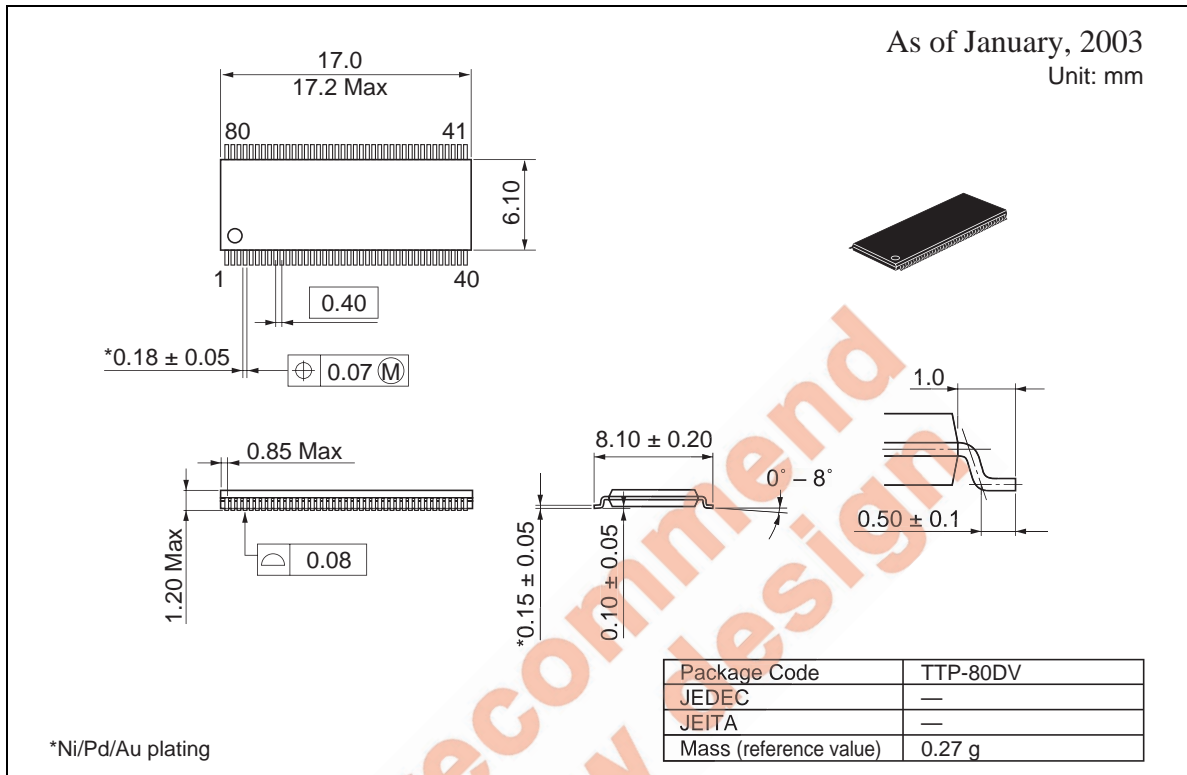
## Waveforms - 1



## Waveforms - 2



## Package Dimensions



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