To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74HC173

4-bit D-type Register (with 3-state outputs)

REJ03D0583-0300
Rev.3.00
Jan 31, 2006

Description

The four D type Flip-Flops operate synchronously from a common clock. The 3-state outputs allow the device to be used in bus organized systems. The outputs are placed in the 3-stage mode when either of the output disable pins are in the logic high level.

The input disable allows the flip-flops to remain in their present states without having to disrupt the clock. If either of the 2 input disables are taken to a logic high level, the Q outputs are fed back to the inputs, forcing the flip-flops to remain in the same state. Clearing is enabled by taking the clear input to a logic high level. The data outputs change state on the positive going edge of the clock.

Features

- High Speed Operation: t_{pd} (Clock to Q) = 14 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC173P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74HC173FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74HC173RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

Inputs					Output Q
		Data Enable			
Clear	Clock	G_1	G_2	Data D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	⎍	H	X	X	Q_0
L	⎍	X	H	X	Q_0
L	⎍	L	L	L	L
L	⎍	L	L	H	H

Note: When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

Q_{A0} to Q_{H0} = Outputs remain unchanged.

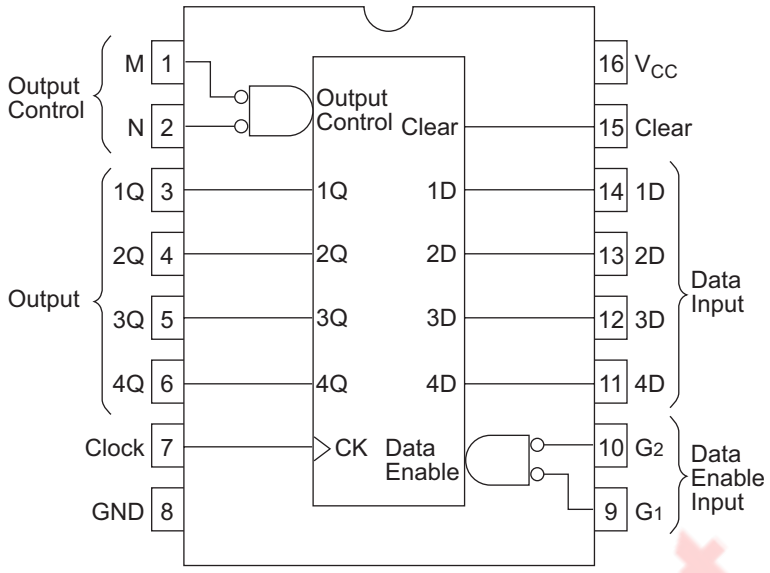
Q_{An} to Q_{Gn} = Data shifted from the previous stage on a positive edge at the clock input.

H : High level

L : Low level

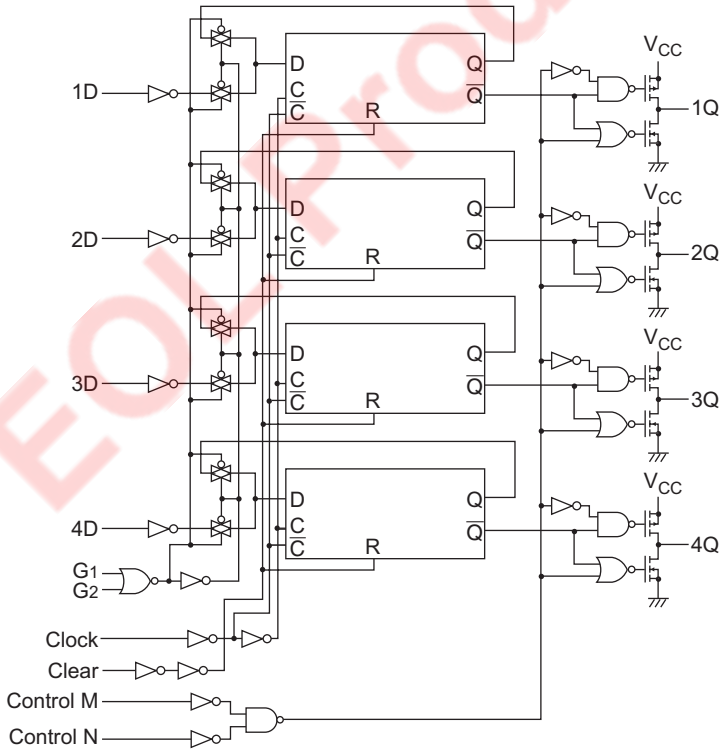
X : Irrelevant

Pin Arrangement



(Top view)

Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	–0.5 to 7.0	V
Input / Output voltage	Vin, Vout	–0.5 to V_{CC} +0.5	V
Input / Output diode current	I_{IK}, I_{OK}	±20	mA
Output current	I_O	±35	mA
V_{CC}, GND current	I_{CC} or I_{GND}	±75	mA
Power dissipation	P_T	500	mW
Storage temperature	Tstg	–65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	Ta	–40 to 85	°C	
Input rise / fall time*1	t_r, t_f	0 to 1000	ns	V_{CC} = 2.0 V
		0 to 500		V_{CC} = 4.5 V
		0 to 400		V_{CC} = 6.0 V

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

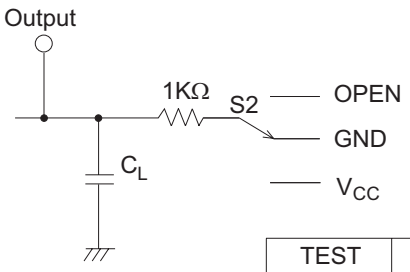
Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = –40 to+85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I_{OH} = –6 mA
		6.0	5.68	—	—	5.63	—			I_{OH} = –7.8 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I_{OL} = 6 mA
		6.0	—	—	0.26	—	0.33			I_{OL} = 7.8 mA
Off-state output current	I_{OZ}	6.0	—	—	±0.5	—	±5.0	µA	Vin = V_{IH} or V_{IL}, Vout = V_{CC} or GND	
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA	

Switching Characteristics

(C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	t_{PLH}, t_{PHL}	2.0	—	—	175	—	220	ns	Clock to Q
		4.5	—	14	35	—	44		
		6.0	—	—	30	—	37		
	t_{PHL}	2.0	—	—	150	—	190	ns	Clear to Q
		4.5	—	14	30	—	38		
		6.0	—	—	26	—	33		
Enable time	t_{ZH}, t_{ZL}	2.0	—	—	150	—	190	ns	
		4.5	—	12	30	—	38		
		6.0	—	—	26	—	33		
Disable time	t_{HZ}, t_{LZ}	2.0	—	—	150	—	190	ns	
		4.5	—	12	30	—	38		
		6.0	—	—	26	—	33		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	
		4.5	20	4	—	25	—		
		6.0	17	–	—	21	—		
Removal time	t_{rem}	2.0	90	—	—	115	—	ns	
		4.5	18	0	—	23	—		
		6.0	15	—	—	20	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	
		4.5	5	–2	—	5	—		
		6.0	5	—	—	5	—		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	4	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t_{TLH}, t_{THL}	2.0	—	—	60	—	75	ns	
		4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
Input capacitance	Cin	—	—	5	10	—	10	pF	

Test Circuit

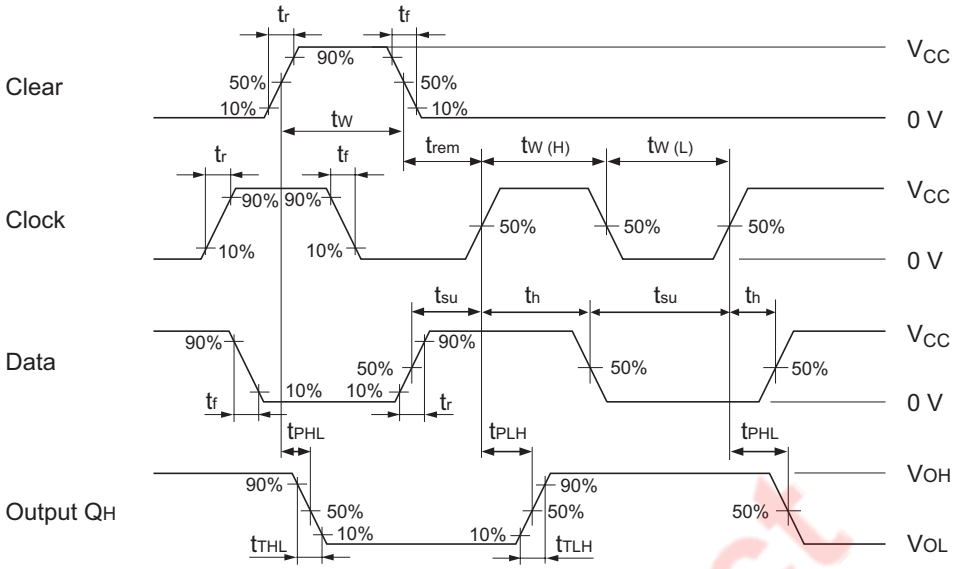


TEST	S2
t_{PLH} / t_{PHL}	OPEN
t_{ZH} / t_{HZ}	GND
t_{ZL} / t_{LZ}	V_{CC}

Note 1. C_L includes probe and jig capacitance

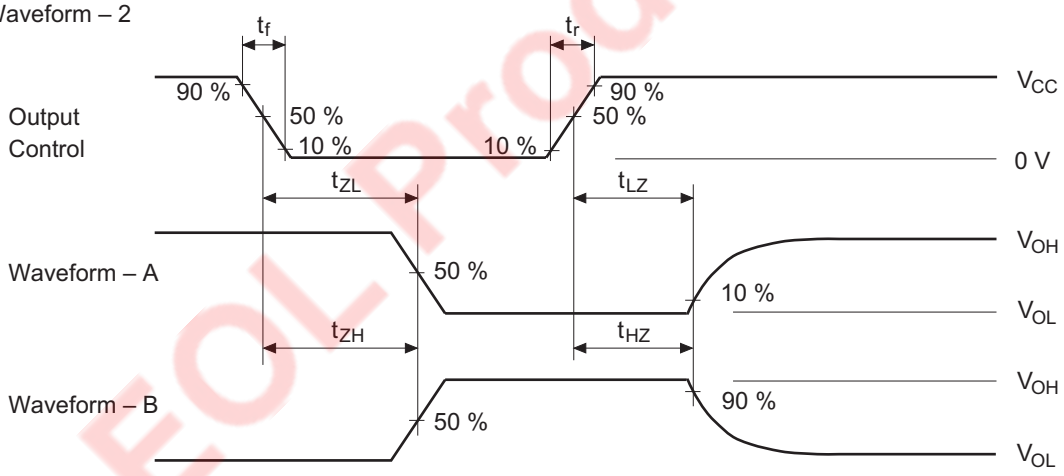
Waveforms

• Waveform – 1



Note 1. Input pulse : PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns

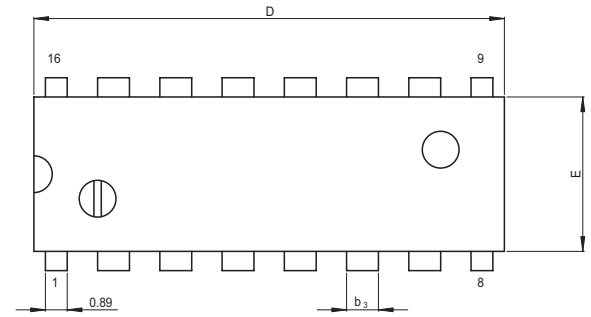
• Waveform – 2

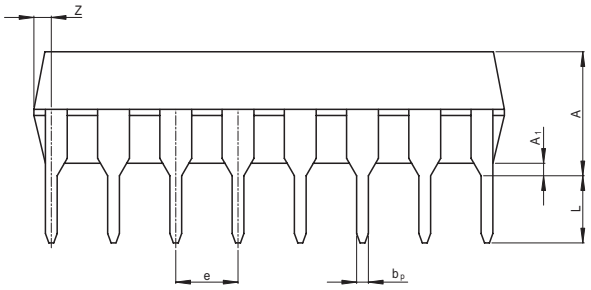


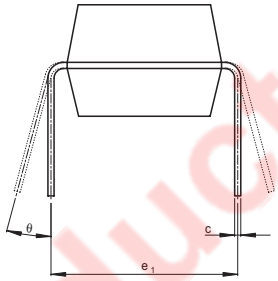
Notes 1. Input pulse PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns
2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
3. waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g



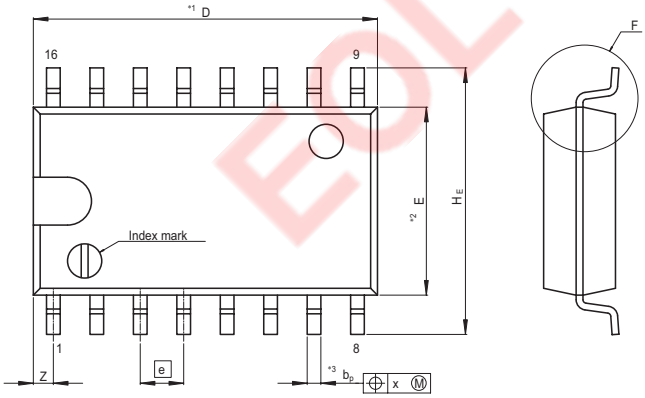


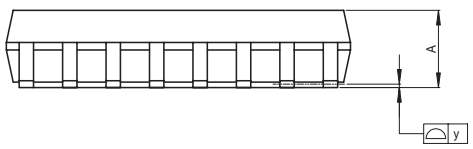


(Ni/Pd/Au plating)

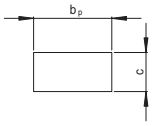
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e 1	——	7.62	——
D	——	19.2	20.32
E	——	6.3	7.4
A	——	——	5.06
A 1	0.51	——	——
b p	0.40	0.48	0.56
b 3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	1.12
L	2.54	——	——

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g

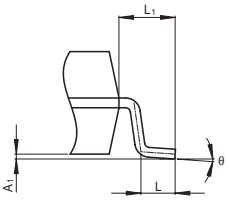




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
   DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
   INCLUDE TRIM OFFSET.



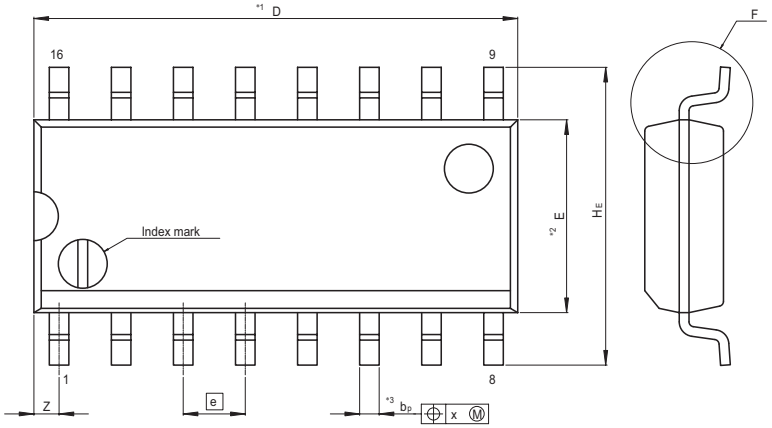
Terminal cross section
(Ni/Pd/Au plating)



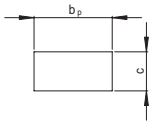
Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	10.06	10.5
E	——	5.50	——
A 2	——	——	——
A 1	0.00	0.10	0.20
A	——	——	2.20
b p	0.34	0.40	0.46
b 1	——	——	——
c	0.15	0.20	0.25
c 1	——	——	——
θ	0°	——	8°
H E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.80
L	0.50	0.70	0.90
L 1	——	1.15	——

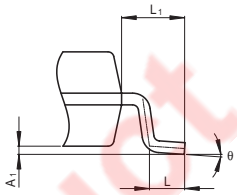
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-3.95x9.9-1.27	PRSP0016DG-A	FP-16DNV	0.15g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	9.90	10.30
E	——	3.95	——
A_2	——	——	——
A_1	0.10	0.14	0.25
A	——	——	1.75
b_p	0.34	0.40	0.46
b_1	——	——	——
c	0.15	0.20	0.25
c_1	——	——	——
θ	0°	——	8°
H_E	5.80	6.10	6.20
e	——	1.27	——
x	——	——	0.25
y	——	——	0.15
Z	——	——	0.635
L	0.40	0.60	1.27
L_1	——	1.08	——

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