To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74HC592

8-bit Register/Binary Counter

REJ03D0633-0200
(Previous ADE-205-513)
Rev.2.00
Mar 30, 2006

Description

The HD74HC592 consists of a parallel input, 8-bit storage register feeding an 8-bit binary counter. Both the register and the counter have individual positive edge-triggered clocks. In addition, the counter has direct load and clear functions. Expansion is easily accomplished by connecting $\overline{RCO}$ of the first stage to the count enable of the second stage, etc.

Features

- High Speed Operation: t_{pd} (CCK to $\overline{RCO}$) = 24 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC592FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

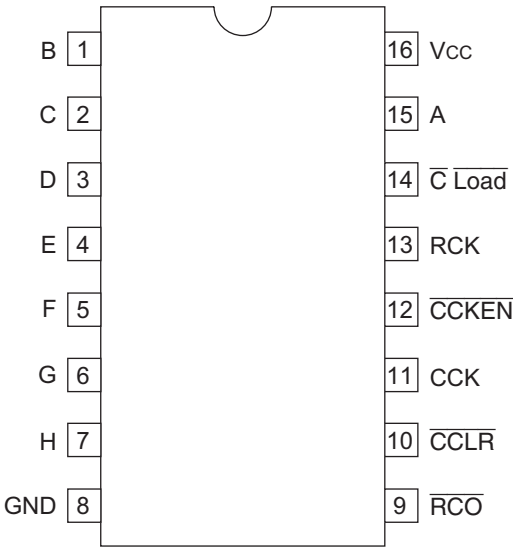
Function Table

Inputs					Function
RCK	$\overline{CLoad}$	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
X	L	H	X	X	Register data loaded into counter
X	H	L	X	X	Counter clear
↑	H	H	X	X	Input data A to H stored into register
↓	H	H	X	X	No change in register
X	H	H	L	↑	Count up
X	H	H	L	↓	No count
X	H	H	H	X	No cont

$\overline{RCO}$ = QA'•QB'•QC'•QD'•QE'•QF'•QG'•QH'• $\overline{(\overline{CCKEN})}$

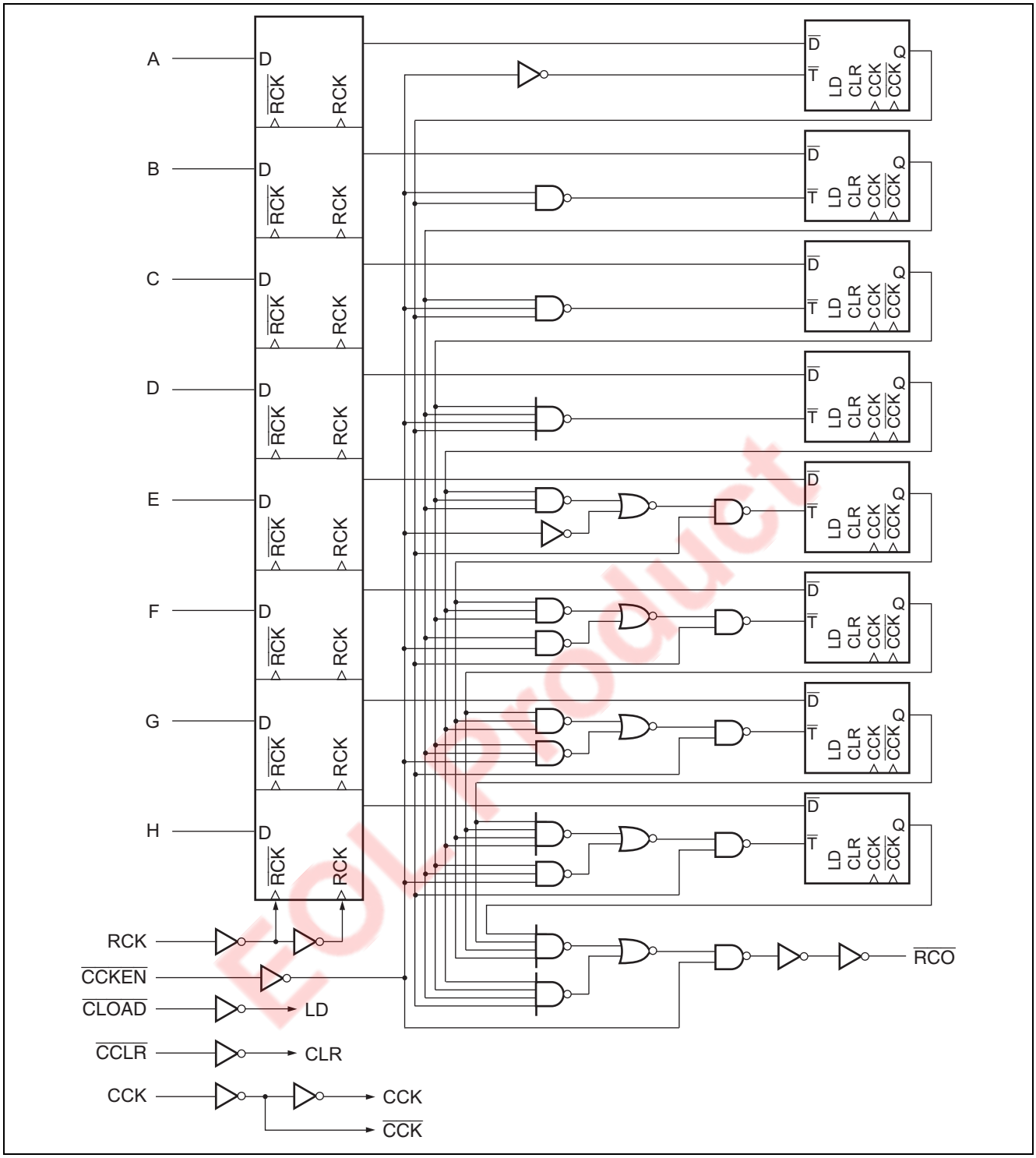
(QA' to QH': Output of Internal Counter)

Pin Arrangement



(Top view)

Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	–0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	–0.5 to V_{CC} +0.5	V
Input / Output diode current	I_{IK}, I_{OK}	±20	mA
Output current	I_{OUT}	±25	mA
V_{CC}, GND current	I_{CC} or I_{GND}	±50	mA
Power dissipation	P_T	500	mW
Storage temperature	Tstg	–65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	Ta	–40 to 85	°C	
Input rise / fall time*1	t_r, t_f	0 to 1000	ns	V_{CC} = 2.0 V
		0 to 500		V_{CC} = 4.5 V
		0 to 400		V_{CC} = 6.0 V

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

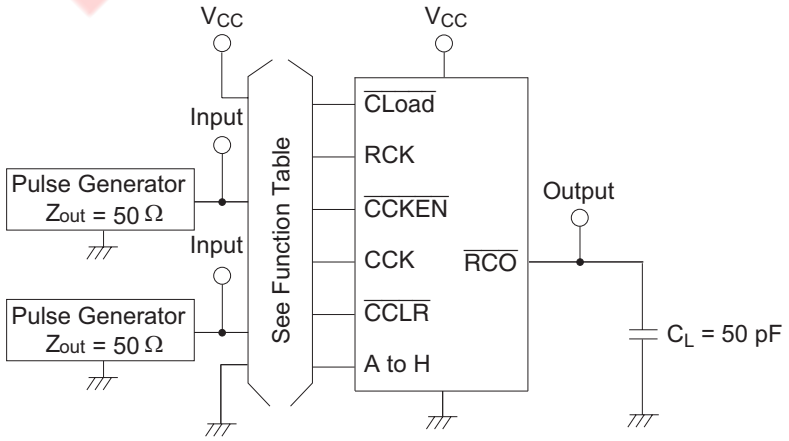
Electrical Characteristics

Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = –40 to+85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—			I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I_{OH} = 4 mA
		6.0	—	—	0.26	—	0.33			I_{OH} = 5.2 mA
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA	

Switching Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	25	—	20		
		6.0	—	—	29	—	24		
Propagation delay time	t_{PLH} t_{PHL}	2.0	—	—	200	—	250	ns	CCK to $\overline{RCO}$
		4.5	—	24	40	—	50		
		6.0	—	—	34	—	43		
	t_{PLH} t_{PHL}	2.0	—	—	200	—	250	ns	$\overline{C\ Load}$ to $\overline{RCO}$
		4.5	—	27	40	—	50		
		6.0	—	—	34	—	43		
	t_{PLH}	2.0	—	—	200	—	250	ns	$\overline{CCLR}$ to $\overline{RCO}$
		4.5	—	26	40	—	50		
		6.0	—	—	34	—	43		
	t_{PLH} t_{PHL}	2.0	—	—	300	—	375	ns	RCK to $\overline{RCO}$
		4.5	—	29	60	—	75		
		6.0	—	—	51	—	64		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	8	–	20	—		
		6.0	14	—	—	17	—		
Removal time	t_{rem}	2.0	100	—	—	125	—	ns	$\overline{CCLR}$ to CCK
		4.5	20	12	—	25	—		
		6.0	17	—	—	21	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	$\overline{CCKEN}$ to CCK
		4.5	20	0	—	25	—		
		6.0	17	—	—	21	—		
		2.0	200	—	—	250	—	ns	CCK to RCK
		4.5	40	14	—	50	—		
		6.0	34	—	—	43	—		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	—	5	10	—	10	pF	

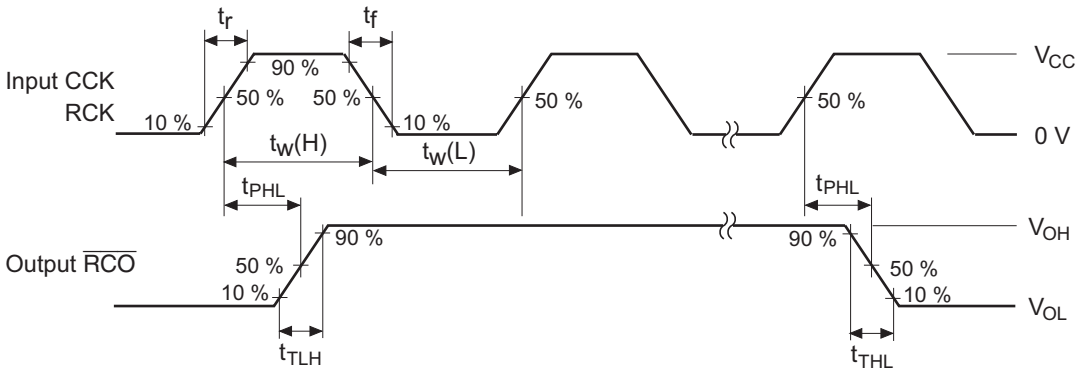
Test Circuit



Note : 1. C_L includes probe and jig capacitance.

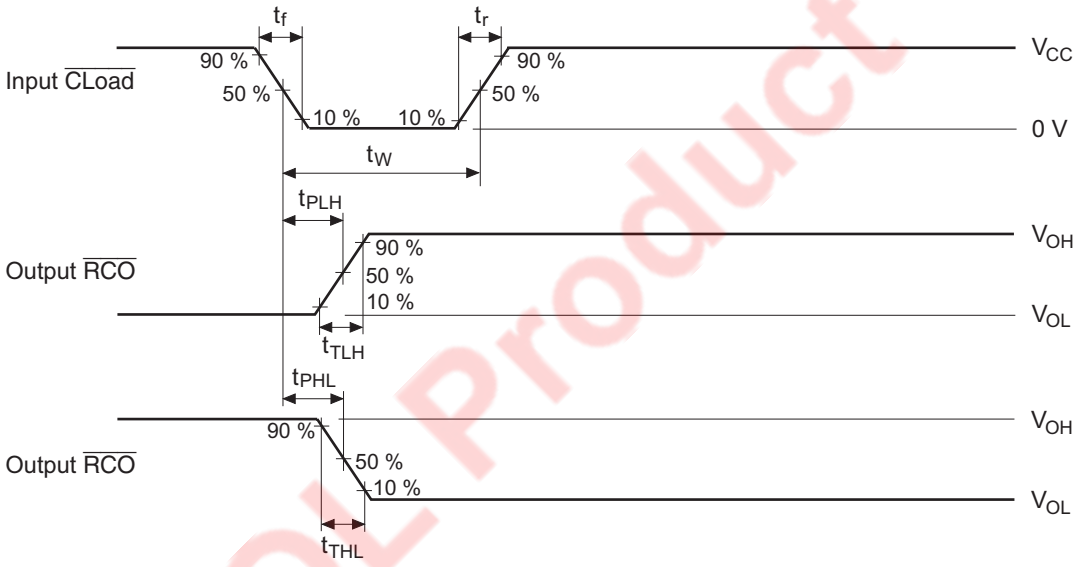
Waveforms

• Waveform – 1 (CCK, RCK to $\overline{RCO}$)



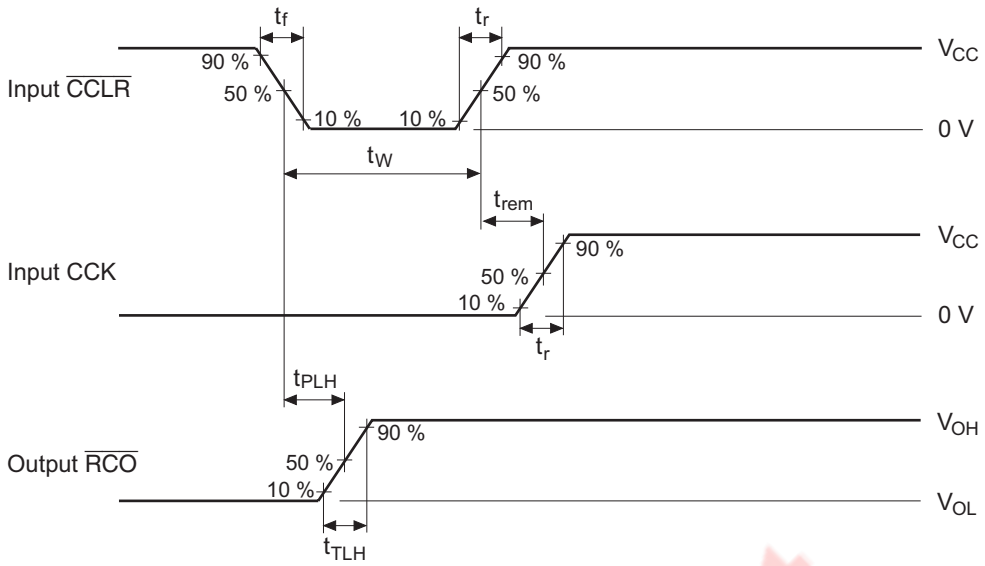
Note : 1. Input waveform : PRR ≤ 1 MHz, duty cycle 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns

• Waveform – 2 ($\overline{CLoad}$ to $\overline{RCO}$)



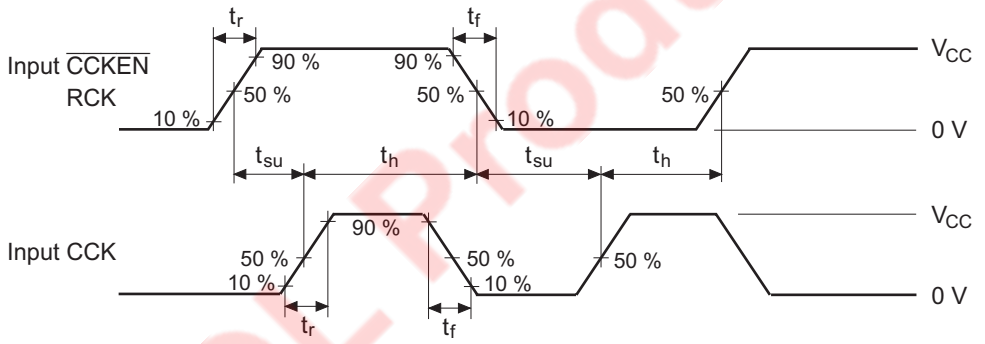
Note : 1. Input waveform : PRR ≤ 1 MHz, duty cycle 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns

• Waveform – 3 ($\overline{CCLR}$ to $\overline{RCO}$, $\overline{CCLR}$ to CCK)



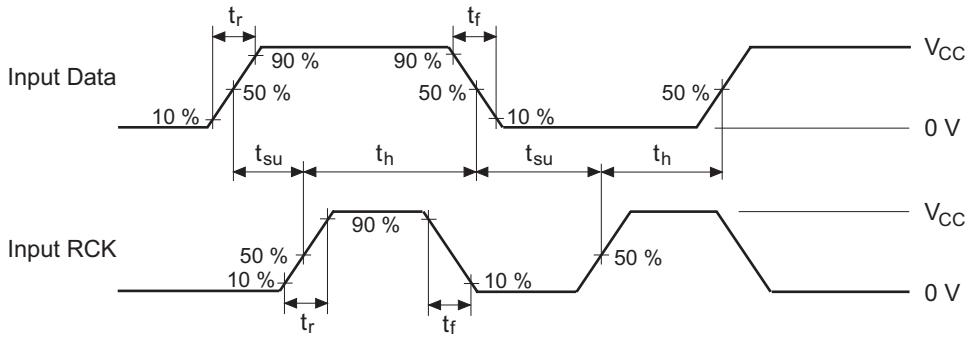
Note : 1. Input waveform : PRR ≤ 1 MHz, duty cycle 50%, t_r ≤ 6 ns, t_f ≤ 6 ns

• Waveform – 4 ($\overline{CCKEN}$, RCK to CCK)



Note : 1. Input waveform : PRR ≤ 1 MHz, duty cycle 50%, t_r ≤ 6 ns, t_f ≤ 6 ns

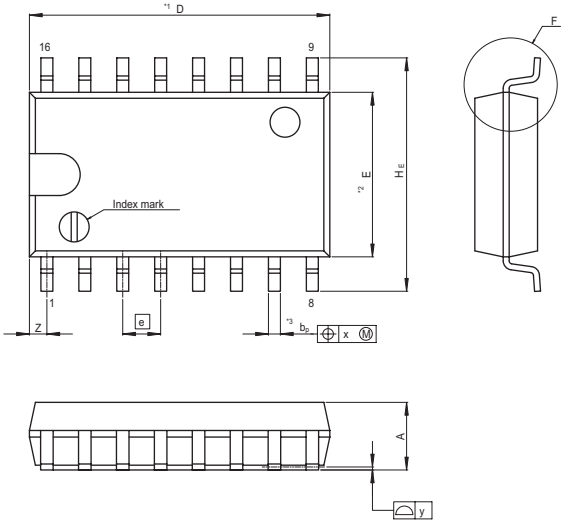
• Waveform – 5 (Data to RCK)

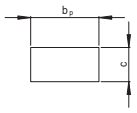


Note : 1. Input waveform : PRR ≤ 1 MHz, duty cycle 50%, t_r ≤ 6 ns, t_f ≤ 6 ns

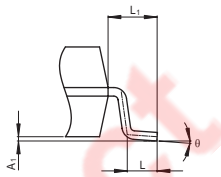
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g





Terminal cross section
(Ni/Pd/Au plating)



Detail F

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A_2	—	—	—
A_1	0.00	0.10	0.20
A	—	—	2.20
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L_1	—	1.15	—

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