

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HD74HC668, HD74HC669

## Synchronous UP/Down Decade Counter Synchronous Up/Down 4-bit binary Counter

REJ03D0638-0200  
(Previous ADE-205-520)  
Rev.2.00  
Mar 30, 2006

### Description

This synchronous presettable decade counter features an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters.

A buffered clock input triggers the four master-slave flip-flops on the rising (positive going) edge of the clock waveform. This counter is fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count enable inputs and a carry output. Both count enable inputs ( $\bar{P}$  and  $\bar{T}$ ) must be low to count. The direction of the count is determined by the level of the up/down input. when the input is high, the counter counts up; when low, it counts down. Input  $\bar{T}$  is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the  $Q_A$  output when counting up and approximately equal to the low portion of the  $Q_A$  output when counting down. This low level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable  $\bar{P}$  or  $\bar{T}$  inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transission-line effects, thereby simplifying system design. This counter features a fully independent clock circuit. Changes at control inputs (enable  $\bar{P}$ , Enable  $\bar{T}$ , load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

### Features

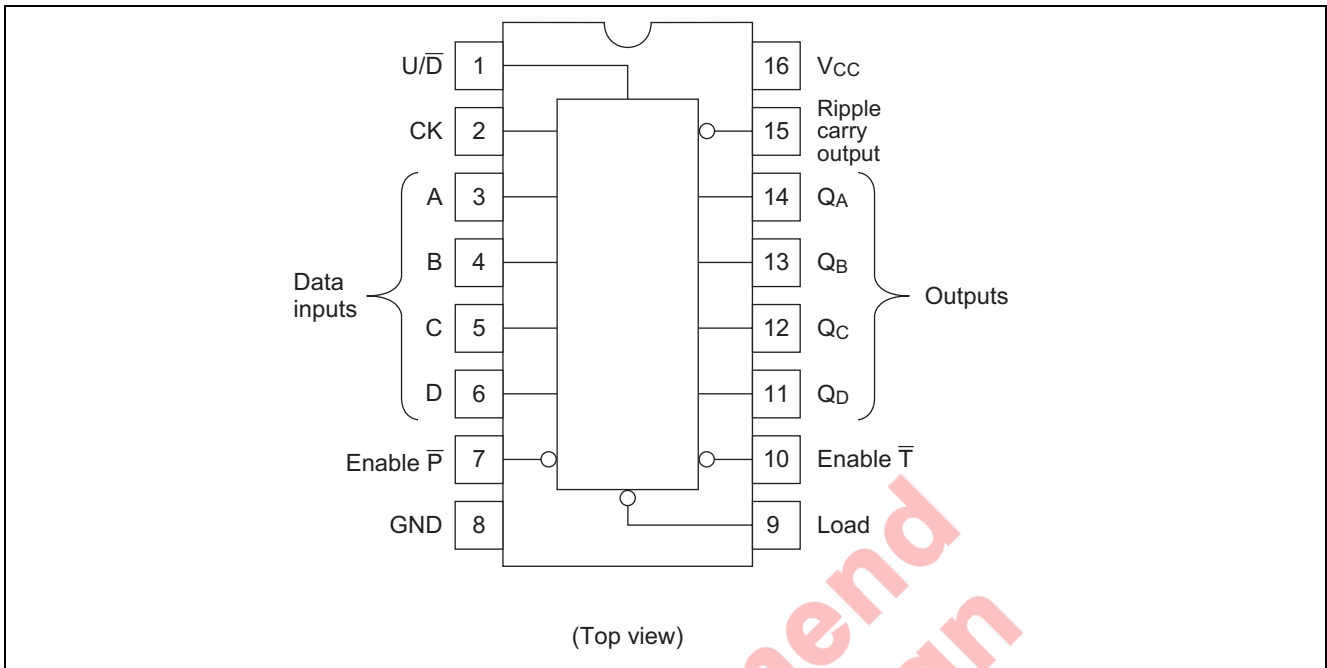
- High Speed Operation
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC669P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74HC669FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74HC668RPEL HD74HC669RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (1,000 pcs/reel)

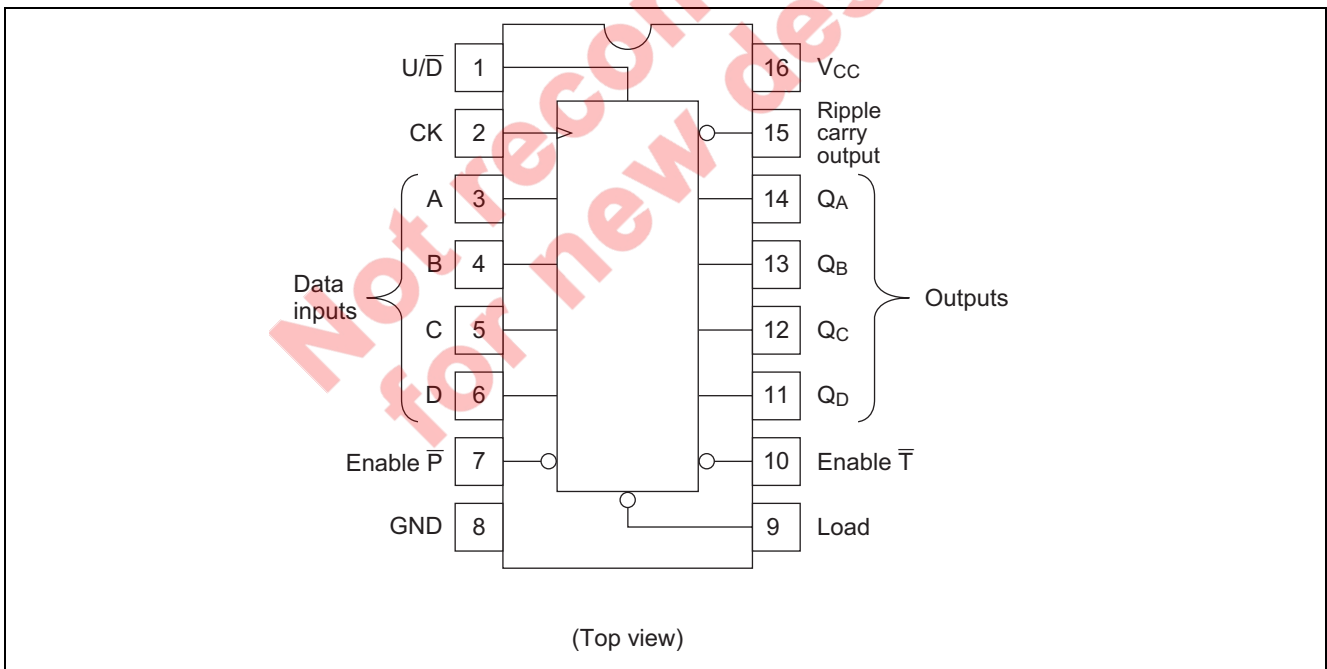
Note: Please consult the sales office for the above package availability.

Pin Arrangement

HD74HC668

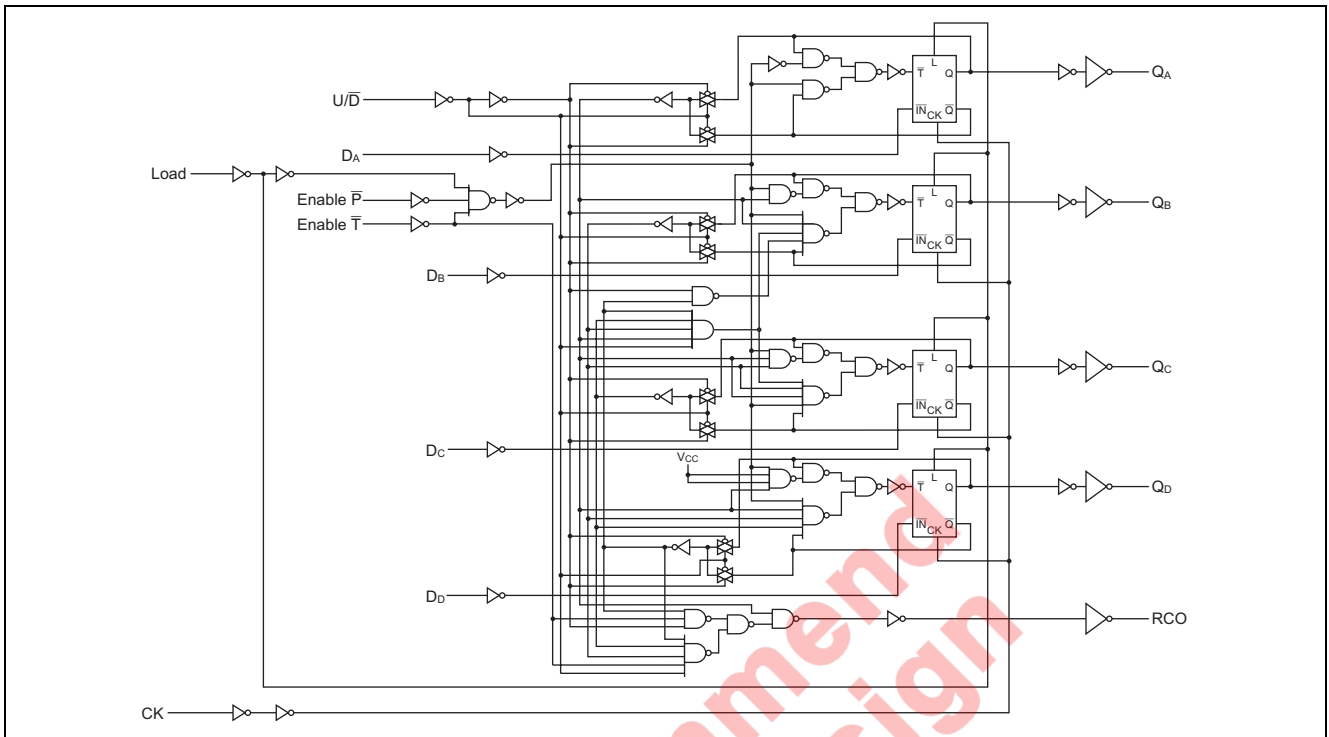


HD74HC669

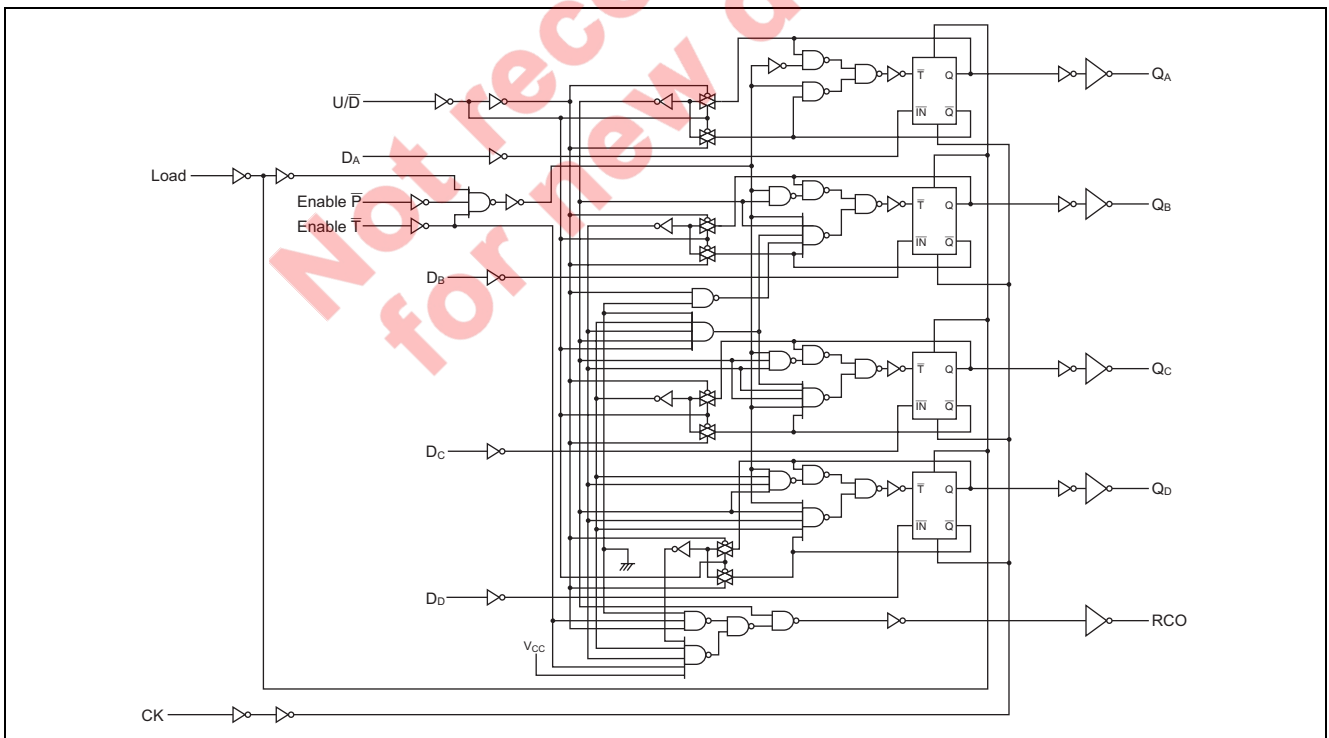


Logic Diagram

HD74HC668

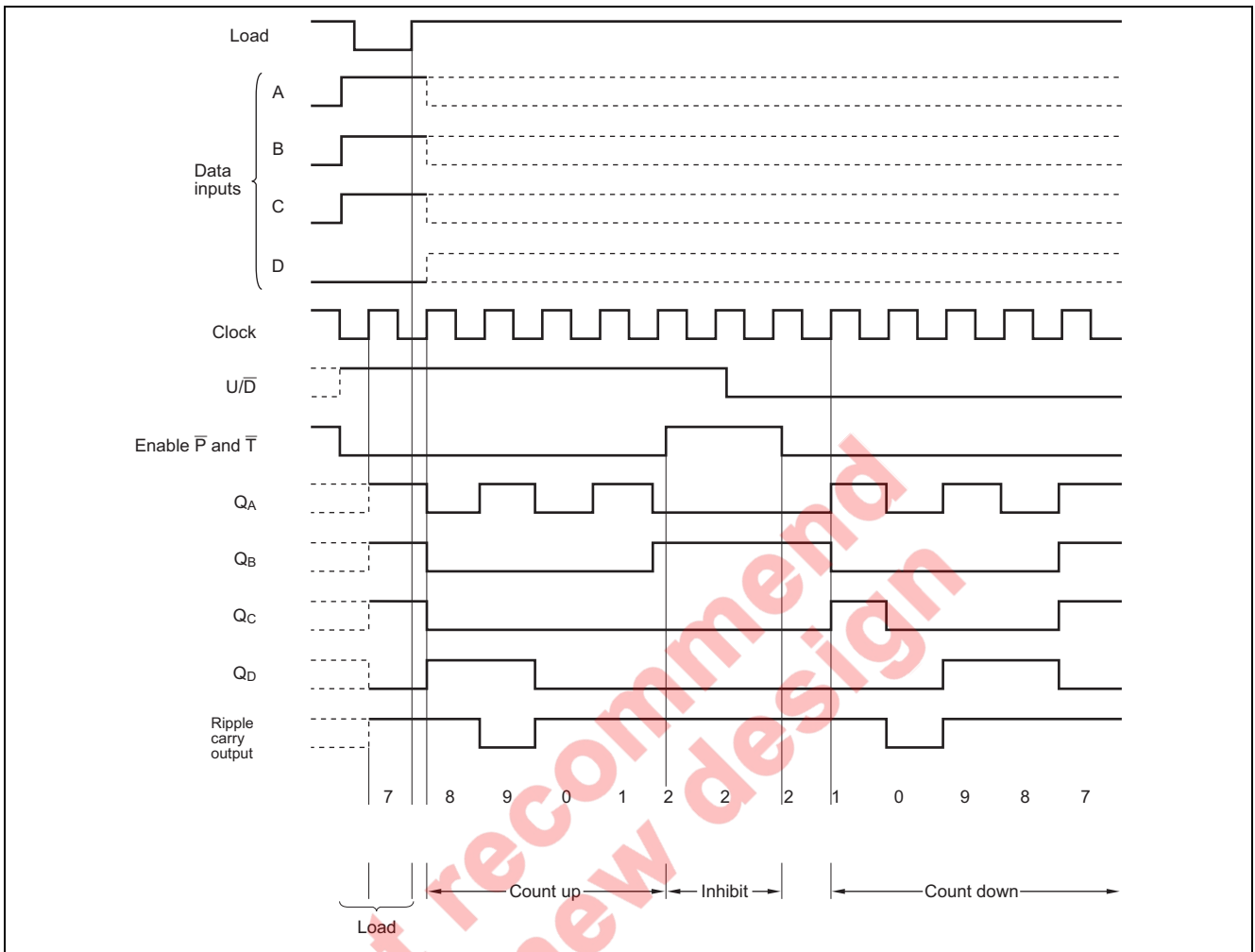


HD74HC669

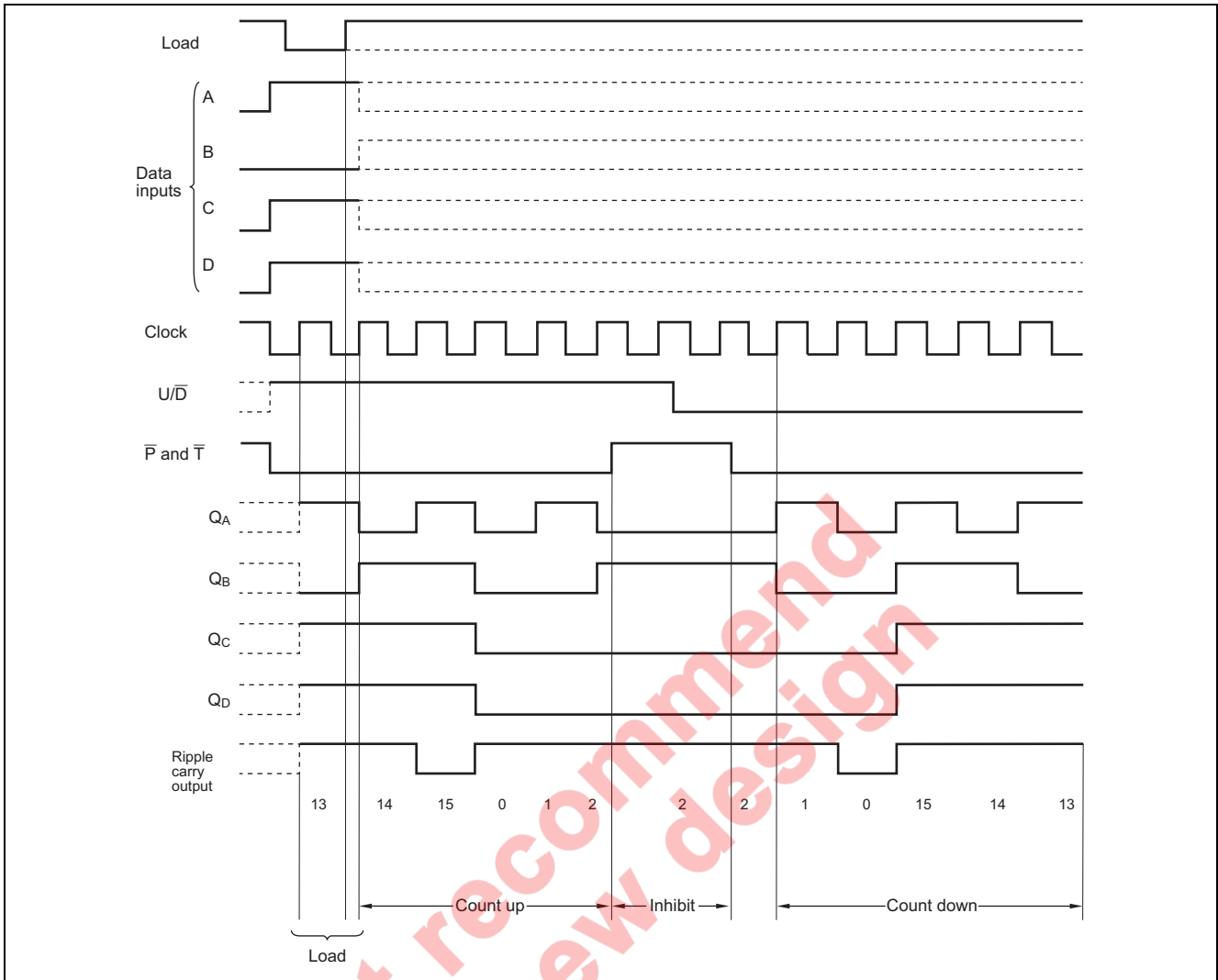


# Timing Chart

## HD74HC668



HD74HC669



**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
Input / Output voltage	$V_{IN}, V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	$I_{IK}, I_{OK}$	$\pm 20$	mA
Output current	$I_O$	$\pm 25$	mA
$V_{CC}$ , GND current	$I_{CC}$ or $I_{GND}$	$\pm 50$	mA
Power dissipation	$P_T$	500	mW
Storage temperature	$T_{stg}$	-65 to +150	$^{\circ}C$

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

### Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	2 to 6	V	
Input / Output voltage	$V_{IN}, V_{OUT}$	0 to $V_{CC}$	V	
Operating temperature	$T_a$	-40 to 85	°C	
Input rise / fall time*1	$t_r, t_f$	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

### Electrical Characteristics

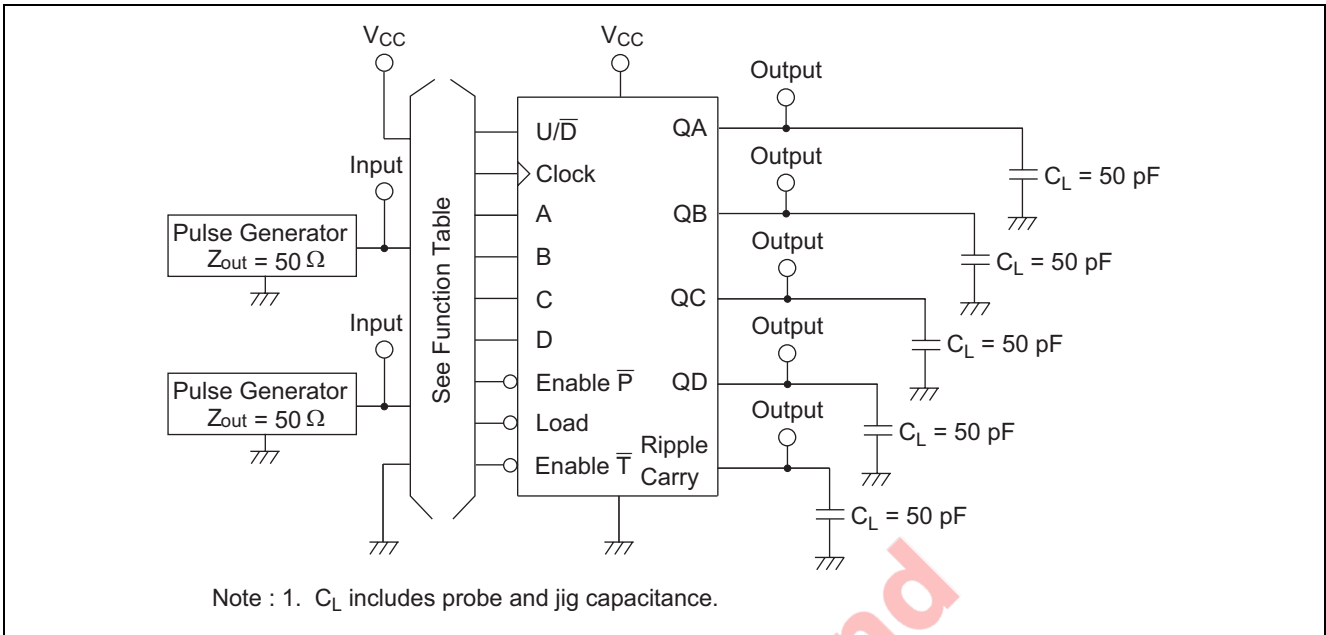
Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\text{ to }+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	$V_{IH}$	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	$V_{IL}$	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	$V_{OH}$	2.0	1.9	2.0	—	1.9	—	V	$V_{in} = V_{IH}\text{ or }V_{IL}$	$I_{OH} = -20\ \mu\text{A}$
		4.5	4.4	4.5	—	4.4	—			$I_{OH} = -4\ \text{mA}$
		6.0	5.9	6.0	—	5.9	—			$I_{OH} = -5.2\ \text{mA}$
		4.5	4.18	—	—	4.13	—			
		6.0	5.68	—	—	5.63	—			
	$V_{OL}$	2.0	—	0.0	0.1	—	0.1	V	$V_{in} = V_{IH}\text{ or }V_{IL}$	$I_{OL} = 20\ \mu\text{A}$
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			$I_{OL} = 4\ \text{mA}$
		6.0	—	—	0.26	—	0.33			$I_{OL} = 5.2\ \text{mA}$
Input current	$I_{in}$	6.0	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$	$V_{in} = V_{CC}\text{ or GND}$	
Quiescent supply current	$I_{CC}$	6.0	—	—	4.0	—	40	$\mu\text{A}$	$V_{in} = V_{CC}\text{ or GND}, I_{out} = 0\ \mu\text{A}$	



**Switching Characteristics** ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

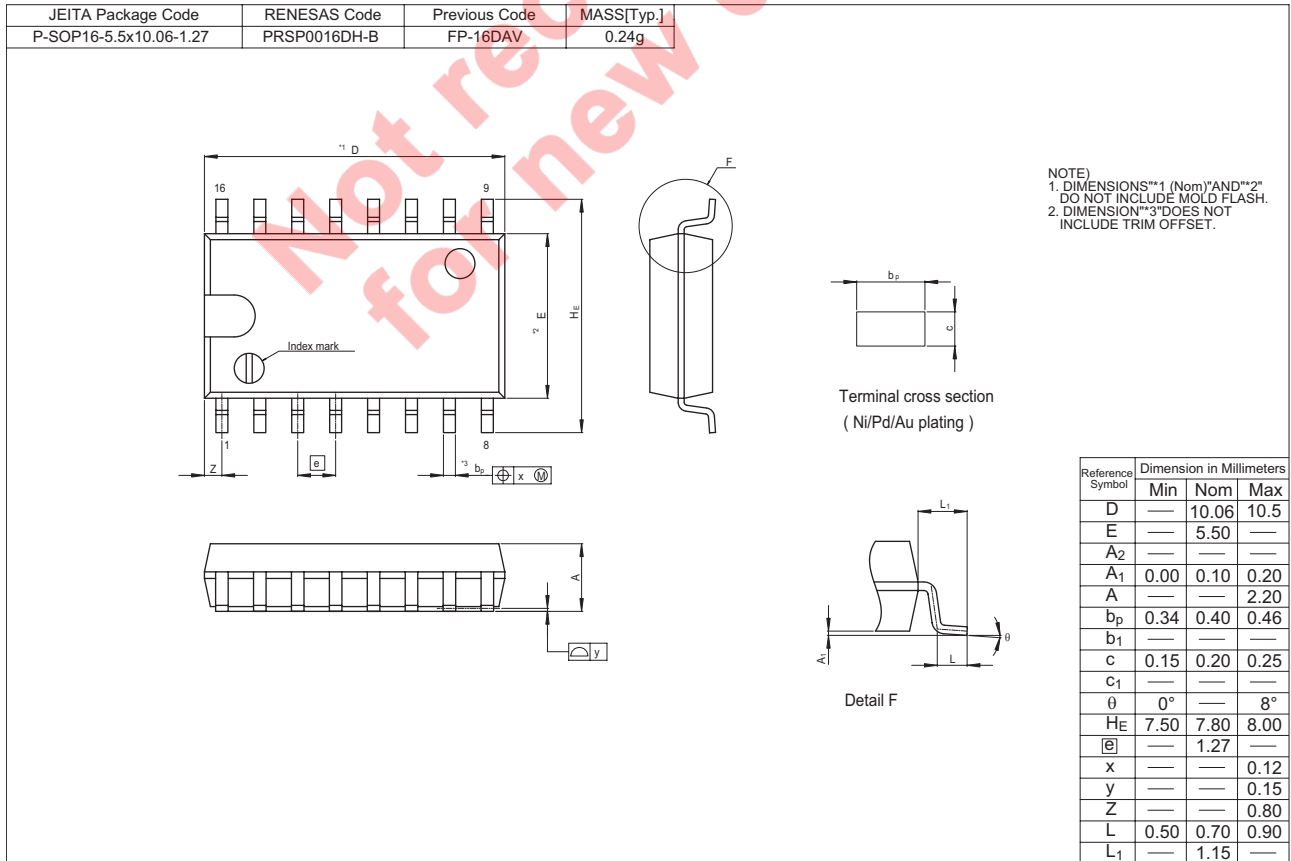
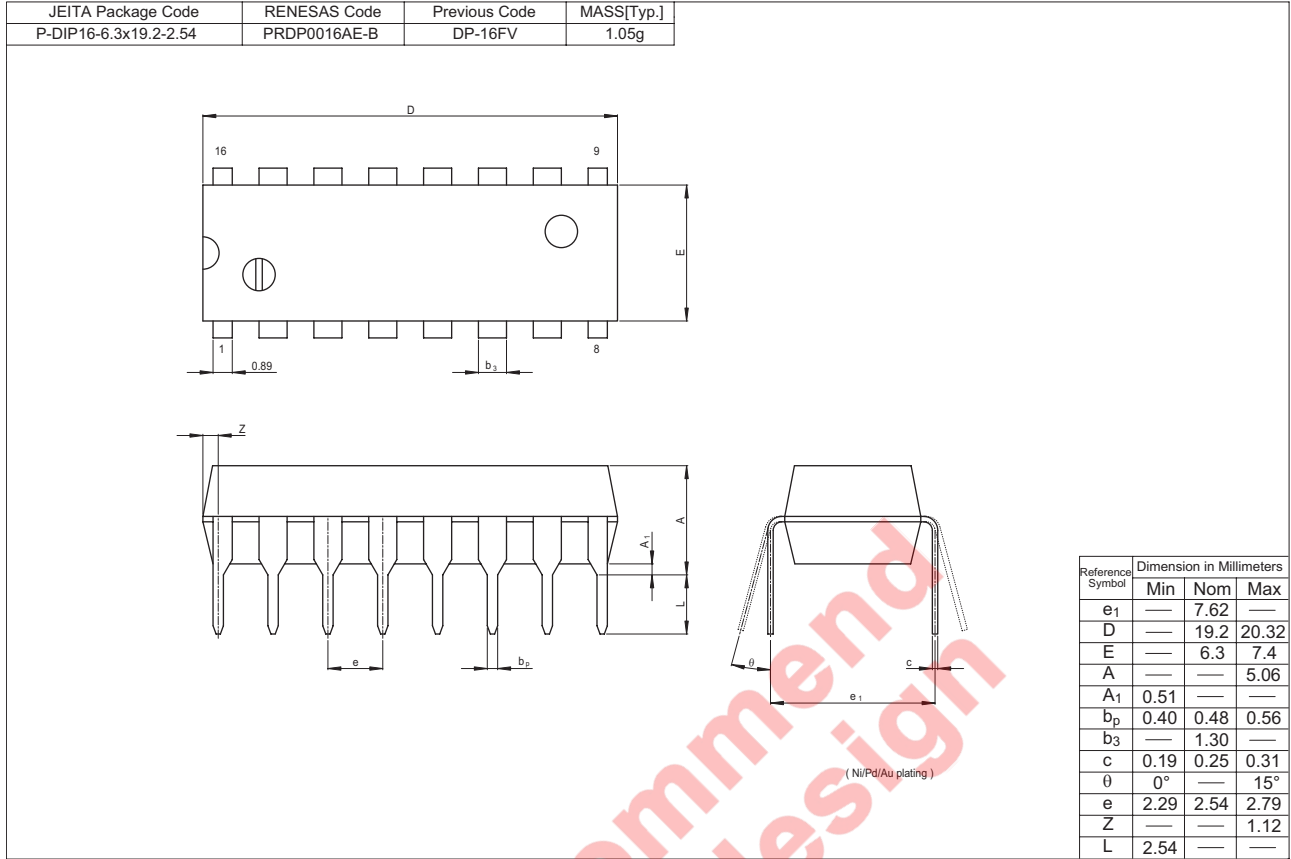
Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock Frequency	$f_{max}$	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	$t_{PLH}$ $t_{PHL}$	2.0	—	—	200	—	250	ns	Clock to Ripple carry out
		4.5	—	—	40	—	50		
		6.0	—	—	34	—	43		
	$t_{PLH}$ $t_{PHL}$	2.0	—	—	225	—	280	ns	Clock to Q
		4.5	—	—	45	—	56		
		6.0	—	—	38	—	48		
	$t_{PLH}$ $t_{PHL}$	2.0	—	—	150	—	190	ns	Enable $\bar{T}$ to Ripple carry out
		4.5	—	—	30	—	38		
		6.0	—	—	26	—	33		
	$t_{PLH}$ $t_{PHL}$	2.0	—	—	200	—	250	ns	$U/\bar{D}$ to Ripple carry out
		4.5	—	—	40	—	50		
		6.0	—	—	34	—	43		
Pulse width	$t_w$	2.0	80	—	—	100	—	ns	
		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		
Setup time	$t_{su}$	2.0	100	—	—	125	—	ns	Data to Clock
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
	$t_{su}$	2.0	150	—	—	190	—	ns	Enable $\bar{P}$ , $\bar{T}$ to Clock
		4.5	30	—	—	38	—		
		6.0	26	—	—	33	—		
	$t_{su}$	2.0	150	—	—	190	—	ns	Loadk to Clock
		4.5	30	—	—	38	—		
		6.0	26	—	—	33	—		
	$t_{su}$	2.0	150	—	—	190	—	ns	$U/\bar{D}$ to Clock
		4.5	30	—	—	38	—		
		6.0	26	—	—	33	—		
Hold time	$t_h$	2.0	5	—	—	5	—	ns	
		4.5	5	—	—	5	—		
		6.0	5	—	—	5	—		
Output rise/fall time	$t_{TLH}$ $t_{THL}$	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	$C_{in}$	—	—	5	10	—	10	pF	

Test Circuit



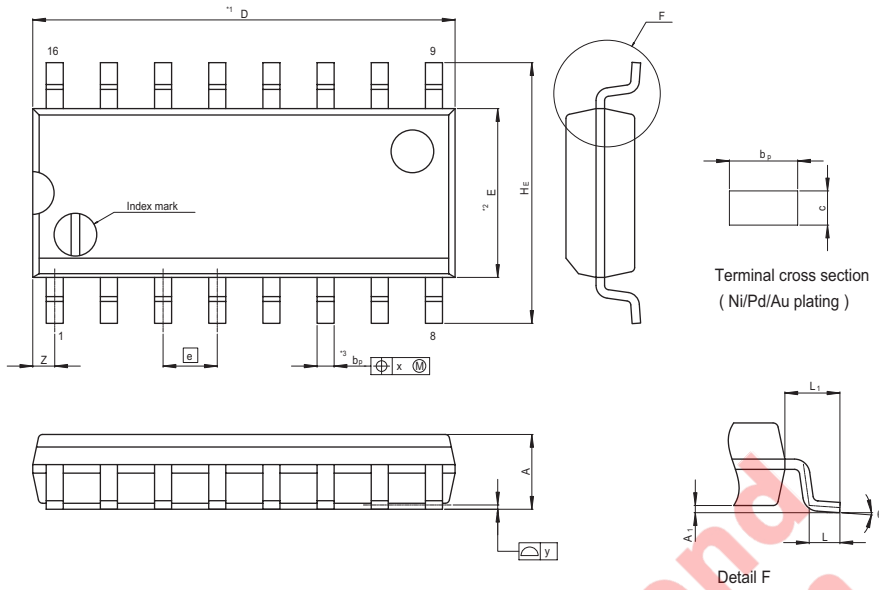
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Package Dimensions



# HD74HC668, HD74HC669

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-3.95x9.9-1.27	PRSP0016DG-A	FP-16DNV	0.15g



NOTE)  
 1. DIMENSIONS\*\*1 (Nom)\*\*AND\*\*2\*  
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION\*\*3\*DOES NOT  
 INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	9.90	10.30
E	—	3.95	—
A <sub>2</sub>	—	—	—
A <sub>1</sub>	0.10	0.14	0.25
A	—	—	1.75
b <sub>p</sub>	0.34	0.40	0.46
b <sub>1</sub>	—	—	—
c	0.15	0.20	0.25
c <sub>1</sub>	—	—	—
θ	0°	—	8°
HE	5.80	6.10	6.20
Ⓧ	—	1.27	—
x	—	—	0.25
y	—	—	0.15
Z	—	—	0.635
L	0.40	0.60	1.27
L <sub>1</sub>	—	1.08	—

Not recommended for new design

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