To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74LS165A

Parallel-Load 8-bit Shift Register

REJ03D0449–0300
Rev.3.00
Jul.15.2005

The LS165A are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift / load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift / load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift / load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift / load input independently of the levels of the clock, clock inhibit, or serial inputs.

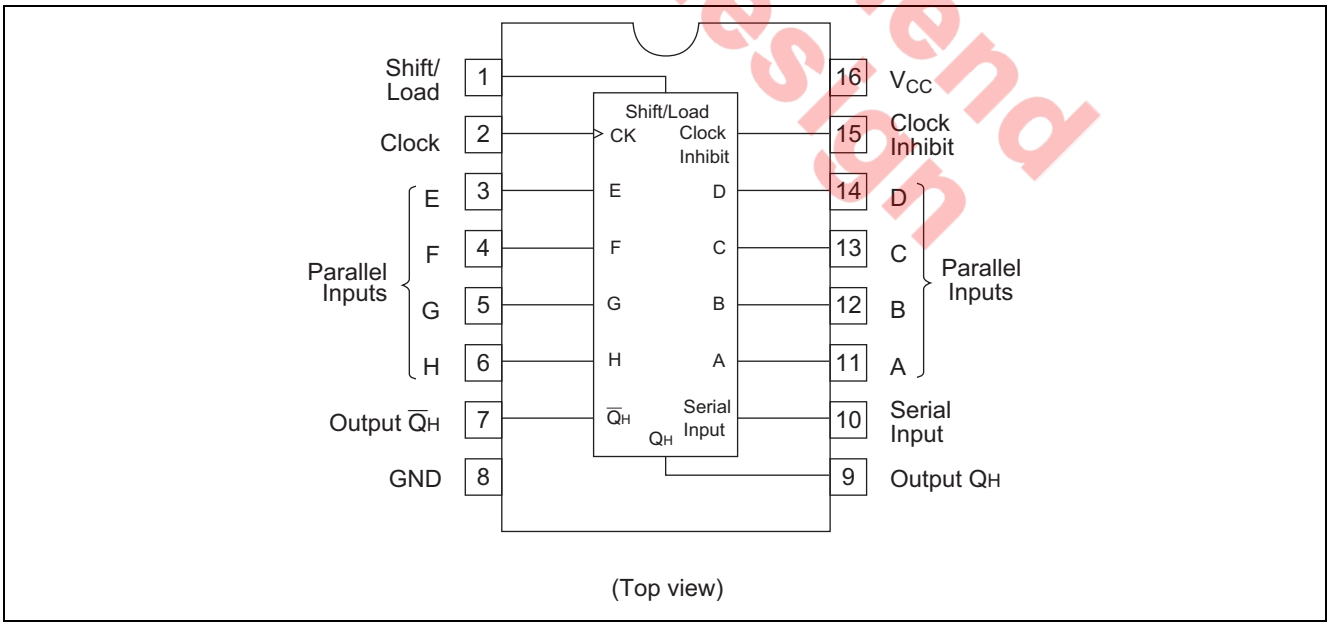
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS165AP	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS165AFPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



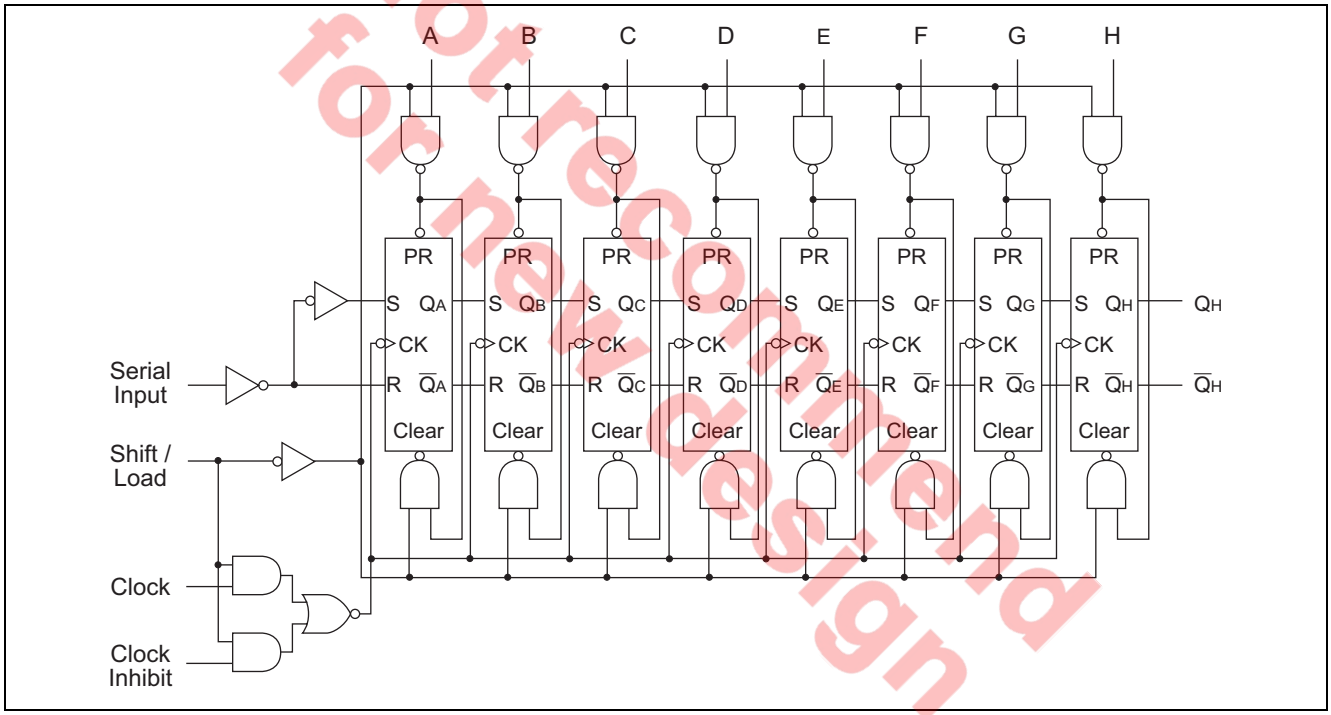
(Top view)

Function Table

Inputs					Internal outputs		Output
Shift / Load	Clock Inhibit	Clock	Serial	Parallel			
				A…H	Q_A	Q_B	Q_H
L	X	X	X	a…h	a	b	h
H	L	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

Notes: 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. a to h; the level of steady-state input at inputs A to H respectively
4. Q_{A0} to Q_{H0}; the level of Q_A to Q_H, respectively, before the indicated steady-state input conditions were established.
5. Q_{An} to Q_{Gn}; the level of Q_A to Q_G, respectively, before the most recent ↓ transition of the clock.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	–400	µA
	I_{OL}	—	—	8	mA
Operating temperature	T_{opr}	–20	25	75	°C
Clock frequency	f_{clock}	0	—	25	MHz
Clock pulse width	$t_{w\ (clock)}$	25	—	—	ns
Load pulse width	$t_{w\ (load)}$	15	—	—	ns
Clock enable setup time	t_{su}	30	—	—	ns
Parallel input setup time	t_{su}	10	—	—	ns
Serial input setup time	t_{su}	20	—	—	ns
Shift setup time	t_{su}	45	—	—	ns
Hold time	t_h	0	—	—	ns

Electrical Characteristics

(Ta = –20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V_{IH}	2.0	—	—	V	
		V_{IL}	—	—	0.8	V	
Output voltage		V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA
		V_{OL}	—	—	0.4	V	I_{OL} = 4 mA; V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
			—	—	0.5		I_{OL} = 8 mA
Input current	Shift / Load	I_I	—	—	0.3	mA	V_{CC} = 5.25 V, V_I = 7 V
	Other inputs		—	—	0.1	mA	
High level input current	Shift / Load	I_{IH}	—	—	60	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	Other inputs		—	—	20	µA	
Low level input current	Shift / Load	I_{IL}	—	—	–1.2	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	Other inputs		—	—	–0.4	mA	
Short-circuit output current		I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current**		I_{CC}	—	21	36	mA	V_{CC} = 5.25 V
Input clamp voltage		V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Note: * V_{CC} = 5 V, Ta = 25°C

**. With the outputs open, clock inhibit and clock at 4.5 V, and a clock pulse applied to the shift / load, I_{CC} is measured with the parallel inputs at 4.5 V, than with the parallel inputs grounded.

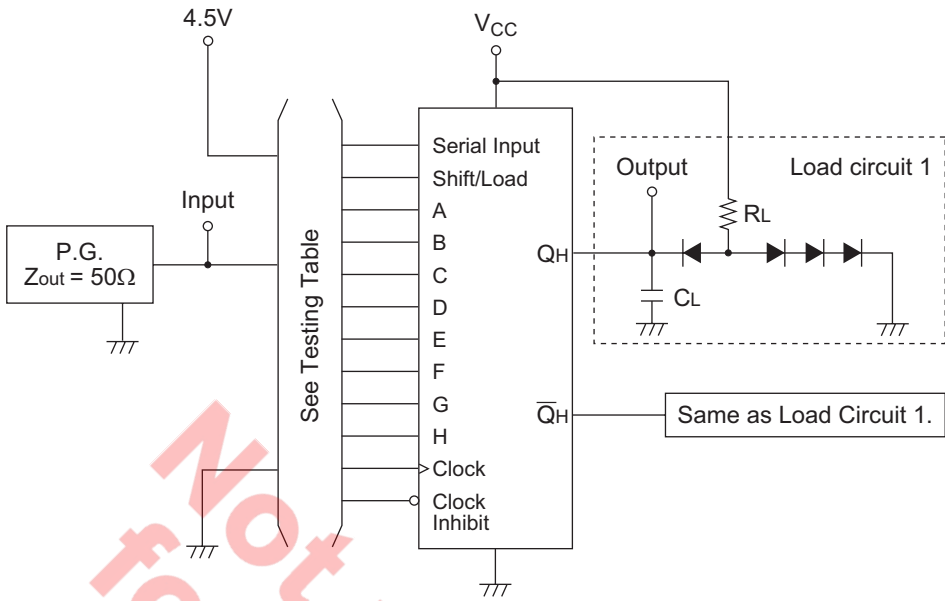
Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}			25	35	—	MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PLH}	Load	Any	—	21	35	ns	
	t_{PHL}			—	26	35	ns	
	t_{PLH}	Clock	Any	—	14	25	ns	
	t_{PHL}			—	16	25	ns	
	t_{PLH}	H	Q_H	—	13	25	ns	
	t_{PHL}			—	24	30	ns	
	t_{PLH}	H	Q_H	—	19	30	ns	
	t_{PHL}			—	17	25	ns	

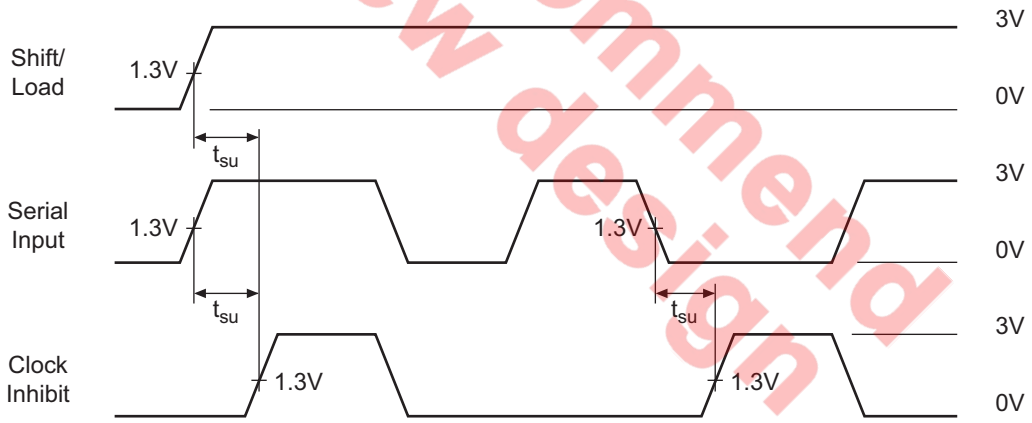
Testing Method

Test Circuit



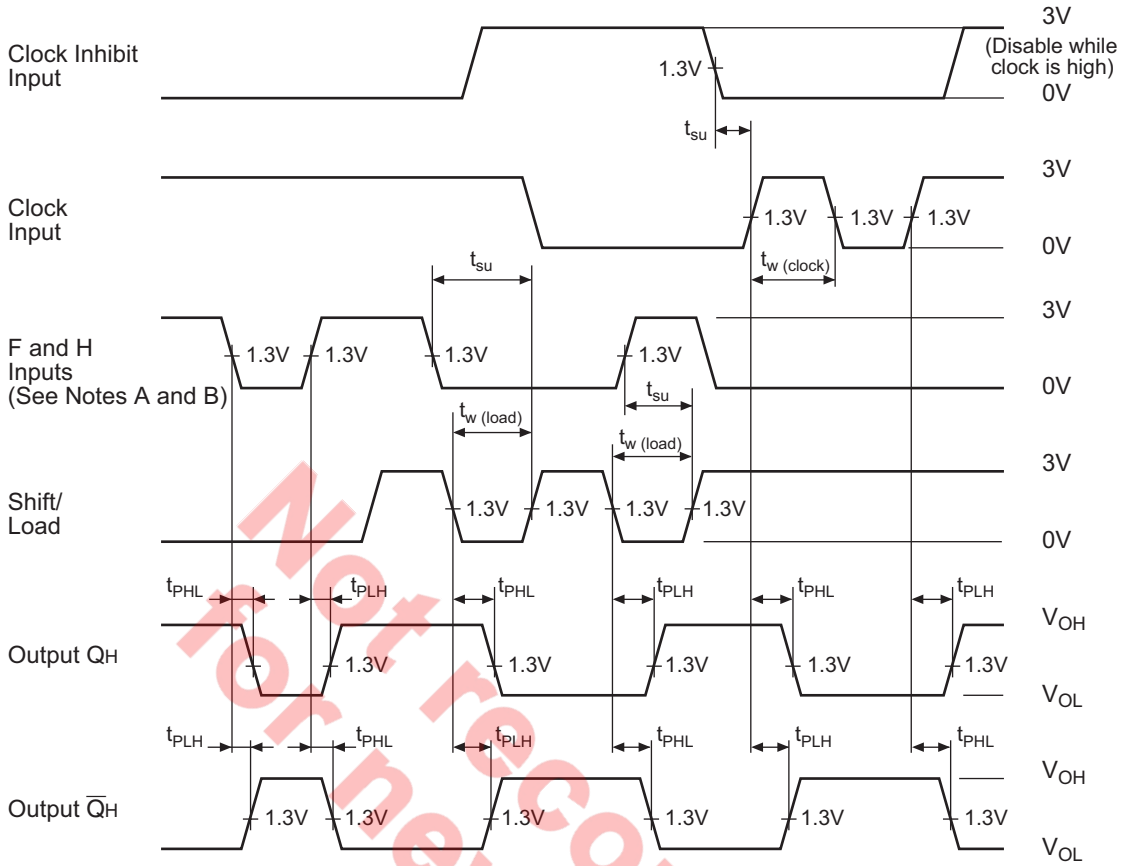
Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

Waveforms 1



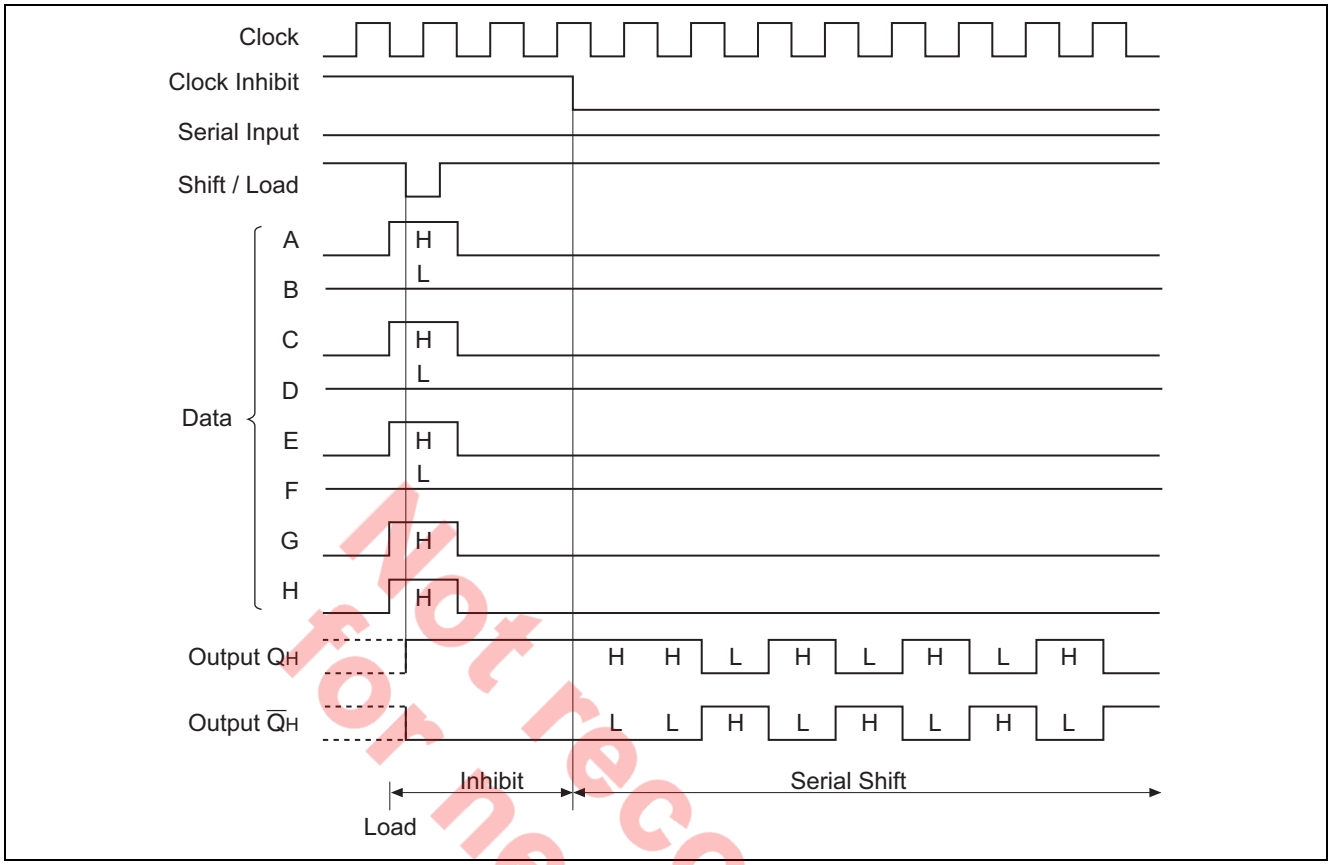
Notes: A. The eight data inputs and the clock-inhibit input are low. Results are monitored at output Q_H at T_{n+7}.
B. The input pulse generators have the following characteristics: PRR < 1 MHz, duty cycle < 50%, $Z_{out} \approx 50\ \Omega$, $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns.

Waveforms 2



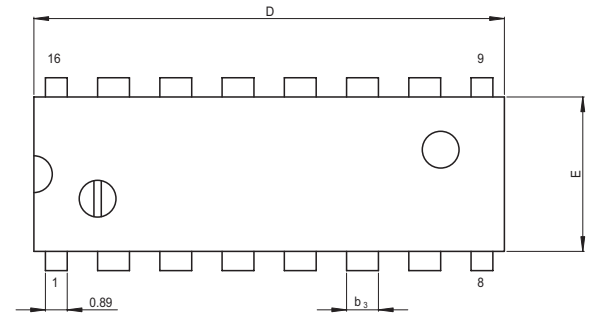
Notes:
A. The remaining six data inputs and the serial input are low.
B. Prior to test, high-level data is loaded into H input.
C. The input pulse Generators have the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$, $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns.

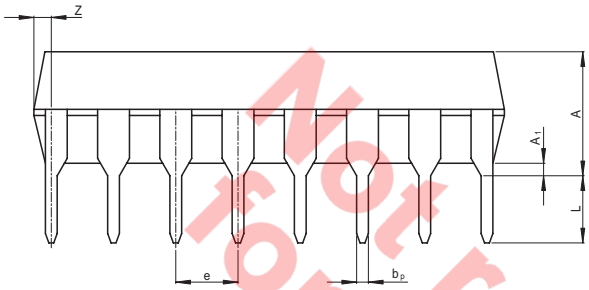
Typical Shift, Load and Inhibit Sequences

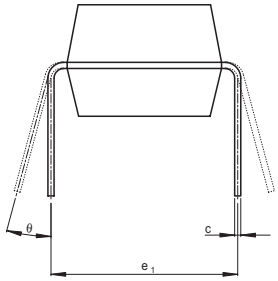


Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g



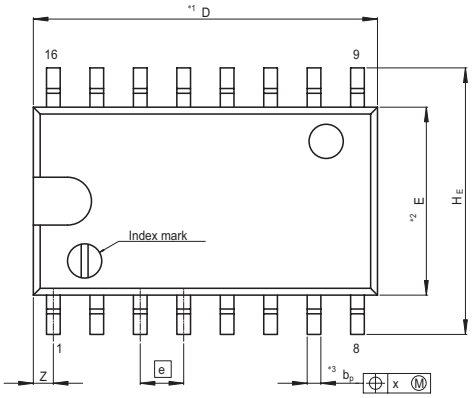


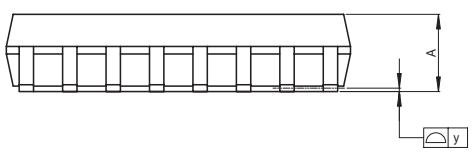


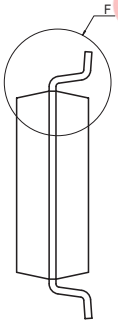
(Ni/Pd/Au plating)

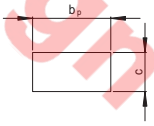
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e 1	——	7.62	——
D	——	19.2	20.32
E	——	6.3	7.4
A	——	——	5.06
A 1	0.51	——	——
b p	0.40	0.48	0.56
b 3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	1.12
L	2.54	——	——

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g



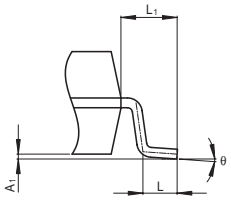






Terminal cross section
(Ni/Pd/Au plating)

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	10.06	10.5
E	——	5.50	——
A 2	——	——	——
A 1	0.00	0.10	0.20
A	——	——	2.20
b p	0.34	0.40	0.46
b 1	——	——	——
c	0.15	0.20	0.25
c 1	——	——	——
θ	0°	——	8°
H E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.80
L	0.50	0.70	0.90
L 1	——	1.15	——

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

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