To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74LV244A

Octal Buffers / Drivers with 3-state Outputs

REJ03D0328–0300Z
(Previous ADE-205-246A (Z))
Rev.3.00
Jun. 24, 2004

Description

The HD74LV244A has eight line drivers with three-state outputs in a 20-pin package. Four non-inverters are included in one circuit. Each circuit can be independently controlled by the enable signal $1\overline{OE}$ or $2\overline{OE}$, which enables outputs when receiving a low-level signal. Low-voltage operation is suitable for battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- V_{CC} = 2.0 V to 5.5 V operation
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- All outputs V_O (Max.) = 5.5 V (@V_{CC} = 0 V)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.3 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Output current ±8 mA (@V_{CC} = 3.0 V to 3.6 V), ±16 mA (@V_{CC} = 4.5 V to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV244AFPEL	SOP–20 pin (JEITA)	FP–20DAV	FP	EL (2,000 pcs/reel)
HD74LV244ARPEL	SOP–20 pin (JEDEC)	FP–20DBV	RP	EL (1,000 pcs/reel)
HD74LV244ATELL	TSSOP–20 pin	TTP–20DAV	T	ELL (2,000 pcs/reel)

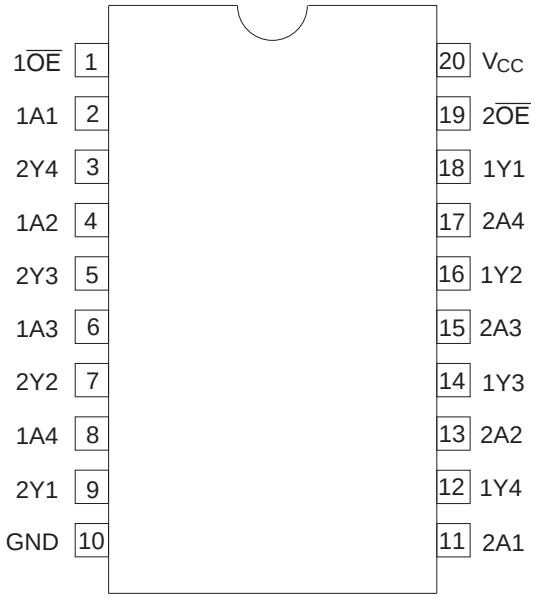
Note: Please consult the sales office for the above package availability.

Function Table

Inputs		
$\overline{OE}$	A	Output Y
L	H	H
L	L	L
H	X	Z

Note: H: High level
L: Low level
X: Immaterial
Z: High impedance

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	–0.5 to 7.0	V	
Input voltage range*[1]	V_I	–0.5 to 7.0	V	
Output voltage range*[1, *2]	V_O	–0.5 to V_{CC} + 0.5	V	Output: H or L
		–0.5 to 7.0		V_{CC}: OFF or Output: Z
Input clamp current	I_{IK}	–20	mA	V_I < 0
Output clamp current	I_{OK}	±50	mA	V_O < 0 or V_O > V_{CC}
Continuous output current	I_O	±35	mA	V_O = 0 to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±70	mA	
Maximum power dissipation at Ta = 25°C (in still air)*[3]	P_T	835	mW	SOP
		757		TSSOP
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not be individually be exceeded, and furthermore, no two of which may be realized at the same time.

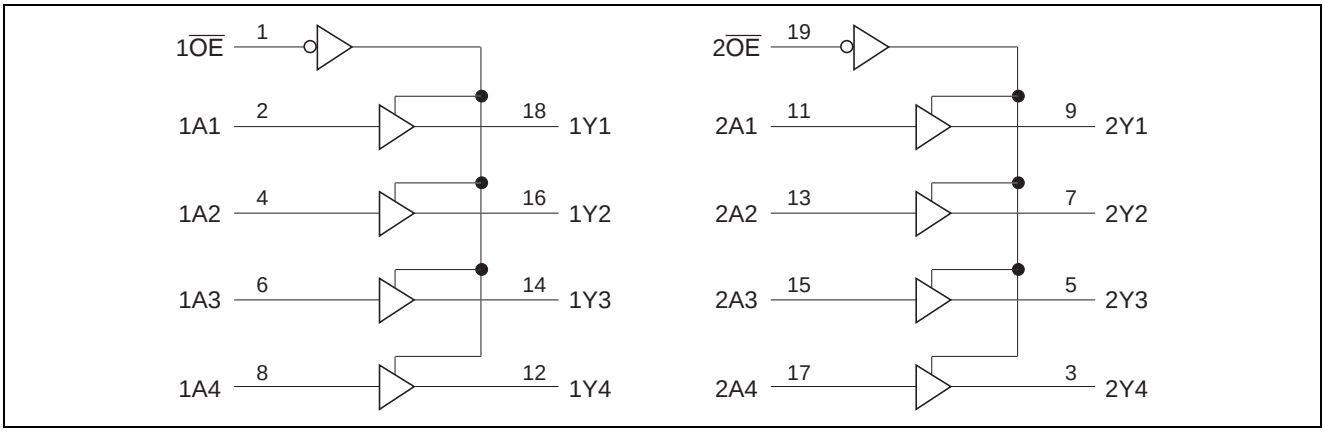
1. The input and output voltage ratings may be exceeded even if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The data above are measured by ΔV_{BE} method mounting on glass epoxy board (40 × 40 × 1.6 mm) with 10% of wiring density.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
		0	5.5		High impedance state
Output current	I_{OH}	—	–50	μA	V_{CC} = 2.0 V
		—	–2	mA	V_{CC} = 2.3 to 2.7 V
		—	–8		V_{CC} = 3.0 to 3.6 V
		—	–16		V_{CC} = 4.5 to 5.5 V
	I_{OL}	—	50	μA	V_{CC} = 2.0 V
		—	2	mA	V_{CC} = 2.3 to 2.7 V
		—	8		V_{CC} = 3.0 to 3.6 V
		—	16		V_{CC} = 4.5 to 5.5 V
Input transition rise or fall rate	Δt /Δv	0	200	ns/V	V_{CC} = 2.3 to 2.7 V
		0	100		V_{CC} = 3.0 to 3.6 V
		0	20		V_{CC} = 4.5 to 5.5 V
Operating free-air temperature	Ta	–40	85	°C	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



DC Electrical Characteristics

Ta = –40 to 85°C

Item	Symbol	V_{CC} (V)	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	$V_{CC} \times 0.7$	—	—		
		3.0 to 3.6	$V_{CC} \times 0.7$	—	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—	—		
	V_{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	$V_{CC} \times 0.3$		
		3.0 to 3.6	—	—	$V_{CC} \times 0.3$		
		4.5 to 5.5	—	—	$V_{CC} \times 0.3$		
Output voltage	V_{OH}	Min to Max	V_{CC} – 0.1	—	—	V	I_{OH} = –50 µA
		2.3	2.0	—	—		I_{OH} = –2 mA
		3.0	2.48	—	—		I_{OH} = –8 mA
		4.5	3.8	—	—		I_{OH} = –16 mA
	V_{OL}	Min to Max	—	—	0.1		I_{OL} = 50 µA
		2.3	—	—	0.4		I_{OL} = 2 mA
		3.0	—	—	0.44		I_{OL} = 8 mA
		4.5	—	—	0.55		I_{OL} = 16 mA
Input current	I_{IN}	0 to 5.5	—	—	±1	µA	V_{IN} = 5.5 V or GND
Off-state output current	I_{OZ}	5.5	—	—	±5	µA	V_O = V_{CC} or GND
Quiescent supply current	I_{CC}	5.5	—	—	20	µA	V_{IN} = V_{CC} or GND, I_O = 0
Output leakage current	I_{OFF}	0	—	—	5	µA	V_I or V_O = 0 V to 5.5 V
Input capacitance	C_{IN}	3.3	—	2.3	—	pF	V_I = V_{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

V_{CC} = 2.5 ± 0.2 V

Item	Symbol	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	—	7.5	12.5	1.0	15.0	ns	C_L = 15 pF	A	Y
	t_{PHL}	—	9.5	15.3	1.0	18.0		C_L = 50 pF		
Enable time	t_{ZH}	—	8.9	14.6	1.0	17.0	ns	C_L = 15 pF	$\overline{OE}$	Y
	t_{ZL}	—	10.8	17.8	1.0	21.0		C_L = 50 pF		
Disable time	t_{HZ}	—	9.1	14.1	1.0	16.0	ns	C_L = 15 pF	$\overline{OE}$	Y
	t_{LZ}	—	13.4	19.2	1.0	21.0		C_L = 50 pF		

V_{CC} = 3.3 ± 0.3 V

Item	Symbol	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	—	5.4	8.4	1.0	10.0	ns	C_L = 15 pF	A	Y
	t_{PHL}	—	6.8	11.9	1.0	13.5		C_L = 50 pF		
Enable time	t_{ZH}	—	6.3	10.6	1.0	12.5	ns	C_L = 15 pF	$\overline{OE}$	Y
	t_{ZL}	—	7.8	14.1	1.0	16.0		C_L = 50 pF		
Disable time	t_{HZ}	—	7.6	11.7	1.0	13.0	ns	C_L = 15 pF	$\overline{OE}$	Y
	t_{LZ}	—	11.0	16.0	1.0	18.0		C_L = 50 pF		

V_{CC} = 5.0 ± 0.5 V

Item	Symbol	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	—	3.9	5.5	1.0	6.5	ns	C_L = 15 pF	A	Y
	t_{PHL}	—	4.9	7.5	1.0	8.5		C_L = 50 pF		
Enable time	t_{ZH}	—	4.5	7.3	1.0	8.5	ns	C_L = 15 pF	$\overline{OE}$	Y
	t_{ZL}	—	5.6	9.3	1.0	10.5		C_L = 50 pF		
Disable time	t_{HZ}	—	6.5	12.2	1.0	13.5	ns	C_L = 15 pF	$\overline{OE}$	Y
	t_{LZ}	—	8.8	14.2	1.0	15.5		C_L = 50 pF		

Output-skew characteristics

C_L = 50 pF

Item	Symbol	V_{CC} (V)	Ta = 25°C		Ta = –40 to 85°C		Unit
			Min	Max	Min	Max	
Output skew	$t_{sk\ (O)}$	2.3 to 2.7	—	2.0	—	2.0	ns
		3.0 to 3.6	—	1.5	—	1.5	
		4.5 to 5.5	—	1.0	—	1.0	

Note: Skew between any outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

Operating Characteristics

C_L = 50 pF

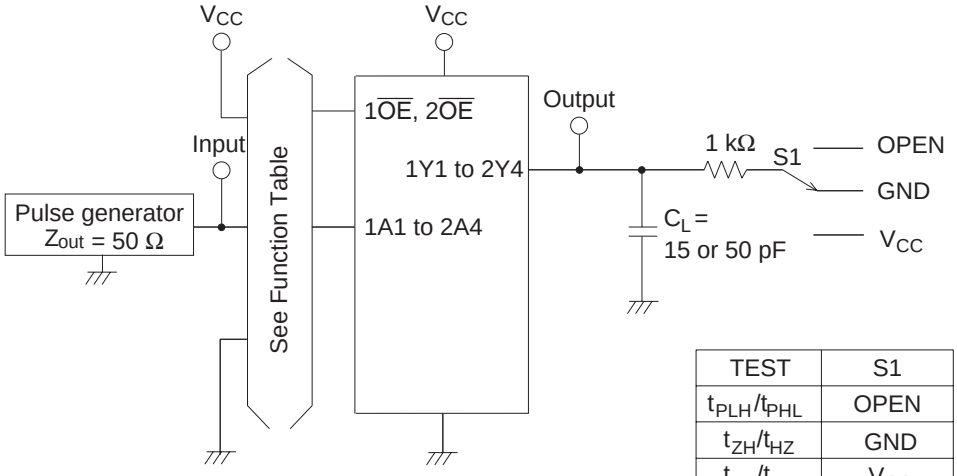
Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Unit	Test Conditions
Power dissipation capacitance	C_{PD}	3.3	—	14.0	—	pF	f = 10 MHz
		5.0	—	16.0	—		

Noise Characteristics

C_L = 50 pF

Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Unit	Test Conditions
Quiet output, maximum dynamic V_{OL}	$V_{OL (P)}$	3.3	—	0.6	0.8	V	
Quiet output, minimum dynamic V_{OL}	$V_{OL (V)}$	3.3	—	–0.5	–0.8	V	
Quiet output, minimum dynamic V_{OH}	$V_{OH (V)}$	3.3	—	2.9	—	V	
High-level dynamic input voltage	$V_{IH (D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL (D)}$	3.3	—	—	0.99	V	

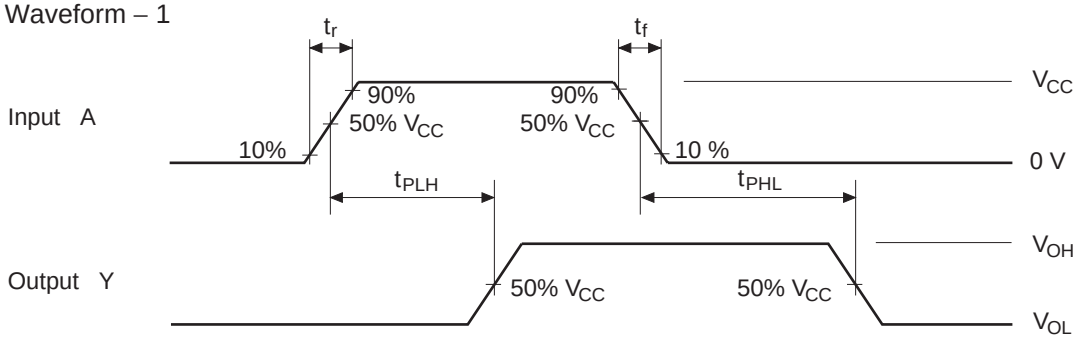
Test Circuit



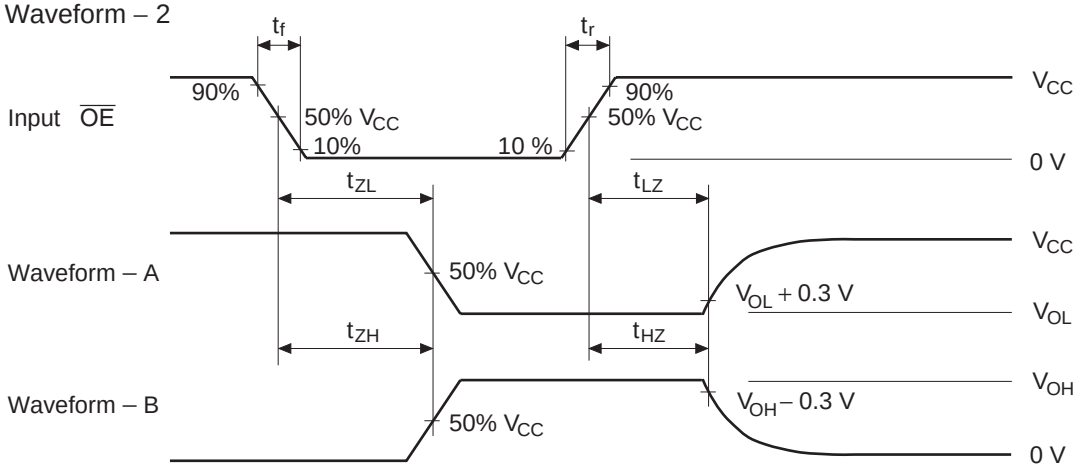
TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{ZH}/t_{HZ}	GND
t_{ZL}/t_{LZ}	V_{CC}

Note: C_L includes the probe and jig capacitance.

• Waveform – 1



• Waveform – 2

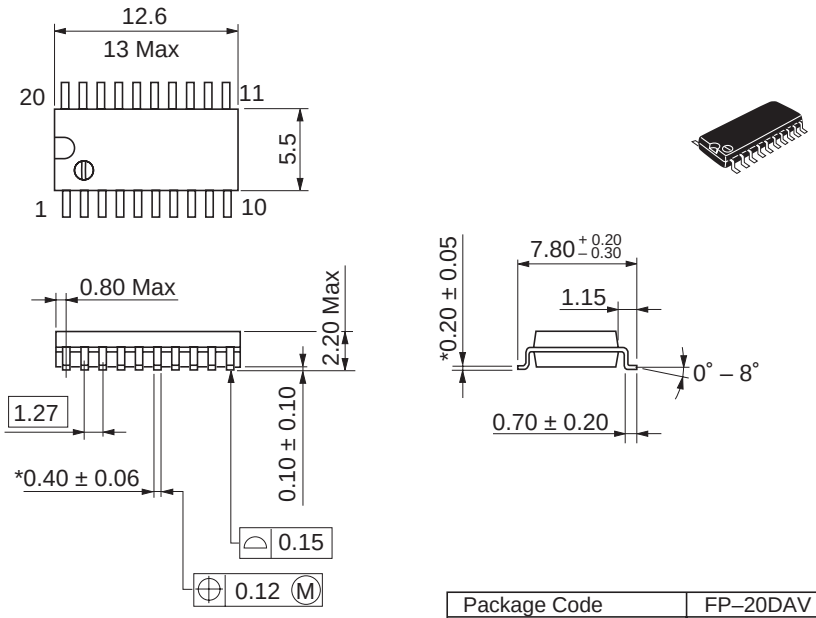


Notes: 1. Input waveform: PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns
2. Waveform–A is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform–B is for an output with internal conditions such that the output is high except when disabled by the output control.
4. The output are measured one at a time with one transition per measurement..

Package Dimensions

As of January, 2002

Unit: mm

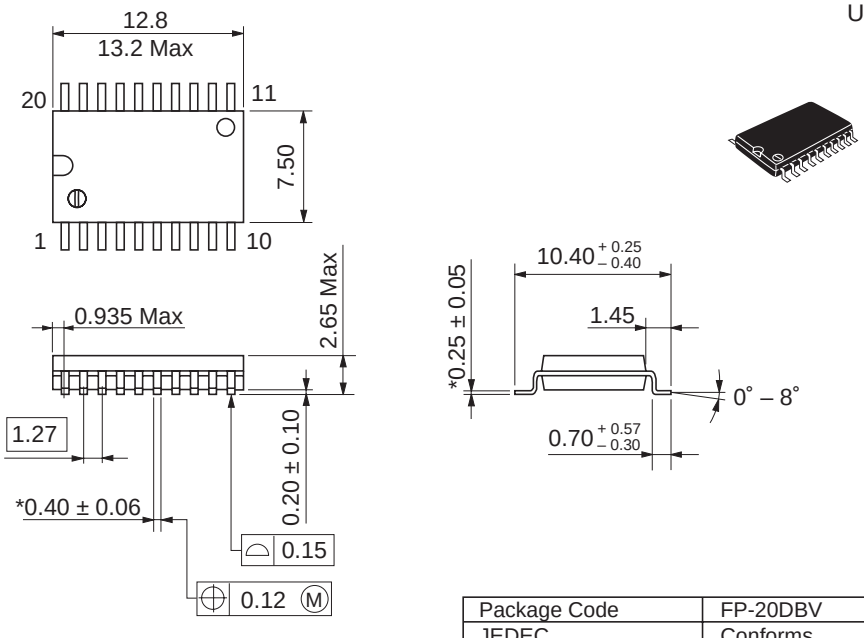


*Pd plating

Package Code	FP–20DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g

As of January, 2003

Unit: mm

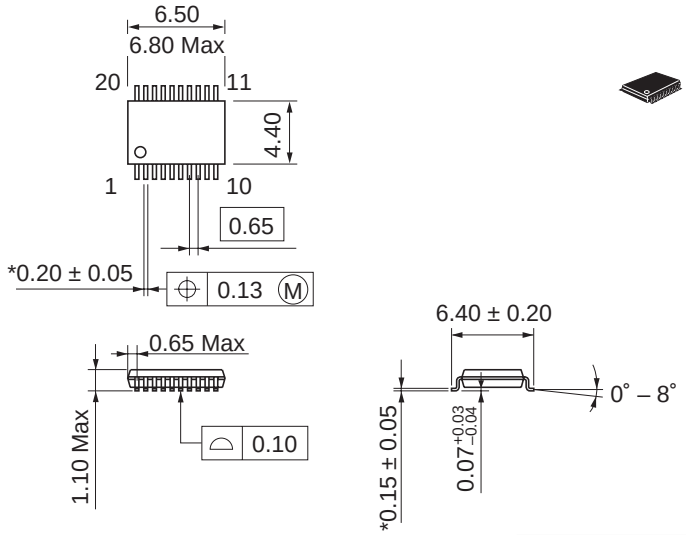


*Ni/Pd/Au plating

Package Code	FP-20DBV
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.52 g

As of January, 2002

Unit: mm



Package Code	TTP–20DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.07 g

*Pd plating

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