HI-5051/883

Dual SPDT CMOS Analog Switch

FN8289
Rev.0.00
May 3, 2012

This CMOS analog switch offers low resistance switching performance for analog voltages up to the supply rails and for signal currents up to 70mA. “ON” resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 25Ω.

The HI-5051/883 provides break-before-make switching and is TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at +25°C). The HI-5051/883 switch also features very low power operation (1.5mW at +25°C). The HI-5051/883 is available in a 20 Ld CLCC package and operates over the -55°C to +125°C temperature range.

Features

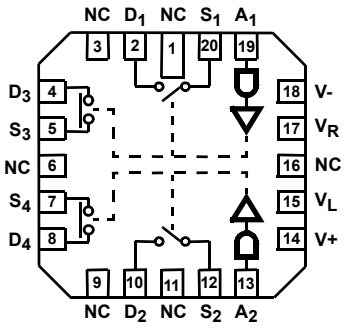
- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Wide Analog Signal Range . . . . . ±15V
- Low “ON” Resistance . . . . . 25Ω (Typ), 50Ω (Max)
- High Current Capability . . . . . 70mA (Max)
- Break-Before-Make Switching
  - Turn-On Time. . . . . .370ns (Typ), 800ns (Max)
  - Turn-Off Time . . . . . 280ns (Typ), 400ns (Max)
- No Latch-Up
- Input MOS Gates are Protected from Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

Pin Configuration

HI-5051/883
20 LD CLCC
TOP VIEW
LOGIC “0” INPUT



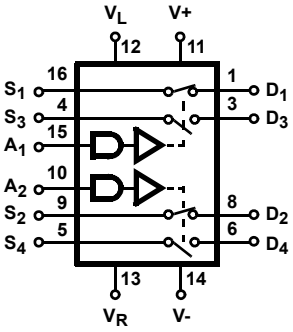
NOTE: Unused pins may be internally connected. Ground all unused pins.

Ordering Information

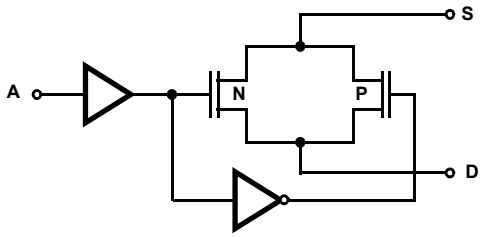
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI4-5051/883	HI4-5051 883	-55 to +125	20 Ld CLCC	J20.A

Functional Diagram

LOGIC “1” INPUT



TYPICAL SWITCH



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output, respectively. They may be interchanged without affecting performance.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) . . . . . $\pm$18V
V_R to Ground . . . . . $-V_{SUPPLY}$
V_L to Ground . . . . . $+V_{SUPPLY}$
Digital and Analog Input Voltage (V_A, V_S, V_D) . . . . . $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Peak Current (Source to Drain)
(Pulse at 1ms, 10% Duty Cycle Max) 70mA
Continuous Current (Any Pin) 20mA
ESD Rating . . . . . <2000V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CLCC Package	80	20

Package Power Dissipation at +75°C
CLCC Package 1.0W
Package Power Dissipation Derating Factor above +75°C
CLCC Package . . . . . 12.5mW/°C
Junction Temperature . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C

Recommended Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage . . . . . $\pm$15V
Logic Supply Voltage (V_L) . . . . . +5.0V
Logic Reference Voltage (V_R) 0.0V
Analog Input Voltage (V_S) . . . . . $\pm V_{SUPPLY}$
Address Low Level (V_{AL}) . . . . . 0V to 0.8V
Address High Level (V_{AH}) . . . . . 2.4V to +5.0V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: Supply Voltage = $\pm$15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, unused pins are grounded, unless otherwise specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Switch "ON" Resistance	R_{DS2}	V_D = -10V, I_S = 10mA S1/S2/S3/S4	1	+25	-	45	Ω
			2, 3	-55 to +125	-	50	Ω
		V_D = 10V, I_S = -10mA S1/S2/S3/S4	1	+25	-	45	Ω
			2, 3	-55 to +125	-	50	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = -10V, V_D = 10V S1/S2/S3/S4	1	+25	-1	1	nA
			2, 3	-55 to +125	-100	100	nA
		V_S = 10V, V_D = -10V S1/S2/S3/S4	1	+25	-1	1	nA
			2, 3	-55 to +125	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -10V, V_S = 10V S1/S2/S3/S4	1	+25	-1	1	nA
			2, 3	-55 to +125	-100	100	nA
		V_D = 10V, V_S = -10V S1/S2/S3/S4	1	+25	-1	1	nA
			2, 3	-55 to +125	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = 10V S1/S2/S3/S4	1	+25	-2	2	nA
			2, 3	-55 to +125	-200	200	nA
		V_D = V_S = -10V S1/S2/S3/S4	1	+25	-2	2	nA
			2, 3	-55 to +125	-200	200	nA
Low Level Address Current	I_{AL}	V_A = 0V A_1, A_2	1	+25	-1	1	µA
			2, 3	-55 to +125	-10	1	µA
High Level Address Current	I_{AH}	V_A = 2.4V, 5V A_1, A_2	1	+25	-1	1	µA
			2, 3	-55 to +125	-1	10	µA
Positive Supply Current	$+I_{CC}$	V_A = 0V, 5V A_1, A_2	1	+25	-	200	µA
			2, 3	-55 to +125	-	300	µA
Negative Supply Current	$-I_{CC}$	V_A = 0V, 5V A_1, A_2	1	+25	-200	-	µA
			2, 3	-55 to +125	-300	-	µA

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, unused pins are grounded, unless otherwise specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Logic Supply Current	$+I_L$	V_A = 0V, 5V	1	+25	-	200	µA
			2, 3	-55 to +125	-	300	µA
Reference Supply Current	$+I_R$	V_A = 0V, 5V	1	+25	-200	-	µA
			2, 3	-55 to +125	-300	-	µA

TABLE 2. A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = +5.0V, V_{AL} = +0.0V, unused pins are grounded, unless otherwise specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Turn "ON" Time	t_{ON}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55	-	450	ns
			9	+25	-	500	ns
			10	+125	-	800	ns
Turn "OFF" Time	t_{OFF}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55	-	350	ns
			9	+25	-	450	ns
			10	+125	-	600	ns

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (NOTE 1)

Device Characterized at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 4.0V, V_{AL} = 0.8V, unused pins are grounded, unless otherwise specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE (°C)	MIN	MAX	UNITS
"ON" Resistance Match (Channel to Channel)	R_{ON2} Match	V_D = ±10V I_D = 10mA	1	+25	-	10	Ω
Address Capacitance	C_A	V_A = 0V, 5V	1	+25	-	45	pF
Switch Input Capacitance	$C_{S(OFF)}$	Switch Off: V_A = 0V	1	+25	-	60	pF
Switch Output Capacitance	$C_{D(OFF)}$	Switch Off: V_A = 0V	1	+25	-	60	pF
	$C_{D(ON)}$	Switch On: V_A = 5V	1	+25	-	60	pF
Drain to Source Capacitance	$C_{DS(OFF)}$	Switch Off: V_A = 0V	1	+25	-	10	pF
Off Isolation	V_{ISO}	V_S = $2V_{P-P}$ @ f = 100kHz, R_L = 100Ω	1	+25	-	60	dB
Crosstalk	V_{CT}	V_S = $2V_{P-P}$ @ f = 100kHz, R_L = 100Ω	1	+25	-	60	dB
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 0.01µF V_A = 0V to 4V @ f = 200kHz	1	+25	-	30	mV

NOTE:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (See Tables 1 and 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1 (Note 2), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

NOTE:

2. PDA applies to Subgroup 1 only.

Test Circuits

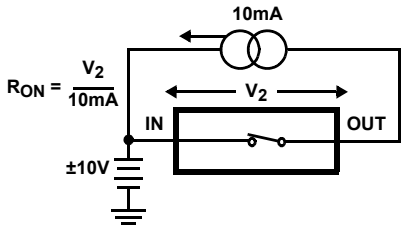


FIGURE 1. R_{DS}

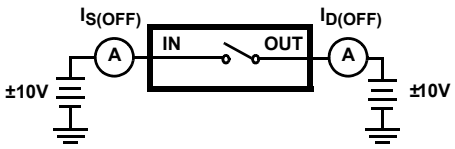


FIGURE 2. $I_{S(OFF)}$

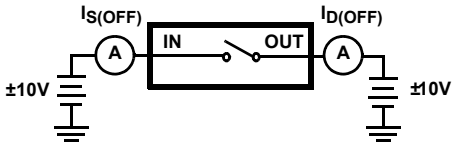


FIGURE 3. $I_{D(OFF)}$

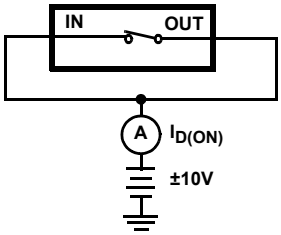


FIGURE 4. $I_{D(ON)}$

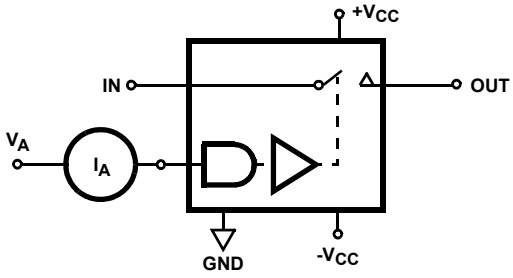


FIGURE 5. ADDRESS CURRENT

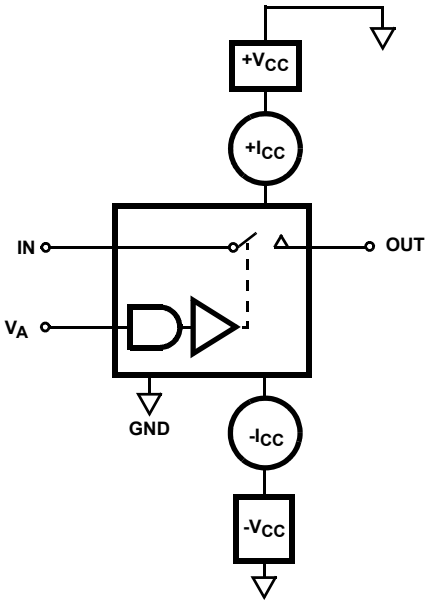


FIGURE 6. SUPPLY CURRENTS

Test Circuits (Continued)

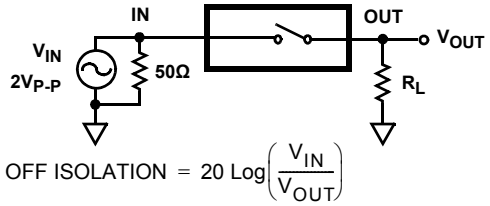
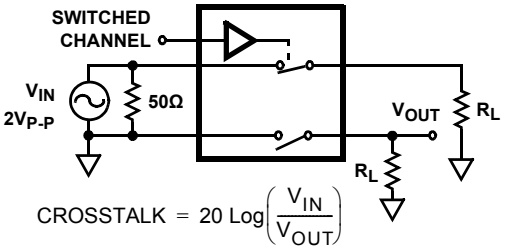
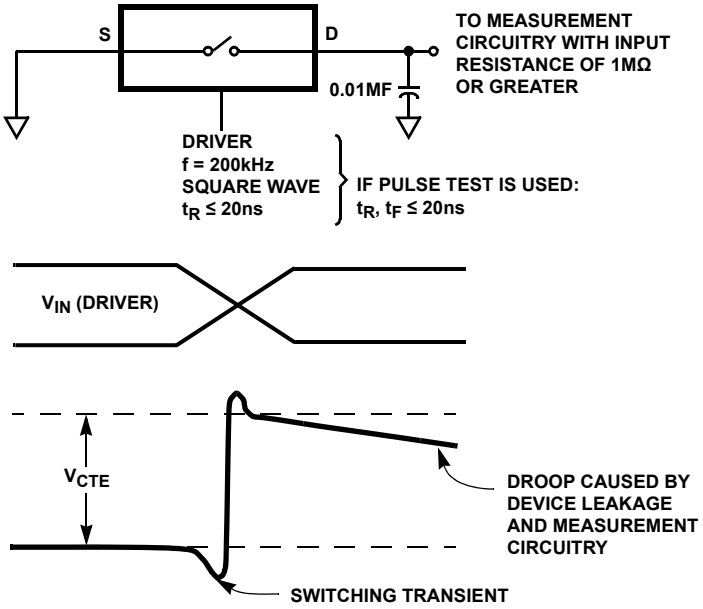


FIGURE 7. OFF ISOLATION



NOTE: Applies only to dual or double throw switches.

FIGURE 8. CROSSTALK



NOTE: V_{CTE} may be a positive or negative value.

FIGURE 9. CHARGE TRANSFER

Test Characteristics

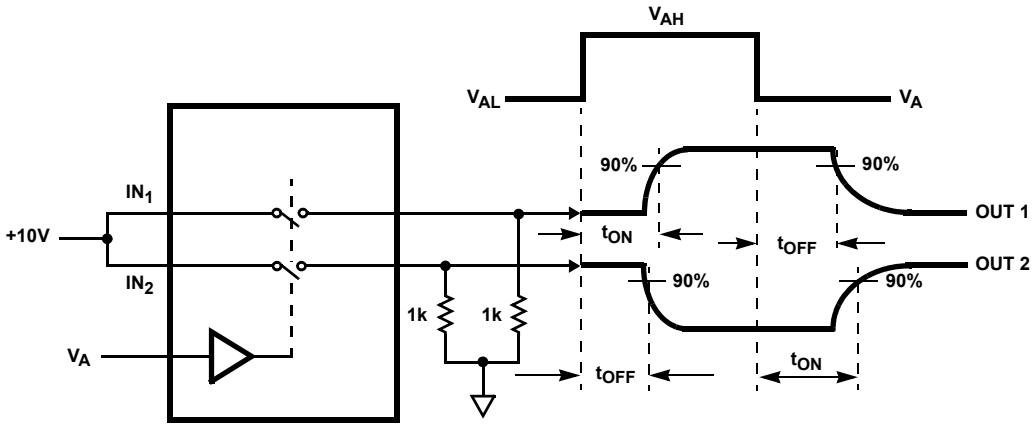


FIGURE 10. ON/OFF SWITCH TIME (t_{ON}, t_{OFF})

Test Characteristics (Continued)

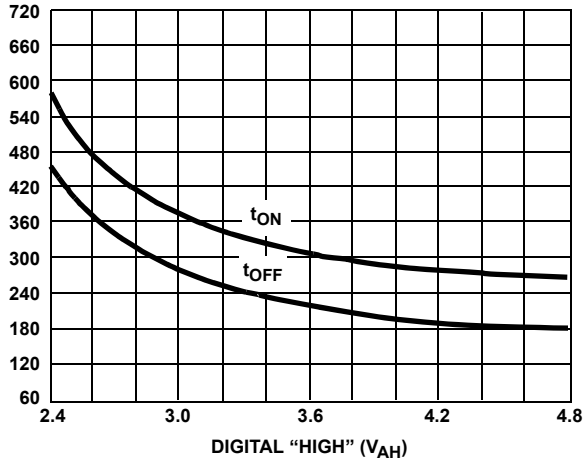


FIGURE 11. SWITCHING TIMES FOR DIGITAL TRANSITION

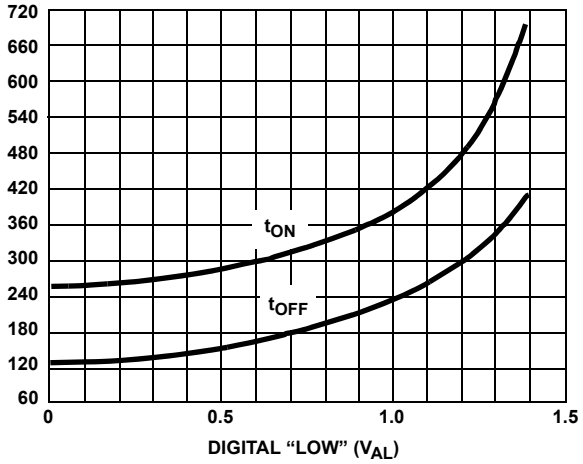
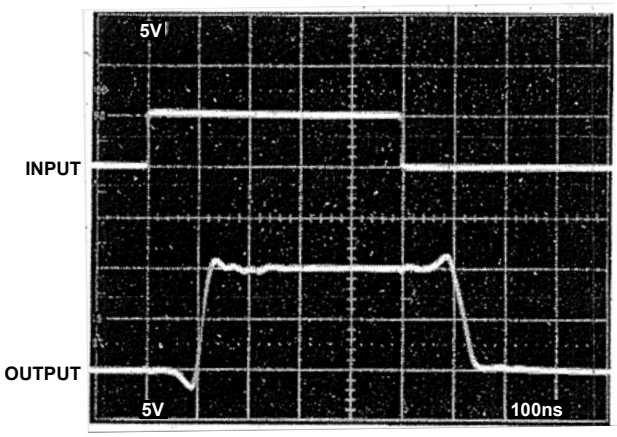


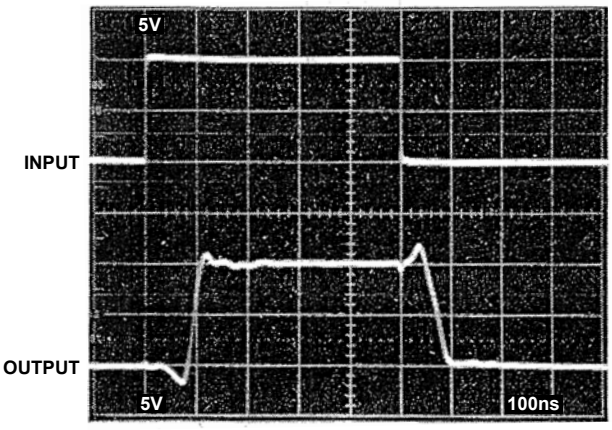
FIGURE 12. SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION

Test Waveforms



Vertical Scale: Input = 5V/Div, (TTL; V_{AH} = 5V, V_{AL} = 0V)
Output = 5V/Div
Horizontal Scale: 100ns/Div

FIGURE 13.

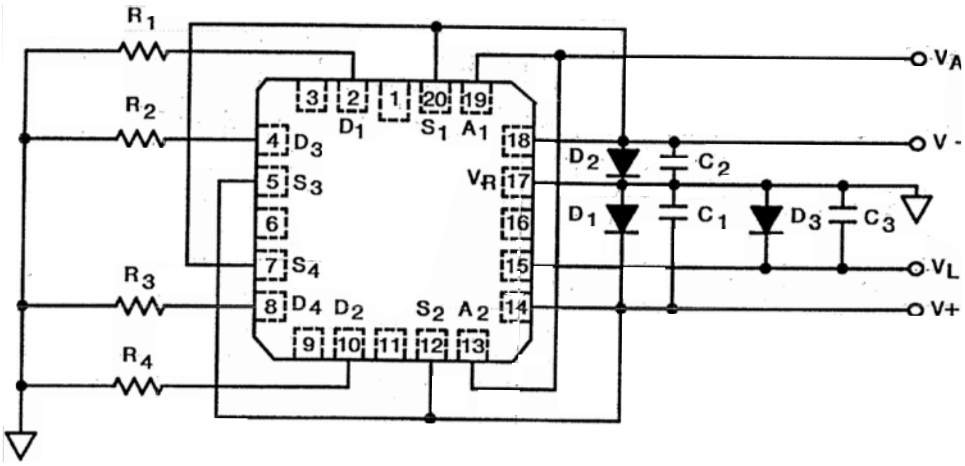


Vertical Scale: Input = 5V/Div, (CMOS; V_{AH} = 10V, V_{AL} = 0V)
Output = 5V/Div
Horizontal Scale: 100ns/Div

FIGURE 14.

Burn-In Circuit

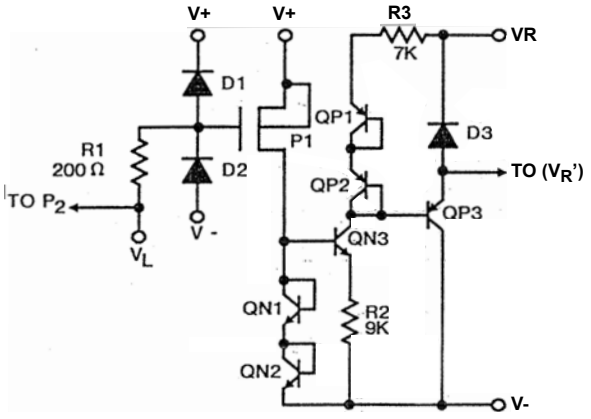
HI-5051/883 CERAMIC LCC



NOTES:

R_1 thru R_4 = 10kΩ, ±5%, 1/4W (Min)
C_1, C_2, C_3 = 0.01µF/Socket (Min) or 0.1µF/Row, (Min)
D_1, D_2, D_3 = 1N4002 or Equivalent/Board
V_L = 5.5V ±0.5V
$A_2 = A_2$ = 5.5V ±0.5V
|(V+) - (V-)| = 30V

Schematic Diagrams



NOTE: Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

FIGURE 15. TTL/CMOS REFERENCE CIRCUIT

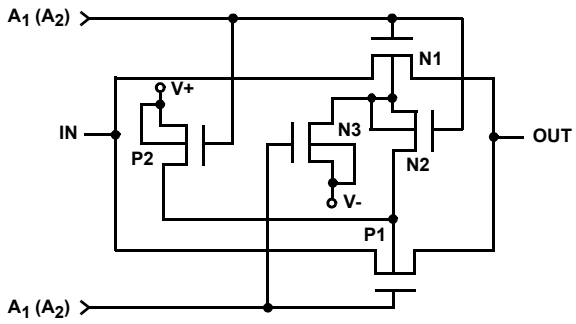
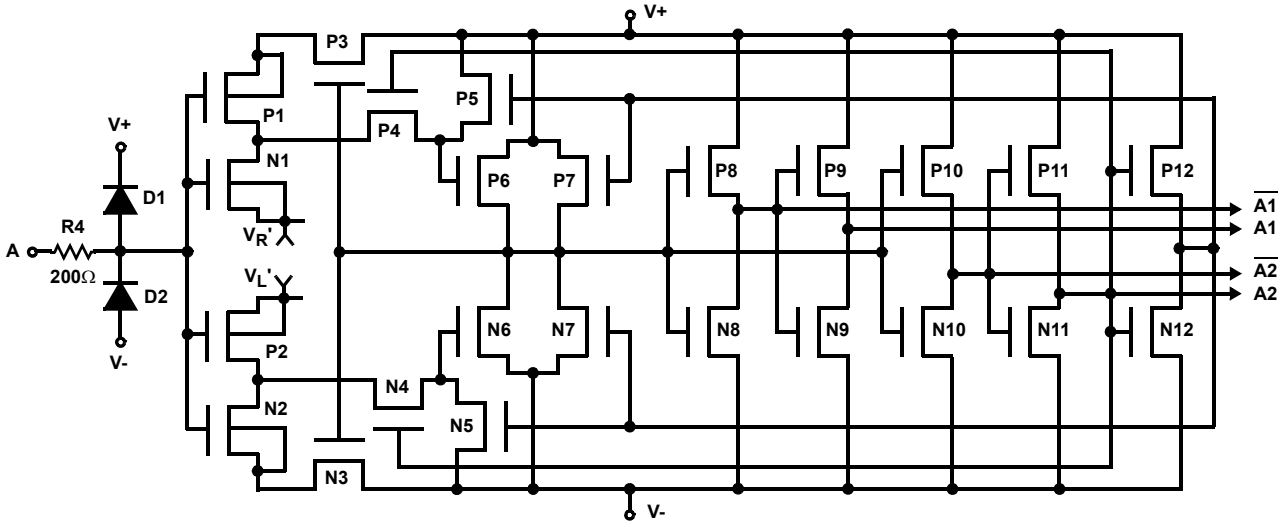


FIGURE 16. SWITCH CELL



NOTE: All N-Channel bodies to V-, all P-Channel bodies to V+ except as shown.

DIGITAL INPUT BUFFER AND LEVEL SHIFTER

Die Characteristics

DIE DIMENSIONS:

96mils x 81mils x 20mils
(2430µm x 2050µm x 508µm)

METALLIZATION:

Type: Aluminum
Thickness: 16kÅ ±2kÅ

GLASSIVATION:

Type: Nitride over Silox
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1kÅ

SUBSTRATE POTENTIAL (Powered-up): V-

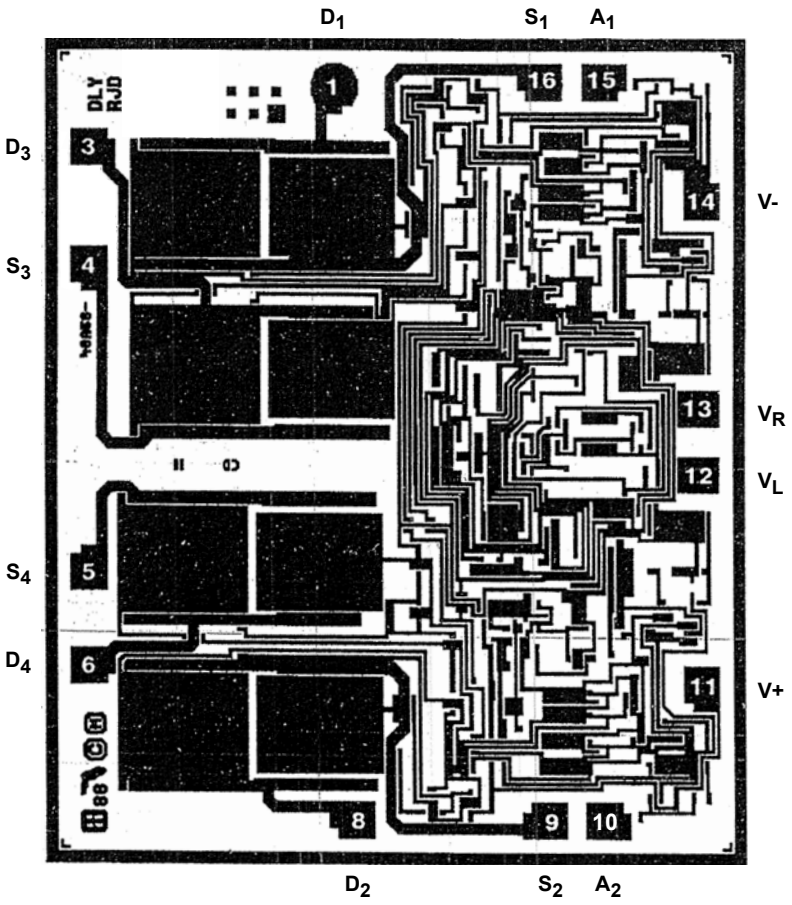
DEVICE COUNT: 82

WORST CASE CURRENT DENSITY:

1.0 x 10^5A/cm^2 at 20mA

Metallization Mask Layout

HI-5051/883



Design Information

The information contained in this section has been developed through characterization and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$

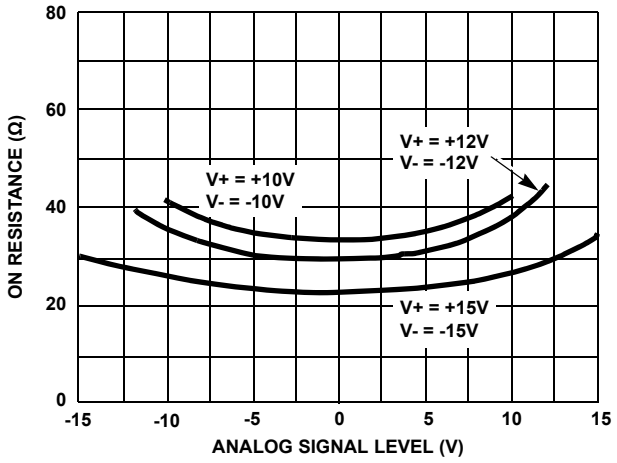


FIGURE 17. ON RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

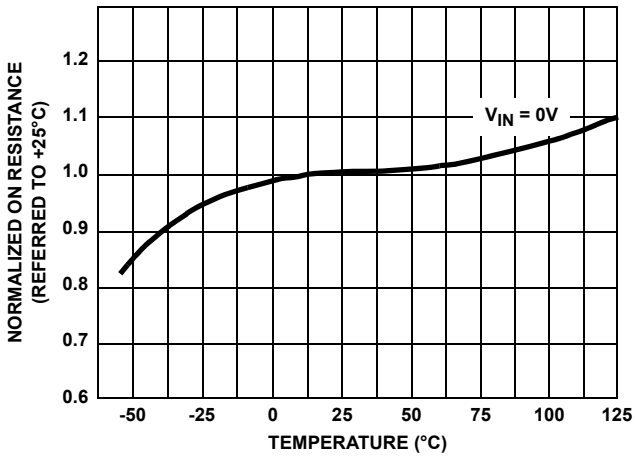


FIGURE 18. NORMALIZED ON RESISTANCE vs TEMPERATURE

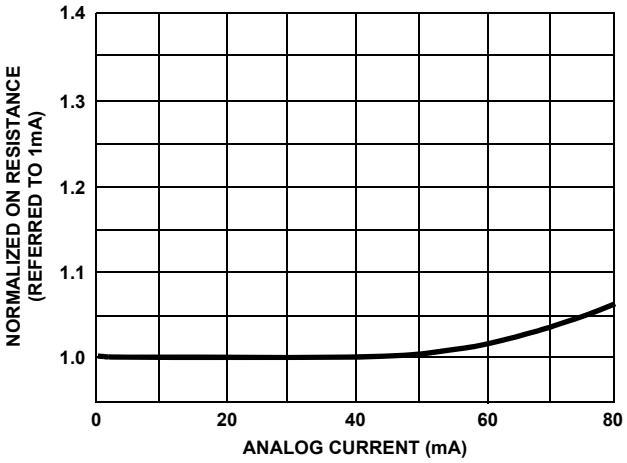


FIGURE 19. NORMALIZED ON RESISTANCE vs ANALOG CURRENT

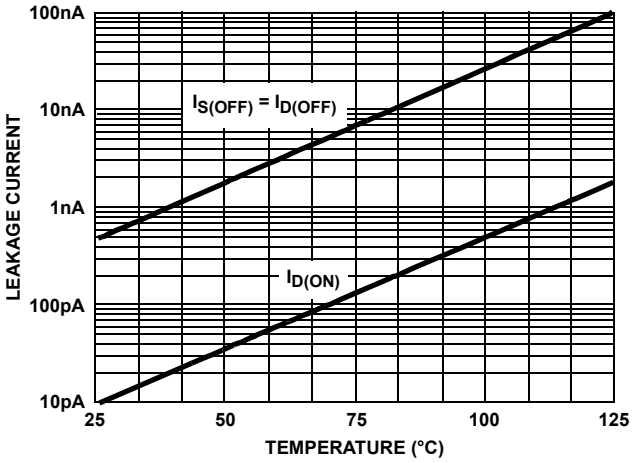


FIGURE 20. ON/OFF LEAKAGE CURRENTS vs TEMPERATURE

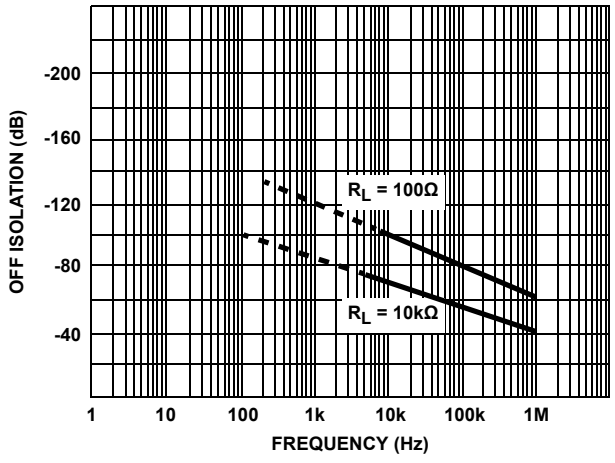


FIGURE 21. OFF ISOLATION vs FREQUENCY

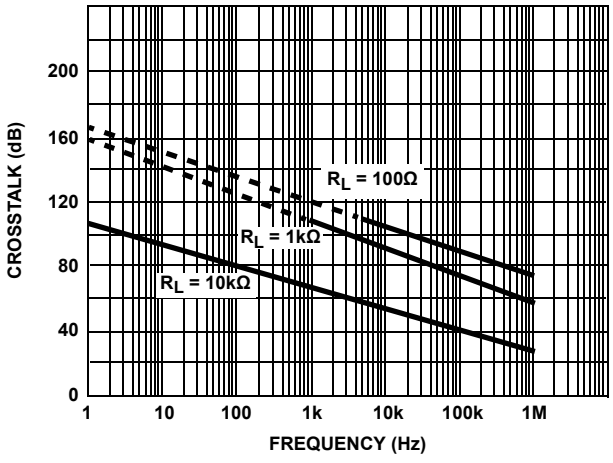


FIGURE 22. CROSSTALK vs FREQUENCY

Design Information

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Typical Performance Curves $T_A = +25°C, V_{SUPPLY} = \pm15V$ (Continued)

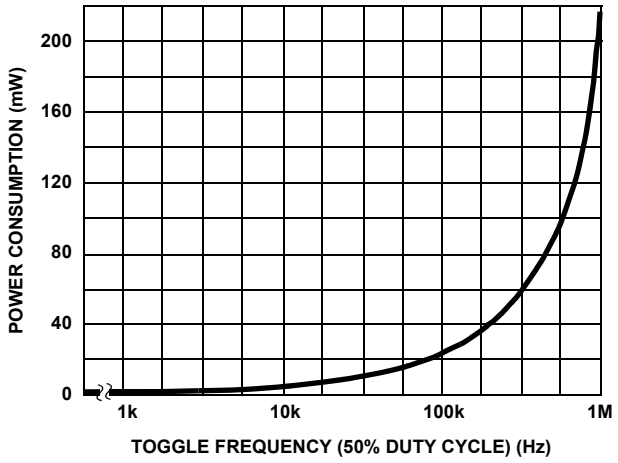
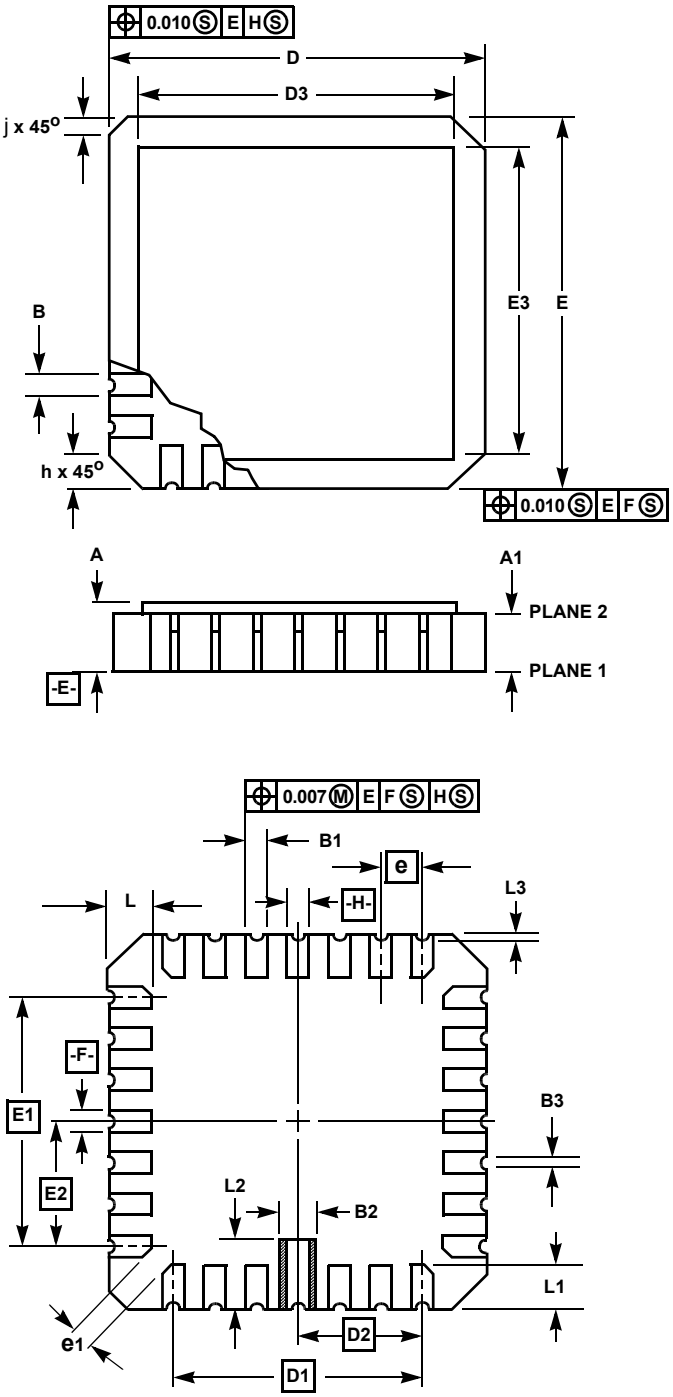


FIGURE 23. POWER CONSUMPTION vs FREQUENCY

Ceramic Leadless Chip Carrier Packages (CLCC)



J20.A **MIL-STD-1835 CQCC1-N20 (C-2)**
20 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

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NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol “N” is the maximum number of terminals. Symbols “ND” and “NE” are the number of terminals along the sides of length “D” and “E”, respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension “A” controls the overall package thickness. The maximum “A” dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.